A HYBRID POWER CONVERTER WITH ENHANCED SWITCHING RIPPLE CANCELLATION

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Abstract

As worldwide electricity demand increases, so does the requirement for effective power conversion combining increased efficiency with minimal harmonic pollution at the lowest financial cost. For medium to high voltage grid-connected applications, multilevel converter topologies enabled the use of lower rated and more efficient self-commutated switches. Due to practical limitations, efficient operation of converters with a low number of levels is restricted to low switching frequencies which in turn becomes a limiting factor for the design of smaller passive filters that are required to limit the associated switching harmonics injected in the AC grid.

This thesis investigates the use of a novel hybrid converter concept aimed at medium-voltage (MV) grid-connected applications. Hybrid converters consist of a main inverter processing the bulk of the power with poor waveform performance and a fast and versatile auxiliary inverter to correct the distortion. In this case, the main converter is a medium-voltage three-level Neutral Point Clamped (NPC) inverter and the auxiliary inverter is a low-voltage and low-current rated Current Source Inverter (CSI), fitted with a series capacitor that is used to minimise the CSI voltage stress. As a result the added installed power by the auxiliary CSI switches can remain at very low levels (theoretically <4%), resulting in a minimal added cost, whilst offering a substantial harmonic improvement to the main VSI. Furthermore the auxiliary converter can be retro-fitted to an existing MV inverter installation to improve the current harmonic quality as required by new grid standards, at a minimal cost.

The performance of the proposed hybrid solution is evaluated through simulation at 3.3 kV MV level under various grid interconnection scenarios. The feasibility of the concept is validated experimentally, scaled to 415V grid voltage level (a more realistic level for a laboratory demonstrator) while operating under more challenging conditions such as switching ripple levels of 50% peak relative to the fundamental peak, showing that the added installed power can be as low as 7% with very high output grid current quality under all grid scenarios considered.

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Nomenclature

Symbol	Meaning
§	Section
3L-NPC	Three-Level Neutral Point Clamped
AC	Alternating Current
ADC	Analogue To Digital Converter
ANPC	Active-Neutral-Point-Clamped
APF	Active Power Filter
CHB	Isolated/Cascaded H-Bridge
CSI	Current Source Inverter
DC	Direct Current
DDSRF	Double Decoupled Synchronous Reference Frame
DFT	Discrete Fourier Transformation
DPF	Displacement Power Factor
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMIF	External Memory Interface
FC	Flying Capacitor
FFT	Fourier Transform
FPGA	Field-Programmable Gate Array
GaN	Gallium Nitride
GS/s	Giga-Samples
GTO	Gate Turn-Off Thyristor
GUI	Graphical User Interface

HAPF	Hybrid Active Power Filters
HPI	Host-Port Interface
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
kS/s	Kilo-Samples
LCC	Line Commutated Converter
LPF	Low Pass Filter
MA	Moving Average
MMC	Modular Multilevel Converter
MV	Medium Voltage
NPC	Neutral Point Clamped
NTC	Temperature Coefficient Thermistor
PCB	Printed Circuit Board
PCC	Point Of Common Coupling
PEMC	University Of Nottingham Power Electronics, Machines And Control Group
PI	Proportional Integral
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
RB-IGBT	Reverse Blocking Insulated-Gate Bipolar Transistor
SCR	Short Circuit Ratio
SHE-PWM	Selective Harmonic Elimination Pulse Width Modulation
SiC	Silicon Carbide

TCLC-HAPF	Thyristor Controlled LC-Coupling Hybrid Active Power Filter
TCR	Thyristor Controlled Reactor
THD	Total Harmonic Distortion
TRL	Technology Readiness Level
TTL	Transistor–Transistor Logic
VSI	Voltage Source Inverter

List of passive component names

Name	Unit	Description
C_{clamp}	F	Clamp circuit dc side capacitance
C_{dc}	F	VSI dc side capacitance
C_{p}	F	CSI output parallel capacitor
C_{s}	F	Series capacitor
L_{1}	H	VSI line side inductor
L_{2}	H	LCL output side inductance
L_{dc}	H	CSI dc side inductance
L_{f}	H	Filter inductance
L_{g}	H	Grid inductance
R_{clamp}	Ω	Clamp dc resistance
R_{dc}	Ω	VSI dc side resistance
R_{f}	Ω	Damping resistance
$R_{pd/sd/cs/fo}$	Ω	Damping resistor

Name	Unit	Description
f_{sw}^{CSI}	Hz	CSI switching frequency
f_{sw}^{VSI}	Hz	VSI switching frequency
f_0	Hz	Fundamental frequency
G	-	Gain
I_c	A	Series capacitor current
I_c max	A	Maximum CSI fundamental component magnitude
I_{c_d} lim	A	CSI active current component limit
I_{L1}	A	VSI current through inductor L_1, equivalent to I_s
Ic_d	A	Active current component
Ic_q	A	Reactive current component
I_{csi}	A	CSI PWM current
I_{dc}	A	CSI dc current
I_{dc} ABC	A	Three phase grid currents
I_g	A	Grid current
I_{grid}	A	Grid current
$I_{ref_}$ABC	A	CSI abc reference waveform
I_{ripple}	A	Extracted current ripple
I_s	A	Main VSI AC side current
I_s abc	A	VSI three phase currents
I_s dq	A	VSI dq current components
I_{s_d}	V	VSI active current component
I_{s_d}*	V	VSI active current component reference
$\widehat{I_{CSI}}$	A	Peak CSI current stress

$\widehat{I_{VSI}}$	A	Peak VSI current stress
ΔI_{max}	A	Maximum current ripple
K	-	Coefficient of fundamental voltage drop on CSI
Ki	-	Integral gain of PI controller
Kp	-	Proportional gain of PI controller
M_abc	-	Modulating wave
Nsw_{CSI}	-	Number of CSI semiconductor switches
Nsw_{VSI}	-	Number of VSI semiconductor switches
Q	VAr	Reactive power
S	VA	Apparent power
t	S	Time
V_c	V	Series capacitor voltage
$V_{c\&Lf}$	V	Series capacitor voltage across the series capacitor and the CSI AC filter inductance
V_{ca}, V_{ab}, V_{bc}	V	Line-line voltage
V_{clamp}	V	Clamp DC voltage
V_{csi}	V	CSI voltage
V_{dc}	V	VSI dc voltage
V_g	V	Grid voltage peak line to neutral grid voltage
V_{grid}	V	Grid voltage
$V_{ph\_}ABC$	V	Phase –neutral voltages for phases ABC
$\widehat{V}_{c_d}$	V	Series capacitor voltage active component
$\widehat{V}_{c_q}$	V	Series capacitor voltage reactive component
$\widehat{V}_{csi_d}$	V	CSI voltage active component
$\widehat{V}_{csi_q}$	V	CSI voltage reactive component

$\widehat{V}_g^{ln}$	V	Grid phase voltage peak
$\widehat{V_{CSI}}$	V	Peak CSI voltage stress
$\widehat{V_{VSI}}$	V	Peak VSI voltage stress
X_c	Ω	Series Capacitor Impedance
τ	S	Time constant
ω_r	rads	Resonant frequency

CHAPTER 1. Introduction

1.1. Motivation for Project

Mitigating the switching harmonics generated by medium to high voltage power electronic converters has proven to be challenging due to the low switching frequency required to maintain high efficiency and the compromise between simple but bulky or smaller complicated filter designs [1]. The uptake of multilevel converters at medium-voltage (MV) levels, which have been theoretically proposed as a solution to reducing filtering requirements, has been also been restricted to a low number of voltage levels by the preference of reduced complexity and also cost. This thesis is aimed at investigating a low cost solution to improve the harmonic quality of the waveforms associated with such a converter.

1.2. Overview

Processing electrical energy efficiently via power electronic converter technology delivered to/from medium and high voltage grids is predicted to increase in usage in the future [2]. This trend is driven by the need to interface large offshore wind farms [3] to mainland grids or to interconnect distribution systems to HVDC transmission systems of the future.

The radical evolution of power semiconductors in the past decades has been an enabling technology which has elevated the technological capabilities with the introduction of self-commutated devices like the GTO, IGCT and IGBT and the introduction of new solutions for the advancement of AC/DC conversion [4]. Before new solutions can be assimilated and utilised in industry however, they must first undergo thorough investigation to meet the pragmatic requirements of maintaining high efficiency and reliability, low installation and running cost, reduced size and weight as well as compliance with grid regulations.

In the field of power electronics, different topological and control approaches have been proposed to utilise the capabilities of each new generation of semiconductor technology. The venture to improve beyond the prevailing constraint between the maximum voltage/current ratings of switches whilst also decreasing the reliance on passive elements is still enduring.

In order to go beyond the rated capabilities of the semiconductors used, the first generation of high voltage power converters favoured standard two-level topologies with series connection of multiple switches due to a simple implementation and ability to achieve redundancy [5]. This however led to static and dynamic voltage sharing problems and poor output quality [6].

The first generation of multilevel converters, based on the Flying Capacitor (FC), Neutral Point Clamped (NPC) and isolated/cascaded H-bridge (CHB) have been proposed more than 20 years ago as a solution to the problems of two-level converters with series connected devices. For a large number of levels, the benefits of multilevel conversion are particularly advantageous to lower filtering requirements, maintaining a low switching frequency while also utilising low voltage rated switches. The expansion of these topologies (FC and NPC) to a large number of levels however has been limited due to added complexity associated with non-standard connections which could lead to increased development costs, increased control complexity and difficult implementation.

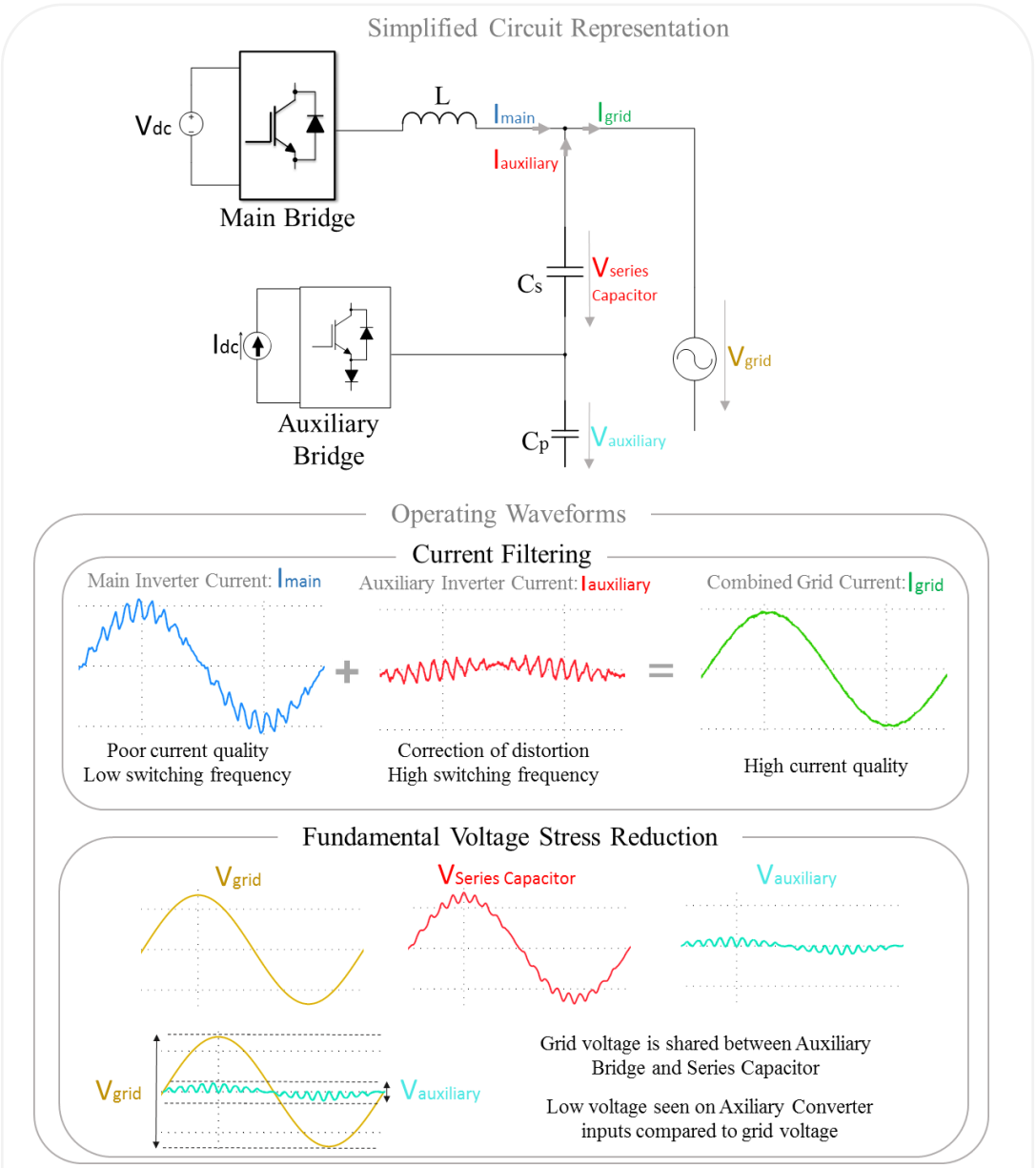
Despite this limitation, multilevel topologies found widespread use for MV applications [7]. The highest market penetration is attributed to the three-level Neutral Point Clamped (3L-NPC) converter due to its high reliability, low installed power in the switches and high efficiency. On the other hand, as a compromise, the filtering requirement has remained challenging. The reason is that the level of switching harmonics is high, a characteristic of a 2/3-level PWM, and that the switching frequency has to be kept low to preserve power converter efficiency. Furthermore the attenuation of passive filters for single order (L) or third order (LCL) filters is limited by the relative ratio of switching to cut-off frequency which is related to the fundamental frequency or one of the significant harmonics ($5^{th}/7^{th}$) [8, 9].

Another direction of research which has been shown to improve the utilisation of switches at a low cost is the development of hybrid converter solutions. By the combination of technological solutions associated with different attributes, substantial overall performance improvements can be achieved which in turn maximise the impact of the technology. Such an improvement has been demonstrated by the development of "transformer-less" Hybrid Active Power Filters (HAPF) used as harmonic compensators in MV grids while utilising low voltage rated semiconductor devices. The minimisation of the active filter solution power rating, increased efficiency and most importantly the reduced cost has been a significant impact factor on the uptake of HAPF as a research topic and industrial solution.

This thesis proposes and presents experimental evaluation of the performance of a hybrid power converter solution that consists of a slow-switching medium-voltage main inverter whose large switching harmonics are actively filtered by an auxiliary inverter which has a very low VA rating as a result of significantly lower voltage and current rated devices when compared to the main inverter.

The topology consists of a 3-phase Voltage Source Inverter (VSI) connected to a MV grid acting as a main inverter bridge connected in parallel to a Current Source Inverter (CSI) acting as an active filter to cancel out the switching current ripple produced by the VSI. The CSI is connected via a series capacitor which minimises the voltage stress to only a small fraction of the fundamental grid voltage via a developed control approach. An overview of this arrangement is shown in Fig. 1-1.

The main benefit of this circuit is that the added installed power of the CSI can be reduced to a fraction of the main inverter bridge leading to a lower cost for a given performance. As a result, the hybrid topology allows for optimal device utilization to achieve high output current quality with minimal device ratings and potentially improved efficiency. The control of the auxiliary CSI could remain independent of the main inverter bridge which means that the auxiliary converter solution can be retrofitted to existing MV installations for power quality improvement.



Main Bridge	Auxiliary Bridge
VSI	CSI
Medium Voltage	Low Voltage
Low Switching Frequency	High Switching Frequency
IGBT	RB-IGBT or equivalent

Fig. 1-1: Generic overview of proposed topology operation, configuration and features

1.3. Aims and Objectives

This thesis aims to identify and report on the development of a new hybrid converter arrangement for use in MV grid applications and provide a thorough investigation into its suitability, performance and possible advantages as well as acknowledging factors which could inhibit the desired performance.

The objectives are:

- Investigation of existing technological solutions and their associated advantages through literature followed by identification of areas of improvement
- Development of a new Hybrid converter with identified advantages over existing solutions.
- Proposition of a suitable theoretical analysis for the operation of the Hybrid topology along with power system scaling and a suitable control scheme
- Evaluation of overall performance at medium-voltage levels through software simulation
- Experimental validation of the hybrid concept at low voltage levels
- Identification of areas for improvement or any possible future direction for the project

1.4. Thesis Outline and Content

Chapter 2 presents the literature review of the existing technological solutions for electrical power conversion with a focus on proposed or demonstrated solutions for MV applications. The main approaches to harmonic mitigation for MV are also outlined before the hybrid concepts relevant to the hybrid topology implemented in this project are introduced. Finally the main choices behind the development of the hybrid topology are discussed.

Chapter 3 presents the design procedure which is based on a simplified equivalent model followed in order to size the topology for MV applications. The operation and performance of the topology is then evaluated via simulations for MV levels for a stiff grid which constitutes an ideal connection scenario.

Chapter 4 presents the additional considerations that need to be taken into account when a grid impedance is included in the model. The MV design point is kept from chapter 3 with the additional implications explained for a small grid impedance, and large grid side impedance which considers an interconnection scenario of the auxiliary converter as part of a MV VSI with an LCL output filter. Simulation results are evaluated for the latter scenario as well as along the further topological development required to address the presence of high frequency voltage ripple at the PCC.

Chapter 5 presents the details of the setup of the experimental rig used to achieve the experimental validation of the circuit operation scaled to standard grid voltage 415V level. The measurement equipment is also presented along with the experimental procedure followed to achieve the experimental validation. Finally the chapter outlines how the grid interconnection scenarios in Chapter 3 and 4 have been approached and implemented.

Chapter 6 presents the experimental results and a performance evaluation for the hybrid topology connected to an electronic three phase AC source, representing the circuit operation under ideal grid conditions, similar to Chapter 3. The feasibility of the proposed concept is thus validated

while the experimental performance is also evaluated over a range of selected CSI switching frequencies.

Chapter 7 presents the experimental results and a performance evaluation under operation with the real power grid. Due to grid voltage imbalances and harmonics, the operation of the converter is compromised. The effects are analysed before a revised control approach is proposed and implemented. The second part of the chapter evaluates the circuit performance when connected to the grid via an added grid side impedance, demonstrating the presence of effects outlined in Chapter 4.

Chapter 8 presents a final comparison of the performance under the different operating conditions considered. A discussion is then included summarising the system performance and operation. A summary of the main findings in this project is finally presented.

Chapter 9 presents the conclusions, highlighting key performance advantages and disadvantages offered by the proposed hybrid concept, followed by a summary of the novel aspects derived from this work and then concluding with proposals for future research work on this topic.

CHAPTER 2. Literature Review and Background

The basis of the proposed Hybrid topology involves the combination of ideas from a wide pool of power converter solutions. This chapter therefore presents the current state of the art around what are considered to be existing or emerging solutions applicable to medium-voltage (MV) while also outlining existing literature related to the hybrid techniques similar to the one used in this project. The first section of this chapter presents a brief history of power converters suitable for MV applications to outline the requirement for power quality filtering and the main approaches which have been deployed. The second section reviews related hybrid topologies and concepts such as active filtering and rated power minimisation techniques. Many of these techniques are associated with low cost solutions which could be implemented in MV applications.

2.1. Voltage and Current Source Inverters: a Brief History

Current source power conversion was the predominant technological solution for high voltage conversion after the emergence of the semi-controlled Thyristor valves in the 1970s. The high power rating in terms of voltage and current as well as the high efficiency established Line Commutated Converter High Voltage Direct Current (LCC HVDC) systems as the standard in high voltage power conversion with a transfer capability exceeding one GW. However, commutation at line frequency and dependency on the AC voltage to turn the devices off meant that the LCC had limited flexibility in terms of control. Additionally very large passive filters were required which increased losses whilst occupying a significant volume as a proportion of the converter station [10].

The use of Thyristors has been in decline with the introduction of lower rated but self-commutated devices. The introduction of Gate Turn-Off Thyristors (GTO), Integrated Gate-Commutated Thyristors (IGCT) and Insulated Gate Bipolar Transistors (IGBT) enabled the possibility of

implementing large Voltage Source Conversion (VSC) [11, 12]. The desire to evaluate the potential and limits of VSC technology has monopolised industrial and academic interest for the past few decades. Pulse Width Modulated (PWM) VSCs offer many advantages in HVDC transmission applications [13] due to the relatively compact size, bidirectional power flow and good utilisation of new cable technologies [14, 15]. However the higher cost of an HVDC converter station compared to HVAC based solution means that HVDC implementation is favoured over longer distances where the need to transfer very large amounts of power could make it a cost effective solution [16].

2.2. Converters for Medium Voltage Applications

In the past few years the advantage of Medium Voltage Direct Current (MVDC) based distribution over MVAC started to be considered [17, 18]. Based on the criteria of distance and power levels which are currently defining the economic viability of HVDC, the electrical distribution system in the medium term would be expected to remain AC. By extension the AC distribution system will require the use of high voltage DC/AC inverters to interface the transmission and distribution systems, as well as interfacing renewable energy sources that reach power levels which favour MV conversion [3].

Although slow switching PWM Current Source Rectifiers could also be used for MV applications [7, 19] the losses are usually higher than Voltage Source topologies [20]. Standard two-level Voltage Source Inverters built using series connected devices were initially used in the first generation of forced commutated high and medium voltage systems. This approach was favoured due to the simplicity and the easiness to embed the required redundancy by adding additional devices in series. However, difficulties in achieving static and more importantly dynamic voltage sharing during switching [21, 22] meant that the harmonic performance of such inverters was poor due to the low number of voltage levels and further limited by the low switching frequency

[6]. In the last 5 years, forced commutated IGBTs with ratings of 6.5kV [23, 24] and up to 1kA [25] became commercially available, reducing the number of series connected devices needed in a higher voltage two-level inverter which could potentially lower the complexity and cost.

However MV rated forced commutated devices, with ratings above 2kV, exhibit poorer switching performance for same kVA switched compared to lower rated devices. The higher switching loss therefore also becomes a limiting factor that will restrict the switching frequency to approximately 1 kHz [26]. As a result, the low switching frequency means that power quality will remain a problem for a two-level medium/high voltage inverter implementation.

A possible future improvement would be expected to stem from the recent developments in wide bandgap devices. Silicon Carbide (SiC) or Gallium Nitride (GaN) based switches could potentially offer a reduction of the switching losses and an improvement on the associated restriction on switching frequency. However these are yet to be industrially developed and proven as a MV solution. Additional concerns could be created by the electromagnetic interference (EMI) produced by switching very fast at large voltages [27]. In the most recent development a 6.5kV 1kA SiC diode module has been characterised [28].

2.2.1. Multilevel Inverter Solutions

Multilevel inverters operate by interchanging the AC voltage output between smaller discrete voltage steps which are a fraction of the total DC voltage. The principle of multilevel operation is beneficial in multiple ways. The reduction of voltage stress allows the use of lower voltage rated and better performance semiconductors which can reduce the overall system losses. Furthermore the improved dv/dt characteristic on the AC side modulated voltage reduces the filtering required to achieve the same power quality as a two-level inverter. By extension, independent of topology and modulation strategy used, for a high number of voltage levels the requirement for filtering could be minimal based on minimisation of dv/dt.

The most common Multilevel converter topologies [29-33] are based on the Isolated/Cascaded H-Bridge (CHB) [31], the Flying Capacitor (FLC) [30, 32] and the Diode Clamped converter also

known as Neutral Point Clamped (NPC) Inverter [29]. These topologies were proposed more than 20 years ago and have been commercialised with the aim of addressing the static and dynamic stress sharing limitations of the two-level inverters using series connected switches.

These topologies have been investigated in the past decades in an effort to assess their associated advantages/disadvantages, their suitability for different applications [31, 34-36] and propose variants which can offer specific performance advantages. They can be considered the benchmarks in multilevel converter topologies and the competitive advantages between them and novel topologies will continue to be considered for optimal scaling in terms of output power, efficiency, sizing and cost [37-41].

Based on the aforementioned investigations the limitations of each topology have been acknowledged. The cascaded H-bridge topology, which is a modular solution, requires DC side isolation between each H-bridge which is usually addressed via the use of multi-pulse transformers which can be costly and non-standard to design[34, 36]. The balancing of DC capacitor voltages for these topologies has also been a challenge but different control approaches have been demonstrated as a solution [31, 36].

The most cited specific disadvantage of the NPC is the unequal loss distribution between the inner and outer switches in each phase leg[34] which could lead to a reduction of the maximum apparent power processed by the overall converter. The active-neutral-point-clamped (ANPC) topology has been proposed as an alternative improved topology to address this issue [42-44]. The ANPC however requires semiconductor switches in place of the clamping diodes used in the NPC topology, thus increasing the overall cost of the devices.

The most important drawbacks for these multilevel topologies are the scalability to increase the number of voltage levels which is not straightforward and is associated with an increased complexity in the modulation and control as well as practical implementation issues. Building an inverter leg with a high number of levels requires different connection paths for the clamping diodes in the case of the NPC or capacitors in the case of the FLC that resulted in large and uneven

stray inductances and made the implementation of building blocks quite problematic[36]. A single phase representation of the aforementioned topologies is shown in Fig. 2-1.

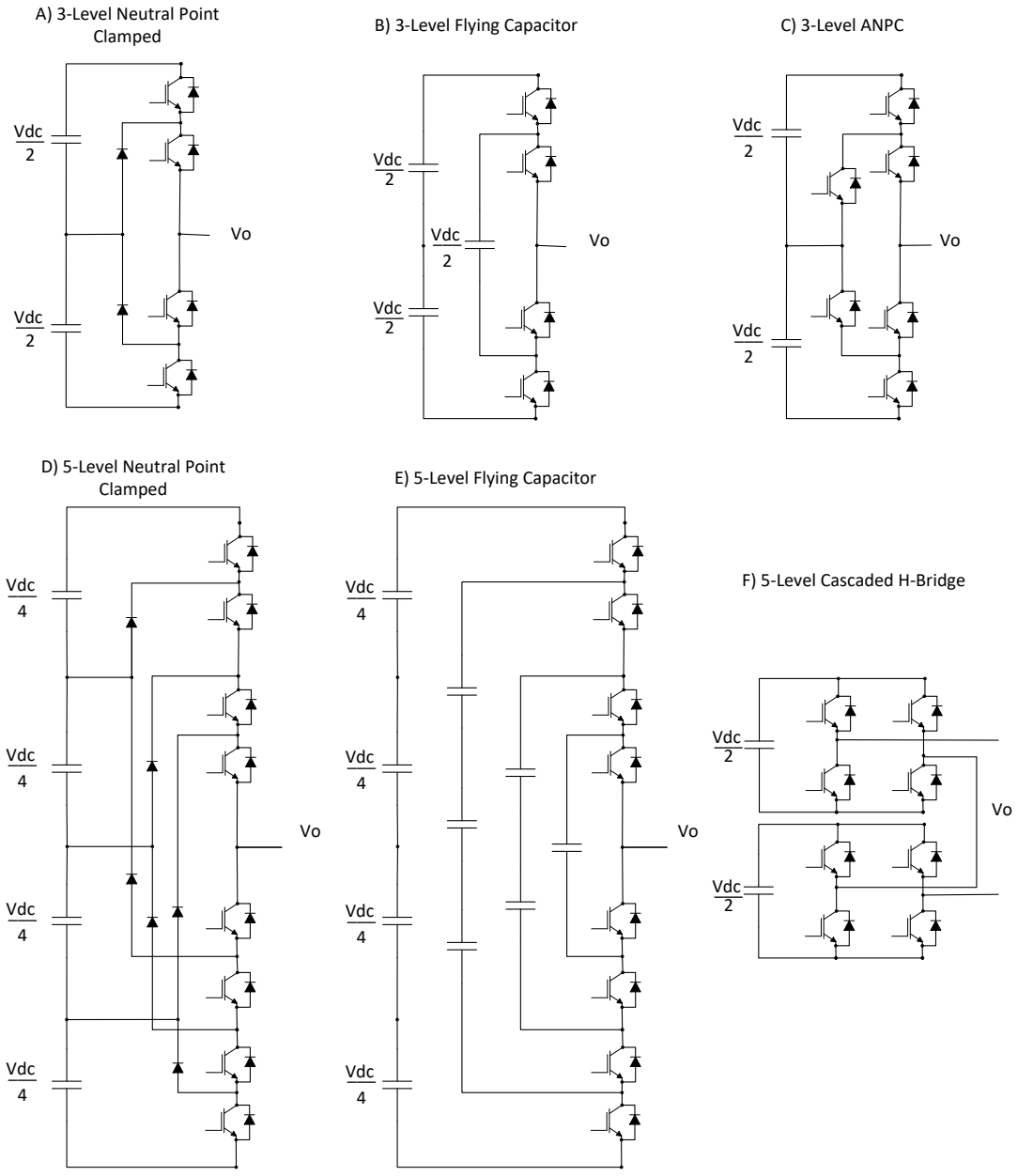


Fig. 2-1: Single phase representation of multilevel topologies: a) 3-level NPC ; b) 3-level FLC; c) 3-level ANPC; d) 5-level NPC; e) 5-level FLC and e) 5-level CHB

Due to the above reasons the implementation of these topologies is practically limited to a low number of levels, usually less than 5. The most popular MV topology is the three-level NPC(3L NPC) due to its high efficiency, high power density and simplicity of control [39], but to maintain a high efficiency the switching frequency is typically restricted around 1 kHz in high power applications [26].

The Modular Multilevel Converter (MMC) proposed 16 years ago [45, 46] has gained increased popularity in a short period of time. This popularity is due to its reliance on identical building blocks that would enable cost effective mass production and allow flexibility in implementing any custom design system solutions.

Other advantages of the MMC are that a single isolated DC source is needed unlike the cascaded H-bridge [47], flexibility in the topological implementation of each cell [48] and possibility of including redundancy while also maintaining high efficiency. Additionally, the need for AC filtering is reduced due to the high quality AC currents. These advantages associated with a large number of levels also require a high device count and added cost due to sensing and control although cost minimisation is theoretically delivered by means of mass production at the manufacturing level. A disadvantage of MMC is the sizing of DC capacitors needed to attenuate the voltage ripple, something which could lead to a compromise between the system size and cost [49] or a limitation of the operating range by the minimisation of the circulating current [47].

While the MMC is undeniably a highly advanced technological solution, particularly suited to high voltage applications, the advantages may be less favourable at MV compared to the low cost, proven high efficiency and simplicity offered by the conventional multilevel topologies. On the other hand, the aforementioned topologies are restricted to a low number of output levels where output current quality for a low switching frequency will still remain a problem for the reduction of passive filter size and cost.

2.3. Harmonic Mitigation Techniques

This section presents the main techniques reported in literature which are used to improve the harmonic quality of low switching frequency converters with a low number of output voltage levels.

2.3.1. Higher Order Passive Filters

One solution for the improvement of a converter current harmonic performance is the use of higher order passive filters. For Voltage Source Inverters, LCL filters are known to achieve better attenuation at the switching frequency compared to 1st order (L) filters. However the design of LC filters is more challenging due to the need to carefully consider the resonant frequency placement and the potential need for damping of resonance to maintain waveform stability [8]. A damping resistance which can sufficiently reduce the resonance also causes significant additional losses. Stability can sometimes be achieved without damping [50] or via the use of active damping solutions applied in the control system [51-58]. Recently another interesting solution has been proposed where the provision of active damping in an LCL filter is implemented via the connection of a VSI to replace the damping resistance, a method of damping with loss minimisation [59].

In many MV applications LCL filter design is even more restricted by the low converter switching frequency, often less than 1 kHz. The filter resonant frequency must therefore be placed close to the typical low order harmonics (5th, 7th etc.) present in distribution grids in order to achieve significant attenuation of the converter switching harmonics [9, 60]. The problem is outlined in [9] where the concept of virtual harmonic content is introduced in order to design the LCL filter to comply with grid code requirements with the lowest possible filter size.

2.3.2. Selective Harmonic Elimination PWM

Mitigation of harmonics can be achieved using different control approaches. Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) has been proposed as a method to manipulate the output harmonic profile of PWM converters [61-63]. The method requires the pre-calculation of switching angles to eliminate specific even/odd orders of harmonics and is particularly suitable for high power converters where the switching frequency is limited [64].

This task of calculating angles is computationally demanding and can increase in complexity depending on the topology as well as the number of harmonics to be eliminated and therefore is predominantly performed offline. Generalised approaches have been outlined for switching angle calculation [65] are usually further refined using different optimisation methods [66, 67] with the output stored in look-up tables. The technique has also been applied to AC motor drives [62] and in [68] for DC motor drives where it has been demonstrated that the objective function could also be changed to provide minimisation of torque ripple.

In [69] a generalised modulation technique using logic-based signal conditioning has been proposed to provide SHE for Current as well as Voltage Source Inverters. The advantage is that SHE can be performed online, but the order of eliminated odd harmonics is dependent on the switching frequency. A limitation of this approach is that it cannot compensate for unpredictable grid induced harmonics. More recently [70] proposed an online modification as an improvement to the offline approach. An active compensation method is used to "deviate" from the pre-calculated switching angles in order to compensate for grid induced (5^{th} order) harmonics. The approach has been demonstrated for a Current Source Rectifier with a low switching frequency.

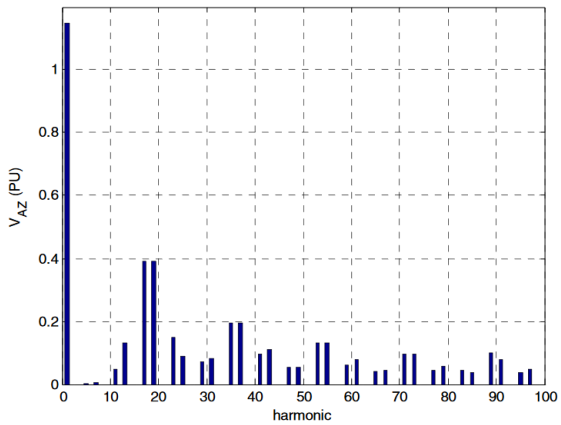


Fig. 4 VVHD of PODPWM strategy

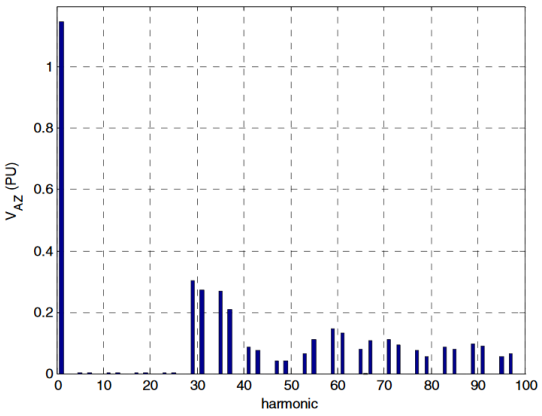


Fig. 3 VVHD of SHEPWM strategy

Fig. 2-2: Theoretical Harmonic spectrum produced by Phase opposition PWM (left) and using SHE-PWM for harmonic cancellation up to the 29th order as presented in [60]

More importantly [60] demonstrated the use of SHE-PWM for a 3.3 kV MV three-level NPC to eliminate harmonics up to the 29th order in combination with an optimised LCL filter design approach. This has been shown to achieve a more optimal filter size while providing attenuation within grid code regulations. The use of SHE-PWM in combination with an optimized LCL filter design for MV has also been demonstrated [71], achieving a highly notable performance with THD levels of 2-0.5% with efficiency ranging from 97-99% for output power ranging from 1-5MW.

2.3.3. Active Power Filtering for Low Order Harmonics

The use of power converters for active power filtering is established as a method of improving harmonic performance as well as performing reactive power compensation [72]. Many topological variations exist with the main classifications being series or shunt connected arrangements, or in some cases both. A commonly cited overview of active power filters has been presented in [73], while an overview of control techniques is presented in [74].

Series connected Active Power Filters (APF) can be used to improve harmonic voltage performance at the point of connection. Shunt connected APFs behave like a current source at the point of connection and can be used to eliminate current harmonic disturbances as well as to

provide reactive current compensation. Typically three phase shunt APF topologies are used to compensate for low order odd harmonics in the current drawn by a non-linear load. The performance is typically assessed using an inductive or capacitive load, or combination of both. The basic principle of shunt APF operation is based on the detection and elimination of any current distortion. The detected distortion is cancelled by the injection of a current equal in amplitude to the distortion but of the opposite polarity, resulting in sinusoidal grid side current waveforms. The rating of active power filter topologies is investigated in [75] while it is generally acknowledged that the semiconductor ratings will largely dictate the cost of an active filter, which can be significant depending on the processed power.

2.4. Hybrid Topologies

Another direction of power converter research is hybrid topology arrangements which in principle benefit from the combination of positive attributes associated with different converter topologies to offer a performance enhancement from the overall hybrid arrangement.

For medium-voltage these could include the alternative utilisation of switching devices and scaling for a given “standard” topology. An example is the asymmetrical cascaded-H bridge multilevel topology [76] where an asymmetry in the voltage level of each DC link capacitor provides a larger number of output voltage levels. This asymmetric voltage synthesis can enable the combination of IGCT with IGBT bridges [77, 78] with the aim of improving efficiency and achieving better utilisation of power semiconductor devices.

Hybrid solutions could also involve the combination of different converter topologies. A common approach involves the utilisation of a main converter, usually of higher voltage or current rating, with a lower rated auxiliary converter which provides added functionality. In [79] the series connection of H-bridges to each output phase of a three-phase MV 3L-NPC can provide additional voltage levels to achieve a reduced filter size. The three single-phase H-Bridges in this case must be rated at the full converter current whist the DC-link voltage is significantly lower.

A different approach to hybridisation has been the combination of active and passive filters. One solution is the parallel placement of an active filter to a passive filter at the Point of Common Coupling (PCC) to increase attenuation. A series connection of the two however can provide further advantages; [80] proposed the series connection of a VSI active filter to a two stage passive (L+LC) filter to achieve increased attenuation while also minimising the power rating of the active filter.

The implementation of a hybrid active power filter HAPF consisting of a series LC filter controlled with a floating isolated inverter to dampen resonances, increase filter attenuation, and mitigate harmonics while also benefitting from a low active filter VA rating was demonstrated in [81]. The topology is shown in Fig. 2-3.

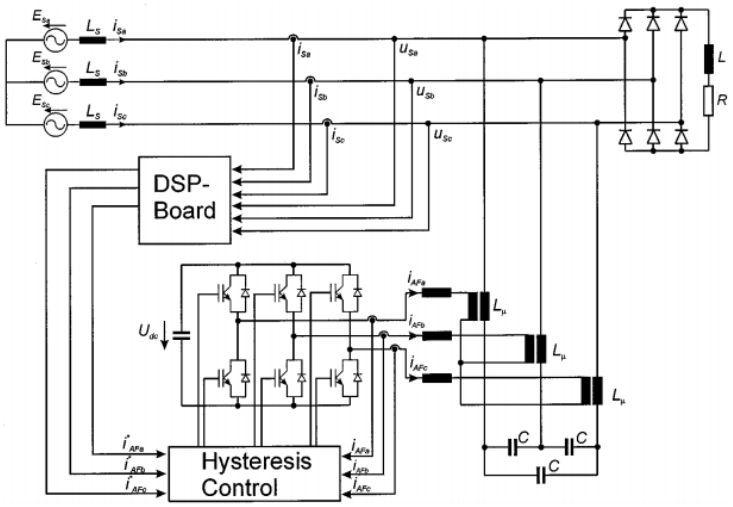


Fig. 2-3: Hybrid active power filter connected to LC filter as proposed in [81]

2.4.1. Use of Series Capacitors for Reduction of Voltage Rating

Expanding on the concept of hybrid active power filters, [82, 83] proposed the idea of implementing a three phase active filter that works at MV by using a low voltage VSI connected in series with capacitors to block the 50Hz fundamental voltage component. The use of series capacitors has been presented as an alternative to a step down transformer therefore reducing the passive component cost. Most importantly the minimisation of the inverter voltage stress leads to

a low installed power and low cost solution which could enable the use of low voltage rated semiconductors in a MV application.

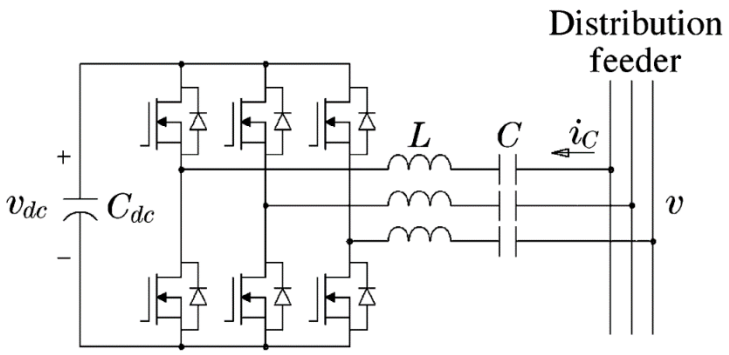


Fig. 2-4: Series capacitor connected active filter topology as proposed in [82]

The arrangement as shown in Fig. 2-4 is considered hybrid by the combination of passive filtering provided by the tuning of the LC response, formed by the combination of a series capacitor and the VSI filter inductance. The capability of this topology for reactive power compensation is limited by the LC circuit scaling and the requirement to sustain the grid voltage drop across the series capacitor.

The tuning of the filter is therefore also designed with regard to the reactive current compensation [84] and is typically chosen around low frequency odd harmonics (3^{rd},5^{th}, 7^{th}, 11^{th}) according to the requirement of the application. Another benefit for further reduction of cost in some applications comes from the possibility of connecting the inverter to an existing LC trap filter to provide harmonic improvement.

The suitability of these topologies for MV applications has been investigated in [85, 86] where the Hybrid Active Power Filter (HAPF) is a three-level NPC acting as the active filter (60kVA) utilising IGBTs rated at 1.2kV in a 6.6 kV MV grid. The HAPF is used to provide harmonic compensation to the distorted currents at the input of non-linear load used in a 1 MW motor drive application. The resulting voltage reduction is quoted to 20% of the grid voltage [87].

The use of a hysteresis controller, which can provide accurate tracking performance, fast dynamic response and benefits from an easy implementation has been presented as an appropriate

modulation method [88]. A linearized hysteresis controller for operation within the non-linear inverter current slope given by the LC impedance has been investigated in [89] for a three phase four wire system. The effects of sampling time on the effectiveness of the hysteresis controller have also been investigated [90].

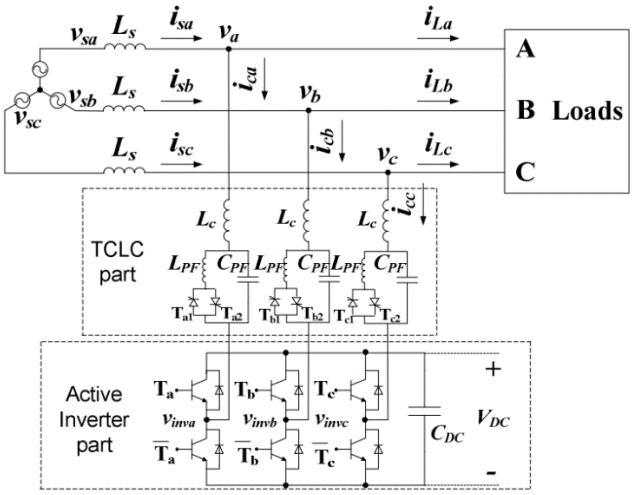


Fig. 2-5: Thyristor Controlled LC-Coupling Hybrid Active Power Filter (TCLC-HAPF) topology as presented in [91]

More recently a variation of the hybrid active power filter topology has been proposed using a series capacitor connected VSC coupled with a Thyristor Controlled Reactor (TCR), as shown in Fig. 2-5. The proposed advantage of this arrangement is the capability of simultaneously performing both reactive power and harmonic compensation for a non-linear load while also operating at reduced switching device voltage levels [92]. The concept has also been demonstrated to operate in the case of unbalanced currents in a non-linear load [91, 93]. A comprehensive review on the development of shunt connected active and hybrid active harmonic filters was presented in [94].

2.4.2. Series Capacitors with a Current Source Inverter

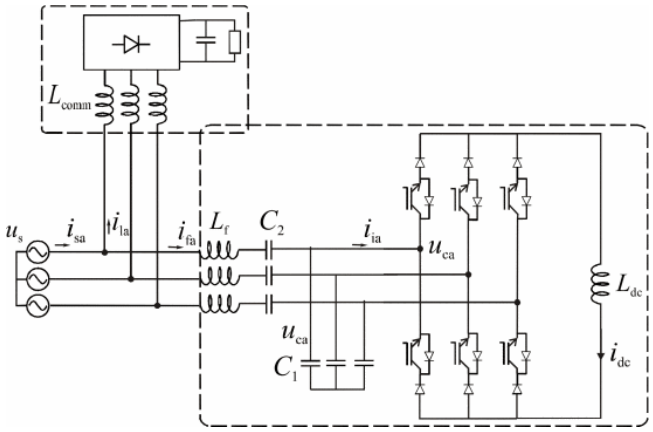


Fig. 2-6: Series capacitor connected CSI HAPF as proposed in [95]

The use of a series capacitor with a CSI has been investigated [95-98] for low voltage active power filter applications, as shown in Fig. 2-6. Furthermore [97] investigated the comparative performance advantages between series capacitor connected and conventional active filter topologies. The outlined advantages of the CSI HAPF are the ability to synthesize current without requiring closed loop control as well high efficiency matching the performance of the series capacitor connected Voltage Source Inverter. The device voltage stress given by the peak line to line AC voltage has been reduced to around 50% of the grid voltage 690Vrms (line-line) thus enabling the use of 1.2kV devices. This is a big improvement compared to the 1.7kV devices which would be needed for a CSI active power filter without the use of series capacitors.

In low voltage renewable energy applications a series capacitor connected CSI has been used for matching the voltage characteristic of photovoltaics with the AC grid voltage level to maximize efficiency [99].

2.4.3. Active Current Ripple Cancellation Technique

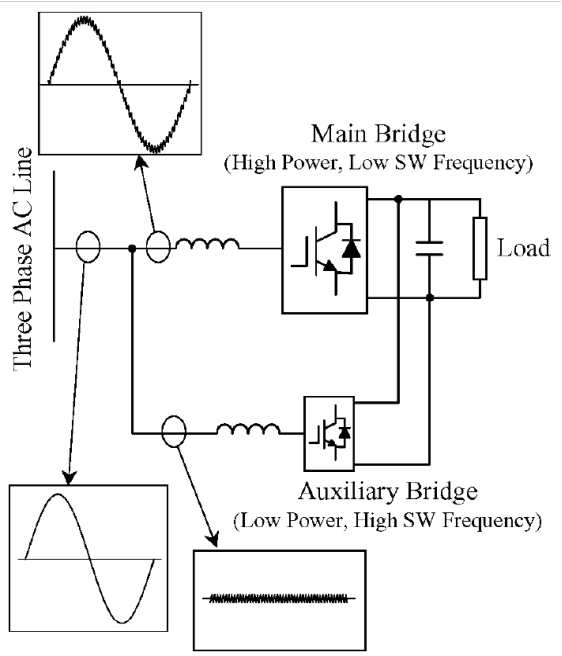


Fig. 2-7: Hybrid topology using auxiliary converter to provide ripple cancellation for current quality improvement [100]

A technique to improve the output current harmonic quality of a main high-power-rated inverter has been proposed in [100]. The auxiliary inverter shown in Fig. 2-7 cancels the main current switching ripple, which is a small fraction of the main inverter current, whilst operating on the same DC-link voltage level. The proposed control strategy involves subtracting the current reference from the measured main current to extract the current ripple which, after inversion, forms the reference waveform to the hysteresis controlled auxiliary converter. The reported current total harmonic distortion (THD) is at 0.6% using a main converter switching at 1.2 kHz, compared to 0.9% THD for a non-hybrid converter switching at 10 kHz.

The most important advantage of this topology is the dramatic decrease in current rating of the auxiliary inverter which only needs to be scaled at the peak current ripple amplitude of the main inverter. This mode of operation is therefore significant towards the power reduction to the auxiliary inverter.

2.5. The Hybrid Topology

This section describes the general idea behind the Hybrid topology and mode of operation as inspired from the literature presented in the previous section. Some of the challenges in the operation are then described, which lead to the choices of topology for the main and auxiliary inverter bridges. The detailed topology is presented later in Fig. 3-1 of CHAPTER 3. The main advantages of the hybrid topology are described compared to previous state of the art. The final section describes the approach followed towards evaluating the aforementioned advantages and system performance.

The idea behind the hybrid topology is to improve the output power quality of a slow switching medium-voltage inverter typical of MV applications by using a low current and low voltage rated auxiliary converter. Building on the techniques used to achieve voltage and current reduction in hybrid active power filters; the auxiliary inverter in this topology acts as an active harmonic filter to cancel the switching ripple produced by the main inverter. Thus the current rating of this part of the converter can be a small fraction of the total current. By also connecting the auxiliary inverter behind a set of series capacitors most of the grid voltage, which is expected to be at the grid fundamental frequency, is blocked therefore resulting in a dramatic decrease of the switching device voltage stress.

The installed kVA of the switching devices in the auxiliary converter will therefore be a small percentage of the installed kVA of the main inverter. This is considered to be particularly suitable for 3.3kV MV grids as it could enable the use of low voltage rated fast switching devices (up to 1.2kV). The solution has potential to benefit from an improved utilisation of switching devices and improved performance at minimal additional cost.

The low output power quality assumed for the main inverter in this application has a number of implications which can be used as performance indicators. The switching frequency is low, which could be beneficial in maintaining low semiconductor losses therefore a high efficiency can be expected. Furthermore a small output filter (considering a single order filter) can be used, which

should also have a lower reactive power requirement and theoretically require a lower DC-link voltage for the same fundamental current level.

In the proposed solution the main converter is a three-level Neutral Point Clamped (NPC) VSI due to its suitability for MV operation, but the auxiliary converter could also be combined with a two-level or another three-level topology. Although the auxiliary converter could operate independently, it must be designed and operated within the context of the main inverter's capabilities. Much like the topology shown in §2.4.3, the switching current ripple produced by the main converter will have a major influence on the current rating and the performance requirement of the auxiliary converter. The assessment of the current ripple characteristics is therefore important from a problem definition perspective towards the development of the proposed topology.

2.5.1. Harmonic Output of a PWM VSI

The current ripple in the AC side inductor of a PWM VSI in a grid connected application is formed by the voltage across the converter inductance. This voltage is based on the instantaneous difference between the grid voltage and the PWM output voltage of each converter phase. The envelope of the current ripple shape in a fundamental cycle will vary based on the topology, the modulating technique chosen whilst having a dependency on the maximum DC-link voltage, the switching frequency and the inductor size.

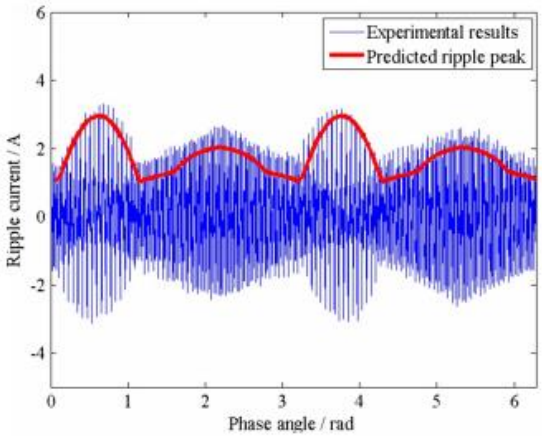


Fig. 19. Experimental results of current ripple with SVPWM.

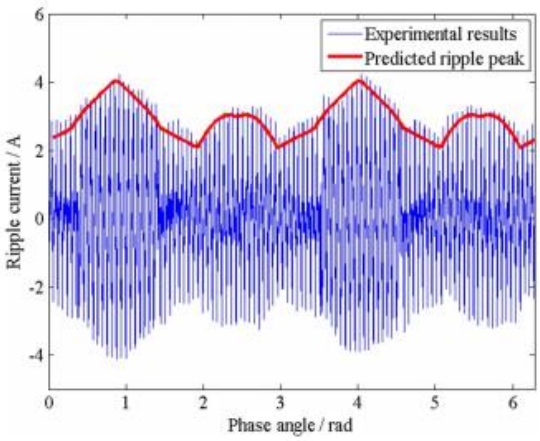


Fig. 20. Experimental results of current ripple with DPWM.

Fig. 2-8: Experimental and predicted current ripple profile [101]

A prediction of the instantaneous current ripple amplitude profile for a three-phase two-level VSI with carrier based and space vector PWM was described in [101] with reasonably good experimental validation, as shown in Fig. 2-8. The discrepancy between measured current ripple and the prediction has been attributed to the effects of dead-time, measurement errors and non-ideal behaviour of components. Predicting the current ripple shape with high accuracy could be difficult outside of a controlled lab environment, therefore a reliance on current sensing would be necessary in an active filtering application, such as the one proposed in this thesis.

Investigations have been recently reported in literature aiming to evaluate the theoretical amplitude of the switching current ripple produced by a VSI. To acquire the normalised current ripple amplitude over the modulating depth and angle, an analytical approach must be performed considering the modulation strategy applied to each topology. The peak to peak current ripple for a two-level and a three-level converter (NPC) is analysed for carrier-based and space vector modulation in [102], but with an induction motor as the load. An analytical evaluation of the peak to peak amplitude for a two-level three-phase grid connected VSI has been presented in [103] using space vector modulation.

Rather than following an extensive analytical approach as done in the above papers, the proposed design procedure for the hybrid topology has been kept generic by defining the maximum VSI current ripple amplitude. The achieved converter scaling will therefore apply to most scenarios

where the current ripple amplitude is maintained under the maximum limit. The scaling of the VSI filter inductance was calculated based on simplified expressions relating the switching frequency, DC-link voltage and peak current ripple, with further adjustments done if necessary, to ensure the evaluation is performed at the intended maximum current ripple level.

Further to defining the maximum current ripple amplitude which will define the current rating of the auxiliary converter, the VSI current harmonic spectrum is also a consideration for the selection of a suitable auxiliary converter switching frequency. The triangular ripple shape will create harmonic clusters at multiples of the switching frequency, as shown in Fig. 2-9. Depending on the modulation strategy used, harmonic side bands will appear around the switching frequency at multiples of the fundamental frequency. A detailed analytical solution for the switching frequency harmonic production in voltage source converters can be found in [104].

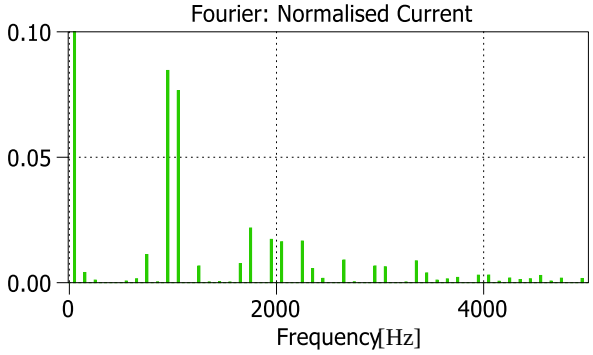


Fig. 2-9: Example harmonic content of a VSI current for a switching frequency of 1 kHz

The sidebands around the switching frequency harmonics will typically have the largest amplitude [104] with the amplitude of remaining sidebands decreasing as the harmonic order increases. Considering a main voltage source inverter with a switching frequency of around 1 kHz, the most significant sidebands will appear around the switching frequency with negligible amplitudes upwards over about 5 kHz compared to the fundamental amplitude. The auxiliary inverter bandwidth requirement is therefore significantly higher than a conventional active power filter.

2.5.2. Choice of Auxiliary Inverter Topology

With respect to the hybrid filter concept, most papers use a Voltage Source Inverter as the auxiliary bridge, which if used to synthesize currents for this application would require a very fast current controller and therefore a relatively high switching frequency. For this reason a Current Source Inverter has been chosen as the auxiliary converter due to its ability to directly synthesize the AC current ripple reference whilst switching slower for a similar current tracking performance. A VSI with a hysteresis controller could have been used as an alternative solution, however the reduced DC-link voltage of the auxiliary VSI in conjunction with a residually high level of grid impedance may limit the current ripple tracking capability (di/dt). Furthermore using capacitors to decouple the grid inductance may lead to resonance being excited by the wide and uncontrolled harmonic profile of the hysteresis control.

Although the weight of DC-link inductor of the CSI tends to be large compared to DC-link capacitor of a VSI, the inductor lifetime and its ability to handle surge stresses (over-currents and over-voltages) is superior compared to electrolytic capacitors, which are more sensitive to over voltages, current ripple and temperature variations. The losses due to the auxiliary CSI as part of the hybrid assembly should in ideally amount to a small percentage of the total output power processed.

2.5.3. Novelty and Potential Benefits of the Proposed Topology

The novelty of the proposed power converter topology in relation to [95-98] is that it addresses applications where the main inverter is of a different voltage class. The installed kVA in the auxiliary inverter is further reduced by the series connected capacitors that block most of the fundamental AC voltage in a similar way to the technique report in [83] while also benefiting from a significantly reduced current rating as in [100]. Although reactive power compensation via the CSI is not possible in this arrangement [91] , it is possible to achieve unity power factor by means of the main Inverter that can also compensate for the reactive power associated with the

use of the series capacitors. The impact on the power factor can also be limited via the choice of series capacitance. Conceptually the topology shares the attributes of multilevel converters in terms of the ability of using lower voltage rated switching devices as well as providing high output current quality with a small current ripple.

From a combined bandwidth perspective any low-order harmonics (3^{rd}, 5^{th}) could theoretically be mitigated by the main converter control, while harmonics beyond the VSI bandwidth can be cancelled by the CSI. A limitation of this topology is that the CSI should not compensate for low order harmonics as this would affect the voltage reduction capability due to the large harmonic voltage that these harmonics create across the series capacitors.

Perhaps the most important advantage of this topology is that the auxiliary system can be retro-fitted to an existing MV VSI installation, which can deliver a significant current quality improvement at a minimal cost with a very small impact on the overall system efficiency.

2.5.4. Performance Evaluation Approach

Power Quality

The current harmonic quality indicator used in this thesis is the Total Harmonic Distortion (THD) which relates the root of the added squared harmonic amplitudes to the fundamental current magnitude. However THD figures do not fully account for the significance of individual harmonics, therefore in this investigation the approach taken was to outline the specific amplitudes of what are considered to be the most significant harmonics. Although compliance with grid harmonic codes and standards for power quality and EMC compliance (e.g. BS EN 61000-3-3/4 [105, 106] and in accordance to the Engineering Recommendation G5/4-1[107]) would be essential in a real implementation; the motivation in this project was to quantify the full potential of the harmonic reduction technique as a percentage amplitude reduction of the input harmonics which have been set at an arbitrary high level. The followed approach, considering very poor VSI output quality, is used to clearly quantify the effectiveness of the CSI filtering

capability but without evaluation of compliance to grid harmonic standards. Additionally the maximum CSI voltage stress which, as will be shown, is also dependent on the maximum ripple amplitude is demonstrated to be within the desired levels.

Main Inverter performance

In this investigation, simple carrier-based modulating techniques have been used for the main VSI, with the filter inductance scaled to achieve the desired large current ripple amplitude. The assumption of a main VSI operating with large current ripple for a given switching frequency is considered to be equivalent for an inductance which is undersized for the application and therefore implies a small physical size and cost. The VSI performance could be improved with the application of SHE-PWM (§2.3.2) or other optimal modulating strategy which could result in either current ripple minimisation or smaller filter inductance or switching frequency minimisation. This was considered unnecessary as the investigation is mainly focused on the performance improvement brought by the series capacitor connected CSI whose application is only necessary and beneficial within the context of the aforementioned main inverter.

Installed power

The minimisation of CSI voltage and current stress is assessed in terms of the installed power in the switches. The installed power considers the maximum voltage and current stress experienced by the devices during steady state operation as opposed to inferring to a choice between existing commercial device ratings. To relate this to the main converter, the key performance indicator used is the added installed power by the auxiliary converter semiconductors in comparison to the installed power of the main 3L-NPC converter. As the 3L-NPC is already known to benefit from good and cost effective utilisation of switches [39], a small added installed power will indicate a small financial cost of the hybrid system implementation which is not directly investigated in this project.

2.6. Conclusion

This chapter has outlined the requirement for alternative and cost effective filtering solutions for medium-voltage converters operated at a low switching frequency and with a low number of voltage levels. These converters currently require complex or large passive filter components. The technological innovations which formed the foundations and principles for the development of the proposed topology have been presented with particular emphasis on hybrid techniques regarding cost and installed semiconductor kVA reduction while improving the output power quality.

The approach behind the design of converter topology in the proposed hybrid arrangement has been outlined and the potential advantages have been identified. The next chapter will present the further choices with regard to scaling and the simulated performance evaluation of the topology in a MV application.

SECTION A: Theoretical Analysis and Simulation

CHAPTER 3. Three-Phase Hybrid Inverter Using Series Capacitor

This chapter presents the proposed converter topology and analysis of the converter operation when supplied from a stiff medium-voltage (MV) grid. After the topology has been introduced and the overall operation explained, a generic design procedure is outlined. The corresponding control is also presented before the performance at 3.3kV MV level is assessed using simulation results. The assumption of a stiff grid, modelled as an ideal voltage source, simplifies the design and scaling of the converter. As the effect of grid impedance is considered negligible in this analysis the point of common coupling (PCC) is also the point of connection of the series capacitor.

3.1. Topology Introduction

The converter topology is shown in Fig. 3-1 with the main aspects of the circuit highlighted and labelled. The main converter topology is a three-level Neutral Point Clamped Voltage Source Converter (VSC), which has been selected since it is currently an industry standard and typically used in existing MV applications [39] as it enables the use of 3.3kV devices which offer good switching performance for the power processed. The VSC is interfaced to the three phase MV grid via a line side inductance L_1 which is designed to limit the maximum switching current ripple. The auxiliary converter is a three-phase, two-level Current Source Converter where inductance L_{dc} is the storage element. The CSI switches have been implemented by pairing each IGBT with a blocking diode to ensure unidirectional current flow. A second order low pass AC side filter is used to smooth the output PWM CSI currents. This filter is formed with the combination of capacitor C_p along with an inductor L_f and resistor R_f. This resistor is not shown as its placement

can vary, this is explained in §3.3.3. Finally the CSI is interfaced to the grid at the PCC via series capacitance (C_s), which is designed to block the bulk of fundamental grid voltage.

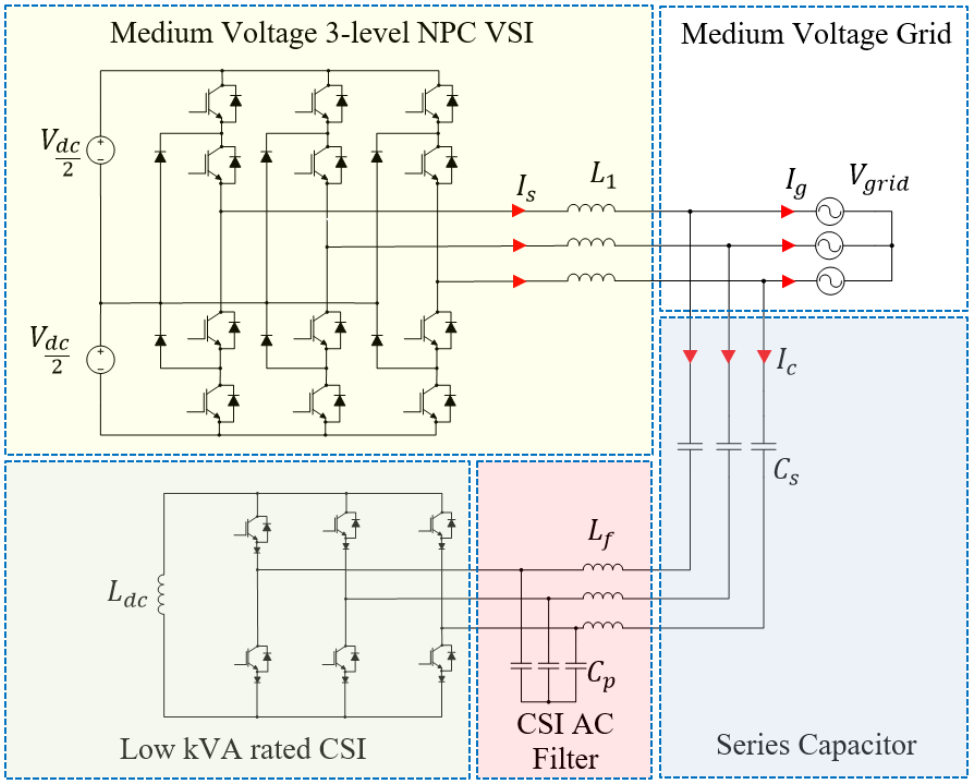


Fig. 3-1: Hybrid system topology highlighting the main features

3.2. Circuit Operation

The bulk power in the hybrid circuit topology is processed by a slow switching, medium-voltage three-level Neutral Point Clamped (NPC) VSC. The control of the main converter is independent of the CSI and can remain largely unchanged compared to a standalone VSI installation with four quadrant operation. The CSI primary role is to act as an active filter to the switching current ripple produced by the VSI. By injecting a calculated fundamental current via the series capacitor it is possible to control of the fundamental voltage sharing between the CSI and series capacitors while also ensuring DC-link current regulation and therefore ensure minimal switching device voltage stress in the CSI. The reference to the CSI is therefore the switching current ripple of the main VSI Bridge, which can be sensed, and the calculated reactive fundamental current component to achieve the desired voltage drop.

3.3. Design Procedure

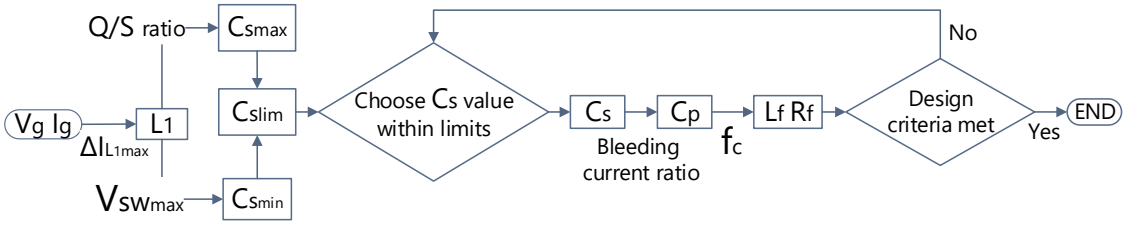


Fig 3-2 : Flowchart of the design procedure for the passive components of the hybrid converter

The proposed design procedure can be implemented in stages considering both the frequency and the time domain equations that define the limits for the desired operating point. The design procedure flowchart is shown in Fig 3-2 with each step explained in detail in the following sections. The main VSI is designed based on the grid requirements, the voltage level and maximum current with the interface inductor L_1 designed for a given maximum switching current ripple based on the DC link voltage level. The procedure then considers the design of the auxiliary converter by choosing the range of value of the series capacitance. As explained in §3.3.2, the maximum capacitance is given by limiting the reactive power associated with the series capacitance (Q) with respect to the apparent power processed by the VSI (S). The minimum capacitance is given by limiting the maximum CSI harmonic voltage stress (caused by the injection of the VSI anti-ripple through the capacitor). An iterative procedure can be used to select a series capacitance value by first selecting an appropriate filter capacitance C_p.The capacitance choice will then define the CSI output filter (C_p, L_f, R_f) if all design criteria are met.

3.3.1. VSI Design

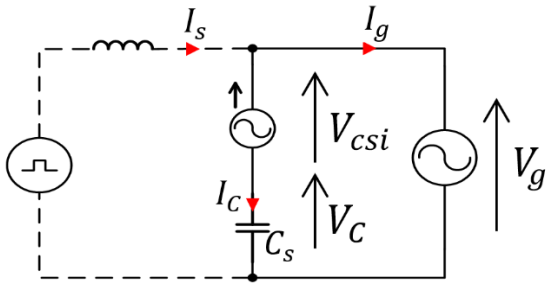
The main VSC design is defined around the choice of output power, which will define the maximum fundamental current amplitude for a given grid voltage level. The current ripple produced by a three phase converter can vary depending on the topology and corresponding modulation strategy. Assuming an integer ratio between the VSI switching frequency and the grid

frequency, the instantaneous current ripple amplitude will vary depending on the instantaneous modulation depth but with the resulting pattern over a fundamental cycle remaining identical. Similarly, the maximum switching ripple amplitude is calculated based on the maximum duty cycle and DC link voltage level for the corresponding modulation strategy [9, 104, 108]. The design requirement is to limit the maximum current ripple to a percentage of the peak to peak fundamental current by choosing an appropriate interface inductance L_1.

The modulation strategy will therefore influence the interface inductor size for a given maximum current ripple level. Once L_1 is chosen, the modulation strategy will not alter the design considerations for the CSI. The amplitude of the maximum current ripple which needs to be cancelled by the CSI will subsequently define the maximum CSI current rating.

3.3.2. Series Capacitor Design

As one of the main components in this topology, the design of the series capacitance is critical in the sizing of the CSI both in terms of current and voltage ratings. The voltage stress of the CSI, defined by its peak line to line voltage, consists of the fundamental and switching voltage harmonics. Assuming the validity of the superposition principle, the analytical design can be considered separately at the fundamental and VSI switching frequencies. The maximum CSI voltage stress is given by the addition of the maximum voltages at the two frequencies considered.



Where $V_g = V_{csi} + V_C$ and $I_{csi} = I_C$

Fig 3-3: Hybrid Circuit Single Phase Equivalent at the Fundamental frequency

At the fundamental frequency, the grid voltage is shared between the CSI and series capacitor based on the injection of the current I_c as shown in Fig 3-3. To explain the approach to the voltage reduction strategy, the next section will focus on the fundamental frequency equivalent circuit where the control approach is explained using phasor diagrams. As the desired CSI current is injected per phase, the control has been designed considering the line to neutral voltage with the equivalent reduction also reflected on the line-line voltage stress assuming balanced conditions.

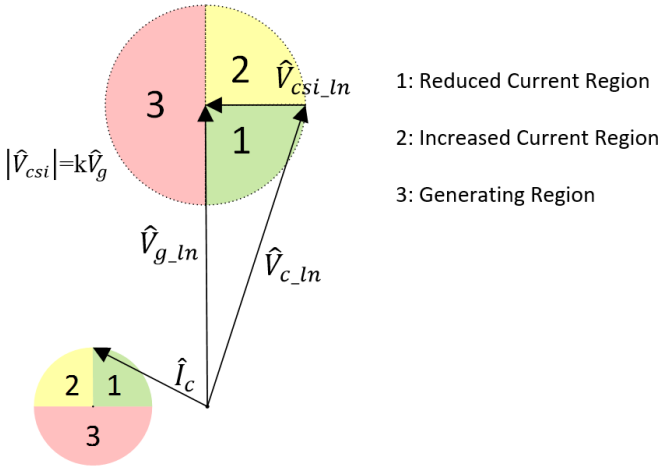


Fig. 3-4: Fundamental frequency phasor diagram showing possible operating regions

Fig. 3-4 shows the fundamental frequency phasors for the system voltages where V_g signifies the peak line to neutral grid voltage, V_{csi} the CSI voltage drop with V_c being the capacitor voltage and I_c the capacitor current which is perpendicular to the voltage. The objective is to minimise the CSI fundamental voltage drop to a fraction "K" of the grid voltage. This will result in a circular locus for the CSI voltage vector with radius K*Vg having as origin the tip of the grid voltage. This leads to a corresponding circular locus for the CSI current I_c phasor as shown in Fig. 3-4. (e.g. K=0.1 corresponds to a CSI fundamental voltage reduction to 10% of the grid voltage). This circle can be divided into three operating regions. Region 3 signifies the generating region. Given that the CSI active power is absorbed from the AC side, operation in Region 3 is impossible. Although operation in Region 2 is possible, it requires a larger capacitor current (as well as series capacitor voltage) for the same fundamental CSI voltage stress compared to Region 1, making it undesirable. Operation should therefore be limited to the quadrant shown as Region 1.

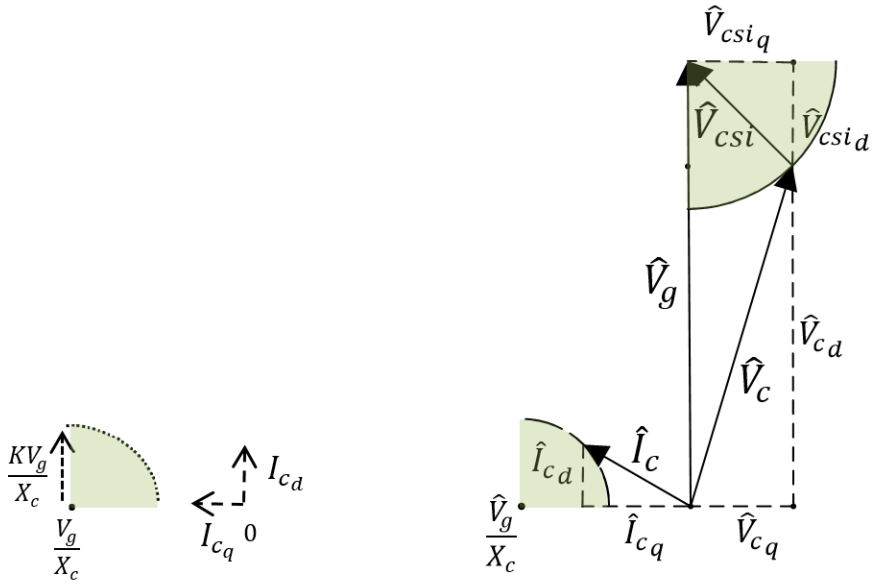


Fig. 3-5: Fundamental frequency phasor diagram showing synchronous reference frame dq components (right) and zoom in on current circle showing the radius and placement.

The synchronous reference frame dq components for operation within Region 1 (green) are shown in Fig. 3-5. The zoom-in on the current circle reveals that for a given voltage reduction coefficient K, both the diameter and centre of the circle are scaled by the capacitance C_s. As a result, at the fundamental frequency the choice of a smaller capacitance is favoured due to the smaller fundamental current requirement for a given voltage drop.

The boundary conditions for operation within Region 1 must also be considered. Fig. 3-6 shows the two corresponding limits for maximum and minimum operating limits for the capacitor voltage and current. For each case the boundary conditions are shown below the phasor diagrams and the amplitude of the capacitor current is shown by the following equations. The active current component Ic_d, contributes towards delivering active power to the CSI DC-link and will be zero in a lossless situation (operating limit 1). The reactive current component Ic_q contributes towards the active capacitor voltage (Vc_d) defined by the circle limit and is used to control the CSI voltage drop within the operating quadrant. At operating limit 1, the current amplitude reaches a minimum; contributed only by the reactive component which also leads to a minimum capacitor voltage amplitude (only active).

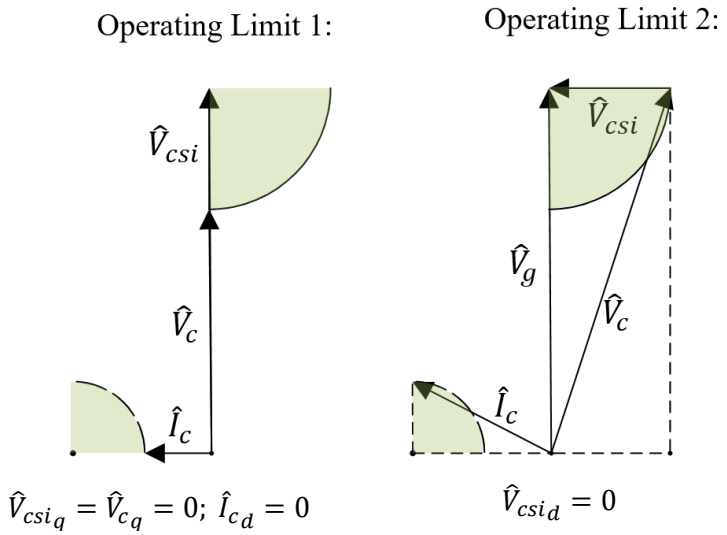


Fig. 3-6: Phasor diagram showing operating limits for maximum and minimum current for operation within region 1.

The amplitude of the minimum possible series capacitor current which occurs at operating limit 1 is given by:

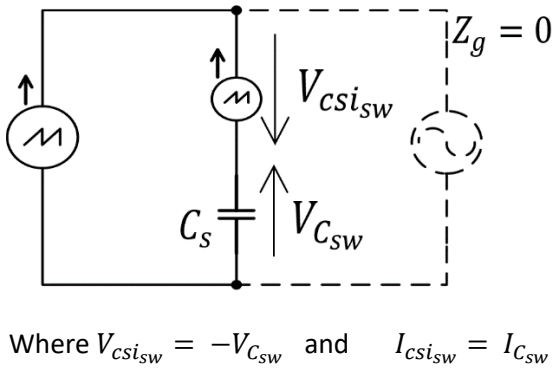
$$|\mathrm{I_c}| = \mathrm{I_{c_q}} = \frac{(1-\mathrm{K})\hat{\mathrm{V}}_{\mathrm{g}}^{\mathrm{ln}}}{\mathrm{X_c}} \qquad \text{(Eq.1)}$$

The maximum possible active power is absorbed by the CSI at operating limit 2 where the maximum permitted active current component will lead to the maximum possible series capacitor fundamental current and voltage. The maximum fundamental voltage and current stress will also define the component rating. At this limit, the CSI voltage will be purely reactive while the calculated peak fundamental current is given by:

$$|\mathrm{I_c}| = \frac{\sqrt{(\mathrm{K}^2+1)}\hat{\mathrm{V}}_{\mathrm{g}}^{\mathrm{ln}}}{\mathrm{X_c}} \qquad \text{(Eq.2)}$$

The second part of the series capacitor design considers the circuit at the VSI switching frequency. The single phase equivalent circuit at the VSI switching frequency is shown in Fig 3-7. Under the assumption of negligible grid impedance, the voltage ripple caused by the switching frequency harmonics is shared equally across the series capacitance and auxiliary bridge. This amplitude is inversely proportional to the capacitance:

$$\mathrm{V_{csi_{sw}}^{ln}} = |\mathrm{I_{sw}}|\mathrm{X_c} = \frac{|\mathrm{I_{sw}}|}{\omega_{sw}\mathrm{C_s}} = -\mathrm{V_{c_{sw}}^{ln}} \qquad \text{(Eq.3)}$$



Where $V_{csi_{sw}} = -V_{C_{sw}}$ and $I_{csi_{sw}} = I_{C_{sw}}$

Fig 3-7: Hybrid Circuit Single Phase Equivalent at the VSI Switching Frequency

Considering the VSI switching frequency equivalent circuit and the relationship given by (Eq.3), a larger series capacitance is favoured for minimisation of the voltage harmonics across the CSI. Given the multi-variable dependency of the harmonic content present in the current ripple, accurate modelling in the frequency domain would be an arduous task requiring the estimation of amplitude and phase per harmonic. The assumption that all the ripple amplitude will occur at the switching frequency therefore constitutes a worst case scenario considering that higher harmonic orders will produce lower voltage stress across the capacitance. This simplified approach thus provides enough margin to account for the variability which could be observed in current ripple profiles under different modes of operation.

Given that the apparent power S, processed by the VSI in the three phase system is given by:

$$S = \sqrt{3}\mathrm{I}_{\mathrm{s}}^{\mathrm{RMS}}\mathrm{V}_{\mathrm{g}}^{\mathrm{RMS}} \quad \text{(Eq.4)}$$

And the reactive power Q associated with the series capacitor is given by:

$$Q = \frac{\mathrm{V}_{\mathrm{g}}^{\mathrm{RMS}^2}}{\mathrm{X}_{\mathrm{c}}} = j\omega C_s \mathrm{V}_{\mathrm{g}}^{\mathrm{RMS}^2} \quad \text{(Eq.5)}$$

Then, by relating the ratio of Q/S will result in the following equation to calculate the maximum capacitance.

$$\mathrm{C}_{\mathrm{s}_{\mathrm{max}}} = \left(\frac{\mathrm{Q}}{\mathrm{S}}\right)\frac{\sqrt{3}\mathrm{I}_{\mathrm{s}}^{\mathrm{RMS}}}{\mathrm{V}_{\mathrm{g}}^{\mathrm{RMS}}\omega} \quad \text{(Eq.6)}$$

The minimum capacitance is based on choosing a maximum line-neutral CSI voltage at the VSI switching frequency. The equation is shown below, where I_{sw} is the maximum expected amplitude of the VSI current ripple.

$$\mathrm{C}_{\mathrm{s}_{\mathrm{min}}} = \frac{|\mathrm{I}_{\mathrm{sw}}|}{\omega_{\mathrm{sw}}|\mathrm{V}_{\mathrm{c}_{\mathrm{sw}}}|} \quad \text{(Eq.7)}$$

The choice of series capacitor is therefore a compromise between ensuring a limited harmonic voltage drop and maintaining a low fundamental current demand. As the series capacitor voltage drop is proportional to the reactive current component injected by the CSI, the maximum capacitance limit can be chosen by imposing a limit on the maximum reactive power (Q) produced by the series capacitors as part of the hybrid system assembly (Eq.6) while the minimum is based on limiting the voltage ripple caused by the switching harmonic current to be cancelled (Eq.7). The selected capacitance therefore ensures that the peak voltage will not exceed the device ratings with limited CSI reactive power requirement.

3.3.3. CSI AC Filter Design

The CSI output filter design is restricted by the choice a parallel decoupling capacitor C_p which has to be as small as possible to limit the circulating current based on the ratio to capacitor C_s (Eq.8) but needs to be large enough to provide sufficient smoothing of the PWM currents. The filter inductance L_f is subsequently chosen based on imposing a suitable cut-off frequency, ideally less than half of the CSI switching frequency, to give sufficient attenuation of the PWM ripple.

$$\frac{I_{c_{s\,fund}}}{I_{c_{p\,fund}}} = \frac{|V_{c_{max}}|C_s}{|V_{csi_{max}}|C_p} \qquad \text{(Eq.8)}$$

A typical open loop filter response is shown in Fig 3-8 reflecting the ratio of I_{csi} (PWM current produced by the CSI) to the series capacitor current I_c. Increasing the ratio of C_p to C_s will lead to an increased negative offset (caused by the bleeding current) that needs to be compensated to achieve accurate VSI anti-ripple synthesis which occurs in the filter linear region. The damping resistance R_f is calculated to provide sufficient damping at the filter resonant frequency with parallel placement favoured in this application due to lower losses as well as the requirement of negligible phase shift within the bandwidth of interest (up to 5kHz). On the other hand, for the same resonance damping level, parallel placement of R_f may result to reduced attenuation at the CSI switching frequency. Finding the ideal filter values may take a few iterations until the design criteria shown in Fig 3-2 are met. Given the high cut-off frequency, the small size of the filter inductance is expected to have a very small effect on the CSI voltage drop at the fundamental and VSI switching frequency.

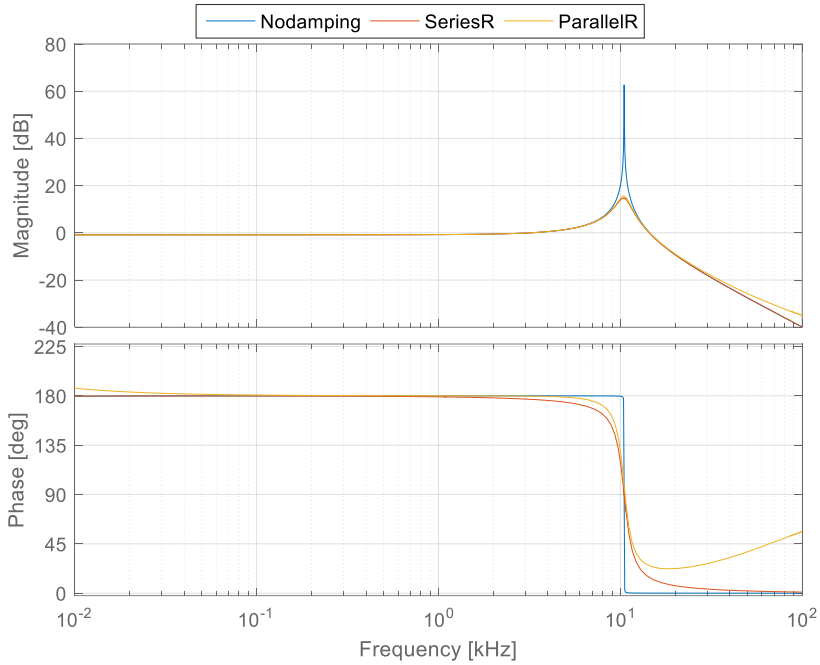


Fig 3-8: Bode diagram showing output filter response (I_{csi}/I_c) with different damping options.

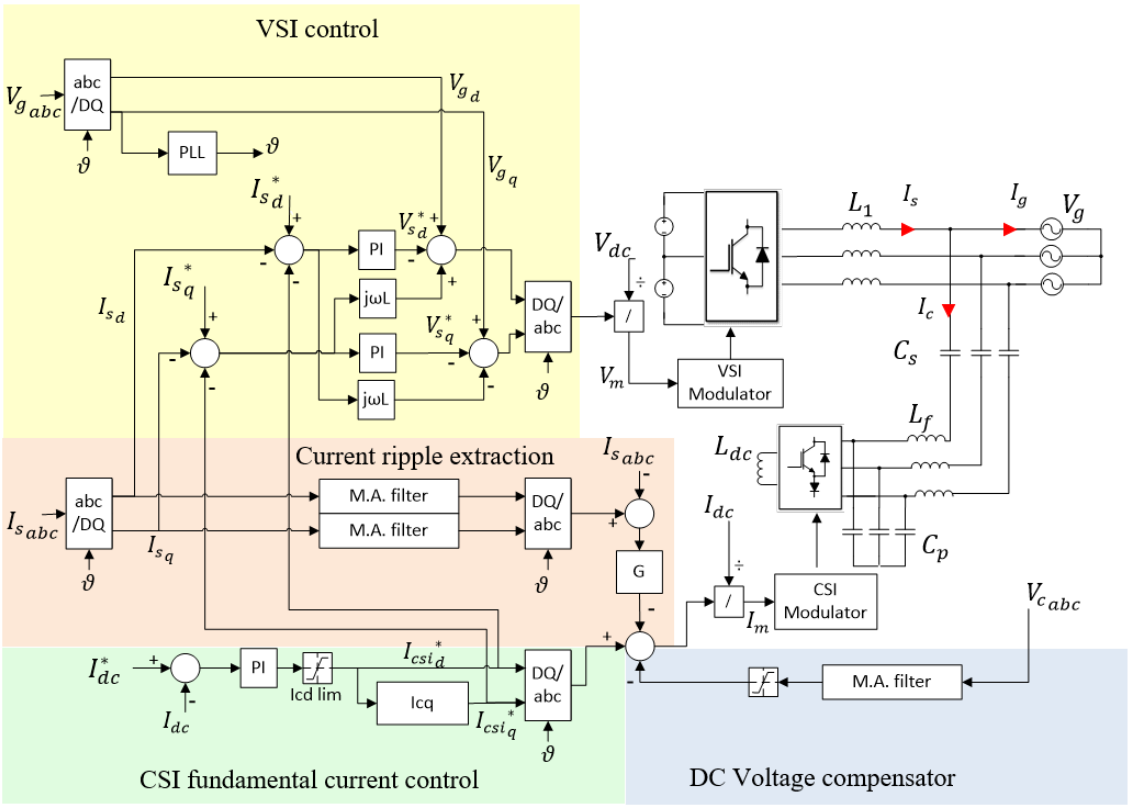


Fig. 3-9: Control scheme of the hybrid assembly

3.4. Control Circuit

The proposed control for the hybrid topology is implemented as shown in the control diagram in Fig. 3-9 where the main sub-sections of the controller are highlighted. The operation, generic requirements and characteristics for each segment of the control are described in the next section.

3.4.1. CSI Fundamental Current Reference Synthesis

The fundamental current component is calculated in the *dq* rotating frame with the active component contributing towards maintaining the DC-link current above the peak of the AC current reference. The DC link current controller determines the active current requirement for the CSI while the fundamental reactive component is calculated using (Eq.15) based on the current locus trajectory for to achieve a required fundamental voltage drop.

For operation within the desired operating region shown in Fig. 3-5 and by using Pythagorean mathematics, the VSI voltage is given by:

$$V_{csi} = \sqrt{{V_{csi}}_q{}^2 + {V_{csi}}_q{}^2} \quad \text{(Eq.9)}$$

By limiting the maximum CSI voltage to a fraction K of the grid voltage:

$$V_{csi} = KV_g \quad \text{(Eq.10)}$$

Since for operation within Region 1

$${V_{csi}}_q = -{V_c}_q \ and \quad {V_{csi}}_d = V_g - {V_c}_d \quad \text{(Eq.11)}$$

The equation of the CSI voltage can be rearranged as:

$$(KV_g)^2 = (V_g - {V_c}_d)^2 + (-{V_c}_q)^2 \quad \text{(Eq.12)}$$

The series capacitor dq voltages can be related to the current by the equations:

$${V_c}_q = {I_c}_d X_c \quad and \quad {V_c}_d = {I_c}_q X_c \quad \text{(Eq.13)}$$

Which can be substituted in the previous equation to result to

$$\left(KV_g\right)^2 = \left(V_g - I_{c_q}X_c\right)^2 + \left(I_{c_d}X_c\right)^2 \quad \text{(Eq.14)}$$

The equation can then be rearranged to its final form, as used in the control system:

$$\mathrm{I_{c_q}} = \frac{\hat{\mathrm{V}}_{\mathrm{g}}^{\mathrm{ln}} - \sqrt{\left(\mathrm{K}\hat{\mathrm{V}}_{\mathrm{g}}^{\mathrm{ln}}\right)^2 - \left(\mathrm{I_{c_d}X_c}\right)^2}}{\mathrm{X_c}} \quad \text{(Eq.15)}$$

In order to maintain operation within the desired operating quadrant as shown in Fig. 3-5, and prevent a possible calculation error, resulting from a negative root if the second term exceeds the first, the active current component has to be limited as shown in (Eq.16).

$$\left|\mathrm{I_{c_d}}\right| \leq \frac{\mathrm{K}\hat{\mathrm{V}}_{\mathrm{g}}^{\mathrm{ln}}}{\mathrm{X_c}} \quad \text{(Eq.16)}$$

The DC link controller needs to be sufficiently slow to avoid rapid variations in the *dq* current components, something which could lead to a voltage disturbance. Due to the slow nature of the controller, it is possible to feed the fundamental component CSI reference current to the VSI controller. The controller is sufficiently fast to compensate for the reactive power that is inherently injected by the auxiliary bridge and can therefore maintain a high output power factor on the grid side of the converter system.

Finally, the dq reference output currents are transformed into the abc equivalent currents by an inverse Park transformation. The angle is supplied by a Phase Locked Loop (PLL) which must be synchronised to the grid voltages. The angle is also used for all other Park/inverse Park transformations in the control system. Given that the CSI dq current control is performed in open loop, the output will be purely sinusoidal assuming no distortion is present in the angle signal.

3.4.2. Current Ripple Extraction

The requirement for the current ripple reference synthesis is the rejection of the fundamental current component whilst maintaining negligible phase shift for all higher order VSI switching harmonics. Given the close proximity of the fundamental frequency to the VSI switching frequency this requirement would be challenging without using a complex filter design which would also be computationally demanding for implementation at the high CSI switching frequency. In the proposed method, the current ripple reference is created by extracting the fundamental current component (and ideally any low order harmonics present) from the measured VSI converter currents $I_{s\,abc}$. To provide accurate tracking of the fundamental current component, a moving average filter is used to extract the average amplitude of the I_s dq currents which is then transformed into the filtered fundamental current abc current components. The moving average window design is discussed in §3.6.3. Finally the ripple reference is multiplied by the factor given in (Eq.17) which is an approximation used to compensate for the fraction of the CSI current that is trapped by the CSI filter capacitors C_p.

$$G = 1 + \frac{C_p}{C_s} \qquad \text{(Eq.17)}$$

3.4.3. DC Voltage Compensator

Given that a zero sequence current component cannot be synthesised in a three wire configuration, the CSI modulator will automatically reject any zero sequence or symmetrical DC current components from the three phase reference currents. Furthermore the connection of the CSI using series capacitors which theoretically exhibit infinite impedance at zero frequency should prevent any DC current synthesis. In practice however, low frequency current subharmonics could still be synthesised and for the purposes of this investigation they are approximated as DC component. In the case of asymmetrical DC current synthesis, combined by a lack of any additional resistances in the circuit, a DC voltage drift could occur where the CSI and series capacitor voltage offset will diverge from zero thus increasing the maximum voltage stress on the CSI. Practically, placing a parallel resistance (in the range of tens of kΩ) to the series capacitor provides a path for any DC

current to flow towards the grid, while the resistance also dissipates any DC component caused during large AC side transients.

In a realistic implementation the main source of DC voltage disturbances is caused by residual DC components injected in the current ripple reference. With the current ripple extraction method outlined in the previous section, where the fundamental component is extracted from the three phase VSI currents (I_s), the presence of any DC component in current I_s, means that a disturbance will propagate through as a reference to the CSI and therefore requires special consideration. The proposed compensator, used to mitigate any DC voltage component requires the measurement of either the CSI or series capacitor phase voltages. A moving average filter with a large window is used to extract any DC voltage offsets from the three phase voltages which are then scaled down and fed to the CSI reference signals. One disadvantage is that the compensator may worsen the transient behaviour by causing additional small DC disturbances, although these should not lead to dangerously high device voltage levels.

3.4.4. VSI Control

The VSI control is performed using a typical VSI control scheme operating in the *dq* rotating reference frame which is synchronised with the grid voltage. Given that in this particular implementation the VSI is purposefully designed to operate with large AC current ripple, the cross coupling terms, which are typically used to aid transient performance have been found to have a negative role in the presence of residual oscillations in the dq currents and should be omitted in that case. The VSI could theoretically also operate in open loop and should not alter the overall system operation from a CSI point of view. In the scenario that the two converters are not running independently, the feedforward of the CSI dq reference currents, mentioned in §3.4.1, could be used. For the reactive component, this will provide compensation for the series capacitor reactive current controlled by the CSI, associated with the CSI voltage reduction, to achieve unity power factor at the point of common coupling (PCC).

3.5. Medium Voltage Hybrid System Design

The design procedure for a 1.9MVA system has been followed at MV levels to investigate the validity of the idea. The system has been designed considering a MV grid of 3.3kVrms line-to line and 330Arms rated line main converter current. The initial design specifications are given below in Table 3-I .

Table 3-I: Specifications for simulated Hybrid Converter Medium Voltage Design

$V_{g\,L-L}$	I_g	$V_{g\,ph}$	S	$\frac{\Delta I_{max}}{2}$	f_{sw}^{VSI}	f_{sw}^{CSI}
3.3 kVrms	330 Arms	2.7 kVpk	1.89 MVA	94A	1kHz	30kHz

The VSI maximum current ripple has been limited to 20% of the peak to peak maximum current giving a maximum current ripple amplitude of 94A. The reactive power has been limited to 20% of the apparent power for the system which based on the above design procedure gives a maximum capacitance of 110µF. The maximum voltage stress has been chosen as 20% of the line grid voltage which practically translates to a low voltage rated CSI (under 1kV) that can use 1.2kV devices. As an initial design point, the maximum switching and fundamental voltage stresses have been divided equally at 10%. The above design requirements give a series capacitance range of 55-110µF.

3.5.1. Optimisation Results

As mentioned previously, an increased capacitance could potentially result in lower voltage stress on the auxiliary CSI Bridge at the cost of increased DC link current due to the largest 50Hz current requirement. A simplified analytical system model has been used investigate the implication of varying the series capacitance on achieving minimum installed power in the converter switches. The added installed power is calculated by comparing the peak voltage and current stress on the CSI over the VSI peak voltage and current stress while also considering the number of switches Nsw as given by (Eq.18).

$$Added\ Installed\ Power\ [\%] = \frac{\#\ Nsw_{CSI} * \widehat{V_{CSI}} * \widehat{I_{CSI}}}{\#Nsw_{VSI} * \widehat{V_{VSI}} * \widehat{I_{VSI}}} * 100 \quad \text{(Eq.18)}$$

For the VSI, the peak current stress is given by the AC side current while the peak voltage stress is given by the DC-link voltage level. For the CSI the peak current stress is given by the DC-link current while the peak voltage stress is given by the peak line-line voltage.

This preliminary optimisation has been conducted prior to the circuit development to estimate the circuit potential for minimising the added installed power on the CSI. Due to the nature of the task, a number of assumptions have been taken. The main assumption is that all CSI losses are represented by an equivalent DC-link resistance on the DC link, thus not separately accounting for switching losses. Under the assumption that the CSI efficiency typically ranges from 85%-95% of the apparent power processed, depending on switching frequency, three $R_{dc\text{-}csi}$ steps that correspond to a CSI loss percentage 5-10-15% of the apparent CSI AC power have been considered. As the main consideration is the trade-off between the series capacitance, the DC-link current level and fundamental voltage minimisation, the CSI voltage caused by the VSI switching ripple is only accounted at the 1 kHz switching frequency (Eq.3). Furthermore, the design does not take into account any further voltage drop which would occur across the CSI output filter. A flowchart showing the steps followed is shown in Fig. 3-10 while the results are shown in Fig. 3-11.

Rather than operating within the circle boundaries, the optimisation starts at the designated initial operating point (operating limit 1) using (Eq.1), and then keeps Ic_q constant while calculating the new Ic_d requirement which will increase only the active component of the fundamental CSI voltage. The operation is closer to a linear trajectory tangential to the bottom of the circle instead of the circular trajectory where the fundamental voltage would remain constant. Thus approach was considered more appropriate in order to avoid reaching the saturation point which could be reached for a given V_{csi} fundamental component. (Eq.16)

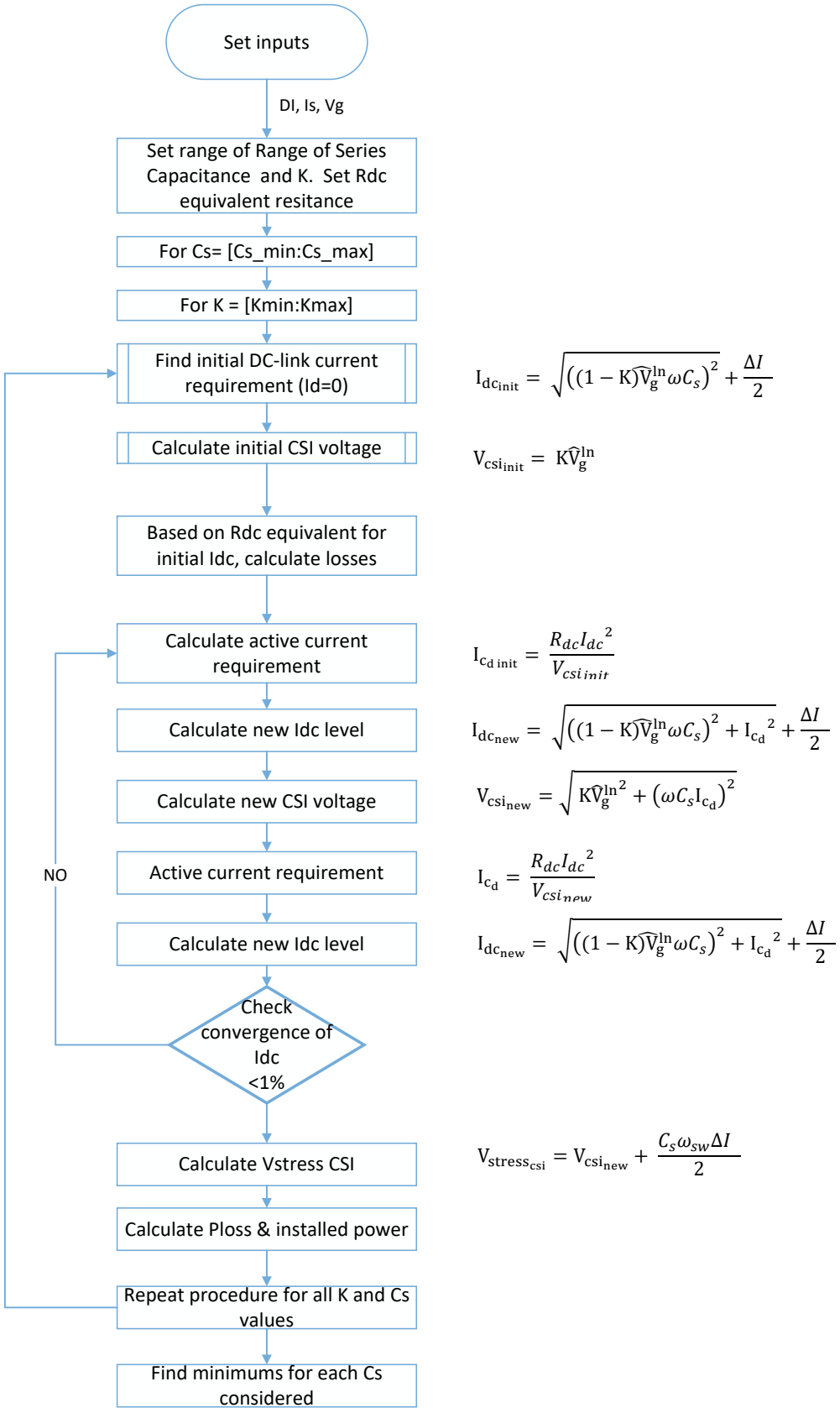


Fig. 3-10: Flowchart representing the preliminary optimisation procedure followed with the corresponding equations on the right.

(a) (b)

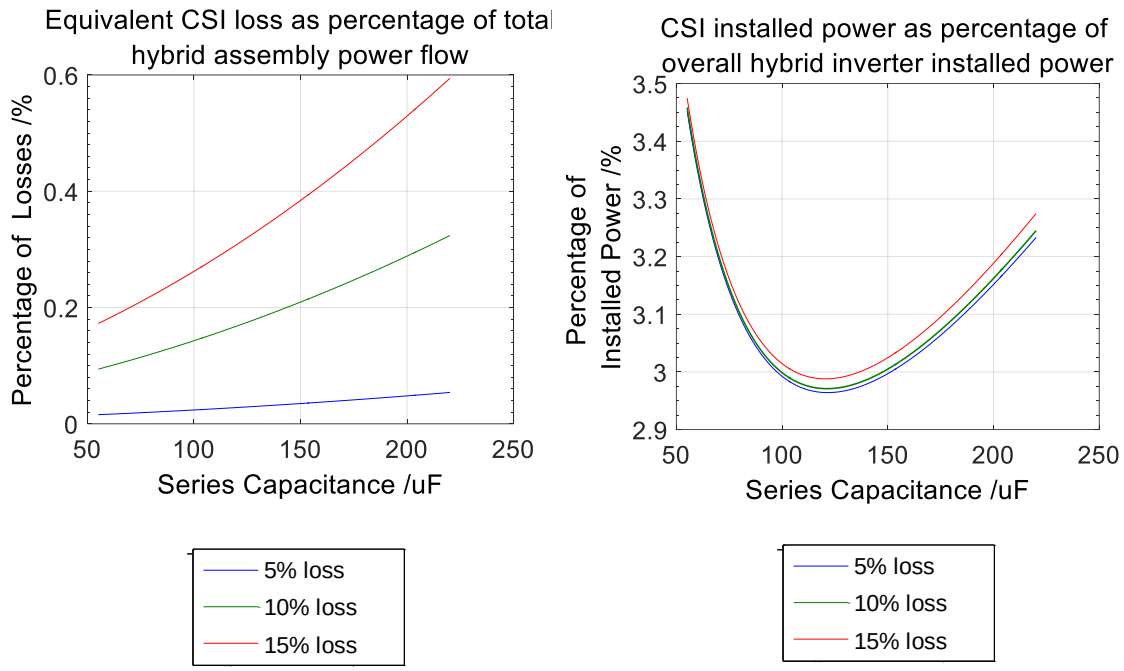


Fig. 3-11: a) CSI Losses as percentage of hybrid system loss and b) Added Installed Power versus size of Series Capacitance at different DC-link resistance equivalent to 5-10-15% loss of processed apparent CSI power.

The resulting added installed CSI power for different $R_{dc\text{-}csi}$ over a wide range of series capacitances, is shown in Fig. 3-11b. It can be seen that the curve reaches a minimum of 3% at around 130μF and overall remains well under 4% throughout the whole Cs range. The gain at minimum installed CSI power is very small (+0.45%) compared to lowest Cs which means that if minimisation of the overall cost (CSI + Cs) is sought, the overall minimum could move towards smaller Cs values if 3x75μF is more expensive than 13% (0.45%/3.4%) of the CSI cost. It can be seen that large variations in the series capacitance have a limited effect on the losses as more AC reactive current will reflect in higher DC-link current. The important finding is that for a given series capacitance, the percentage of added installed power remains largely unchanged.

3.6. Simulation Results for Operation with Ideal Voltage Source

The simulated performance evaluation of the hybrid topology is presented in this section. The simulations have been carried out with the use of PLECS software package which is principally suited for simulation of power electronics. Based on the design exercise, two sets of parameters have been chosen to carry forwards the simulation based study of the hybrid circuit performance to validate the design procedure with the main aim to show the achieved voltage reduction and potential for grid current quality improvement. Finally other aspects which could inhibit the desired performance are discussed and demonstrated.

Table 3-II shows the calculated component parameters used as well as the current limits for each capacitance value considered. In this case the CSI AC filter has been designed for a cut-off frequency of 10 kHz while a parallel filter resistance R_f has been chosen at 10Ω to provide critical damping with the filter response matching the one shown in Fig 3-8.

Table 3-II: Component Parameters and Settings for the Desired Operating Points used in Simulations

C_s min	C_s max	L_f	R_f	L_{dc}
55μF	110μF	23μH	10Ω	20mH
C_p	K	I_c max @55/110 μF	I_{cd} lim @55/110 μF	I_{dc} @55/110 μF
11μF	0.1	47A/94A	4.66A/9.32A	140/184

The dead-time, required to prevent current shoot-through and a short circuit of the VSI DC link capacitor has been set at 1μs, while the overlap, required to prevent an open-circuit of the CSI DC link inductor has been set at 300ns. As will be shown, the dead-time effects are not noticeable on the VSI currents which may be due to the influence being much smaller at low switching frequencies and increase of number of levels.

3.6.1. Steady State Performance

The steady state operation is presented for both capacitor values considered to ensure the validity of the fundamental grid voltage reduction scheme and allow for direct comparison of the relative amplitudes. The performance is presented at steady state operation by showing the line-to-line CSI voltages (a), the line to neutral voltages across the Series Capacitor and the CSI input filter capacitors (b), the currents in corresponding main inductor (L_1) (c), the CSI currents (d) and the cumulated resulting grid output currents (e) for the two values of series capacitance.

Fig. 3-12 shows the steady state waveforms for two 50Hz cycles during fundamental current synthesis, where the auxiliary inverter operates with a fundamental voltage drop coefficient K=0.1 prior to ripple cancellation. The set of waveforms on the left column, corresponding to the minimum capacitance (Cs=55μF) show the CSI operating with a DC-link current of 140A whilst producing a fundamental AC current of around 40A whilst when the capacitance is doubled (right column), the DC current reference is increased to 184A with a fundamental AC component of around 85A required to achieve the desired voltage drop.

The fundamental current passing through the series capacitor in each case results in a series capacitor voltage of 2490V for a grid voltage of around 2.7 kV (not shown). The phase CSI and series capacitor voltages are plotted together to clearly show the proportion of reduction.

The corresponding reduced CSI voltage stress in this mode of operation is contributed by the fundamental component and the CSI switching ripple created by the CSI current. Due to the higher DC-link current, operation at maximum capacitance will have a larger 30 kHz ripple reflected on the both the CSI AC currents I_c, and voltages and which in combination with the CSI modulator used (§5.2.1) results in the distinct line-line CSI voltage shape.

As a result of this added ripple, at 110uF, the peak line-line voltage reaches 470V (10% of V_{grid}), but with the negative peak recorded at -530V (11%) whilst for the minimum capacitance the CSI voltage peaks have been measured at 410V and -438V. Despite this small discrepancy the comparison with the theoretical values given in Table 3-II to the simulated values for CSI AC

current amplitude I_c and fundamental voltage reduction (10%) are in line with the theoretical expectations.

The main converter is following the 470A reference current required to output approximately 1.89 MW to the grid. As the ripple cancellation is disabled, the large VSI current ripple, which increases the peak current to 555A, propagates to the grid. The effect of the ripple cancellation is presented in Fig. 3-13, showing the hybrid system in full operation, by the absence of any VSI switching ripple in the output I_g currents which remain sinusoidal (with most of the remaining ripple at the 30 kHz CSI switching frequency).

The addition of the voltage drop across the series capacitors caused by the CSI current (current anti-ripple) passing, can be seen in inverse proportion to the series capacitance where the peak Series Capacitor voltage V_c reaches almost 2.6 kV for Cs of 110μF and 2.75 kV for the smaller capacitance. Due to this additional voltage drop reflected on the CSI voltage, the CSI voltage stress for the minimum capacitance increases to 780Vpk (line-to-line) but remains below the 20% limit of 940V. At the maximum series capacitance considered, the peak stress is decreased further to 650V corresponding to 14% of the peak grid voltage.

As a result it can be concluded that at the minimum capacitance, the required AC side currents of the CSI reach a minimum; reflected by a CSI DC link current reference of 140A. The downside is that the CSI peak voltage stress that accounts for the fundamental and switching voltage components reaches a maximum but remains well below the imposed 20% MV peak limit (940V). Doubling the series capacitance will reduce the voltage stress but requires an increased DC link current level of 184A due to the increased 50Hz reactive current that needs to be synthesised by the CSI to keep constant the fundamental voltage drop across the series capacitor. A secondary aspect also being that for a given CSI AC filter, the increase in dc-link current will also induce an increase in the CSI voltage ripple but this has a smaller impact on the maximum CSI voltage stress.

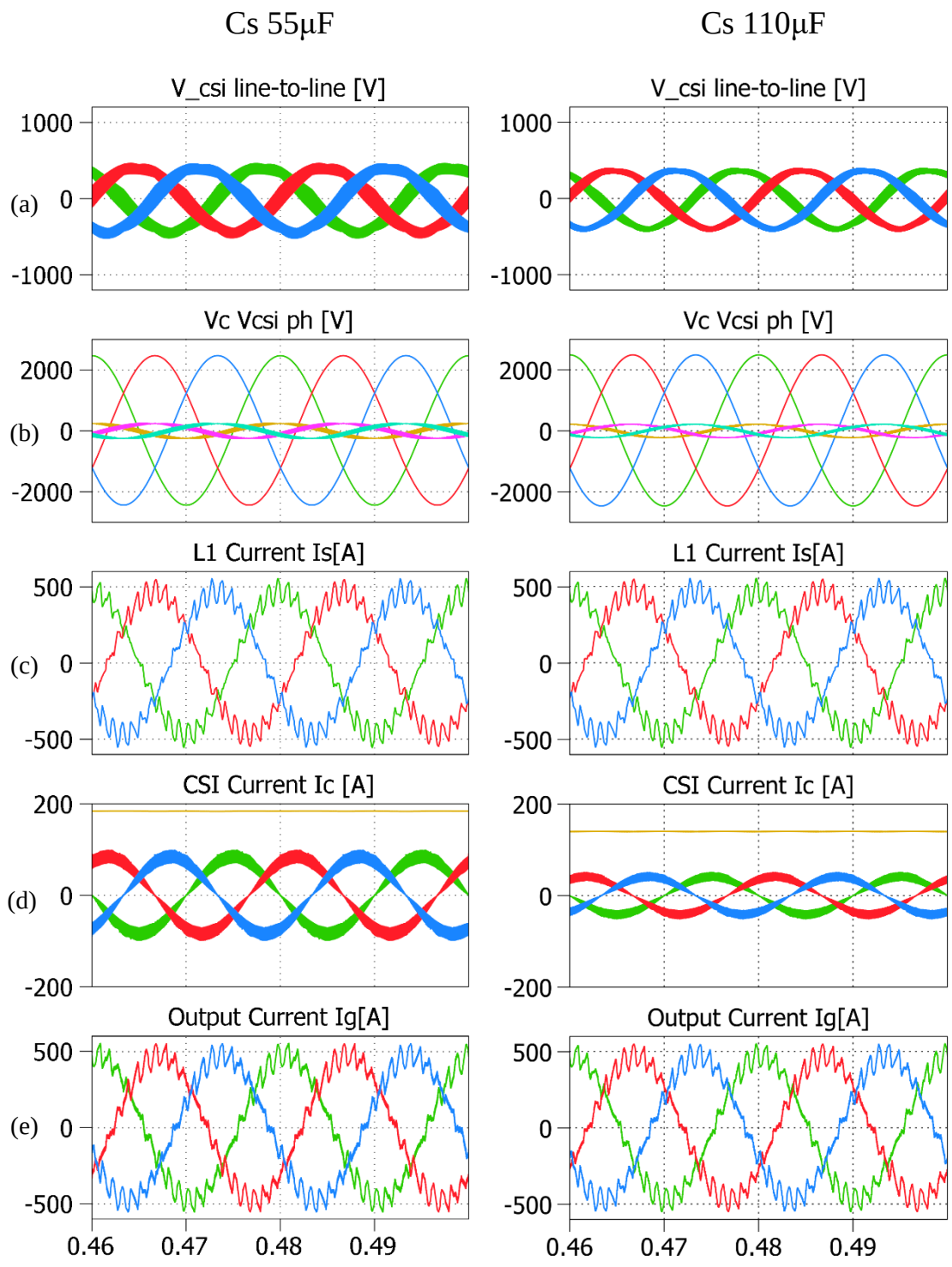


Fig. 3-12: Simulation waveforms during steady state operation before ripple cancellation considering the two series capacitor values a) Line-To-Line CSI Voltages; b) Line-To-Neutral CSI And Series Capacitor Voltages; c) Input (Main Converter) Current through the Interface Inductor (L1). d) CSI Current; e) Cumulated Output Current;

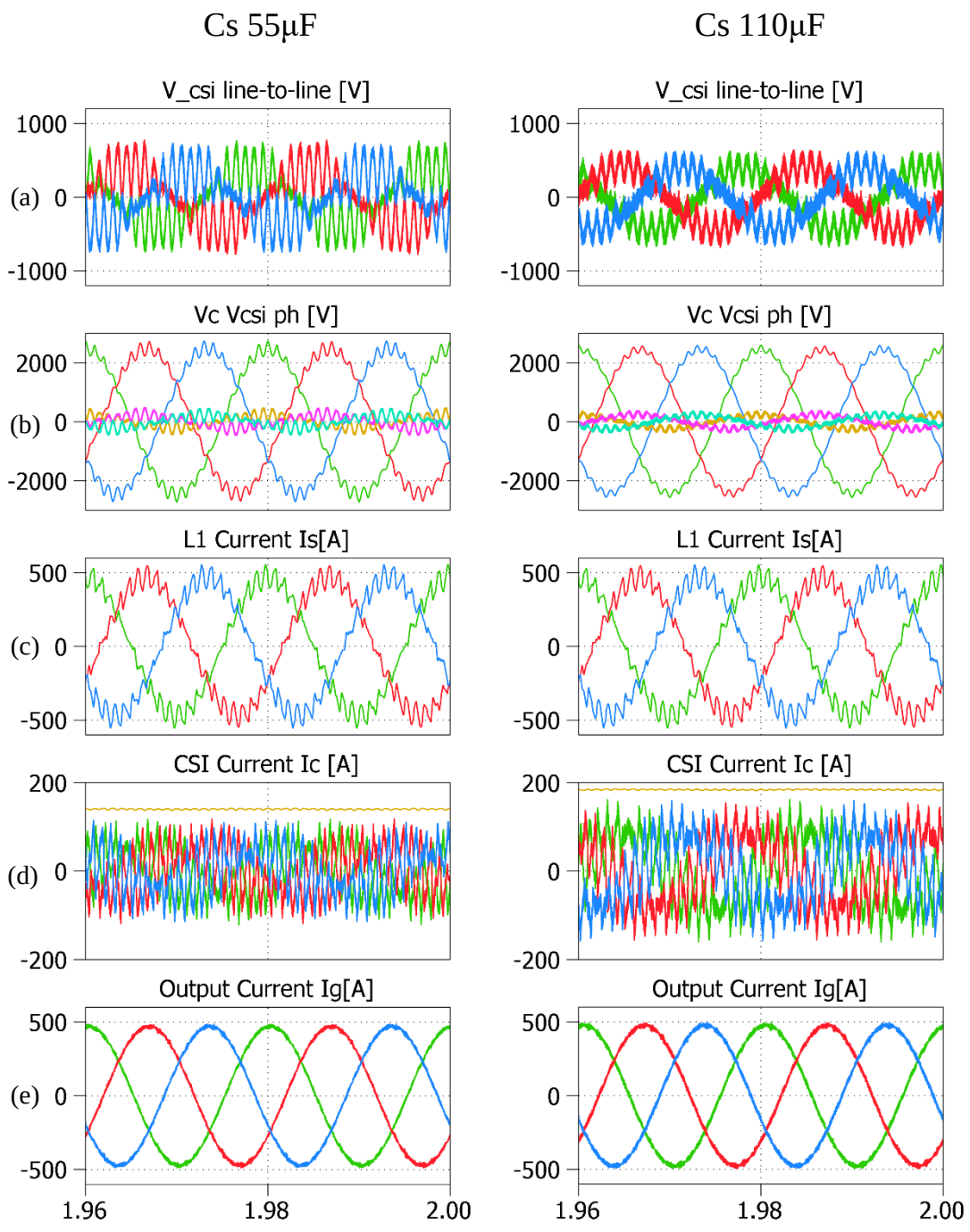


Fig. 3-13: Simulation waveforms during steady state operation considering the two series capacitor values a) Line-To-Line CSI Voltages; b) Line-To-Neutral CSI And Series Capacitor Voltages; c) Input (Main Converter) Current through the Interface Inductor (L1). d) CSI Current; e) Cumulated Output Current;

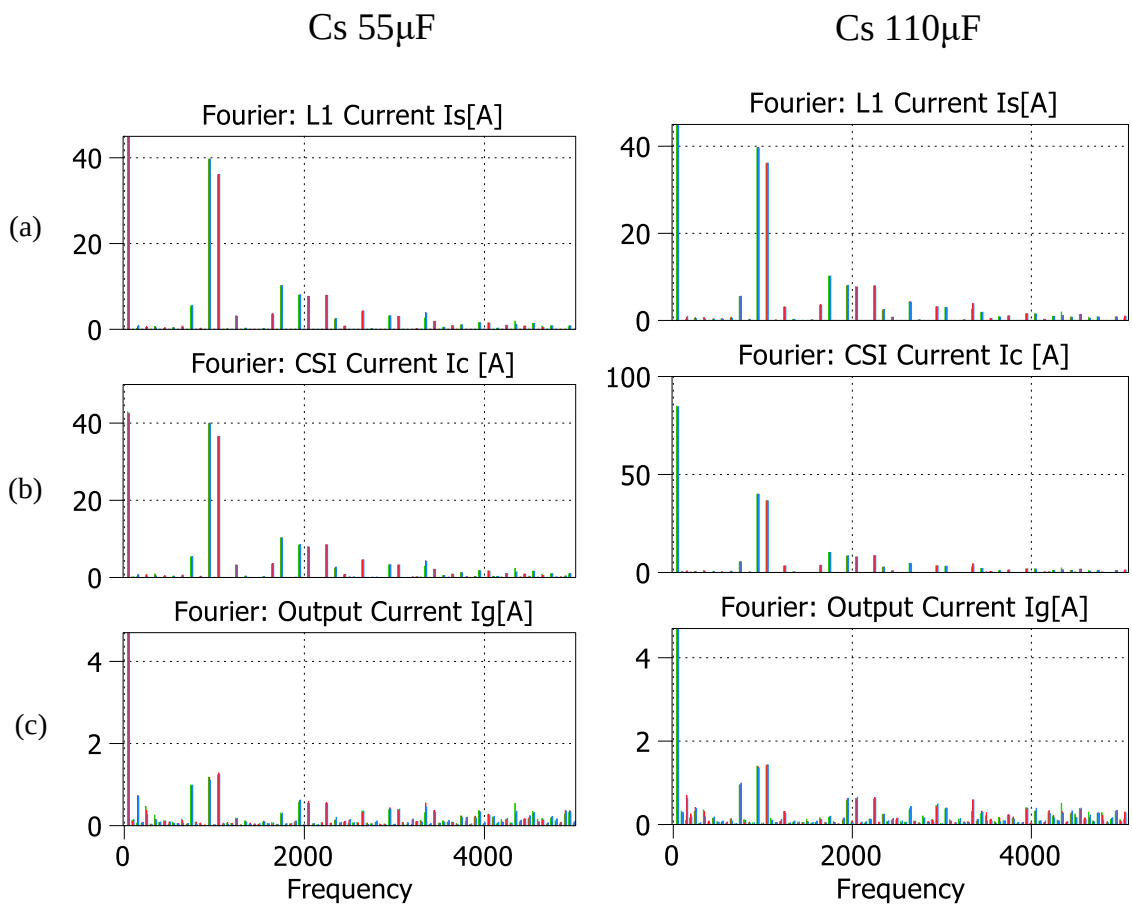


Fig. 3-14a-c: Current harmonic content up to 5 kHz for two series capacitor values in: a) VSI Current (the fundamental current is clamped); b) the CSI Current and c) the zoomed in resulting cumulated grid current (fundamental component clamped)

Table 3-III: Most significant current harmonic amplitudes and corresponding reduction

Frequency	750Hz	950Hz	1050Hz	1750Hz	1950Hz	2050Hz	2250Hz
Is	5.5A	40A	36.5A	10.15A	8A	7.7A	7.9A
Ig Cs=55 µF	1A	1.17A	1.28A	0.3A	0.6A	0.6A	0.55A
Percentage reduction	18.2%	2.9%	3.5%	3.5%	7.5%	7.8%	7%
Ig Cs=110 µF	1A	1.4A	1.43A	0.2A	0.6A	0.6A	0.65A
Percentage reduction	18.2%	3.5%	3.9%	2%	7.5%	7.8%	8.2%

The extent of the current quality improvement can be quantified in the frequency domain where the harmonic content for the VSI current I_s (a), CSI current I_c (b) and the resulting grid current I_g is shown in the Fast Fourier Transformation (FFT) plots in Fig. 3-14 for harmonics up to 5kHz.

Looking at the current harmonic spectrum it can be seen that for both scenarios the main VSI switching harmonics are eliminated with grid harmonic amplitudes under 2A, at levels lower than 1% (4.7A) of the fundamental current processed by the VSI. The biggest amplitude decrease is observed for the 950Hz harmonic which is reduced to from 40A to 1.2A for Cs 55μF and 1.4A for Cs=110uF, at 3% and 3.5% of the original amplitude. A similar percentage reduction can be observed for the 1050Hz harmonic which is reduced to 3.56% (1.28A) and 3.9% of the original amplitude.

At the second harmonic cluster (1950 Hz and 2050 Hz) the percentage reduction is decreased with each harmonic reduced to 7.5% and 7.8% for both capacitance scenarios but with amplitudes at less than 1A. The lowest percentage reduction in both cases is at the 750Hz harmonic which is reduced to 18% (1A) of the original 5.5A. This is attributed to insufficient extraction in the control system where, in this case, a 2ms moving average filter has been used. The comparison between converter and grid current harmonic amplitudes and the associate reduction is shown in Table 3-III for the most significant harmonics based on original amplitude. Overall the results verify the effectiveness of the ripple cancellation as observed in the time domain grid current waveforms.

The amplitude difference between the converter and grid current fundamental frequency components, which have been clamped to focus on the harmonic content , is very small as the majority of the fundamental current injected through the series capacitor is reactive. At the minimum capacitance the fundamental component increases from 470A to 472A while for the maximum capacitance the fundamental component increases from 470 to 476A.

Fig. 3-15 reveals the current harmonic spectrum for frequencies up to 50 kHz to account for the remaining significant current harmonics injected by the CSI. For both scenarios considered, a small harmonic cluster occurs at the CSI AC filter resonant frequency around 10 kHz as expected

from the filter response shown in Fig 3-8. However the local maximum amplitude remains under 2A, at similar levels with the residual harmonics in the 5 kHz range which can be considered negligible.

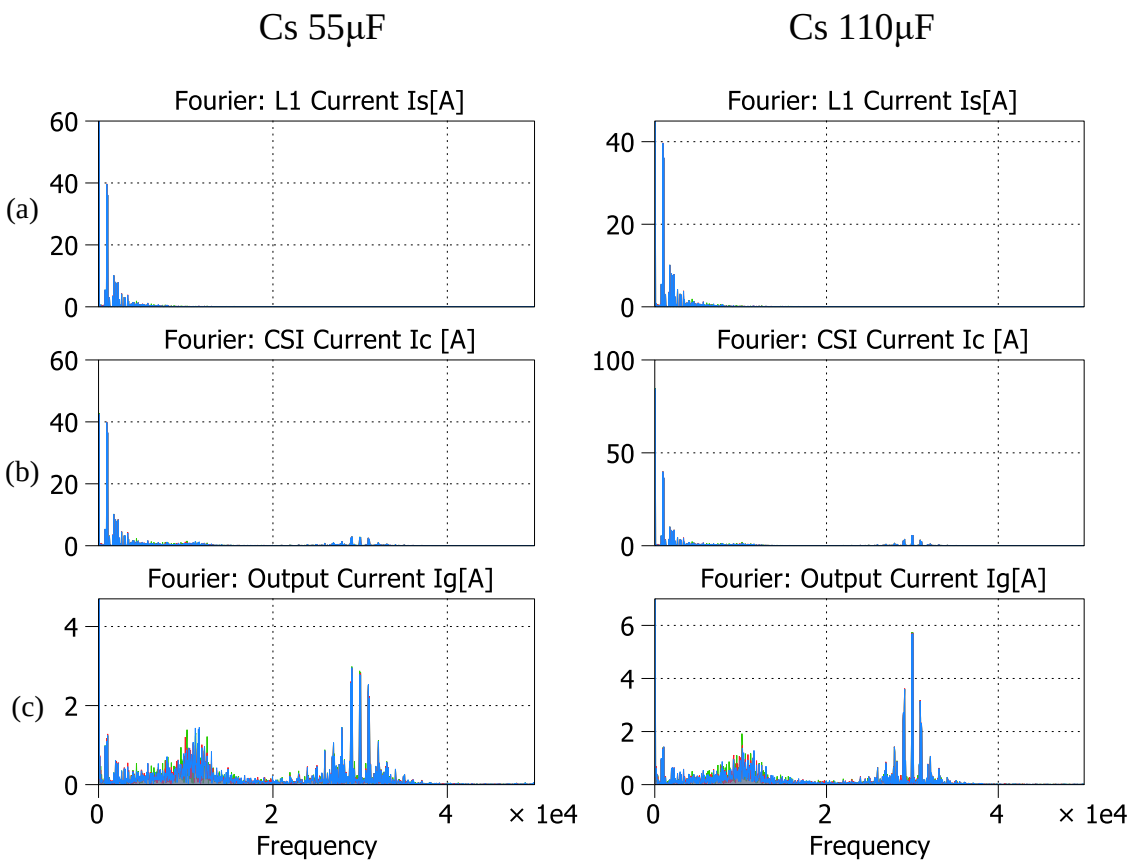


Fig. 3-15a-c: Current harmonic content up to 50 kHz: a) VSI Current (fundamental current clamped); b) the CSI Current and c) the zoomed in resulting cumulated grid current (fundamental component clamped)

The most important remaining amplitudes will occur around the cluster created around the CSI switching frequency of 30 kHz. The maximum amplitude remains below 3A for the minimum capacitance scenario while in the maximum capacitance, due to the higher current processed by the CSI, the cluster reaches up to 5.8A for the harmonics around 30 kHz (±50Hz) which reflects the additional switching ripple seen in the time domain waveforms. In comparison to the fundamental grid current amplitude, this corresponds to only 1.2% while all other grid harmonics remain below 1% of the fundamental current as previously observed.

The effectiveness of the current ripple cancellation is also seen in the grid current Total Harmonic Distortion THD which has been calculated at 2.9% and 2.2% for the two scenarios considered compared to 12.2% on the VSI current. The increase in THD between the two operating points is also accounting for the increase of the switching harmonic cluster at 30 kHz as shown in Fig. 3-15. The CSI switching harmonics would be expected to be naturally contained in the hybrid assembly due to the inductive behaviour of the grid although, as explained in §4.1, this can introduce further LC resonance challenges.

The simulated performance at both operating points shows that the CSI can offer a significant harmonic improvement to the grid currents by cancelling the large switching ripple produced by the VSI which is switching at 1 kHz. This is achieved while also operating at a fraction of the grid voltage stress, showing that the CSI can operate at less than 20% of the peak grid voltage over a wide range of series capacitor choices.

Based on the maximum CSI line-line voltage stress of 780V and a maximum DC-link current of 142A, compared to a 3kV and 555A experienced by the VSI semiconductors, the added installed power by the CSI for the minimum capacitance considered (55μF) is calculated using Eq. 10 at 3.3%. At the maximum capacitance considered, where the maximum DC-link current in steady state reaches 186A with a maximum voltage stress of 650V, the added installed power reaches 3.6%.

Although these values show some discrepancy with the result presented in §3.5.1, which does not account for the added stress at the CSI switching frequency, the overall figure for CSI installed power remains considerably low and satisfies the intended performance objectives.

3.6.2. DC Voltage Compensator Validation

To highlight the requirement, as well as to show the validation of the proposed DC voltage compensator, the following test has been conducted using the maximum series capacitance of 110μF. By evaluating the probable scenario of voltage disturbances being caused by residual DC current components propagating through the current ripple reference signals, a DC offset has been

intentionally fed as a reference to the CSI modulator, measuring at -0.35A, 0.2A and 0.5A on phases A-B-C. No additional resistances have been added to the circuit.

Fig. 3-16 shows the three-phase grid currents I_g, the CSI AC currents I_c along with the DC side current, the line-line CSI voltages and the combined phase voltages for the series capacitor and CSI. The test starts by considering that the DC voltage compensator is disabled, while the CSI is synthetizing only the fundamental current component required to give a 10% fundamental CSI voltage drop.

Current ripple cancellation is activated at t=0.3s revealing that the residual DC current component propagating through the CSI modulator creates a DC voltage offset build-up. On the phase voltage plot it can be seen that the DC voltage drift is reflected per phase between the series capacitor and CSI capacitor voltage with the maximum absolute DC voltage reaching 142V, 1V, and 180V for phases A-B-C. The CSI line-line voltage V_{ca} reaches up to 880V on the positive peak, while the V_{ab} and V_{bc} slightly exceed -800V therefore causing a significant disturbance in the CSI line-line voltages, although not at dangerously high levels where it would exceed the maximum permitted voltage stress. The CSI voltage offset will also create DC link oscillations at the fundamental frequency which reach up to 30A causing the current to peak at 206A. As observed by the grid current however, these oscillations will not affect the CSI AC current synthesis (and by extent the grid current quality) given that the minimum DC link current remains above the maximum ripple reference thus avoiding over-modulation.

The activation of the compensator at t=0.6s creates an immediate albeit slow reduction of the voltage DC offset which approaches zero at t=0.8s with negligible DC levels observed after t=0.9 which is also witnessed by the lack of oscillations on the CSI dc link current which settles at the 184A reference with oscillations less than 5Apk-pk. The results reveal the sensitivity of the fundamental voltage reduction scheme to small current disturbances which could create additional voltage stress across the CSI. As demonstrated, the use of a DC voltage compensator can mitigate the build-up of DC voltage offset and thus protect the semiconductors from any possible overvoltage.

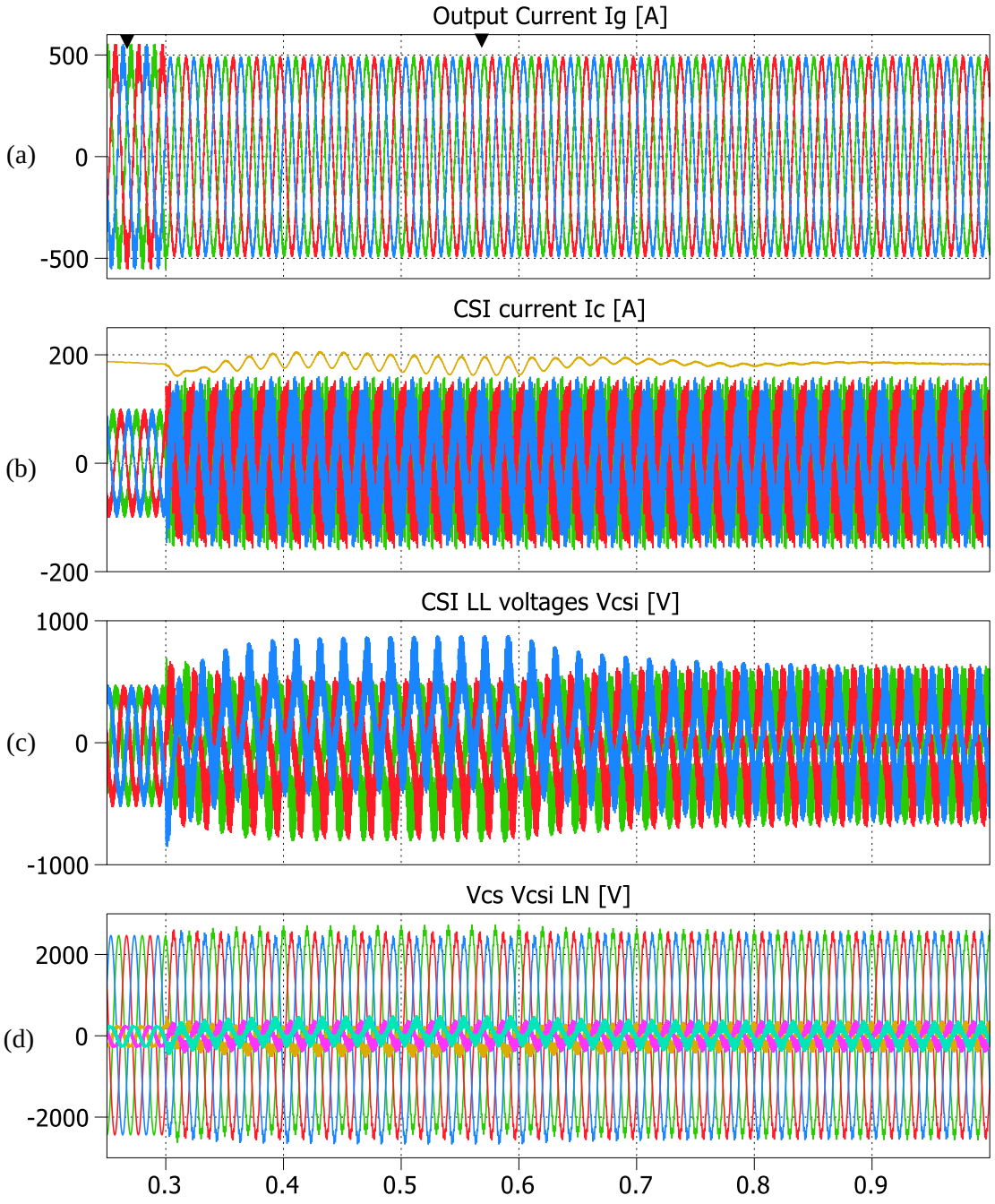


Fig. 3-16: DC voltage compensator validation showing activation of current ripple cancellation at t=0.3s including DC current disturbances and activation of DC voltage compensator at t=0.6s. a) Grid Current; b) CSI Current; c) Line-To-Line CSI Voltages; d) Line-To-Neutral CSI And Series Capacitor Voltages.

3.6.3. Current Ripple Extraction and Transient Performance

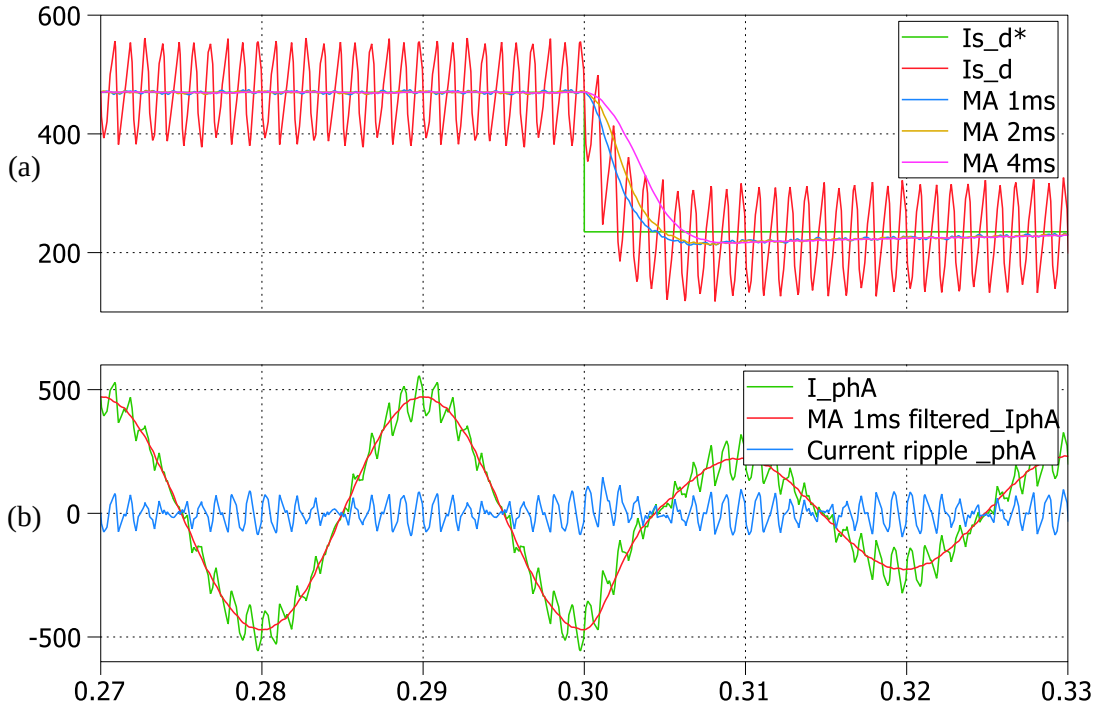


Fig. 3-17: a) Step change in VSI current component; and b) the effect on current ripple extraction.

Although active power filter performance is typically assessed in steady state conditions, the transient performance must also be considered. In the proposed topology the use of the series capacitance which, as previously demonstrated, is particularly sensitive to low order harmonic disturbances creates a further challenge for achieving good transient performance.

The transient response for the VSI active current component I_{s_d} (red) for a step command (green) from full to half rated load is shown in Fig. 3-17 showing that steady state is reached within one cycle (20ms). The output of three different moving average (MA) filters is superimposed for a window of 1ms (equal to the VSI switching frequency) 2ms and 4ms. In order to minimise low order harmonic disturbances propagating to the CSI modulator, the requirement for the current ripple extraction is to follow the I_{s_d} component as close as possible during transients, while ensuring that in steady state no residual oscillations remain on filter output, which would compromise the current filtering capability. Extracting the current ripple against the reference d current value I_{s_d}* or with a larger MA window (4ms) will ensure good current ripple extraction

in steady state but will result in a large error during transients. As a result, the minimum recommended MA window to facilitate accurate transient tracking is suggested at the VSI switching frequency of 1 kHz. The current ripple extraction using a 1ms MA filter window is shown for the Phase A VSI current (Fig. 3-17b) where it can be seen that the step response will still result in a small low order harmonic disturbance in the extracted current ripple the effects of which will be demonstrated in the following transient evaluation.

Fig. 3-18 reveals the transient behaviour for the circuit under different modes of operation using a series capacitance of 110μF to demonstrate the dynamics of the circuit voltages and currents. To capture a more realistic performance of the CSI DC current controller, a resistance of 0.1 Ω has been added to the DC side, which at the nominal 184A current emulates losses of about 3kW which need to be provided by the CSI active current component. The fundamental reactive current required to minimise the CSI AC side voltage is continuously produced according to the requirement while the current ripple cancellation is activated later with intermediate changes in the main inverter load current and the imposed fraction of CSI fundamental voltage drop.

The coefficient of AC voltage reduction "K" which is controlled by the level of reactive current injected through the series capacitors is decreased in steps: 0.2 (modes 1-2), 0.1 (modes 3-6) and 0.05 (mode 7). The AC side CSI current increase can be observed at the beginning of mode 3 showing that at the fundamental frequency, a marginal increase in current (~10A) can provide significant voltage reduction (940V to 470V) for a given series capacitance. The transient evaluation starts by considering that the main converter operates with half the rated current of the main inverter bridge (also in modes 4 and 5) while the rated current is used for modes 2, 3, 6 and 7. VSI load changes occurring during modes 1-4 do not cause any disturbances therefore verifying that, during fundamental frequency synthesis, the CSI is immune to any changes occurring in the VSI and vice versa. On the other hand, changes in the fundamental voltage coefficient K will cause an immediate change of the CSI line-line voltage and as a consequence will create a dip in the CSI dc-link current.

Transition Mode	1	2	3	4	5	6	7
Ripple Cancellation		×			√		
Output current THD		12.2%		24.5%	4.9%	2.9%	
Load Level		full		half		full	
K	20%		10%				5%

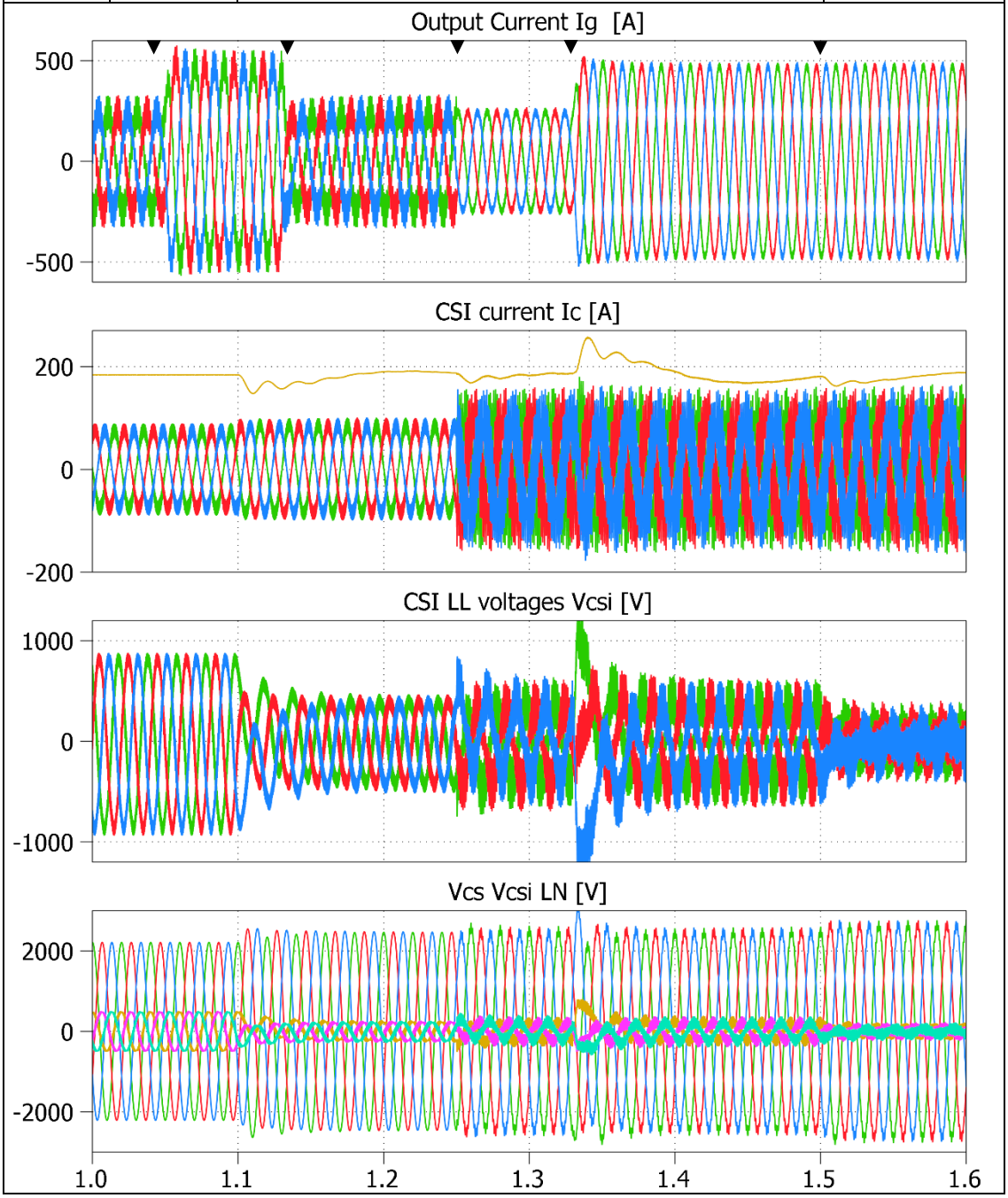


Fig. 3-18: Voltage and Current Transient Behaviour under Different Operating Modes using Cs 110uF

As observed in the previous section, the presence of DC voltage offset created during transients will be reflected as fundamental frequency DC-link current oscillations which however are mitigated within a few cycles.

Current ripple cancellation is activated for modes 5-7 where a significant THD reduction is seen from 25 to 5% at half load and from 12% to 3% for full load. Most significantly, it can be seen that harmonic cancellation can be performed during a large load current step change (mode 6) however it causes large CSI voltage disturbances which also create an overshoot in the DC link current that could potentially damage the CSI semiconductors. Even a small low frequency disturbance in the CSI reference current during the transient (a 10A current increase seen on the CSI AC current profile) could cause a steep voltage increase even though for a small time period. It can be observed that after two cycles, the DC voltage compensator will return the voltages to steady state levels.

Ultimately a clamp circuit should be used to protect the CSI from overvoltage and prevent the overcurrent from occurring but nevertheless; this test shows the requirement of filtering out any DC components and low order harmonics in the current ripple extractor which effectively means a compromise between good steady state operation and high dynamic response. The effect of the decrease of the MA window from 2ms to 1ms is shown in the harmonic content of the grid current in Fig. 3-19 where a 1A increase can be observed for the 750Hz harmonic, although this has a minor impact on the output THD.

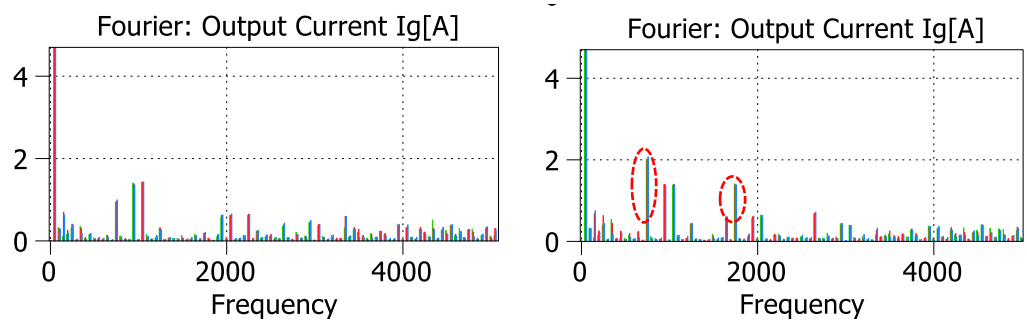


Fig. 3-19: Harmonic content of filtered grid current for moving average filter windows of 2ms (left) and 1ms used for improving transient response (right).

Finally as seen by the step change in mode 7, for the 110μF capacitance considered, a further small increase in the CSI reactive current could provide a further reduction of the fundamental CSI voltage stress to 5% of the grid voltage. Any reduction beyond this point will practically be limited by the DC-link current and the maximum permitted active current component. For operation with a voltage reduction coefficient K of 5%, the maximum CSI line-line voltage stress reaches 480V which further reduces the added installed power to 2.7%.

Although the transient system behaviour of the CSI has been demonstrated for a worst case scenario involving a large VSI current step change, the results could be improved via modifications of the main converter including the adjustment of the VSI transient response or the introduction of a limit for the maximum VSI current step which could be ramped instead. Alternatively future solutions could investigate the introduction of a second filtering stage following the current ripple extraction to remove any residual low order harmonic components. This could allow for better dynamic performance but at the cost of additional control complexity and computational requirements.

3.6.4. Series Capacitor Impact on the Output Power Factor

The impact of the series capacitor on the output power factor remains limited for the VSI operating at full load. For the maximum series capacitance of 110μF, operation with a voltage reduction coefficient K of 0.1 will result in a power factor PF = 0.986 while for a further decrease to K=5% the power factor decreases further to PF= 0.983. At the minimum capacitance considered however the operation of the CSI has a minimal effect with the output power factor measured at slightly higher than 99%. It should be noted however that for a lower VSI loading the effect on the output power factor will be more significant. For VSI operation at half load, using Cs=110μF, the power factor is reduced to 0.94 reflecting the relatively more significant reactive requirement of the auxiliary converter.

3.6.5. Semiconductor Loss Estimation

The semiconductor losses for the hybrid system have been estimated in simulation for the different operating points considered in Fig. 3-18. For the VSI, the IGBT semiconductor model chosen is the FF400R33KF2C made by Infineon which is rated at 3.3kV/400A but can reach up to 660A. The Semikron SEMiX202GB12E4s IGBT model has been used for the CSI which is rated at 1.2 kV/200A. The reverse blocking diodes in the CSI and clamping diodes in each VSI leg have also been modelled based on the corresponding model characteristics although potentially higher performance fast-recovery diodes could be used. The device loss model has been based on the datasheet characteristics at operating temperatures of 150º for the CSI and 125º for the VSI.

Similar to the approach followed in §3.5.1, the total CSI semiconductor losses, which are averaged over a fundamental period, have been scaled by the nominal DC link current and fed as an equivalent DC side resistance to induce an equivalent increase in the CSI active current component. The resulting steady state losses are presented in the following charts showing the conduction, switching as well as total losses for each converter.

For independent converter operation, the losses are shown (Fig. 3-20) per converter bridge at different operating points. The minimum CSI semiconductor losses have been achieved at minimum capacitance operation (55μF) close to 2kW. The CSI DC link current increase at the maximum capacitance is reflected by the relative increase in conduction losses which reach 1660W. For the same capacitance (110μF) and DC current, a 400W decrease in switching losses can be observed for a CSI fundamental voltage reduction of 5% compared to 10%.

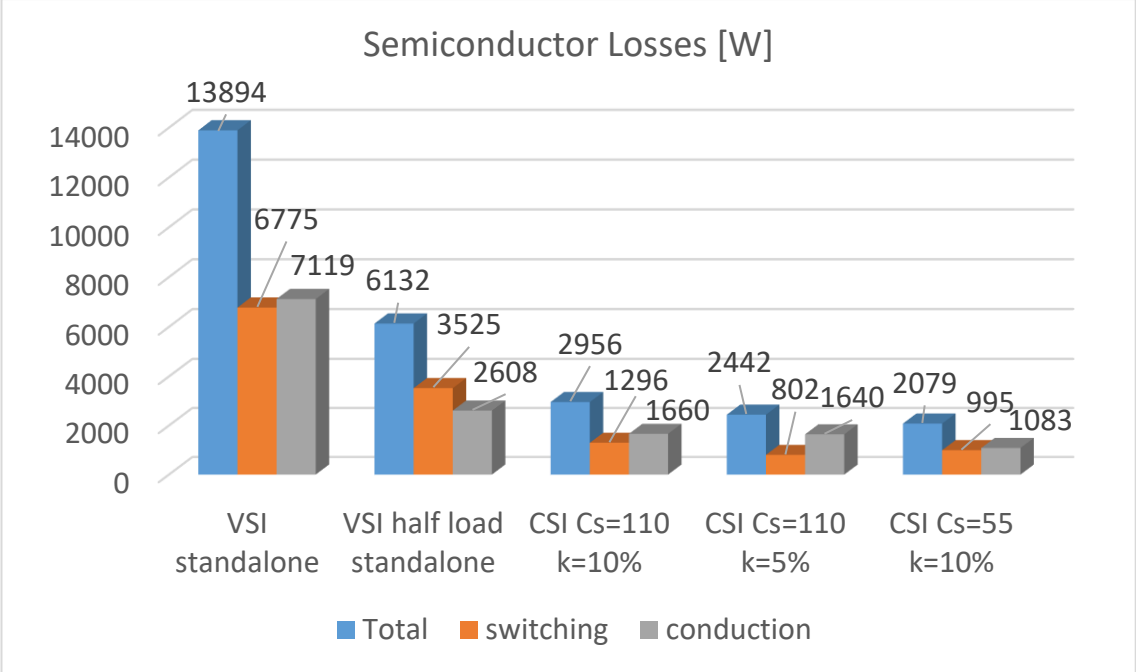


Fig. 3-20: Estimated semiconductor losses for VSI at full and half load operation and CSI at different series capacitance and voltage reduction operating points

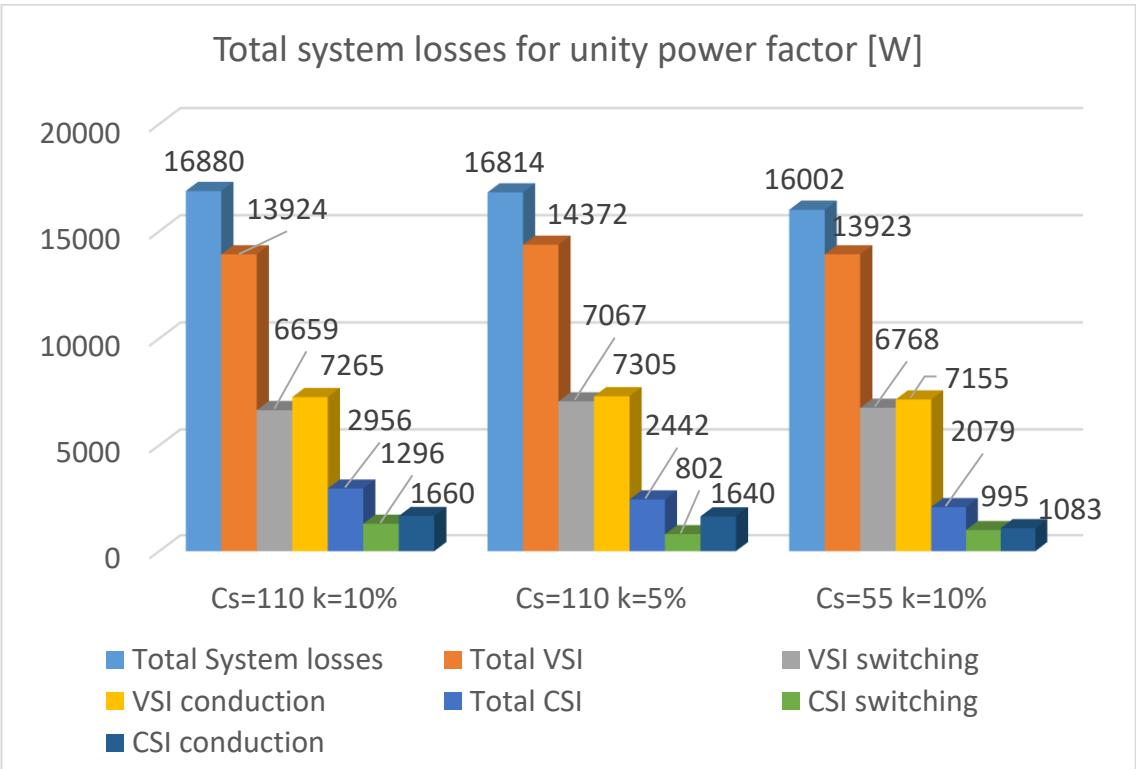


Fig. 3-21: Estimated total semiconductor losses for combined VSI and CSI operation where the VSI is compensating for the series capacitor reactive power to achieve unity power factor.

At full load, the VSI switching and conduction losses are relatively balanced indicating good loading of the semiconductors chosen. The total VSI loss at full load reaches 13.9 kW which is reduced to 6.1 kW at half load operation. The VSI losses reach 0.7% of the output power, while when considering the added CSI losses, at around 3 kW in the worst case scenario, the total semiconductor losses amount to 0.89 % of the output power.

A second set of results is shown in Fig. 3-21, considering the effect of the VSI performing reactive power compensation and evaluating the impact on the total losses of the hybrid assembly. From a CSI point of view, as expected, the losses at each operating point remain unchanged. The VSI losses increase although a clear pattern cannot be observed based on the breakdown of switching and conduction losses showing that the impact can vary according to the CSI operating point. For the two scenarios considering a 10% fundamental voltage stress, the added loss is negligible around 30W while a more significant increase of almost 480W when operating at a 5% fundamental voltage coefficient at maximum capacitance. This is partly explained by considering that this operating point requires the maximum reactive current component. The overall effect of the total system semiconductor losses compared to the total power processed in the hybrid assembly remains quite small, measuring at 0.9% of the output power.

3.7. Conclusions

A medium-voltage power conversion solution implemented as a hybrid inverter has been proposed, consisting of a slow switching medium-voltage rated 3-level NPC inverter interconnected with a low VA rated CSI acting as an Active Power Filter to remove its switching current harmonics while a series connected capacitor ensures reduced fundamental component voltage stress on the CSI thus facilitating low voltage device ratings.

The dependency between the switching current ripple, the size of the series capacitance and the resulting fundamental voltage/current CSI stresses have been discussed. A design procedure detailing design considerations for ensuring reduced voltage drop has been outlined that suggests the possibility to optimise the size of the installed CSI power versus the size of series capacitance and CSI losses.

Preliminary optimisation results that assume a simplified loss model for the CSI reveal that the installed power may be reduced to below 4% of the rating of the main converter for a range of operating points which have also been validated through simulation. A reduction of up to 96% of the main switching current harmonics has been obtained.

The semiconductor losses for the Hybrid system have been estimated at lower than 1% of the output power while a small impact on the output PF has been recorded, associated with the reactive current required to maintain a given voltage drop across the series capacitor.

Future work includes the improvement of the dynamic performance of the circuit due to the impact that low order current harmonic disturbances injected through the series capacitors which can affect the CSI voltage reduction scheme.

CHAPTER 4. Non-Zero Grid Impedance: Three-Phase Hybrid Inverter Connected to LCL Filter

This chapter expands on the Hybrid concept by investigating the hybridisation of a MV inverter with an existing LCL filter and explores the additional challenges related to resonances with a proposed solution for stable operation.

An initial brief overview is first given on the effects of an increased grid impedance to the resonant characteristics of the Hybrid converter topology with the perspective of introducing the challenges which are then encountered for operation of the CSI in combination with a VSI connected to an LCL output filter.

Section 4.1.2 then follows into the main scope of this investigation which outlines the procedure followed into designing the LCL filter and CSI along with the design considerations taken and alterations compared to the previous design. Section 4.3 outlines the options for resonance damping and proposes an active damping compensator before showing the simulation results that validate the expected operation of the hybrid system. An increase in complexity of the system to account for the mitigation of the voltage ripple seen at the input terminals of the hybrid system (equivalent to point of common coupling – PCC) caused by the CSI switching harmonics, along with an evaluation of the sensitivity to wide grid impedance variation is also included. The impact on efficiency is explored by estimating the semiconductor losses.

4.1. Topology Introduction with Non-Zero Grid Impedance

4.1.1. Small Grid Impedance

This section provides a generic outline on the resonant effects created when non-zero grid impedance is considered compared to the topology and scaling presented in the previous chapter. Fig. 4-1 shows the single phase equivalent circuit for the proposed hybrid topology taking into account the grid inductance.

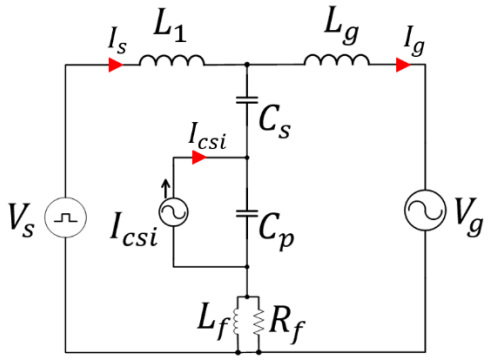


Fig. 4-1. Single Phase equivalent circuit for Hybrid topology with non-zero grid impedance

From a CSI operation point of view, the addition of a small grid impedance could be beneficial for providing additional attenuation at the CSI switching frequency. Considering the grid will be mostly of inductive nature, the grid inductance L_g will be summed to the filter inductance L_f, which will therefore cause the filter resonant frequency to shift towards a lower frequency without changing the order of the filter response. As the inductance increases however, the resonant frequency will inevitably move within the bandwidth of interest making harmonic cancellation of the VSI switching harmonics more challenging. To quantify this statement, the effect of added grid side inductance is demonstrated by plotting the CSI filter response for increasing inductance values. To correlate this to the previous chapter, the grid inductance values are shown as a ratio/factor of the previously chosen CSI filter inductance L_f of 23µH while keeping the values for series and parallel capacitors C_s and C_p constant at 110µF and 11µF.

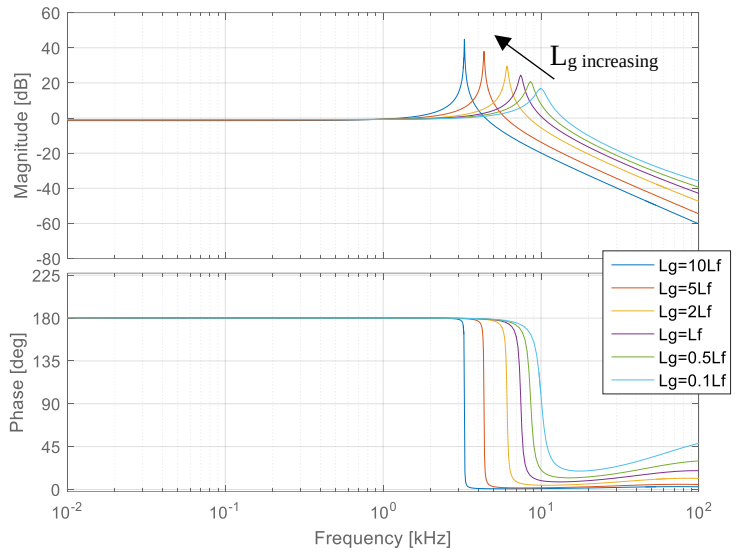


Fig. 4-2: Bode plot showing the CSI I_{csi} to grid current I_g response for an increasing grid inductance.

For a grid inductance in the range of a few μH, the CSI filter response (Fig. 4-2) will remain largely unchanged. A shift of more than one kHz in the resonant frequency can be observed when the grid inductance is increased to just half the filter inductance (11.5μH). For a unit ratio between the two inductances the resonance is moved to 7.5 kHz while it can be noticed that the resonant peak also increases to 24dB (in comparison to 16dB at 10 kHz) as the damping resistance R_f becomes less effective. It is therefore demonstrated that the benefits of the additional attenuation at the CSI switching frequency which could provide additional damping for the CSI switching ripple, could be outweighed by the effect of further excitation at the filter resonant frequency which may consequently necessitate a redesign of the CSI output filter.

In addition, for a grid inductance larger than the considered filter inductance, the resonant frequency will move within the bandwidth of harmonic cancellation. The resonant frequencies for a grid inductance at twice, five, and ten times the filter inductance are at 6 kHz, 4.35 kHz and 3.27 kHz which for the CSI would inhibit the filtering ability in the open loop control method previously considered. This imposes an unusual situation where, if the grid inductance is small enough, the resonance will be outside of the effective CSI bandwidth but may not significantly affect the CSI filtering capability, while when the grid impedance increases, the resonance could

interact with the VSI switching harmonics, but will also be within the CSI theoretical control bandwidth where a closed loop approach could be applied.

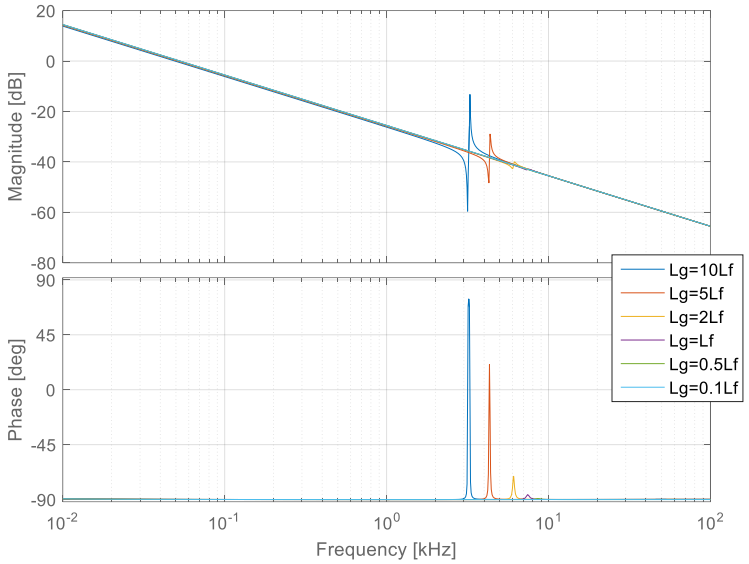


Fig. 4-3: Bode plot showing the VSI converter voltage to VSI current I_s response for an increasing grid inductance.

From a VSI perspective, a small grid inductance (smaller or equal to L_f) will have a negligible effect as shown by the bode plot for the VSI voltage to VSI current in Fig. 4-3 where the first order response is unchanged. For larger inductance values the consideration of the grid inductance will transform the system response from a first order to a third order system, matching an LCL characteristic response with the resonant notch occurring at the same frequency observed in the CSI filter response. While for all scenarios the resonance will be higher than the VSI switching frequency, the risk is that as the grid impedance increases the resonant notch will interfere with main VSI switching harmonics. Although this would be unlikely to occur based on the grid inductance alone, the overall grid impedance needs to be carefully considered before the hybrid topology is implemented.

The operation of the hybrid system with a resonant frequency situated around 6 kHz is investigated experimentally in §7.2.

4.1.2. Large Grid Impedance: LCL Interconnection

This section expands on previous work relating to the Hybrid concept by investigating the challenges of applying the same technique to connect the auxiliary CSI via series capacitors to the MV grid/main inverter via their split inductance that typically will form an LCL filter and lead to the known associated stability problems reported already in literature [54]. The resulting topology is shown in Fig. 4-4. It contains also a set of damping resistors and a contactor that can be used to switch the main VSI operation mode from passive LCL filtering of the switching current ripple to active/hybrid operation.

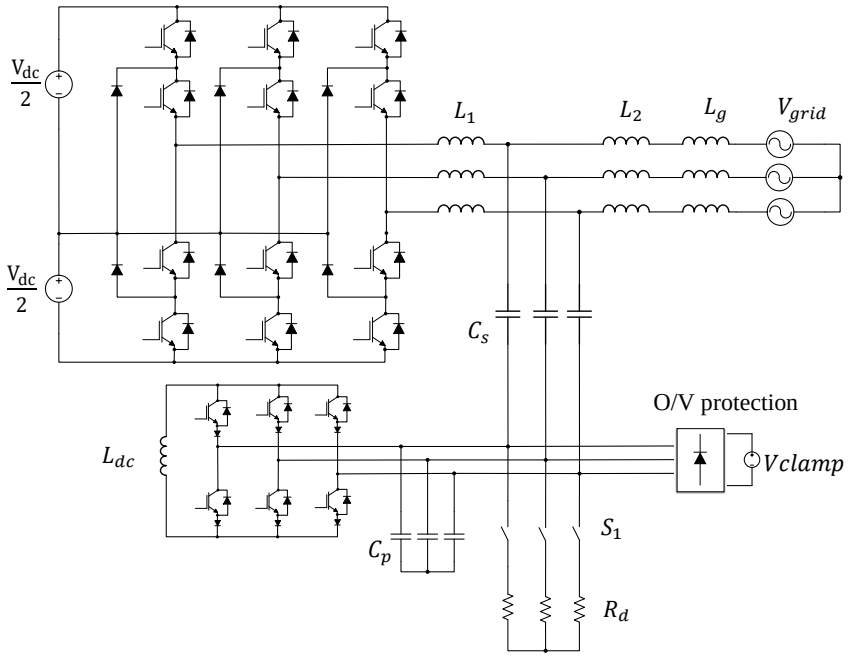


Fig. 4-4: Hybrid converter topology with LCL filter interconnection

The evolution from the Hybrid topology shown in Fig. 3-1 , which assumes an ideal stiff grid, to the LCL connected Hybrid topology comes as a logical progression when taking into account the supply line inductance as explained in the previous section. This could be considered a more realistic implementation for MV (and perhaps weaker) grids, as the grid line inductance will naturally form an output LCL filter when combined with the series capacitance and VSI side inductance.

Although in this investigation, a more simplistic approach was taken towards the LCL filter design, the considerations are in line with existing literature [9, 54, 60]. The connection of the CSI operating as an Active Power Filter (APF) on an existing LCL filter has the potential to achieve further improvement in the harmonic current filtering with very low added installed power with the possibility of adding only the auxiliary CSI, its AC side filter capacitor C_p and the overvoltage protection, with no other additional components (AC side inductors).

The resulting topology shown in Fig. 4-4 allows for two modes of operation via switch S1. When the switch is closed and the CSI disabled, the VSI operates using passive LCL filtering with the resistors R_d providing damping. When the switch is opened and the CSI is enabled, the circuit operates as a Hybrid active filter with the damping resistor R_d and its associated losses removed. As a result the overall topology can be considered hybrid in two ways, due to the combination of a main VSI and auxiliary CSI as well as the option of choosing between passive and active filtering.

Switch S1 in this simulation study is used to compare the harmonic performance between passive and active filtering. Realistically it could be implemented as a mechanical or electronic (Triac) switch depending on the functionality needed: redundancy or safe start-up/shut-down (inrush current limitation). Although the switch could be realised with semiconductors there is no clear advantage given that it must be rated at the full grid voltage and more than 20% of the current. An electromechanical switch (contactor) would be sufficient to provide the required protection, synchronisation and meet the ratings at a reduced cost.

The addition of the CSI to the LCL has two main topological implications. During active filtering, the damping resistor R_d of the LCL filter is no longer needed therefore a source of resistive losses is removed. Compared to the stiff grid design, the AC side filter inductor of the CSI (L_f) is no longer necessary as sufficient attenuation is achieved by the combination of capacitor C_p and grid side inductance. The overvoltage protection clamp shown on the circuit is necessary to absorb any surge voltages created during the transition from passive to active filtering.

4.2. Modified Design Procedure

The following section outlines the additional design considerations along with the procedure required to obtain a stable performance when the hybrid converter is connected to the grid via an LCL filter under the same requirements for the maximum CSI voltage stress and grid specifications outlined in CHAPTER 3. Since the system in Fig. 4-4 can operate as two different circuits, they will be treated as such in the design procedure and referred to as Passive mode, when the switch S1 is closed and CSI is disabled and Active mode when S1 is open and CSI is enabled. The procedure starts by designing the LCL circuit, ensuring proper Passive mode operation. The focus is afterwards centred on the design of the CSI and the choices made in order to meet the aforementioned design requirements. The single phase equivalent circuits for each mode are shown in Fig. 4-5 where the inductances of the LCL output and grid side (L_2 and L_g) are grouped as a single inductance L_o to reflect the frequency response of the system.

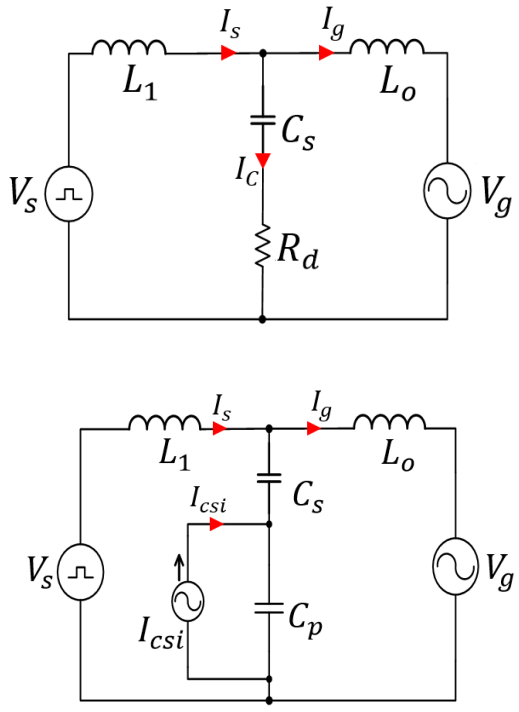


Fig. 4-5: Single Phase equivalent circuits for a) Passive; b) Active Filtering

4.2.1. LCL Filter Design Procedure

The VSI inductance L_1 is chosen to limit the maximum switching current ripple at 20% giving the same value as in the stiff grid situation of 3.6mH. The Grid side impedance is then calculated based on [109] for a *SCR*= 10 and *X/R* = 5 resulting in L_g=1.8mH and R_g=0.113Ω. This values have been chosen to be representative of a near weak grid situation, usually identified as having a SCR lower than 10, to reflect the possibility of the system operating in non-ideal grid situations. The inductance L_2 is chosen at 1.8mH so that L_g+L_2 match the converter side inductance therefore avoiding extra resonances in the system.

The LCL/series capacitor C_s must then be chosen to place the resonant frequency (Eq.19) at approximately half of the switching frequency or below. The maximum capacitance value is usually restricted based on the allowed reactive power generated therefore a similar range of capacitances for C_s can be considered as the previous design i.e. 55-110μF with respective resonant frequencies between 500-360Hz

$$\omega_{res1}=\frac{1}{\sqrt{L_t C_s}} \quad \text{where } L_t = \frac{L_1 L_o}{L_1+L_o} \qquad \text{(Eq.19)}$$

4.2.2. CSI Active Filter Design

The connection of the CSI and its filter capacitor C_p in neutral point of the LCL filter presents a convenient place from the point of view of maintaining low voltage insulation and voltage CSI ratings, as the neutral potential is closest to ground but leads to an intriguing design problem to provide stable operation. In addition to the CSI design restrictions existent for the stiff grid connection, the placement of the new resonant frequency needs careful consideration as it may be significantly higher, influenced by a smaller capacitance (C_p). For a 10:1 C_s/C_p ratio, the new resonant frequency may three times higher than for the passive LCL.

The problem can be explained by considering the harmonic current spectrum produced by the VSI that needs to be removed. The triangular shape of the current ripple means that the first harmonic will cause the largest sidebands around the switching frequency and the remaining

harmonic clusters situated around multiples of the switching frequency with negligible amplitudes above 5 kHz as shown in Fig. 4-6.

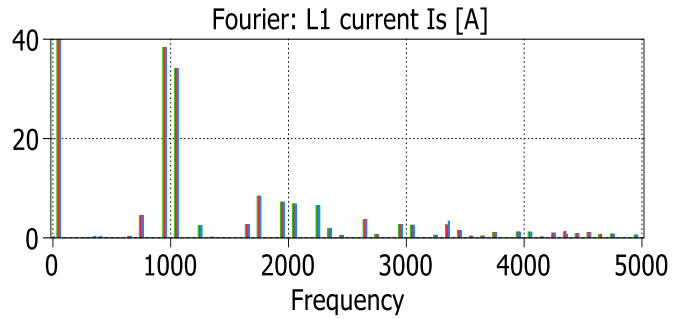


Fig. 4-6: Main VSI inductor (L1) current harmonics

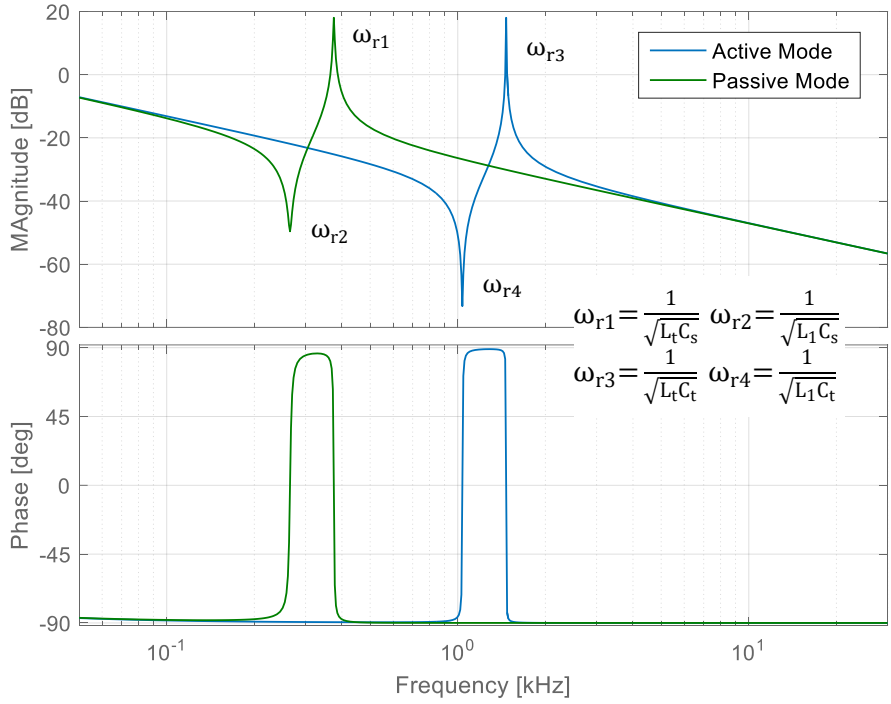


Fig. 4-7: Converter Voltage to Converter Current Bode plot for active and passive filtering mode.

In a stiff grid situation, the CSI design is implemented by matching the parallel capacitance C_p as a fraction of C_s to limit the circulating current and then choosing an appropriate filter inductance to place the cut-off frequency at less than half of the CSI switching frequency (typically 10-15 kHz for 30 kHz CSI switching frequency). This means that the CSI filter produces no/constant attenuation for the VSI current ripple (f<5 kHz) to be cancelled shown in Fig. 4-6.

In the LCL scenario, the connection of capacitance C_p to C_s will shift the resonant frequency of the LCL filter. Fig. 4-7 illustrates the resonant frequency shift by showing the Bode plot of converter voltage V_s to current I_s with the corresponding resonances for active and passive mode.

Considering that the resonant frequency of a MV LCL filter is typically situated around half of the most significant lowest switching frequency harmonic, it makes it impossible to place the new resonant frequency ω_{r3} outside of the current harmonic range to be cancelled shown in Fig. 4-7. Placing the resonance below the switching frequency sidebands is impossible as it would require a much larger capacitance ratio compared to C_s and placing the resonance above 5 kHz is also not feasible as the capacitance would be too small causing large switching harmonic voltage across it.

The capacitance value must therefore be selected to avoid placing the resonant frequency where a switching current harmonic is situated as this could excite resonance and would create instability. In this case the suggested value would be near 1.5 kHz, equally spaced between the harmonic clusters of the switching frequency and twice switching frequency.

4.3. Resonance Damping: Passive and Active Damping

4.3.1. Passive Damping

One option of dealing with resonance is via the use of passive damping. Fig. 4-8 reveals three possible damping options and Fig. 4-9 shows the corresponding frequency response on the input voltage to input current for the values listed below.

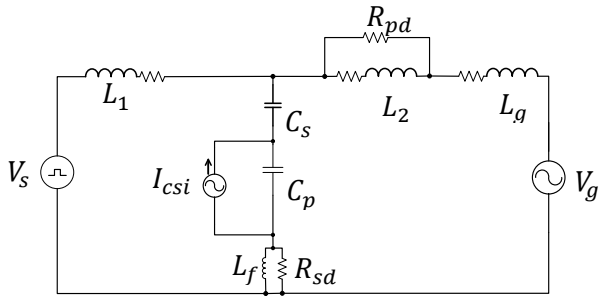


Fig. 4-8: Single Phase Equivalent circuit showing passive damping options

L_2 parallel damping resistor R_{pd} =50Ω

Series capacitor damping resistor R_{sd} =1Ω

Series capacitor LR damping R_{sd} =1Ω, L_f =0.3mH

The option of adding a parallel resistance to L_2 is effective, but as the parallel resistor cannot be removed during passive mode the losses are increased. Thus one of the other two methods could be pursued with the advantage that if critical damping can be achieved, a simpler CSI control scheme could be used, although a closed loop control method may still be required to be put into place of the open loop control scheme proposed for a stiff grid scenario. Realistically, some damping is achieved by the internal AC resistance of the components, which for high current rating inductors (L_1, L_2, L_g) may have significant skin effect around 1kHz. However the addition of extra damping resistance would lead to additional cost and losses, making passive damping undesired.

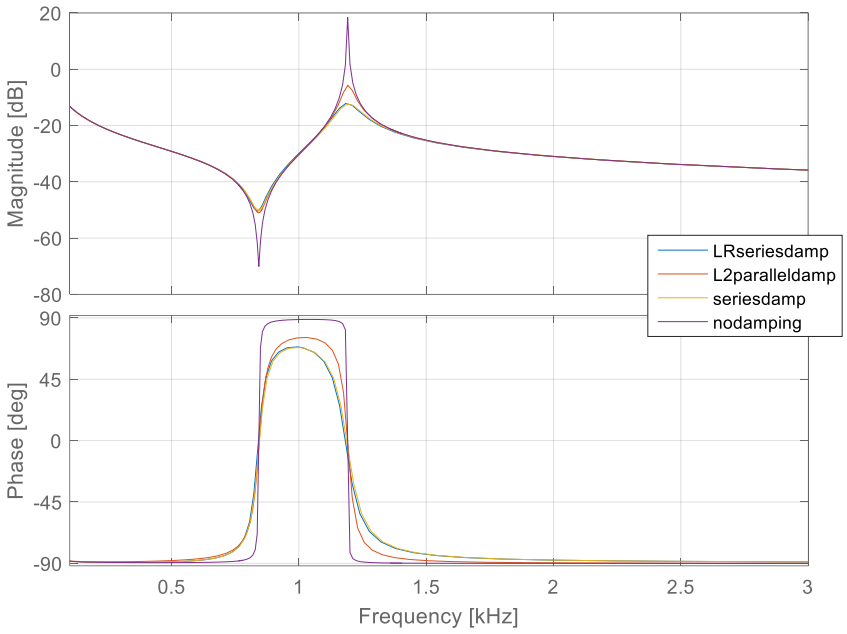


Fig. 4-9: Frequency response under different passive damping scenarios

4.3.2. Active Damping

The high switching frequency and application of the CSI in this hybrid topology to cancel the switching disturbance means that any resonance which is situated within the bandwidth of the controller should theoretically be contained by default. The placement of the resonant frequency within the current spectrum of harmonics to be eliminated means that using only the gain stated in (Eq. 9) is no longer sufficient and that the frequency characteristic of the CSI to grid current needs to be considered in order to achieve stability.

This task however is not straightforward due to the associated phase characteristic at around the resonant frequency. Unlike active damping requirements in other applications which are focused mainly on the reduction of the gain characteristic at the resonant frequency, this application requires that the phase characteristic of the VSI converter side current must be maintained and reproduced accurately in order for the ripple cancellation to take place. As a result a closed loop control system approach must be put in place to achieve unity gain and zero phase characteristic throughout the frequency range of interest.

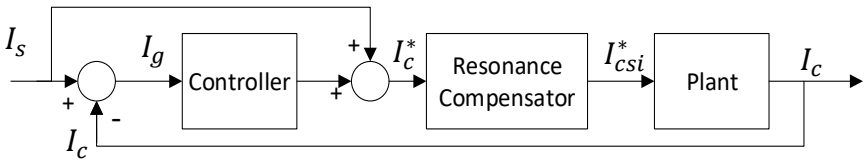


Fig. 4-10: Active damping implementation for Ripple Cancellation

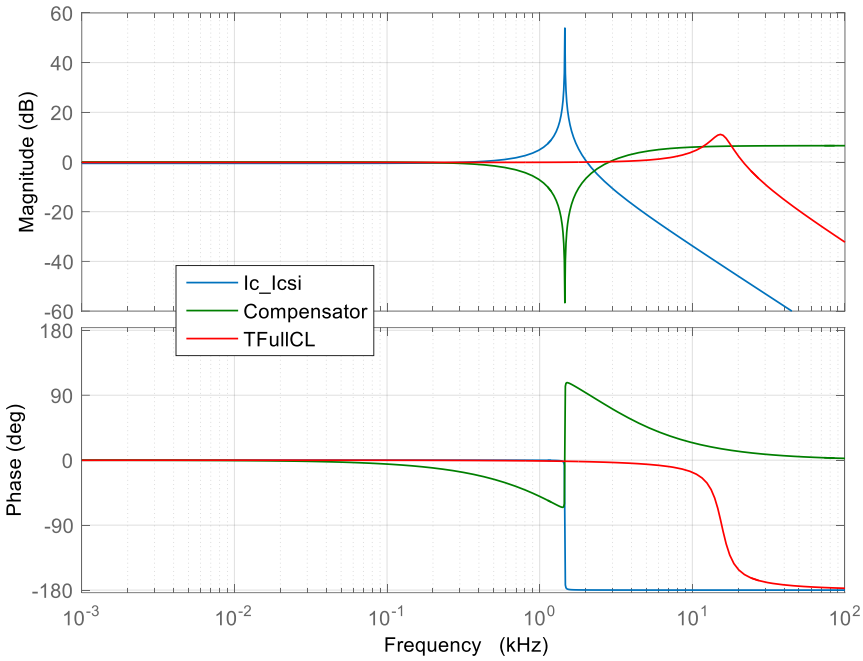


Fig. 4-11: Bode plots of the following transfer functions: I_{csi} to I_c, the resonance compensator and the overall closed loop active damped system

Fig. 4-10 shows the proposed active damping control system while Fig. 4-11 shows separately, the corresponding Bode plots of the Plant (I_c/I_{csi}), of the resonance compensator and of the overall closed loop response. The switching current ripple extracted from the main converter (L_1) current I_s is the reference signal for the series capacitor current I_c. The resonance compensator acts as a notch filter at the resonant frequency as shown in Fig. 4-11. The controller is designed so that the closed loop response behaves like a low pass filter with cut-off frequency around 15 kHz and zero or negligible phase shift up to 5 kHz. The actual implementation means that the "(Eq.17)" block in Fig. 3-9 is replaced with the resonance compensator scheme.

4.4. Simulation Results

The performance evaluation of the proposed hybrid system is carried out by implementing the simulation model and the control in PLECS. The first step includes a test to validate the operation of the active damping control system shown previously. Steady state harmonic performance is evaluated in terms of grid current and PCC voltage quality. A solution is discussed to remove the PCC voltage ripple caused by CSI switching including also the assessment of grid impedance variation. Finally the semiconductor losses are estimated to investigate the full impact of adding the auxiliary CSI to the system.

The series capacitor has been set at 100μF to give a resonant frequency of 375Hz during passive mode and R_d=50mΩ has been chosen to give sufficient damping and very good attenuation of the 1 kHz switching frequency ripple during passive filtering operation. For the design however C_p has been chosen at 10μF placing the resonant frequency at 1190Hz, close to the 1250Hz sideband in order to demonstrate that stable circuit operation is possible under certain damping options which means the component design is not so strict.

One aspect which has been simplified for this investigation, is that the main VSI has been operated in open loop with the modulation adjusted to match the power processed as shown in the previous chapter. This was necessary to avoid the further instability caused by interactions of the VSI control system which would be difficult to recover from. This therefore ensures that any instability/resonance excitation shown takes place only due to the output filter resonance, which is then stabilised by the CSI control system. Furthermore, an ideal current source has been set as the CSI DC-link but with the current active component clamped to zero to ensure it does not contribute any power.

4.4.1. Active Damping Validation

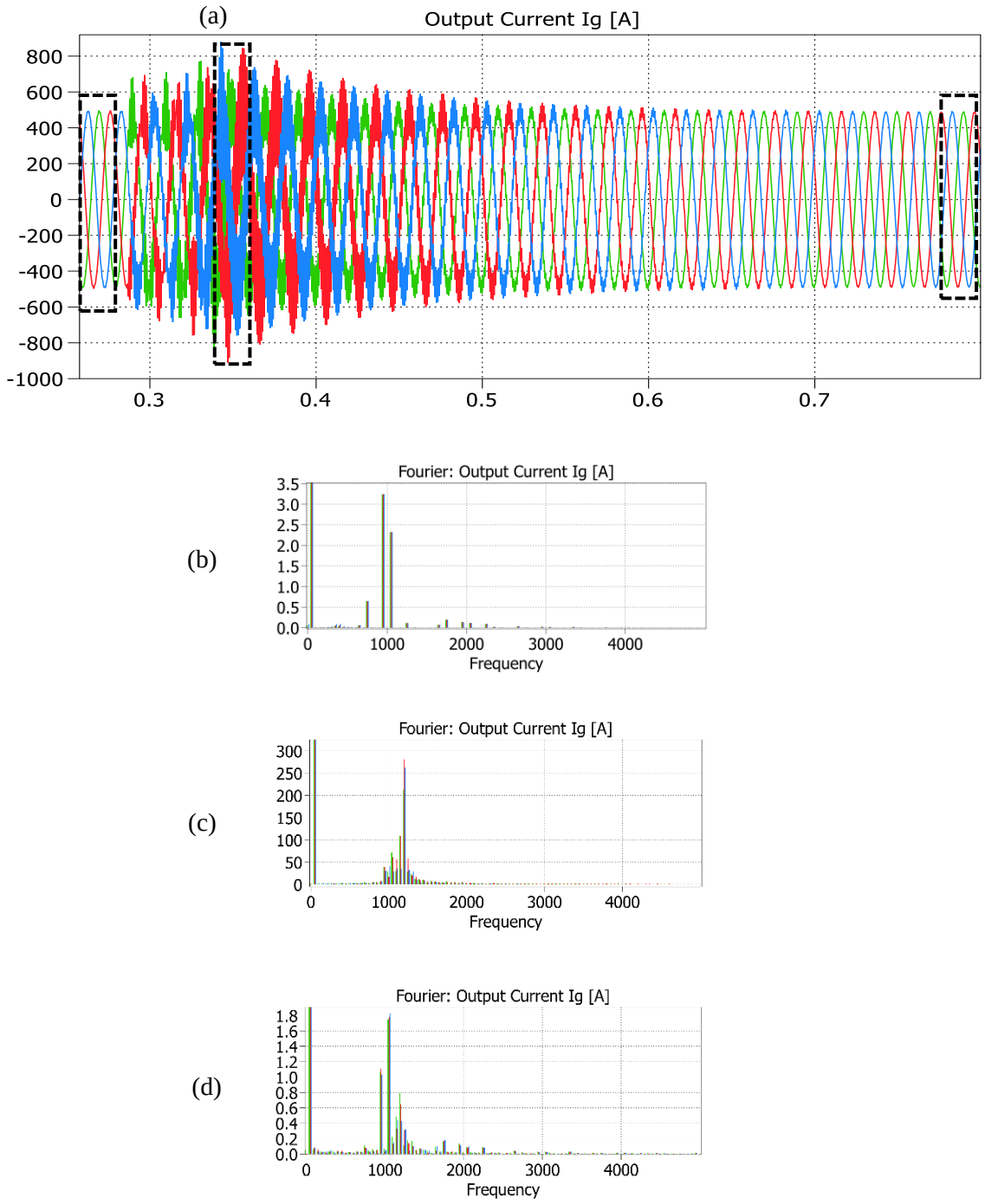


Fig. 4-12a-d: Transient operation showing activation of CSI at t1=0.28s followed by LC circuit resonance build-up and activation of the resonance compensator at t2=0.36s followed by resonance being actively damped (t>0.7s). b)-c)-d) FFT of the MV grid currents when b) CSI was off and switching ripple is passively damped by the LCL filter; c) just before active damping activation (t=0.34-0.36); d) at end of simulation when resonance levels are not visible.

Fig. 4-12 reveals the transient performance of the system when operation is changed from passive LCL filtering mode (t<0.28s) to activation of the CSI (t1=0.28s) followed by a rapid build-up of resonance of the LC circuit that includes the small CSI filter capacitor C_p. This results in a resonant frequency in the proximity of the upper switching sideband which makes things worse but was deliberately chosen to demonstrate the effectiveness of the active damping compensator which is activated at t=0.36s and facilitates full damping of the resonance (t>0.7s) without involving any dissipative element (damping resistance).

In order to assess accurately the performance, the grid currents were sampled at key moments during this transient and the resulting grid current FFTs are shown in Fig. 4-12b-d. All three FFTs are performed on a 20ms window (one grid fundamental frequency period). In Fig. 4-12b and Fig. 4-12d, the system is operating in steady (passive LCL filtering in Fig. 4-12b) or near steady state conditions (hybrid filtering Fig. 4-12d) therefore the FFT is indicative of the attenuation of the harmonic filter (passive or active). In Fig. 4-12c, the FFT has been performed on a 20ms window during the peak of the transient to show the rapid build-up of resonance and hence the larger current scale. It can be observed that passive LCL filtering mode offers a good power quality with the highest switching harmonic being reduced from 38Apk (Fig. 4-6) to 3.2Apk which means by almost 12 times (-21.5dB). A residual current harmonic is present at approx. 750Hz that corresponds to the resonance frequency of the LC circuit formed by the grid/main inverter inductance and the series capacitor Cs. The X/R ratio considered however provides sufficient damping to this circuit and the resonant harmonic stays reasonably low.

When active filtering is enabled and after the resonance damped, it can be noticed that same switching harmonic considered before (950Hz) is reduced to 1.1Apk, by a factor of 34.5 (-30.8dB). However, the most important harmonic is the upper sideband which peaks at 1.8A which corresponds to a smaller attenuation compared to Fig. 4-6 and the cause is that the active damping compensator of the LC filter having a resonance at 1.25kHz, very close to the upper side that needs to be attenuated, is altering the active filter behaviour of the circuit. This can be potentially improved by decreasing the CSI filter capacitor so that the resultant resonant frequency is moved

at 1.5 kHz, equally spaced between upper switching frequency sideband and lower twice the switching frequency sideband which should minimise the interaction between the resonant compensator and the active filter at the relevant switching harmonics.

4.4.2. Transient and Steady State Results

The choice of placement of the resonant frequency in the previous test has been done to demonstrate the functionality of the resonant compensator in a worst case scenario but this does not result in the best filtering performance of the hybrid system in steady state conditions. To achieve best performance, the system has been retuned in order to place the resonant frequency at an optimal point which is equally spaced from the largest current harmonics of main VSI. Capacitor C_s remains unchanged at 100μF while the redesign of the filter required a C_p of 7μF to move the resonant frequency from 375Hz during LCL passive mode to 1.46 kHz during active filtering mode.

A similar procedure to enable the operation of the auxiliary CSI has been repeated with the resonance compensator activated immediately when transitioning from passive to active filtering. To make the implementation as realistic as possible, the following changes in the simulation models have been implemented for the following tests: a deadtime of 1μs has been used for the main VSI; an overlap time of 300ns has been used for the CSI; a 20mH inductor was connected to the CSI DC-link (with the reference current set at 160A) and an overvoltage protection clamp circuit set at 1kV for protection of the CSI switches was also added. The clamp circuit, implemented using a three phase diode rectifier with a constant DC voltage source, will be active during the transition if the CSI AC line-line voltages exceed the clamp DC link voltage and as will be later shown, the clamp remains idle during steady state operation.

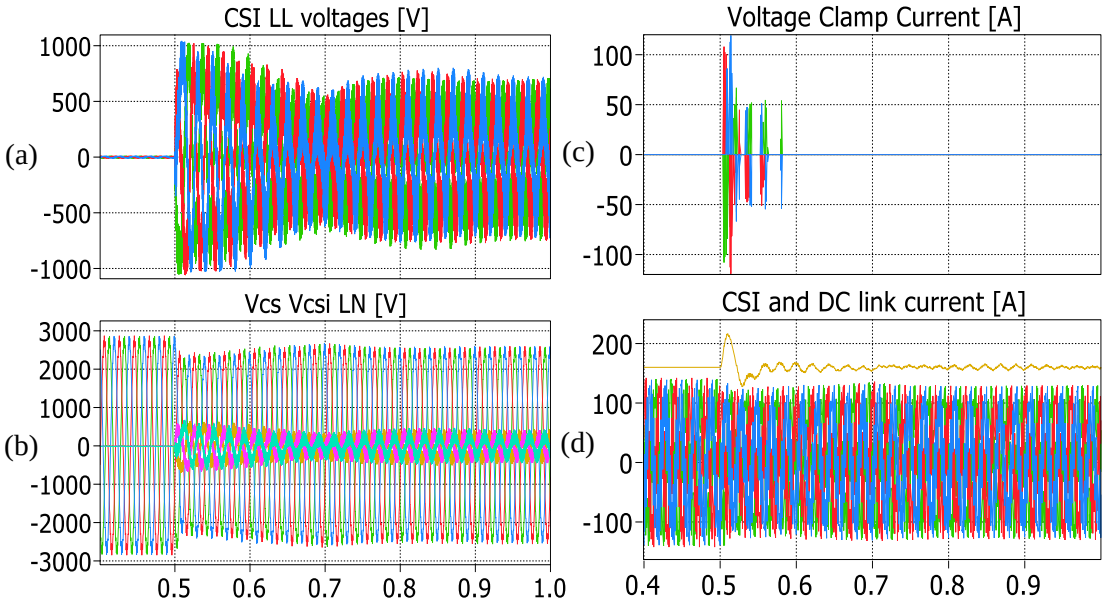


Fig. 4-13a-d: Transient between passive and active filtering mode at t1 showing a)CSI l-l voltage b)Series capacitor and CSI phase voltages c)Voltage clamp current and d) Series capacitor current along with CSI DC link current.

Fig. 4-13a-d reveals the transition from passive filtering to active filtering at time (t=0.5s) by showing the series capacitor and CSI line-line voltages(a), CSI phase voltages(b), voltage clump currents(c) as well as the series capacitor currents and CSI DC-link current (d). During passive filtering, the CSI outputs no current but with one phase continuously conducting to maintain the DC-link precharge level of 160A.

At t=0.5s, the resistor R_d is removed simultaneously to CSI activation. During the transition, a surge of currents in the clamp circuit is noticed as well as an overshoot of the CSI DC-link current but the CSI peak voltage stress remains at 1kV, limited by the voltage clamp. It can be observed that once active filtering is activated, the fundamental voltage component (Fig. 4-13b) that is proportional with the fundamental current passing through the series capacitor C_s (Fig. 4-13d) will be slightly reduced with the difference being shared with the CSI voltage. The waveforms are investigated in steady state for two fundamental cycles in Fig. 4-14.

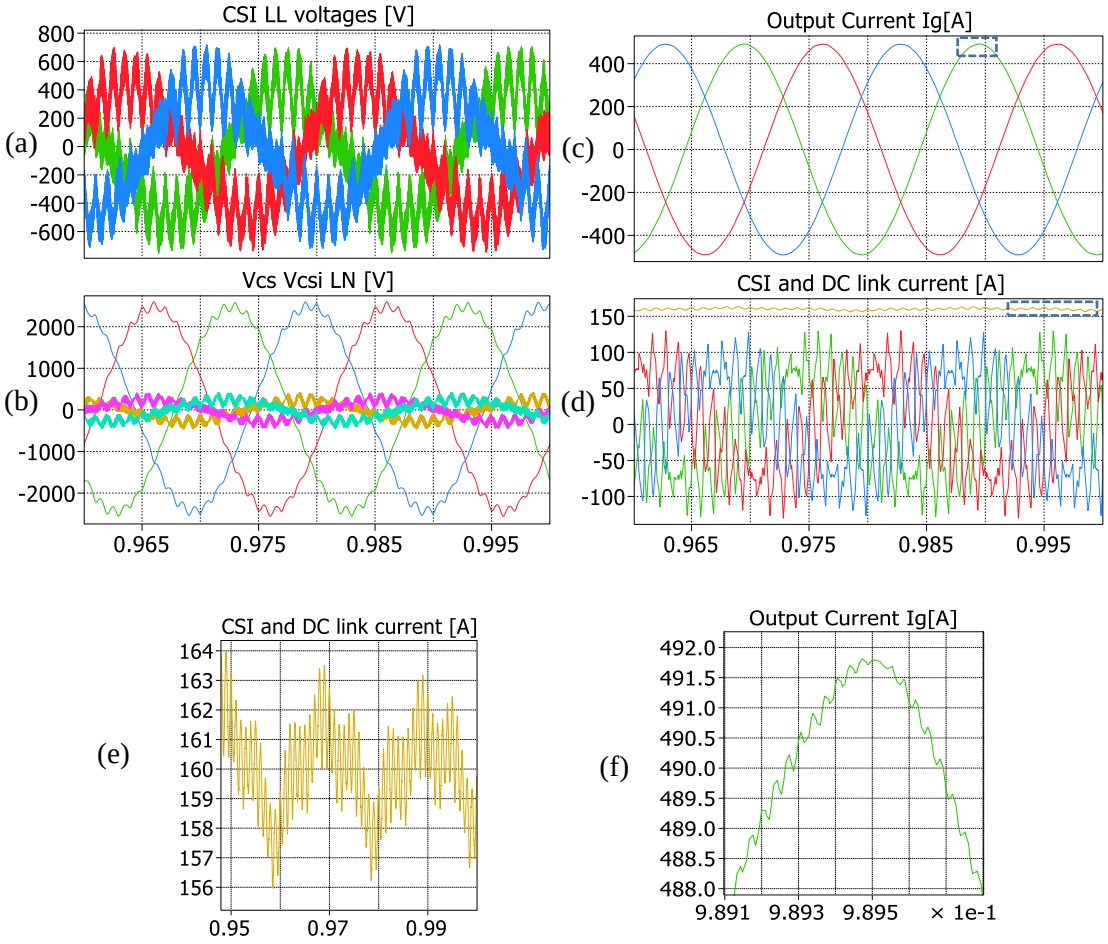


Fig. 4-14a-f: Zoom in on waveforms shown in Fig. 4-13 showing steady state conditions during active filtering mode showing a)CSI l-l voltage b)Series capacitor and CSI phase voltages c)Output current d) Series capacitor current e) further zoom-in on DC link current f)zoom-in on phase A grid current peak

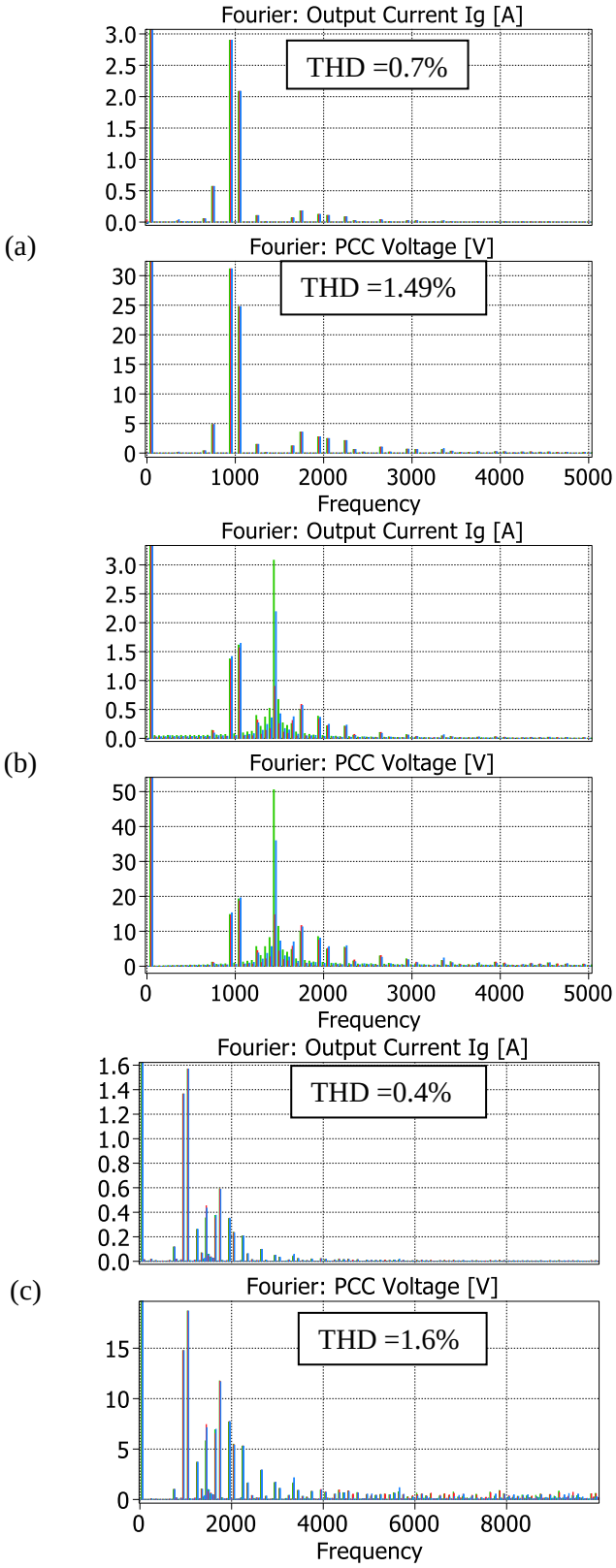


Fig. 4-15a-c: Output current and PCC voltage harmonic content a) during passive filtering mode b)during active filtering transient showing small resonance excitation and finally c) steady state performance during active filtering.

Fig. 4-14a-b shows the details at the end of the simulation in Fig. 4-13, when the models reached steady state. The voltages seen on the AC side of the CSI when the hybrid converter operates in active filtering mode are below 1kV, in line with the design specification with the fundamental component remaining at 10% of the voltage at the point of connection. Fig. 4-14c reveals that the main inverter switching ripple is eliminated from the grid side currents shown while in Fig. 4-14f which is a zoom-in shows that there is still some residual ripple remaining at minor levels but this is at the CSI switching frequency of 30 kHz.

Fig. 4-14d reveals the CSI current through the series capacitor along with the DC-link current during steady state. A closer look on the DC link current shown in Fig. 4-14e shows that its average remains at the 160A reference value having harmonics at the switching frequency and twice the fundamental frequency (100Hz) but at relatively low levels. The overall peak to peak ripple is approximately 5% of the DC reference value.

The harmonic content for significant frequency components less than 10 kHz is shown in Fig. 4-15 on the output grid current and voltage at the point of common coupling (PCC) at different moments during the transient performed in Fig. 4-13 while also showing the corresponding THD values. Fig. 4-14a shows the harmonic content during passive filtering which results in a current THD of 0.7% and voltage THD of 1.49%.

Once active filtering is enabled, an expected small resonance excitation can be observed in both the output current and voltage as shown in Fig. 4-15b but at lower levels compared to the previous test in Fig. 4-12. Finally Fig. 4-15c reveals the harmonic content close to steady state (t=1s) with the highest current harmonic reduced to 1.6A and a resulting grid current THD of 0.4%. Although the voltage harmonic content appears to be reduced around 1kHz, the THD appears to be slightly increased at 1.6% compared to 1.49% during passive filtering.

This can be seen more clearly in Fig. 4-16a-b showing steady state waveforms during passive and active filtering. In passive mode (Fig. 4-16a) a small 1 kHz ripple can be observed in both current and voltage waveforms. During active filtering the ripple caused by the 1 kHz VSI switching will

be mitigated by the CSI at the cost of injecting a small 30 kHz current ripple. On the output current this is barely noticeable due to the high impedance of the filters. However, due to the same large grid impedance, this small 30 kHz residual CSI current ripple that escapes into the AC grid causes a noticeable voltage ripple at PCC which requires additional consideration.

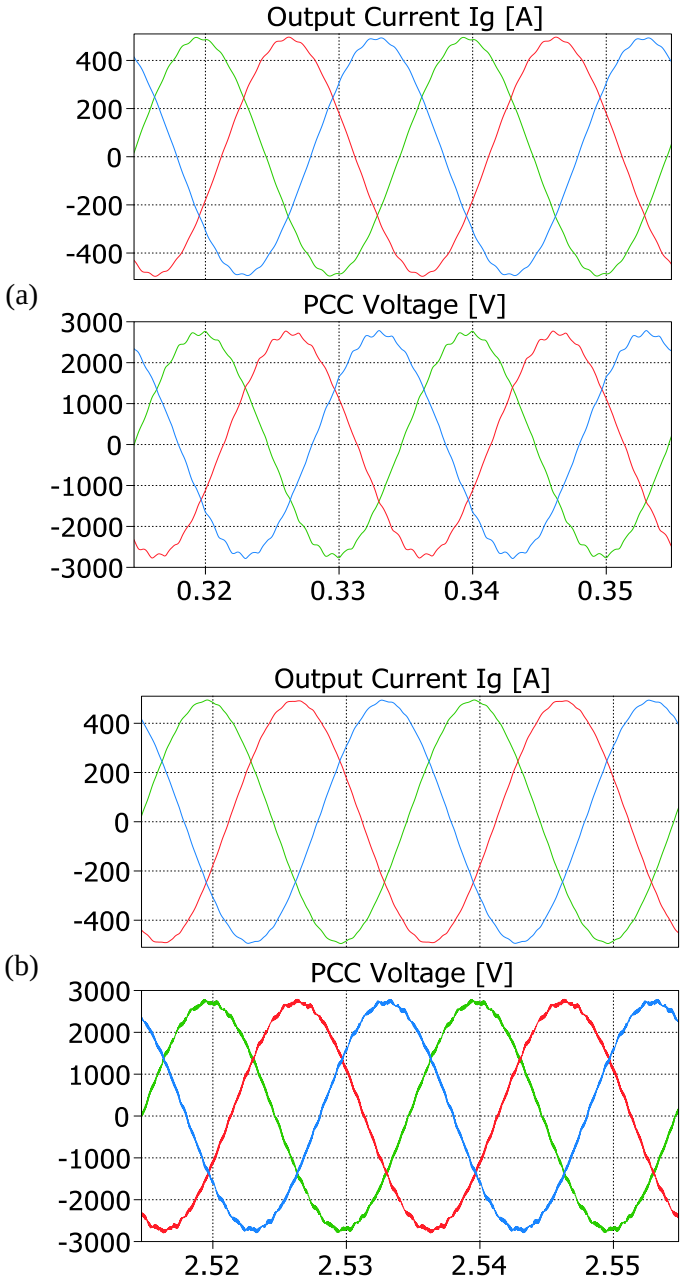


Fig. 4-16a-b: Steady state output current and PCC voltage a) during passive filtering mode and b) during active filtering.

4.5. Higher Order Grid Impedance and Effect of Impedance Variation: PCC Voltage Filtering

4.5.1. PCC Voltage Filter Design

To assess the possibility of addressing the aforementioned PCC voltage ripple issue, an investigation is presented regarding the possible introduction of a shunt capacitance at the point of common coupling to prevent the 30 kHz switching harmonics from being injected in the grid as shown in the single phase equivalent circuits in Fig. 4-17.

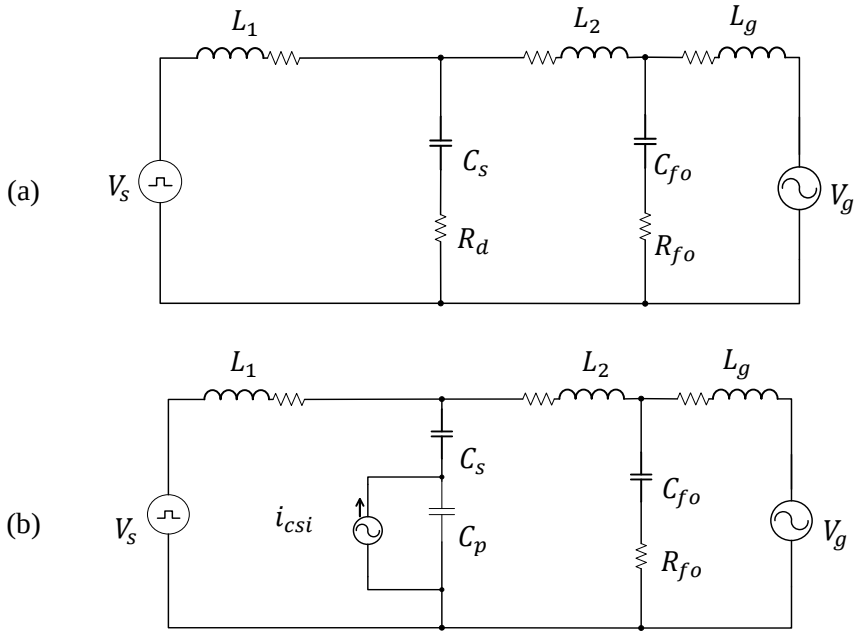
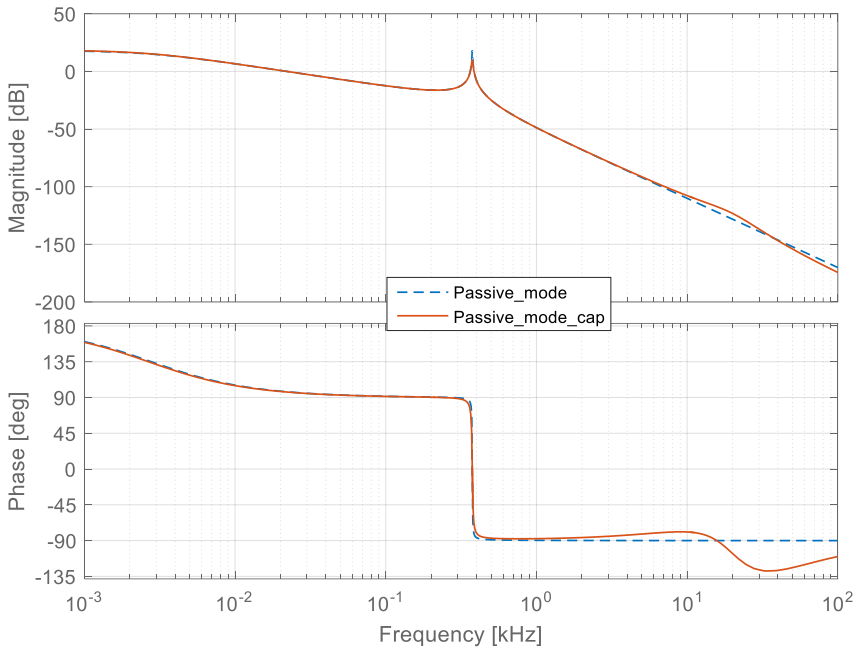


Fig. 4-17a-b: Single Phase Equivalent Circuit with output RC filter during: a) passive filtering; and b) during active filtering.



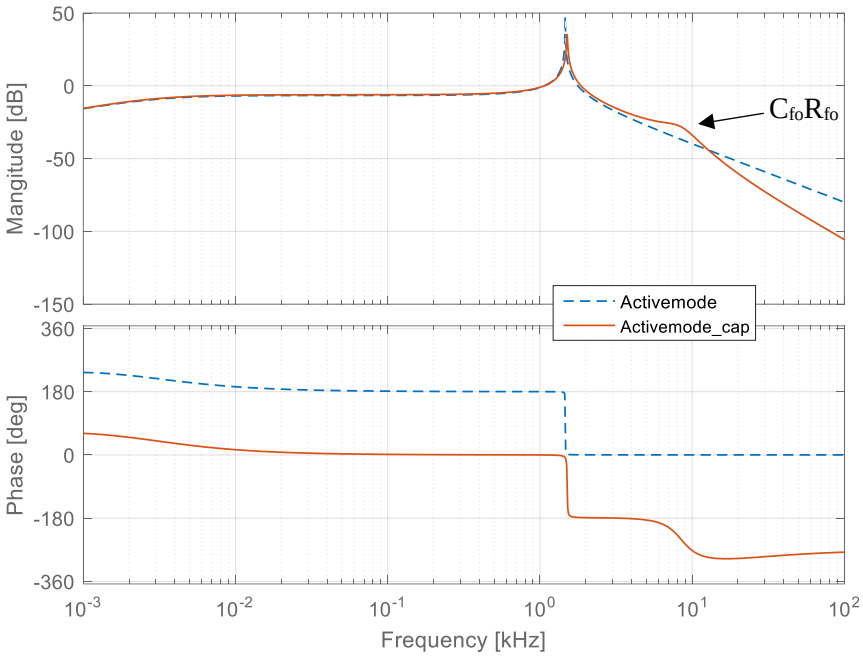


Fig. 4-18a-b: Bode plot showing Gain Vs frequency for I_g/V_s (VSI behaviour) as well as I_g/I_{csi}(CSI behaviour) with and without RC filter.

The requirement for this capacitance is to be smaller than Capacitor C_p so that the additional resonance is generated at a higher frequency well above the main resonance of 1.46 kHz (5-10 kHz). The 30 kHz voltage harmonic is small in amplitude and high enough in frequency so that a small capacitance in combination with a damping resistor to prevent resonances can provide

sufficient attenuation while meeting the requirement of no interference with the fundamental voltage component. To demonstrate this, two situations are compared: with a 1μF capacitance C_{fo} along with a resistance R_{fo} of 10Ω and without. The resulting frequency responses are plotted in Fig. 4-18 for VSI voltage to grid current and CSI current to output current. Although the equivalent circuit for passive filtering shown in Fig. 4-18 suggests a fifth order response, the capacitance is small enough to have a negligible effect on the output harmonics produced. The addition of the RC circuit becomes apparent on the CSI transfer function where the additional resonance can be observed as well as a slight shift in the main resonant frequency.

4.5.2. Effect of Grid Inductance Variation

The relatively low SCR chosen resulting in an output inductance ratio of 1 (L_2: L_g) means that the addition of any capacitive element at the PCC will have a significant effect on the main resonant frequency reducing the effectiveness of the active damping compensator. This is also true of any fluctuations in grid inductance indicating that the proposed system is not ideally suited for weak grid situations where the grid inductance is significantly large compared to the line side inductance. This is not the case for a higher inductance ratio where the shift in resonance is less significant although it would still result in a small error around the resonant frequency.

In order to demonstrate the effect of grid variations on the active damping compensator the circuit has been simulated using the above C_{fo}/R_{fo} combination starting with an inductance ratio of 3:5 (L_2=2.8mH and L_g=0.8mH). Subsequently a 50% decrease in the grid inductance to L_g=0.4mH has also been simulated to verify that for the given situation, there is reasonable tolerance to grid impedance variations. Fig. 4-19a shows the output PCC voltages as well as grid currents without capacitor C_{fo} where the highest harmonic amplitude around 30 kHz is around 12V as shown on the corresponding harmonic content plotted on the right column. Fig. 4-19b-c and the corresponding FFT plots show the effectiveness of Capacitor C_{fo} in attenuating the 30 kHz voltage to negligible levels with some improvement evident also around the 1 kHz frequency harmonics.

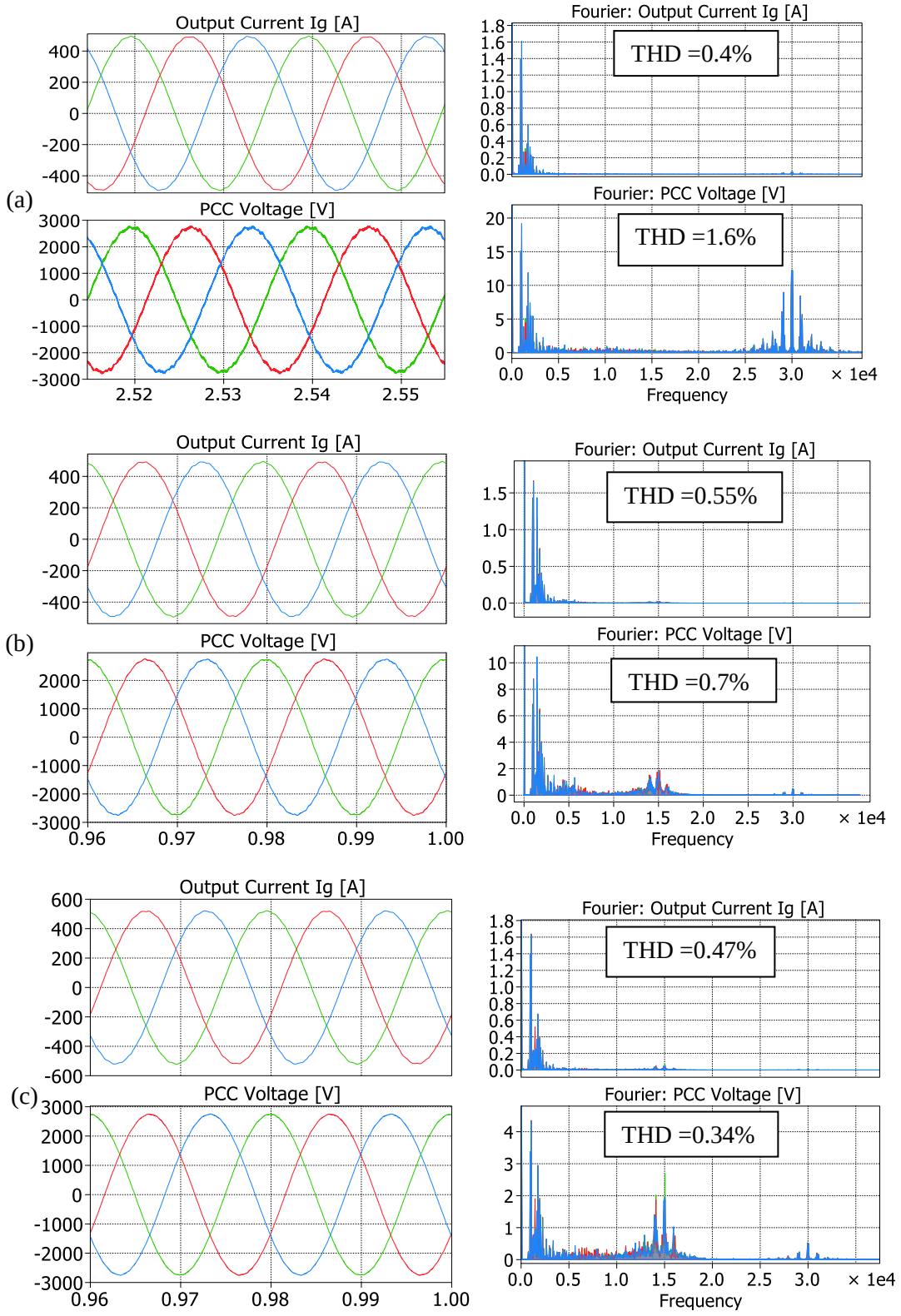


Fig. 4-19a-c: Steady state output current and PCC voltage during active filtering a)without voltage filtering b)using C_{fo}/R_{fo} and L_2=2.8mH, L_g=0.8mH and using C_{fo}/R_{fo} and L2=2.8mH, L_g=0.4mH (50% grid impedance variation). Corresponding FFT shown on the right column.

As the presence of the additional output capacitance has not been accounted for in the active damping compensator, it therefore creates an error around the 1.4 kHz resonant frequency in conjunction with the grid impedance variation.

This is indicated by the slight increase in the output grid current THD. When the output impedance is reduced further from 0.8 to 0.4mH (Fig. 4-19c), the compensator error seems to be reduced around 1 kHz as the resonant frequency moves towards lower frequencies although with a slight harmonic increase at 15 kHz due to a resonance created by the controller. It can be concluded that the addition of C_{fo} is highly effective providing high PCC voltage quality along with high current quality with some flexibility towards grid impedance variations given that the ratio of line inductance is higher than the grid inductance.

4.5.1. Semiconductor Loss Estimation

To evaluate the increase of system losses, the semiconductor power loss models have been used to estimate semiconductor losses. The choice of semiconductors has been kept the same as in §3.6.5 to ensure comparable results.

The total semiconductor losses during steady state operation are summarised in Table 4-I. Both VSI and CSI have similar distribution of switching and conduction losses indicating good loading of the switches. The total losses amount to 1% of the system output power (approx. 2MVA) with the VSI dissipating 14.3kW and the CSI 2.7kW which is 15.4% of the VSI losses, a level that can be considered as reasonable and typical also for the losses expected in passive filters.

The results are in line with previous estimates for the Hybrid system operation with a stiff grid showing that the system losses do not vary greatly for the different CSI operating points considered.

For a standalone VSI system that would produce the same semiconductor losses, the equivalent switching frequency will be around 1.35 kHz which will result in a limited reduction of the current ripple, significantly inferior to what the hybrid approach offers. It can therefore be concluded that the use of the CSI is done at the lowest possible cost with respect to efficiency.

Table 4-I: Estimated Semiconductor Losses in kW

	Conduction	Switching	Total
VSI losses	7,201	7,131	14,332
CSI losses	1,330	1,284	2,615
Total			16,947

4.5.2. Added Installed Power

Based on the steady state operating condition shown in Fig. 4-14 and the peak voltage and current stress values of 3 kV/560A for the VSI and 700V/164A for the CSI, the added installed power is given by (Eq. 10) at less than 3.6%, in line with the theoretical calculations.

The series capacitor is rated at 12% of the VSI output power, mainly contributed by the 50Hz component, at less than the 20% limit imposed in the design, which in terms of stress is similar to a capacitor in a standalone LCL installation. Although some additional cost will be added towards the CSI voltage protection circuit the overall installation cost is at a minimum for a MV system.

4.6. Conclusion

This chapter validates the feasibility of the hybrid concept resulting by adding an auxiliary CSI to a medium-voltage LCL filter to enhance the switching ripple cancellation while maintaining low installed power on the CSI. The design criteria to achieve low installed power in the CSI that are defining the design of the hybrid system with a stiff grid have been introduced and validated by simulations.

The LCL-CSI connection scenario which is relevant for upgrading existing MV inverter installations introduces some new design challenges related to LC resonance, which have been explored in this chapter. To address this challenge, a resonance compensator that behaves similar

to a notch filter on the resonance but guarantees zero phase-shift in the frequency range of interest for the switching ripple has been added to the control structure.

To validate the effectiveness of the proposed resonance compensator, the resonant frequency of the hybrid system has been intentionally placed near the biggest VSI current harmonics in order to demonstrate that the design requirements are not strict as long as the compensator is properly designed but the attenuation performance of the switching ripple nearest to the resonant frequency is affected. This is proven via a set of transient simulation tests by enabling the resonance compensator after the CSI was enabled and a resonance has build-up, followed by an effective removal of the resonance after the compensator was activated. Proper placement of the resonant frequencies allows for even better filtering performance. Further investigations into improving the voltage quality affected by the residual CSI switching current ripple in conjunction with high impedances due to high switching CSI frequencies have also been investigated. A study of the semiconductor power losses revealed a reasonable increase of 15% which is justified by the improved attenuation of the hybrid active filter while the added installed power remains under 4%.

SECTION B: Experimental Validation

CHAPTER 5. Experimental Setup

In order to experimentally validate the system operation, the Hybrid system has been downscaled to a standard three phase 415V grid voltage level. The following chapter will present the experimental setup. The first part of the chapter focuses on hardware system design and choices in terms of passive component and power semiconductor scaling; the second part outlines the implementation of the digital control system design within the hardware framework and the third part describes the measurement equipment used to evaluate the system performance. The final section outlines the methodology followed to obtain the experimental results presented in the following chapters of this thesis.

5.1. Experimental Rig Overview

The experimental setup involved the design of the two converters which have been assembled following a rapid prototyping approach rather than producing a fixed PCB design (normally associated with higher Technology Readiness Level TRL); thus aiming to prove the concept whilst maintaining the ability to do quick modifications, maximising flexibility.

For the purposes of validating the system operation, it was considered unnecessary to use a multilevel VSI. The benefits of using a three-level VSI in a true MV implementation have been justified in CHAPTER 2 but as the scope of the experimental assessment is weighted towards evaluating the CSI performance, the use of a two-level VSI was considered rational. The VSI and its associated switching filters have been designed for a 1 kHz switching frequency whilst a 40 kHz switching frequency has been considered for the CSI to enable for best capability to synthetize accurately the VSI switching ripple whilst loading the CSI devices with a realistic switching stress that a Si Mosfet or SiC device can handle.

The main converter design has been based on bi-directional power capability (inverter/rectifier) for a maximum power level considered. The experimental evaluation in this thesis is presented

only for rectifier operation with a DC-link load resistance selected to set the total power processed at 4kW. The series capacitor and other associated passives have been scaled according to the proposed design procedure for the operation at 4kW, although at a different operating point to the previously suggested values for reasons that will be outlined in the design section.

The converter control has been implemented using an in-house control platform developed by the University of Nottingham Power Electronics, Machines and Control (PEMC) group. A combination of a 32bit floating point DSP board and two FPGA boards (one per converter) have been used and programmed to enable the implementation of the specific control of the hybrid system at a 40 kHz sampling frequency. The control scheme has been designed and several versions have been implemented and tested to achieve the best possible steady state performance.

Measures to provide system protection have been implemented at different levels, a clamp circuit has been used to ensure the CSI overvoltage protection, hardware and software voltage and current trip limits have been set and monitored via the control platform and optic isolation has been used between the digital outputs of the FPGA and the inputs in the converter gate drivers to reduce EMI and enhance safety.

The performance assessment has been conducted using dedicated measurement equipment at a sufficient bandwidth to ensure sufficient accuracy of measurements. All tests reported in this thesis have been conducted at the full 415V grid voltage level with the PCC connection to either a three phase electronic AC supply or via an autotransformer connected to the grid.

5.1.1. CSI and VSI Implementations

The two power converters have been designed to allow for a wide range of operating points, with the VSI design considering a maximum dc voltage level of 1 kV and output power up to 8 kW although practically used at lower power. The followed design approach prioritised achieving the desirable CSI high performance to meet the necessary fast switching characteristic, while the VSI has been selected to match the higher relative voltage ratings and slow switching typically expected in this application.

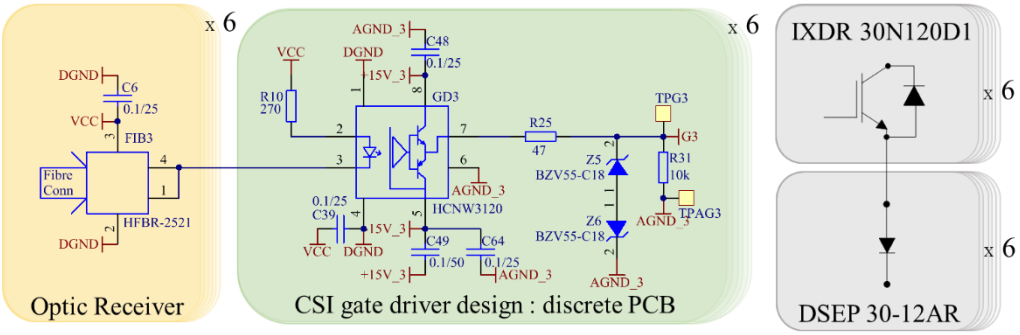


Fig. 5-1: Overview of gate driver configuration and CSI switches

In order to enable a cost effective implementation that can be also repaired quickly, it was chosen to construct the CSI using discrete IGBT devices in combination with series connected diodes used to ensure unidirectional current flow. The IXDR 30N120D1 IGBT model by IXYS, is rated at 1.2kV/50A and the 1.2kV DSEP 30-12AR soft recovery diode is rated at 30A with a typical reverse recovery time of 40ns [110]. Both devices feature electrically isolated backsides (ISOPLUS 247) to allow for placement on the same heatsink and they have been arranged to minimise the conduction and commutation paths between devices and the output filter capacitor set.

Each IGBT is soldered to a discrete gate-driver circuit printed circuit board (PCB) at the highest possible proximity to achieve the required high switching performance. The generic IGBT gate driver PCB has been kindly provided by Dr Nicholas Shattock and populated accordingly to suit the requirements of this application. The overall simplified configuration (excluding power supplies) per switch is shown in Fig. 5-1. Six optic fibre receivers (Avago R-2521Z) are used to convert the optical gate signal to TTL as required by the input of the gate drivers. Optic isolation between the power circuit and control platform is necessary to safeguard the low voltage peripherals and PC in case of a fault, as well as to prevent switching noise circulation which could deteriorate the performance. The gate signal is passed on to the HCNW3120 Optocoupler which, in combination with an isolated DC-DC power supply, provides 1.4 kV [111] of electrical isolation to each gate signal at the required ±15V gate voltage. The gate resistance has been set at 47Ω to achieve the fastest switching performance in accordance to the manufacturer

recommendation [112]. The peak resultant gate current for this resistance value is 0.64A, well within the capabilities of the gate driver IC which can provide up to 2.5A.

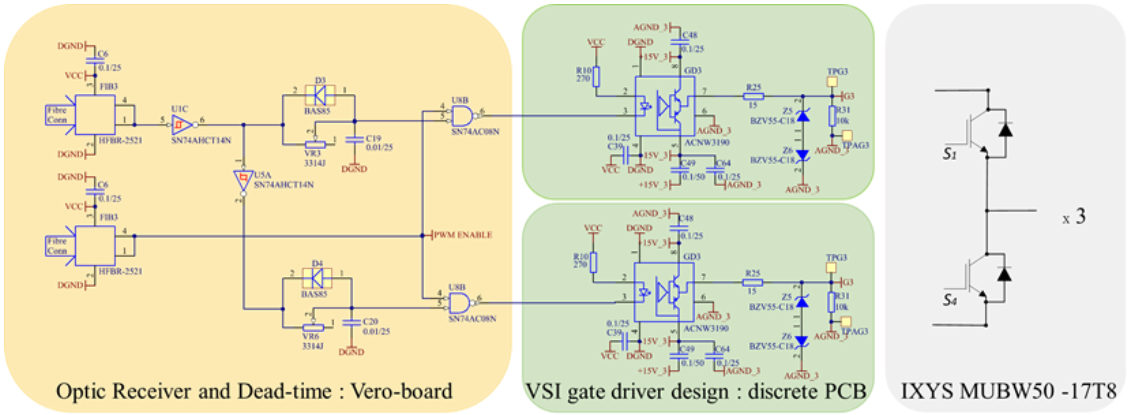


Fig. 5-2: Implementation of the optical receiver, hardware dead-time generator and the gate driver for a full leg single phase VSI.

A full 3-phase inverter leg integrated in a power module solution from IXYS has been used for the main VSI. The MUBW 50-17 T8 includes a Diode rectifier – the switches for the Braking chopper and a three phase Inverter Module combination of which only the three phase inverter has been used. The three phase IGBT stage is rated at 1.7kV and 74A which should enable experimental work with 1-1.2kV DC-link voltage. The gate drivers used are the ACNW3190 model, also providing electrical isolation, but capable of providing gate current up to 5A [113]. The gate resistance has been set at 15Ω rather than the recommended 8.2Ω [114] to slow down the switching speed, similar to the expectation for this application. Experimentally, the devices have been utilised to only a fraction of the maximum capability but the aim was to have a more reasonable reflection on losses based on the device ratings.

$$C_{dc\,min} = \frac{\Delta P * t_r}{2 * V_{dc} * \Delta V_{dc}} = \frac{2000 * 0.06}{2 * 750 * 20\% * 750} = 533\mu F \qquad \text{(Eq.20)}$$

$$\tau = RC \qquad \text{(Eq.21)}$$

The minimum DC link capacitance has been calculated to give a 20% maximum DC-link voltage change considering a power step of 2 kW based on (Eq.20) [115]. A 60ms controller delay t_r has been used considering that the inner current loop is typically around 6 times slower than the

switching frequency and the outer loop voltage controller is typically 6-10 times slower than the inner loop. Four RIFA PEH200YT4220M, 2.2 mF electrolytic capacitors rated at 450Vdc have been connected in series to increase the maximum possible DC voltage to above 1kV and give an equivalent dc capacitance of 550μF. Each capacitor has been connected in parallel to a 27 kΩ power resistor to give an RC discharge time constant (Eq.21) of 60 seconds as well as to ensure equal voltage sharing. The associated losses of the discharge/balancing resistors for a maximum dc-link of 1kV are limited to below 10W which has a minimum impact on the inverter efficiency. Finally three Vishay 1μF 2kV film capacitors have been placed in close proximity to the module to provide high frequency voltage decoupling during switching transitions.

The direct placement of the discrete gate drivers on the VSI module was physically impossible therefore short wires have been used for the gate connections. The parasitic inductance in the path to the device gate which could interact with the device gate capacitance was not found to have a significant effect possibly due to the slower switching of the VSI devices. Three optic fibre receivers have been used for receiving the gate signals from the FPGA, one per phase, as top and bottom switches in a leg are switched on in opposition. To ensure all six devices can be turned off, an additional optic fibre "enable" signal was required.

The necessary signal inversion of each phase gate signal, addition of dead-time and enable signal control have been implemented on a separate hardware stage prior to the gate driver circuit as shown in Fig. 5-2. Schmitt triggers invert the low voltage signal from the optic receiver, followed by a variable resistor to control the charging (turn-on delay) time of a 10nF capacitor whilst the discharge, significantly faster, takes place via the parallel Shottky diode. The output is connected to an open collector NAND gate along with the enable signal to select between PWM and OFF mode. The dead-time has been set at 1μs reflecting the value used in simulations.

A negative temperature coefficient thermistor (NTC) included in the module also enabled the monitoring of the internal device temperature which remained below 40º C under all experiments due to the oversized heatsink and low converter loading.

5.1.2. The Overvoltage Protection

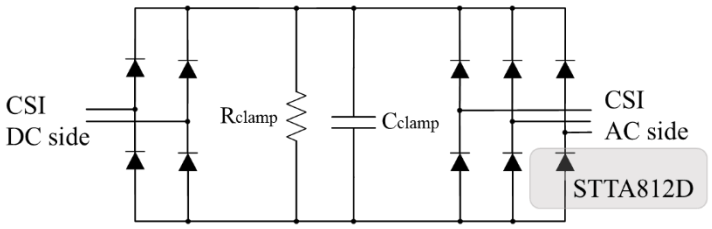


Fig. 5-3: Schematic of the voltage clamp circuit used for CSI protection and voltage monitoring

In order to guarantee CSI overvoltage protection, which is critical since in the CSI there is no natural freewheeling path for the inductive DC-link current, a clamp circuit has been connected to both the CSI DC and AC sides as shown in Fig. 5-3. Further to ensuring semiconductor safety, the clamp will absorb any CSI commutation energy but also allow monitoring of the CSI voltage stress. The diode rectifier uses STTA812D fast recovery discrete diodes by STMicroelectronics, with a quoted 50ns [116] typical reverse recovery time. The devices are rated at 1.2kV and 8A, but capable of withstanding surge currents up to 70A for 10ms.

$$E_{L_{dc}} = \frac{L_{dc} I_{dc}^2}{2} \quad \text{(Eq.22)}$$

$$C_{clamp\_min} = \frac{L_{dc} I_{dc}^2}{V_{clamp_{max}}^2 - \left(\sqrt{2} V_{rms}^{l-l}\right)^2} \quad \text{(Eq.23)}$$

The clamp DC voltage in this application can also be used to indicate the CSI voltage reduction without requiring a high bandwidth. Most crucially, when PWM is disabled or in case of an emergency shutdown, the CSI semiconductors are all turned off and the energy stored in the DC link inductance will flow into the clamp capacitor. The clamp DC capacitance (C_{clamp}) must be sized based on the maximum energy present in the CSI DC link inductor (Eq.22) for a maximum permitted clamp voltage but also considering the voltage already present across the clamp capacitor (Eq.23). For a worst case scenario where the DC-link current is at 10A and the DC inductance is 30mH, the energy in the inductance will reach 1.5 J. The minimum capacitance to absorb this energy based on a 750V maximum voltage, considering a scenario of 415Vrms line-

line AC side voltage has been calculated at 14μF. For the implementation, a 20μF film capacitor has been used with a 100kΩ resistance (R_{clamp}) chosen in order to achieve a time constant of 2s, thus making sure the clamp resistor does not absorb too much energy during steady state operation. The steady state clamp resistive losses for a worst case scenario clamp voltage of 600V reach 3.6W, but for CSI operation that results in a clamp voltage level under 200V, this drops to under 0.4W.

5.1.3. Design Procedure and Passive Component Sizing

The following section outlines the design procedure corresponding to the experimental setup used in the evaluation presented in the following chapters. The circuit has been adapted to be used as a rectifier with power transferred from the AC to the DC side. The DC load resistance has been implemented using three series connected 47Ω TE1500B47RJ (with 5% tolerance [117]) ceramic core power resistors, rated at 1.5 kW each allowing for a total power dissipation of approximately 4 kW for a DC-link voltage of 750V (Eq.24).

$$P_{dc} = \frac{V_{dc}^2}{R_{dc}} = \frac{750^2}{3*47} = 3.99\ kW \quad \text{(Eq.24)}$$

The circuit has been designed to operate at a much larger switching current ripple compared to the simulated operating point. The design procedure has been followed to account for a 50% switching ripple amplitude, as opposed to 20% considered in the simulation. For operation at 4kW with for a 415V grid voltage, the VSI fundamental current peak has been calculated around 8A:

$$\widehat{I_{L1}} = \frac{\sqrt{2}P_{dc}}{V_{rms}^{l-l}\sqrt{3}} = \frac{4000\sqrt{2}}{415\sqrt{3}} = 7.87A \quad \text{(Eq.25)}$$

The inductance required to maintain the maximum current ripple peak (DI/2) at 50% of the fundamental VSI current component(7.87A) has been calculated based on the simplified equation derived in (Eq.27) [118] for a DC voltage of 750V and 1 kHz switching frequency at 13.8mH.

$$\Delta I_{max} = 50\% * 2 * \widehat{I_{L1}} = 7.87A \quad \text{(Eq.26)}$$

$$L_1 = \frac{V_{dc} * m}{2\sqrt{3}\,\Delta I_{max}\, f_{sw}} = \frac{750 * 0.5}{2\sqrt{3}*7.87*1000} = 13.8\ mH \quad \text{(Eq.27)}$$

Due to availability, a set of three 11mH single phase inductors has been used which are close to the target inductance value. The inductors, originally commissioned for the UNIFLEX project [119, 120], are designed for operation in 3.3kV MV applications therefore having less parasitic capacitance which gives minimal high frequency current oscillations following VSI switching. The inductors are rated at 7kV and 50A. The small signal analysis of the inductance characteristic can be found in the Appendix A. The VSI switching current ripple peak (DI/2) for operation at 750V has been calculated at a theoretical maximum of 4.92A using (Eq.28).

$$\Delta I_{max} = \frac{V_{dc} * m}{2\sqrt{3}\, L\, f_{sw}} = \frac{750*0.5}{2\sqrt{3}*0.11*1000} = 9.84 \text{ A} \quad \text{(Eq.28)}$$

Series Capacitor and CSI filter scaling

The maximum value for the series capacitance assuming a reactive power limitation of 20% which was used in simulations (Eq.6) could reach 26μF which would require a maximum fundamental current component amplitude of 2.6A to achieve fundamental CSI voltage reduction to 10% of the grid. Based on the VSI current ripple peak which exceeds 4A, a CSI fundamental current component of 2.6A would require a CSI DC-link current close to 7A. As it was considered counterproductive to operate the CSI with a DC link current amplitude which would be similar to the fundamental current component of the VSI current a smaller capacitance has been chosen.

The series capacitance has therefore been designed for a 10% reactive power limitation, with the capacitor value chosen at 12μF. For this operating point the reactive fundamental current required to achieve a 10% voltage reduction has been calculated at 1.3A. For this operating point the maximum switching voltage created by the 1 kHz ripple component is calculated at 65V (Eq.7), which means that the maximum CSI voltage stress would be expected to reach up to 30% of the grid voltage, larger than the 20% reduction achieved in the simulated results but directly related to the increased switching ripple to be cancelled.

The output filter capacitance of the CSI has been chosen at 1μF which was the nearest available value around the 10% of the series capacitance while a CSI filter inductance L_f of 300μH has been

selected to place the resonant frequency at around 9.5 kHz. The filter damping resistance has been selected at 50Ω to reduce the filter amplification around the resonance point to lower than 10dB as shown in Fig. 5-4. This however compromised the attenuation for the CSI switching frequency, in particular the attenuation at 40 kHz which reaches -20dB.

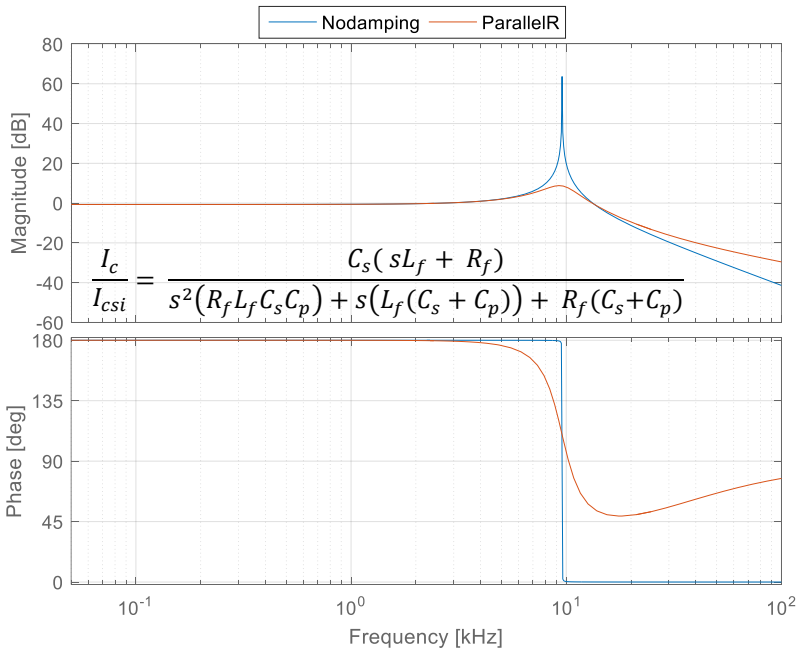


Fig. 5-4: Calculated CSI AC filter open loop response for the component values used in the experimental prototype.

The inductor of the LC filter has been designed based on the manufacturer magnetisation curves of the smallest Metglass core available (AMCC 6.3) due to the good performance (linearity) in the frequency range. To achieve the 300μH inductance with a peak current of 8A, 40 turns and a 1mm airgap have been necessary. Two strands of 0.7mm wire have been used to avoid any skin effects at 40 kHz although for this application, the presence of skin effect could be beneficial by providing additional series resistance damping at the resonant frequency of the CSI LC filter.

All three inductors have been characterised using small signal analysis for frequencies up to 100 kHz to verify the inductance characteristic. (Appendix A) Finally a 100kΩ resistance (R_{cs}) has been added in parallel to each series capacitor to clear any DC offsets however it is expected to have negligible impact on the overall filter response.

Fig. 5-5 shows the implemented VSI, Series capacitor and filter and CSI including the voltage clamp. The main features are highlighted with arrows.

(a)

(b)

(c)

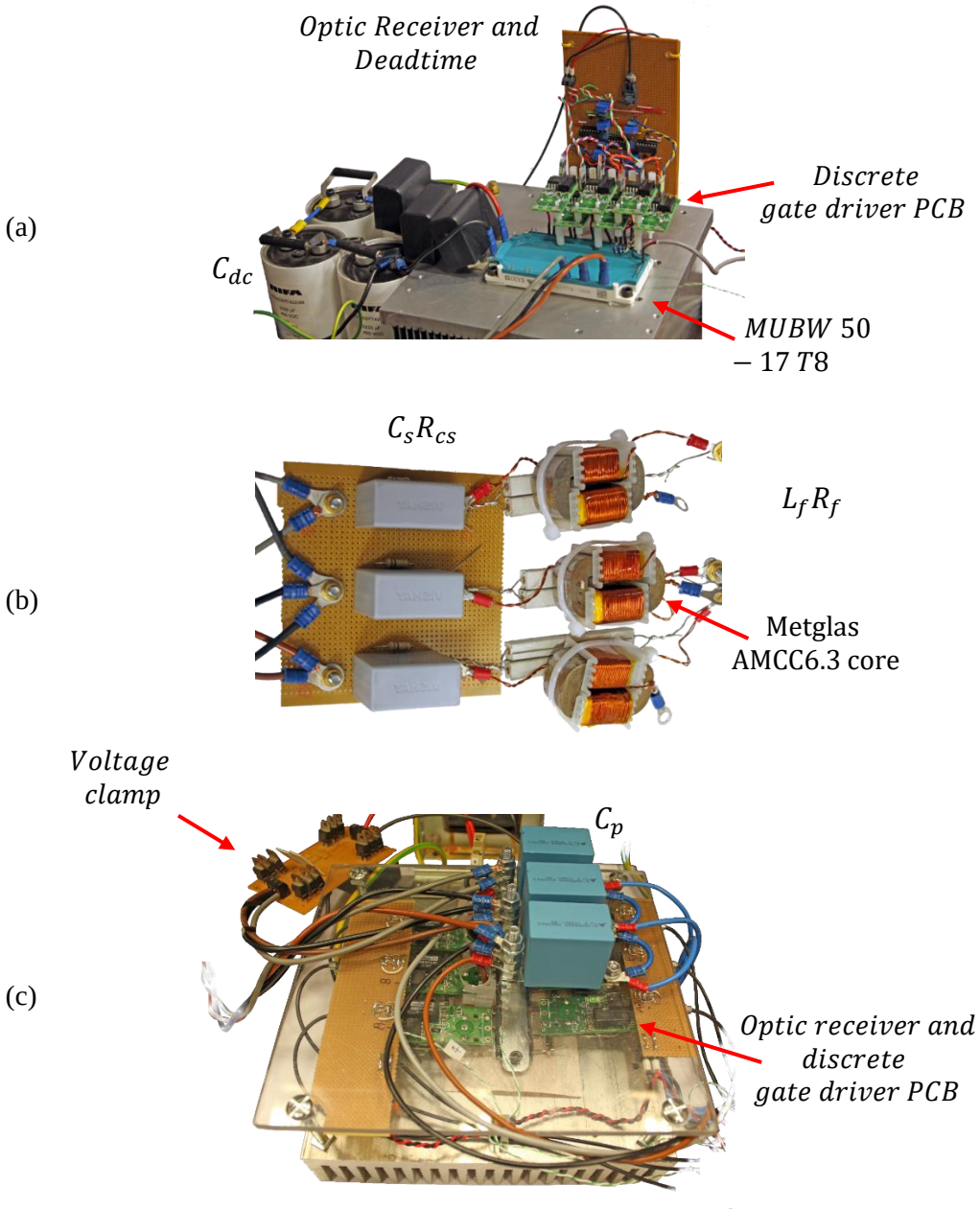


Fig. 5-5: Pictures showing the main stages of the experimental rig: a) VSI and DC capacitance; b) Series capacitor and filter inductors and c) CSI with parallel capacitors and voltage clamp circuit.

5.2. Control Platform

The control has been implemented using a flexible control platform combining a Texas Instruments TMS320C6713 DSP along with the Microsemi ProASIC3 A3P400 series FPGA IC. The FPGA board and its associated peripherals has been developed in the Power Electronics, Machines and Control Group (PEMC) of the University of Nottingham by Dr Lee Empringham around 10 years ago with further improvements also added by other PEMC group researchers. The platform has been used for the majority of research projects in the Group due to its readiness and suitability to meet the functionality required of most power electronic converter/drive applications as well as the flexibility to achieve customisation.

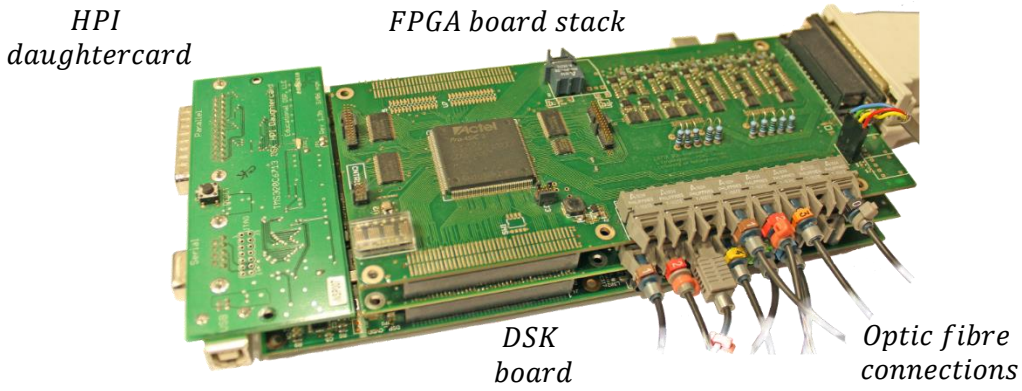


Fig. 5-6. Picture of Control platform utilising two FPGA boards and HPI daughtercard mounted on the DSK board.

The platform design is based around the commercially available TMS320C6713 DSK evaluation board designed by Spectrum Digital, utilising a 32-bit wide External Memory Interface (EMIF) which is shared with the FPGA as well as an HPI daughtercard. The now obsolete daughtercard, designed by Educational DSP, allows for fast access to the DSK memory locations without interfering with the DSP processing. The daughtercard is also used to interface the host PC via a Graphics User Interface (GUI) also developed in the PEMC group and enables the on-line monitoring, plotting as well as setting of various DSP program variables.

The DSP, clocked at a nominal frequency of 225 MHz, is used for floating point calculations while time constrained functions like PWM generation, analogue to digital conversion and hardware trip monitoring are performed using the FPGA which is clocked at 50 MHz . The FPGA board is assigned with thirty-two addressable 32-bit wide registers and features 10 analogue to digital converter (ADC) channels used for data acquisition, trip monitoring capability as well as the provision of outputting PWM signals via optic fibre connection.

The control scheme has been set up with the aim of operating the two converters independently, thus considering the retro fitment scenario. For the purposes of this project, two FPGA boards have been used, one per converter, however fitted to a single DSP thus independent converter operation is emulated and not strictly attained. A number of concessions, made to enable the converter operation for the particular setup, will be outlined in the next section.

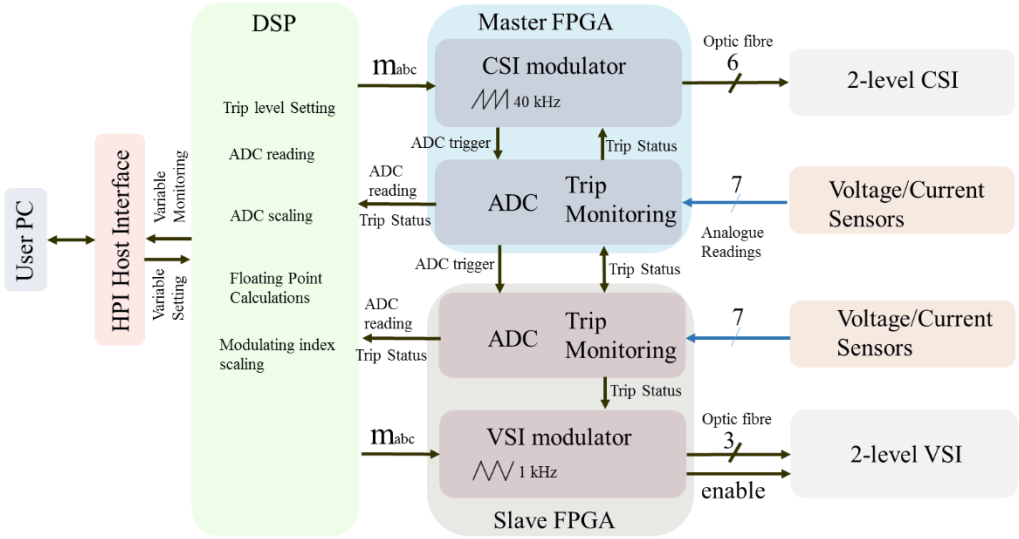


Fig. 5-7. Control platform system overview showing basic functionality associated with each element/board of the control platform

The general operation of the control platform requires that the interrupt signal, which triggers the ADC and DSP interrupt routine execution (including computation), is associated to the FPGA carrier generation. This will ensure that the modulating signal update for space vector/carrier based modulation is done at the beginning of each sampling period. As the use of multiple interrupt signals from each FPGA is not feasible, the DSP calculations must be executed at the

maximum sampling frequency. As a result the interrupt signal is generated at the CSI switching frequency using the corresponding FPGA board as the master FPGA while the second FPGA is used as a slave to control the main VSI. The main PWM interrupt routine is initiated by the master FPGA which triggers the ADC reading in both FPGAs. The slave FPGA has been programmed to generate a local interrupt signal which is used to trigger the modulating signal buffers at the VSI switching frequency. The routine is therefore executed at the CSI switching frequency also updating the VSI modulating waves, however the buffers will only release the signals to the PWM stage at the 1 kHz switching frequency or twice the switching frequency if double edge modulation is selected. The generic operation of the digital control platform implementation is depicted in Fig. 5-7.

5.2.1. VSI and CSI Modulator

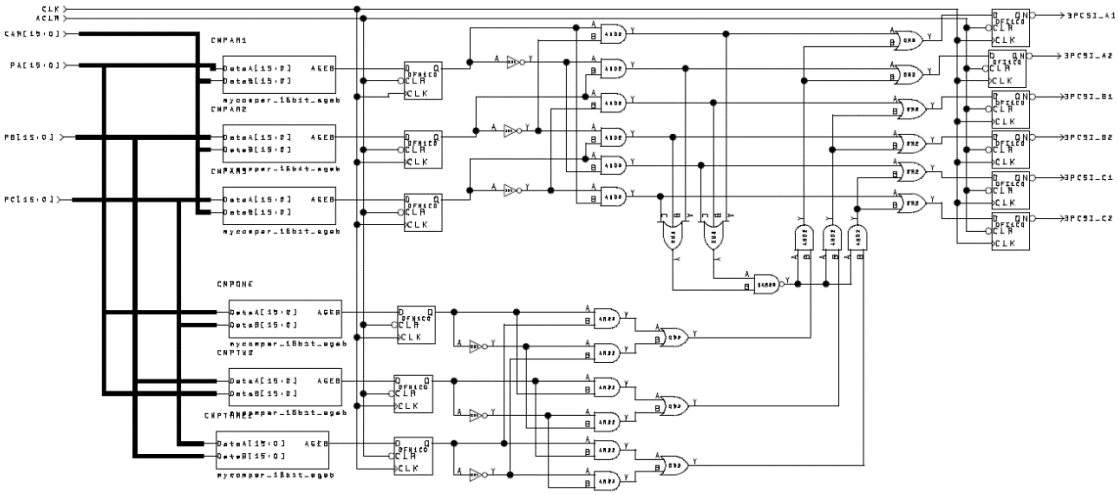


Fig. 5-8. Carrier Based three phase CSI modulator implemented in the FPGA

The CSI modulator has been implemented according to the carrier based design firstly proposed in [121]. Further studies have shown that the logic gate stage can also be implemented in combination with a method of selective harmonic elimination [69, 122]. The operation of the logic based circuit is designed to emulate space vector modulation where the sector is designated based on a comparison of the modulating signal amplitudes and the placement of a shorting pulse on the appropriate phase signals. For sinusoidal current synthesis, the shorting pulses will be arranged as such to have alternating switches clamped on for 60º during each cycle. The circuit thus

satisfies the requirement of two switches conducting at any time, providing a continuous conduction path for the inductor current. Within any given sampling period, one of the top/bottom switches will be clamped on while the bottom/top switches will actively switch to form the PWM current pulses.

For the purposes of this project, the given modulator has been found to perform well in synthetizing the required current ripple demand, despite the reference waveforms not necessarily obeying the half-wave symmetry required. Most importantly, it is particularly advantageous due to the straightforward implementation in the FPGA (Fig. 5-8) allowing for high switching frequency gate pulse generation without burdening the limited DSP computational capability; as would be the case for space vector modulation

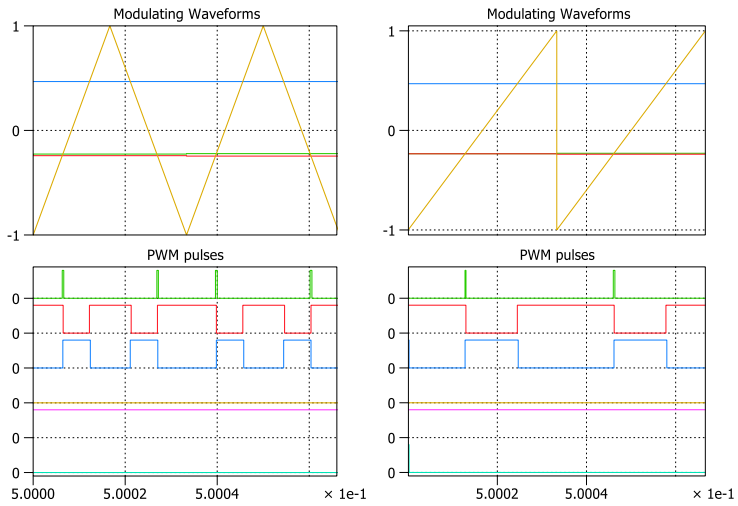


Fig. 5-9. Pulse generation for two carrier wave periods shown for triangular carrier and sawtooth carrier waveforms.

For a symmetrical triangular carrier wave, the modulator will generate two sets of symmetrically distributed pulses for each of the three active switches as demonstrated in Fig. 5-9. The advantages of this method are the symmetrical current ripple shape and the lower amplitude of the CSI switching current ripple. The output current harmonics will form clusters of similar amplitude around the switching and double the switching frequency (demonstrated in [121]) therefore requiring less filtering. This also results in symmetrical ripple on the output line-line voltage however at the cost of having three semiconductors undergoing four switching transitions per

period leading to a switching loss increase. Given that in this application the CSI is required to modulate non-sinusoidal waveforms at a high switching frequency, the split pulse distribution may be overly demanding on the semiconductor switching performance by the requirement to synthetize very short PWM current pulses. For the above reasons, a sawtooth carrier waveform has been used. The limitation is that this modulating strategy will create a larger switching current ripple compared to the triangular carrier and a larger corresponding harmonic at the CSI switching frequency, thus requires more filtering. Furthermore, it will also create the distinct slightly asymmetrical line-line input voltage shape, previously shown in §3.6.1. The modulating waves using this modulator must be scaled using:

$$m_a = \frac{2}{3}\left(\frac{I_{ref\_A} - I_{ref\_C}}{I_{dc}}\right)$$

$$m_b = \frac{2}{3}\left(\frac{I_{ref\_B} - I_{ref\_A}}{I_{dc}}\right) \qquad \text{(Eq.29)}$$

$$m_c = \frac{2}{3}\left(\frac{I_{ref\_C} - I_{ref\_B}}{I_{dc}}\right)$$

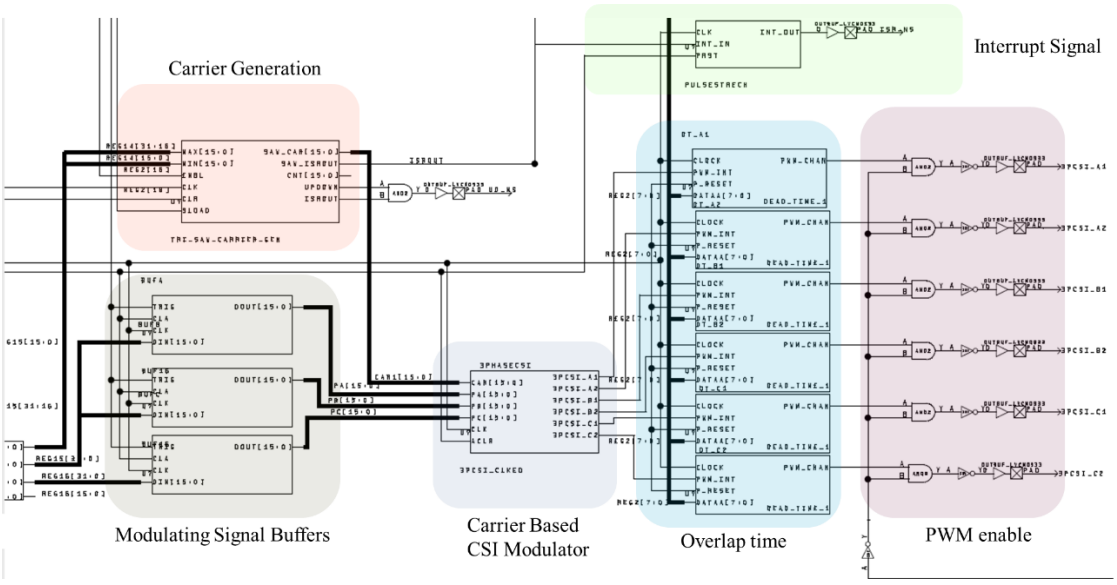


Fig. 5-10: CSI modulator, carrier and overlap block arrangement as implemented in the Master FPGA

The carrier generation in the FPGA is done using a counter, counting upwards in steps of 20ns to reach the carrier period. The interrupt which triggers the ADC reading and execution of the DSP interrupt routine, is generated when the carrier reaches the maximum value where the counting is reset to zero. The required overlap time added to the reference pulses has also been implemented in the FPGA, with the value set via the DSP at 300ns.

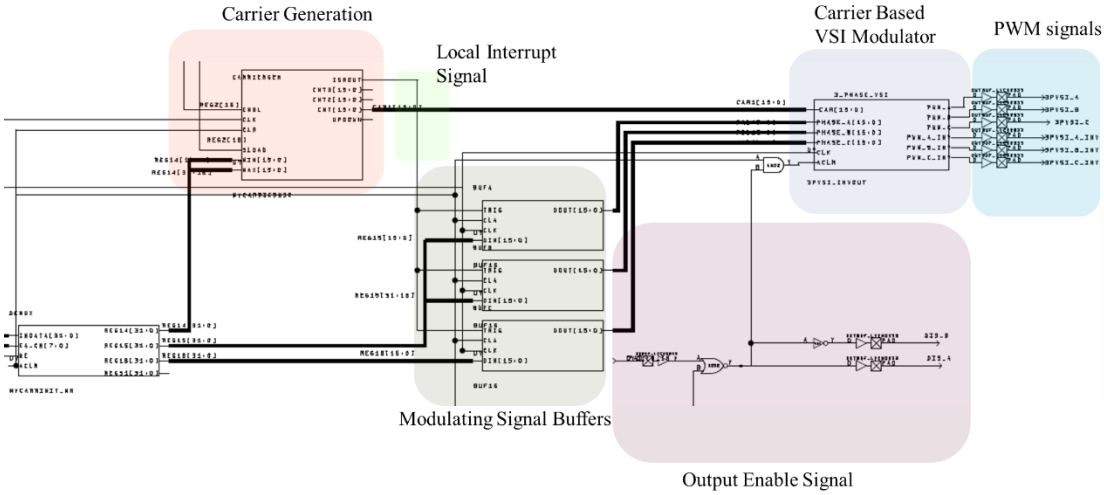


Fig. 5-11: VSI modulator, carrier and buffer arrangement as implemented in the Slave FPGA

The VSI carrier wave generation has been implemented based on a similar approach however using a triangular carrier. The carrier is generated based on a bi-directional counter, counting up/down to half the VSI switching period (in 20ns steps) where comparators are used to reset the direction of counting. As independent operation is desired, to separate from the rest of the system which is executed at the CSI switching frequency, the VSI modulator is updated on a local interrupt generated by the local carrier. The input to the comparators is therefore only updated by the modulating signal buffers at the VSI interrupt frequency as shown in Fig. 5-11. The option to switch between single and double edge sampling can be adjusted by generating the local interrupt signal upon reaching the minimum/maximum of the triangle carrier, or both. Finally the output enable signal is true if the user toggle switch is activated and no trips are detected.

5.2.1. Data Acquisition

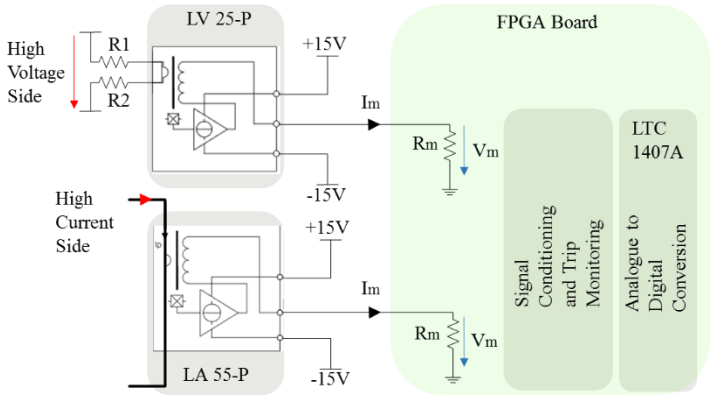


Fig. 5-12: Overview of data acquisition showing the connection of sensors to the FPGA.

Voltage and current sensing has been done using Hall Effect closed-loop current transducers. Voltage sensing has been implemented using the LEM LV 25-P model, recommended for measuring voltages up to 500V. A high and low side sensing resistor has been used, as shown in Fig. 5-12, where the total resistance (R1+R2) must be designed to limit the input side peak current for a given nominal voltage. The quoted accuracy for the recommended 10mA current is at ±0.9% of the nominal current for an ambient temperature of 25º C. The LEM LA-55P model has been used for current sensing allowing for a nominal current measurement of up to 50A. The nominal current is reduced depending on the number of turns chosen. The burden resistance (R_m), on the FPGA board, is scaled as such so that the maximum injected secondary side current (I_m) will produce a specified voltage, which can range up to ±5V. The maximum secondary side current I_m is at 25mA for the LV 25-P [123] and 50mA for LA 55P [124].

$$V_{ADC} = 1.25 - 0.25V_m \qquad \text{(Eq.30)}$$

The burden resistor voltage reading is then conditioned and scaled to the input range of the LTC1407A Analogue to Digital Converter (ADC). Each LTC1407A chip is containing two channels of 14-bit conversion providing a maximum resolution of 16384 bits for the peak to peak input signal range which in this case ranges from 2.5V(minimum reading) to 0V(maximum reading) given by (Eq.30). The conversion is triggered by the FPGA in two consecutive 32 pulse

bursts with the process requiring about 2μs. Hardware trip limits for each signal can be set at 8bit resolution (via the DSP) which sets the threshold on digital potentiometers at the input stage of each ADC. A comparator is used to trigger a trip signal if the ADC input signal exceeds the permitted limit which will subsequently disable PWM as explained in the previous sections. A calibration process is used to scale the ADC reading to the corresponding voltage/current measured.

$$Gain = \frac{Reading_{ADC} - offset}{Vpn} \quad \text{(Eq.31)}$$

The ADC readings have been calibrated (Eq.31) using dedicated equipment in order to give minimum offset (at no load) and error at an operating temperature of 30C. Practically the expected accuracy can vary depending on loading of the transducers, ambient and transducer temperature which could also depend on operating time. The calibration process may have to be repeated at a very specific time of the test, to compensate for any drift of the zero voltage/current measurement point.

The chosen values for the resistances R1 and R2 are shown in Table 5-I. It should be noted that a substantial overrating has been provided for the voltage sensing for both the nominal value considered as well as the burden resistance which has been scaled to utilise only half of the 14-bit range to prevent damage on the ADC in case of a fault. The voltage accuracy shown in Table 5-I quantifies the maximum error at the nominal reading (based on the transducer quoted percentage accuracy) which is at less than 6V for the AC phase voltage measurements. For operation under normal conditions however this value is reduced to 3V. The maximum resolution achievable via the ADC is at 146 mV for the AC side voltages, and 244 mV for the DC voltage measurement while the measurement noise at no load typically varies around 5 increments.

The burden resistance for the current sensors has been used to utilise the full 14-bit measurement range for a maximum current of 50A on the VSI inductor side currents while the maximum CSI DC-link and series capacitor current measurements have been set to 25A for a maximum current

reading, as shown in Table 5-II. This was based on the higher VSI peak current level expected in comparison to the CSI. The maximum resolution for the VSI currents has been calculated at 6mA. Although it would be possible to further increase the accuracy of both the voltage and current measurements; it has been chosen to maintain these levels to reflect the more realistic conditions as sensing equipment for medium-voltage levels would not necessarily exhibit the high performance of the sensors used in this project.

Table 5-I: Component scaling and resulting expected minimum accuracy of voltage sensors

Input	R1	R2	Vpn	Accuracy (0.9%Vpn)	Rm	Resolution
Vgrid_ph ABC	60k Ω	0	600V	±5.4V	100Ω	146mV/bit
Vc_ph ABC	30k Ω	30k Ω	600V	±5.4V	100Ω	146mV/bit
Vdc	50k Ω	50k Ω	1000V	±9V	100Ω	244mV/bit

Table 5-II: Component scaling and resulting expected minimum accuracy of current sensors

Input	Ipn	Turns	Accuracy (0.65%Ipn)	Rm	Im pk	Resolution
Idc	25A	2	162.5mA	100Ω	50mA	3.05mA/bit
Is ABC	50A	1	325mA	100Ω	50mA	6.1mA/bit
Ic ABC	25A	2	162.5mA	100Ω	50mA	3.05mA/bit

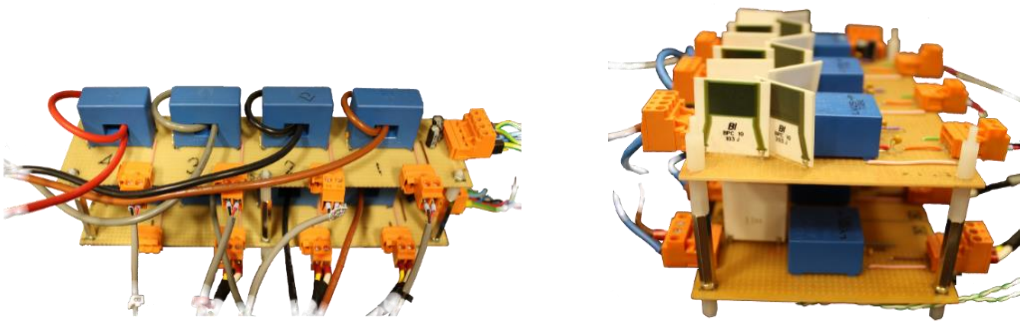


Fig. 5-13: Picture of current and voltage sensing boards

5.2.2. Control System Outline

5.2.2.1. Current Ripple Extraction and Downscaling to VSI Frequency

Based on the implementation of the control of both inverters using a single DSP, the current ripple extraction had to be combined with the need to downsample the main VSI dq current to the VSI switching frequency. As the VSI modulator is operating independently, it is not possible to control the exact sampling instance by selectively sampling the acquired measurement signals.

On the other hand, due to the larger current ripple processed, the moving average filter was found to be less effective than in simulations for the extraction of the current ripple reference. To minimise the residual oscillations on the filter output, a filter window wider than 1ms would be required, slower than the VSI switching frequency. As it was desired to achieve the best possible steady state performance, the current ripple extraction scheme was slightly modified. In the implemented control scheme, a moving average filter with a window equal to the VSI switching period has been used to downscale the sampled converter currents to 1 kHz which are then used as the measurements by the VSI current controllers. An additional low pass filter LPF has been used to provide further filtering to extract the main VSI fundamental current component. To achieve sufficient attenuation, the cut-off frequency has been set at 120Hz or lower. This is discussed further in §7.1.5.

5.2.2.2. Current Ripple Delay Compensation

As the discretisation of the control system has been considered as an implementation issue in the former parts of this investigation, the simulated and theoretical performance had been evaluated in the continuous time domain. The additional phase shift caused by the sampling delay as well as the propagation delay in the hardware implementation can hinder the effectiveness of anti-ripple synthesis.

By assuming that in steady state conditions the current ripple produced by the VSI will not vary significantly between successive fundamental cycles, a current ripple delay compensation scheme has been devised. The extracted current ripple, acquired using the control platform for one fundamental cycle is shown as number of samples in Fig. 5-14 (at 40 kHz), with three cycles superimposed on the same graph. Although minor changes can be observed under close scrutiny, the general shape of the ripple remains identical. Under the proposed method the extracted current ripple per phase is stored in an array equal to one fundamental frequency cycle (the number of array elements varies according to the sampling frequency) plus an additional 5 array elements. The instantaneous current ripple reference is then formed by reading the stored array element corresponding to the previous cycle and delay time. Under the aforementioned assumptions it is therefore possible to compensate for a sample delay of up to 5 samples. The main drawbacks of this method are the possible loss of accuracy in the current synthesis and the additional implications associated with VSI transient conditions which have not been investigated.

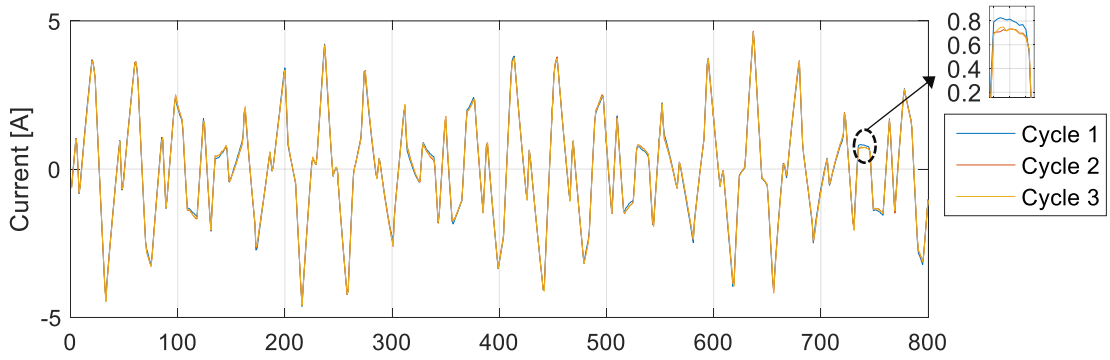


Fig. 5-14: Extracted VSI current ripple superimposed for three consecutive fundamental cycles captured via the control platform

5.2.2.1. Equivalent Control system

The trapezoidal rule has been used for the implementation of the discretised PI controllers which was found to offer a better performance although with the limitation that the output of the integral and proportional part cannot be monitored separately. To provide controllability of the VSI DC-

link Voltage, an additional PI controller was implemented whose output is the reference for the VSI active current component. With the K_p and K_i constants chosen, the bandwidth of the VSI current controller has been calculated at 290Hz (K_p=20, K_i =500) while the outer loop for the VSI DC- link voltage controller, the bandwidth was set at 5 Hz (K_p=0.01, K_i =0.5). Due to residual ripple in the dq currents on the output of the moving average filter, the cross-coupling d/q terms due to the line reactance have been omitted. The feedforward of the grid voltage V_q term, which was initially assumed to be zero as the initial investigations have been performed in ideal grid conditions, has also been left out. It will be later shown in CHAPTER 7 that in the case of grid voltage unbalance, omitting the grid voltage q-axis feedforward terms will have a negative influence on the output VSI currents which can subsequently affect the CSI performance.

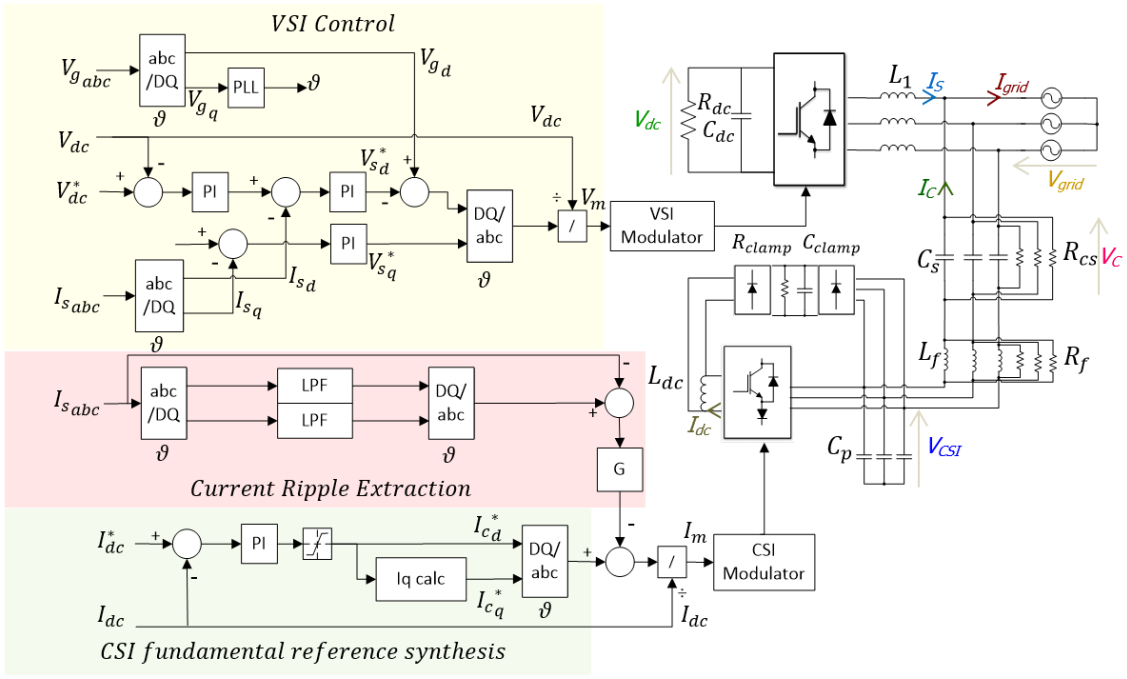


Fig. 5-15: Equivalent control system diagram and circuit interconnection

The CSI DC-link current controller K_p and K_i have been set at 0.03 and 1 respectively (bandwidth 0.9Hz), to provide DC link controllability without being able to undergo fast transients which could interfere with the output voltage balancing The CSI reactive current reference has been calculated based on (Eq.15) for a nominal grid voltage of 240Vrms and a series capacitance of

12μF while K has been set at 10% but with the option of on-line adjustment along with the corresponding active current limit.

$$\mathbf{I_{c_q}} = \frac{\hat{V}_g^{ln} - \sqrt{\left(K\hat{V}_g^{ln}\right)^2 - \left(I_{c_d} X_c\right)^2}}{X_c} = \frac{340 - \sqrt{(K*340)^2 - \left(I_{c_d} * 265.26\right)^2}}{265.26} \qquad \text{(Eq.32)}$$

5.2.2.2. Main Interrupt Execution Time Minimisation

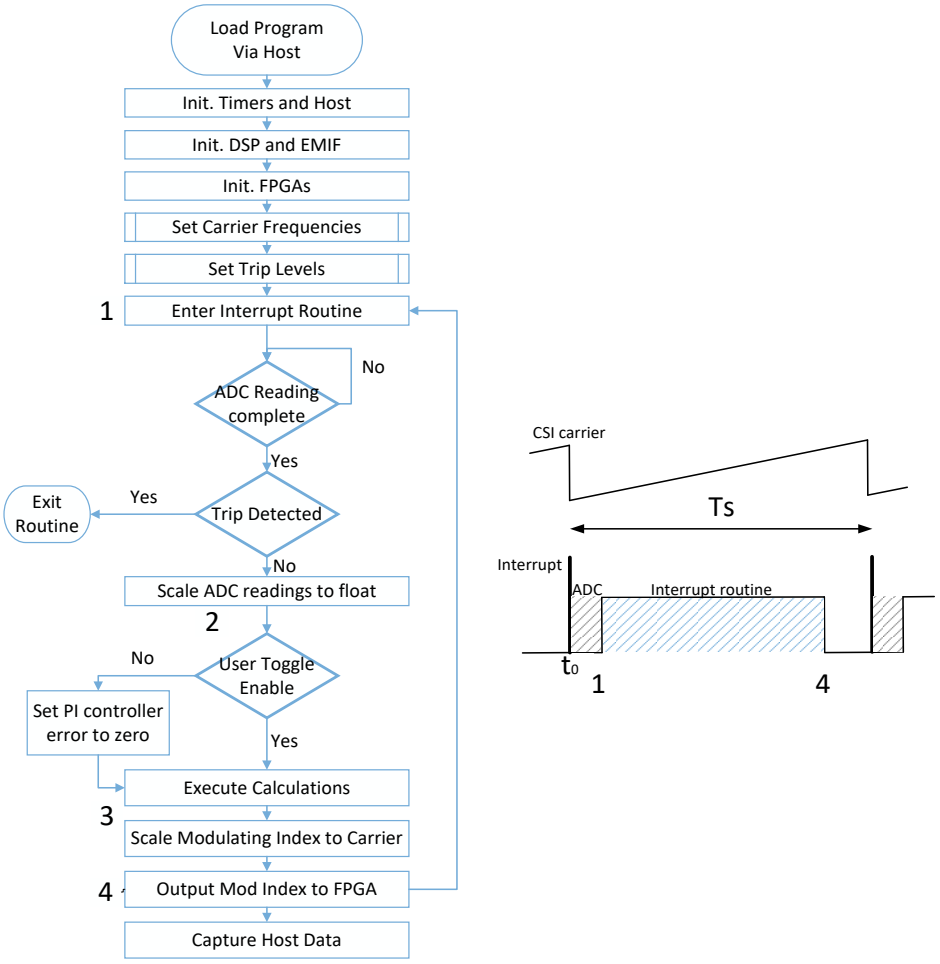


Fig. 5-16: Flowchart of DSP initialisation procedure and execution of the main interrupt routine

One of the major practical challenges in the implementation of the hybrid system has been the control of both inverters at 40 kHz using the rather limited DSP processing power. The processing time required to execute the basic routine including reading and scaling ADC signals and writing in the FPGA registers but excluding calculations, has been measured at 12.5μs. Minimising the execution time has not been a straightforward task with several optimisation steps taken to enable execution of the interrupt routine in less than 25μs, equivalent to 40 kHz. Fig. 5-16 shows the

flowchart corresponding to the DSP initialisation process and the main interrupt routine execution with an equivalent timing diagram shown on the right. For the implemented code required for this project, the following processing time has been recorded starting from t_0 when the interrupt signal triggers the ADCs: step 2 is completed at t_0+8.75μs, step 3 (calculations) is completed at t_0+18.5μs and finally the interrupt routine execution (end of step 4) is finalised at t_0+ 22μs, at 88% of the 40 kHz period. To achieve the fitting of the routine execution within 90% of the period the following measures have been taken:

The DSP code has been optimised to reduce the number and type of calculations performed. Mathematical operations (Sin, Cos, sqrt) have been performed with single precision commands which are executed faster while still maintaining 32-bit accuracy. The use of divisions, which are the most computationally demanding operations for the given processor, has been limited to two, necessary to scale the modulating index by the instantaneous DC level of each converter. Only one Sine and one Cosine calculation has been performed on the PLL angle. All Park/Inverse Park transformations have therefore been performed only with multiplications via the use of trigonometric identities:

$$\cos\left(\theta \mp \frac{2\pi}{3}\right) = \cos(\theta)\cos\left(\frac{2\pi}{3}\right) \pm \sin(\theta)\sin\left(\frac{2\pi}{3}\right)$$
$$\sin\left(\theta \pm \frac{2\pi}{3}\right) = \sin(\theta)\cos\left(\frac{2\pi}{3}\right) \pm \cos(\theta)\sin\left(\frac{2\pi}{3}\right) \quad \text{(Eq.33)}$$

All calculating functions have been grouped and separated from the main execution routine to allow for compiler optimisation, which can give up to a 30% performance increase. The use of the latter has not been a trivial task, requiring precaution as to ensure the correct execution of all calculations.

Furthermore the DSP clock frequency has been increased to 300MHz, as opposed to the 225MHz nominal value, to provide an equivalent decrease in calculation time. As the placement of a heatsink is not possible due to the stacked PCB arrangement, to protect against overheating the DSP, a thermocouple has been placed to monitor the processor external temperature. This has

been checked to ensure it remains below 50º C, at a safety margin from the maximum 90º C internal temperature quoted in the datasheet [125].

5.3. Methodology

This section outlines the considerations and approach taken towards evaluating the system performance. The first section outlines the specifications of the measurement equipment used to evaluate the hybrid system performance. The procedure followed to capture the experimental behaviour under different operating modes is then outlined. The final section presents the different grid interconnection scenarios considered.

5.3.1. Measurement Equipment

To avoid any limitations set by the control platform measurement accuracy and sampling frequency, the performance evaluation presented in the next chapters has been conducted using dedicated measurement equipment and the data has been subsequently correlated through different evaluation methods to account for any discrepancies. The sampling frequency limitation of the control platform has been considered inadequate for evaluation of harmonic performance and as a result, the waveforms captured through the HPI interface have only been used to depict the operation of the internal control by analysing the state variables, where necessary.

Oscilloscope, differential voltage probes and current probes.

Two four-channel oscilloscopes have been used for the measurement of time domain signals. Particular effort has been put in the maximum utilisation of their capabilities along with the available measurement probes. LeCroy WaveRunner HRO 64Zi 12-bit scope has the highest bandwidth of 400 MHz [126] while the second oscilloscope used was the 200 MHz LeCroy WaveSurfer 424 8-bit scope. Both are capable of sampling at 2 Giga-Samples (GS/s) although the former is restricted by the available memory limitation which can reduce sampling rate to values as low as 250 kS/s for a large capture window (1s). For the majority of waveforms presented, the number of samples captured from the 12-bit scope are ten times larger than the 8-bit scope for the same window length. As the main aim of the experiments is to validate the CSI

current ripple cancellation capability, the 12-bit scope has been used exclusively to capture the more dynamic current waveforms, while the 8-bit scope has been set to capture the voltages where the bandwidth and accuracy requirement is less demanding.

The following LeCroy current measurement probes were used: one CP030 and two AP015[127] models both with specified 50 MHz bandwidth, capable of measuring up to 50A, with ±2% accuracy for readings up to 30A at a minimum sensitivity of 10mA/div. These current probes have been used along with the high bandwidth scope to capture the AC side current waveforms where it was important to accurately measure the harmonic content. The fourth current probe was a lower performing LeCroy CP150A model which has been used to measure the CSI DC-link current which remaining fairly constant is less affected by the decreased sensitivity limitation of 200mA/div and lower bandwidth (10MHz).

All voltage measurements have been captured using four LeCroy ADP300 differential voltage probes capable of measuring up to 1400V with a maximum sensitivity of 1V/div and 20MHz bandwidth. The experimental procedure has been adjusted accordingly to account for the relatively limited resolution and noise levels of these voltage measurements. The assessment of no load voltage measurement resolution at different scaling can be found in Appendix J.

Power analyser

In order to evaluate the harmonic performance and impact of the hybrid solution on losses and reactive power, accurate voltage/current/power measurements had to be taken using a high spec N4L 5530 power analyser (30Arms 1kVrms) with 2MHz bandwidth, connected in a three-phase two-wattmeter setup [128] to correlate the current THD measurement with the harmonic quality observed in the time-domain. Additional measurements have been taken for AC grid and DC power of the VSI, displacement power factor (DPF), AC voltage frequency, and current THD for phases A and B. The power analyser has been connected to the host PC allowing for real time monitoring and capturing of results which were logged at 1 second intervals for a duration of a

few minutes considering that the hybrid system needs some time to settle when transitioning between the main modes of operation.

5.3.2. Experimental Procedure

The performance evaluation is carried out at different stages (§5.3.2.2) for each circuit configuration/interconnection considered. The performance is investigated in different modes of operation (§5.3.2.1) from start-up with full input voltage at the terminals, towards achieving the full hybrid operation performing switching ripple cancelation. This gave the opportunity to scrutinise the behaviour with emphasis on aspects affecting the desired operation.

5.3.2.1. Evaluation under Different Modes of Operation

For the circuit setup where the VSI is operating as a rectifier with a resistive DC load, three main modes of operation have been identified and assessed:

- **PWM disabled**: during this mode, the VSI is operating as a diode rectifier drawing distorted load currents. The VSI dc-link is below the reference level and in consequence the power absorbed by the load resistors is smaller than in the other operating modes. The same is the case for the currents towards the voltage clamp circuit although it is not shown as the amplitude is minimal. During this mode of operation, the majority of the grid voltage is seen across the CSI input voltages.

- **Fundamental voltage reduction - PWM enabled without current ripple cancellation**: during this mode of operation the VSI DC-link voltage is at the reference value while the large current ripple on the Main VSI currents propagates into the grid. The CSI synthesises only the fundamental current component required to cause the desired fundamental voltage drop on the CSI input voltages (reactive component) and to maintain the DC-link current at the reference value (active component).

- **Full hybrid system operation – current ripple cancellation enabled**: during this mode of operation, the switching current ripple cancellation is activated. The CSI will synthetize the anti-ripple shape required to achieve a sinusoidal grid current shape. The current ripple injected through the series capacitors will create additional harmonic voltage across the series capacitors and in consequence, across the CSI inputs. The added

installed power is evaluated by the maximum voltage and current stress in each converter during steady state in this mode of operation.

5.3.2.2. Different Measurement Stages

As the simultaneous observation of the plethora of operational waveforms, done in simulation, is unattainable, the experimental procedure has been adjusted to accommodate for the limitation imposed by a relatively reduced number of available measurements (8 oscilloscope channels). As a result, each circuit configuration tested, has been evaluated several times with different measurement points and settings.

Transient and steady state operation for Phase A

To validate the feasibility of the proposed hybrid system operation, it was deemed necessary to observe the relative voltage reduction/sharing with respect to the grid voltage as well as the current harmonic improvement with respect to the main VSI current. This has been possible by using the available measurements to monitor voltages and currents on Phase A as well as the converter DC sides. The corresponding waveforms for the VSI current, Grid current, CSI DC-link and AC current have been captured using the high bandwidth scope and the Grid voltage, CSI voltage, Series capacitor voltage and VSI DC link Voltage were acquired using the low bandwidth scope. The resulting waveforms have been captured at the same instant by synchronising both scopes in a master-slave connection using an external trigger output (master)/input (slave) signal.

The results from this test are presented for key transient moments between the aforementioned modes of operation. The simultaneous activation of PWM in both converters (before ripple cancellation is enabled) is used to demonstrate that the CSI fundamental voltage is reduced via the fundamental current injection through the series capacitor. The second transient is used to reveal the activation of the harmonic cancellation which will demonstrate the elimination of VSI switching ripple from the grid current and the additional voltage ripple across the CSI capacitors

following the activation transient and during steady state. Results are also presented for Phase A under steady state operation.

Three-phase CSI voltage measurement

For the above capture, the voltage scaling in the corresponding scope had to be set at around 200V/div, which resulted in relatively low resolution and reduced accuracy for assessing the maximum CSI voltage. Furthermore, as only one phase is monitored due to limitations of available acquisition channels, phase symmetry between the voltages cannot be guaranteed and the maximum CSI voltage stress, given by the peak of all three line-line voltages, cannot be quantified.

The assessment of the maximum voltage stress has been performed in a separate test, where all three CSI input voltage have been measured after voltage reduction reached steady state using a lower volts/div setting to minimise the measurement error. The three phase CSI voltage measurement will also depict any unbalance occurring between phases. It will be therefore shown that the DC-link voltage of the clamp circuit can also be used as an accurate indication of the maximum CSI voltage stress and for this reason will be used in subsequent tests where acquisition of all three CSI input voltage was not possible.

Power quality and efficiency measurement

The assessment of the hybrid system performance using the Power Analyser has been conducted in a similar test where the procedure of transitioning between diode rectifier to PWM operation and then full system operation has been performed over a duration of 150s. The power analyser measurements have been logged at 1 second intervals for: 30 second of operation before PWM is enabled followed by one minute after PWM is enabled (without current ripple cancellation) and one minute of full Hybrid system operation. These power analyser measurements have been used to correlate the time domain and frequency domain performance observed using the oscilloscope.

5.3.2.3. Other Aspects of the Experimental Procedure

Other minor details which may be noteworthy of the experimental procedure are detailed in the following section. The use of the HPI daughtercard played a significant role in the development and optimisation of the circuit performance. The host interface (GUI) has been modified with the option of automatically performing FFT on the captured waveforms to monitor and assess harmonic performance online allowing for rapid modifications/adjustments of the control. The host interface has also been used to make minor calibration adjustments to the ADC measurement offset at the beginning of each experiment to compensate for momentary drifts noticed.

A thermocouple data logger (Picolog TC-08 [129]) has been used to monitor the CSI device temperatures as well as the DSP temperature as mentioned previously. Finally the resistor bank temperature has been monitored using a Fluke Ti25[130] thermal camera as the temperature with forced cooling exceeded 300º C at full rig power which was very close to the maximum dissipation power of the resistors. For safety purposes the testing has been restricted to short stints, of up to 15 minutes, also to minimise harmonic pollution towards the grid when operating the VSI without performing harmonic cancellation.

5.3.3. Different Grid Scenarios

The aforementioned experimental procedure has been performed in its entirety for the following grid interconnection scenarios considered.

Ideal grid: The hybrid converter performance is firstly evaluated under the most ideal conditions, connected to a three phase electronic AC source to validate the performance with balanced and sinusoidal grid voltage waveforms and negligible grid side impedance where the highest performance is achieved. The performance evaluation for this configuration is presented in CHAPTER 6. To ensure that the sampling frequency does not affect the VSI performance and investigate the effects of varying the CSI switching frequency, the performance is evaluated and compared over a range of selected CSI switching frequencies.

Real power grid: CHAPTER 7 evaluates the converter performance and operation under real grid conditions that is reflected by the presence of grid voltage imbalances and harmonics which constitute a more challenging operating environment for both the VSI and CSI. The hybrid topology is interfaced to the grid via a three phase autotransformer (Variac) set at the full grid voltage. The interaction between the VSI controllers with the grid voltage imbalance makes the ripple extraction to output also low frequency disturbances which have an impact on the voltage reduction capability of the CSI. A revised control system is subsequently proposed for the CSI to mitigate the effects of voltage unbalance with the experimental procedure repeated and the performance reassessed.

Real power grid & filter: The hybrid converter operation is also evaluated in §7.2, operating under the same real grid conditions but with an added LC filter between the connection of the series capacitors and the Variac. The performance is thus evaluated under resonant conditions albeit to a lesser extent than investigated in CHAPTER 4.

The grouped power analyser results and three phase current quality assessment is presented in CHAPTER 8 where an overall comparative assessment of the performance is done for all the different grid interconnection scenarios considered.

5.3.1. Minimisation of CSI Voltage Stress

For each of the above circuit configurations the CSI DC-link current reference was set at the minimum possible value to provide sufficient harmonic reduction. The fundamental voltage drop coefficient K was subsequently adjusted to the lowest possible value to provide minimisation of the fundamental voltage drop across the CSI whilst also ensuring that the CSI active current component does not reach the saturation limit (Eq. 8) which would distort the results. Due to the different operating conditions outlined in the next chapters, the active current component required to sustain the DC-link current at the reference value varied, depending on the minimum fundamental voltage which in turn limits the CSI input active power. For each test, the coefficient K is quoted along with CSI active current component limit.

CHAPTER 6. Experimental Validation under Ideal Grid Conditions

This chapter presents the results and performance evaluation of the Hybrid converter under ideal operating conditions used to achieve experimental validation in line with the simulated results. The hybrid system is evaluated in a wide range of CSI switching frequencies allowing for the investigation of different effects and their impact on the hybrid system performance.

6.1. Main VSI Operating as Rectifier Connected Directly to a Pure Three Phase AC Sinewave Supply

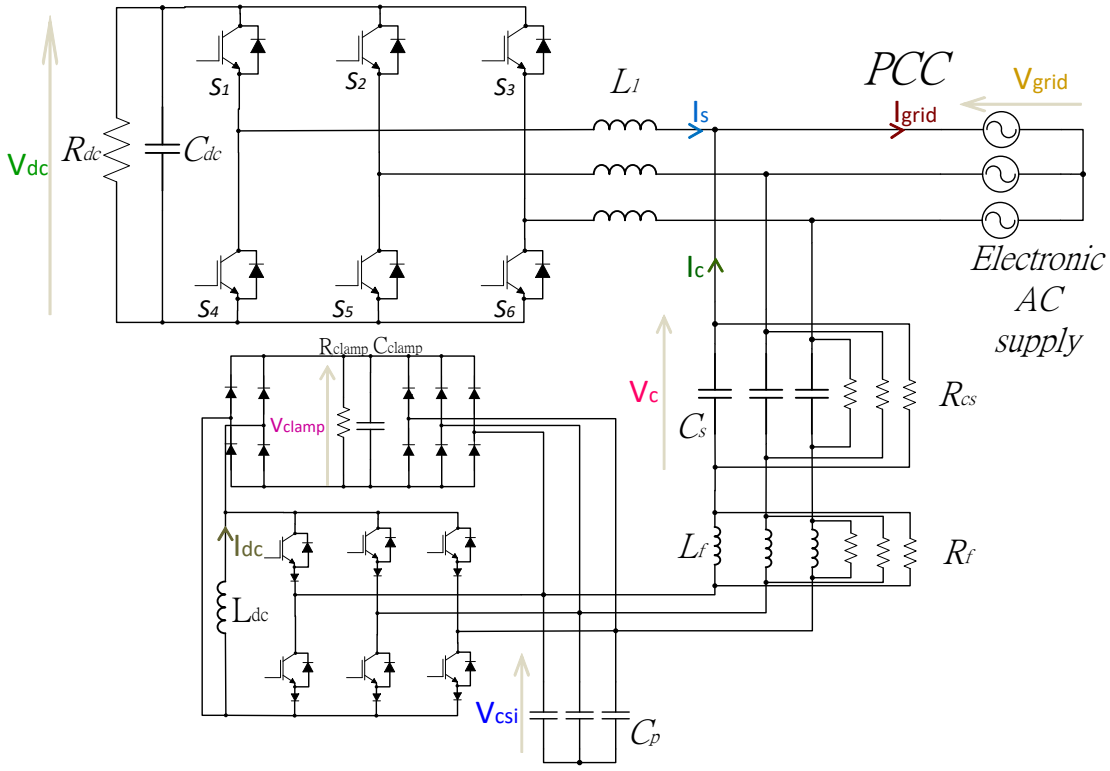


Fig 6-1: The circuit topology of the experimental setup.

In order to evaluate full extent of the ripple cancellation potential of the hybrid solution, a three phase electronic AC power supply (12kVA Chroma 61705) set to generate a set of perfectly balanced pure sinewave voltages has been used, that emulates the best a stiff grid with negligible impedance thus allowing for comparison with the theoretical and simulation results shown in CHAPTER 3. The experimental setup is briefly introduced before results are presented for the converter DC sides and phase-A currents and voltages captured at key transient moments to validate the voltage reduction and ripple cancellation. The maximum CSI voltage stress is determined in a separate test by capturing three phase voltages; also establishing series capacitor voltage balancing by verifying symmetry between phases. The performance is also compared and correlated to results captured using a power analyser. Finally the results are also presented for the circuit operating with different CSI switching frequencies to investigate the effect of sampling and switching frequency.

6.1.1. Experimental Setup

As the AC power supply can only provide unidirectional power flow, all experimental results are acquired having the VSI operating in rectifier mode with a resistor connected as a DC-link load as shown in

Fig 6-1. Due to the presence of DC-link inductance, a clamp circuit is connected on both the DC and AC sides of the CSI to provide overvoltage protection in case of an emergency shutdown and since the clamp circuit collects the largest voltage seen across the CSI switches, to provide voltage stress monitoring. The component values and operating conditions are summarised in Table 6-I.

Table 6-I: Component values and operating parameters for experimental topology

R_{dc}	C_{dc}	L_1	L_f	L_{dc}	R_f	R_{clamp}	R_{cs}	C_{clamp}	C_s	C_p
140Ω	550µF	11mH	300µH	30mH	50Ω	100kΩ	100kΩ	20µH	12µF	1µF
P	V_{dc}	V_{grid}	I_s	I_{dc}	K	I_{c_d} lim	I_c max	f_o	f_{sw}^{VSI}	f_{sw}^{CSI}
4.2kW	750V	415 V_{rms}	8Apk	5A	10%	128 mA	1.286 A	50 Hz	1 kHz	40 kHz

The reactive power compensation loop which would enable the main converter to compensate the reactive current injected by the CSI associated with the voltage reduction and achieve unity power factor has been omitted. This allows to quantify the impact of the CSI reactive current requirement (associated with the series capacitors) on the power factor and demonstrate that the reactive power injected is very small.

Furthermore, the DC voltage compensator loop presented in 3.4.3 has been disabled to verify expectations that in a practical setup any DC Voltage components will be restrained to small or negligible levels, also assisted by the presence of resistance (R_{cs}) placed in parallel to the series capacitors.

6.1.2. Transient and Steady State Operation Results for Phase A

The first set of results presented for phase A has been captured to show the transition for enabling PWM for both converters, focusing on the fundamental CSI input voltage reduction and subsequently the deployment of current ripple cancellation for full operation performance evaluation.

For the purposes of this test it was required to capture the relative amplitudes of the voltages on an increased scale (200V/div). Due to the limited capabilities of the voltage scope and probes, one bit filtering was enabled on the scope ADC to prevent measurement noise (ranging around 10V) from interfering with the results. The implication is that the filtering will also affect the high frequency switching ripple created by the CSI. Nevertheless the filtering has little effect on the evaluation of fundamental voltage reduction and voltage frequency analysis at the fundamental and VSI switching frequency which is the target for quantifying the fundamental voltage reduction.

The evaluation of the maximum CSI voltage stress under full system operation, where the overall amplitude must take account the effect of the ripple at the switching frequency and symmetry between all phases has been performed separately at a lower voltage scale for increased accuracy by measuring all three phase voltages and is presented in the steady state analysis of this section.

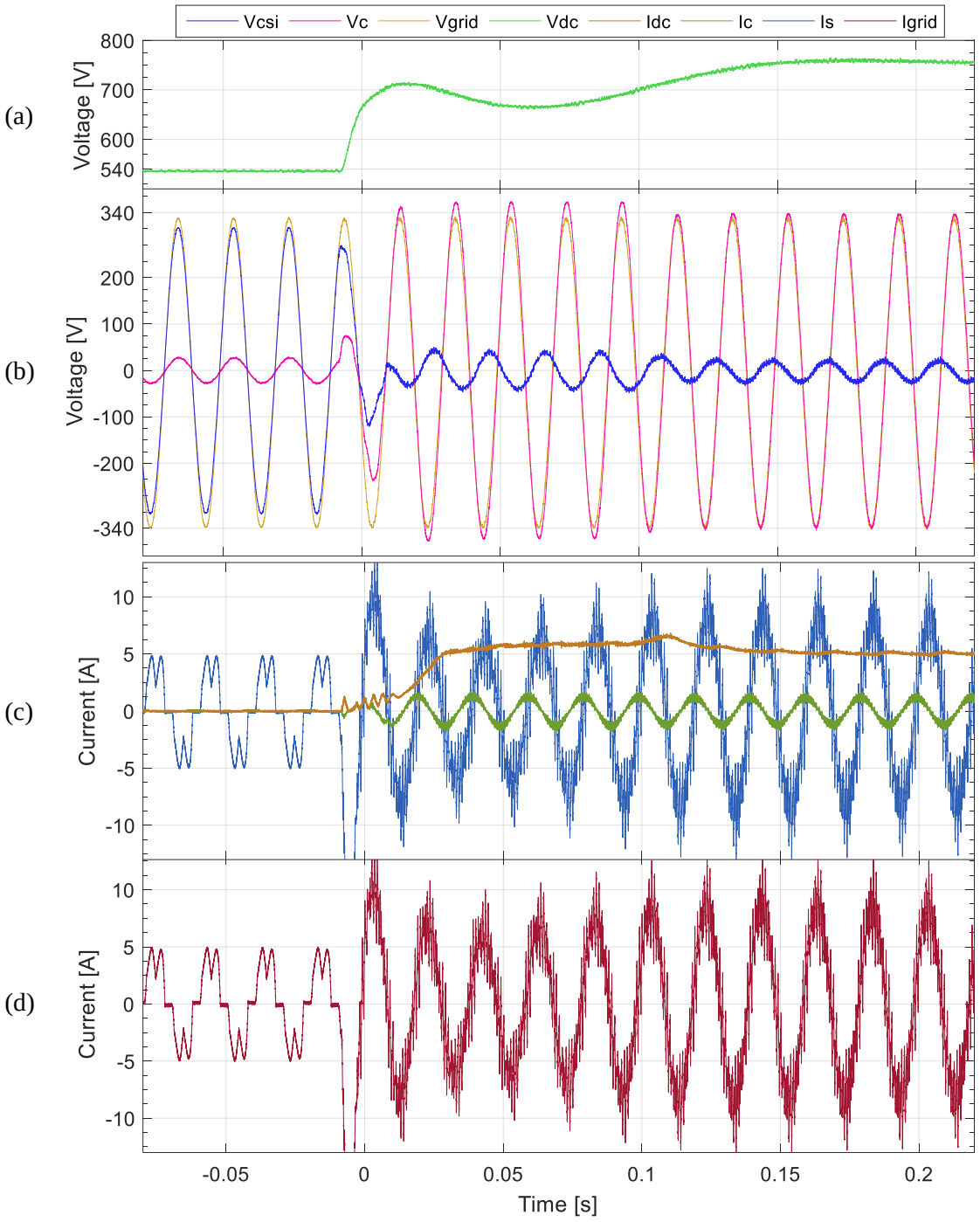


Fig 6-2: Experimental results showing PWM activation for VSI and CSI for K=0.1 (sans ripple cancellation) for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

Fig 6-2 shows the VSI and CSI DC and phase-A voltages and currents during system start-up. Before PWM activation, the VSI is operating as a diode rectifier non-linear load, therefore accounting for the grid and VSI current distorted shape, drawing a measured 2kW of power to the DC load resistor, with the VSI DC-link mean voltage at 536V. The grid voltage peak has been measured at 340V. Key measurements for minimum, maximum, mean and RMS values for all waveforms are provided in Appendix C for each mode of operation. Due to a very low current absorbed by the CSI filter capacitors (CSI disabled), most of the grid voltage can be seen across the CSI inputs with the peak fundamental at 307V for a grid voltage peak of 328V. The voltage sharing proportion of approx. 8% across the series capacitor (27V) is reflecting the ratio of the capacitances C_p and C_s (1/12) with both voltages appearing in phase.

Upon activation of both the main VSI and CSI converters at time (t=-8ms) an initial current overshoot, observed at the converter and grid current (Fig 6-2c-d), leads to a steep increase in DC-link voltage towards 700V (Fig 6-2a) until t=0s. The dynamic behaviour of the VSI controller (proportional control is predominant during initial moment of the start-up) then creates an initial dip at 660V before the VSI DC-link voltage ramps up to the 750V reference value with the DC load power dissipation increasing to approximately 4.2kW.

Fig 6-2c shows that once the DC-link current of the CSI is high enough to facilitate the synthesis of the desired fundamental AC current production, it becomes immune to any subsequent DC-link current controller overshoot due to the feedforward compensation of the DC-link current variation. The CSI DC-link current overshoots to 7A for about 0.12s. During the transient period the active current component is clamped at the maximum limit of 128mA (Eq. 8).

Fig 6-2b shows the activation of the CSI causes an immediate reduction of the CSI voltage within one cycle however the CSI controller saturation results in a slight voltage misalignment reflected by the phase shift of 130 degrees between the CSI and series capacitor voltages. During this five cycle period, the CSI voltage reduces to 44V while the series capacitor voltage increases to 360V indicating a temporary shift from the desired operating quadrant (see §3.3.2). At time t=0.12s the

voltages are realigned and all controllers reach steady state. The peak CSI input voltage in steady state has been recorded at 31V, which is within the theoretical value of 10% of grid voltage (~340V peak phase) while the series capacitor voltage has been recorded at a 336V.

The activation of ripple cancellation, shown in Fig 6-3, results in an immediate and significant improvement of the grid current quality observed by the disappearance of the VSI switching ripple from the sinusoidal grid current waveform (Fig 6-3d). The additional power required to synthetize the ripple causes the CSI DC-link current to dip to 4.5A before reaching steady state within one cycle (Fig 6-3c). The mean DC link current with only fundamental current synthesis ($t<0s$) has been measured at 4.97A with the peak measured at 5.14A and the minimum at 4.84A with the oscillation caused at the second harmonic. Under full operation, the DC link current ripple increases by the harmonic cancellation with the peak measured at 5.5A and trough at 4.5A while the mean is at 4.99, close to the reference value. As expected, the VSI DC-link voltage (Fig 6-3a) and main VSI current I_s remain unaffected by the transition to ripple cancellation. The mean DC voltage has been calculated at 753V with the slight discrepancy between the reference values accounted by an offset of the DC voltage sensor value. The maximum value, defining the peak VSI voltage stress has been measured at 760V.

In accordance with theoretical and analytical expectations, the voltage drop caused by the switching current ripple as it passes through the series capacitors, is mirrored on the CSI inputs, since the main AC voltage source is producing a controlled and pure sinewave.

The waveforms for full hybrid system operation after reaching steady state are shown in Fig 6-4 for one cycle for better clarity. The peak of the VSI fundamental current component is approx. 8A. The highest peak current is recorded at 12.57A while the negative is at -11.9A which means the current ripple peak at the maximum fundamental amplitude is approx. 4.2A close to the theoretical value. Compared to the peak of the fundamental component, the ripple is at 50% of the peak VSI output current.

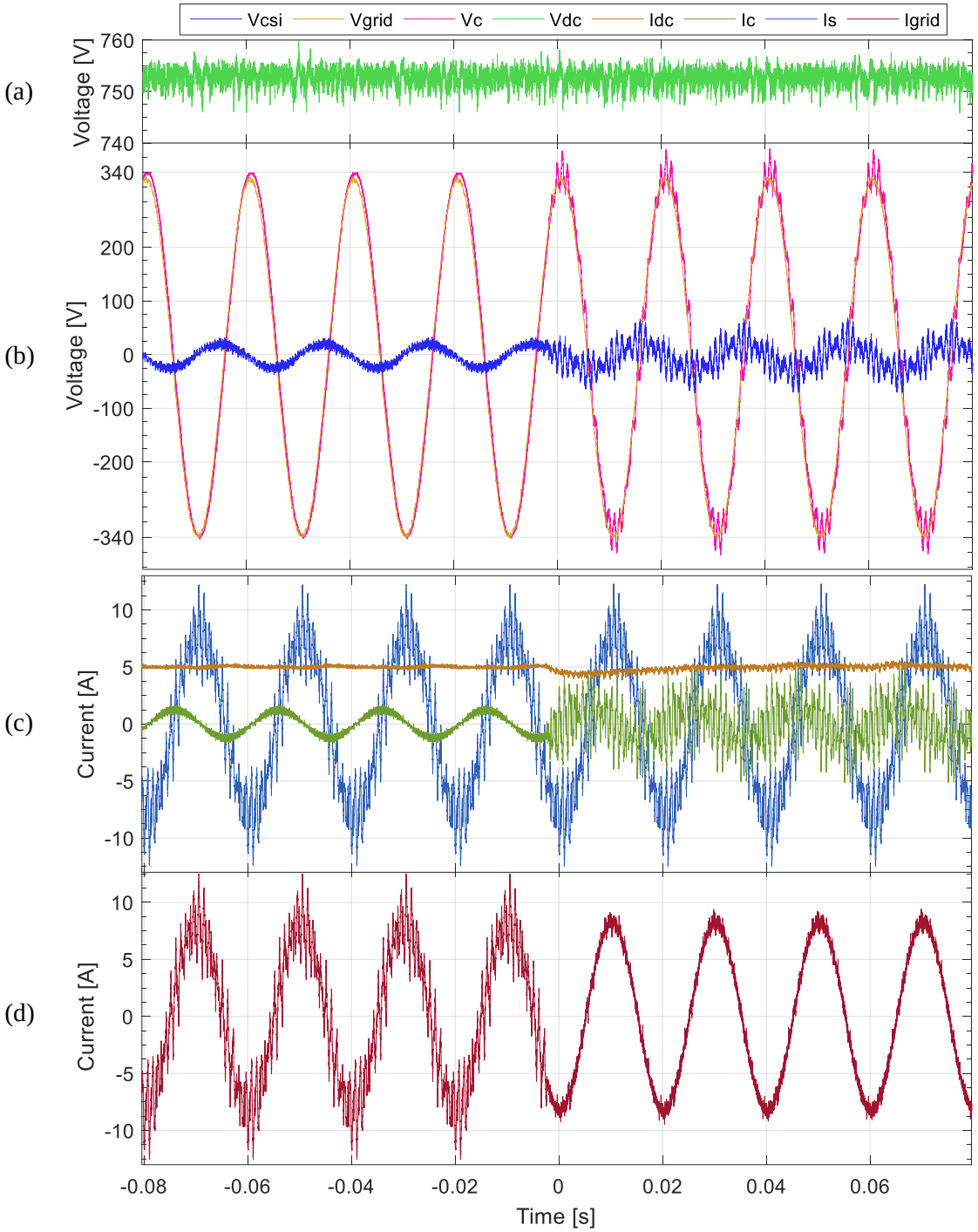


Fig 6-3: Experimental results showing activation of ripple cancellation for VSI and CSI for K=0.1 for Phase A: a) VSI DC-link voltage (V_{dc}) ;b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

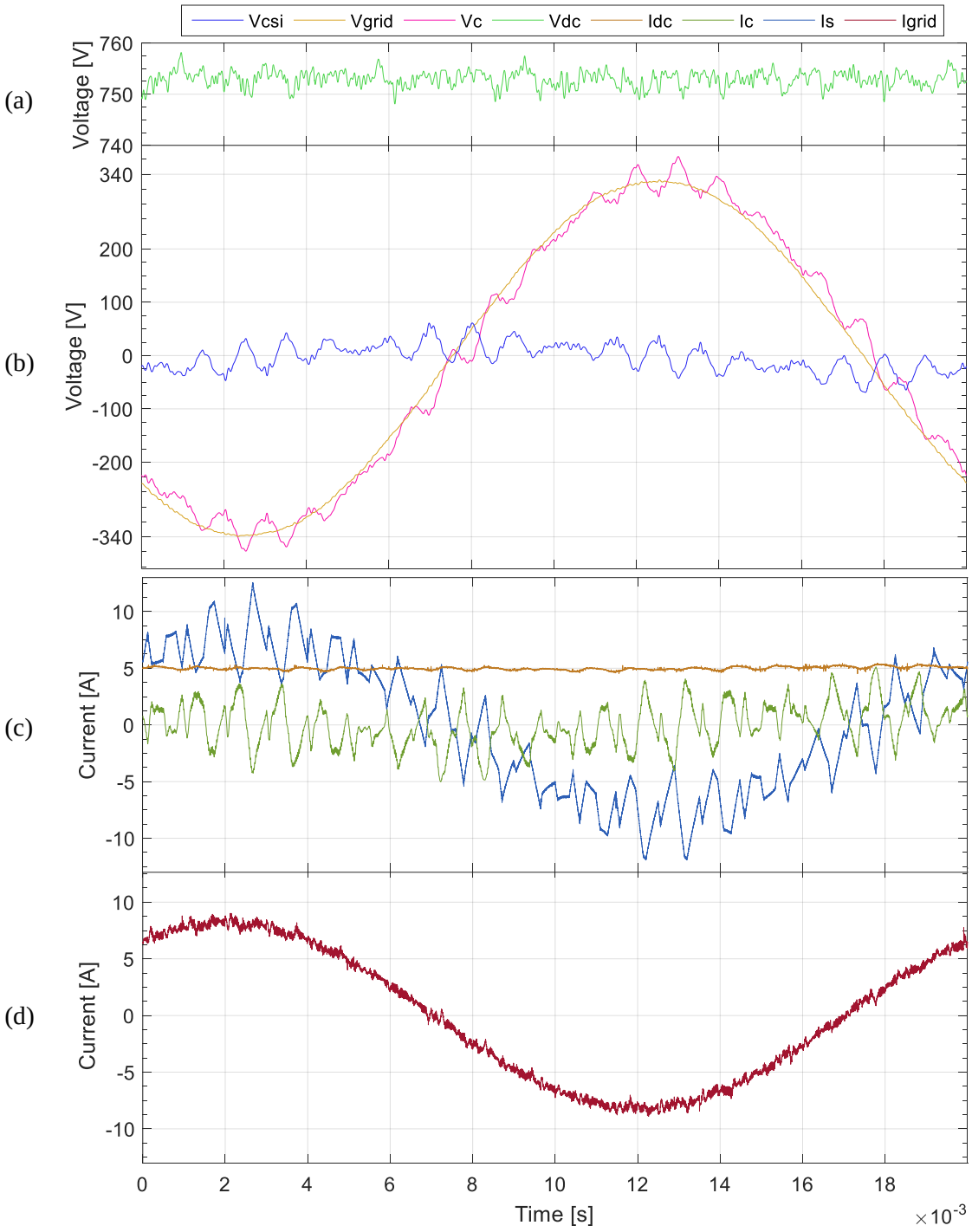


Fig 6-4: Experimental results showing one steady state cycle under full hybrid system operation for VSI and CSI for K=0.1 for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

The use of a significantly higher switching ripple to be cancelled allows for a better demonstration of the harmonic cancellation capability and could be considered representative for the operation of the system at reduced load; as switching ripple tends to remain independent on loading for same DC-link voltage.

During ripple cancellation, the DC-link current is kept at a level as close as possible compared to the peak ripple, with the mean value matching the 5A reference value (Fig 6-4c). A shown in Fig 6-4d, the resulting grid current shape is very close to a pure sinusoidal waveform with the CSI switching ripple at 40 kHz being the main disturbance noticeable throughout the waveform while some notches are observed periodically. These spikes occur when the triangular current ripple peaks and suddenly changes slope/derivative. Due to waveform clean-up, the grid current positive peak is reduced to 9A compared to 12.57A.

The peak of the CSI input voltage waveform in Fig 6-4b has been recorded at 71V, accounting for both the 50Hz and VSI switching ripple) compared to 31V before cancellation (only 50Hz component), amounting to a peak CSI voltage at 20% of the grid voltage, which is identical to the analytical design requirements to enable the use of 1.2kV devices in a 3.3kV MV grid. The RMS CSI voltage is at 11% (26.5V) of the grid voltage (235.7V) showing an even more significant reduction, but this doesn't have a direct impact in the auxiliary inverter design.

To investigate the experimental performance of the hybrid system under more scrutiny, the results under each mode of operation have been analysed in the frequency domain and are presented in the following section.

Fig 6-5 shows the FFT of the CSI, series capacitor and grid voltage before PWM activation, during voltage reduction (fundamental current synthesis only) and under full system operation. Results are presented separately for the fundamental frequency (0-100 Hz) and harmonics up to 3 kHz, where the most significant harmonics occur, on a smaller horizontal scale.

Before PWM activation (Fig 6-5a) the fundamental peak component has been measured at 308V for the CSI voltage, 27.6V for the series capacitor and 334V for the grid voltage, matching the

measurements taken in the time domain. The DC component is at 8.4V for the grid and 1.5V for both the CSI and series capacitor voltage while all other harmonics remain at negligible levels.

When PWM is activated (Fig 6-5b), the fundamental CSI component is reduced at 22.3V compared to 333.4V for the grid voltage and 340V for the series capacitor voltage. The measured DC component is at 9V for the grid, 6V at the CSI and zero for the series capacitor. Some harmonic excitation around the VSI switching frequency is also observed at minor levels reflected across the CSI and series capacitor voltages with the maximum amplitude at 1.4V.

During full system operation (Fig 6-5c) the DC component is at 7V for the grid, 2.6V for the CSI and 9.7V on the series capacitor voltage. Given the varying and small measurement levels of DC components under all modes of operation, it can be assumed any DC presence is likely to be due to a measurement offset rather than a disturbance caused by the CSI control system. The fundamental component is measured at 26.6V for the CSI compared to 333V for both the series capacitor and grid voltage showing minor alteration to the previous measurement. The biggest harmonic voltages appear at 900Hz, measured at 19V for V_c and 18.3V for the CSI and at 1100Hz at 14.25V for V_c and 13.63V for the CSI. All remaining harmonics appear at negligible levels (below 3V). The effect of the voltage drop across the filter inductance L_f, cannot be observed due to acquisition filtering however it will be presented in following experimental results in §7.1.7.

The effectiveness of the ripple cancellation is also assessed in more detail in the frequency domain where the FFT of the VSI, CSI and grid current are shown (Fig 6-6) for in a similar format prior and after harmonic cancellation for frequencies up to 5 kHz on a linear scale and on a semi logarithmic scale focusing on harmonics for frequencies of 700Hz to 50kHz. The highest harmonic at 900Hz is reduced from 1.486A to 80.6mA (5.4% of original harmonic level), the 1.1kHz harmonic is reduced to 8.3% of the original harmonic (122mA compared to 1.476A), 1950Hz harmonic to 8.2% (0.876A to 72mA) and the 2050 Hz harmonic is reduced to 5.1% (0.66A to 34mA). The fundamental component in Fig 6-6c is measured at 7.94A on the VSI current compared to 8.18A on the grid current with the difference accounting for the current going towards the CSI (mostly reactive) at 1.23A. These show a small deviation from the 8A, 1.26A

and 8.2A which has been recorded in Fig 6-6b before ripple cancellation for $I_{s,}$ I_c and I_{grid} respectively.

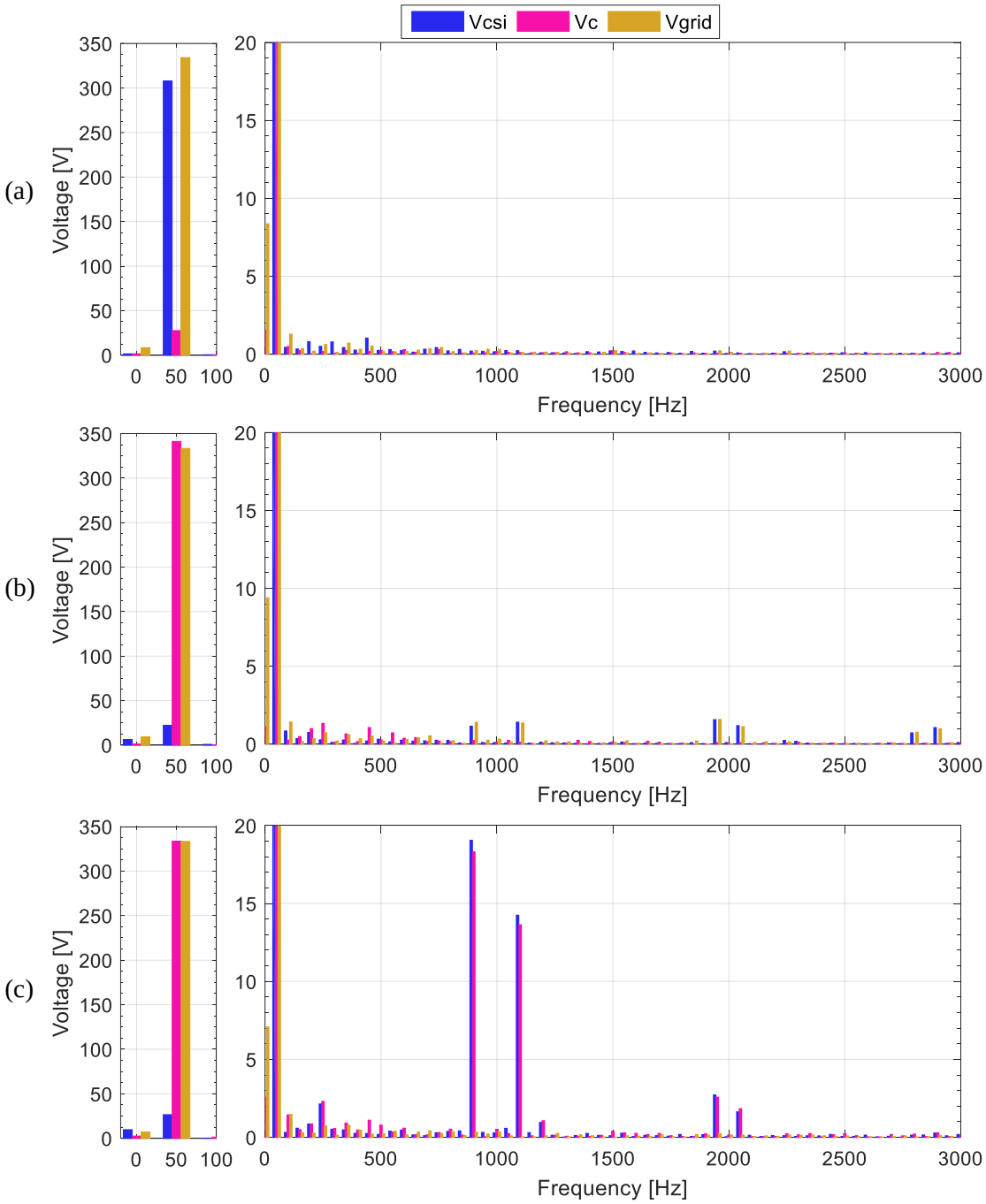


Fig 6-5: FFT of Phase A voltage of the Grid (V_g), Series capacitor (V_c) and CSI phase voltage (V_{csi}) during: a) No PWM; b) PWM enabled showing fundamental voltage reduction; and c) full system operation (harmonic cancellation).

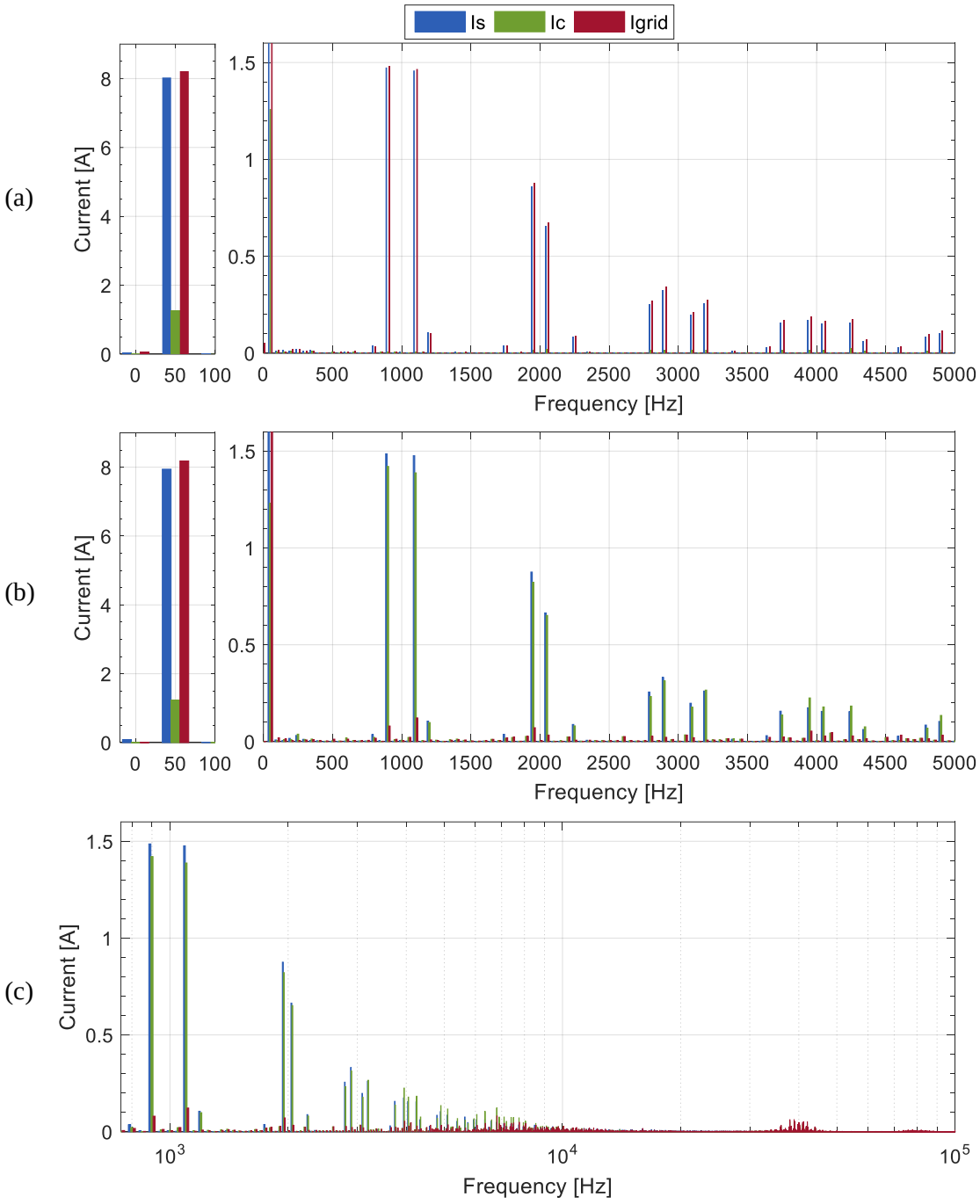


Fig 6-6: FFT of Phase A VSI current (I_s), CSI current (I_c) and grid current (I_{grid}) : a) without ripple cancellation ; b) full system operation up to 5 kHz; and c) expanded to show harmonics from 700Hz to 100kHz on a semi logarithmic scale.

6.1.3. Maximum Voltage Stress and Phase Symmetry

In order to accurately assess the maximum CSI voltage stress and symmetry between all phases, the steady state operation for the circuit prior and after harmonic cancellation is presented for all three phases of the CSI phase to neutral and line to line voltages over two cycles. Furthermore, the DC-side voltage of the CSI clamp circuit is plotted together with the line-line voltages to demonstrate that the clamp voltage is directly correlated to the maximum/peak CSI voltage stress. The waveforms have been captured without any filtering enabled, therefore permitting the accurate assessment of harmonics for all significant frequencies, which are expected up to 100 kHz.

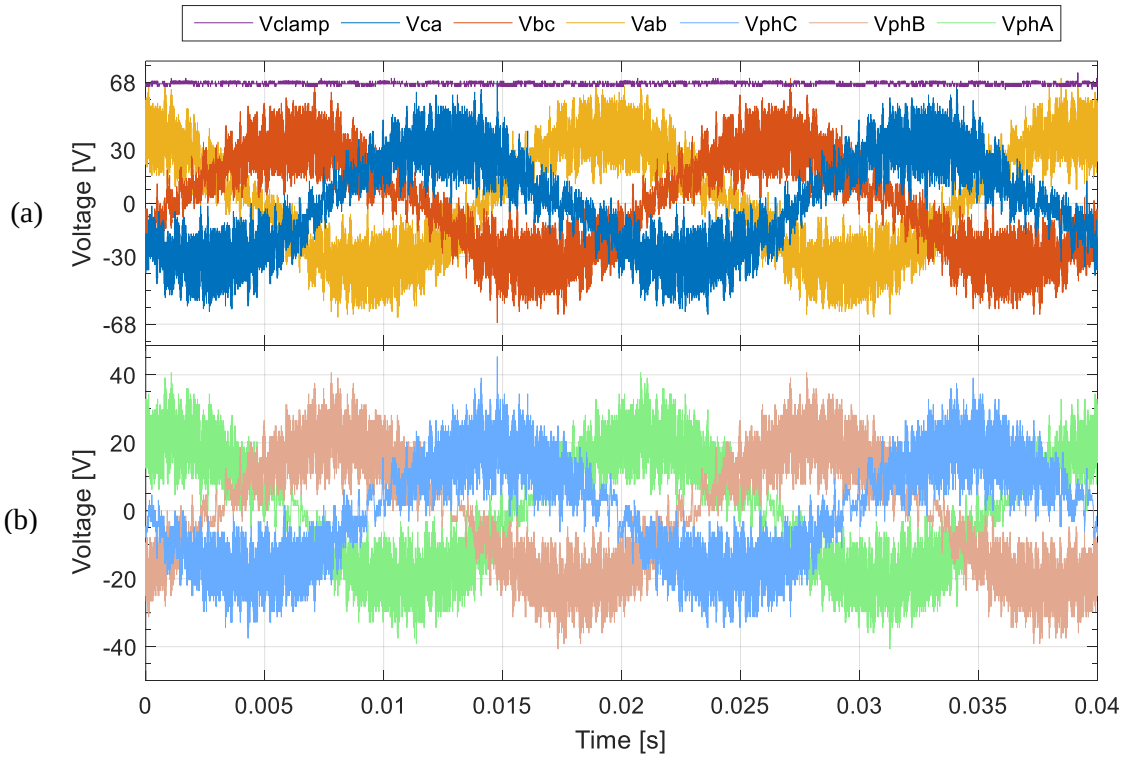


Fig 6-7: The CSI input voltages showing the fundamental voltage reduction in: a) the three phase line-line CSI voltages and the clamp voltage and b) the three phase-neutral CSI voltages.

Fig 6-7 reveals that the phase to neutral voltages reach up to 40V, slightly higher than the previously measured 31V due to the additional ripple created at the CSI switching frequency. The line to line input CSI voltage which defines the maximum CSI voltage stress reaches 68V which is also reflected by a similar clamp voltage reading.

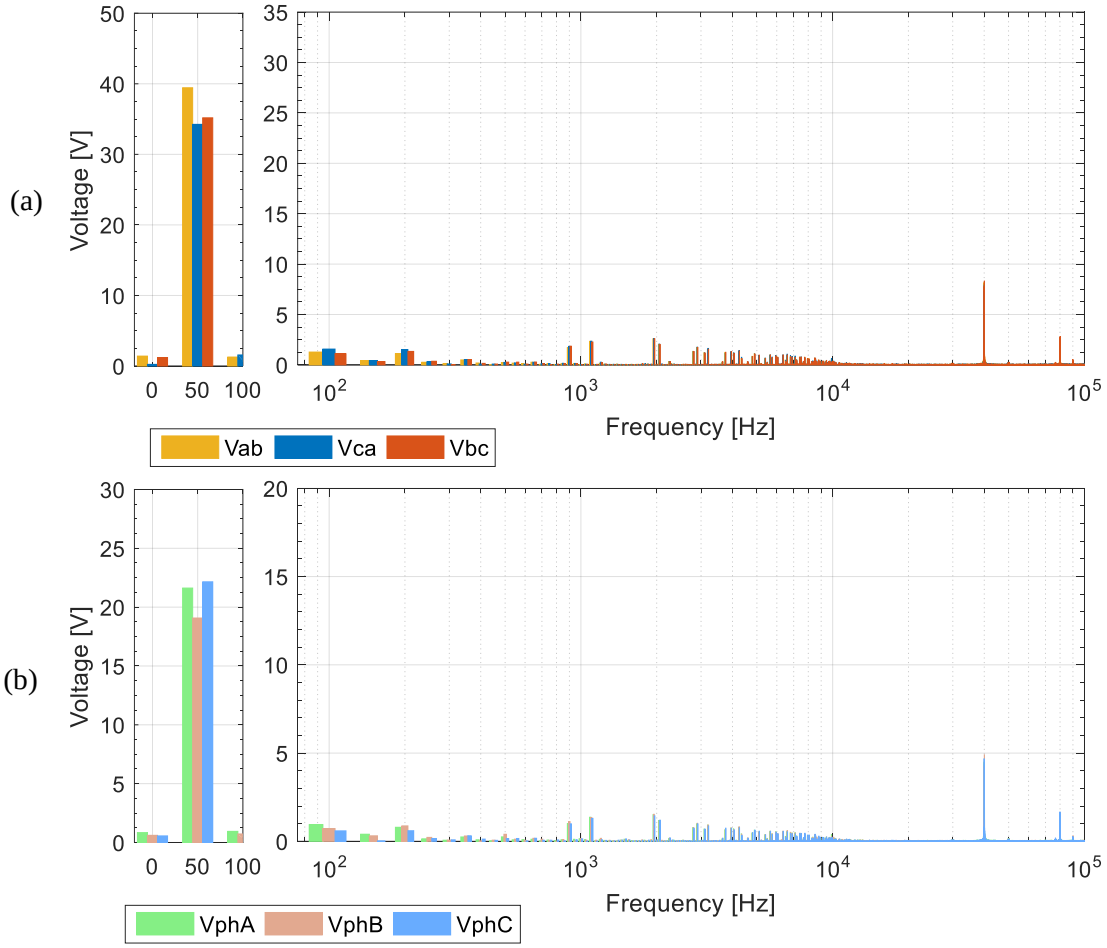


Fig 6-8: FFT of the CSI input voltages under fundamental voltage reduction mode showing the harmonics in: a) the three phase line-line CSI voltages and b) the three phase-neutral CSI voltages.

The corresponding frequency content of the AC voltage waveforms is shown in Fig 6-8. The fundamental component of phase A-B-C phase voltages (Fig 6-8b) has been measured at 21.6V, 19V and 22V respectively showing a deviation of 3V between phases.

It can be observed that a small excitation occurs around the VSI switching harmonics and around the CSI AC side filter resonant frequency although the peak values for the latter remain under 0.6V. The most significant harmonic cluster can be observed at 40 kHz(±50Hz), caused by the CSI switching frequency with amplitudes reaching 8.2V while the cluster at 80 kHz reaches 3V having a lesser effect. The CSI line-line waveforms (Fig 6-8a) reveal a similar effect for higher order harmonics however it can be observed that the fundamental component asymmetry appears more pronounced with V_{ab} measured at 39.5V while V_{ca} and V_{bc} at 34V and 35V.

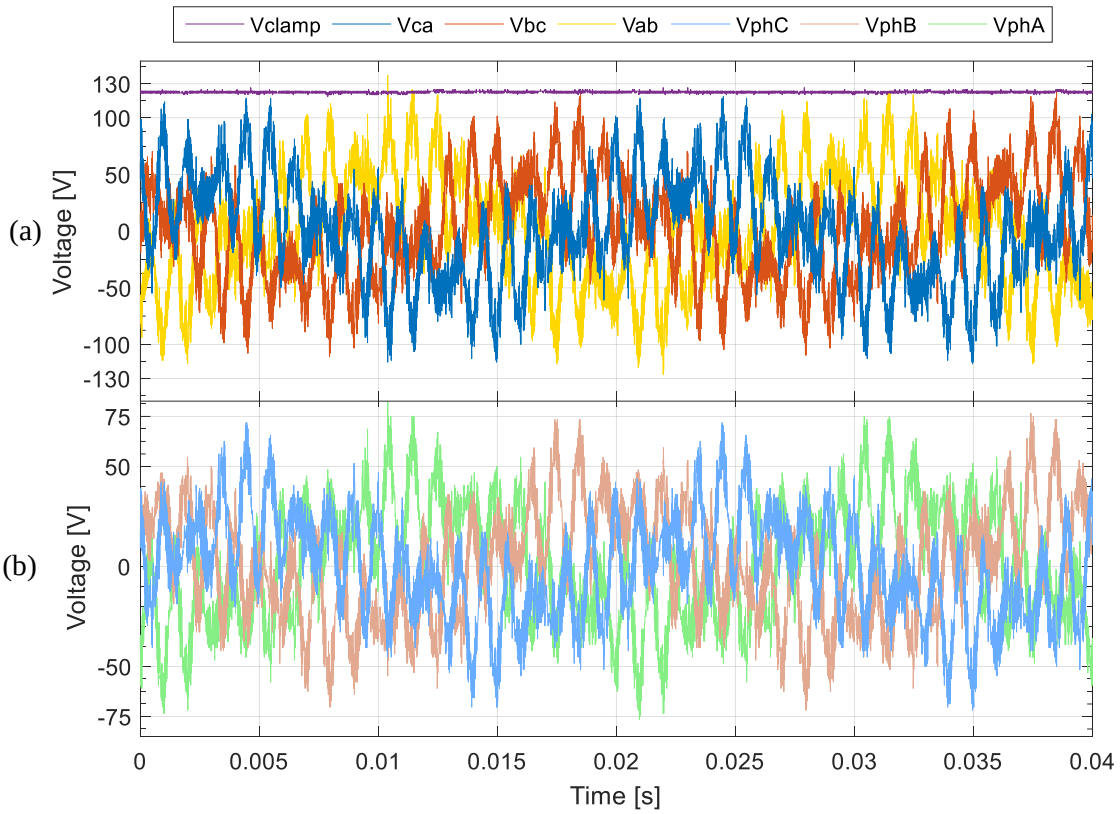


Fig 6-9: The CSI input voltages under full system steady state operation showing: a) the three phase line-line CSI voltages and the clamp voltage and b) the three phase-neutral CSI voltages.

All three phase and line-line CSI voltages, along with the clamp voltage, under full operation are shown in Fig 6-9. Phase to neutral voltages are shown in Fig 6-9b with the maximum voltage peak reaching 75V for all phases accounting for the cumulated effect of the fundamental, VSI switching ripple and CSI switching ripple along with any DC component. The voltage reduction is therefore at 22% compared to the maximum phase grid voltage.

The line to line voltages are shown in Fig 6-9a to determine the maximum CSI voltage stress. It can be seen that the maximum voltage reached is 122V, matching the DC voltage reading on the clamp circuit. The clamp circuit reading is directly reflecting the voltage stress on the CSI switches and will be used as a reference for assessing the peak voltage stress in the following performance evaluation. Although the symmetry between the three phase waveforms is evident in the time domain, the frequency content is examined to allow for direct comparison with results under different operating conditions.

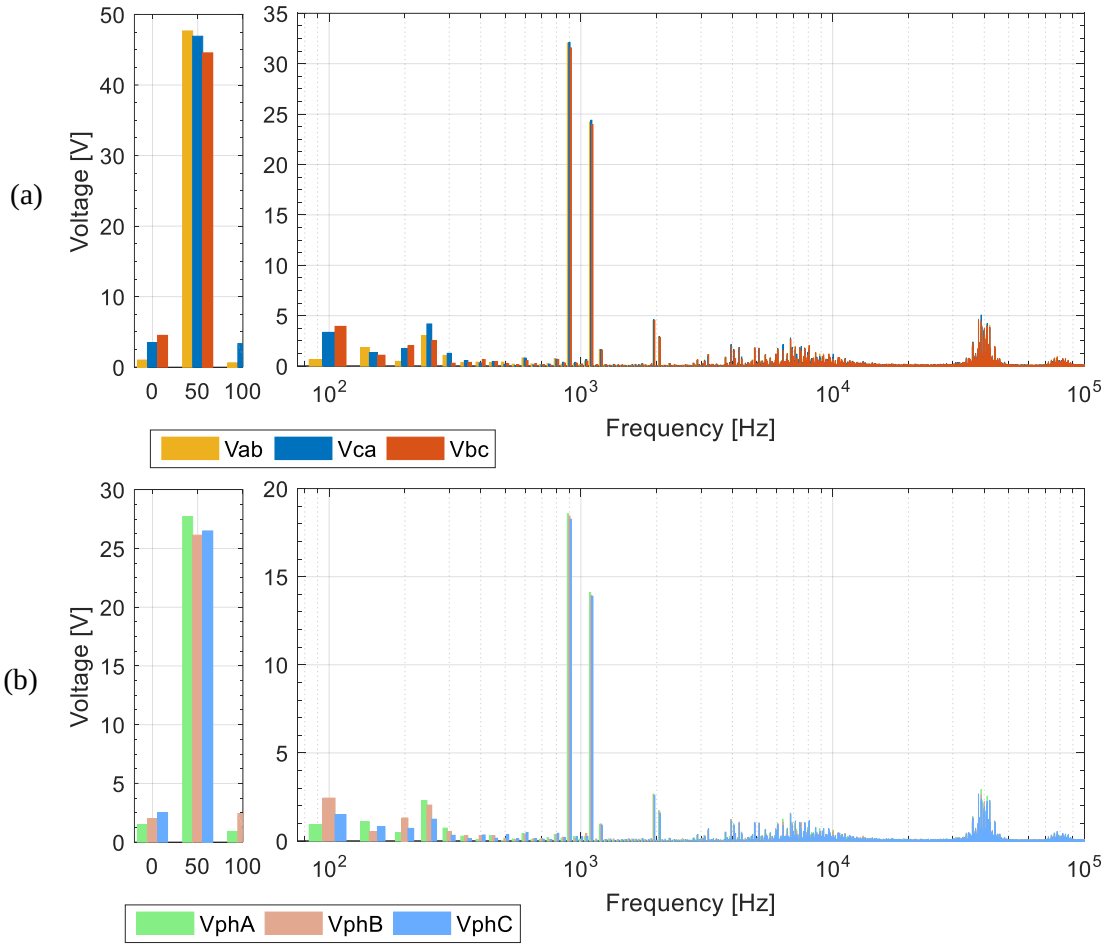


Fig 6-10: FFT of the CSI input voltages under full system steady state operation showing the harmonics in: a) the three CSI line-line voltages and b) the three phase-neutral CSI voltages.

The fundamental component for phase A-B-C voltages has been measured at 27.7V, 26.1V and 26.5V showing very small deviation between the three values. Similarly the highest harmonics have been measured at 18.6V, 18.4V and 18.3V at 900Hz and 14.1V, 13.9V and 13.9V at 1.1 kHz.

On the CSI line-line voltage FFT in Fig 6-10a, the fundamental component for V_{ab}, V_{ca} and V_{bc} has been measured at 47.7V, 46.9V and 44.6V. Harmonics at 900Hz are measured at 32V and harmonics at 1.1 kHz at 24V showing symmetry for higher order harmonics occurring around the VSI and CSI switching frequencies. The DC component has been measured at 1.5V, 3V and 4.5V respectively. Compared to operation prior to harmonic cancellation(Fig 6-8) it can be seen that the harmonic cluster around the CSI AC filter resonant frequency has increased due to further

excitation by the CSI injected harmonics while a wider harmonic spread is observed at the 40 kHz switching frequency.

Finally a slight increase of 2nd and 5th order harmonics is visible for phases B and C under full system operation. Although the harmonic voltage amplitudes remain relatively small due to negligible amplitudes of the harmonic current injected, it is an indication that a disturbance is propagated through the current ripple reference of the CSI control system which has poor low order harmonic rejection and this will be later demonstrated in CHAPTER 7. The 5th order harmonic on the line-line voltages has been measured at 3V, 4V and 2.5V for V_{ab}, V_{ca} and V_{bc}.

6.1.4. Performance Evaluation for Different CSI Switching Frequencies

The effectiveness of the current harmonic cancellation over a range of CSI switching frequencies (20/ 25/ 30/ 33/40kHz) is presented in this section. The processed steady state results are shown together to allow for demonstration of the detrimental effects due to the switching frequency and sampling frequency as well as the identification of error sources.

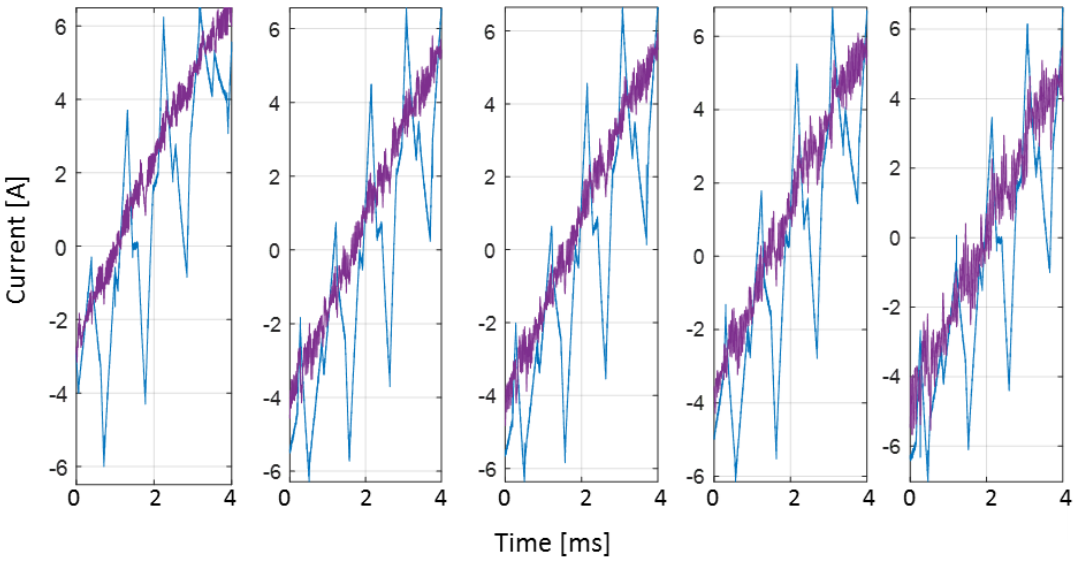


Fig 6-11: Zoom in on the main VSI current zero crossing showing superimposed the converter-side and the filtered grid current for different CSI switching frequencies (40/33/30/25/20 kHz left to right)

Fig 6-11 presents a zoom-in of the superimposed grid current I_{grid} and VSI current I_s under full hybrid operation focusing on a 4ms window around the main VSI current zero crossing. It can be observed that the main visible disturbance at 40 kHz occurs at the peaks of the triangular current ripple shape revealing that although the tracking of the current slope is accurate, a slight mismatch in the peak due to a phase or amplitude error creates a visible notch when the current slope reverses with a peak-peak amplitude around 1A. At 33 kHz the current tracking capability does not seem to be compromised, with the notches observed at a slightly lower levels for a similar switching ripple amplitude. The current tracking capability at 30 kHz is similar with 40 kHz although with a slightly increased switching ripple amplitude. For lower switching frequencies however the attenuation provided by the CSI AC filter is low therefore for 25 and 20 kHz, the ripple caused by the CSI switching frequency is the main observed disturbance but still having a noticeable notch occurring when the current ripple peaks albeit at an amplitude similar to the switching ripple at approx. 1A. The effectiveness of the ripple cancellation is therefore affected due to the low filter attenuation.

The harmonic contents of the VSI, CSI and grid currents have been plotted in separate 3D plots for all CSI switching frequencies. Rather than commenting on individual harmonic amplitudes, the purpose is to show the created harmonic profile and identify the relative amplitude of relevant harmonic clusters. Each FFT has been taken over 50 cycles (1 second) to minimise spectral leakage in the frequency range of interest.

Fig 6-12 is showing the harmonic content (excluding fundamental) of the VSI current I_s for each CSI switching frequency. For the VSI, this translates to a different sampling frequency that is then downscaled to the 1 kHz switching frequency as explained in §5.2.2.1. It can be observed that the two main harmonics at (900Hz and 1.1 kHz) remain at similar levels, slightly below 1.5A while the harmonic amplitudes decrease towards zero at around 10 kHz. Ensuring that the VSI harmonic profile remains unaltered when using different sampling frequencies is important for the comparative validity of the assessment of harmonic cancellation. The identical harmonic profile is also verified through the power analyser THD readings presented in §6.1.4.1.

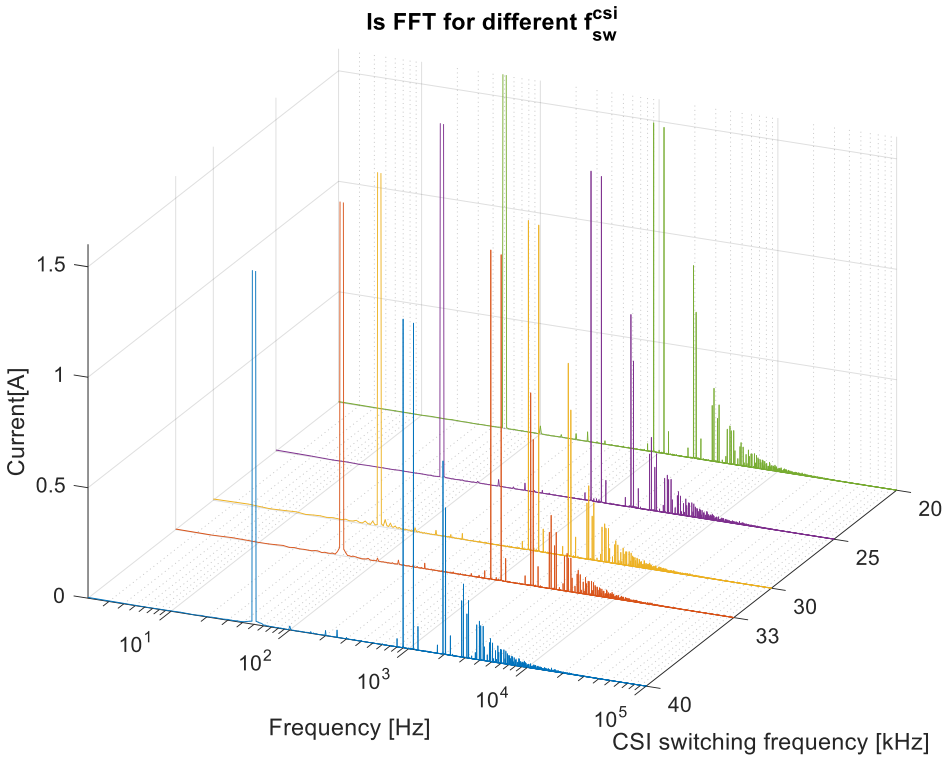


Fig 6-12: Cumulated FFT for VSI current harmonics excluding the fundamental component for different base sampling frequencies defined by the CSI switching frequency.

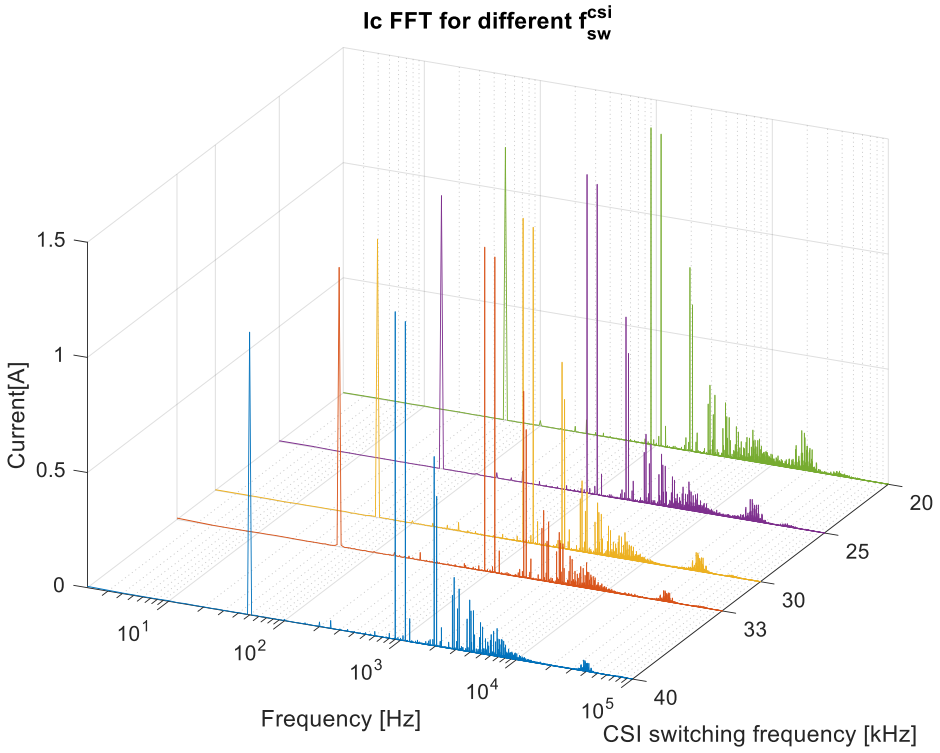


Fig 6-13: Cumulated FFT for CSI current harmonics for different CSI switching frequencies.

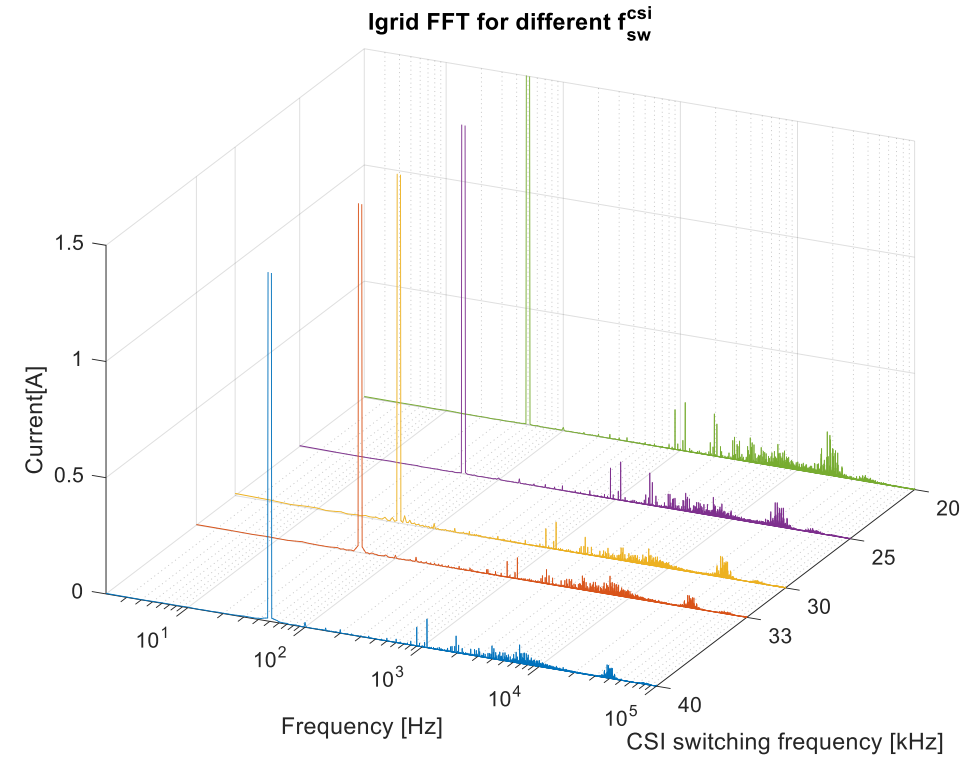


Fig 6-14: Cumulated FFT for grid current harmonics for different CSI switching frequencies (fundamental component clamped).

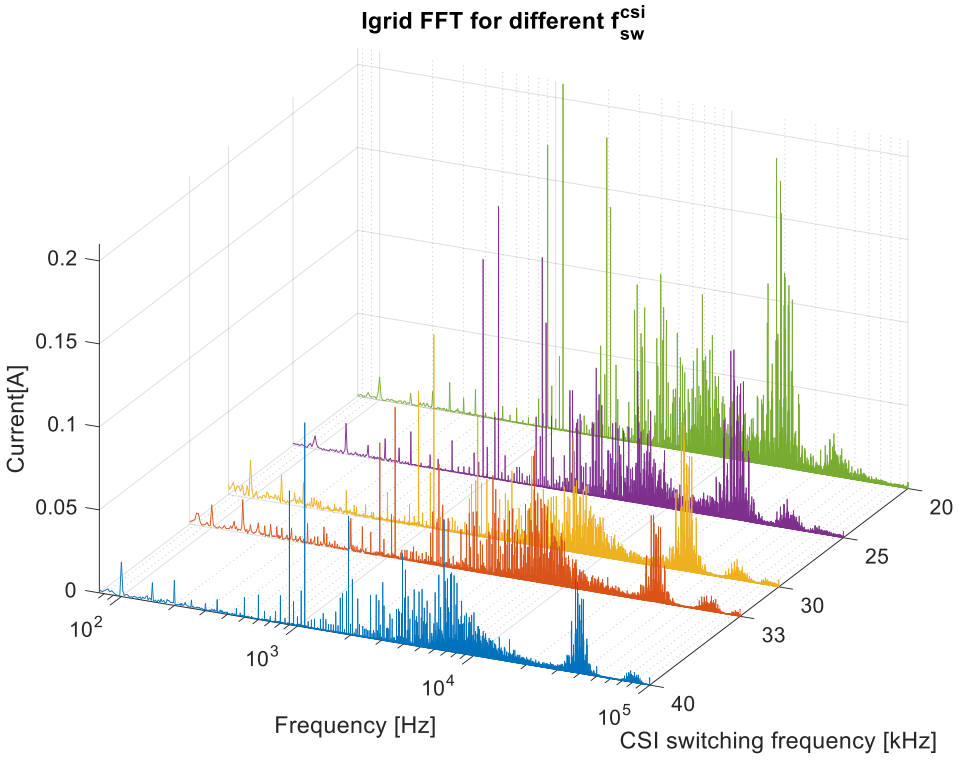


Fig 6-15: Zoom-in on cumulated FFT for grid current harmonics for different CSI switching frequencies focusing harmonics (excluding fundamental).

Fig 6-13 shows the current spectrum created by the CSI under full operation revealing that the fundamental and main switching harmonics remain similar in amplitude. A slight harmonic excitation can be observed in comparison to Fig 6-12 around 9 kHz caused by the small resonant excitation given by the CSI AC filter response. Finally a harmonic cluster can be observed around each respective CSI switching frequency.

This can be seen in more detail in Fig 6-14 at the remaining grid current harmonics and the zoom-in in Fig 6-15 focusing only on the remaining harmonics. As observed in the time domain waveforms, operation at 20 kHz will result in a significant reduction of the main VSI switching harmonics. However due the to the low CSI filter attenuation, the CSI switching harmonics reach a similar amplitude to the remaining grid harmonic sidebands around 1 and 2 kHz and wide harmonic spreading is observed due to the excitation at the LC filter resonant frequency.

As the CSI switching frequency is increased, it can be observed that the cluster around the CSI switching frequency decreases in amplitude and separates from the excitation around the filter resonant frequency which remains at similar levels for the highest switching frequencies (25-40 kHz). It can be also observed that the main VSI harmonics are reduced with the further increase of switching frequency.

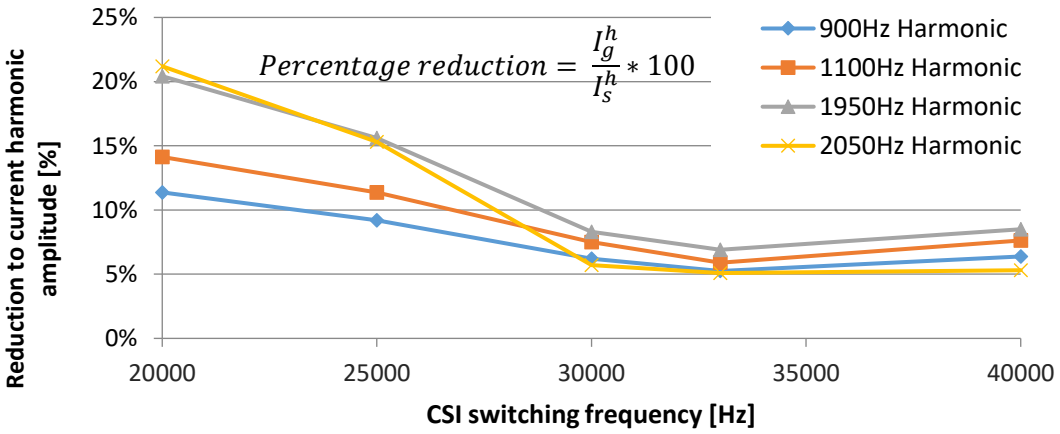


Fig 6-16: Hybrid grid current harmonics as a percentage of the main VSI relevant current harmonics over a range of CSI switching frequencies

The amplitude reduction for each of the four main harmonics comparing amplitude between the converter and grid side as a percentage is presented in Fig 6-16. The least reduction is observed at 20 kHz with the most significant sidebands (900Hz and 1.1 kHz) reduced to 11% and 14% and the second set of sidebands (1950Hz and 2050Hz) reduced to 21% revealing a limited cancellation effectiveness for harmonics below 1/10 of the CSI switching frequency. This is verified by the significant improvement in harmonic reduction for the second set of sidebands as the CSI switching frequency is increased from 20 kHz to 30 kHz. This improvement levels between 30 kHz and 40 kHz where the harmonic reduction remains unchanged. For switching frequencies of 30 kHz or higher, all harmonics are reduced to less than 10% with values ranging from 5% to 8%. A slight increase of harmonics at 40 kHz compared to 33 kHz could be explained by the increasing effect of the overlap time for higher switching frequencies or by an aliasing effect due to the sampling frequency.

A further investigation of the source of error in the harmonic reduction, considering the four main harmonics is shown in Fig 6-17. The total Error percentage, symbolised in different colours for each switching frequency, is the percentage of the residual grid current amplitude compared to the corresponding VSI current harmonic.

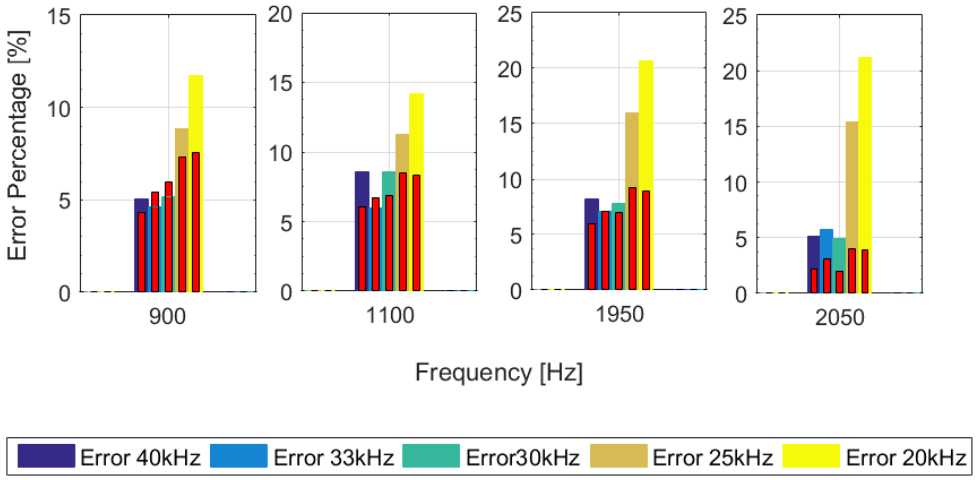


Fig 6-17: Bar charts showing resulting total error in reduction for each of the main current harmonics for different CSI switching frequencies and superimposed (in red) the error due to amplitude mismatch produced by the CSI.

$$Error\_fsw = 100 * \frac{I_{grid}}{I_s} \qquad Amplitude\ Error\ (red) = 100 * \frac{|I_s - I_c|}{I_s}$$

The calculated error due to amplitude mismatch, calculated by comparing the absolute difference between the amplitude of the CSI and Main VSI current harmonics to the VSI harmonic amplitude, is shown superimposed in red for each bar. This enables the separation of the error due to amplitude synthesised by the CSI and the total error, thus implying that the difference is due to a phase shift between main VSI and CSI harmonics. For all harmonics it can be seen that the amplitude mismatch is at similar levels for the different switching frequencies of 4-8%, with a variation of up to 4%. For 20 kHz and 25 kHz switching frequencies the error due to the phase shift, given by the difference between the actual error and the red bar, increases with the harmonic order confirming that the reduction in sampling frequency results in a significant phase shift of the injected harmonic that limits the bandwidth of the active CSI filter.

For switching frequencies above 30 kHz it can be seen that the effectiveness of harmonic cancellation is mainly limited by an amplitude mismatch which is due to limitations in harmonic extraction, including also the errors in the sensing equipment.

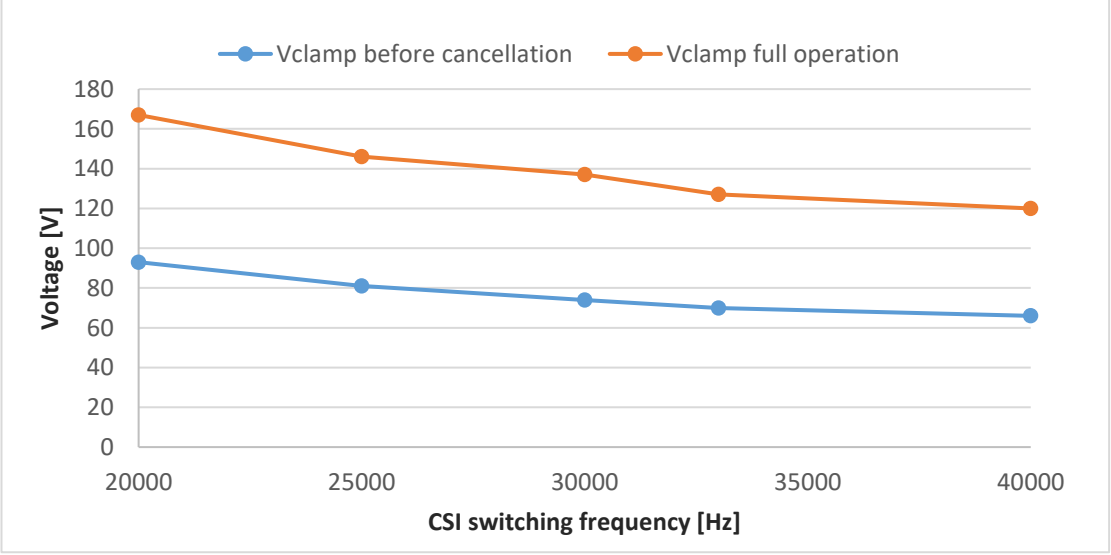


Fig 6-18: Voltage reading of the clamp circuit for different CSI switching frequencies showing the two operating modes of the CSI.

Fig 6-18 shows the DC voltage reading taken on the dc-link voltage of the clamp circuit that has been shown to signify the maximum CSI voltage stress for different switching frequencies, plotted for fundamental synthesis (no ripple cancellation) and full system operation. The results quantify the level that the increasing switching frequency is contributing towards further lowering the CSI voltage stress. This can be observed by the downward trend from 93V at 20 kHz to 66V at 40 kHz accounting for the reduction of the voltage ripple at the CSI switching frequency and CSI filter resonant frequency. The same trend can be observed for full system operation, implying that the margin between the two curves is the added voltage stress created by the current switching ripple at the VSI switching frequency. Compared to the maximum nominal line-line grid voltage of 587V (415Vrms), the voltage reduction seen on the CSI inputs is at 28.5% at 20 kHz, 24.8% at 25 kHz, 23.3% at 30 kHz, 21.6% at 33 kHz and 20.4% at 40 kHz. It should be noted that the figures show a slight discrepancy of around 1% compared to the previously recorded scope results.

In terms of added installed power, based on the maximum VSI voltage stress given by the DC-link voltage at 750V, the maximum current stress as the peak of the VSI current is 12.5A and the CSI maximum current stress is measured at 5.4A under full operation, therefore the added installed power in the CSI switches ranges from 9.6% to as low as 7% depending on the CSI switching frequency.

6.1.4.1. Power Analyser Results

The experimental procedure, enabling PWM and ripple cancellation, has been repeated for different CSI switching frequencies with power quality measurements logged at one second intervals using a power analyser (N4L PPA 5530). The power analyser enables the measurement of the efficiency by recording the AC power in (two wattmeter method) and DC power out as well as the calculated grid current total harmonic distortion (THD) up to the 100th harmonic. The high THD levels typical to a diode rectifier type of non-lineal load behaviour can be observed in

the following recordings of the current THD up to approximately t=30s where PWM is enabled for both converters, and full system operation is enabled at t=90s.

The grid current THD is reduced from initially 33% during diode rectifier operation to approximately 23% when PWM is enabled; with some reasonable fluctuation observed between waveforms. The effect of ripple cancellation is apparent by the immediate further reduction of the THD during full hybrid system operation for all CSI switching frequencies. At 20 kHz CSI switching frequency, the current THD value is approx. 3.5% with a slight improvement to less than 3% for 25 kHz and reducing to below 2% THD for all other CSI switching frequencies above 30kHz. It can be noticed that the average THD per switching frequency matches the switching ripple reduction as measured in Fig 6-16.

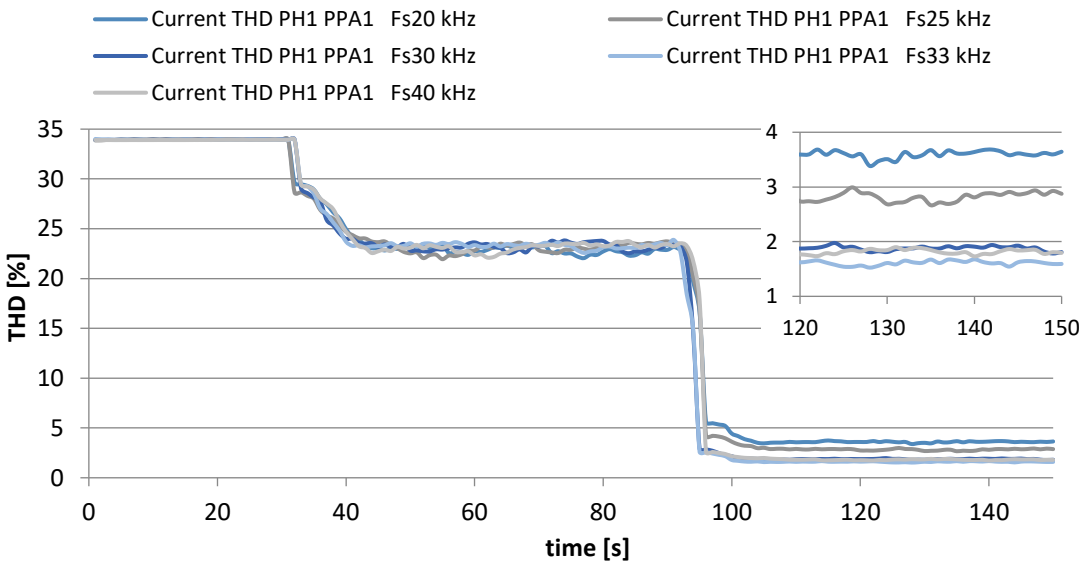


Fig 6-19: Power analyser grid current THD data for operation before PWM (0 to 30s), PWM prior to ripple cancellation (30 to 90s) and during switching ripple cancellation with zoom in on low THD values during ripple cancellation period for different CSI switching frequencies.

The recorded efficiency for the same test is shown in Fig 6-20. As expected, diode rectifier operation before PWM is enabled has the highest efficiency at 98.5%. When the VSI and CSI operate in voltage reduction mode, the efficiency is approx. 5% whilst a further minor drop of around 0.2% occurs for full hybrid operation. The recorded efficiency reveals negligible effects

of the CSI switching frequency under all modes of operation. A small deviation at 20 kHz could be caused by the additional voltage CSI stress due to the reduced AC side filter attenuation but is considered negligible (less than 5W). During full hybrid system operation the efficiency, including the passive losses of the system, remains approximately 94.8% compared to 96% for VSI standalone operation (assessed separately and not shown above) where the CSI and associated passives have been physically disconnected from the VSI.

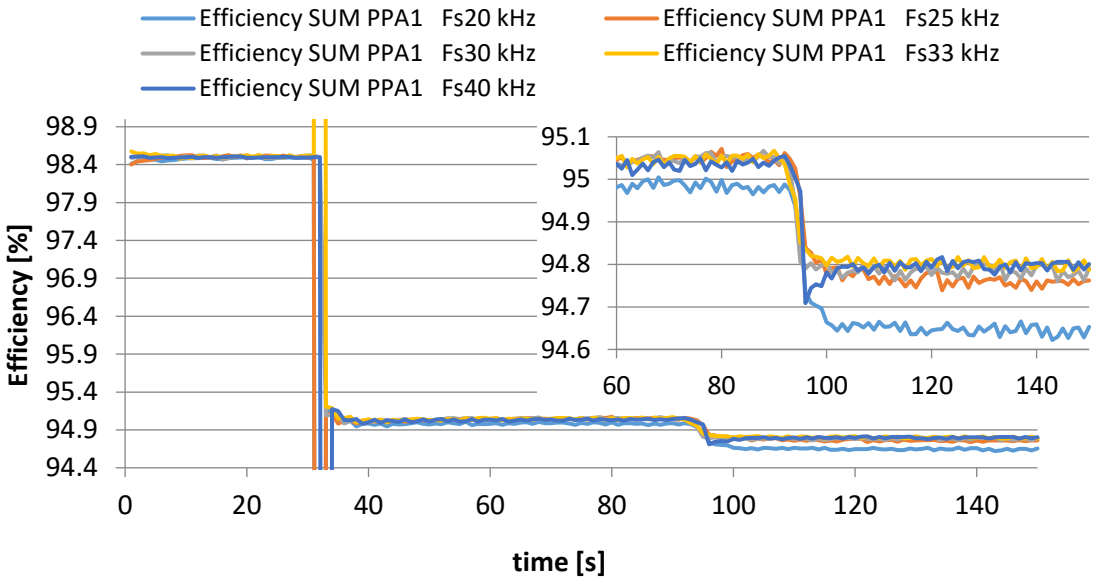


Fig 6-20: Power analyser efficiency data for operation before PWM (0 to 30s), PWM prior to ripple cancellation (30 to 90s) and during cancellation for different CSI switching frequencies. Zoom in (top right) showing effect of enabling ripple cancellation.

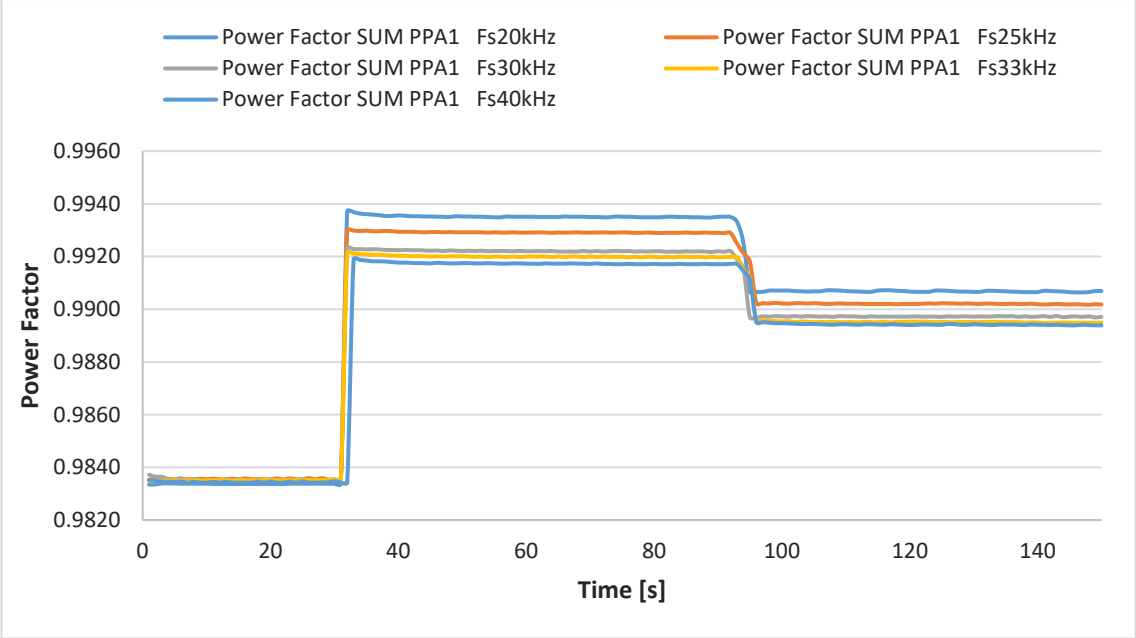


Fig 6-21: Power analyser Displacement Power Factor (DPF) data for operation before PWM (0 to 30s), PWM prior to ripple cancellation (30 to 90s) and during cancellation for different CSI switching frequencies.

In comparison, the displacement power factor (DPF) has been reduced from 1.0 for standalone VSI operation (not shown) to above 0.9916 before ripple cancellation is activated. During full hybrid system operation the DPF remained above 0.989 for all switching frequencies considered showing an insignificant impact of the series capacitor on the overall reactive power.

6.2. Conclusion

It can be concluded that the overall experimental system performance in ideal grid conditions is very similar to the simulated performance when connected to a stiff grid. It is also proven that the analytical design procedure to define the choice of series capacitor and the scaling of CSI and output filter has indeed yielded the expected performance target of reducing the fundamental voltage drop on the CSI. Under steady state operation the peak CSI voltage stress is at 22% of the grid voltage peak with the overall system benefitting from very low grid current distortion verified by the harmonic performance evaluation over a relevant range of CSI switching frequencies.

The use of the CSI has been shown to be effective at synthesising the reference currents necessary for current ripple cancellation. The current harmonic reduction is obvious in the time and frequency domain waveforms with the main VSI switching harmonics reduced to 5-8% of the original amplitude, resulting in a significant increase of the grid current quality. The THD100 measurement also showed the decrease in the current THD from 23% (VSI) to below 2% (grid).

The CSI is shown to have a small effect on the overall losses which can is partly compensated by the reduction of losses in the supply as the current ripples are smaller. The impact on the output power factor is also shown to be small. The added installed power in the CSI switches compared to the main VSI which considers the peak voltage and current stresses and the number of switches is calculated to approx. 7%, showing an increase from the 4% theoretical value stated in CHAPTER 3, but accounting for the additional CSI loading caused by additional commutation voltage spikes and extra current ripple processed.

CHAPTER 7. Experimental Validation under Real Grid Conditions

This chapter continues the experimental evaluation of the hybrid assembly by presenting the experimental performance evaluation while operating with real grid conditions. The experimental procedure used in Chapter 6 is replicated here with the only change of using a stiff (low impedance) interconnection with the real power grid. Although the initial scope of this experimental work has been to investigate the effects of grid inductance, the non-ideal grid conditions (voltage harmonics and unbalance), which have not been theoretically addressed up to this point, presented a bigger challenge which partially compromised the performance of the hybrid system and required additional investigations and remedial work and these will be presented first.

The grid represents a realistic and non-ideal operating scenario unlike §6.1, where the supply emulated by the use of the Chroma electronic source was considered ideal, the voltages of the real grid exhibit both unbalanced and distorted waveforms with noticeable level of low order harmonic components. The first section of this chapter analyses the quality of the grid voltage waveforms before the circuit setup is presented. The operation with the same control system used in the previous chapter is presented with only minor adjustments done to the CSI DC-link current reference and voltage reduction coefficient K. The results show that although the current ripple cancellation remains largely unaffected, with similar output grid current quality, the voltage reduction capability of the CSI is compromised whilst also showing significant unbalance.

To verify that this result is an effect of the real grid (unbalance), simulations of the hybrid assembly operation with unbalanced grid to match the experimental conditions are carried out, therefore deducing the unbalance mechanism and its impact on the performance which is thoroughly discussed. Different solutions to the unbalance are explored before an improved control scheme is proposed for the CSI with the performance validated experimentally to demonstrate that CSI voltage balancing is restored and CSI voltage reduction is again operational and matching expectations. It is also shown that it is possible for the CSI to partially compensate for low order current harmonics in the VSI current however at the cost of additional voltage stress but this should be avoided as it doesn't serve the main purpose of the application.

The final section of this chapter evaluates the operation and performance of the Hybrid System considering the resonant effects created by a larger grid side inductance. The evaluation is performed under the same real grid conditions therefore maintaining the added effects and challenges which were previously mentioned. For this experiment an LC filter has been added at the PCC which results in shift of the CSI output filter resonant frequency from 9.5 kHz to 6.4 kHz. It is subsequently shown that although the resonant effects are noticeable, the added impact on the CSI voltage stress under full hybrid operation is relatively small. The current harmonic quality is also affected as the remaining ripple on the grid current will be at the resonant frequency rather than the CSI switching frequency.

7.1. Grid Voltage Quality Assessment

The grid voltage phase waveforms are shown in Fig 7-1 where the voltage distortion results in visible flat tops and small oscillations around zero crossings. An unbalance is also noticeable affecting the voltage peaks which reach 328V, 334V and 336V for phases A, B and C. The zero sequence grid voltage, defined as $(V_a+V_b+V_c)/3$ is shown in Fig 7-2 for the equivalent period with the maximum amplitude reaching 9V occurring at the positive zero voltage crossing of phase B.

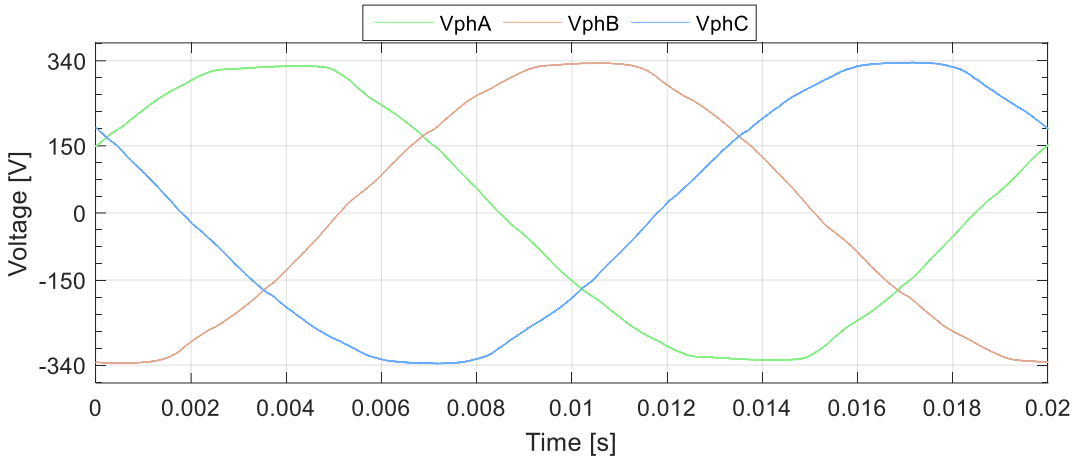


Fig 7-1: The phase to neutral grid voltage waveforms showing harmonic distortion.

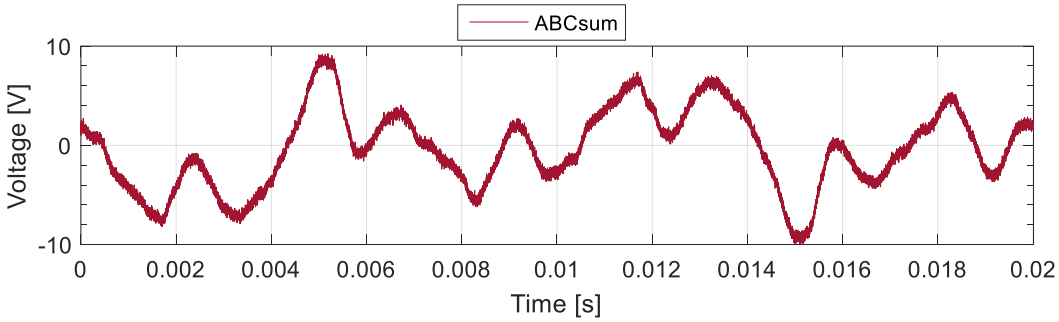


Fig 7-2: Zero sequence component in grid voltage

The harmonic analysis of the real grid voltages presented in Fig 7-3, shows that the fundamental component amplitude is at 336V for phase A and 340V for phases B and C for one cycle, and 322V and 319V when a one second period is analysed. Low order harmonics are also observed with the 3rd harmonic measured at 5V, 3V and 3.6V. 5th harmonic is predominantly noticed only on phase A at 2.96V. The 7th harmonic amplitudes for phases A-B-C are 4V, 2V, and 3V whilst the 9th harmonic amplitudes are 3.5V for phase A and 2.5V for phases B and C.

Although the maximum amplitude of these harmonics remains within grid regulations, the harmonic order and varying amplitude levels for each phase that have been noticed to occur in real grid conditions lead to more challenging conditions and eventually constitute an additional source of disturbance for the hybrid system control which until now have not been tested .

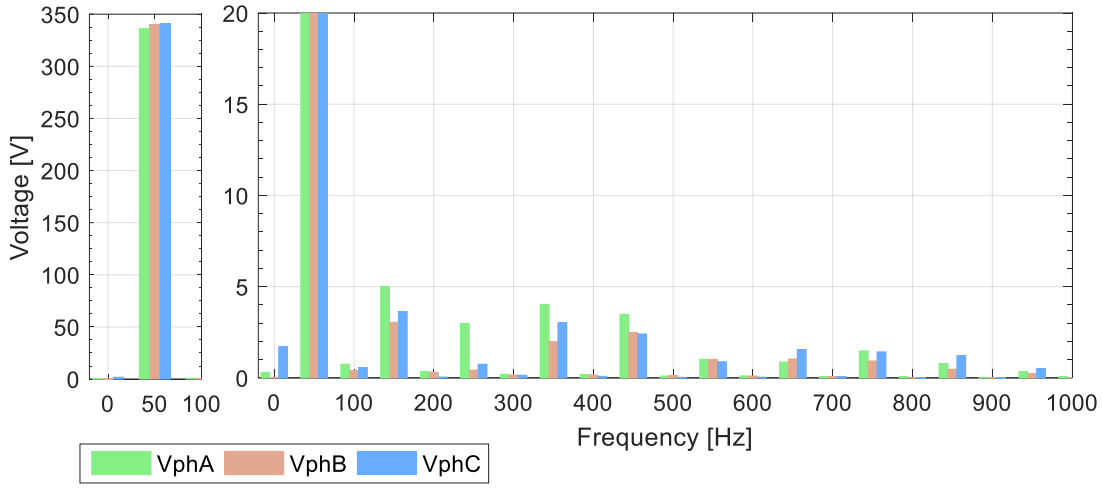


Fig 7-3: FFT showing the harmonic content of the three phase-neutral grid voltages

7.1.1. Experimental Setup

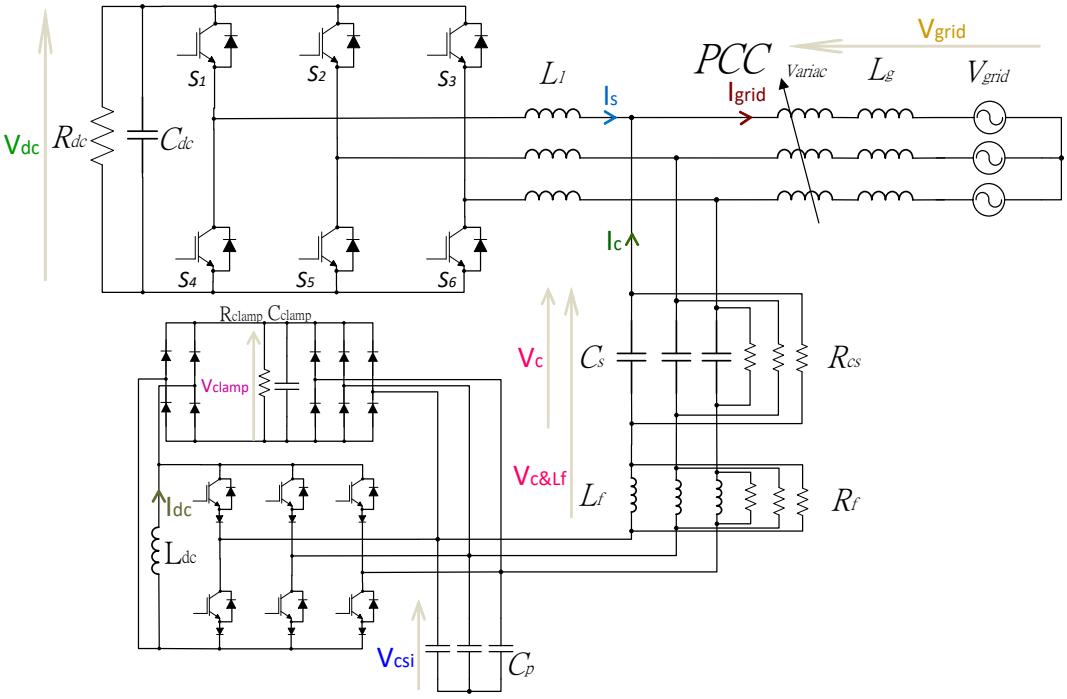


Fig 7-4: Circuit topology of the experimental setup connected to the real power grid.

The connection to the grid has been done via an autotransformer (Variac) as shown in Fig 7-4 with the voltage set at 100%. The grid impedance is shown as L_g, separate to the variac

impedance. On the left side of the PCC the overall hardware component values and circuit interconnections have been kept identical to CHAPTER 6 as is also the case with the control structure where the PI controller tuning has been left unchanged to allow for comparison between results.

In the following section it will be demonstrated that, for the control structure proposed and validated in Chapters 4 and 6, the inability of the CSI current ripple extraction scheme to reject low order harmonics which were not present in the ideal grid conditions but present now, leads to an unbalance of the fundamental current component injected through the series capacitors. The resultant CSI voltage unbalance induces low frequency power oscillations which are reflected by the CSI DC link current waveform. In order to avoid over-modulation thus maintaining the CSI filtering capability, the DC link current reference had to be increased to 5.5A. Subsequently, to avoid saturation of the active current controller (Eq. 8), which would further distort the results, the voltage reduction coefficient K has been increased to 0.15, resulting in a larger level for the fundamental voltage reduction of 15%. The component values and operating parameters are shown in Table 7-I.

Furthermore, to clearly highlight the negative effects of the unbalanced operation of the CSI input voltage V_{csi}, the phase A series capacitor voltage measurement has been taken across both the series capacitor and the CSI AC filter inductance, and is referred as $V_{c\&Lf}$. Under hybrid system operation, it can be seen that the voltages of the CSI and Series Capacitor move in antiphase with the sum of the absolute amplitudes exceeding the grid phase voltage.

Table 7-I: Component values and operating parameters for experimental topology

R_{dc}	C_{dc}	L_1	L_f	L_{dc}	R_f	R_{clamp}	R_{cs}	C_{clamp}	C_s	C_p
140Ω	550µF	11mH	300µH	30mH	50Ω	100kΩ	100kΩ	20µH	12µF	1µF
P	V_{dc}	V_{grid}	I_s	I_{dc}	K	I_{c_d} lim	I_c max	f_o	f_{sw}^{VSI}	f_{sw}^{CSI}
4.2kW	750V	415 V_{rms}	8Apk	5.5A	15%	191.9 mA	1.29 A	50 Hz	1 kHz	40 kHz

7.1.2. Transient and Steady State Operation Results for Phase A

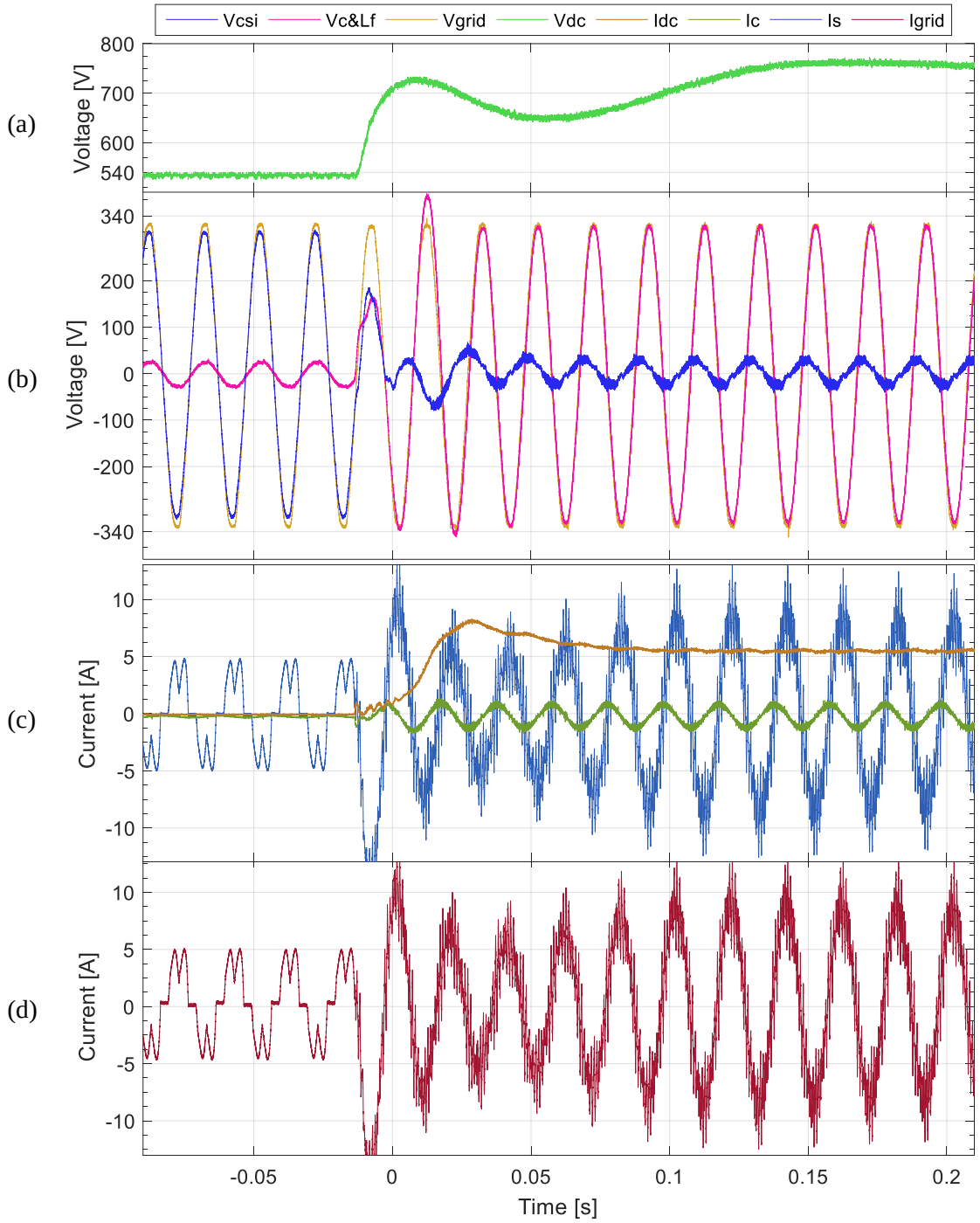


Fig 7-5: Experimental results showing PWM activation for VSI and CSI for K=0.15 (sans ripple cancellation) for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor and filter ($V_{c\&Lf}$), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

The experimental results for DC and phase-A Hybrid system currents and voltages are presented for the grid connected scenario in a similar format to §6.1.2, showing the transition following the PWM activation as well as the deployment of ripple cancellation in separate plots.

The results for PWM activation of the setup are shown in Fig 7-5. Prior activation, the setup operates in a non-linear load mode with the VSI behaving as a 6-pulse diode rectifier. The positive and negative peaks of the phase A grid voltage that is monitored are 320V and -331V, the CSI voltage V_{csi} ranges between ±304V and the series capacitor voltage $V_{c\&Lf}$ is at 27.5 and -28V (Fig 7-5b) closely matching the ideal grid scenario in CHAPTER 6. Upon PWM activation (t=-10ms) it can be seen that the voltage reduction reaches immediately steady state condition (in approx. 2 fundamental frequency cycles) with the CSI phase voltage peak reduced to -39V and +41V approximately showing a value of 12.5% compared to the grid voltage (87.5% reduction). During the transient, $V_{c\&Lf}$ experiences peaks of 380V before reaching the steady state value where peaks are matching the grid voltage. The DC link voltage of the main VSI (Fig 7-5a) shows identical behaviour to the ideal grid scenario showing that the VSI control dynamics remain the same. The DC link current of the CSI (Fig 7-5c) overshoots to 8A and then reaches steady state of 5.5A at approx. t= 80ms. The period during which the CSI active current component is clamped (Eq. 8) is at approximately 3ms (monitored through the state variables and not presented here), lower than the results in CHAPTER 6 due to the increased active current margin (191mA compared to 128mA) that corresponds to the increase of input CSI voltage (K) to 15%. During fundamental current synthesis, it can be concluded that the CSI voltage and current waveforms and their corresponding peaks match the theoretically expected behaviour.

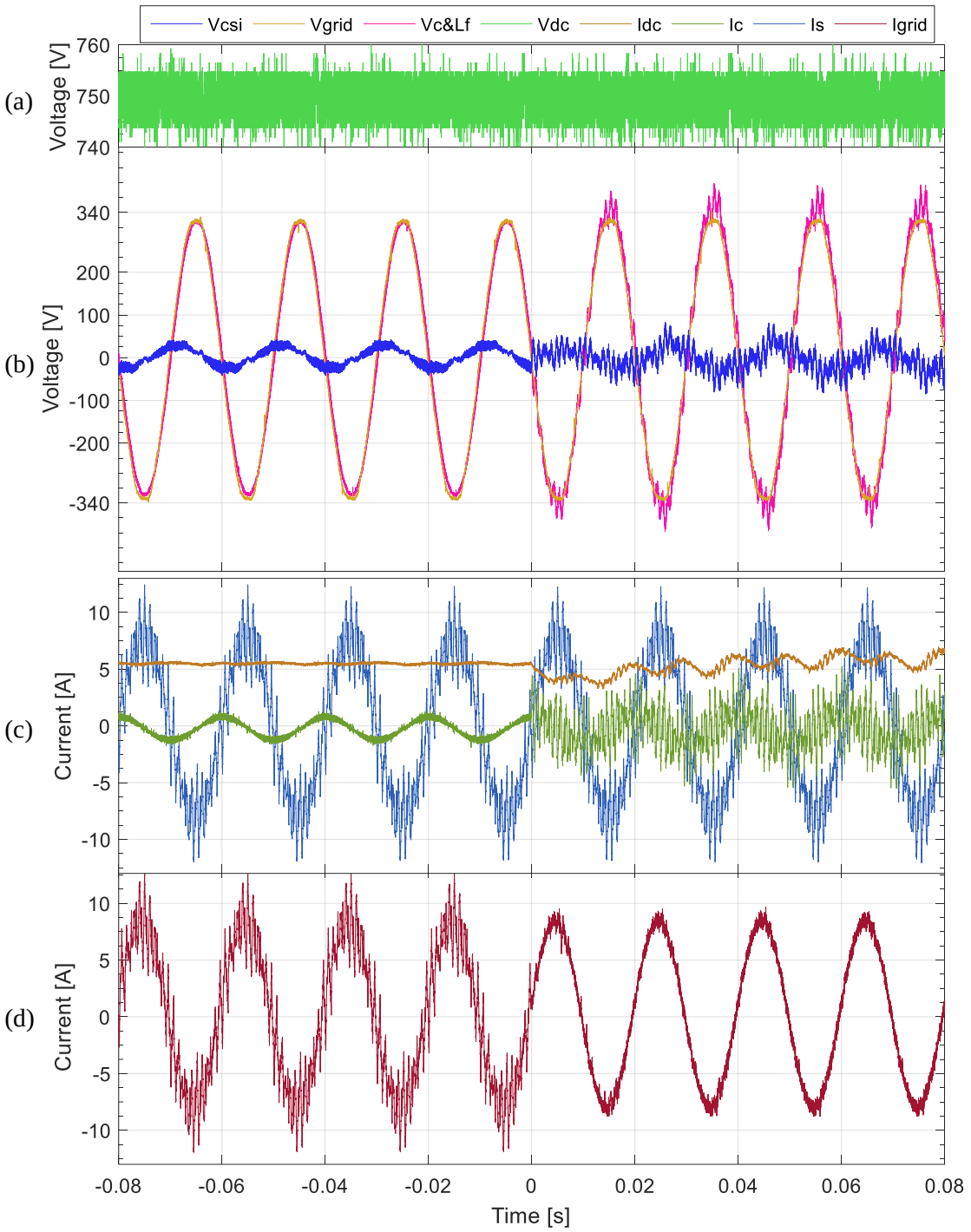


Fig 7-6: Experimental results showing activation of ripple cancellation for VSI and CSI for K=0.15 for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor and filter ($V_{c\&Lf}$), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c), ; and d) combined grid side current (I_{grid}).

Fig 7-6 shows the behaviour of the system before and after the activation of current ripple cancellation (t=0s). After ripple cancelation is activated, the CSI DC link current (Fig 7-6c) dips briefly before returning to the reference value however large first and second order harmonic oscillations (50Hz and 100Hz) can be observed signifying power oscillations that are specific to the presence of unbalance. The aforementioned action to increase the DC-link current reference (with a corresponding increase of the voltage reduction coefficient K to 0.15) however allows for sufficient margin for the AC current ripple synthesis. The successful avoidance of CSI overmodulation can be observed by looking at the CSI current I_c peaks, which remain under the I_{dc} minimum trough. The successful synthesis of harmonic currents is also evident by the visible and immediate grid side current clean-up (Fig 7-6d) which remains close to a pure sinewave with the majority of the remaining ripple at the CSI switching frequency.

As established by previous experiments, the VSI DC link voltage (Fig 7-6a) remains at the reference value and seems unaffected by the activation of ripple cancellation.

Some discrepancies can be observed during full system operation on the series capacitor and CSI voltages (Fig 7-6b) compared to previously investigated scenarios. Focusing on the CSI voltage V_{csi}, it can be seen that after the deployment of ripple cancellation, besides the expected addition of switching ripple harmonics at the VSI switching frequency, the fundamental voltage orientation is shifted. The phase shift between $V_{c\&Lf}$ and V_{csi} increases to around 134 degrees compared to around 90 degrees seen in simulations/ideal grid case, with the fundamental voltages aligned closer to anti-phase and verifying that operation has moved outside of the desired operating quadrant (see §3.3.2). The series capacitor voltage amplitude appears larger than the grid voltage with a visible low order harmonic distortion also observed on the shape.

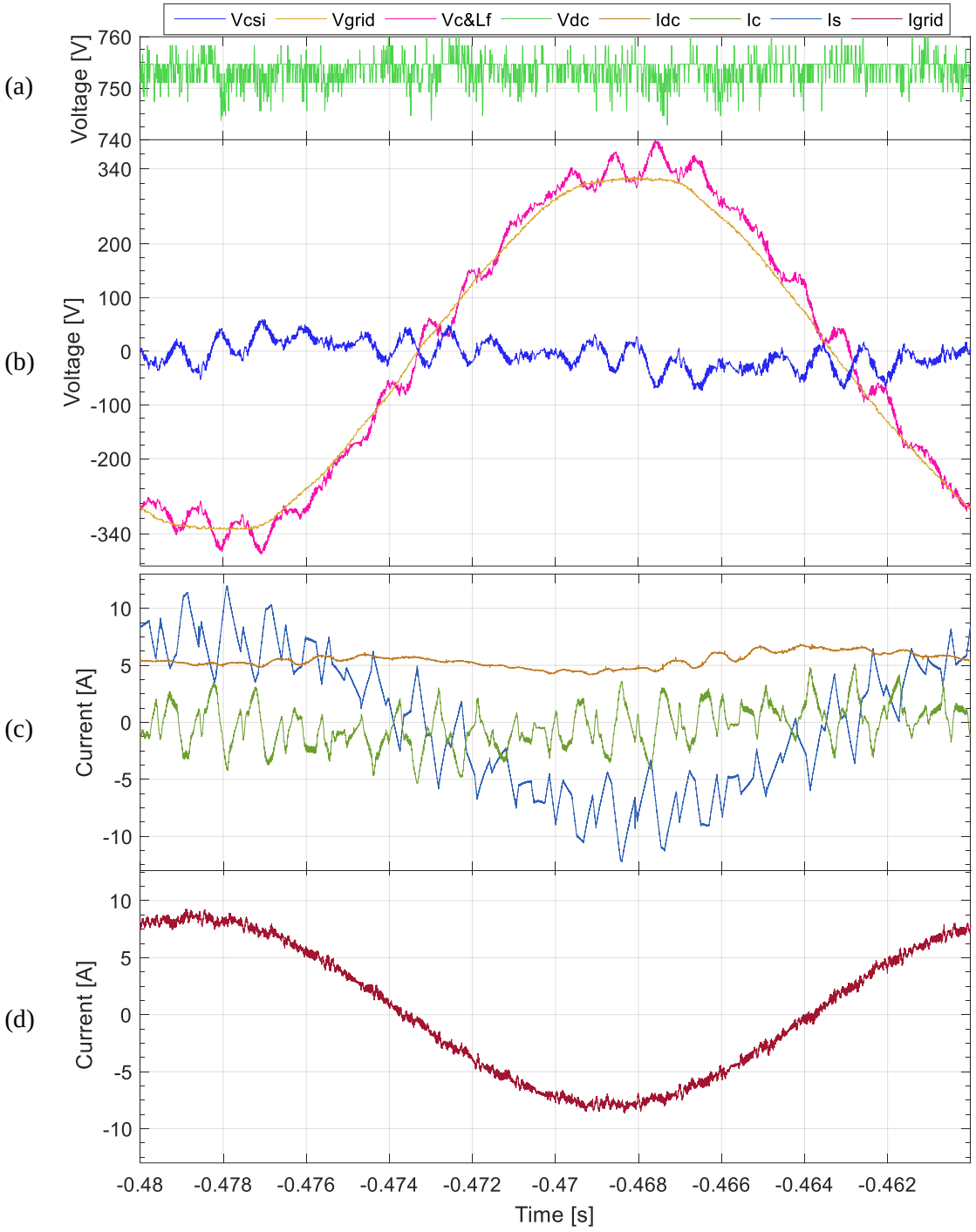


Fig 7-7: Experimental results showing one steady state cycle under full hybrid system operation for VSI and CSI for K=0.15 for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor and filter ($V_{c\&Lf}$), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

The waveforms can be inspected in more detail in Fig 7-7 where the waveforms are zoomed over a single cycle of steady state operation. The series capacitor voltage reaches a peak of 407V and minimum of -405V (Fig 7-7b) compared to ±318V before harmonic cancellation is activated while the CSI voltage positive and negative peaks have been recorded at 59V and -73V with the grid voltage at 322V and -330V. The percentage CSI voltage reduction for phase A is at 22% of the grid voltage, at relatively low levels considering the voltage reduction coefficient of K=15%. §7.1.3 will show that this is not the case for the other two phases B and C which will prove that the cause is the unbalance.

The DC link current (Fig 7-7c) mean value is at 5.44A, close to the chosen reference value. The current reaches a peak of 6.8A and a trough at 4.15A due to the prominent second harmonic oscillations. The peak-peak DC-link current ripple shows a tenfold increase in comparison with operation without ripple cancellation, where the peak and trough current values have been recorded at 5.6A and 5.4A.

The filtered grid current quality (Fig 7-7d) closely resembles the results observed under ideal grid conditions with minor notches observed corresponding to current ripple peaks. The peaks of the VSI current I_s (Fig 7-7c) have been measured at 11.9A and -12.2A while the grid current peaks have been recorded at 9.2A and -8.7A with the fundamental component peak at approximately 8A.

The harmonic content of the currents before and after the deployment of ripple cancellation is shown in Fig 7-8 where the currents are shown before cancellation, on both a linear (Fig 7-8a) and semi logarithmic scale (Fig 7-8b), and after ripple cancellation on a semi logarithmic frequency scale (Fig 7-8c). The fundamental current component before cancellation (Fig 7-8a) has been measured at 8.02A for the VSI current I_s, 1.087A for I_{csi} and 8.21A for the cumulated grid side current I_{grid}. The main I_s current harmonics at 900Hz reach 1.47A and at 1.1 kHz reach 1.455A, similar to the levels measured under ideal grid conditions.

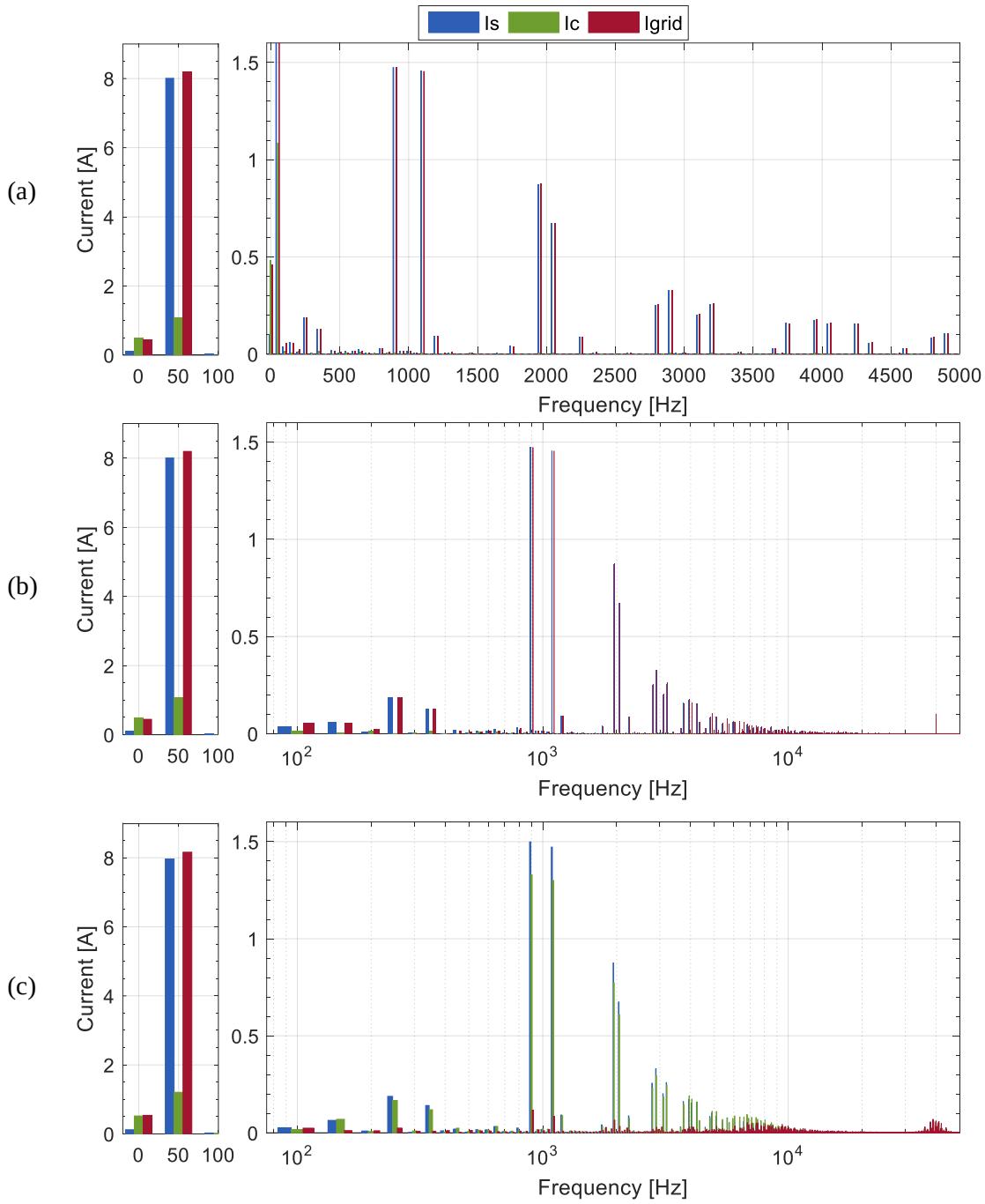


Fig 7-8: FFT of Phase A VSI current (I_s), CSI current (I_c) and grid current (I_{grid}) : a) without ripple cancellation up to 5 kHz ; b) without ripple cancellation showing harmonics up to 50kHz on a semi logarithmic scale; and c) full system operation up to 50kHz on a semi logarithmic scale.

It can be observed however that there is a noticeable increase of low order harmonic amplitudes with the largest amplitudes corresponding to the 5^{th} and 7^{th} harmonics. After switching ripple cancellation is enabled (Fig 7-8c), it is noticed that the CSI is also compensating for low order harmonics, contrary to the initial design requirements. The 3^{rd} harmonic amplitude is measured at 64.5mA for I_s, 70mA for I_c which results in the remaining harmonic in the grid side current I_g to be only 12mA (18.6% of original VSI value). The 5^{th} harmonic is reduced from 188.5mA in I_s, to 25mA (13%) in I_{grid} with the I_{csi} producing a harmonic of 166.7mA while the 7^{th} harmonic has also been reduced from 141mA (I_s) to 9mA (6%) (I_{grid}).

The current harmonics at the VSI switching frequency show a similar reduction level to the ideal grid scenario. The 900Hz harmonic is measured at 1.499A for I_s, 1.329A for I_c leaving a remaining 116.9mA residual harmonic in I_{grid}, showing a reduction to 7.8% of the original VSI harmonic level. The 1100Hz harmonic has been reduced from 1.472A to 84.87mA with I_{csi} measured at 1.31A, showing a reduction to 5.77% of the original VSI harmonic level. The harmonic at 1950 Hz has been reduced to 7.5% of the original amplitude, from 875mA to 65.66 mA and the 2050 Hz harmonic was reduced from 674mA to 33.68mA (5%). The peak level of the CSI switching harmonics cluster, at 40 kHz, is measured at less than 60mA while for the harmonics around the CSI AC filter resonant frequency it is at approx. 50mA.

The fundamental component during full system operation has been measured at 7.965A for I_s, 1.2A for I_c, and 8.16A for I_{grid} showing a marginal amplitude increase of 0.1A for I_c compared to the current injected before ripple cancellation, inferring a direct effect on the unbalance effects noticed in the time domain waveforms.

The DC component before ripple cancellation, has been measured at 0.1A for I_s and 0.5A for I_c and 0.46A for I_{grid}, while during full operation it reached 122mA for I_s, 0.52A for I_c and 0.537A for I_{grid}.

Fig 7-9 shows the corresponding frequency content for the voltages before PWM activation, during fundamental synthesis and full operation. Before PWM is enabled (Fig 7-9a), the DC

component is measured at 5.5V on the grid voltage and 4.3V for $V_{c\&Lf}$ (V_{csi} is close to zero) while after PWM activation (Fig 7-9b), the DC component is measured at 7V for V_{grid} and 1.3V for $V_{c\&Lf}$ and V_{csi}. During full system operation (Fig 7-9c) the DC component increases to 14V for the V_{csi}, 16V for $V_{c\&Lf}$ while the grid voltage remained similar at 6.9V thus showing that in this case a sizable DC offset is present and reflected across the CSI and series capacitor voltages.

It can be observed that following the PWM activation, the fundamental component of V_{csi} is reduced to 27V from 308V, while the series capacitor fundamental voltage component increases from 27.3V to 321V for a grid fundamental of 332V. Under full operation however, the fundamental component for $V_{c\&Lf}$ increases significantly to 350V, which is higher than the grid voltage, confirming that the voltage phasors V_{csi} and V_c are pointing in opposite directions as observed also in the time domain waveforms (Fig 7-7b). The CSI voltage, V_{csi} is decreased further to 23V. For the remaining spectrum, the largest harmonic amplitudes are at 900Hz and 1.1 kHz, mirrored across $V_{c\&Lf}$ and V_{csi} at 18.7V and 13.8V however a significant increase can be observed in the low order harmonic content up to the 7^{th} order.

Due to the aforementioned indiscriminate current cancellation inadvertently occurring at low order current harmonics, noticable voltage harmonic amplitudes are observed across the series capacitor and the CSI input voltage under full hybrid operation. The third harmonic amplitude is measured at 6.5V for V_{csi} and 7.9V for $V_{c\&Lf}$ from 0.8V and 1.7V before ripple cancellation is enabled while the grid harmonic remained at 2.9V. The fifth harmonic voltages also increase to 8.5V and 9.7V for V_{csi} and $V_{c\&Lf}$ while before cancellation, the amplitudes have been less than the grid voltage harmonic of 3.2V. Finally the 7^{th} harmonic is also slightly increased with 2.5V for V_{csi}, 4.6V for $V_{c\&Lf}$ and 3.2V for V_{grid}.

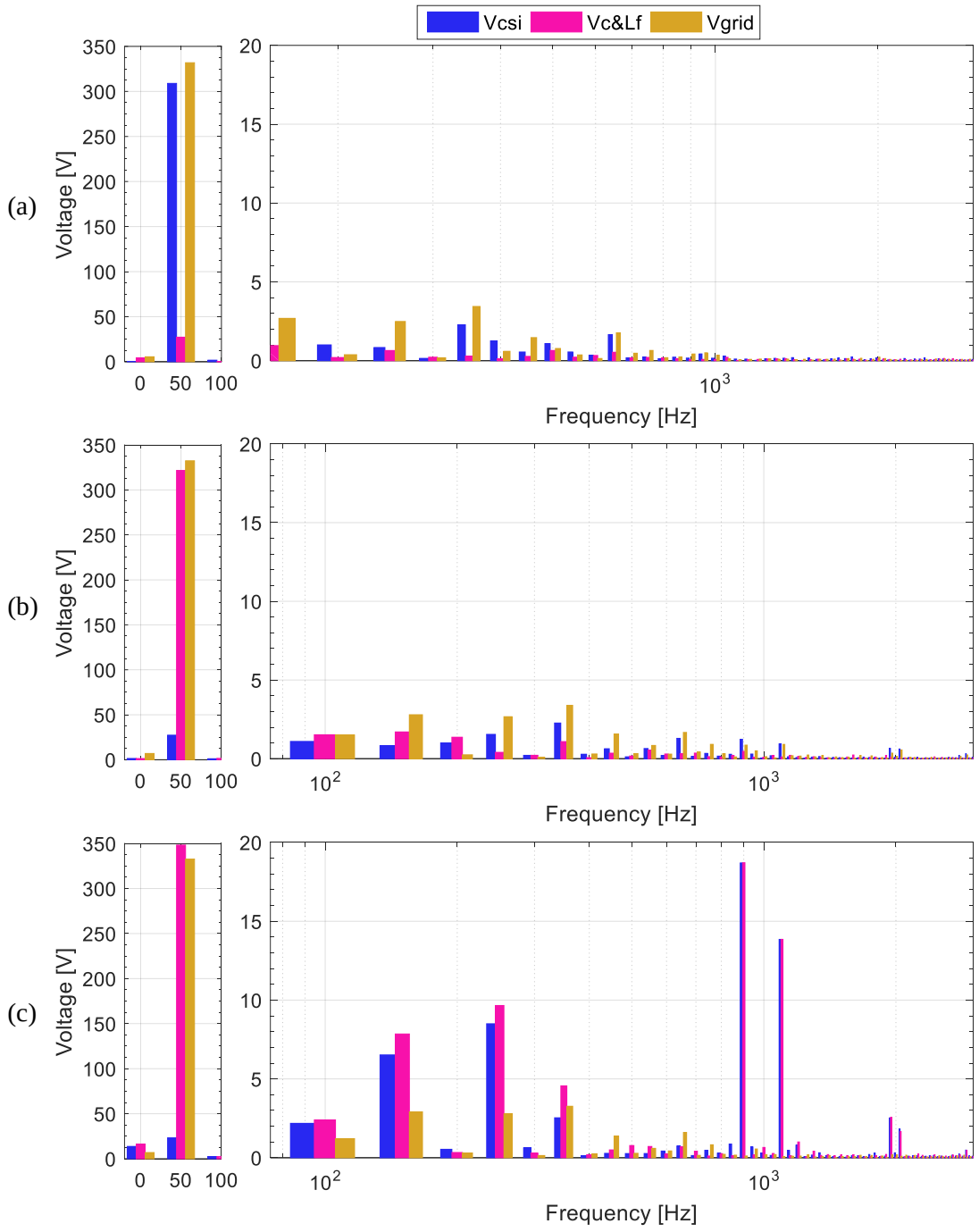


Fig 7-9: FFT of Phase A voltage of the Grid (V_{grid}), Series capacitor ($V_{c\&Lf}$) and CSI phase voltage (V_{csi}) during: a) No PWM; b) PWM enabled showing fundamental voltage reduction; and c) full system operation (harmonic cancellation).

7.1.3. Maximum Voltage Stress and Lack of Phase Symmetry

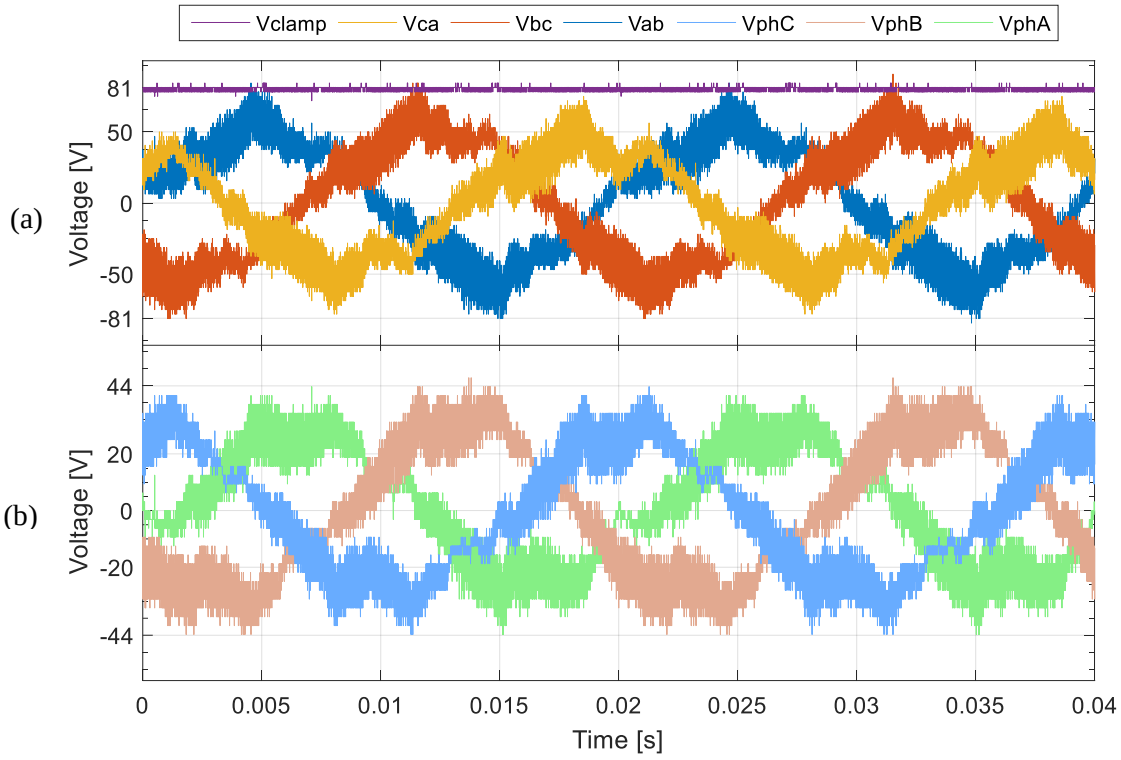


Fig 7-10: The CSI input voltages showing the fundamental voltage reduction in: a) the three phase line-line CSI voltages and the clamp voltage and b) the three phase-neutral CSI voltages.

The investigation of phase symmetry is presented in this section in order to inspect the effects of unbalance and low order harmonics present in the real grid voltage under the proposed control system presented in §5.2.2.1. Fig 7-10 shows the phase to neutral CSI voltages as well as the line-line voltages along with the DC clamp voltage before ripple cancellation. The resulting phase voltage shape is not purely sinusoidal but resembles more trapezoidal shape reflecting flat top of the grid voltage waveforms while the peak voltage reaches ±44V (Fig 7-10b). On the line to line, the harmonics appear as triangular, due to the effect caused by the aforementioned grid harmonics. The level of distortion observed is therefore due to the grid voltage shape reflected in full on the CSI voltages. As the CSI fundamental current synthesis is operating in open loop, a symmetrical fundamental current component causes the series capacitor voltages to be sinusoidal and balanced with most of the asymmetry therefore observed on the CSI voltages. Whilst distorted, the CSI voltages appear relatively balanced with the peak CSI voltage stress measured at 81V (Fig 7-10a).

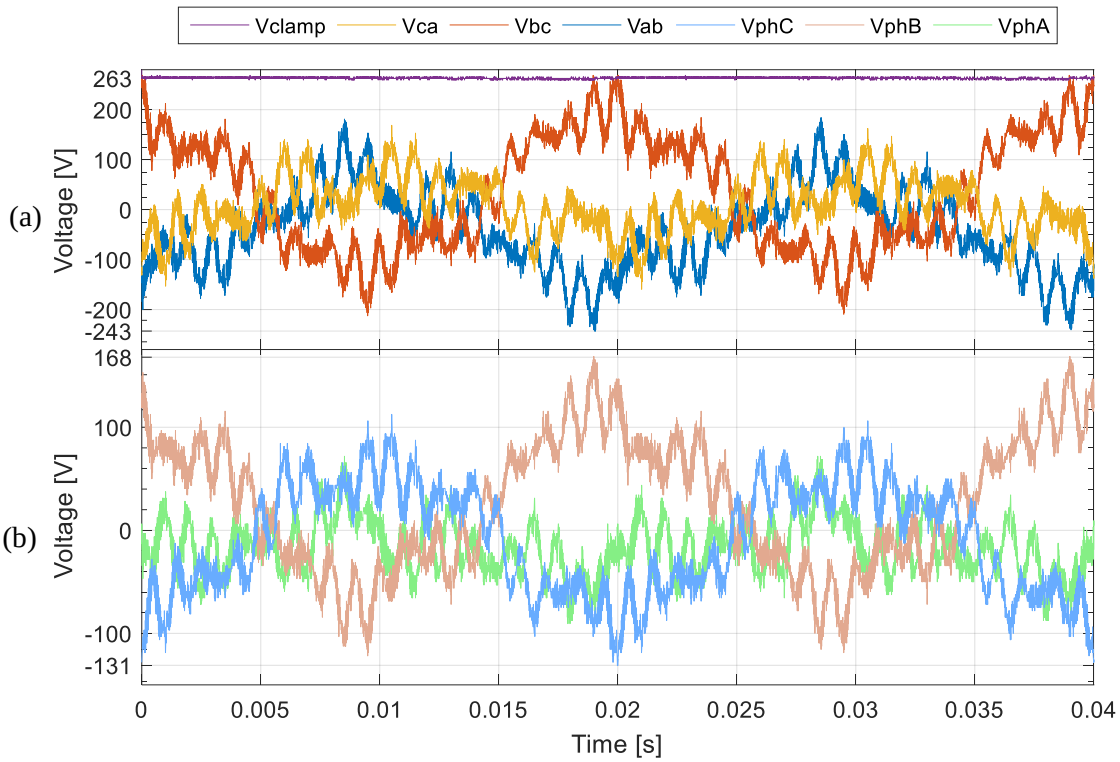


Fig 7-11: The CSI input voltages under full system steady state operation showing unbalance for: a) the three phase line-line CSI voltages and the clamp voltage and b) the three phase-neutral CSI voltages.

Fig 7-11 shows that when ripple cancellation is activated, the CSI voltages are severely distorted and unbalanced. In this case, the cause of disturbances and unbalance is not a direct effect of the grid voltage shape but rather due to the interaction of the control system combined with the inability to reject completely the low order harmonics from appearing the reference CSI currents while also altering with the fundamental component value. The phase voltages are shown in Fig 7-11b where it can be seen that while phase A voltage is at the lowest levels, phase B and C are in anti-phase with the three phase waveforms no longer attaining/exhibiting the 120 degree that is characteristic for a three phase symmetrical system. The highest positive peak phase voltage is recorded at 168V for phase B while the highest negative peak is at -131V for phase C. The line-line voltage waveforms (Fig 7-11a) show a similar level of disturbance with the peak CSI voltage stress at 263V representing a percentage of 45% compared to the grid, much larger than the theoretically expected minimum of 25% (15% fundamental & 10% switching harmonics).

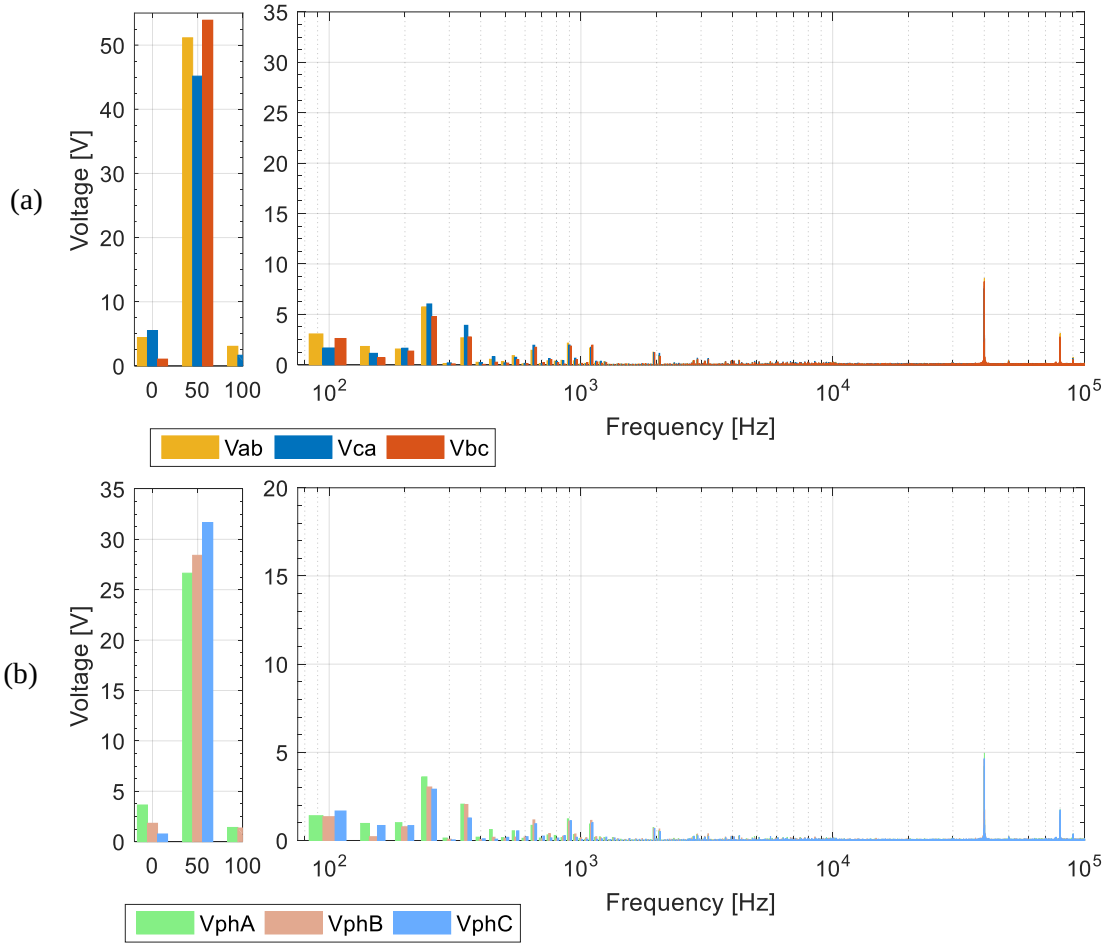


Fig 7-12: FFT of the CSI input voltages under fundamental voltage reduction mode showing the harmonics in: a) the three phase line-line CSI voltages and b) the three phase-neutral CSI voltages.

Fig 7-12 shows the frequency content of the three phase-neutral and line-line CSI voltages before current ripple cancellation. The fundamental frequency components reach 26.6V, 28.4V and 31.7V for phase A, B and C respectively while on the line to line voltage spectrum they reach 51V, 45V and 54V for V_{ab}, V_{ca} and V_{bc}. A small DC component can be observed at 3.6V, 1.8V and 0.8V for phases A, B and C while this appears as 4.4V, 5.5V and 1V on the line to line FFT spectrum. Excluding the fundamental component, the biggest harmonic amplitude is created around the CSI switching frequency with the amplitude of 40 kHz ±50Hz harmonics reaching 4.6V on the phase voltages and approx. 7.5V on the line-line voltage. The 5^{th} harmonic which appears to be the most pronounced low order harmonic is at 1.4V for phases A and B and 1.7V for phase C and 5.7V for V_{ab}, 6V for V_{ca} and 4.8V for V_{bc}, similar to grid voltage levels.

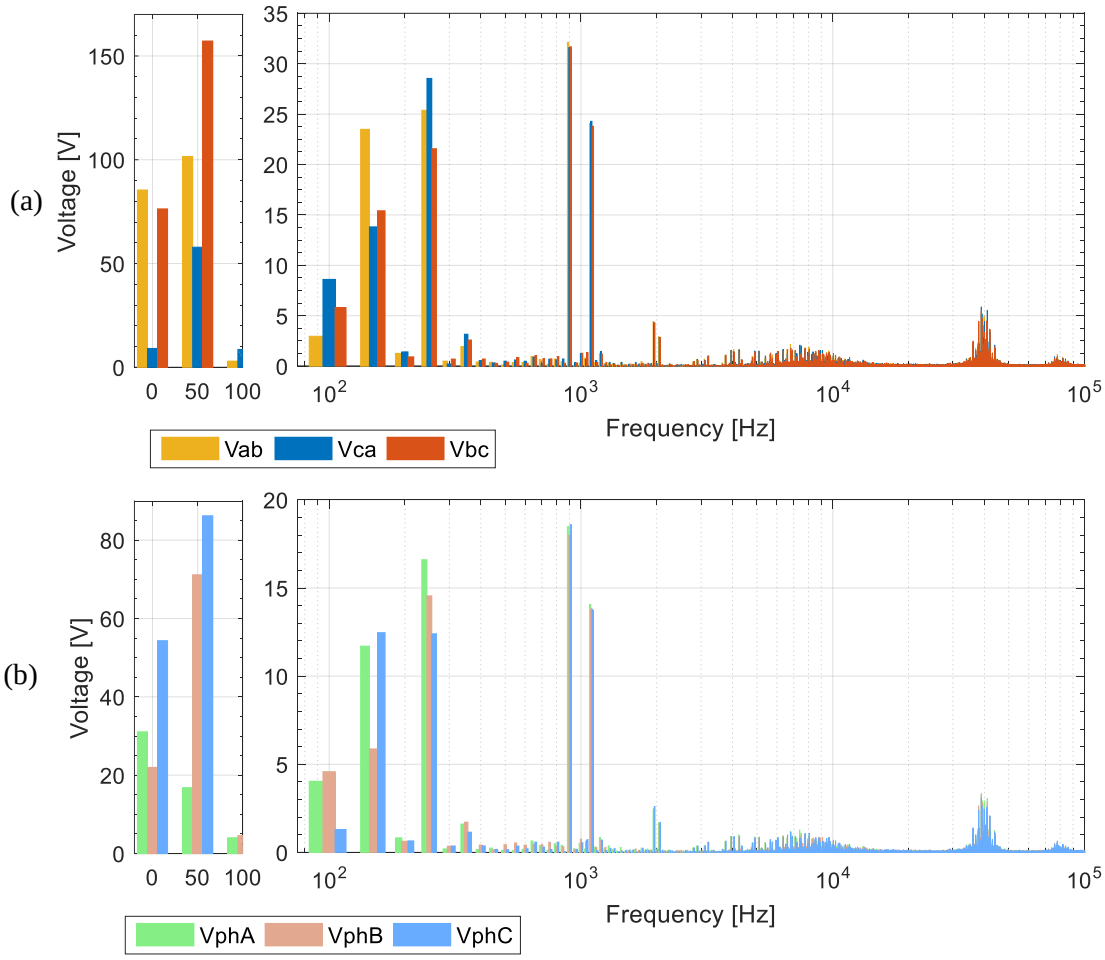


Fig 7-13: FFT of the CSI input voltages under full system steady state operation showing the harmonics in: a) the three CSI line-line voltages and b) the three phase-neutral CSI voltages.

Fig 7-13 shows the three phase and line CSI voltages under full system operation revealing the large level of unbalance for all harmonics below 500 Hz. The fundamental component have been measured at 16.8V, 71.2V and 86.2V for phases A, B and C while the line-line voltage fundamentals are at 101.5V, 57.9V and 157.2V for V_{ab}, V_{ca} and V_{bc}.

In addition the DC component has been measured at 31V, 22V and 54V for the A-B-C phase voltages while the line to line has been measured at 85.4V, 9V and 76.3V, at detrimental levels for the voltage reduction scheme. The third harmonic phase voltages are measured at 11.7V, 6V and 12.4V and line harmonics at 23.5V, 13.8V and 15.4V. Fifth order harmonics appear at 16.6V, 14.6V and 12.4V for phases A-B-C and 25.38V, 28.54V, and 21.56V for the line-line 5^{th} harmonics.

The harmonics caused at the VSI switching frequency appear to be balanced with the amplitude of the 900Hz harmonics at 18.5V, 18V and 18.6V and the line to line measured at 32.1V,31.6V and 31.7V. Similarly the harmonics at 1.1 kHz are measured at 14V, 13.8V, 13.8V for phase A-B-C harmonics and 24V, 24.3V, 23.8V for the line-line voltage harmonics.

The harmonic analysis of the CSI input voltage waveforms verifies that the severely distorted CSI input voltages observed are due to fundamental voltage component unbalance (as well as lack of associated phase alignment visible on the time domain waveforms), a significant DC voltage offset, and in part due to the presence of low order harmonic voltages caused by the generation of low order current harmonics by the CSI. The fact that this behaviour is not observed before the activation of current ripple cancellation signifies that the unbalance is not a direct effect of the grid voltage imbalances. Furthermore the change in amplitude of the CSI current observed previously implies that the CSI voltage unbalance is associated with the control system operation which is affected by the interaction with the grid imbalances. The unbalanced behaviour observed causes an increase in both the maximum CSI voltage stress as well as current stress due to large DC link oscillations.

7.1.4. Simulation of Hybrid Converter Operation Emulating the Real Grid Imbalance and Harmonics

To further scrutinise the dynamics of unbalanced voltage operation under the specific grid imbalances (whilst isolating/excluding specific effects) the investigation has been carried out in simulation. The simulated grid voltage has been replicated considering harmonics up to the 9^{th} order, according to the harmonic content shown in Fig 7-3. The frequency of the grid voltage has been set at the nominal 50Hz. No grid side inductance was modelled thus investigating only the effect of the control system operating under the particular grid harmonic conditions. Thus the simulated operation is excluding the effects of grid frequency variation, grid impedance as well as the possibilities of errors due to sensing, propagation delays in the control system or hardware/equipment induced issues.

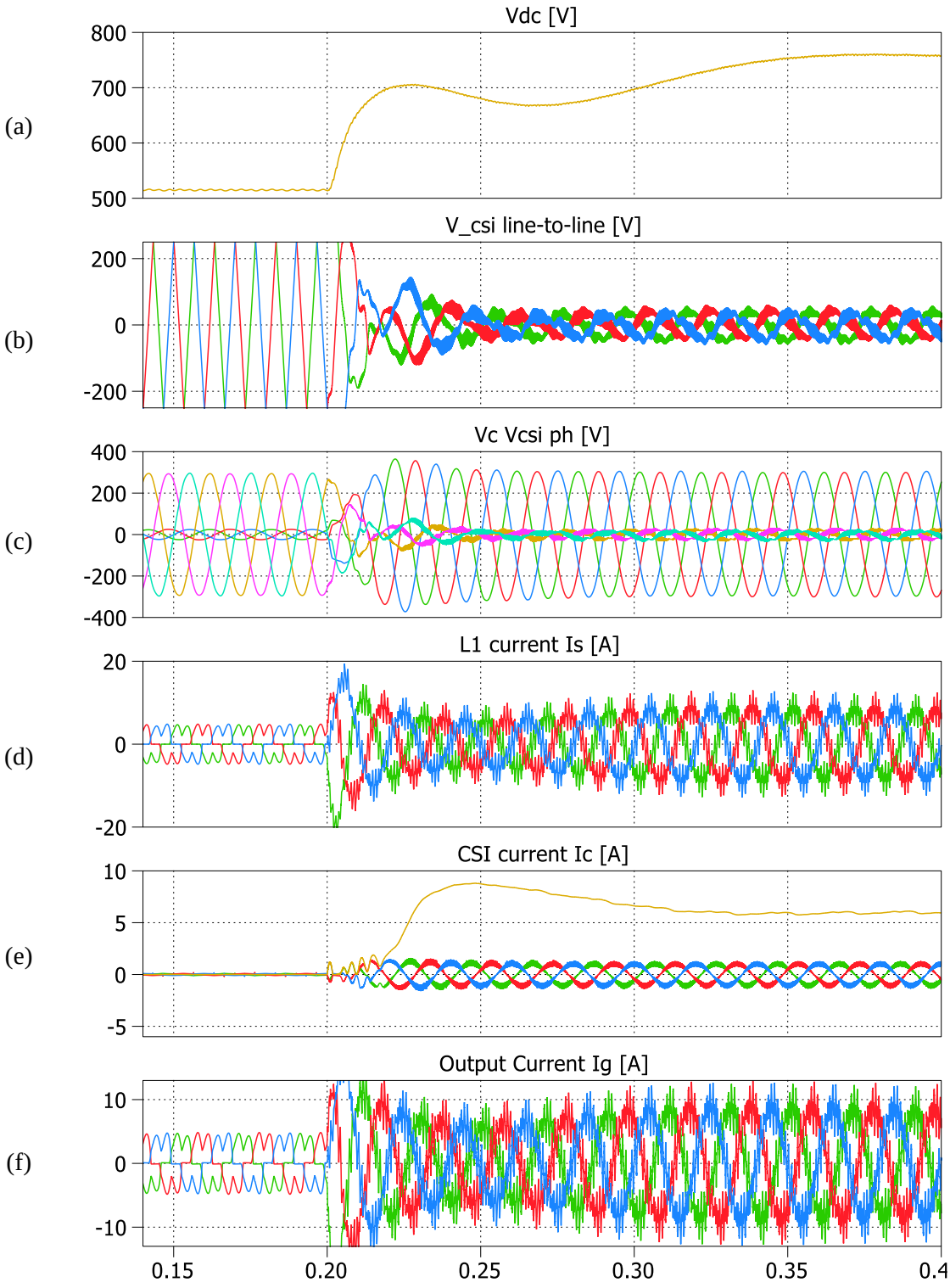


Fig 7-14: Simulation showing the waveforms prior and after PWM activation for: a) VSI DC-link voltage; b) Line-To-Line CSI Voltages; c) Line-To-Neutral CSI And Series Capacitor Voltages; d) Input (Main Converter) Current ; e) CSI Current on the DC and AC side; f) Output Grid Current.

The control system as implemented in the experimental rig has been replicated in its discretised form, including sampling delay, with the VSI modulator operating independently from the CSI matching the control scheme outlined in CHAPTER 5. The voltage reduction coefficient K has been set at 15% with a DC-link current reference of 5.5A.

Fig 7-14 shows the operating waveforms for the system during the activation of PWM for both converters. Before t=0.2s, the DC link voltage (Fig 7-14a) is at 515V, approx. 20V lower than the corresponding experimental voltage showing some discrepancy between the results. The enabling of PWM creates a current overshoot observed on the grid and converter side currents reflected by the steep rise of the voltage, reaching 700V after one cycle (t=0.22s). A small VSI DC-link voltage dip to 670V is then observed (t=0.27) with the 750V reference value reached within ten fundamental cycles (t=0.4s). The VSI transient behaviour shows good correlation with the experimental waveforms seen in the previous chapter.

After PWM activation, the DC link current (Fig 7-14e) of the CSI overshoots to 8.8A, slightly higher than the peak seen experimentally, before settling to the 5.5A reference value (t=0.32s). The CSI voltage reduction is immediately apparent (Fig 7-14c) on the phase voltage which is reduced from a 295V peak, to 31V. The series capacitor voltage increases from 26V to approximately 306V on all three phases. The line to line CSI voltage (Fig 7-14c) reaches 60V, lower than the experimentally acquired value.

The activation of ripple cancellation, shown in Fig 7-15, has no noticeable effect on the VSI waveforms as seen by the VSI DC-link voltage, remaining constant at the 750V reference value, or the main VSI currents I_s. On the other hand the CSI AC and DC side waveforms demonstrate the severe distortion previously noticed in the experimental evaluation which can now be observed for all three phase AC waveforms. As observed previously, the CSI DC-link current oscillations, reflect the AC side voltage unbalance and DC offsets.

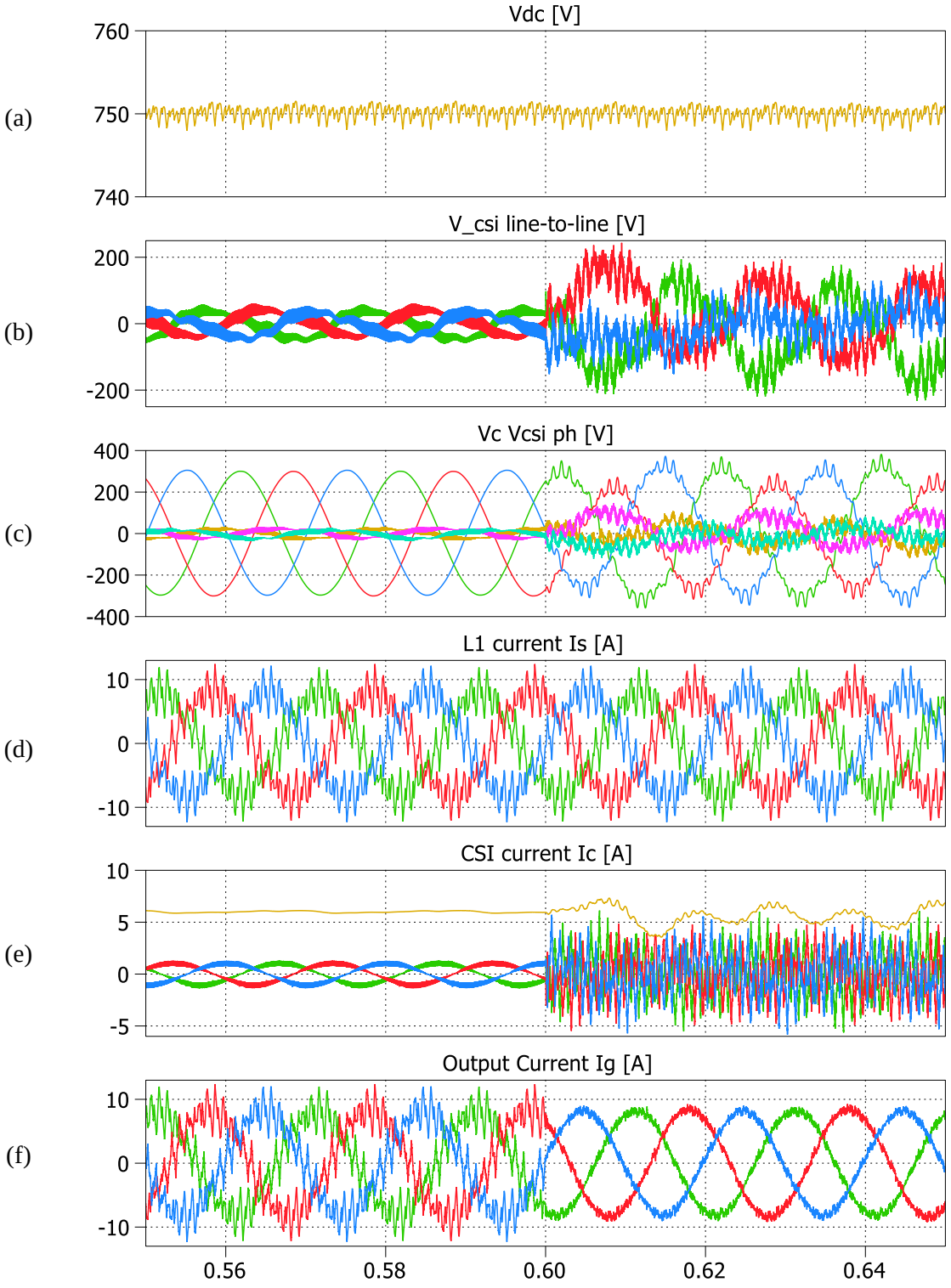


Fig 7-15: Simulation of the transient caused by the activation of ripple cancellation showing the waveforms of a) VSI DC-link voltage; b) Line-To-Line CSI Voltages; c) Line-To-Neutral CSI And Series Capacitor Voltages; d) Input (Main Converter) Current ; e) CSI Current on the DC and AC side; f) Output Grid Current.

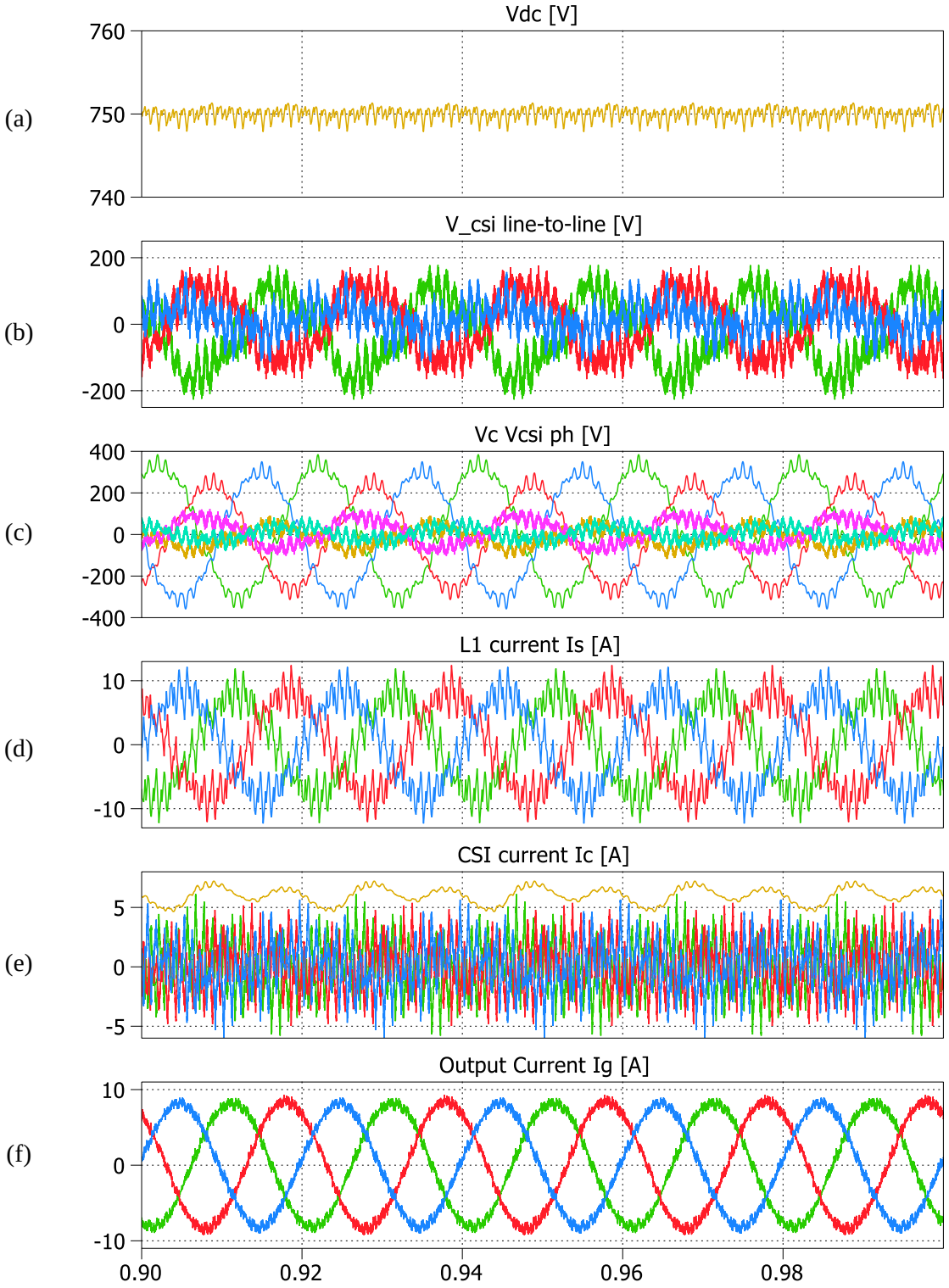


Fig 7-16: Simulation of the full hybrid operation in steady state showing the waveforms of: a) VSI DC-link voltage; b) Line-To-Line CSI Voltages; c) Line-To-Neutral CSI And Series Capacitor Voltages; d) Input (Main Converter) Current ; e) CSI Current on the DC and AC side ; f) Output Grid Current.

The waveforms are analysed more closely in steady state conditions shown in Fig 7-16. The CSI DC link current shows significant ripple reaching a peak of 7A with the trough measured at 4.1A due to the oscillations at the first and second harmonic as seen in Fig 7-16e caused by the interaction of 50Hz current with the DC offset and unbalance present in the input CSI voltages. The unbalance can be observed on the series capacitor voltages, which are close to the 120º phase symmetry but have variable fundamental amplitudes which cause a subsequent phase and amplitude unbalance on the CSI phase voltages. The unbalance is then reflected on the CSI line-line voltage waveforms which range from 195V to -235V, closely matching the maximum voltage stress experienced experimentally.

Nevertheless, the positive effect of the current ripple cancellation is evident on the quality of the output grid side currents (Fig 7-16f) where most of the remaining ripple occurs at the CSI switching frequency. The THD is reduced from 29% to 5.8% with the peak current being reduced from 12.35A on the main VSI current I_s to 9A on the grid side current I_g. However some discrepancies can be observed between the amplitudes of the three phase grid currents which shows that the unbalance also occurs in the current waveforms as it will be discussed in the next section.

The above simulation shows reasonably good correlation between the effects noted in the experimental results and the simulated system behaviour achieved under the replicated grid conditions. The simulations verify that the heavily unbalanced conditions seen at the CSI inputs are not due to grid frequency variations, grid impedance effects or other hardware related issues which are not modelled in the simulations above. Furthermore, as the unbalance occurs only under full Hybrid system operation it can be deduced that the cause is due to the implemented control system under this mode of operation and its interaction with the given grid voltage imbalances. The resulting problems in unbalanced operation significantly inhibit the voltage reduction capability of the CSI, with the maximum voltage stress reaching up to 45% of the grid, cancelling most of the advantages of using the series capacitors. Additionally the maximum CSI current stress is also increased due to DC-link current oscillations resulting in a significant increase of

the installed power in the switches which reaches approximately 17.5% of the VSI in simulation. On the other hand, the ability of the CSI to synthetize a given current demand is not compromised, revealing the robustness of CSI operation under the non-ideal operating conditions. For operation at MV grid levels however, the increase of CSI voltage stress would prohibit the use of low voltage rated semiconductors therefore any CSI problems caused by voltage unbalance should be mitigated.

7.1.5. Analysis of the CSI Voltage Unbalance Mechanism

As previously suggested, the additional CSI voltage stress and unbalance are caused by the interaction of the control system with the grid voltage imbalance when the current ripple cancellation is enabled to achieve full hybrid system operation. The observed behaviour indicates that the problem is associated in particular with the implementation of the current ripple extraction scheme. It should be stressed though that the cause is directly related to the VSI performance where the control has been designed to address the original challenge of achieving good steady state operation considering an ideal grid scenario.

The chosen VSI operating point which considers a large current ripple with respect to the fundamental current component imposed restrictions on the tuning of the PI controllers on top of the limitation due to the relatively low switching frequency. Fig 7-17 shows the filtered and unfiltered VSI active current component (shown as I_d in red) along with the AC current ripple, captured at 40 kHz using the DSP host interface, for two cycles. The moving average (MA) filter output (green), which is used to downscale the waveform to 1 kHz (see §5.2.2.1), is superimposed on the VSI active current component, showing that a significant amount of residual oscillations is still present. These oscillations occur by the instantaneous change of the filter output average during the high di/dt transitions, characteristic of the current ripple waveforms, caused by using a relatively small averaging window of 1ms. As the MA output waveform is used for the VSI current controllers, increasing the MA window would not be desirable as it would also increase the associated delay and possibly interfere with the controller bandwidth and stability. Therefore the residual MA filter output oscillations practically imposed a restriction on the maximum

possible proportional gain used in the VSI current controllers in order to achieve good steady state performance.

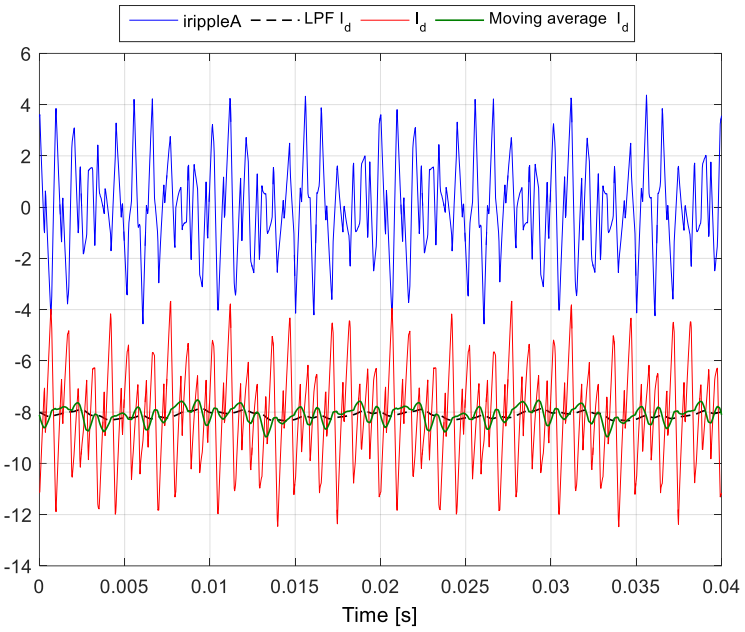


Fig 7-17: VSI current dq components captured through the dsp host interface for two cycles

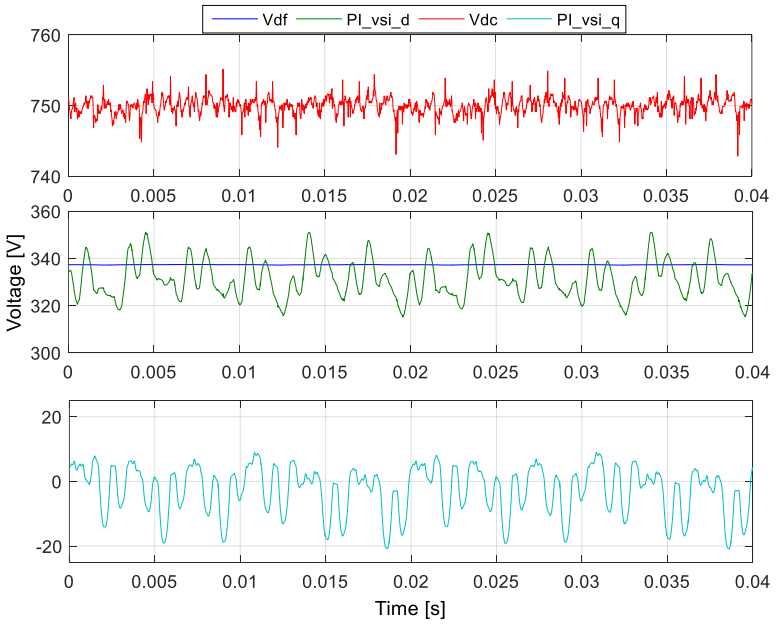


Fig 7-18: VSI DC link voltage as well as PI current controller output waveforms, captured using the dsp host interface for two cycles.

Fig 7-18 shows the dq output waveforms of the VSI PI current controllers, which are subsequently scaled by the DC link voltage as part of the modulation index calculation. A further increase in the VSI current controller proportional gain would also amplify the residual oscillations observed, with the increase leading to an AC current quality reduction or possible instability. A similar effect has also been observed when using the PI cross-coupling terms under these conditions of operation with large DQ current ripple.

Furthermore the operation under the grid voltage imbalances, given the structure of the VSI control scheme where the q-axis grid voltage feedforward term has been omitted, results in a limited resolution 1in the control of the three phase AC current waveforms. If the oscillation caused by the grid voltage unbalance is not fed forward, the PI controllers would need to estimate it which is difficult if the controllers are not fast. A second implication is that the low bandwidth of the VSI current controllers has limited capabilities of dealing with grid induced harmonics, which results in the presence of low order harmonics in the AC current waveforms.

Fig 7-19 shows the three phase grid currents before cancellation. Although the large amount of current ripple in the three phase current waveforms makes it difficult to distinguish any unbalance or low order harmonics, these can be observed in the frequency domain shown in Fig 7-20, which also shows a discrepancy between the fundamental amplitudes produced by each phase. The fundamental component amplitudes for phases A-B-C are 8.335A, 8.454A and 8.2A. The level of mismatch between the amplitudes is approximately 3% at a similar level to the grid side voltages. Furthermore the low order harmonics produced are at approx. 0.122A for the 3^{rd} harmonic, 0.29A for the 5^{th} harmonic and 0.2A for the 7^{th} harmonic.

It can be summarised that the implemented VSI control system under real grid voltage conditions will result in different effects which must then be considered separately from the CSI point of view. The first detrimental effect is the mismatch between the VSI AC current fundamental component amplitudes. The second effect is the presence of low order harmonic content in the currents. Additionally the low order current harmonics amplitudes will not be equal between the three phase VSI currents but instead will occur at variable levels similar to the low order harmonic

content of the grid voltage. These effects make the extraction of the switching current ripple from the VSI currents more difficult.

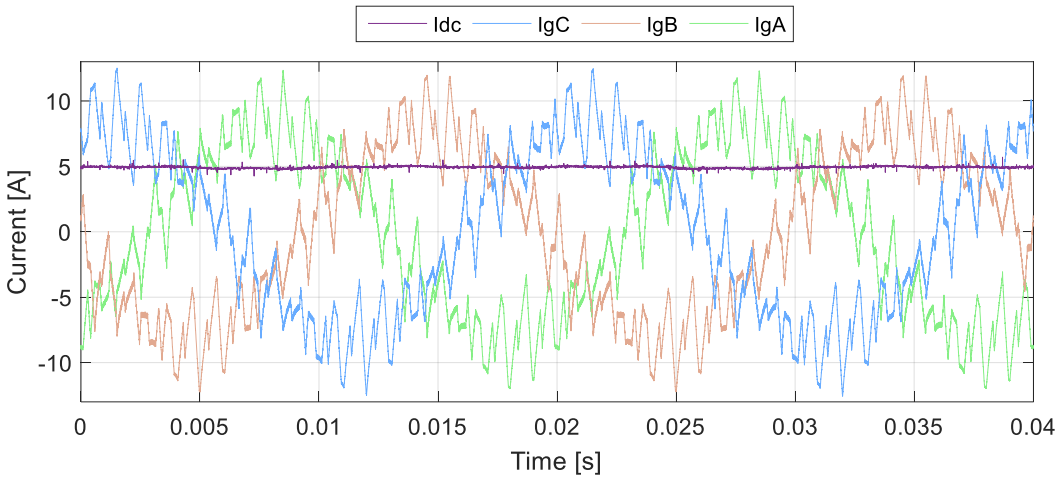


Fig 7-19: The three phase grid currents prior to current ripple cancellation.

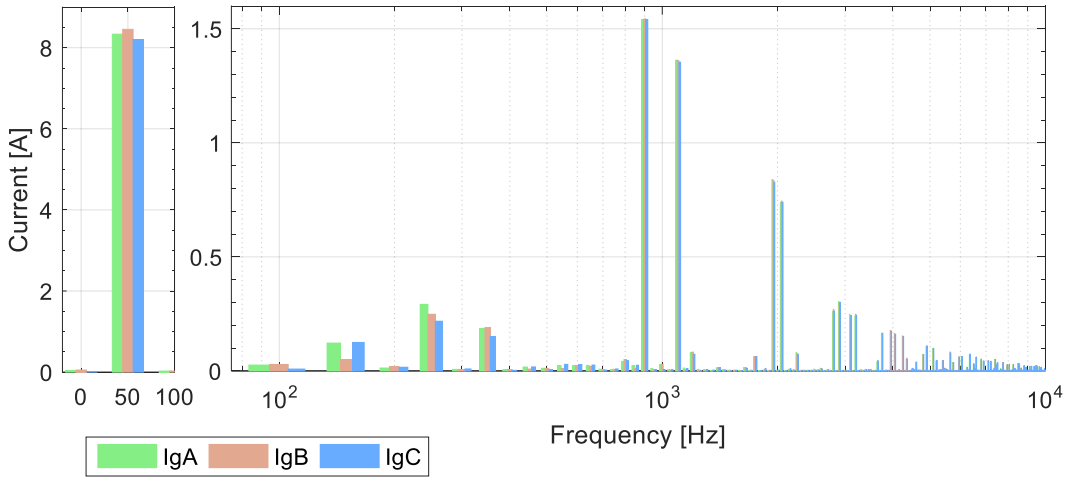


Fig 7-20: FFT of the three phase grid currents prior to current ripple cancellation.

The current switching ripple extraction controller was initially optimised for best steady state performance in ideal grid conditions. This means that in order to extract the current ripple with frequencies higher than 700Hz with negligible phase shift, it has been implemented to use an additional low pass filter (LPF), following the MA filter in the dq reference frame. The outputs of the LPF are then converted to the filtered abc current components using the Park transformation. As a requirement for operation with unbalanced current amplitudes, the

fundamental amplitudes of the filtered VSI abc current outputs must reflect any imbalance as seen in the converter side currents, otherwise risking for the imbalance to be added to the CSI reference currents.

The output of the low pass filter, is also shown superimposed on the d-axis current component in Fig 7-17. The fundamental current imbalance is seen as a 2nd harmonic in the dq-current oscillations and should theoretically propagate through the LPF and therefore should be eliminated from the resulting extracted current ripple that is added to the CSI reference current waveforms.

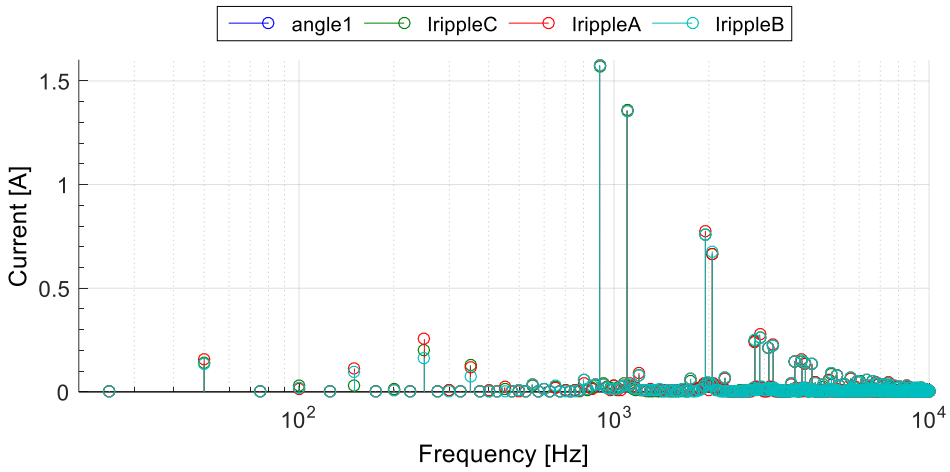


Fig 7-21: FFT of CSI current ripple reference captured using dsp host interface

However on the practical implementation, a residual fundamental component of approx. 0.15A can be seen on all three phases of the CSI reference currents as shown in Fig 7-21. Although this amplitude is small (~2%) compared to the nominal fundamental VSI current, it is significantly large when compared to the desired fundamental CSI current component, reaching up to 12% of its theoretical maximum amplitude calculated at approx. 1.3A. The resulting fundamental current disturbance is therefore propagating through the current ripple reference waveforms causing misalignment and amplitude mismatch on the series capacitor voltages, as previously demonstrated in Fig 7-16, thus creating a significant inverse sequence unbalance on the CSI input voltages.

The current ripple extraction becomes even more challenging when considering the VSI low order harmonic current content (3^{rd}, 5^{th}, 7^{th}). In order for these harmonics to be removed from the current ripple reference waveform, the cut-off frequency of the LPF used would have to be significantly raised. This would be undesirable as it would lead to a decrease in attenuation at 700Hz, thus hindering the filtering capability of the CSI (Fig 7-22). It can be observed that for cut-off frequencies higher than the 120Hz (shown on the left in Fig 7-22) which was which was hitherto the cut-off frequency used for the experimental evaluation the accuracy of extraction of the VSI switching current ripple will be affected. On the other hand, for very low cut-off frequencies of LPF, (Fig 7-22 shows on the right side the result with 8Hz cut off frequency) the maximum VSI switching ripple will be extracted, but also will contain any low order harmonics present in the VSI current waveforms. If a more advanced filtering technique is not implemented, a compromise between accurate switching ripple removal and robustness to imbalance/low order harmonics would be necessary which will result in permitting a level of lower order harmonics to be also cancelled by the CSI. Furthermore, the use of a very low cut-off frequency will result in a residual fundamental current disturbance to propagate to the CSI reference currents in the extracted ripple waveforms which is the case of unbalanced VSI fundamental current component amplitudes. A solution for the former could either be derived by the improvement of the VSI control scheme to mitigate any unbalance in the three phase fundamental VSI currents or by improving the CSI control scheme to prevent any fundamental component unbalance from being synthetized by the CSI.

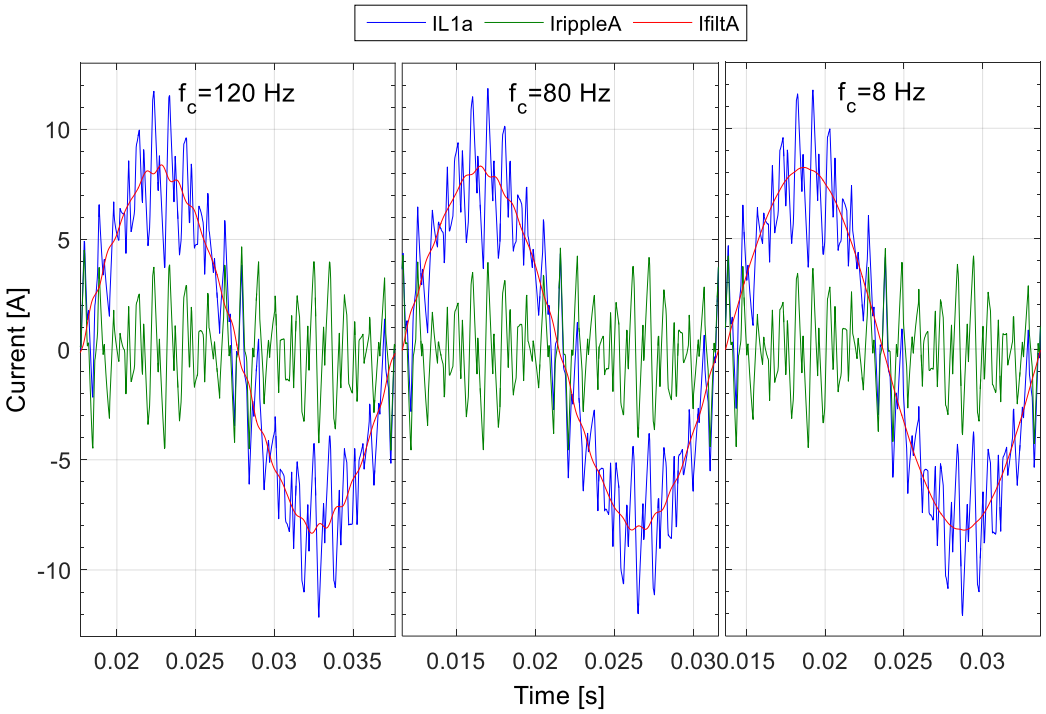


Fig 7-22: Current ripple extraction using different low pass filter cut-off frequency captured through the dsp host interface.

This situation also creates a counter-argument to the initial design choice favouring a smaller series capacitance due to its lower current requirement to synthetize a given fundamental series capacitor voltage. By extension, using a smaller series capacitance becomes more prone to low order current harmonic disturbances due to the larger harmonic voltages created across Cs that are then reflected across the CSI inputs. As a result, for operation under real grid conditions with a small series capacitor, additional control considerations must be put in place.

7.1.6. Solutions for Mitigation of the CSI Voltage Unbalance

The solution to mitigate the voltage unbalance problem previously described, could be delivered through further development of the VSI controller to improve the converter side current quality by minimising unbalance and the low order harmonics. Given that the main scope of this investigation is focused on the CSI performance, it was deemed more relevant to identify solutions which could be implemented through the CSI control which could ultimately enhance the

robustness of the CSI operating in a more general way under unbalanced conditions (grid voltages or unbalance of series capacitors).

Two different directions have been followed towards the identification and evaluation of possible solutions, the first being an offline approach which is shown to be unsuitable, and the second direction focusing on online methods.

7.1.6.1. Using a Look-Up Table for Switching Current Ripple Reference

The following test has been performed to demonstrate the possibility of balanced operation under given grid imbalance conditions using an alternative control approach. The approach used is based on the prevention of any low order harmonic distortion in the CSI reference waveforms. In order to guarantee that the harmonic spectrum of the current ripple reference waveforms to the CSI does not include any low order harmonics, an offline approach to validate the concept was necessary. The results also identified the additional challenges and considerations which need to be taken for such a method to be successfully implemented. First, the CSI reference current ripple waveforms have been captured for the three phases under steady state operation and post-processed to remove all harmonics under 700Hz. Then, the post-processed current reference ripple waveform has been saved for one fundamental cycle (800 samples) in a lookup table which is then aligned at the beginning of each fundamental based on the grid voltage angle extracted by the PLL.

The implication of the grid frequency variation around 50Hz compared to the fixed converter switching frequency (which practically translates to a non-integer number of samples per cycle) means that the switching ripple pattern throughout a cycle does not remain constant but instead can be seen to shift over a large number of cycles.

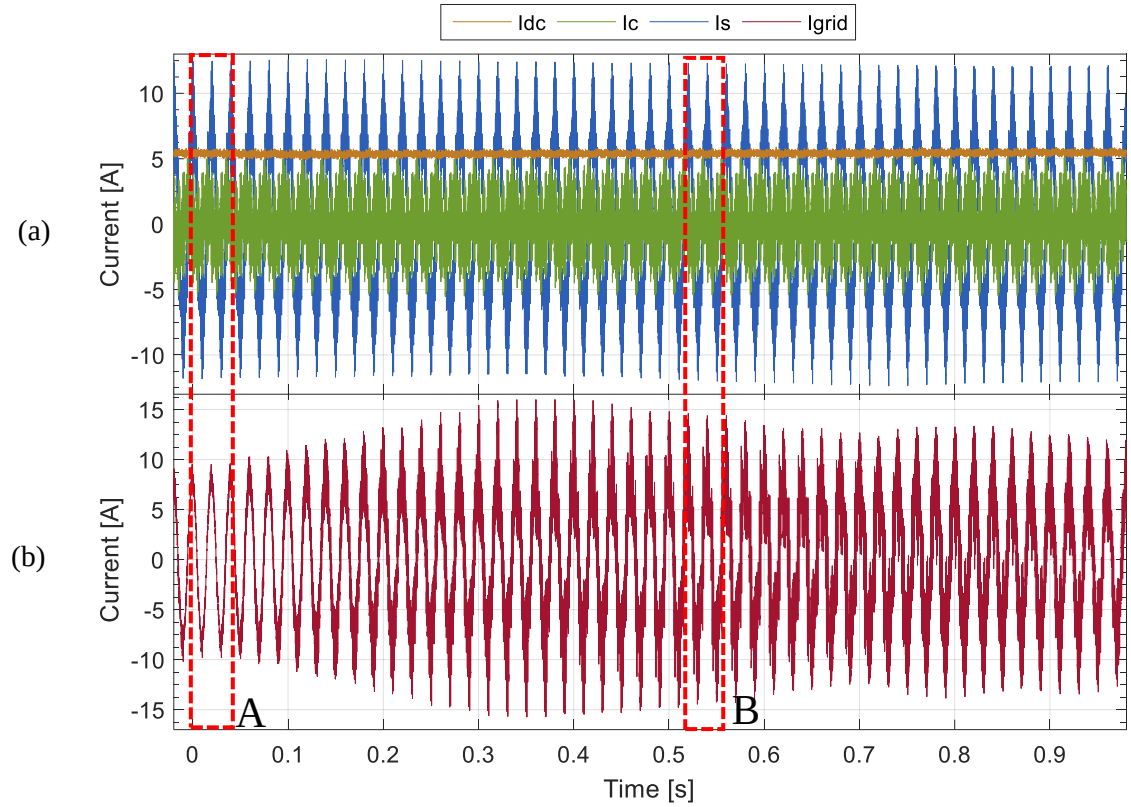


Fig 7-23: Experimental results showing steady state operation for one second under full system operation for Phase A and CSI DC side currents when using a look-up table for current ripple cancellation: a) CSI DC-link, series capacitor current and main VSI current; and b) grid current.

As a result, the effectiveness of storing the current ripple pattern for one cycle is practically limited with cancellation only achieved for a small number of cycles as seen in Fig 7-23 which shows the steady state waveforms for Phase-A currents over a one second period. The highest convergence between the reference current ripple waveforms and the VSI current ripple is achieved for two cycles (0-0.04s). For the remainder of the capture window, the ripple in the waveforms moves out of phase which can be observed by inspecting the envelope of the grid side current (I_{grid}).

The best ripple cancelation waveforms that take place in the first two cycle periods (as highlighted by the dashed lines marked as area “A” in Fig 7-23) ae shown in Fig 7-24, showing the maximum cancellation achieved. In Fig 7-25, the currents are shown when the ripple in the two waveforms are out of phase (area “B” in Fig 7-23) leading to the disturbance to add up/double in the grid side current, a highly undesirable operating condition.

(a)

(b)

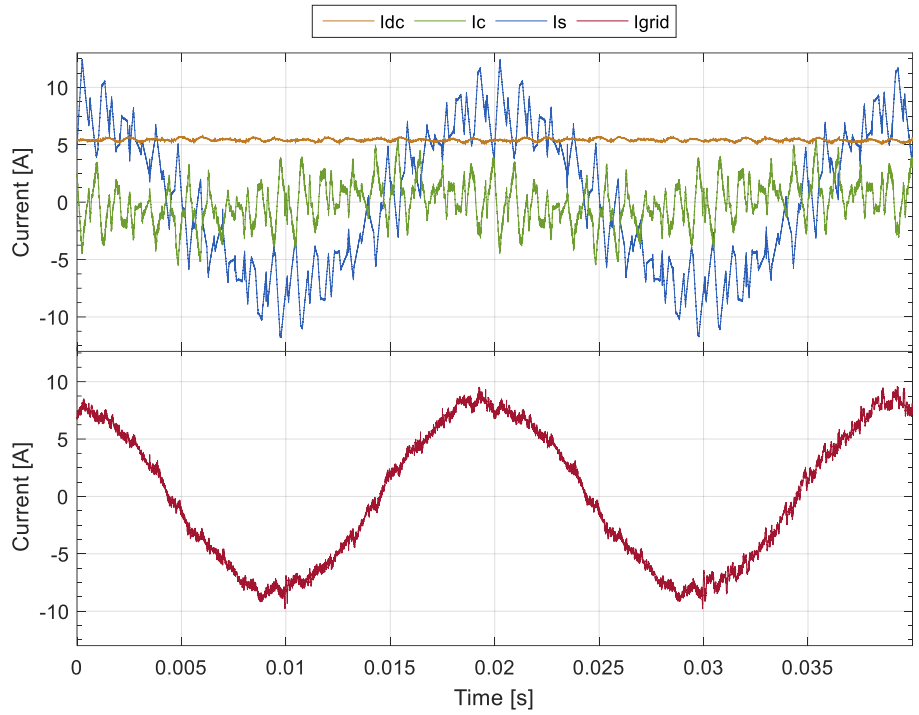


Fig 7-24: Experimental results showing steady state operation for Phase A currents during convergence of ripple cancelation by using a look-up table: a) CSI DC-link, series capacitor current and main VSI current; and b) grid current.

(a)

(b)

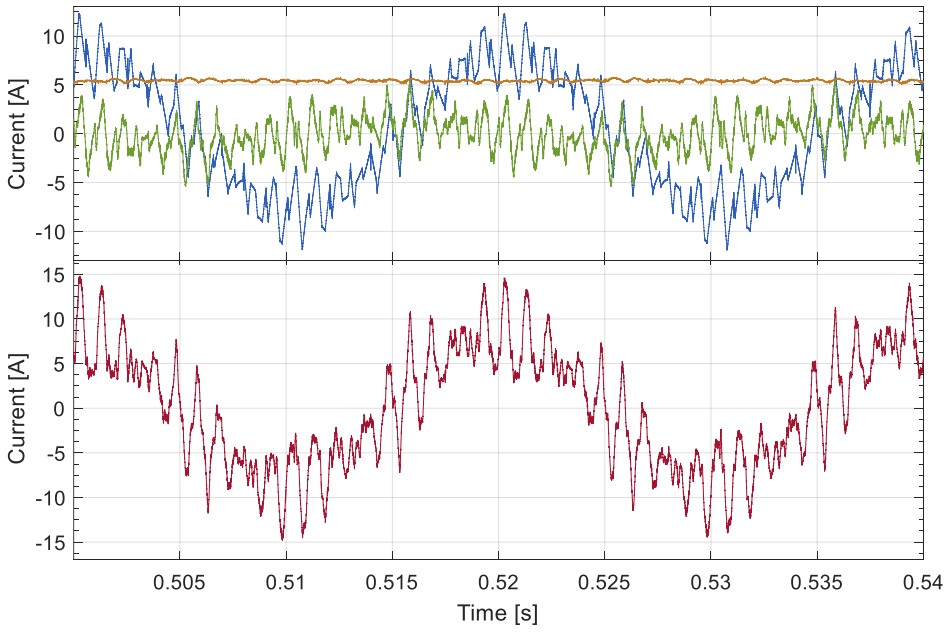


Fig 7-25: Experimental results showing steady state operation for Phase A currents without convergence of current ripple cancellation when using a look-up table : a) CSI DC-link, series capacitor current and main VSI current; and b) grid current.

Fig 7-26 shows the FFT corresponding for one cycle operation (Fig. 7-24) when the best ripple cancellation based on the look-up table is achieved. The 900Hz harmonic has been reduced from 1.576A (I_s) to 0.268A (16.5% of I_s), the 1.1 kHz harmonic has been reduced from 1.388A to 0.1418A (17%), while the 1950 and 2050Hz harmonics have been decreased from 0.8315 and 0.7596A to 0.113A (13.6%) and 67mA (8.8%). As expected, the low order VSI harmonics caused by nonlinear operation remain unchanged at 86mA (3rd harmonic), 261mA (5th harmonic) and 151mA (7th harmonic). It should however be questioned if it is desirable to permit this level of low order harmonics to be absorbed, unaffected, from the grid current or use the CSI V/I ratings to reduce them.

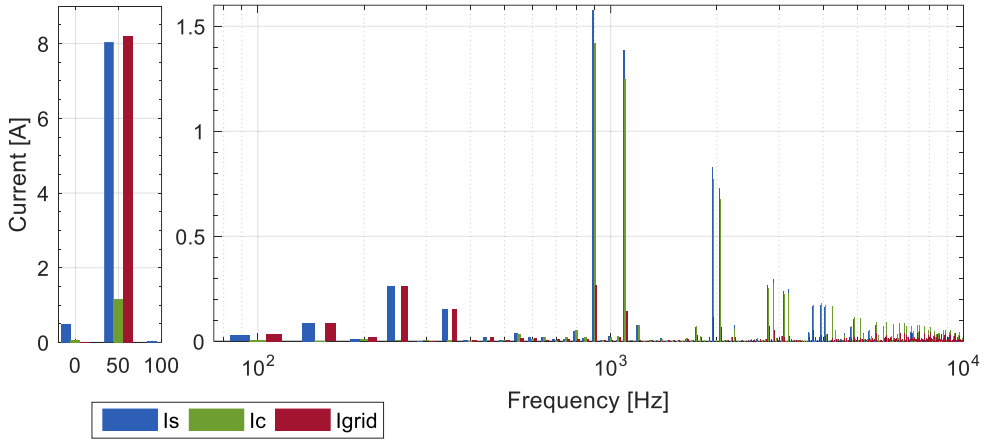


Fig 7-26: FFT of Phase A VSI current (I_s), CSI current (I_c) and grid current (I_{grid}) during full system operation when using look-up table for current ripple cancellation.

Most importantly, for this test the CSI DC-link current remains flat at the 5.5A reference value verifying that balanced operation can be achieved if the CSI current ripple reference waveforms remain free of any unbalance and low order harmonic components. A second conclusion following this test is that even though implementing the current ripple cancellation using an offline digital filtering method remains a theoretical possibility, the solution would need to account for a wide variability of possible operating points (e.g. grid frequency variation) which would result in a very complicated and impractical solution. As a result, the extraction of the

switching current ripple should be limited to real-time methods where different approaches can be used to deal with the unbalance and potentially the low order harmonics.

7.1.6.2. Negative Sequence Voltage Compensator

To minimise the unbalance effects on the fundamental frequency CSI voltage and current components, two different online approaches have been considered, yielding similar results. The first method is the rejection of any residual fundamental harmonic component by using a second filtering stage on the current ripple extraction output as shown in Fig 7-27. This is implemented using a Discrete Fourier Transformation (DFT) filter to extract any remaining fundamental frequency component from the current ripple reference waveforms [131]. For this solution, the current ripple is extracted online and no additional measurements are required thus having the advantage of maintaining open loop operation. A second advantage is that the method could be expanded by the addition of parallel DFT blocks tuned at specific harmonics to additionally remove any low order harmonics.

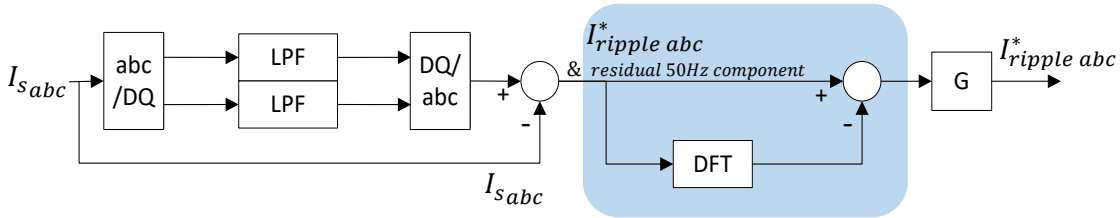


Fig 7-27: Method using second stage DFT-based filtering to remove residual fundamental components from the current ripple reference signals.

The second approach, which will be fully evaluated in the following section requires the use of voltage feedback from either the series capacitors C_s, or CSI output capacitors C_p. Under unbalanced operation, an inverse sequence voltage component, not present in the grid voltage appears and is mirrored between the series capacitors and CSI input voltages. Using the Double Decoupled Synchronous Reference Frame (DDSRF) method [132], any negative sequence

voltage component is extracted from the voltage measurement, appearing as DC quantities, which makes the removal straightforward via PI controllers (D/Q reference negative sequence voltage are considered to be zero in the implementation). The reference to the CSI modulator is the extracted current ripple as well as the combined positive and negative sequence fundamental current. This method has the advantage of also compensating for any unbalance due to external factors including an unbalance on the series capacitor values. As this method is only effective on the fundamental frequency, any low order harmonics extracted from the VSI currents will be synthesised by the CSI. The revised CSI control system is shown in Fig 7-28.

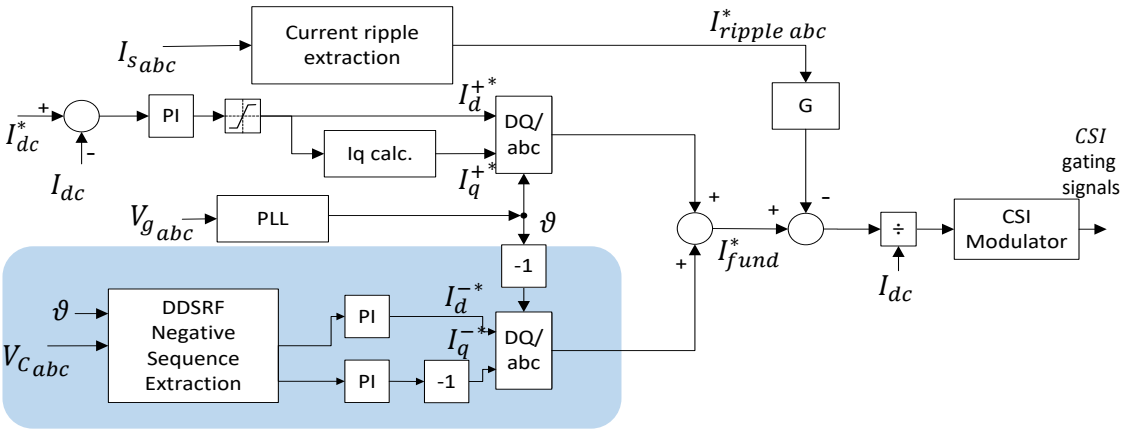


Fig 7-28: Revised CSI control system including negative sequence voltage compensator

7.1.7. Transient and Steady State Operation Results for Phase A

The grid connected performance using the negative sequence compensator is analysed in this section. The minimum value of voltage reduction coefficient K, to allow the DC-link current reference value to be set at 5A while avoiding the CSI dc link controller saturation, was found to be 0.12, corresponding to a fundamental voltage drop at the CSI inputs of 12% of the grid voltage. Other minor changes compared to previous experiments (§7.1.2) are the modification of the VSI modulating scheme to double edge carrier modulation combined with a corresponding decrease

of the moving average window to 0.5ms (2kHz) while the cut off frequency of the LPF, used for the current ripple extraction, has been set at 80Hz. These steps had no notable improvement on the overall system performance with the main noticeable alteration seen in the VSI harmonic profile around the 1 kHz sideband amplitudes which become asymmetrical in the case of double edge updating, as shown in simulations and §7.1.5 . The component values, which have remained unaltered, and operating parameters are summarised in Table 7-II.

Table 7-II: Component values and operating parameters for experimental topology

R_{dc}	C_{dc}	L_1	L_f	L_{dc}	R_f	R_{clamp}	R_{cs}	C_{clamp}	C_s	C_p
140Ω	550µF	11mH	300µH	30mH	50Ω	100kΩ	100kΩ	20µH	12µF	1µF
P	V_{dc}	V_{grid}	I_s	I_{dc}	K	I_{c_d} lim	I_c max	f_o	f_{sw}^{VSI}	f_{sw}^{CSI}
4.2kW	750V	415 V_{rms}	8Apk	5A	12%	153.5 mA	1.29A	50 Hz	1 kHz	40 kHz

Fig 7-29 shows the system start-up where PWM is activated at t= -10ms. The DC link voltage in Fig 7-29a rises from 537V to the 750V reference value within 8 cycles matching the experimental and simulated behaviour presented in previous experimental results. When PWM is activated, the maximum series capacitor voltage increases from 31V and to 328V (Fig 7-29b), with the negative peak recorded at -331V. The CSI voltage is decreased from 303V to 37V, at 11.3% of the grid voltage of 325V (negative peak at -322V). The CSI DC-link current, shown in Fig 7-29c, overshoots to 6.8A before settling at the reference 5A value at t=0.08s. The peak values of the converter side current I_s have been recorded at 12.35A and -12.67A, and at -12.7A and 12.5A on the grid current I_{grid}. It can be concluded that the transient behaviour during start-up remains the same with the use of the negative sequence voltage compensator.

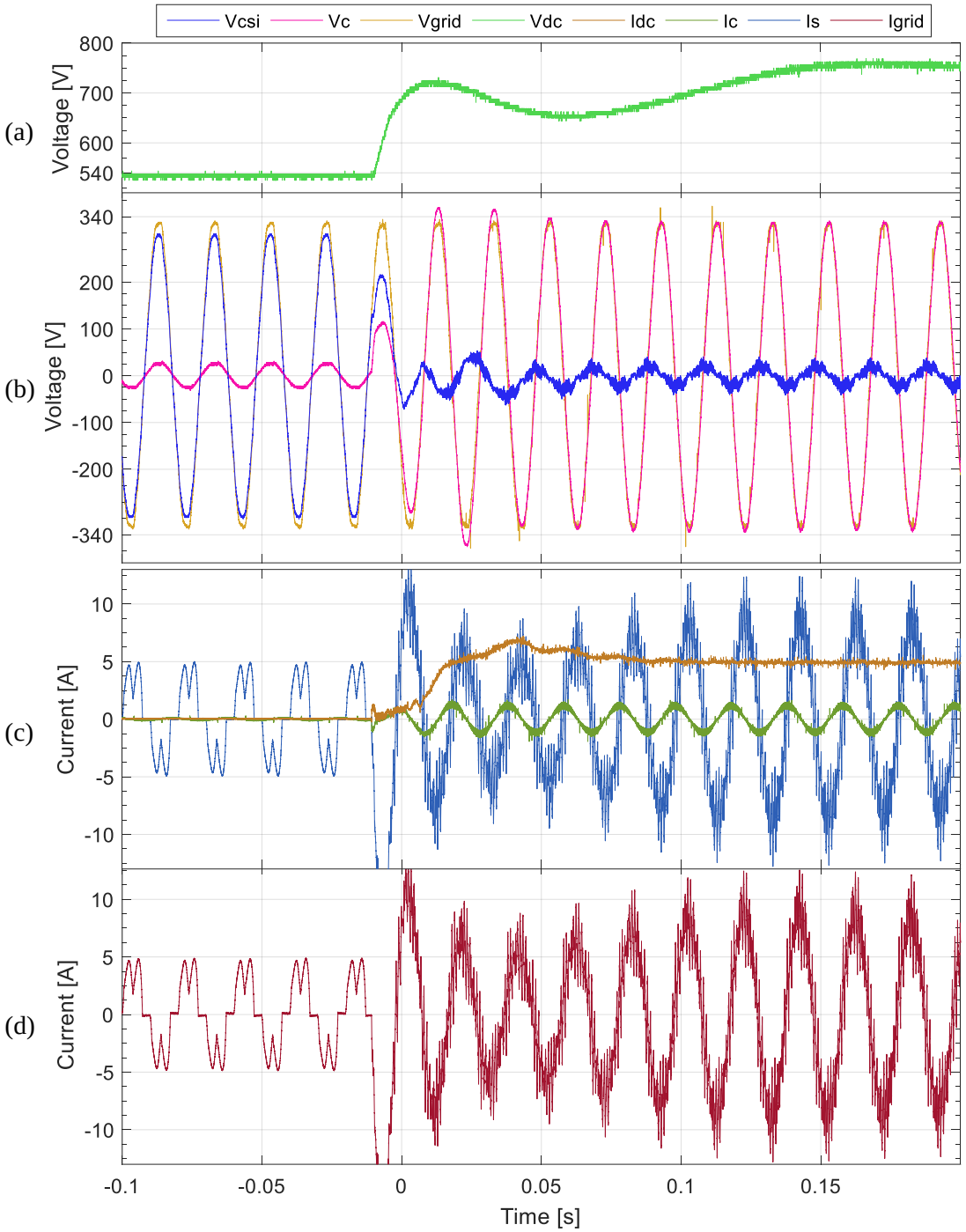


Fig 7-29: Experimental results showing PWM activation for VSI and CSI for K=0.12 (sans ripple cancellation) for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

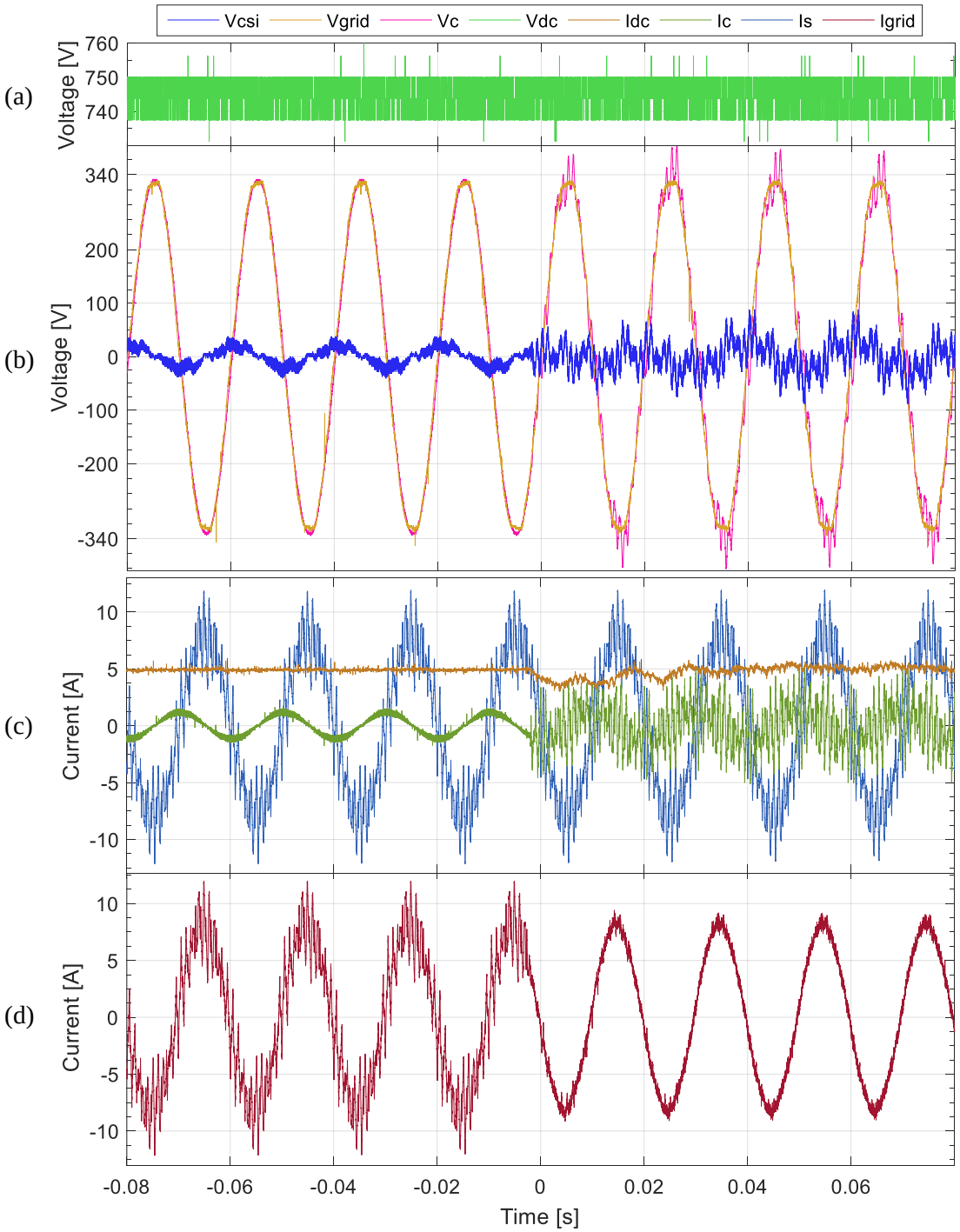


Fig 7-30: Experimental results showing activation of ripple cancellation for VSI and CSI for K=0.12 for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

Fig 7-30 shows the activation of current ripple cancellation, at t = -2ms. The additional ripple seen on the series capacitor voltage in Fig 7-30b, increase the peak voltage from 331V to 385V while the maximum CSI voltage is measured at 87.5V, up from 37.5V before harmonic cancellation. As observed previously, the VSI DC link voltage (Fig 7-30a) remains unaffected during this transient. The additional ripple produced by the CSI after ripple activation causes a dip in the CSI DC-link current (in Fig 7-30c) which is restored to the 5A reference value after approximately 40ms. The effect of the harmonic clean-up is evident on the grid current shown in Fig 7-30d with the peak value measured at 9A, down from 12.1A before cancellation. It should be noted that the series capacitor and CSI voltages are not in antiphase as observed in §7.1.2 and that the CSI DC link current does not contain the large oscillations seen previously, thus indicating balanced operation.

The waveforms over one cycle under steady state operation can be seen in Fig 7-31. The grid voltage peaks in Fig 7-31b, have been measured at 325V and -321V with V_c between -381V and 378V. The DC-link voltage (Fig 7-31a), measured at 743V, is slightly lower than the 750V reference which is possibly caused by a slight offset in the voltage measurement calibration. As observed in all previous experiments, the VSI current switching ripple is cancelled under full hybrid system operation with the majority of the remaining ripple seen on the grid current I_{grid} being at the CSI switching frequency (Fig 7-31d).

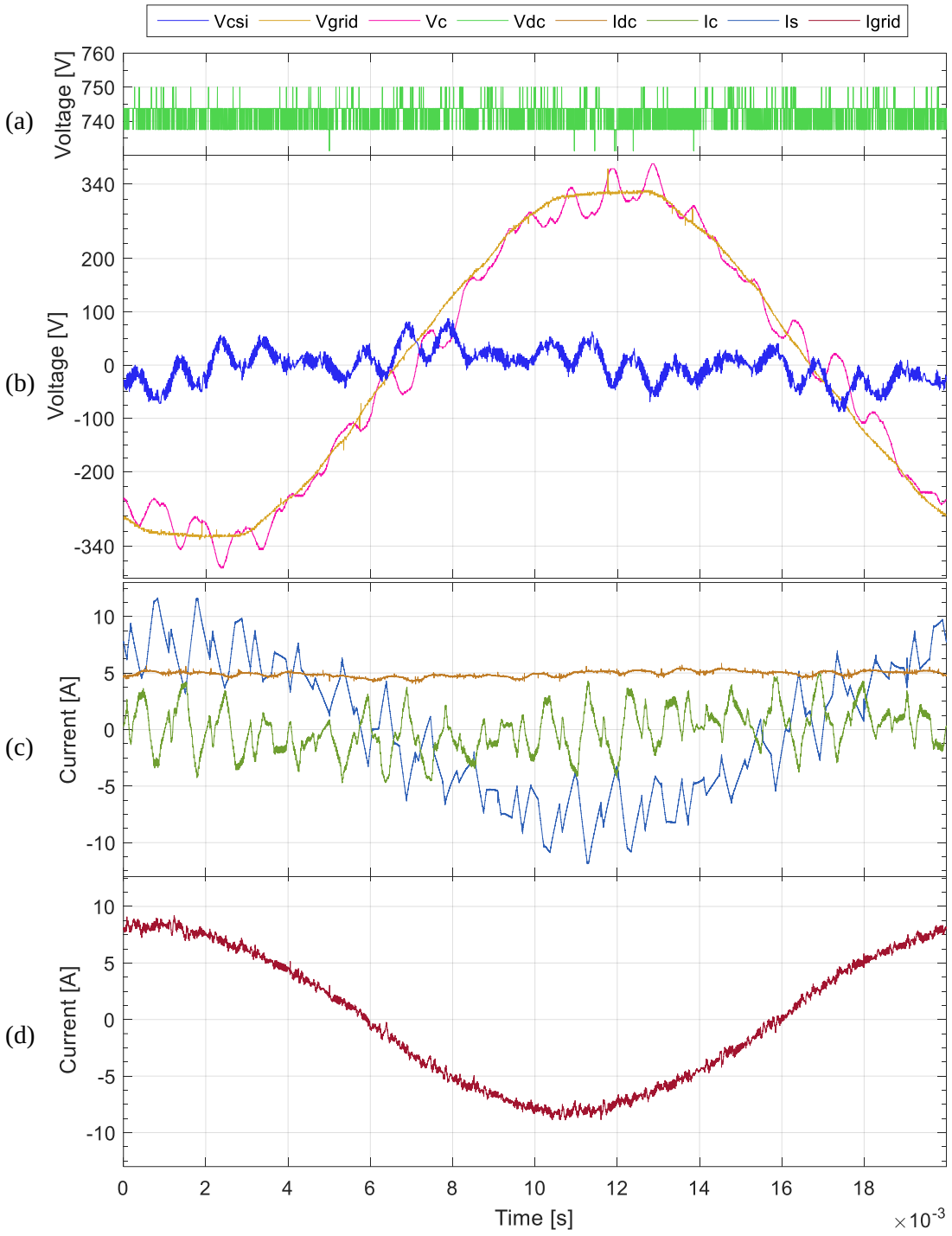


Fig 7-31: Experimental results showing one steady state cycle under full hybrid system operation for VSI and CSI for K=0.12 for Phase A: a) VSI DC-link voltage (V_{dc}) ;b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

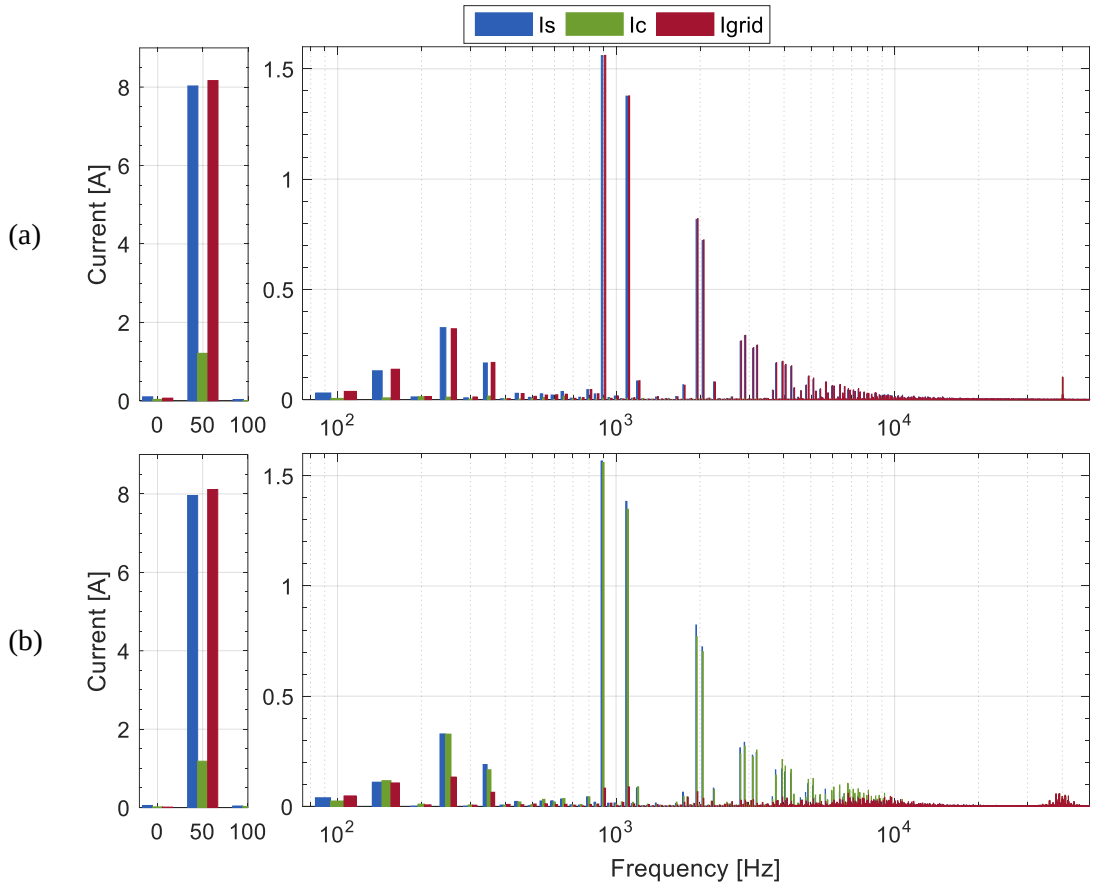


Fig 7-32: FFT (up to 50 kHz) of Phase A VSI current (I_s), CSI current (I_c) and grid current (I_{grid}): a) without ripple cancellation; and b) full system operation on a semi logarithmic scale.

The harmonic content of the currents before and after ripple cancellation is shown in Fig 7-32. Before harmonic cancellation (Fig 7-32a) the fundamental current component is measured at 8.03A for I_s, 1.21A for I_c and 8.17A for I_{grid}. The third order harmonic present in the converter and grid side currents is at 0.13A, with the 5th harmonic is measured at 0.326A and the 7th at 0.166A. Similar to previous experiments, the largest harmonic amplitudes in the VSI current are at 900Hz and 1.1 kHz with the amplitude measured at 1.57A and 1.376A.

Under full operation (Fig 7-32b), the harmonic amplitude at 900Hz is measured at 83mA (reduction down to 5.3%) and at 1.1 kHz at 89mA (6.5%). The harmonics at 1950Hz and 2050Hz are reduced from 0.82A and 0.72A to 66.5mA and 36.5mA, showing a reduction to 8% and 5% of the original VSI harmonic levels. The fundamental current components are measured at 7.96A for I_s, 1.18A for I_c and 8.11A for the grid side current. The CSI fundamental current is thus showing a 30mA change between the two modes of operation, which a smaller difference than

the 0.1A observed in §7.1.2 . Finally it can be seen that some harmonic cancellation also takes place for low order harmonics with the 5th harmonic reduced to 40% of the original amplitude from 329mA to 133mA, while the 7th harmonic is reduced from 190mA to 64mA (33%), which is beneficial for grid interaction. This is expected, since these low order harmonics are not deliberately removed from the CSI reference, as is the case with the inverse sequence. No cancellation is observed however on the 3rd harmonic current, despite a visible CSI harmonic, the grid current amplitude remained at 106mA. The amplitude of the harmonic cluster at the 40 kHz CSI switching frequency reaches 58mA.

The harmonic spectrum of relevant circuit voltages under each mode of operation is shown in Fig 7-33. When PWM is activated (Fig 7-33b), the fundamental voltages for V_{csi} and V_c change from 307V to 20.3V and 26.7V to 331V respectively. The grid voltage fundamental peak remains unchanged at 332V. The following DC components have been measured at 2.1V, 0.65V and 3.78V before activation, and at 1V, 1.5V and 4.4V after activation (Fig 7-33a) thus remaining negligible.

Before cancellation is activated, some low order voltage harmonics can be seen on the CSI voltage with the 5th and 7th harmonic at 2.57V and 3.2V. As only sinusoidal current is injected by CSI in the series capacitors to create a purely sinusoidal series capacitor voltage shape, when subtracted from the grid voltage (that contains 3rd, 5th and 7th at 3.9V, 3.8V and 3.7V), leaves all voltage harmonics present in the grid to appear across the CSI inputs.

When the system is under full hybrid operation, the low order harmonic content of the CSI and series capacitor voltages increases significantly due to the low order harmonic injection seen in Fig 7-32b. The 2nd harmonic remains at relatively low levels at approx. 3V for both V_c and V_{csi}. The 3rd harmonic is measured at 9.6V and 8.9V for V_{csi} and V_c, larger than the 3.7V amplitude in V_{grid}. More significantly, the 5th harmonic amplitude reaches 17V and 18.8V for V_{csi} and V_c compared to 4.8V for the grid while the 7th harmonic is measured at 4.9V, 6V and 3.4V for V_{csi}, V_c and V_{grid}. The additional voltage caused by these low order harmonics is the drawback of the CSI partially cancelling the low order current harmonics present in the VSI current.

The harmonics at 900Hz reach 20.3V for V_{csi} and 23V for V_c while at 1.1kHz the measurements are at 13.5V for V_{csi} and 16.5V for V_c with the difference that increases with the frequency, accounting for the voltage across the CSI filter L_fR_f.

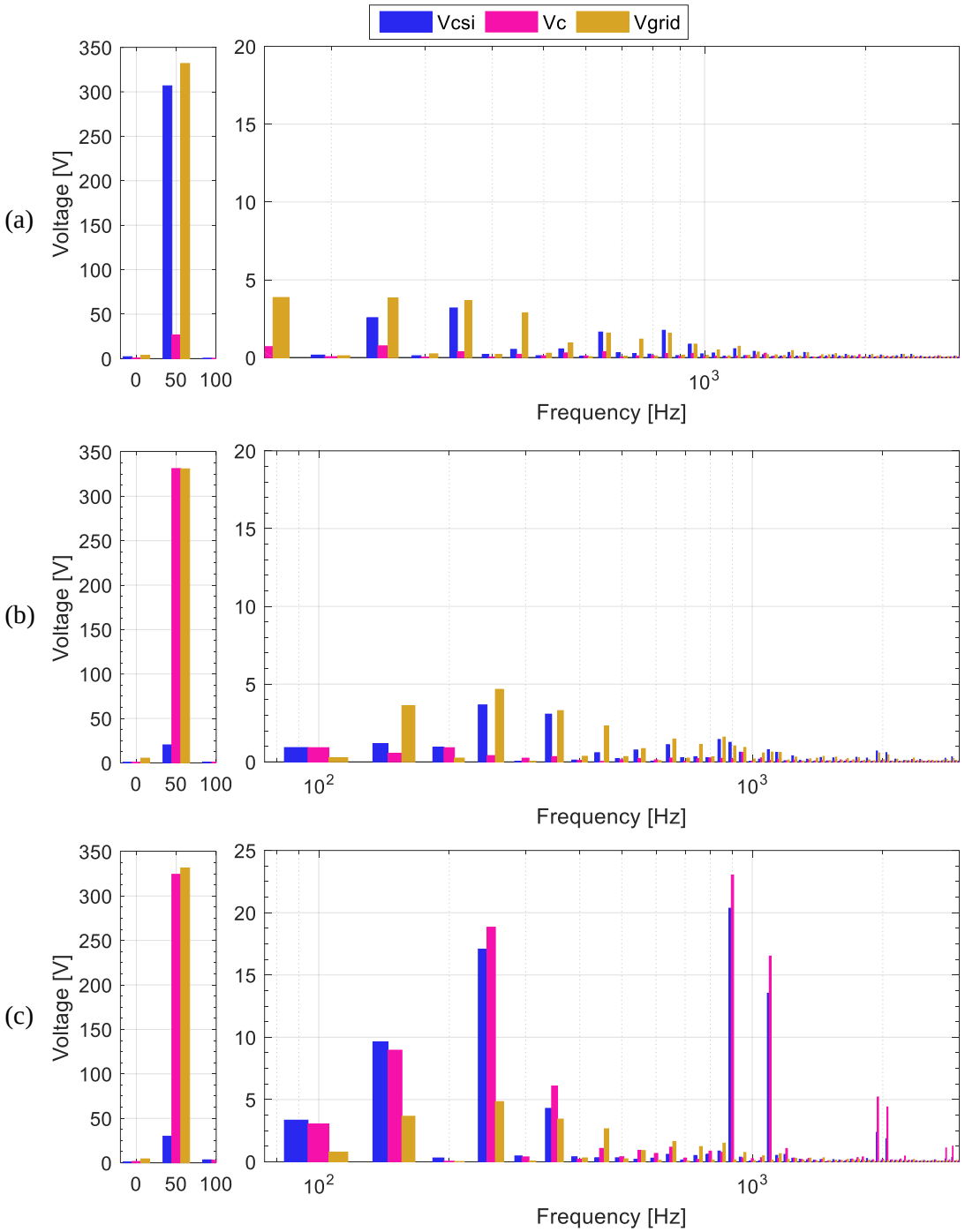


Fig 7-33: FFT of Phase A voltage of the Grid (V_g), Series capacitor (V_c) and CSI phase voltage (V_{csi}) during: a) No PWM; b) PWM enabled showing fundamental voltage reduction; and c) full system operation (harmonic cancellation).

7.1.8. Maximum Voltage Stress and Phase Symmetry

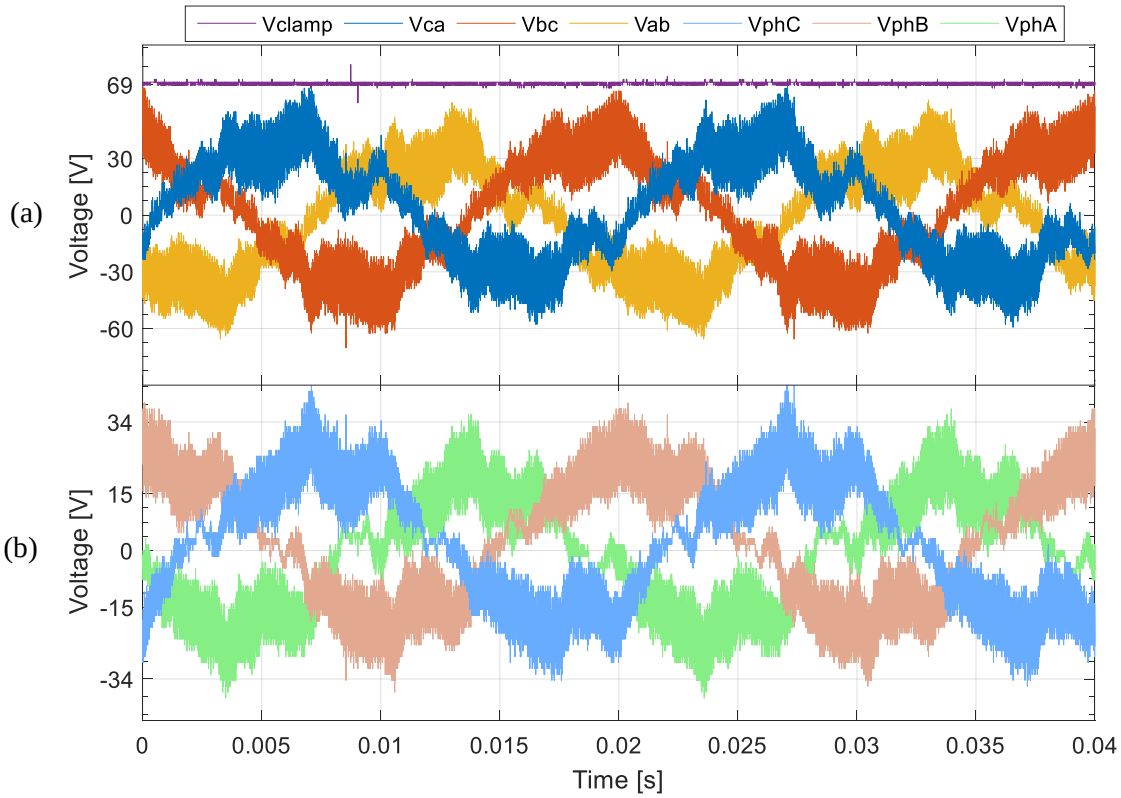


Fig 7-34: The CSI input voltages showing the fundamental voltage reduction in: a) the three phase line-line CSI voltages and the clamp voltage and b) the three phase-neutral CSI voltages.

The three phase-neutral and line-line CSI voltages are shown in Fig 7-34 during fundamental current injection. Although some DC component is visible, the three voltages seem fairly balanced, with the typical trapezoidal and triangular shape observed on the phase and line-line voltages due to the distorted grid voltage as seen previously in Fig 7-10. The majority of the phase voltage peaks in Fig 7-34b remain under 34V. The maximum voltage stress measured on the DC clamp voltage is recorded at 69V, closely matching the 12% voltage drop coefficient K.

The use of the negative sequence compensator has no visible effect before current ripple cancellation. This is verified in Fig 7-35 that shows the corresponding frequency content of the above waveforms. The fundamental component of the CSI phase voltages is measured at 19.6V, 21.7V and 21.8V for phases A-B-C with the maximum deviation at 2.2V while the CSI line-line

voltage peaks reach 35.4V, 35V and 38.8V for V_{ab}, V_{ca} and V_{bc}. The DC component is measured at 1V, 2.85V and 4.6V on the phase voltages with the corresponding line-line voltage at 5.6V, 3.8V and 1.7V.

The most significant harmonic amplitudes are the 5th and 7th harmonic with the amplitude for the 5th measured at 3.3V, 2.7V and 2.5V for phase A-B-C CSI phase voltages and 5.1V, 5. 6V and 4V for V_{ab} V_{ca} and V_{bc} CSI line voltages. The 7th harmonic is measured at amplitudes of 3.9V, 5.2V and 4.2V on the line-line CSI voltage. Finally the switching harmonic cluster at 40 kHz reaches peaks of 4.5V phase and approx. 8V for the line voltages.

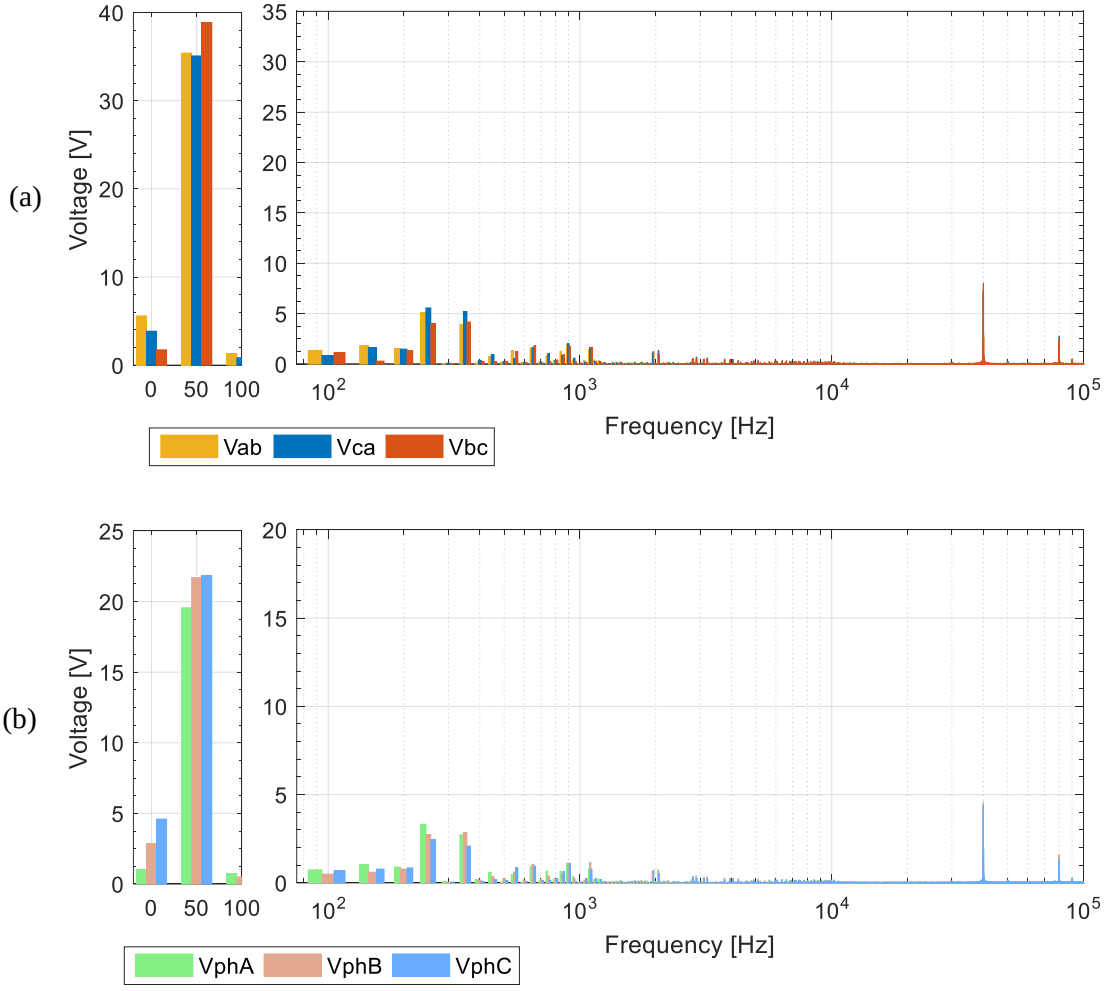


Fig 7-35: FFT of the CSI input voltages under fundamental voltage reduction mode showing the harmonics in: a) the three phase line-line CSI voltages and b) the three phase-neutral CSI voltages.

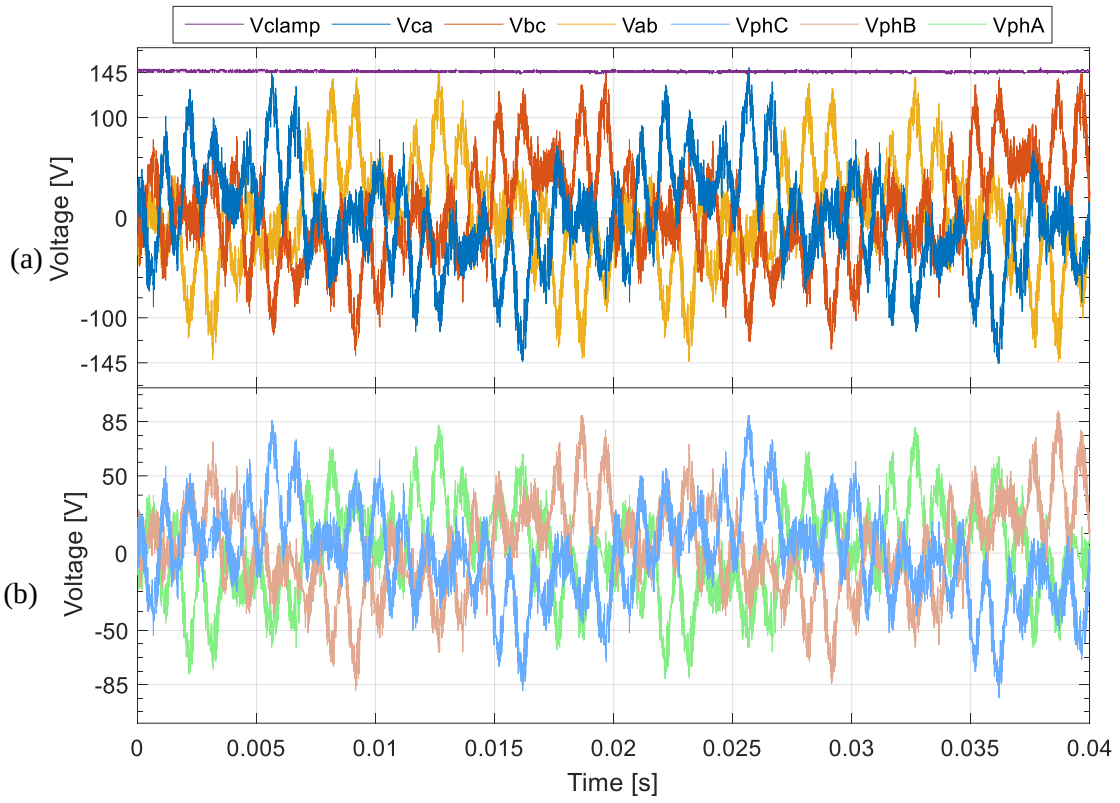


Fig 7-36: The CSI input voltages under full system steady state operation showing: a) the three phase line-line CSI voltages and the clamp voltage and b) the three phase-neutral CSI voltages.

The three phase voltages under full system operation are shown in Fig 7-36. The peak phase-neutral voltage in Fig 7-36b reaches 90V whilst for the majority of the cycle duration the waveforms remain under 85V. The maximum voltage stress, measured on the DC clamp voltage shown in Fig 7-36a is recorded at 145V, which is around 25% of the peak grid line-line voltage. The voltage waveforms do not exhibit the unbalanced behaviour at the same extent observed previously in §7.1.3 thus confirming the effectiveness of the negative sequence voltage compensator. This can be verified by the FFT of these voltages, showing the corresponding harmonic content in Fig 7-37. The fundamental phase-neutral A-B-C voltage amplitudes reach 25.5V, 30V and 27.4V with the line-line voltage amplitude are measured at 43.5V, 48.6V and 51.4V showing a maximum difference of 8V. The DC component reaches 1.5V, 3.5V and 8V on the phase voltage measurement with a corresponding value of 7V, 5V and 12V seen on the CSI line-line voltages.

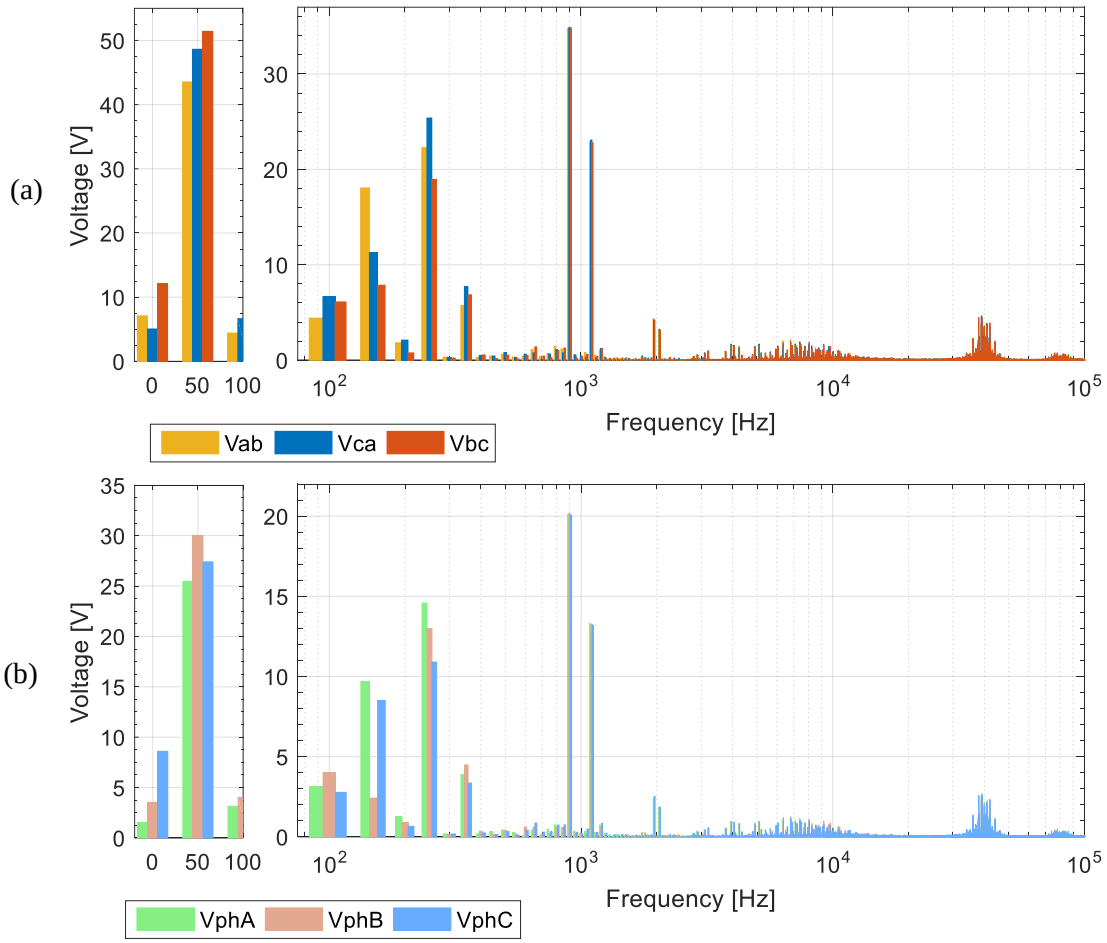


Fig 7-37: FFT of the CSI input voltages under full system steady state operation showing the harmonics in: a) the three CSI line-line voltages and b) the three phase-neutral CSI voltages.

The highest CSI voltage harmonic is at 900Hz, caused by the VSI switching ripple, reaching 20.1V on the CSI phase voltages and 34.9V on the CSI line-line harmonics whilst the 1.1 kHz harmonic amplitudes reach 13.2V (phase) and 23V (line).

The low order harmonic spectrum is significantly polluted. The second harmonic amplitude reaches 4.4V, 6.7V and 6.1V for V_{ab}, V_{ca} and V_{bc} (3.1V, 4.2V and 8V on the phase voltages). The 3rd harmonic reaches higher levels of 9.7V, 2.4V and 8.5V on the A-B-C phase voltages and 18V 11.3V and 7.85V on the CSI line-line voltages. The most significant low order voltage harmonic is the 5th harmonic at 14.6V, 13V and 11V on the phase voltages, with the line-line amplitudes reaching 22.3V, 25.4V, 18.95V. Finally the 7th harmonic is also visible at 3.9V, 4.5V and 3.35V phase and 5.7V, 7.7V, 6.9V line.

As mentioned previously, permitting the CSI to partially cancel any low order current harmonics will create additional low order voltage harmonics across the series capacitor which are mirrored as additional voltage stress on the CSI inputs. The increased voltage stress created by removing the low order current harmonics will add to the CSI installed power and corresponding cost but will offer benefits in the improvement of the grid current quality which is the primary aim of the CSI operation. It would also be possible to design the series capacitance to account for an added low order harmonic voltage stress limit, based on setting a permissible level of low order current harmonic amplitudes to be cancelled. Therefore, an increase in the series capacitance will create smaller voltage harmonic across the CSI for a given harmonic current injected (low order of VSI ripple) but also for the fundamental component.

An aspect which can make this design slightly more challenging is the unbalance in the amplitudes of the low order VSI current harmonics (Fig 7-20). This is a consequence of the harmonic difference seen between the grid voltages (Fig 7-2) and the interaction with the VSI control. The cancellation of these harmonics will create unbalanced voltage harmonic amplitudes across the CSI phase-neutral input voltages which in turn will create unbalanced amplitudes of line-line voltage harmonics that contribute to further increase of the CSI voltage stress. As a result, predicting the exact impact of the low order current harmonic cancellation on the CSI voltage stress can be difficult. A considerable margin in the calculation would be essential to ensure the safety of the semiconductor devices when operating with an unpredictable level of low order harmonics.

7.1.9. Conclusion

The hybrid topology has been tested with a real grid supply voltage, therefore evaluating the operation under non-ideal grid conditions. The grid voltage shape reveals significant distortion with the presence of zero sequence component and low order grid voltage harmonics. Operation under this conditions is proven to significantly impair the voltage reduction capability of the CSI, as a consequence of the control system initially developed under ideal grid conditions. When only

synthesizing a fundamental current reference as used in the voltage reduction mode, the direct effect of the grid voltage unbalance is visible on the CSI voltages however not at significant levels.

The cause is that the main VSI converter operating under the given grid conditions produces a slight asymmetry in the fundamental current components as well as low order harmonic current components. The current ripple extraction method, initially developed for the ideal grid conditions and working in the dq synchronous reference frame, resulted in the fundamental current component asymmetry and the low order harmonics in the abc VSI currents to propagate into the reference signal fed to the CSI modulator leading to a significant series capacitor and CSI voltage unbalance.

The proposed solution for restoring the voltages to balanced operation requires the measurement of the series capacitor voltage unbalance which is subsequently mitigated using a negative sequence compensator integrated in the CSI control. The voltage drop coefficient K has been increased to 12%, (compared to 10% considering an ideal grid scenario CHAPTER 6), the minimum value found to avoid CSI current controller saturation with the maximum CSI voltage stress at full operation reaching 25% of the grid voltage.

The increased voltage stress also accounts for the additional low order harmonic voltages created across the series capacitors due to the CSI also partially compensating for the low order current harmonics created by the VSI due to the non-ideal grid conditions.

Although the initial aim of this experiment has been to demonstrate the effect of grid impedance to the harmonic cancellation performance of the CSI, no such effects have been noticed in this circuit configuration.

7.2. Grid Connected Rectifier with Additional Higher Order Impedance in the AC Filter

The final and most challenging experimental configuration has been set up to test the effects of added grid impedance and to report on the influence of potential resonances that may appear as a result of the larger grid inductance and may affect the hybrid system performance. Although the resonant effects expected from the theoretical analysis in CHAPTER 4 are studied in this experiment, the evaluation of the active damping compensator has not been implemented given the lack of computational power that remained available in the DSP and of the additional issues encountered with grid unbalance that required additional development time.

7.2.1. Experimental Setup

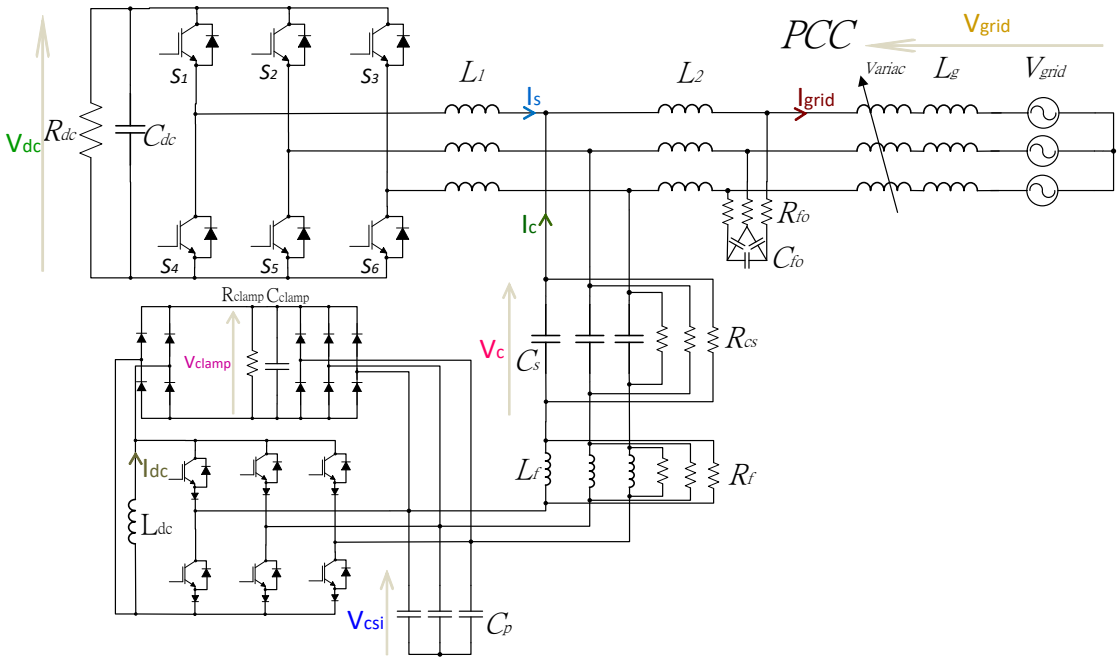


Fig 7-38: Circuit topology of the experimental setup connected to the grid via additional LC impedance.

The circuit set-up presented in Fig. 7-37 has been configured to emulate the topology presented in §4.5.1 where an additional LC impedance has been added between the series capacitor connection and the PCC to the grid. This was done to emulate the Hybrid system implementation where the CSI is connected to VSI using an LCL filter. The Capacitor C_{fo} is used to remove any CSI switching frequency noise from the grid voltage. In this configuration however, the existing

CSI AC filter inductance (L_fR_f) has been kept in place. The open-loop control approach for the current ripple cancellation has been left unchanged, unlike CHAPTER 4 where the active damping compensator (§4.3.2) had been used.

The connection to the grid has been done via an autotransformer (Variac) with the voltage set at 100% of grid voltage similar to §7.1.1. Other than the addition of the grid side filter (L_2, C_{fo} and R_{fo}) the circuit has been kept identical to the configuration investigated previously in chapter 7. The component values and operating parameters are shown in Table 7-III, including the values of the added AC filter components. Similar to the previous grid connected evaluation, the DC link current reference for the CSI has been set to 5A, with the voltage reduction coefficient K set at 12%. Due to the grid imbalance effects, the evaluation of circuit operation has been done using the proposed negative sequence voltage compensator presented in §7.1.6.2 .

Table 7-III: Component values and operating parameters for experimental topology

R_{dc}	C_{dc}	L_1	L_2	L_f	L_{dc}	R_f	R_{clamp} & R_{cs}	C_{clamp}	C_s	C_p	C_{fo}
140Ω	550µF	11mH	280µH	300µH	30mH	50Ω	100kΩ	20µH	12µF	1µF	180nF
P	V_{dc}	V_{grid}	I_s	I_{dc}	K	$I_{c\_d\,lim}$	$I_{c\,max}$	f_o	f_{sw}^{VSI}	f_{sw}^{CSI}	R_{fo}
4.2kW	750V	415 V_{rms}	8Apk	5A	12%	153.5 mA	1.29 A	50 Hz	1 kHz	40 kHz	33 Ω

An initial estimation the grid impedance has been performed with the Fluke 1652C Multifunction Installation Tester that measured approx. 0.5Ω impedance for all three phases with the real term of the impedance measured at 0.1Ω. By assuming the grid is solely inductive, this would result in in having a grid inductance of 1.3mH, which would create a resonance at approximately 3.4 kHz.

Based on the resonant frequency observed experimentally, which was found to be at about 6.4 kHz, the estimated grid inductance, including the Variac inductance set at 100% voltage is deduced to be only around 160µH. Nevertheless the resonance observed is sufficiently big in terms of resonance to investigate its effects on the CSI performance, which is fully assessed in the following section.

7.2.2. Transient and Steady State Operation Results for Phase A

The activation of PWM for both converters is shown in Fig 7-39 for Phase A voltages and currents. Due to the CSI DC link controller saturation, the fundamental voltage drop coefficient K has been set to 12% for a DC-link current reference of 5A, as mentioned in §7.1.7. After PWM is activated at t=-10ms, the series capacitor voltage (Fig 7-39b) increases from 25V to 325V while the CSI voltage decreases from 306V to 56V, higher than previous experiments. The VSI DC-link voltage (Fig 7-39a) increases from 537V to the reference value of 750V after a transient period of 10 cycles, matching the behaviour observed under previous grid interconnection scenarios. The same can be observed from the initial overshoot period seen on the grid and VSI currents as well as the CSI DC-link current (Fig 7-39c-d) which overshoots to 7.3A before reaching the reference value of 5A within 0.1 seconds.

Fig 7-40 shows the activation of ripple cancellation at t=0s. The peak current ripple on the grid current (Fig 7-40d) is reduced from 12.3A to 8.8A. The DC link current dips to about 3A before increasing to the reference value at t=0.04s. The initialisation of harmonic cancelation is clearly visible by the additional voltage ripple produced on the series capacitor voltage which is mirrored across the CSI voltage (Fig 7-40b) while the VSI DC link voltage (Fig 7-40a) remains unaffected. The series capacitor voltage peak increases from 330V to 380V while a low order harmonic component is slightly visible by the non-sinusoidal waveform shape with the negative peak recorded at -400V. The CSI phase voltage increases from 56V before ripple cancelation was activated to 80V with the negative peak recorded at -90V.

The effect of the resonance can be observed on the CSI voltage as well as CSI current waveforms where a larger ripple content can be observed very clearly before the current ripple cancellation is activated, as well as after. The steady state waveforms before ripple cancelation was activated are shown for one cycle in Fig 7-41 with only fundamental current production and in Fig 7-42 for full system operation. It can be observed that the ripple present in the CSI current before cancellation (Fig 7-41c), as well as the resultant ripple on the grid current after cancellation (Fig 7-42d), is not at the 40 kHz switching frequency but instead appears to oscillate at a lower

frequency. A side by side comparison of the results for phase A with and without resonance is given in Appendix H.

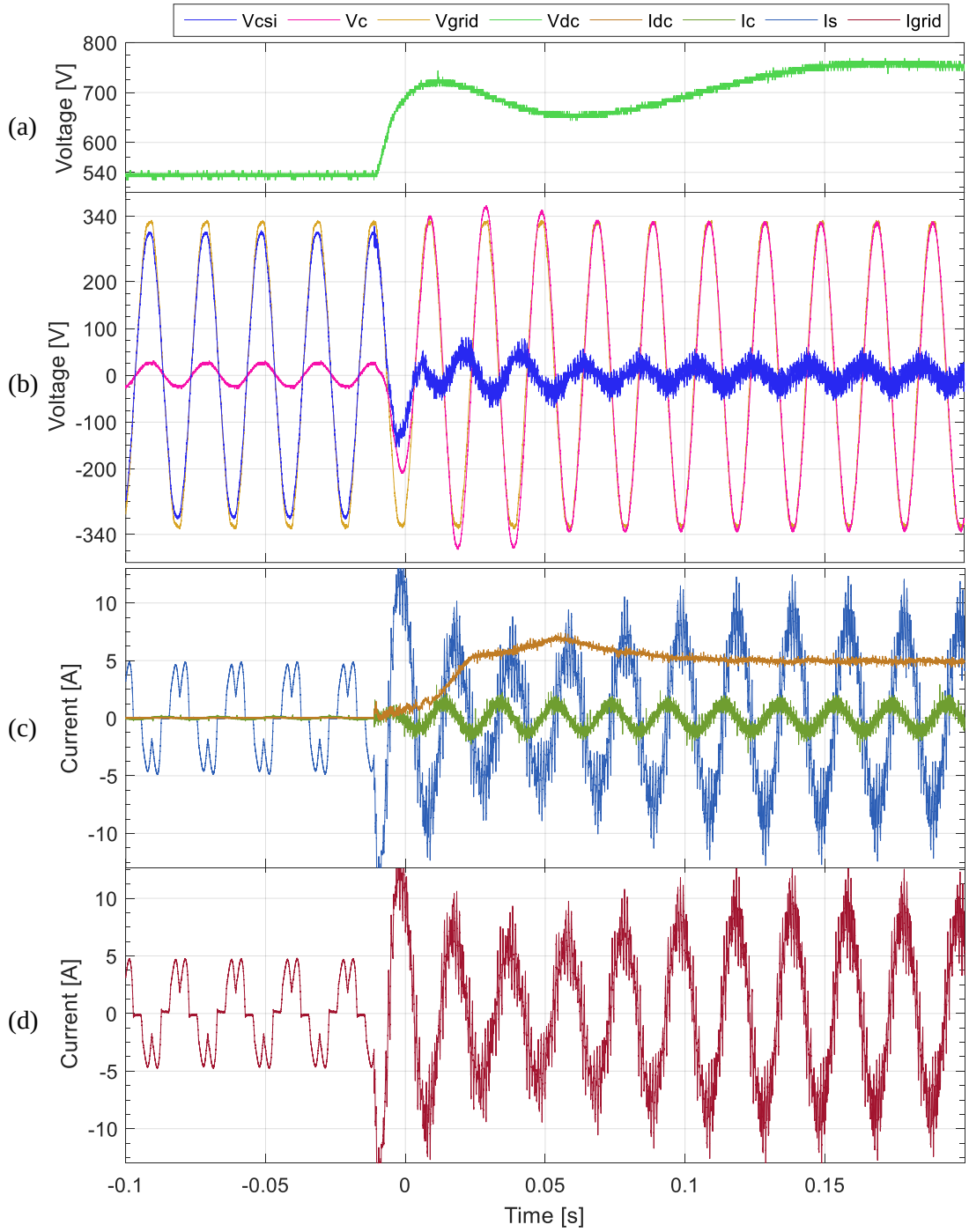


Fig 7-39: Experimental results showing PWM activation for VSI and CSI for K=0.12 (sans ripple cancellation) for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

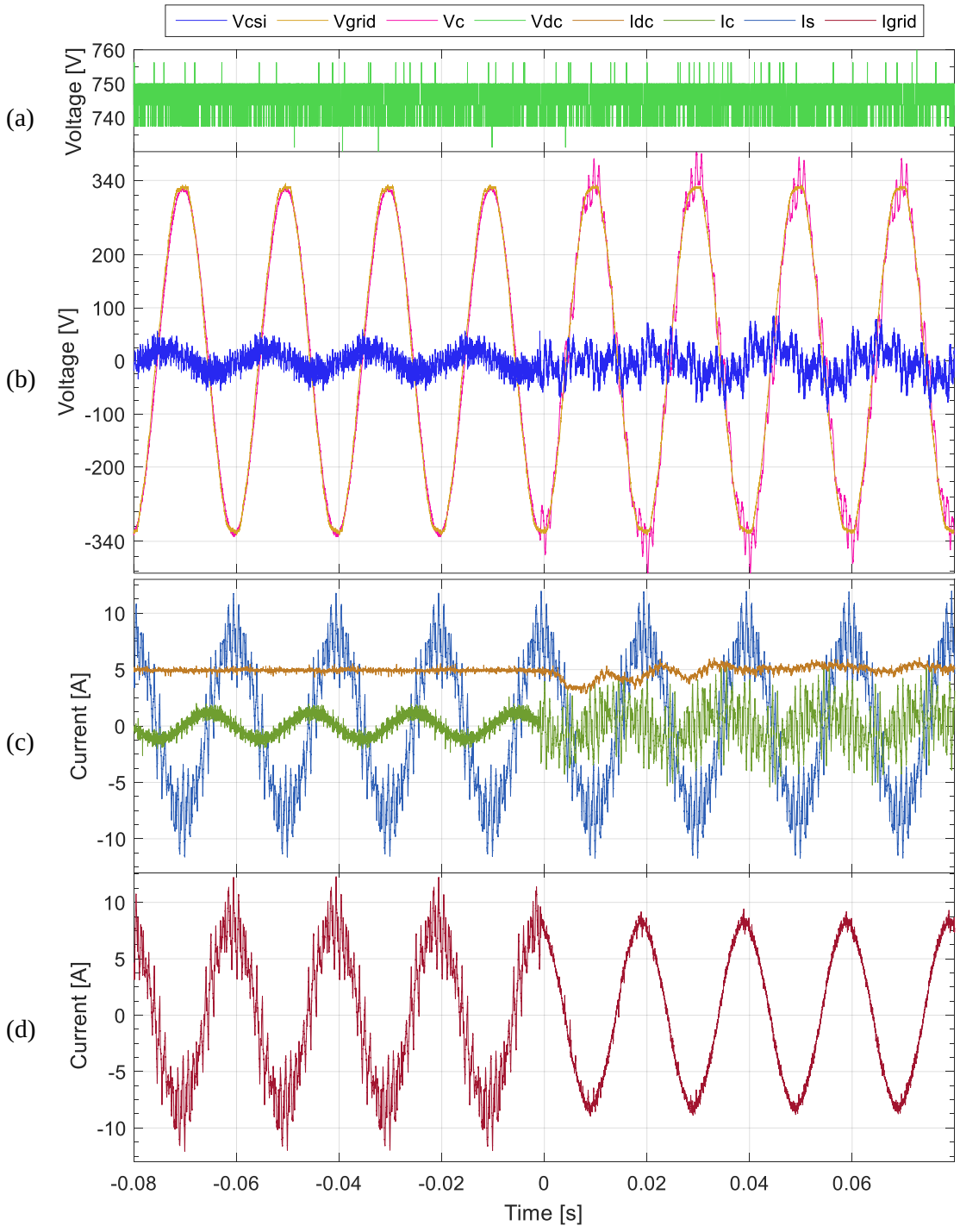


Fig 7-40: Experimental results showing activation of ripple cancellation for VSI and CSI for K=0.12 for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

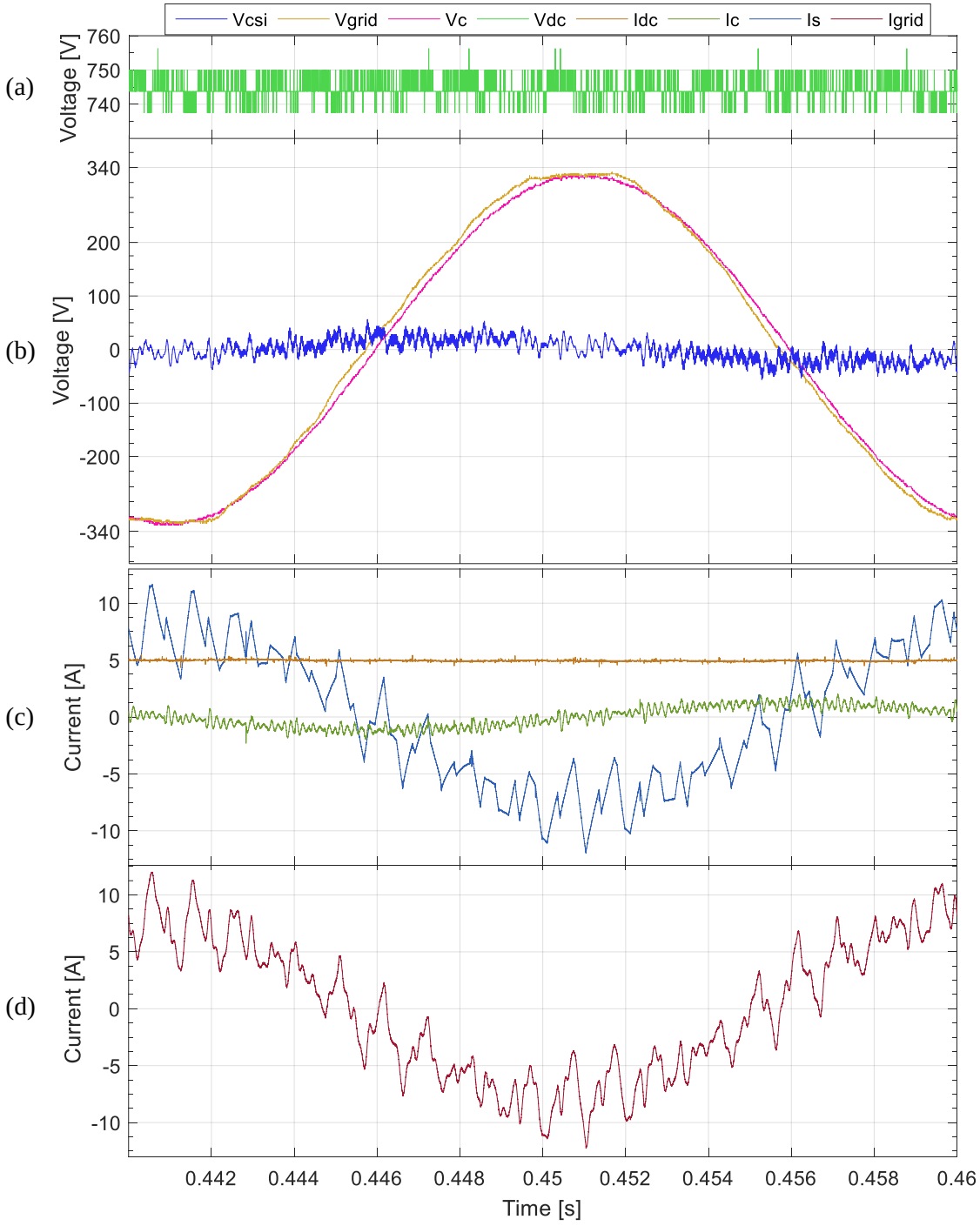


Fig 7-41: Experimental results showing one steady state cycle before ripple cancellation for VSI and CSI for K=0.12 for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

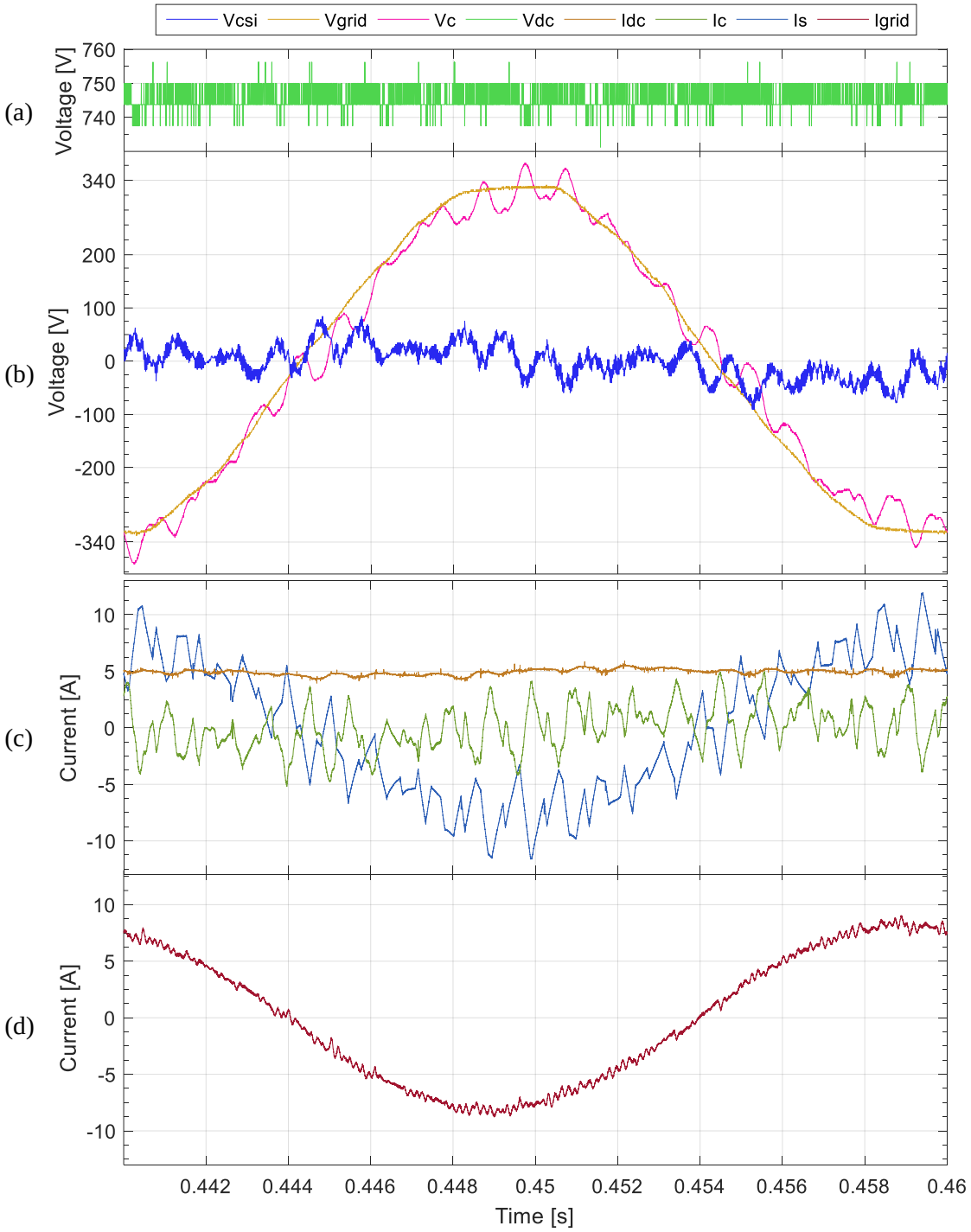


Fig 7-42: Experimental results showing one steady state cycle under full hybrid system operation for VSI and CSI for K=0.12 for Phase A: a) VSI DC-link voltage (V_{dc}); b) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; c) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and d) combined grid side current (I_{grid}).

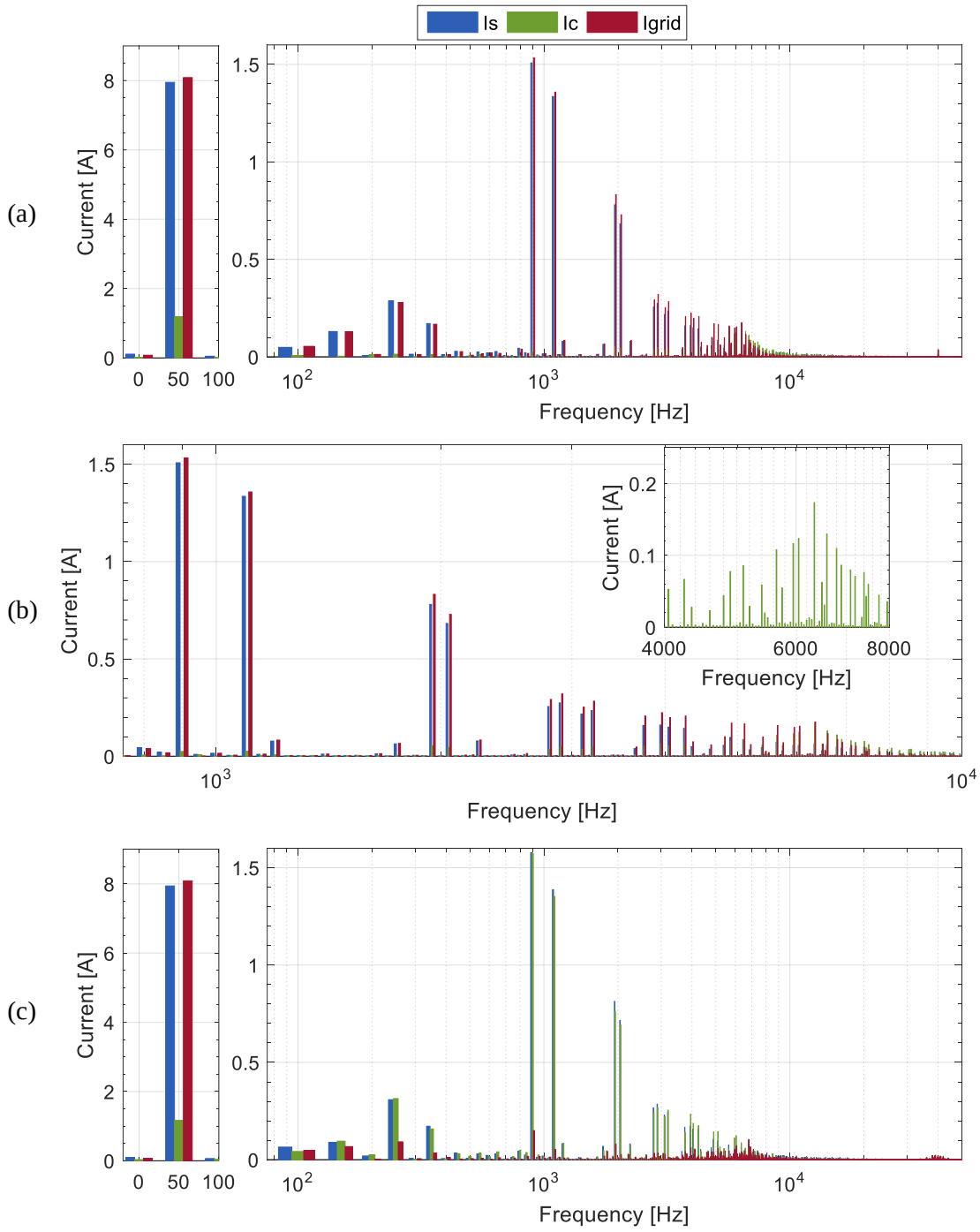


Fig 7-43: FFT of Phase A VSI current (I_s), CSI current (I_c) and grid current (I_{grid}): a) before ripple cancellation up to 50 kHz; b) zoom in between 700Hz and 10kHz before cancellation; and c) full system operation on a semi logarithmic scale.

The resonance seen in the Phase A currents can be investigated further in the frequency domain. The harmonic content of the current waveforms before current ripple cancellation is enabled and during full hybrid operation are presented in Fig 7-43.

Before ripple cancellation (Fig 7-43a), the fundamental component amplitude is measured at 7.95A for I_s, 1.19A for I_c and 8.087A for the grid side current Ig. The harmonic excitation caused by the resonance is more apparent in Fig 7-43b by the amplification of harmonic amplitudes when comparing the grid side current to VSI current harmonics above 700Hz. The 900Hz harmonic amplitude is slightly increased from 1.507 to 1.53A, the 1.1 kHz component is increased from 1.335A to 1.357A, the 1950Hz from 0.78A to 0.83A and the 2050Hz harmonic is increased from 0.68 to 0.72A. The level of amplification for higher order harmonics can be seen clearly by observing the excitation on the CSI current from 4-8 kHz (zoom-in subplot in Fig 7-43b) showing a resonant effect close to 6.4 kHz although the amplification of individual harmonics on the grid side current is small when regarded as an absolute level. The largest harmonic that is generated by the resonance, measured at 6350Hz reaches 0.17A.

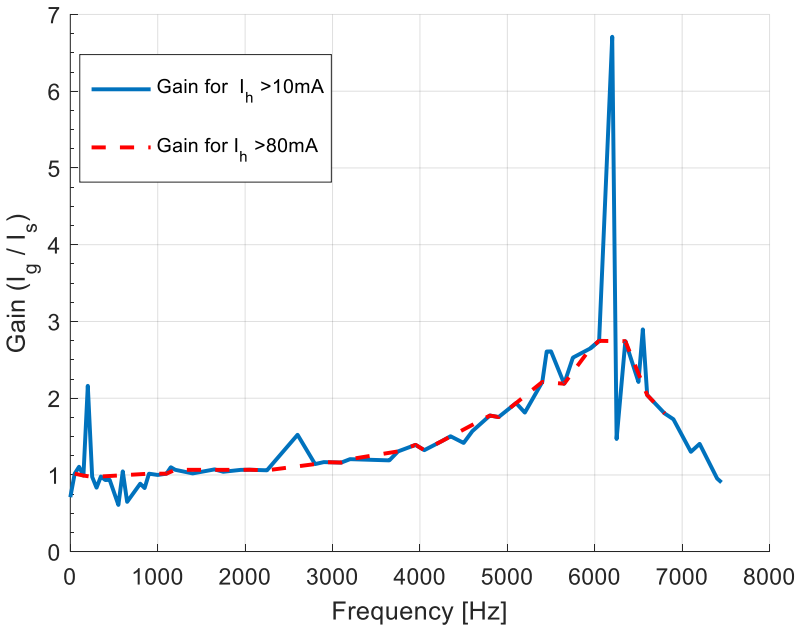


Fig 7-44: Reconstructed bode plot showing the main VSI current to grid current gain considering main VSI current harmonics above 10 mA (blue) and 80 mA (red)

To clearly observe the resonant characteristic of the circuit, the current gain (Fig 7-44) has been reconstructed by comparing the harmonic amplitude of grid current harmonics to VSI current harmonics. Two curves are shown, one considering VSI current I_s harmonics above 10mA, shown by the blue curve, whilst the superimposed red dashed line considers only harmonics above 80 mA, a level chosen as approximately 1% of the fundamental to remove artificial peaks created by noise. The maximum gain at the resonant frequency of 6.3 kHz has been measured at 2.75 (8.8 dB) for the more significant current harmonics recorded and 6.7 (16.5 dB) that correspond for the low level of harmonics recorded

The resonance however does not seem to have a detrimental effect on the CSI active filtering capabilities (Fig 7-43c), although some loss of attenuation can be observed compared to previous experiments (§7.1.7). The 900Hz harmonic reduction to 9.5% (from 1.578A in I_s to 149.8mA in I_{grid}) means that the residual harmonic has almost doubled compared to the result without resonance (5.3%). On the other hand, the residual 1.1 kHz harmonic which is reduced to 3.8% (1.387A to 52mA) is smaller when comparing to the same residual harmonic in §7.1.7 (6.5%). In the harmonic cluster at twice the VSI switching frequency, the 1950Hz harmonic is reduced to 9.8% (0.81A in I_s to 80mA in I_{grid}) and the 2050Hz harmonic is reduced down to 3.6% of the VSI level (0.715A to 26mA). Without resonance the corresponding reduction in §7.1.7 was 8% and 5% thus also showing a slight difference. Under full system operation the fundamental current harmonic amplitudes are measured at 7.94A for the VSI current I_s, 1.167A for I_c and 8.088A for the cumulated grid side current I_{grid}.

The low order harmonics present in the grid current I_{grid} in do not show any sign of resonant excitation compared to the amplitudes in the VSI current I_s. Under full operation, the third harmonic present in the VSI current is reduced to 76% of the original amplitude from 89mA to 68mA as seen in the grid current, the 5^{th} harmonic is reduced to 30%, from 0.3A to 92mA while the 7^{th} harmonic is reduced to 20% from 0.17A to 34mA.

The switching harmonic cluster at 40 kHz is significantly reduced compared to previous experiments with the most significant peak reaching 22mA compared to 58-60mA in §7.1.2 and

§7.1.7 . This is a direct effect of having an additional inductance present to the grid side which provides the associated additional attenuation at the 40 kHz CSI switching frequency.

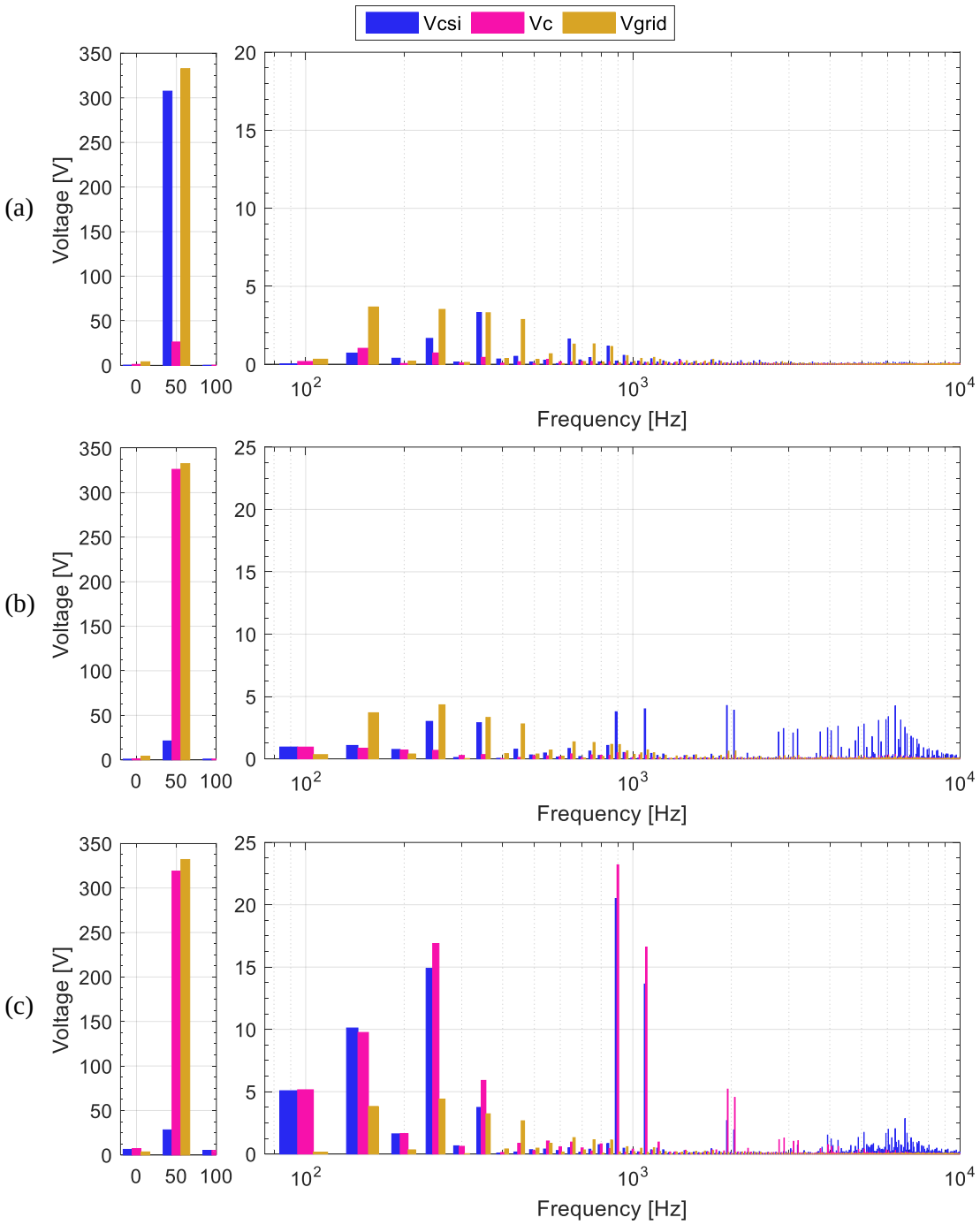


Fig 7-45: FFT of Phase A voltage of the Grid (V_g), Series capacitor (V_c) and CSI phase voltage (V_{csi}) during: a) No PWM; b) PWM enabled showing fundamental voltage reduction; and c) full system operation (harmonic cancellation).

The voltage harmonic spectrum for Phase A voltages is shown in Fig 7-45. Before PWM activation (Fig 7-45a), the fundamental voltage amplitudes are measured at 307.5V for $V_{csi,}$ 332.8V for V_{grid} and at 26V for the series capacitor voltage V_c. The low order grid voltage harmonics are visible with the 3rd, 5th, and 7th all at approximately 3.3V while the 450Hz (9th) harmonic is at 2.9V. During fundamental current component synthesis (Fig 7-45b), the CSI voltage reduces to 21V, while V_c is increased to 326V. As established in the previous experiment, the series capacitor voltage during this mode of operation is purely sinusoidal, which causes the low order 5th and 7th harmonics in the grid to be reflected in full on the CSI inputs, with the corresponding voltage harmonics reaching about 3V, same as seen in the grid voltage. Unlike previous scenarios, a resonance excitation is clearly visible on V_{csi} for harmonics above 900Hz, matching the harmonic excitation seen on the CSI current. The largest harmonic due to the resonance which occurs at 6.35 kHz reaches 4.2V with the overall resonant harmonic profile reflecting the resonance shape as seen in Fig 7-44. The 900Hz and 1.1 kHz switching harmonics reach approximately 4V.

During full hybrid operation (Fig 7-45c), V_{csi} slightly increases to 28V while V_c is measured at 320V and V_{grid} at 332V. The 900Hz harmonic is the largest at 20.5V for the CSI voltage and 23.2V for V_c while the harmonics at 1.1 kHz reach 13.6V and 16.6V for the CSI and Series capacitor respectively. The corresponding voltages caused by the CSI injection of low order harmonic currents that improves the low order harmonic content in the grid can be observed by the significant harmonic voltage amplitudes created, which would increase the CSI voltage ratings and the associated installed CSI power. The 3rd harmonic is measured at approx. 10V for both the series capacitor and CSI while the 5th harmonic reaches 14.9V for V_{csi} and 16.9V for V_c.

For harmonics above 3.5 kHz, the resonance is only observed across the CSI voltage (with the resonant voltage shared also between the L_2 and L_fR_f which are not measured) but at slightly lower levels than measured previously (Fig 7-45b), with the highest harmonic amplitude reaching 2.8V at 6.8 kHz. The effect of the added harmonics on the maximum CSI voltage stress will be shown in the next section.

7.2.3. Maximum Voltage Stress and Phase Symmetry

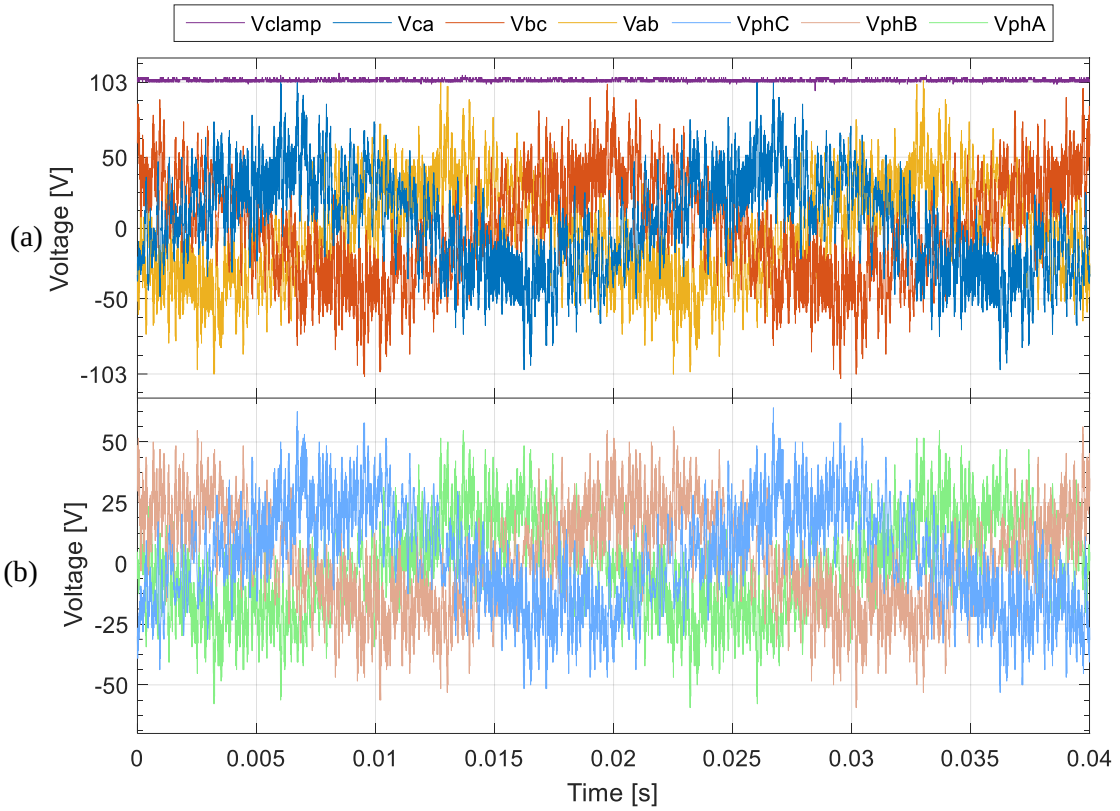


Fig 7-46: The CSI input voltages showing the fundamental voltage reduction in: a) the three phase line-line CSI voltages and the clamp voltage and b) the three phase-neutral CSI voltages.

The three phase-neutral and line-line CSI input voltages are shown in Fig 7-46 before ripple cancellation. It can be seen that the ripple in the waveforms appears to be more significant compared to all previous tests (§6.1.3 & §7.1.8.). The three phase-neutral voltages (Fig 7-46b) appear to be symmetrical, with the shape appearing slightly trapezoidal consistent with the typical distortion created by single phase rectifiers. When analysing the line voltages, the shape looks slightly triangular rather than sinusoidal, as explained in §7.1.8. While the majority of the phase voltage waveforms peaks remain under 50V, the maximum voltage contributed due to the observed spikes, is recorded at 65V. On the line to line voltage waveforms shown in Fig 7-46a, these spikes seem to contribute to the maximum clamp voltage which has been measured at 103V, significantly higher than the previous grid connected scenario (69V) in §7.1.8.

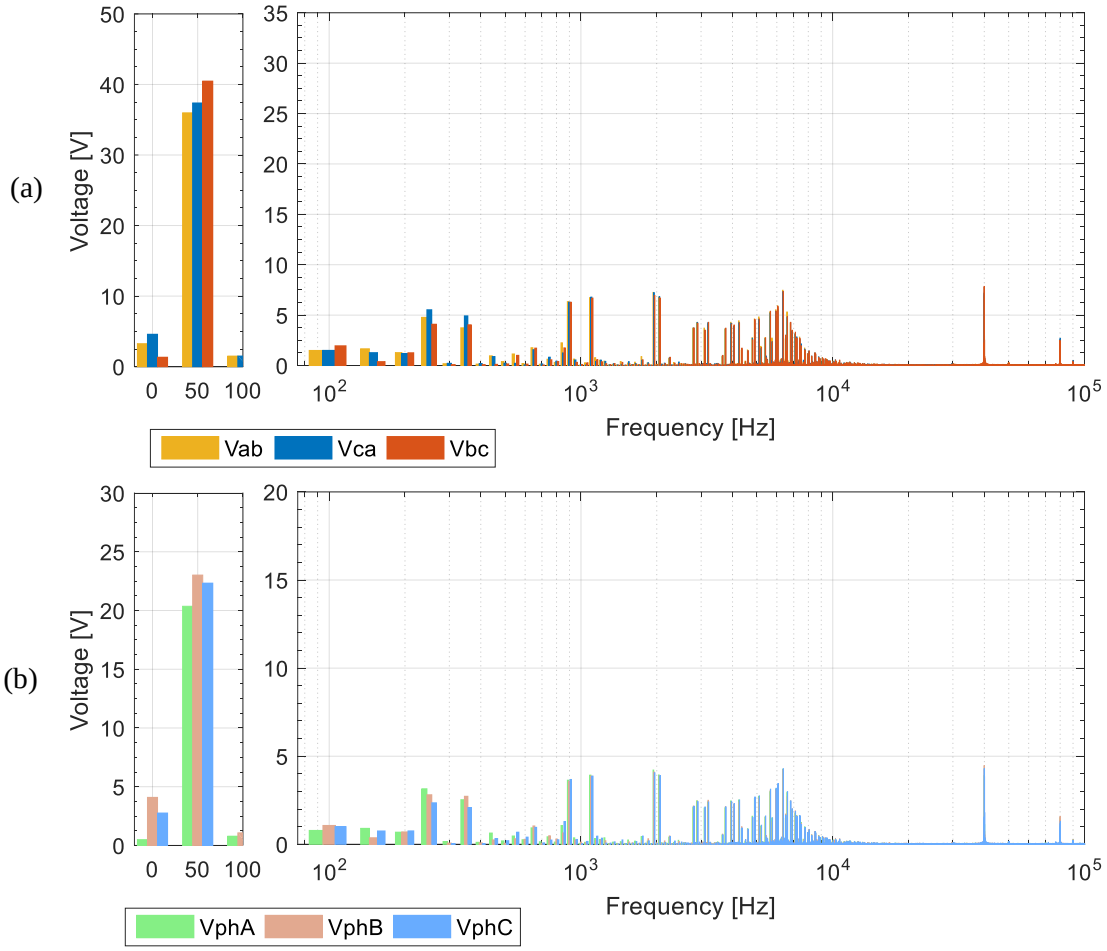


Fig 7-47: FFT of the CSI input voltages under fundamental voltage reduction mode showing the harmonics in: a) the three phase line-line CSI voltages and b) the three phase-neutral CSI voltages.

The fundamental component of the phase voltages A-B-C (Fig 7-47a) is at 20.3V, 23V and 22.3V while on the line voltages (Fig 7-47b) it reaches 35.8V 37.1V and 40.7V, having a maximum of 5V difference between the extremes. The fundamental component is at 7% of the grid voltage, lower than the 12% limit. A small DC component has been measured at 0.5V, 4V and 2.7V on the phase-neutral voltages and at 4.9V, 6.7V and 1.8V on the line voltages for V_{ab} V_{ca} and V_{bc}.

Similar to previous grid connected situations, during fundamental production the low order grid harmonics reflected on the CSI voltage are ranging around 5.6V-4V for the 5^{th} harmonic and 3.8-5V for the 7^{th} harmonic on the line to line voltages. The effect of the resonance can be observed on all three phase voltage waveforms with the excitation noticeable on harmonic orders from 18^{th} (900Hz) up to the filter resonant frequency. This can be compared to the equivalent FFT shown in Fig 7-35 in §7.1.8, where harmonic amplitudes in that frequency range remain under 1V.

The 900Hz harmonic is measured at 6.3V on the line voltages (3.7Vphase), the 1.1 kHz harmonic reaches 6.7V (3.9Vphase) for all three phases whilst the 1950 and 2050Hz harmonics reach 7.2V and 6.8V. In the remaining harmonic spectrum the highest harmonics are measured at the resonant frequency of 6350 Hz reaching 7.5V (4.3V phase) and at the harmonic cluster around the 40 kHz switching frequency which peaks at 4.5V for the phase voltages and 7.6V for the line-line voltage. All other harmonics remain under 6V.

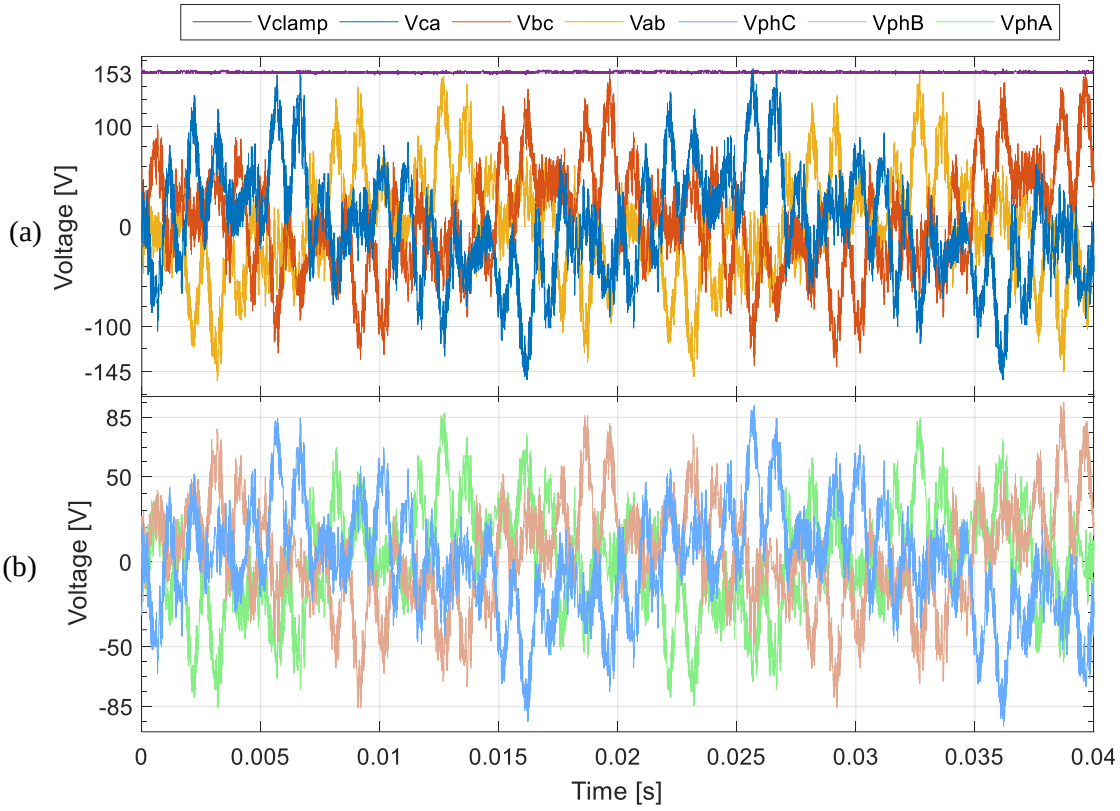


Fig 7-48: The CSI input voltages under full system steady state operation showing: a) the three phase line-line CSI voltages and the clamp voltage and b) the three phase-neutral CSI voltages.

The three phase-neutral and line-line CSI voltages are shown for steady state full hybrid operation in Fig 7-48. It can be observed that the resonant effects are less prominent, while the voltage waveforms seem balanced both in the phase-neutral and line-line waveforms, although a small offset can be observed between the negative peaks, a distortion caused most likely by the low order harmonic production. The voltage slightly exceeds 85V on the phase voltages (Fig 7-48b) while the maximum voltage stress given by the clamp DC voltage is measured at 153V, 26% of

the grid voltage, approximately a 1% increase compared to the previous grid connected scenario in §7.1.8 that had no resonance. In comparison, the discrepancy in the clamp voltage increase under fundamental voltage reduction mode (between resonance and no resonance) reached 5.8% of the line-line grid voltage peak.

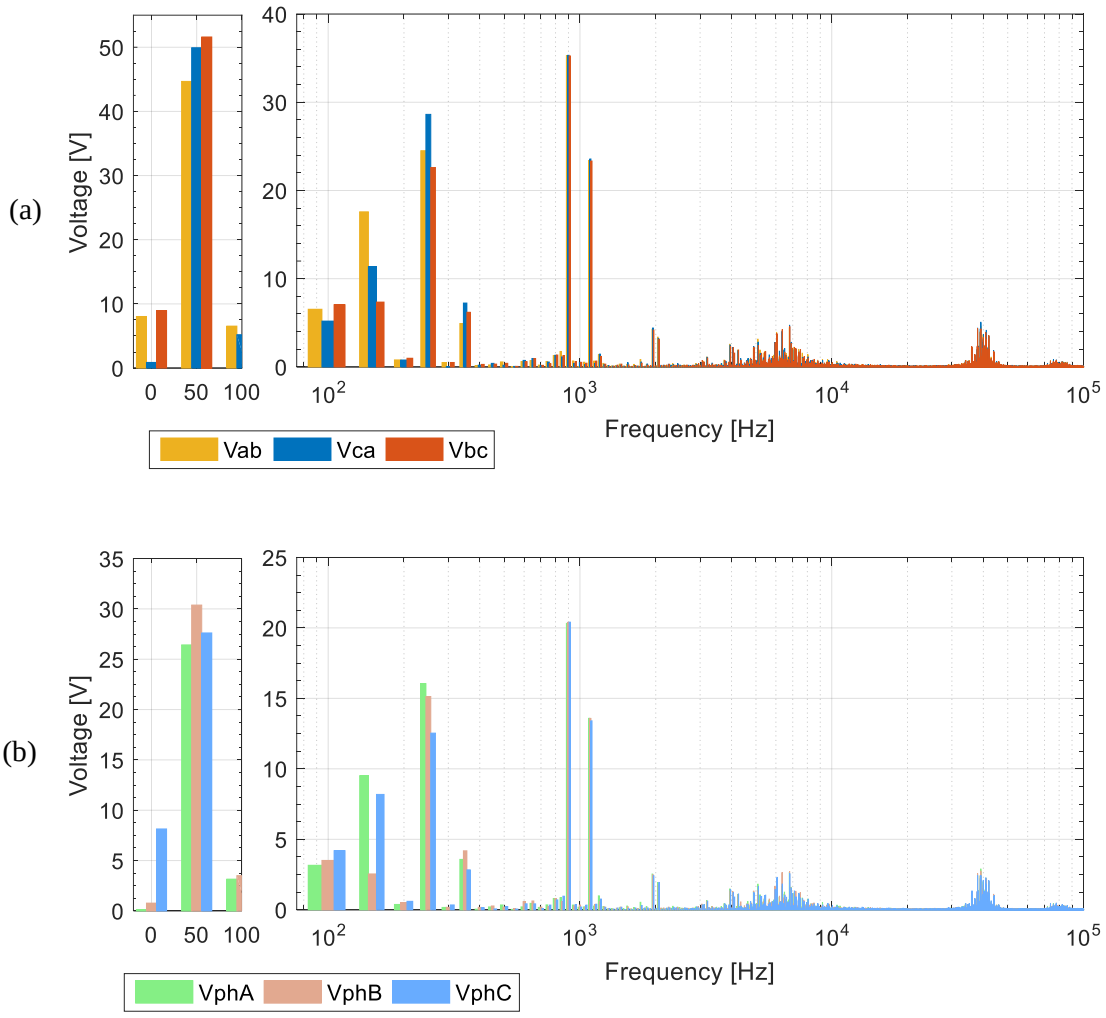


Fig 7-49: FFT of the CSI input voltages under full system steady state operation showing the harmonics in: a) the three CSI line-line voltages and b) the three phase-neutral CSI voltages.

The corresponding three phase CSI voltage harmonic content is shown in Fig 7-49 where the fundamental voltage amplitude is measured at 44.7V, 50V and 51.6V for V_{ab}, V_{ca} and V_{bc}, corresponding to amplitudes of 26.4V, 30.3V and 27.6V for phase-neutral A-B-C voltages. On the phase voltages, the DC component can be seen predominantly on phase C, measured at 8.1V,

while it remains at negligible levels for phase A and B. On the line to line voltage however it creates a more significant effect with 8V and 8.9V observed on phases V_{ab} and V_{bc}.

The increase on the 2nd, 3rd and 5th harmonic amplitudes is at similar levels as seen in §7.1.8 while still to a different magnitude on each phase voltage. The 2nd harmonic has been measured at 3.1V, 4.2V and 3.5V on the phase-neutral A-B-C voltages and 6.5V, 5.2V and 7V on the line voltages V_{ab}, V_{ca} and V_{bc}. The 3rd harmonic has been measured at 17.6V, 11.4V and 7.3V on the line voltages (9.5V, 2.5V and 9.5V on the phase voltages) whilst the 5th harmonic reached 24.5V, 28.6V, and 22.6V (16V, 15.1V, and 12.5V phase-neutral for the A-B-C voltages). The 7th harmonic is also slightly increased measuring approx. 7.2V on the line voltages compared to a maximum of 5V before ripple cancellation is enabled.

Finally the harmonic at 900Hz is measured at 35.25V on all line-line voltages (20.4V phase) and the 1.1 kHz harmonic is measuring 15.1V on the phase voltages with 23.5V reflected on the line waveforms. Most importantly the effect of the resonance is less pronounced, with the maximum amplitude for all higher order harmonics (including the 40 kHz switching harmonic cluster) remaining under 2.5V on the phase measurement and 4.5V on the line measurement.

7.2.4. Conclusion

This experiment has investigated the effects of resonance that appears when more grid inductance is added, albeit not at the full extend where the resonance could cause instability to the VSI, as observed by simulations in CHAPTER 4. The resonant frequency has been measured at 6.3 kHz but with a small excitation observed for all frequencies above 900 Hz, thus affecting the relevant frequency range for the VSI switching ripple.

The harmonic reduction capability of the CSI has been shown to be slightly compromised, with a loss of about 5% in attenuation compared with previous experiments. The added resonant excitation also led to a very small decrease in the CSI voltage reduction capability with the maximum CSI voltage stress measured at 26% of the grid voltage, compared to 25% observed in §7.1.8 without the resonance under the same operating conditions.

SECTION C: Discussion and Conclusions

CHAPTER 8. Comparative Performance Evaluation and Discussion

8.1. Performance Comparison

This section presents the comparative experimental performance evaluation for the different AC interconnection scenarios considered (ideal grid, real grid & real grid with added impedance) in an attempt to offer an overall picture of the performance capability of the hybrid solution. The results from the power analyser for power factor, THD and efficiency are initially presented before a final comparison is performed on the hybrid converter harmonic filtering capability based on the three phase grid current waveforms.

8.1.1. Power Analyser Results

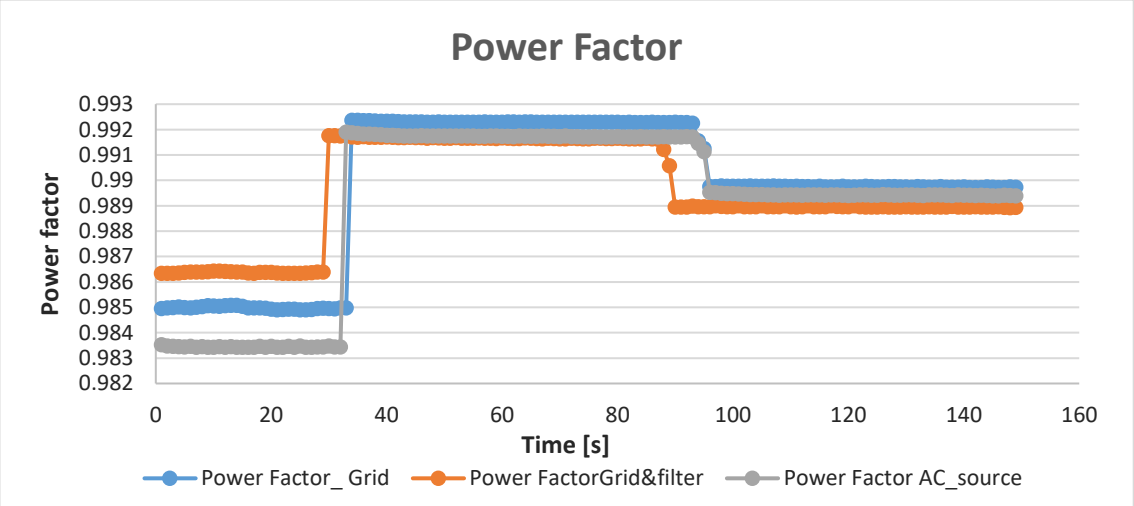


Fig 8-1: Power analyser displacement Power Factor measurement for different AC interconnections

The format of the results presented in this section replicates the experimental three-step transient procedure for converter operation, as described in §6.1.4.1 but will be reiterated for clarity. For the first 30 seconds of operation, PWM is disabled with the VSI operating as a diode rectifier.

After PWM activation, the CSI converter runs for 60 seconds injecting only fundamental reactive current to reduce the CSI voltage stress (without ripple cancellation) while the last 60 seconds are recorded during full hybrid system operation.

The impact of the system on the displacement power factor is shown in Fig 8-1. For all traces, the displacement power factor remains above 99% before ripple cancellation is activated and drops to 98.88% under full ripple cancelation operation. Note that a small difference can be observed as the effect of added grid inductance (orange trace) but this remains at negligible levels.

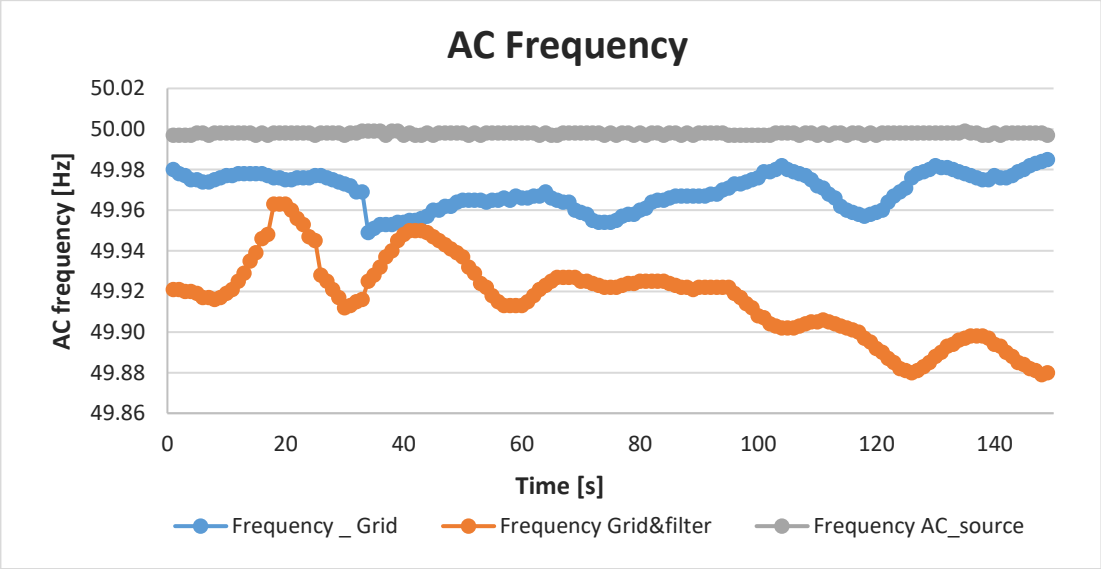


Fig 8-2: Power analyser grid frequency measurement for different AC interconnections

Fig 8-2 shows the power analyser measurement of the supply frequency for the three experimental configurations considered over the 150s period. The three phase electronic supply enforces a constant frequency of 50Hz while in both grid connected situations, the grid frequency fluctuates between slightly lower values. The lowest grid frequency has been recorded in the scenario considering the additional grid impedance where it is shown to decrease to 49.88 Hz. This frequency variation however is shown to have no notable direct effect on the harmonic cancellation as shown by the corresponding THD results in Fig 8-3.

The THD100, which considers harmonics up to the 100th order, has been measured using the power analyser (connected in a three-phase two-wattmeter setup) for phases A and B of the grid

current. The results plotted in Fig 8-3 show a first step around t=30s, when PWM is activated when the VSI starts to absorb sinusoidal currents but with very large switching ripple. Another significantly larger decrease in the THD is recorded when the current ripple cancellation is activated (around t=90s) for all tested configurations.

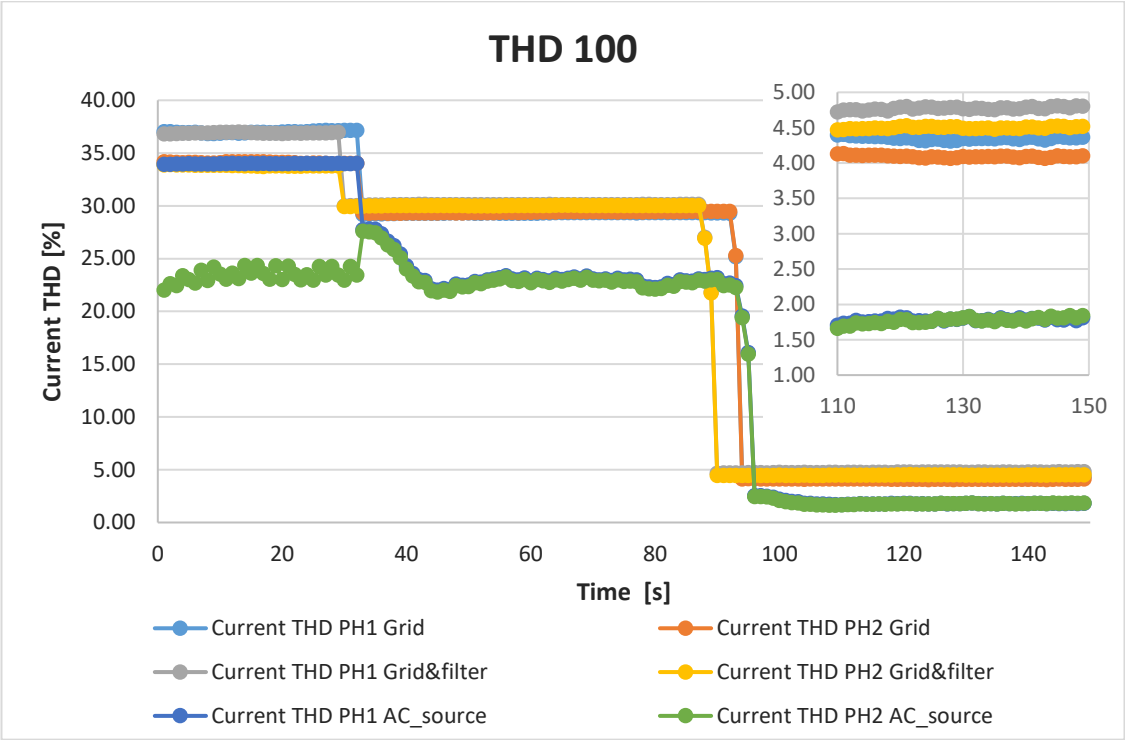


Fig 8-3: Power analyser grid current THD100 measurement for different configurations

During diode rectifier operation, the THD measurement reaches as high as 37% on the phase A currents under grid connection, while all other measurements are at 34%. An error can be initially seen on the phase B measurement when connected to the AC supply (green) up to t=32s but the reading shows convergence to the phase A measurement after PWM is activated.

After PWM is activated, the THD is measured at approx. 23% when connected to an electronic (ideal) AC supply and all this distortion is related to the switching ripple of the VSI. The THD increases to 29% under real grid connection. The change is a result of some small decrease of VSI switching ripple due to added grid inductance overcompensated by a larger increase accounting for the presence of additional low order harmonics. A small further increase to 30% can be seen due to the effects of the resonance caused by the additional AC filter.

The effects of ripple cancellation are obvious on all waveforms after ripple cancelation is activated (t>100s). The lowest THD is recorded at less than 2% when connected to the electronic AC supply but this increases to 4-5% under real grid connections. The highest THD is about 4.8%, for Phase A when grid connected with an added grid side filter.

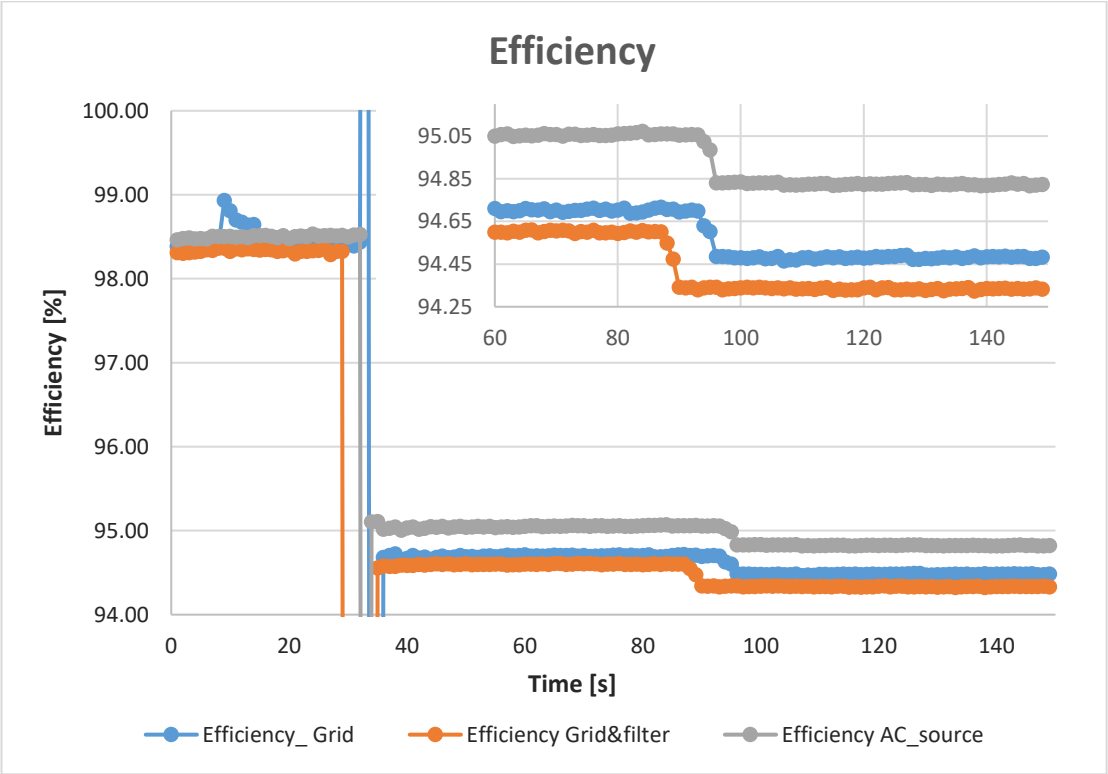


Fig 8-4: Power analyser efficiency measurement for different configurations

The efficiency has been recorded using the Power Analyser connected in a three-phase two-wattmeter configuration between the PCC and the VSI dc-side. For the first 30 seconds considering the VSI operating as a diode rectifier the power processed is approximately 2kW with the highest efficiency recorded. For the following period (t>40s) PWM is activated with the VSI processing approx. 4kW to maintain the 750V DC-link voltage at the reference value. The recorded efficiency in Fig 8-4 that accounts for losses in both the VSI and the auxiliary CSI, remains at the highest levels in the ideal grid connection scenario (AC source) measured at 95.05% before ripple cancellation is enabled, and then decreasing slightly to 94.85% during full operation which quantifies the added losses due to the auxiliary CSI producing the VSI ripple in addition to the reactive current to 0.2% (8W). In the grid connected configuration, the efficiency

is measured at 94.7% before ripple cancelation and 94.5% during full operation. A further drop is noted in the grid connected with added impedance configuration where the efficiency reduces from 94.6% to 94.3% during full operation. The drop in efficiency seems to be consistent with maximum CSI voltage stress as observed previously in these scenarios. Based on the 96.05% efficiency measured for stand-alone VSI operation (where the CSI and associated passive components have been disconnected), and a power processed of about 4.2kW, the maximum power loss added by the CSI is in the range of 70W, approx. 1.7% of the input AC power.

8.1.2. CSI Harmonic Cancellation Performance

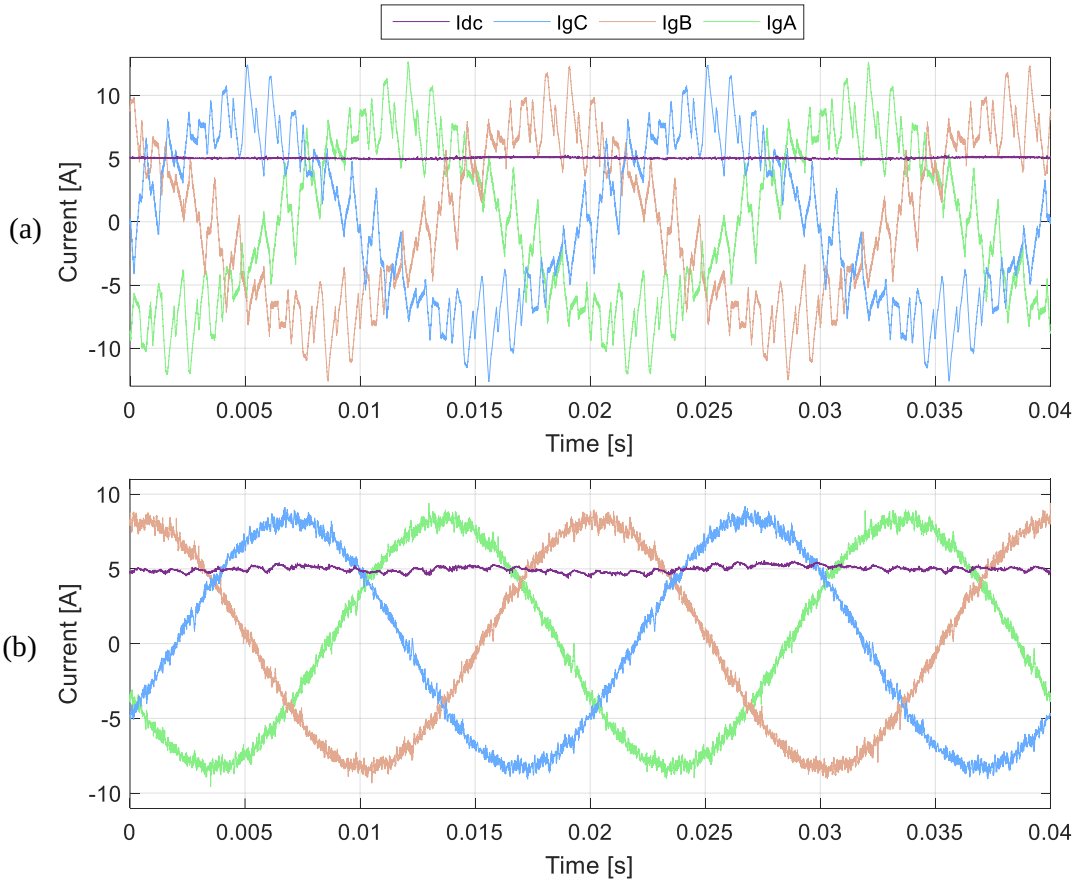


Fig 8-5: Three phase grid currents and CSI dc current under electronic AC source connection: a) before harmonic cancellation; and b) after harmonic cancellation.

This section is presented as a final overview of the three phase current harmonic quality of the hybrid system, assessed by the ripple in the three phase grid currents in the time and frequency

domain. The CSI dc link current is superimposed on the three phase grid currents which are shown before and after current ripple cancellation. The corresponding frequency harmonic content is also shown and discussed.

Considering the case of operation using the electronic AC source, shown in Fig 8-5, the currents before current ripple cancellation are extremely distorted, with the current ripple peak in excess of 4A, thus requiring a CSI DC link current of at least 5A to avoid CSI overmodulation and for the cancellation to be accurate. Under current ripple cancellation the grid side currents become sinusoidal with minor periodical spikes observed at the VSI switching instances. Note that the two sets of waveforms are captured at different instances and thus are unsynchronised.

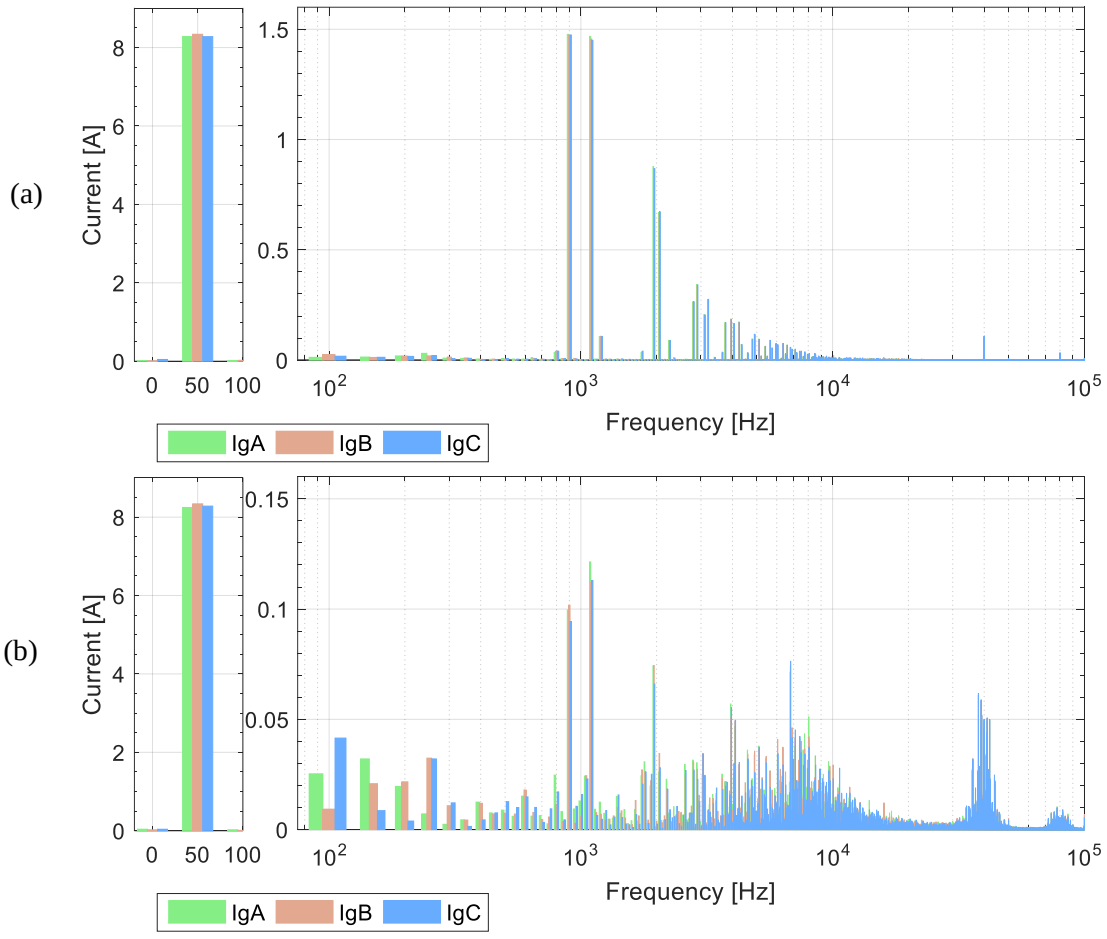


Fig 8-6: FFT of three phase grid currents and CSI dc current under electronic AC source connection: a) before harmonic cancellation; and b) after harmonic cancellation.

In this configuration the harmonic content on the VSI current (Fig 8-6) is observed from 900Hz up to 10 kHz but with amplitudes diminishing to negligible levels beyond 5 kHz. The effectiveness of harmonic cancellation is proven by the low amplitudes of harmonics remaining in the grid current. The largest harmonic amplitudes remain less than 0.11A and 0.13A (0.9 kHz and 1.1 kHz) showing a reduction of up to 95% compared to the original VSI switching harmonic amplitudes. All other harmonics remain at amplitudes below 1% of the fundamental current amplitude (80mApk).

It should be again noted that for the grid connected experiments, the VSI modulator was modified to the double edge option which affected the VSI current harmonic profile by creating a reduction in the 1.1 kHz (and a subsequent increase in the 900Hz harmonic) but this was found to have no impact on the experimental performance.

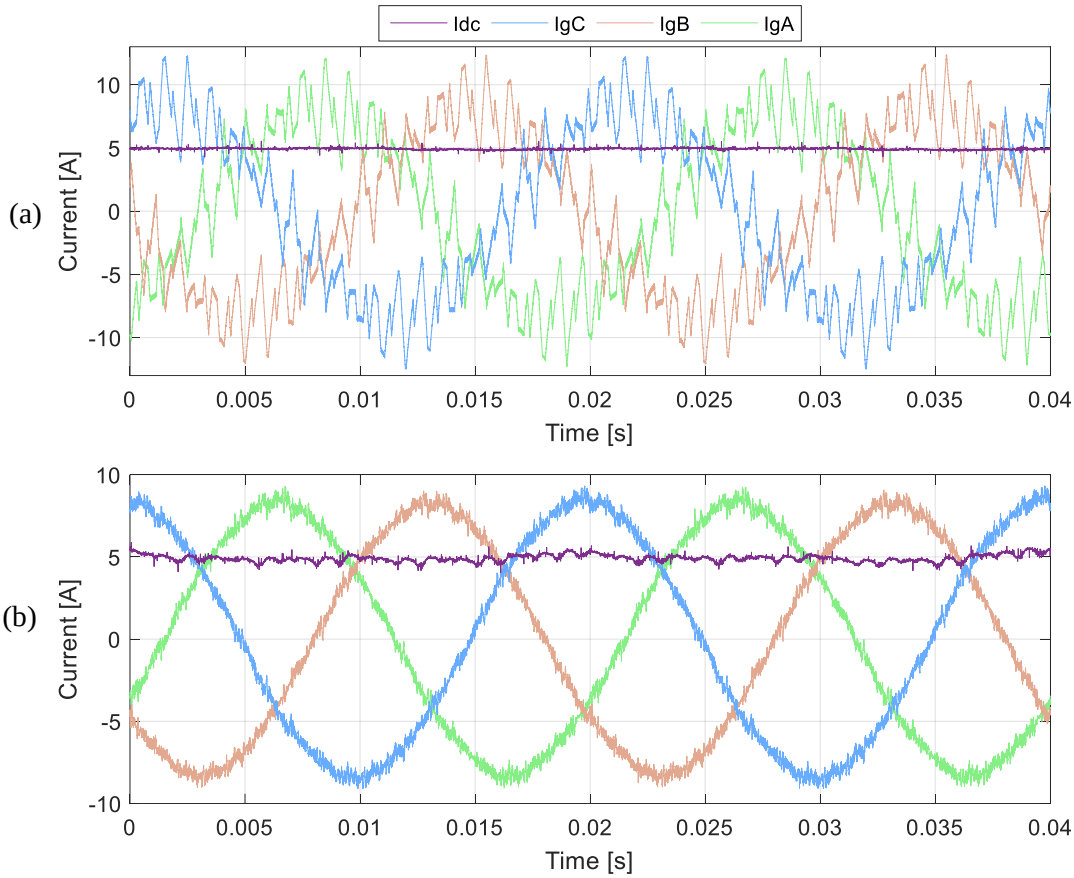


Fig 8-7: Three phase grid currents and CSI dc current under real grid connection: a) before harmonic cancellation; and b) after harmonic cancellation.

The operation of the VSI under the real grid voltage disturbances led to an increase in low order harmonics (3rd, 5th, 7th) on the VSI current (Fig 8-7), although this is not visible prior to harmonic cancellation due to the large amount of switching ripple in the waveforms. Some slight deviation from a perfectly sinusoidal waveform shape may be observed when comparing the time domain output grid current waveforms to the previous scenario. Nevertheless the effectiveness of the waveform clean-up is obvious with very small artefacts remaining on the grid side currents. The previously observed spikes do not occur in this case due to the effect of the added grid inductance.

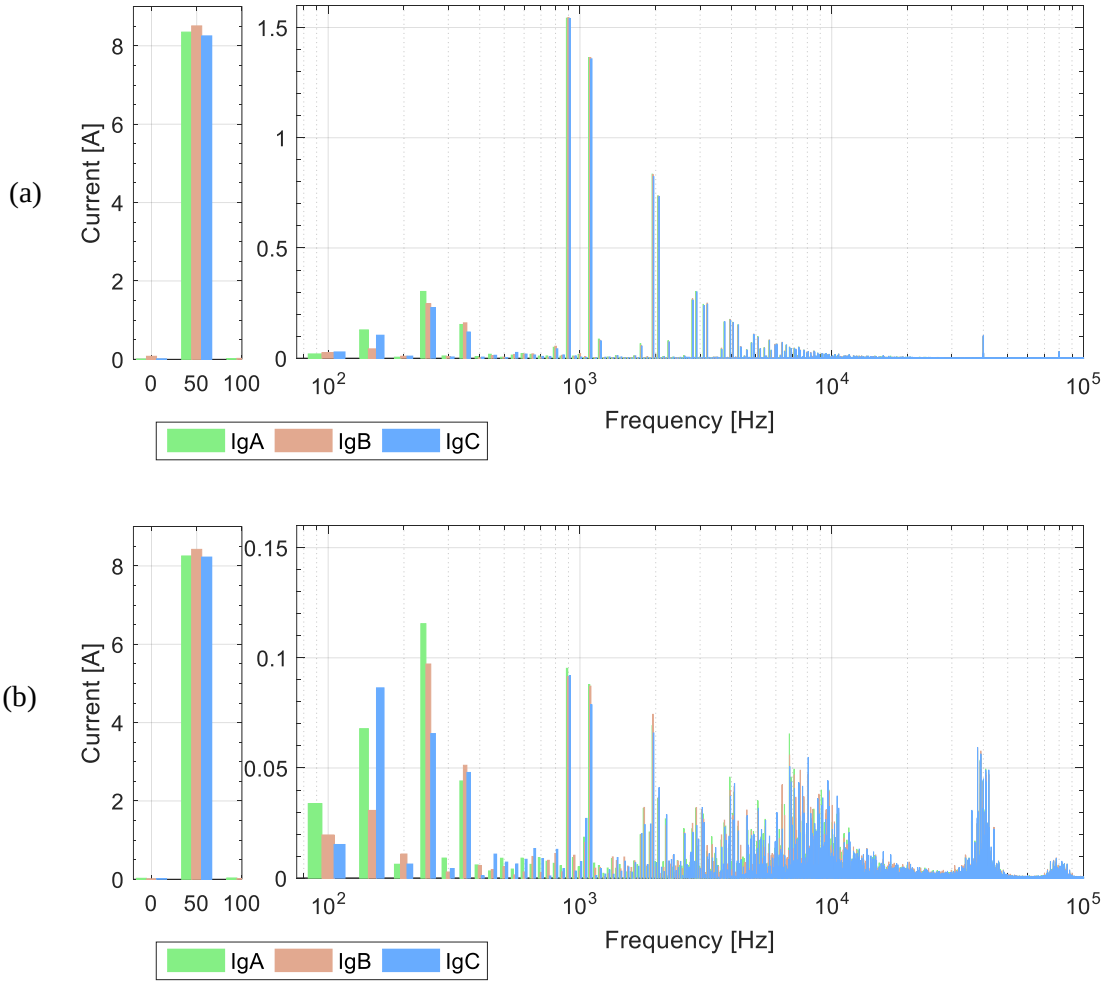


Fig 8-8: FFT of three phase grid currents and CSI dc current under real grid connection: a) before harmonic cancellation; and b) after harmonic cancellation.

The harmonic content of the current before ripple cancellation (Fig 8-8) reveals the small but significant differences under real grid operation. A small imbalance of approx. 0.2A can be observed between the fundamental component amplitudes of the different phases as well as low order current harmonics, unbalanced as well, reaching up to 0.3A.

Although not to the same extend as for switching ripple harmonics, the current ripple reduction is also occurring on the low order harmonics. Most harmonics in the resultant spectrum remain under 0.1A which is approximately 1.2% of the fundamental amplitude (with the exception of the phase-A 5th harmonic).

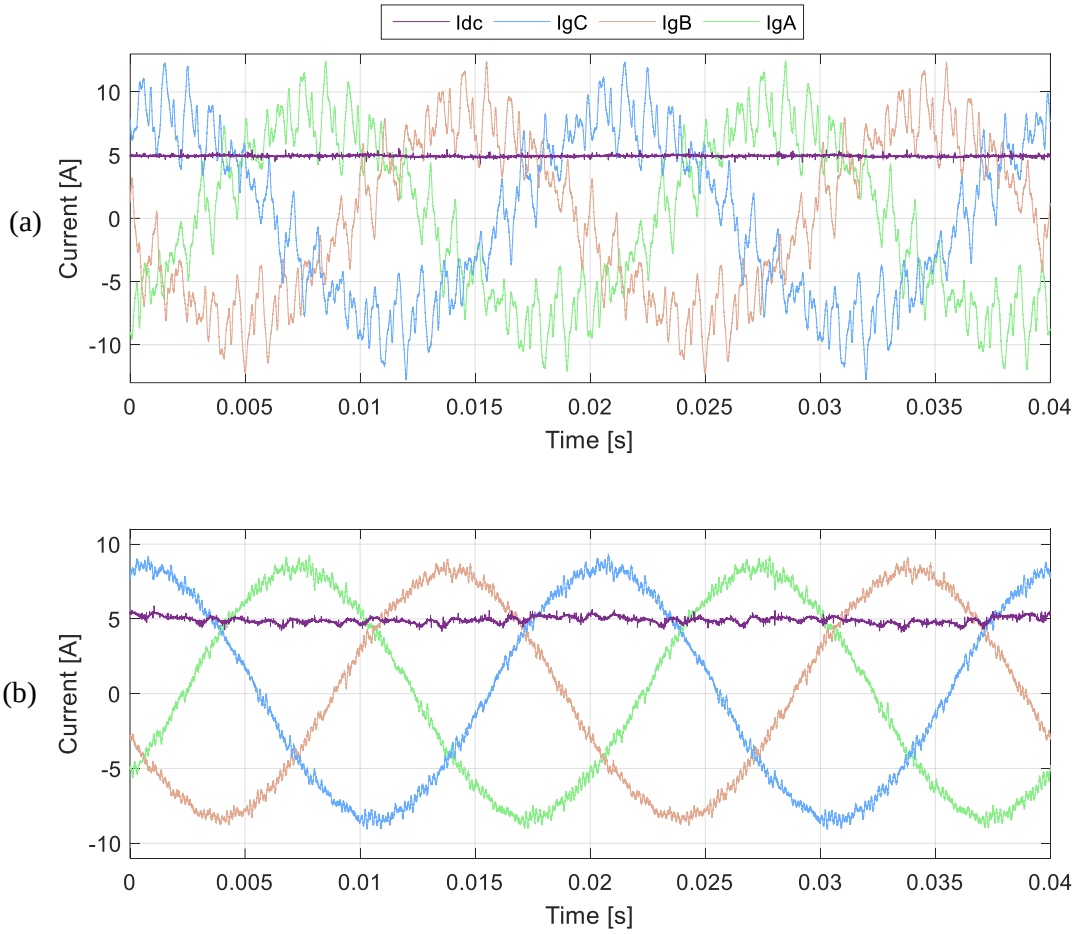


Fig 8-9: Three phase grid currents and CSI dc current under real grid connection via additional AC filter: a) before harmonic cancellation; and b) after harmonic cancellation.

In the final configuration where the converter was connected to the grid via an additional higher impedance (Fig 8-9), the low order harmonic effects are still present in the three phase currents. In addition, a resonant effect created by the filter at about 6 kHz, generates additional oscillations which may be observed on the grid current waveforms before as well as after current ripple cancellation.

In the time domain, the resonance does not seem to affect the effectiveness of the cancellation with the output waveforms being sinusoidal. The ripple remaining in the grid side currents however, is at the filter resonant frequency while the 40 kHz CSI switching ripple harmonics are minimised by the additional attenuation offered by the added AC side impedance.

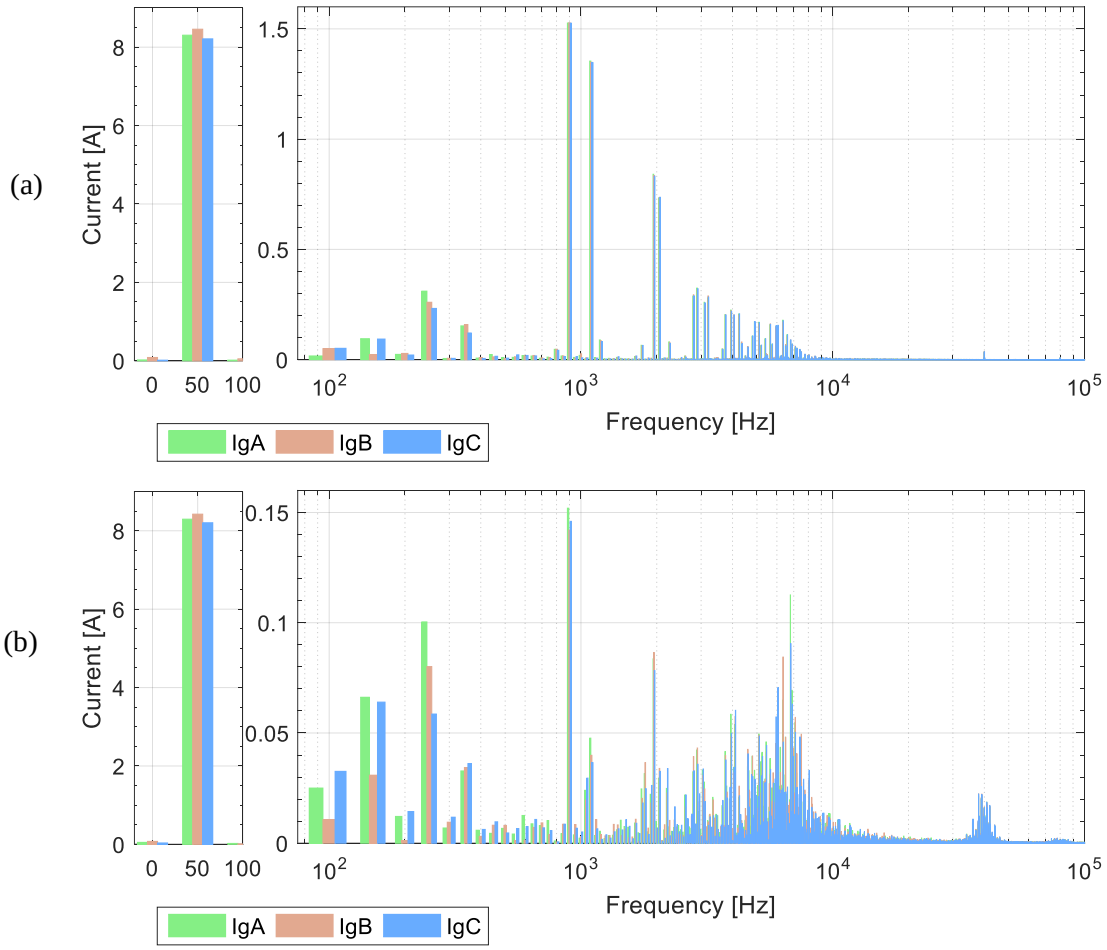


Fig 8-10: FFT of three phase grid currents and CSI dc current under real grid connection via additional AC filter: a) before harmonic cancellation; and b) after harmonic cancellation.

The resonant effect is more obvious when looking at the grid current in the frequency domain, shown in Fig 8-10. Before current ripple cancellation is enabled, a small excitation can be seen around the 6.4 kHz resonant frequency. Similar to the previous scenario, grid connected operation results in a fundamental component imbalance as well as low order harmonics which are also unbalanced in amplitude.

Under full system operation the low order harmonics are cancelled with the remaining harmonics in the grid current at similar levels to results without resonance. However a loss of attenuation is evident at 900Hz (90.5% reduction compared to 94.6% in the case of ideal grid and 94.7% for small impedance). The result of the resonant excitation can also be observed at about 6 kHz on the filtered current, while the cluster at 40 kHz is significantly reduced compared to the previous scenarios. The highest harmonic in this scenario is the 900Hz harmonic approaching 2% of the fundamental current while most other harmonics remain under the 0.1A threshold (around 1.3% of the fundamental component).

8.1.3. Summary

This previous section has provided a comparison of the experimental performance achieved through the different experimental set-ups presented in chapters 6 and 7. The active current ripple cancellation concept has been shown to be highly effective in the reduction of the VSI current switching harmonics throughout all the experimental configurations evaluated. The harmonic reduction capability remains unaffected when operating under an imbalanced grid achieving generally a 95% reduction for the most significant VSI switching current harmonic amplitudes and leaving the remaining current harmonics at less than 2% of the nominal VSI fundamental current amplitude. Some compromise in performance has been observed when the grid impedance is large enough to create a resonance within the frequency range of the VSI switching ripple harmonics (700Hz- 5 kHz). This would mean that additional control considerations will have to be taken to deal with the resonance and maintain the desired current filtering capability.

Fig 8-11 shows the resulting filter attenuation for the three configurations considered, as derived by analyzing the attenuation of relevant VSI relative to the grid current harmonics, in decibels (dB). The resultant performance cannot be directly compared with a passive filter solution but the attenuation reaches or exceeds -25dB for the largest switching harmonics (1-2 kHz) for all experiments. The attenuation reduces for higher harmonic frequencies partly because the VSI harmonics are too small and more influenced by errors and secondly due to the delay becoming fore significant. Another reason may be due to the more significant bleeding current absorbed by the capacitance C_p as observed in the CSI AC filter open loop response. For the scenario considering resonance at 6.3 kHz (shown as Grid&filter in Fig 8-11), a slight further reduction of approx. 5dB can be observed the trend of the attenuation from 4-6kHz compared to the other two curves which don’t consider any resonance.

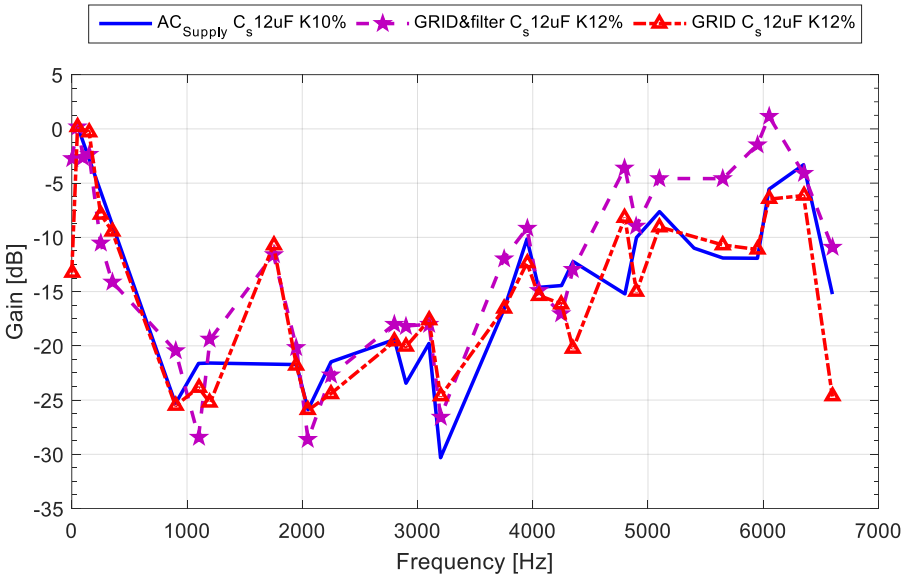


Fig 8-11: Attenuation of relevant VSI current harmonics for the experimental configurations considered.

The experimental procedure has considered a wider variety of operating points and conditions which have not been initially anticipated and as a result have not been theoretically addressed at the simulation stage. The connection to the real grid, has introduced added challenges which have now been addressed (e.g. voltage unbalance) or acknowledged as a further trade-off to achieving the desired performance (e.g. low order harmonics).

The desire for the evaluation to maintain constant operating conditions throughout all experiments (which would make direct comparison of results straightforward) has been partly compromised due to the further investigations at a late experimental stage which consumed time and effort that impacted the consistency of the experimental investigations. On an overall scale however the impact of these discrepancies does not compromise the main findings of the evaluation with respect to the main targets which were the assessment of the filtering capability of the CSI as well as the ability to operate with a significantly smaller voltage stress.

8.2. Discussion on the System Performance

The use of a CSI is associated with simple control system which from a computational requirement would suit the high switching frequency needed in this application. The initial control approach has been designed based on satisfying the basic requirements of system operation for an ideal operating condition. On the development of the hybrid topology, additional requirements have surfaced which demonstrated that a more advanced control approach is required for operation under realistic grid conditions. Some of these problems have been created by the scaling of the system components and also associated with the choice of topology. These observations and requirements are outlined in the following section.

For operation with a stiff/ideal grid, the harmonic cancellation can remain effective in open loop based on the merits of output filter design which has been scaled and adapted to suit this operation having a linear response/negligible phase-shift up to 5 kHz. The direct AC current synthesis of the CSI enables effective reduction of the VSI switching harmonics, however, a high CSI switching frequency has been identified as a requirement to maintain appropriate ripple cancellation, avoiding harmonic interaction with the CSI filter resonant frequency and maintaining low stress due to the CSI switching voltage ripple which is considered a secondary factor adding to the overall CSI voltage stress.

Simulation results with an ideal grid yielded a current THD improvement from 12% to slightly above 2% which accounts for all harmonics present. Experimentally the current THD measurement showed a reduction from 23% to 2% however without accounting for harmonics added by the CSI. The voltage reduction in simulation remained significantly below 20% for both series capacitor values considered which is similar to the lowest experimental reduction achieved of 22%. This increase is attributed to the higher amount of VSI switching ripple cancelled, creating a larger CSI voltage stress. The overall behaviour of the hybrid converter showed very good correlation to the expected performance and therefore the circuit operation under the proposed control scheme has been validated.

Hybrid system operation under connection to the real grid introduced large and unforeseen challenges. The main source of voltage disturbances occurred partly due to the oversimplified VSI control circuit which initially was thought to be acceptable and partly due to the implementation of the current ripple extraction stage, which has proven to be inadequate in satisfying the requirement of extracting only the current ripple harmonics without any low order harmonic disturbances.

The interdependency of achieving good steady state performance against good transient response has been identified at the simulation stage, however in the experimental setup the tuning of the moving average filter at the CSI switching frequency has proven to be less effective when operating with a larger current ripple amplitude. The addition of a low pass filter has improved the ability to extract the maximum current ripple but also increased the propagation of the unwanted low order harmonics to the CSI reference.

Due to an oversimplified VSI control system, a small fundamental current unbalance (~0.1A) has been found to significantly compromise the voltage reduction capability of the CSI. This problems have also been acknowledged in [97] where an inability of the series capacitor CSI HAPF to compensate for current disturbances created by a non-linear load supplied from an unbalanced voltage source has been identified. An asymmetrical current injection through a symmetrical series capacitor set will create a negative sequence voltage which will appear across the series capacitor and be mirrored on the CSI input voltages.

The series capacitance scaling approach, where the capacitance has been minimised to reduce the reactive power requirement has a secondary implication on the voltage reduction scheme. The design, which favours a smaller reactive current component for a given voltage reduction, does not take into account that by extension the smaller series capacitance will lead to larger voltage disturbances for a given low order harmonic current disturbance. To maintain operation under grid disturbances with low CSI voltage stress, these disturbances must be removed via the control system.

To rectify this issue, a revised control system design has been proposed involving a negative sequence voltage compensator based on the measurement of the CSI or series capacitor voltages. The DDSRF approach has been used to extract the inverse sequence voltage of the series capacitor which is then fed to a PI controller and the output is added to the CSI reference as an inverse sequence fundamental current. The solution has been validated experimentally showing that phase voltage balancing is restored. The effectiveness of the solution should in the future be evaluated in the case of a larger grid voltage unbalance.

In addition to the compromising effect created by the fundamental current component unbalance, a second compromising effect to the voltage reduction scheme has occurred due to the presence of low order harmonics in the grid voltage. It should be acknowledged that these harmonics do not directly affect the CSI voltage reduction, as seen experimentally when only the fundamental current is component is synthesised by the CSI. Instead, the problem is created by the low VSI control bandwidth as well as the unequal harmonic amplitudes, which cause low order VSI current harmonics. Due to the tuning of the current ripple extraction stage, these harmonics also propagate as a reference to the CSI where cancellation can be observed. Based on the series capacitor scaling, these low order current harmonics create large and imbalanced low order harmonic voltages on the series capacitors mirrored across the CSI inputs, increasing the voltage stress. Different directions could be followed towards dealing with this problem. Ideally the VSI control can be improved further to mitigate the remaining 3^{rd} 5^{th} 7^{th} current harmonics which has been proven to be possible in literature, but is limited when the VSI switching frequency is low.

Another direction to maintain low CSI voltage stress would be to mitigate these harmonics at the CSI ripple extraction stage of the control and prevent their cancellation by the CSI. However this solution would effectively allow low order harmonics to propagate to the grid which is counterproductive for active filtering operation. Alternatively the series capacitance could be rescaled in order to take into account a permissible level of low order harmonic current will result in a small added CSI harmonic voltage. However this would be done at the expense of an increased current rating associated with a larger fundamental current component needed by the

larger series capacitance to produce a given fundamental voltage drop. The THD100 in this scenario has been measured at approx. 30% before ripple cancellation was enabled compared to 4.5% after activation of ripple cancelation. The THD increase compared to the ideal grid scenario (2%) is attributed to the low order harmonic presence. The CSI voltage stress in this scenario with the negative sequence compensator enabled has been measured at 25% of the grid (§7.1.8) compared to 45% during unbalanced operation (§7.1.3).

The shift in resonant frequency expected in the real grid scenario due to the grid inductance (no added inductance) has not been observed (§7.1.7.) The final experimental setup (§7.2.1) sought to investigate the effects of added grid impedance. The additional grid inductance induced the resonant effects as described in the first section of CHAPTER 4 (§4.1), representing a scenario where the grid side inductance (L_g & L_2) is at similar levels to the filter inductance(L_f) and the associated resonance is moved towards lower frequencies (6.3kHz in this case). At this resonant frequency placement, situated just on the upper range of the VSI switching current harmonics, a small but noticeable excitation can be observed on the CSI AC currents with an equivalent effect observed on the CSI voltages, slightly affecting the voltage stress. The open loop current cancellation scheme under these conditions revealed a small effect in the current filtering capability. It should be noted that this test has also been conducted with the low order current harmonics present in the VSI current as well as the negative sequence compensator enabled to restore CSI voltage balance.

At the level of resonant excitation considered (8.8dB at 6.3 kHz), the majority of the VSI switching ripple can still be cancelled by the CSI. The resulting grid current ripple around the 40 kHz CSI switching frequency is reduced by the added grid impedance. On the other hand the resonance frequency shift from 9.5 kHz to 6.3 kHz causes an increase in harmonic excitation that is observed in the grid current harmonic content. The operation under this conditions has no identified benefits thus, although it is feasible, it is not desirable.

Two solutions which would be implemented would be the addition of further grid side inductance which would lower the resonance within the bandwidth of the CSI where a closed loop system

control should be implemented to damp the resonance. Although the motivation for this test was to validate the active damping resonant compensator as proposed in CHAPTER 4, the additional setbacks mentioned due to operation under the given real grid conditions made this investigation impossible under the limited project time schedule.

An additional aspect which has not been experimentally validated is the proposed compensation of the reactive current injected by the series capacitor by the VSI. This has been omitted due to the assumption of independent operation of the VSI from the CSI and the motivation to demonstrate that based on reasonable series capacitor selection, the impact on the power factor is minimal. The power factor for full load operation in simulation has been measured above 98% for the larger series capacitance and above 99% for the minimum capacitance considered while experimentally it has been measured to be above 98.8% for all scenarios considered.

This is also the case for the DC voltage compensator which has not been implemented. Based on the captured voltage waveforms, although a small DC component is noticeable in most experiments, it remains at relatively low levels having a small impact on the maximum voltage stress. The implementation of the compensator would be still recommended as a safety feature to replace the resistance added in parallel to the series capacitors.

Finally, the impact on efficiency has also been experimentally assessed and accounts for the total hybrid converter losses. VSI standalone operation has yielded the highest efficiency of 96%. The efficiency under full operation ranges from 94.8 to 94.3% meaning that the addition of the CSI and associated passives added a total of 1.2-1.7% losses to the VSI system. This however cannot be directly compared to the simulated loss estimation which only accounted for the semiconductor losses and also refer to a different scaling of the system (MV/MW) which resulted in the CSI operating at a larger relative current stress relative to the VSI. Another aspect worth noting is that the experimental setup used a smaller inductance for the VSI to produce more switching ripple. In a system with passive LCL filtering, a larger value for this inductance would have to be used to provide the necessary level of 1kHz ripple attenuation, resulting in larger inductor and therefore

total inverter losses which would lead to a smaller (potentially negative) difference in efficiency (VSI and filter) compared to the hybrid system proposed and investigated in this thesis.

8.3. Summary of Findings

The operation of the proposed hybrid concept has been validated. The following are the key findings of this investigation:

- The added installed power by the auxiliary CSI converter can remain at very low levels which for a medium-voltage implementation could be below 4%. This has been shown both analytically and via simulations considering a 3.3kV medium voltage grid.

- A dependency exists between the sizing of the series capacitor and the maximum CSI voltage and current stress for a given amount of current ripple to be eliminated which enables the implementation of an optimal design procedure. This has not been reported in previous literature as the minimisation of installed power has not been achieved to this extent

- The use of the CSI has a small impact on the overall system efficiency. The impact of the series capacitors on the output power factor is also small. Experimentally the CSI losses accounted for 1.7% of the AC power measured while in simulation the losses were under 1% including the VSI.

- To ensure a low CSI voltage stress, the CSI must not compensate for low order current harmonics as they will create a large additional voltage across the series capacitance (as the voltage is inversely proportional to the harmonic order) which will in turn result in significant additional CSI voltage stress. This is a limitation of the circuit under the proposed scaling procedure and operation.

- It has been confirmed that current ripple cancellation can significantly improve the harmonic quality of the distorted VSI currents and can be performed without the requirement of a closed loop control circuit. The CSI can provide up to a 95.5% reduction in the main switching current harmonics produced by the VSI.

- Based on the repetitive pattern of the current ripple it is possible to use a current ripple delay compensation scheme by using the instantaneous ripple reference from the ripple

extracted during the previous fundamental cycle similar to the concept of repetitive controllers.

- Grid impedance can affect the CSI AC filter resonant frequency and affect the resulting hybrid system grid current quality. The placement of the series capacitor combined with a grid side inductance can create a 3rd order response which will affect both converters.

- An added grid side inductance could create an LCL type behaviour to shift the filter resonant frequency within the bandwidth of the CSI. An active damping approach could be then implemented to damp the resonance effects and provide stable operation.

- A small asymmetrical fundamental current injection through the series capacitors can create a large CSI input voltage unbalance which can dramatically increase the CSI maximum voltage stress as well as current stress due to DC-link oscillations in the CSI current.

- In case of unbalanced operation (eg unbalanced grid voltages), the CSI voltage balancing and minimisation of the voltage stress could be restored via the use of a negative sequence voltage compensator which can mitigate the negative sequence voltage components created by VSI current imbalance or by imbalance in the series capacitor values.

- DC voltage disturbances in the CSI reference waveforms could create a DC voltage offset which will be mirrored between the series capacitor and CSI voltages. The offset can be removed via the use of a DC voltage compensator or via the placement of a parallel resistance across each series capacitor.

CHAPTER 9. Conclusions

This chapter presents the conclusions, highlighting the key performance advantages and disadvantages offered by the proposed hybrid concept. The following section provides a summary of the novel aspects derived from this work. The final section concludes with proposals for future research work on this topic.

9.1. Conclusions on the Hybrid Concept

A hybrid converter concept has been proposed which enables the use of a low installed power CSI, switching at high frequency to improve the current harmonic performance of a main high voltage/power VSI operating at low switching frequency which would be typical of MV AC/DC conversion grid connected applications. By having the auxiliary CSI cancelling the VSI switching ripple, which is at a fraction of the total current processed by the main VSI and connecting it to the MV grid behind series capacitors to minimise the grid induced fundamental CSI voltage stress, the added installed power in the auxiliary inverter has been shown via simulations to be consistently lower than 4% of the main inverter.

The experimental validation has been performed at 415V grid voltage level but with the VSI producing a much larger current ripple (>50% of the fundamental compared to the specified 20% level used in the simulation). This circumstance has shown that the hybrid operation is feasible under the open loop cancellation technique for a balanced/stiff grid although with a minimum installed CSI power of 7 %.(CHAPTER 6)

9.1.1. Advantages and Disadvantages of the Hybrid Concept

The capability to provide high level of switching ripple attenuation (reduction to 5-8% of the original harmonic level) with low installed power in the auxiliary CSI is proved by both simulation and experimental validation on a prototype scaled at typical grid voltage and power ratings for a realistic implementation of a power electronic demonstrator.

The main drawback of choosing a CSI is the additional voltage stress which could occur during transients or in case that a DC or other low order harmonic current is synthesised by the CSI. The control requirements are therefore stricter than initially considered for the use of the CSI.

Another disadvantage is that for a small grid-side inductance between the series capacitor connection and the grid, a small amount of current ripple which is mainly at the CSI switching frequency and partly at the CSI output filter resonant frequency will propagate towards the grid. In the case of a higher grid-side impedance, the current ripple at the CSI switching frequency will be attenuated however the interaction of the grid inductance with the LC filter of the CSI will cause a significant reduction of the CSI filter resonant frequency towards the frequency range of the VSI switching harmonics. Excitation of this resonance may create additional stability problems and requires a closed loop control method to achieve sufficient damping.

Other disadvantages of using the low power rated CSI as part of the hybrid concept are the increase of converter losses and a slight decrease in the displacement power factor. These would also happen in case a higher order passive filter (LCL) were to be used to provide similar levels of attenuation of the VSI current ripple, whilst also raising the same stability problems which are more difficult to address with a slower inverter. It can be concluded that the proposed hybrid solution provides an interesting added performance vs cost trade-off.

9.2. Novelty

This PhD thesis has proposed and investigated a novel hybrid topology which guarantees high output current quality using a very low installed power auxiliary CSI inverter. The findings of this investigation and the relevant work for the development of the hybrid concept resulted in two journal paper and four conference paper publications which are listed in Appendix L.

The analytical model for the desired circuit operation for reduced CSI fundamental voltage stress has been derived with a suitable design procedure proposed for the passive component and system scaling. The dependency between the main inverter switching current ripple, the desired fundamental voltage/current CSI stresses and the size of the series capacitance has been identified. A numerical simplified model has been used to perform a preliminary optimisation considering a wide range of series capacitance values which showed that the added installed power of the CSI and losses can remain at very low levels for all capacitor values considered. A suitable control strategy to facilitate the harmonic cancellation under reduced CSI stress has been proposed. The low CSI added installed power has been verified via simulation at 3.3 kV level using two different values of series capacitor. The effectiveness of the current ripple cancellation strategy to the improvement of the grid current quality has been confirmed. The impact of the CSI and series capacitor on the total semiconductor losses and output power factor has been investigated. The impact of low order and DC harmonic disturbances on the CSI operation has been demonstrated and a solution proposed to minimise any CSI DC voltage stress. The solution involves either the use of a DC compensator via the control system or by placing parallel resistors to the series capacitors which will dissipate any DC component but not otherwise affect the circuit operation.

The impact of the grid inductance on the CSI output filter characteristic has been analysed. An alternative circuit configuration considering the CSI interconnection to a VSI which uses an LCL filter has been proposed. A modified design procedure based on the resonant behaviour induced by the scaling of the passive components has been proposed. An active damping solution to ensure the stability of the circuit operation has been proposed and validated via simulations. A further modification to the circuit topology has been proposed and validated in simulations to address the

additional voltage ripple created by the CSI switching at the PCC. A small capacitance is connected the PCC to provide additional attenuation for high frequency voltage harmonics but otherwise does not affect the CSI filtering capability.

An experimental prototype of the novel hybrid concept has been designed and built. The performance of the hybrid system has been thoroughly evaluated at a grid voltage of 415V and at a realistic processed power considering both an ideal and real grid connection. The impact of CSI switching frequency on the CSI voltage stress and the CSI harmonic reduction capability has been evaluated. The impact of distorted grid voltages on the hybrid system performance depending on the control scheme has been demonstrated. A revised control system has been proposed and validated to minimise any fundamental voltage unbalance on the CSI voltages. The resonant effects created by an added grid side inductance have been demonstrated experimentally with the impact on the performance evaluated. As a result a wide range of factors affecting the CSI installed power and harmonic performance have been investigated in simulation as well as experimentally.

9.3. Areas of Future Improvement and Investigation

This investigation has only addressed a small number of aspects which would need to be scrutinised before the hybrid system can be utilised at the intended MV levels. The work undertaken as part of this PhD thesis has proven the validity of the CSI as a solution for improving the large current distortion created by the VSI 1 kHz switching frequency while also benefiting from a significant voltage stress reduction which indicates a cost effective alternative for harmonic improvement. As a first step in the evolution of this circuit, a generic design guideline has been proposed which could be further refined. A more advanced methodology to determine analytically the optimal design point for Cs may be also possible as an improvement to the numerical investigation done in this work. The consideration of the virtual harmonic content produced by the VSI, as previously demonstrated in LCL filter design could be one approach.

Perhaps the most essential development for the Hybrid system would be the improvement of the control approach taken in this project.

One major area which has been identified as critical and would produce significant improvement in the performance is the improvement in the method of VSI current ripple extraction. The use of a series capacitance in this application which can provide a large voltage reduction via a relatively small current as a method has also proven to be very sensitive to low order harmonic disturbances. The application of more advanced control solutions could be investigated which could guarantee good rejection of low order harmonics, good transient behaviour as well as meeting the requirement of extracting the relevant VSI switching harmonic amplitudes ranging from 700 Hz-5 kHz with negligible phase shift.

Additionally, future investigations could address the implementation of a more powerful digital control platform that would enable the experimental evaluation of the proposed resonant compensator or other closed loop control approaches needed for the experimental validation of using the hybrid approach as part of an existing MV converter with an LCL filter.

Further development steps could be the formal investigation of the hybrid system behaviour under large grid voltage unbalances. This is an area which has remained generally unexplored for series capacitor connected applications and offers opportunity for producing novel ideas during further exploration.

Other aspects that require investigation are the optimal sizing of the DC-link inductance, including also techniques for using magnetically biased inductances to reduce the size as well as optimal system sizing in terms of total system losses. These could also investigate more optimised operating strategies where the voltage reduction coefficient K or DC link current reference could be adjusted via an automatic control algorithm (similar to Maximum Power Point Tracking MPPT techniques) to meet minimum losses and or voltage stress or find other more favourable operating points.

One final aspect which should be addressed in a realistic implementation regards system start-up to a MV grid, without exceeding the maximum permitted CSI voltage. The start-up could follow a procedure in which initially, the CSI is completely shorted, resulting in the series capacitors to appear as star connected to the MV grid with the grid voltage dropping in full across them, followed by a controlled build-up of the CSI voltage to the chosen level (K%) without dangerous overshoots. Similarly these should focus on the possibility of current pre-charge from the AC side to the required DC-link reference level without an additional circuit. Another smaller aspect which could be investigated, is the modelling of the inrush current levels drawn by the combination of series capacitor and CSI AC filter caused by the connection to the grid voltage via a contactor (zero voltage to full grid AC voltage step).

Reference List

[1] H. A. B. Siddique, M. J. R. Ahmad, and R. W. D. Doncker, "Optimal control and filter sizing of a multi-megawatt medium-voltage voltage-source converter for future grids," in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016, pp. 1-8.

[2] M. R. I. Y. G. J. Zhu, "Power Converters for Medium Voltage Networks," 2014.

[3] F. Blaabjerg, M. Liserre, and K. Ma, "Power Electronics Converters for Wind Turbine Systems," *IEEE Transactions on Industry Applications*, vol. 48, pp. 708-719, 2012.

[4] B. Wu, *High-Power Converters and AC Drives*: Wiley-IEEE Press, 2006.

[5] N. Okada, M. Takasaki, J. Narushima, R. Miyagawa, and S. Katoh, "Series Connection of Snubberless IGBTs for 6.6 kV Transformerless Converters," in *Power Conversion Conference - Nagoya, 2007. PCC '07*, 2007, pp. 1686-1691.

[6] Y. H. L. Jos Arrillaga, Neville R. Watson, Nicholas J. Murray, *Self-Commutating Converters for High Power Applications*: Wiley 2009.

[7] E. P. Wiechmann, P. Aqueveque, R. Burgos, and J. Rodriguez, "On the Efficiency of Voltage Source and Current Source Inverters for High-Power Drives," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 1771-1782, 2008.

[8] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A Review of Passive Power Filters for Three-Phase Grid-Connected Voltage-Source Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, pp. 54-69, 2016.

[9] A. A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-Filter Design for a Multimegawatt Medium-Voltage Voltage-Source Inverter," *Industrial Electronics, IEEE Transactions on*, vol. 58, pp. 1205-1217, 2011.

[10] R. L. Sellick and M. Åkerberg, "Comparison of HVDC Light (VSC) and HVDC Classic (LCC) site aspects, for a 500MW 400kV HVDC transmission scheme," in *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, 2012, pp. 1-6.

[11] S. Bernet, "Recent developments of high power converters for industry and traction applications," *IEEE Transactions on Power Electronics*, vol. 15, pp. 1102-1117, 2000.

[12] S. Bernet, R. Teichmann, A. Zuckerberger, and P. K. Steimer, "Comparison of high-power IGBT's and hard-driven GTO's for high-power inverters," *IEEE Transactions on Industry Applications*, vol. 35, pp. 487-495, 1999.

[13] O. E. Oni, I. E. Davidson, and K. N. I. Mbangula, "A review of LCC-HVDC and VSC-HVDC technologies and applications," in *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, 2016, pp. 1-7.

[14] T. K. Vrana and S. Energi, "Review of HVDC component ratings: XLPE cables and VSC converters," in *2016 IEEE International Energy Conference (ENERGYCON)*, 2016, pp. 1-6.

[15] A. M. Abbas and P. W. Lehn, "PWM based VSC-HVDC systems — A review," in *2009 IEEE Power & Energy Society General Meeting*, 2009, pp. 1-9.

[16] H. Dirk Van, G.-B. Oriol, and L. Jun, "Comparison of HVAC and HVDC technologies," in *HVDC Grids:For Offshore and Supergrid of the Future*, ed: Wiley-IEEE Press, 2016, p. 528.

[17] G. Bathurst, G. Hwang, and L. Tejwani, "MVDC - The New Technology for Distribution Networks," in *AC and DC Power Transmission, 11th IET International Conference on*, 2015, pp. 1-5.

[18] M. Stieneker and R. W. D. Doncker, "Medium-voltage DC distribution grids in urban areas," in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016, pp. 1-7.

[19] J. C. Wiseman and W. Bin, "Active damping control of a high-power PWM current-source rectifier for line-current THD reduction," *Industrial Electronics, IEEE Transactions on*, vol. 52, pp. 758-764, 2005.
[20] Y. Suh, J. K. Steinke, and P. K. Steimer, "Efficiency Comparison of Voltage-Source and Current-Source Drive Systems for Medium-Voltage Applications," *IEEE Transactions on Industrial Electronics*, vol. 54, pp. 2521-2531, 2007.
[21] H. Soonwook, C. Venkatesh, and D. A. Torrey, "Series connection of IGBT's with active voltage balancing," *IEEE Transactions on Industry Applications*, vol. 35, pp. 917-923, 1999.
[22] A. N. Githiari and P. R. Palmer, "Analysis of IGBT modules connected in series," *IEE Proceedings - Circuits, Devices and Systems*, vol. 145, pp. 354-360, 1998.
[23] U. Schwarzer and R. W. D. Doncker, "Characterization of 6.5 kV IGBT modules for hard- and soft-switching operation in medium voltage applications," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, 2005, pp. 329-335 Vol. 1.
[24] F. Auerbach, J. G. Bauer, M. Glantschnig, J. Gottert, M. Hierholzer, A. Porst, *et al.*, "6.5 kV IGBT-modules," in *Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE*, 1999, pp. 1770-1774 vol.3.
[25] J. F. Donlon, E. R. Motto, E. Wiesner, E. Thal, K. Hatori, Y. Sakai, *et al.*, "The next generation 6.5kV IGBT," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 2897-2900.
[26] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2581-2596, 2010.
[27] A. Dutta and S. S. Ang, "Electromagnetic Interference Simulations for Wide-Bandgap Power Electronic Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, pp. 757-766, 2016.
[28] F. Filsecker, R. Alvarez, and S. Bernet, "The Investigation of a 6.5-kV, 1-kA SiC Diode Module for Medium Voltage Converters," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 2272-2280, 2014.
[29] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *Industry Applications, IEEE Transactions on*, vol. IA-17, pp. 518-523, 1981.
[30] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static VAr compensation," in *Industry Applications Society Annual Meeting, 1994., Conference Record of the 1994 IEEE*, 1994, pp. 921-928 vol.2.
[31] L. Jih-Sheng and P. Fang Zheng, "Multilevel converters-a new breed of power converters," *Industry Applications, IEEE Transactions on*, vol. 32, pp. 509-517, 1996.
[32] N. S. Choi, G. C. Cho, and G. H. Cho, "Modeling and analysis of a static VAR compensator using multilevel voltage source inverter," in *Industry Applications Society Annual Meeting, 1993., Conference Record of the 1993 IEEE*, 1993, pp. 901-908 vol.2.
[33] M. D. Manjrekar and T. A. Lipo, "A generalized structure of multilevel power converter," in *Power Electronic Drives and Energy Systems for Industrial Growth, 1998. Proceedings. 1998 International Conference on*, 1998, pp. 62-67 Vol.1.
[34] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Transactions on Industrial Electronics*, vol. 54, pp. 2930-2945, 2007.
[35] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A Survey on Cascaded Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2197-2206, 2010.
[36] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 492-501.
[37] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad, and I. Baraia, "Medium Voltage–High Power Converter Topologies Comparison Procedure, for a 6.6 kV

Drive Application Using 4.5 kV IGBT Modules," *IEEE Transactions on Industrial Electronics*, vol. 59, pp. 1462-1476, 2012.

[38] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "Comparison of Neutral-Point-Clamped, Symmetrical, and Hybrid Asymmetrical Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2297-2306, 2010.

[39] D. Krug, S. Bernet, and S. Dieckerhoff, "Comparison of state-of-the-art voltage source converter topologies for medium voltage applications," in *Industry Applications Conference, 2003. 38th IAS Annual Meeting. Conference Record of the*, 2003, pp. 168-175 vol.1.

[40] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and Comparison of 4-kV Neutral-Point-Clamped, Flying-Capacitor, and Series-Connected H-Bridge Multilevel Converters," *IEEE Transactions on Industry Applications*, vol. 43, pp. 1032-1040, 2007.

[41] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, "Medium voltage three-level converters for the grid connection of a multi-MW wind turbine," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-8.

[42] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Transactions on Industrial Electronics*, vol. 52, pp. 855-868, 2005.

[43] P. Barbosa, P. Steimer, J. Steinke, M. Winkelnkemper, and N. Celanovic, "Active-neutral-point-clamped (ANPC) multilevel converter technology," in *Power Electronics and Applications, 2005 European Conference on*, 2005, pp. 10 pp.-P.10.

[44] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2219-2230, 2010.

[45] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable Modular Multilevel Converters for HVDC-transmission," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 174-179.

[46] P. Sotoodeh and R. D. Miller, "Design and Implementation of an 11-Level Inverter With FACTS Capability for Distributed Energy Systems," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, pp. 87-96, 2014.

[47] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 30, pp. 4-17, 2015.

[48] G. Konstantinou, J. Zhang, S. Ceballos, J. Pou, and V. G. Agelidis, "Comparison and evaluation of sub-module configurations in modular multilevel converters," in *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, 2015, pp. 958-963.

[49] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics*, vol. 30, pp. 37-53, 2015.

[50] R. Teodorescu, F. Blaabjerg, M. Liserre, and A. Dell'Aquila, "A stable three-phase LCL-filter based active rectifier without damping," in *Industry Applications Conference, 2003. 38th IAS Annual Meeting. Conference Record of the*, 2003, pp. 1552-1557 vol.3.

[51] F. Huerta, S. Cobreces, E. Bueno, F. J. Rodriguez, F. Espinosa, and C. Giron, "Control of voltage source converters with LCL filter using state-space techniques," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, 2008, pp. 647-652.

[52] Y. Changzhou, Z. Xing, L. Fang, X. Haizhen, Q. Caixia, S. Zhangping, *et al.*, "A general active damping method based on capacitor voltage detection for grid-connected inverter," in *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, 2013, pp. 829-835.

[53] C. P. Dick, S. Richter, M. Rosekeit, J. Rolink, and R. W. De Doncker, "Active damping of LCL resonance with minimum sensor effort by means of a digital infinite impulse response filter," in *Power Electronics and Applications, 2007 European Conference on*, 2007, pp. 1-8.

[54] M. Liserre, A. Dell'Aquila, and F. Blaabjerg, "Stability improvements of an LCL-filter based three-phase active rectifier," in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, 2002, pp. 1195-1201 vol.3.

[55] M. Routimo and H. Tuusa, "LCL Type Supply Filter for Active Power Filter - Comparison of an Active and a Passive Method for Resonance Damping," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 2939-2945.

[56] Y. Shi and J. Su, "An active damping method based on PR control for LCL-filter-based grid-connected inverters," in *Electrical Machines and Systems (ICEMS), 2014 17th International Conference on*, 2014, pp. 944-948.

[57] M. Malinowski, W. Szczygiel, M. P. Kazmierkowski, and S. Bernet, "Sensorless operation of active damping methods for three-phase PWM converters," in *Proceedings of the IEEE International Symposium on Industrial Electronics, 2005. ISIE 2005.*, 2005, pp. 775-780 vol. 2.

[58] S. Takahiro, H. Iura, S. Matsuda, Y. Takase, S. Morimoto, and K. Ide, "Robust active damping technique for three-phase PWM converter connected to power grid with unknown inductance," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 739-744.

[59] S. N. Usluer and A. M. Hava, "Investigation on series active filter compensated high power grid-connected voltage source inverters with LCL filter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 381-388.

[60] J. San-Sebastian, I. Etxeberria-Otadui, A. Rujas, J. A. Barrena, and P. Rodriguez, "Optimized LCL filter design methodology applied to MV grid-connected multimegawatt VSC," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 2506-2512.

[61] P. N. Enjeti, P. D. Ziogas, and J. F. Lindsay, "Programmed PWM techniques to eliminate harmonics - A critical evaluation," in *Industry Applications Society Annual Meeting, 1988., Conference Record of the 1988 IEEE*, 1988, pp. 418-430 vol.1.

[62] P. N. Enjeti, P. D. Ziogas, and J. F. Lindsay, "A current source PWM inverter with instantaneous current control capability," *Industry Applications, IEEE Transactions on*, vol. 27, pp. 582-588, 1991.

[63] P. N. Enjeti, P. D. Ziogas, and J. F. Lindsay, "Programmed PWM techniques to eliminate harmonics: a critical evaluation," *IEEE Transactions on Industry Applications*, vol. 26, pp. 302-316, 1990.

[64] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications," *IEEE Transactions on Power Electronics*, vol. 30, pp. 4091-4106, 2015.

[65] H. R. Karshenas, H. A. Kojori, S. B. Dewan, and J. H. Choi, "Generalized techniques of selective harmonic elimination and current control in current source inverters/converters," in *Applied Power Electronics Conference and Exposition, 1994. APEC '94. Conference Proceedings 1994., Ninth Annual*, 1994, pp. 107-114 vol.1.

[66] M. S. A. Dahidah and V. G. Agelidis, "Selective Harmonic Elimination PWM Control for Cascaded Multilevel Voltage Source Converters: A Generalized Formula," *IEEE Transactions on Power Electronics*, vol. 23, pp. 1620-1630, 2008.

[67] M. Moranchel, E. J. Bueno, F. J. Rodriguez, and I. Sanz, "Selective Harmonic Elimination modulation for Medium Voltage Modular Multilevel Converter," in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016, pp. 1-6.

[68] H. Le-Huy, R. Perret, and R. Feuillet, "Minimization of Torque Ripple in Brushless DC Motor Drives," *IEEE Transactions on Industry Applications*, vol. IA-22, pp. 748-755, 1986.

[69] J. R. Espinoza, G. Joos, J. I. Guzman, L. A. Moran, and R. P. Burgos, "Selective harmonic elimination and current/voltage control in current/voltage-source topologies: a unified approach," *Industrial Electronics, IEEE Transactions on*, vol. 48, pp. 71-81, 2001.

[70] Y. Zhang, Y. W. Li, N. R. Zargari, and Z. Cheng, "Improved Selective Harmonics Elimination Scheme With Online Harmonic Compensation for High-Power PWM Converters," *IEEE Transactions on Power Electronics,* vol. 30, pp. 3508-3517, 2015.

[71] M. Zabaleta, E. Burguete, D. Madariaga, I. Zubimendi, M. Zubiaga, and I. Larrazabal, "<italic>LCL</italic> Grid Filter Design of a Multimegawatt Medium-Voltage Converter for Offshore Wind Turbine Using SHEPWM Modulation," *IEEE Transactions on Power Electronics,* vol. 31, pp. 1993-2001, 2016.

[72] H. Akagi, "New trends in active filters for improving power quality," in *Power Electronics, Drives and Energy Systems for Industrial Growth, 1996., Proceedings of the 1996 International Conference on*, 1996, pp. 417-425 vol.1.

[73] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," *IEEE Transactions on Industrial Electronics,* vol. 46, pp. 960-971, 1999.

[74] T. C. Green and J. H. Marks, "Control techniques for active power filters," *IEE Proceedings - Electric Power Applications,* vol. 152, pp. 369-381, 2005.

[75] T. C. Green and J. H. Marks, "Ratings of active power filters," *IEE Proceedings - Electric Power Applications,* vol. 150, pp. 607-614, 2003.

[76] C. Rech, H. Pinheiro, H. A. Grundling, H. L. Hey, and J. R. Pinheiro, "Analysis and comparison of hybrid multilevel voltage source inverters," in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, 2002, pp. 491-496 vol.2.

[77] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Transactions on Industry Applications,* vol. 41, pp. 655-664, 2005.

[78] S. Fukuda, T. Yoshida, and S. Ueda, "Control Strategies of a Hybrid Multilevel Converter for Expanding Adjustable Output Voltage Range," *IEEE Transactions on Industry Applications,* vol. 45, pp. 827-835, 2009.

[79] C. A. Silva, L. A. Cordova, P. Lezana, and L. Empringham, "Implementation and Control of a Hybrid Multilevel Converter With Floating DC Links for Current Waveform Improvement," *IEEE Transactions on Industrial Electronics,* vol. 58, pp. 2304-2312, 2011.

[80] R. Geun-Hie, K. Iouri, K. Won-Ho, and K. Jong-Soo, "A shunt hybrid active filter with two passive filters in tandem," in *Applied Power Electronics Conference and Exposition, 1996. APEC '96. Conference Proceedings 1996., Eleventh Annual*, 1996, pp. 361-366 vol.1.

[81] D. Detjen, J. Jacobs, R. W. De Doncker, and H. G. Mall, "A new hybrid filter to dampen resonances and compensate harmonic currents in industrial power systems with power factor correction equipment," *Power Electronics, IEEE Transactions on,* vol. 16, pp. 821-827, 2001.

[82] R. Inzunza and H. Akagi, "A 6.6-kV transformerless shunt hybrid active filter for installation on a power distribution system," *Power Electronics, IEEE Transactions on,* vol. 20, pp. 893-900, 2005.

[83] R. Inzunza and H. Akagi, "A 6.6-kV transformerless shunt hybrid active filter for installation on a power distribution system," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 4630-4636 Vol.6.

[84] V. F. Corasaniti, M. B. Barbieri, P. L. Arnera, and M. I. Valla, "Hybrid Power Filter to Enhance Power Quality in a Medium-Voltage Distribution Network," *IEEE Transactions on Industrial Electronics,* vol. 56, pp. 2885-2893, 2009.

[85] H. Akagi and R. Kondo, "A Transformerless Hybrid Active Filter Using a Three-Level Pulsewidth Modulation (PWM) Converter for a Medium-Voltage Motor Drive," *IEEE Transactions on Power Electronics,* vol. 25, pp. 1365-1374, 2010.

[86] H. Akagi and T. Hatada, "Voltage Balancing Control for a Three-Level Diode-Clamped Converter in a Medium-Voltage Transformerless Hybrid Active Filter," *IEEE Transactions on Power Electronics,* vol. 24, pp. 571-579, 2009.

[87] H. Akagi and T. Hatada, "Voltage Balancing Control for a Three-Level Diode-Clamped Converter in a Medium-Voltage Transformerless Hybrid Active Filter," *Power Electronics, IEEE Transactions on,* vol. 24, pp. 571-579, 2009.

[88] C.-S. Lam, Wong, Man-Chung, *Design and Control of Hybrid Active Power Filters*, 1 ed.: Springer-Verlag Berlin Heidelberg, 2014.
[89] C. S. Lam, M. C. Wong, and Y. D. Han, "Hysteresis current control of hybrid active power filters," *IET Power Electronics*, vol. 5, pp. 1175-1187, 2012.
[90] E. Durna, "Effect of sampling frequency and execution time on hysteresis current controlled three-phase three-wire HAPF converters," in *2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2016, pp. 817-824.
[91] L. Wang, C. S. Lam, and M. C. Wong, "An Unbalanced Control Strategy for a Thyristor Controlled LC-Coupling Hybrid Active Power Filter (TCLC-HAPF) in Three-phase Three-wire Systems," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1-1, 2016.
[92] S. Rahmani, A. Hamadi, K. Al-Haddad, and L. A. Dessaint, "A Combination of Shunt Hybrid Power Filter and Thyristor-Controlled Reactor for Power Quality," *Industrial Electronics, IEEE Transactions on*, vol. 61, pp. 2152-2164, 2014.
[93] W. Lei, C. S. Lam, and M. C. Wong, "Hardware and software design of a low DC-link voltage and wide compensation range thyristor controlled LC-coupling hybrid active power filter," in *TENCON 2015 - 2015 IEEE Region 10 Conference*, 2015, pp. 1-4.
[94] W. Yang-Wen, W. Man-Chung, and L. Chi-Seng, "Historical review of parallel hybrid active power filter for power quality improvement," in *TENCON 2015 - 2015 IEEE Region 10 Conference*, 2015, pp. 1-6.
[95] P. Parkatti, M. Salo, and H. Tuusa, "A Novel Vector Controlled Current Source Shunt Active Power Filter with Reduced Component Voltage Stresses," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 1121-1125.
[96] P. Parkatti, M. Salo, and H. Tuusa, "Modeling and measuring results of a shunt current source active power filter with series capacitor," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 201-206.
[97] P. Parkatti and H. Tuusa, "Comparison of active power filters with series-connected capacitor," in *Power and Energy Conference, 2008. PECon 2008. IEEE 2nd International*, 2008, pp. 329-334.
[98] P. Parkatti, M. Salo, and H. Tuusa, "Experimental results for a current source shunt active power filter with series capacitor," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 3814-3818.
[99] C. Photong, C. Klumpner, and P. Wheeler, "A current source inverter with series connected AC capacitors for photovoltaic application with grid fault ride through capability," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, 2009, pp. 390-396.
[100] Y. Sato, K. Kawamura, H. Morimoto, and K. Nezu, "Hybrid PWM rectifiers to reduce electromagnetic interference," in *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, 2002, pp. 2141-2146 vol.3.
[101] D. Jiang and F. Wang, "Current-Ripple Prediction for Three-Phase PWM Converters," *IEEE Transactions on Industry Applications*, vol. 50, pp. 531-538, 2014.
[102] G. Grandi, J. Loncarski, and O. Dordevic, "Analysis and Comparison of Peak-to-Peak Current Ripple in Two-Level and Multilevel PWM Inverters," *IEEE Transactions on Industrial Electronics*, vol. 62, pp. 2721-2730, 2015.
[103] S. Tewari, K. Basu, and A. Somani, "Analytical evaluation of the peak-to-peak ripple current in the filter inductor for a space vector modulated grid-tied VSI," in *Power Electronics, Drives and Energy Systems (PEDES), 2014 IEEE International Conference on*, 2014, pp. 1-6.
[104] D. L. Holmes, T., *Pulse Width Modulation for Power Converters:Principles and Practice*: Wiley-IEEE Press 2003
[105] B. S. Institution, "BS IEC 61000-3-4:1998 Electromagnetic compatibility (EMC). Limits. Limitation of emission of harmonic currents in low-voltage power supply systems for equipment with rated current greater than 16 A," ed, 1998.
[106] B. S. Institution, "BS EN 61000-3-3:2008 Electromagnetic compatibility (EMC). Limits. Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage

supply systems, for equipment with rated current ≤ 16 A per phase and not subject to conditional connection," ed, 2008.
[107] E. N. Association, "Engineering Recommendation G5/4-1 : Planning Levels for harmonic Voltage Distortion and the Connection of Non-Linear Equipment to Transmission Systems and Distribution Networks in the United Kingdom," ed, 2005.
[108] W. Xing, X. Lan, Y. Zhilei, and G. Chunying, "Design of LCL filter for wind power inverter," in *World Non-Grid-Connected Wind Power and Energy Conference (WNWEC), 2010*, 2010, pp. 1-6.
[109] S. G. F. W. Fuchs, "Effect of wind-energy power injection into weak grids," *Proc of EWEA'12,* p. pp.1204, 2012.
[110] IXYS. (2005). *DSEP 30-12AR HiPerFREDTM Epitaxial Diode with soft recovery Datasheet*. Available: http://ixapps.ixys.com/DataSheet/L189.pdf
[111] A. Technologies. (2016). *HCNW3120 2.5 Amp Output Current IGBT Gate Drive Optocoupler Datasheet*. Available: http://docs.avagotech.com/docs/AV02-0161EN
[112] IXYS. (2006). *IXDR 30N120 D1 High Voltage IGBT with optional Diode ISOPLUS package Datasheet*. Available: http://ixapps.ixys.com/DataSheet/IXDR30N120_IXDR30N120D1.pdf
[113] A. Technologies. (2012). *ACNW3190 5.0 Amp High Output Current IGBT Gate Drive Optocoupler Datasheet*. Available: http://docs.avagotech.com/docs/AV02-0598EN
[114] IXYS. (2009). *MUBW 50-17 T8 Converter - Brake - Inverter Module (CBI) with Trench IGBT technology Datasheet*. Available: http://ixapps.ixys.com/DataSheet/MUBW50-17T8.pdf
[115] L. Malesani, L. Rossetto, P. Tenti, and P. Tomasin, "AC/DC/AC PWM converter with minimum energy storage in the DC link," in *Applied Power Electronics Conference and Exposition, 1993. APEC '93. Conference Proceedings 1993., Eighth Annual*, 1993, pp. 306-311.
[116] STmicroelectronics. (2002). *STTA812D/DI/G TURBOSWITCH ULTRA-FAST HIGH VOLTAGE DIODE Datasheet*. Available: www.st.com/resource/en/datasheet/CD00000747.pdf
[117] T. connectivity. (2011). *TE1500B47RJ RESISTOR 1500W 47R Datasheet*. Available: http://www.farnell.com/datasheets/1468562.pdf?_ga=1.199877223.838269378.1464088202
[118] G. Grandi and J. Loncarski, "Evaluation of current ripple amplitude in three-phase PWM voltage source inverters," in *Compatibility and Power Electronics (CPE), 2013 8th International Conference on*, 2013, pp. 156-161.
[119] A. J. Watson, H. Dang, G. Mondal, J. C. Clare, and P. W. Wheeler, "Experimental implementation of a multilevel converter for power system integration," in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 2232-2238.
[120] J. Clare, "Advanced power converters for universal and flexible power management in future electricity networks," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-29.
[121] J. Espinoza and G. Joos, "On-line generation of gating signals for current source converter topologies," in *Industrial Electronics, 1993. Conference Proceedings, ISIE'93 - Budapest., IEEE International Symposium on*, 1993, pp. 674-678.
[122] J. R. Espinoza, G. Joos, J. Guzman, and L. A. Moran, "Real-time implementation of a generalized approach for SHE and fundamental current control in current source topologies," in *Power Electronics Congress, 2000. CIEP 2000. VII IEEE International*, 2000, pp. 21-26.
[123] LEM. (2014). *Voltage transducer LV 25-P Datasheet*. Available: www.lem.com/docs/products/lv_25-p.pdf
[124] LEM. (2015). *LA 55-P Current Transducer Datasheet*. Available: http://www.lem.com/docs/products/la_55-p_e.pdf
[125] T. Instruments. (2005). *TMS320C6713 Floating-point Digital Signal Processor Datasheet*. Available: www.ti.com/lit/ds/symlink/tms320c6713.pdf

[126] T. Lecroy. (2011). *HRO 64Zi 12-bit High Resolution Oscilloscope Datasheet*. Available: http://teledynelecroy.com/doc/docview.aspx?id=8633

[127] LeCroy. (2015). *Lecroy Current Probe CP030 CP150 Datasheet* Available: http://teledynelecroy.com/doc/docview.aspx?id=9262

[128] N. 4th. (2012). *N4L APPLICATION NOTE - 014 : 3 Phase 2 Wattmeter Power Application Note*. Available: http://www.newtons4th.com/wp-content/uploads/2010/03/APP014-3-Phase-2-Wattmeter-Explained.pdf

[129] P. Technology. (2016). *TC-08 THERMOCOUPLE DATA LOGGER Datasheet*. Available: https://www.picotech.com/download/datasheets/usb-tc-08-thermocouple-data-logger-data-sheet.pdf

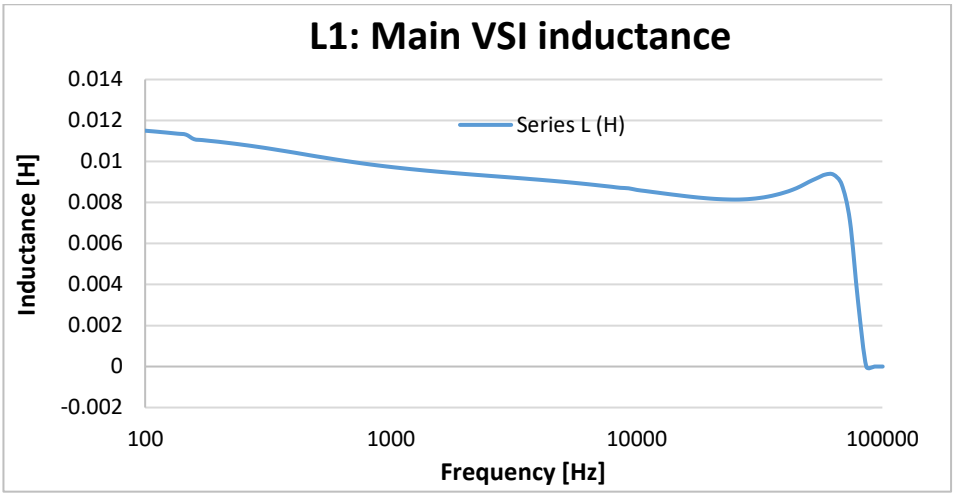
[130] Fluke. (2009). *Fluke Ti25 Thermal Imager Datasheet*. Available: http://assets.fluke.com/appNotes/TI/3035356D_w_Ti25_Ti10_Ti9%20Data%20Sheet.pdf

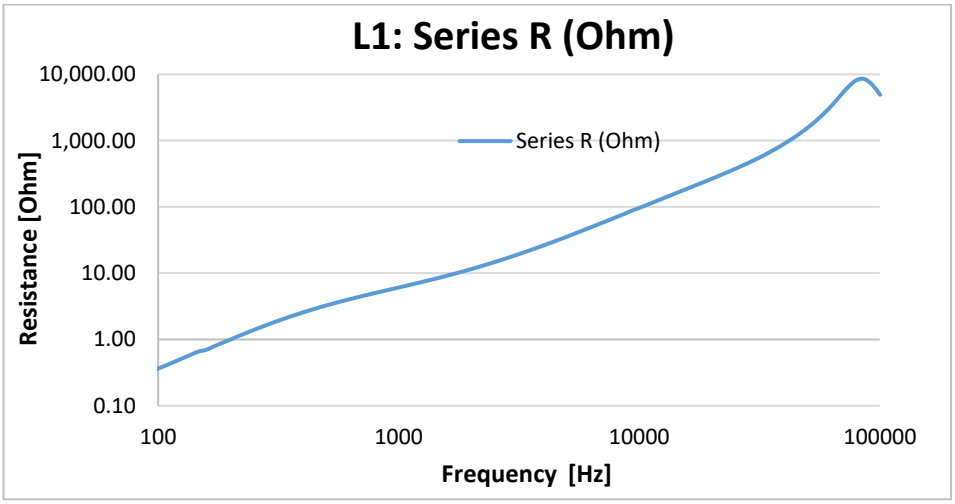
[131] M. Jankovic, A. Costabeber, A. Watson, and J. Clare, "Control of a grid connected modular multilevel converter under pulsed DC load," in *Industrial Electronics Society, IECON 2015 - 41st Annual Conference of the IEEE*, 2015, pp. 002526-002531.

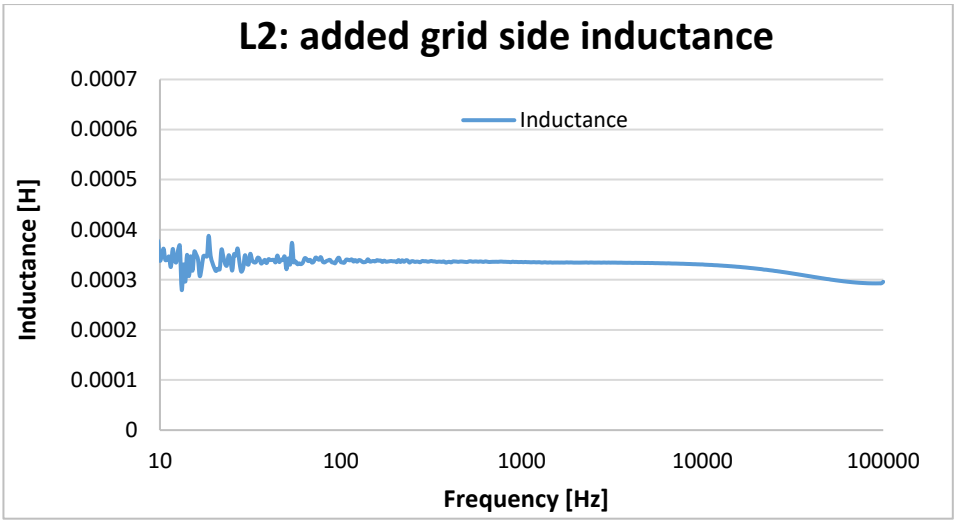
[132] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control," *Power Electronics, IEEE Transactions on*, vol. 22, pp. 584-592, 2007.

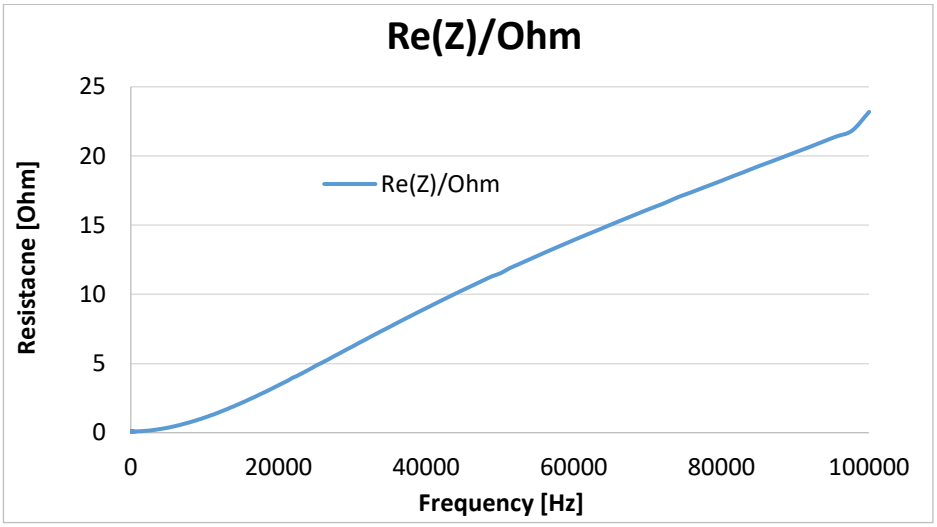
Appendix A. Inductor Characterisation Data

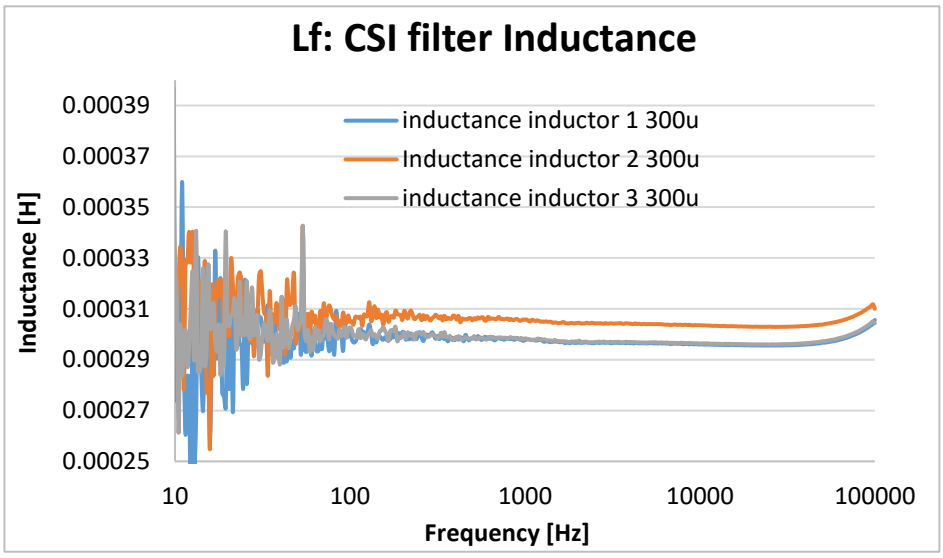
The following inductance characteristics have been achieved using small signal analysis performed using dedicated equipment:

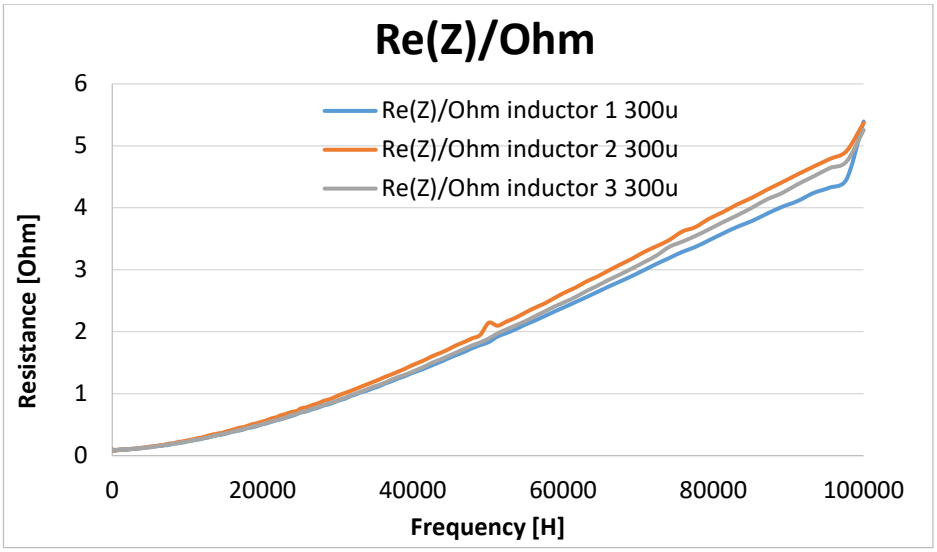


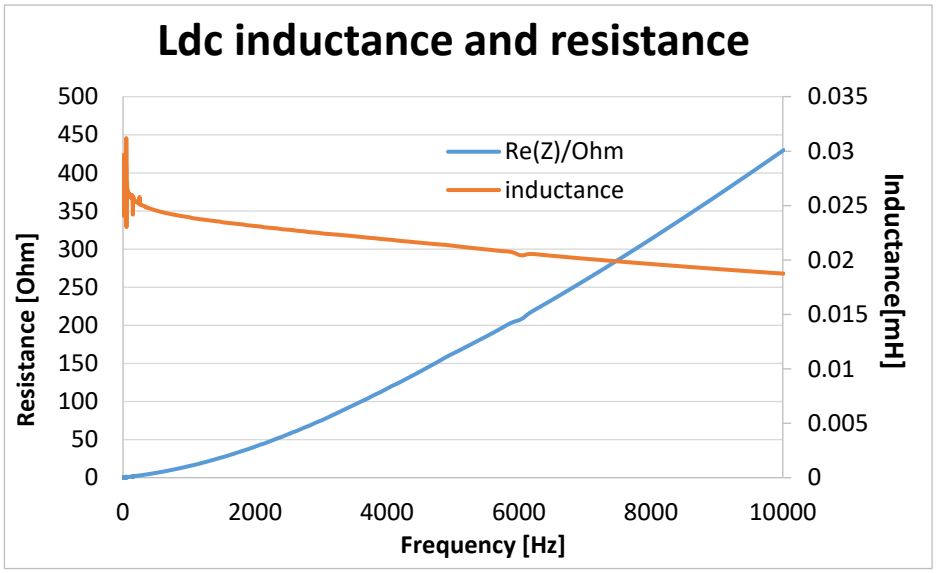



L2: added grid side inductance
Inductance [H]
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
Inductance
10
100
1000
10000
100000
Frequency [Hz]


Re(Z)/Ohm
Resistacne [Ohm]
25
20
15
10
5
0
Re(Z)/Ohm
0
20000
40000
60000
80000
100000
Frequency [Hz]


Lf: CSI filter Inductance
Inductance [H]
0.00039
0.00037
0.00035
0.00033
0.00031
0.00029
0.00027
0.00025
inductance inductor 1 300u
Inductance inductor 2 300u
inductance inductor 3 300u
10
100
1000
10000
100000
Frequency [Hz]


Re(Z)/Ohm
Re(Z)/Ohm inductor 1 300u
Re(Z)/Ohm inductor 2 300u
Re(Z)/Ohm inductor 3 300u
Resistance [Ohm]
Frequency [H]
0
1
2
3
4
5
6
0
20000
40000
60000
80000
100000


Ldc inductance and resistance
Re(Z)/Ohm
inductance
Resistance [Ohm]
Inductance[mH]
Frequency [Hz]
0
50
100
150
200
250
300
350
400
450
500
0
2000
4000
6000
8000
10000
0
0.005
0.01
0.015
0.02
0.025
0.03
0.035

Appendix B. State Space Models

STATE SPACE MODELS

The following state space models have been used to model the single phase equivalent circuit behaviour which can then be used to obtain the open loop passive component response or manipulated further to enable the design of the closed loop system response.

For each circuit configuration considered the matrices A, x, B and u are presented where the state space solution can be computed as:

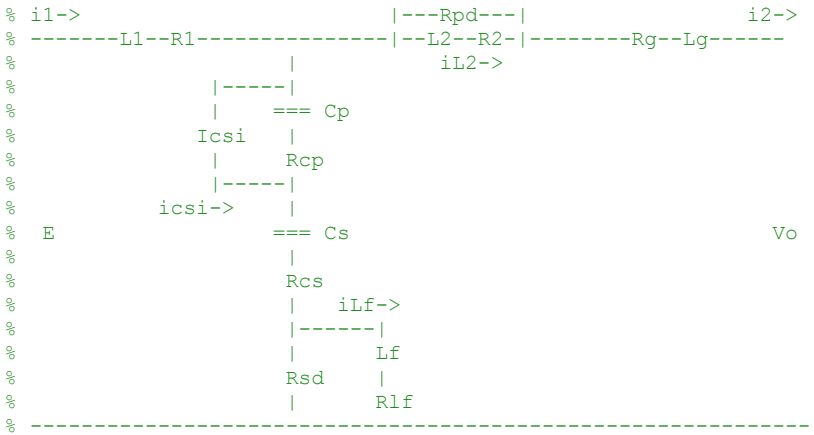
$$[\dot{x}] = [A][x] + [B][u]$$

And the output matrix equation is

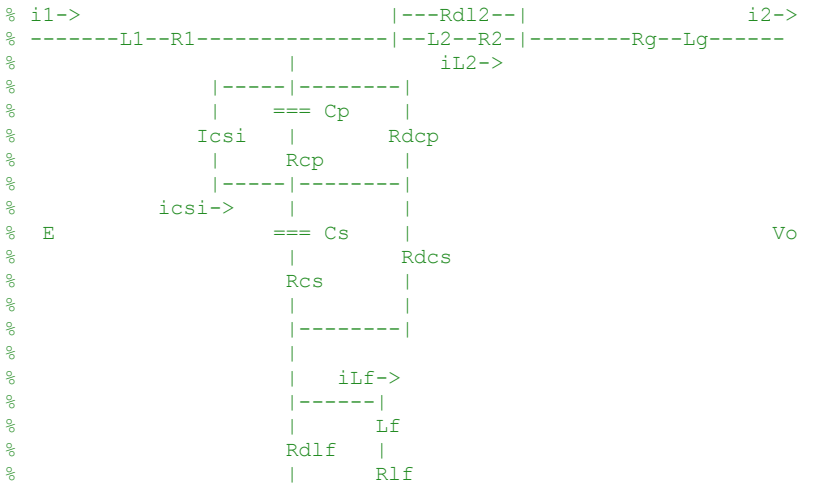
$$[\dot{y}] = [C][x] + [D][u]$$

Where C is the identity matrix of equal dimensions to matrix A

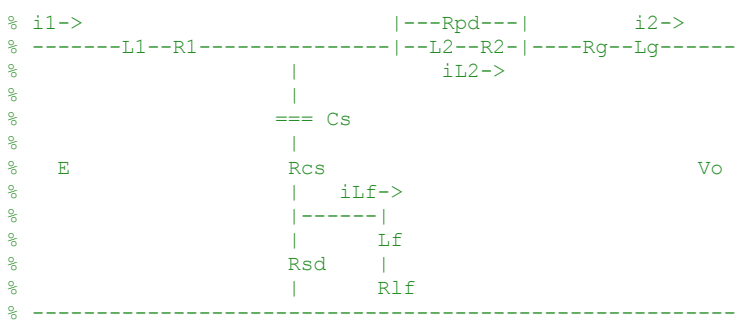
and D is a matrix of zeros (for open loop response) equal to the dimensions of matrix B



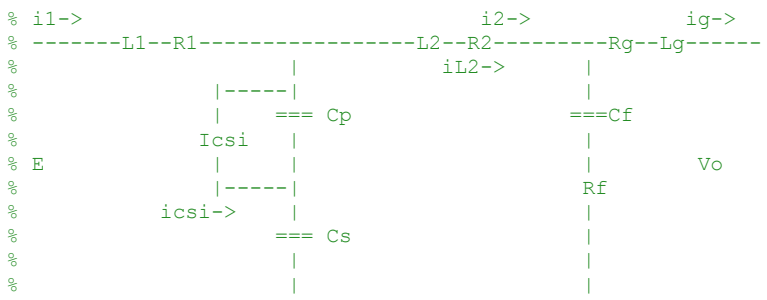
$$A=\begin{bmatrix} -\frac{(R_1+R_{cp}+R_{cs}+R_{sd})}{L_1} & \frac{(R_{cp}+R_{cs}+R_{sd})}{L_1} & 0 & \frac{R_{sd}}{L_1} & -\frac{1}{L_1} & -\frac{1}{L_1} \\ \frac{(R_{cp}+R_{cs}+R_{sd})}{L_g} & -\frac{(R_{cp}+R_{cs}+R_g+R_{pd}+R_{sd})}{L_g} & \frac{R_{pd}}{L_g} & -\frac{R_{sd}}{L_g} & \frac{1}{L_g} & \frac{1}{L_g} \\ 0 & \frac{R_{pd}}{L_2} & -\frac{(R_2+R_{pd})}{L_2} & 0 & 0 & 0 \\ \frac{R_{sd}}{L_f} & -\frac{R_{sd}}{L_f} & 0 & -\frac{(R_{lf}+R_{sd})}{L_f} & 0 & 0 \\ \frac{1}{C_s} & -\frac{1}{C_s} & 0 & 0 & 0 & 0 \\ \frac{1}{C_p} & -\frac{1}{C_p} & 0 & 0 & 0 & 0 \end{bmatrix} \quad x=\begin{bmatrix} i_1 \\ i_2 \\ i_{L_2} \\ i_{L_f} \\ V_{C_s} \\ V_{C_p} \end{bmatrix} \quad B=\begin{bmatrix} \frac{1}{L_1} & 0 & \frac{R_{cp}}{L_1} \\ 0 & -\frac{1}{L_g} & -\frac{R_{cp}}{L_g} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_p} \end{bmatrix} \quad u=\begin{bmatrix} E \\ V_o \\ i_{csi} \end{bmatrix}$$



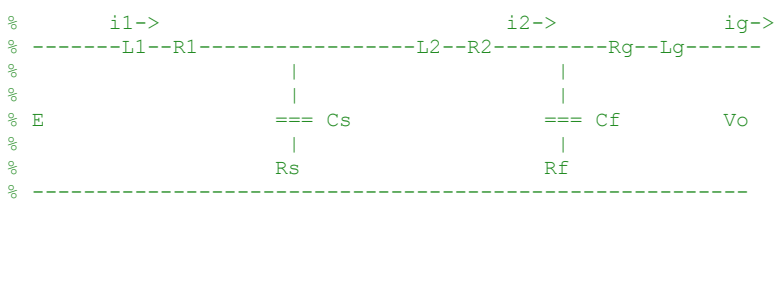
$$A=\begin{bmatrix} -\frac{\left(R_1+\frac{(R_{cp}*R_{dcp})}{(R_{cp}+R_{dcp})}+\frac{(R_{cs}*R_{dcs})}{(R_{cs}+R_{dcs})}+R_{dlf}\right)}{L_1} & \frac{\left(R_{dlf}+\frac{(R_{cp}*R_{dcp})}{(R_{cp}+R_{dcp})}+\frac{(R_{cs}*R_{dcs})}{(R_{cs}+R_{dcs})}\right)}{L_1} & 0 & \frac{R_{dlf}}{L_1} & -\frac{R_{dcs}}{L_1(R_{cs}+R_{dcs})} & -\frac{R_{dcp}}{L_1(R_{cp}+R_{dcp})} \\ \frac{\left(R_{dlf}+\frac{(R_{cp}*R_{dcp})}{(R_{cp}+R_{dcp})}+\frac{(R_{cs}*R_{dcs})}{(R_{cs}+R_{dcs})}\right)}{L_g} & -\frac{\left(R_{dl2}+R_{dlf}+R_g+\frac{(R_{cp}*R_{dcp})}{(R_{cp}+R_{dcp})}+\frac{(R_{cs}*R_{dcs})}{(R_{cs}+R_{dcs})}\right)}{L_g} & \frac{R_{dl2}}{L_g} & -\frac{R_{dlf}}{L_g} & \frac{R_{dcs}}{L_g(R_{cs}+R_{dcs})} & \frac{R_{dcp}}{L_g(R_{cp}+R_{dcp})} \\ 0 & \frac{R_{dl2}}{L_2} & -\frac{(R_2+R_{dl2})}{L_2} & 0 & 0 & 0 \\ \frac{R_{dlf}}{L_f} & -\frac{R_{dlf}}{L_f} & 0 & -\frac{(R_{lf}+R_{dlf})}{L_f} & 0 & 0 \\ \frac{R_{dcs}}{C_{s(R_{cs}+R_{dcs})}} & -\frac{R_{dcs}}{C_{s(R_{cs}+R_{dcs})}} & 0 & 0 & -\frac{1}{C_{s(R_{cs}+R_{dcs})}} & 0 \\ \frac{R_{dcp}}{C_{p(R_{cp}+R_{dcp})}} & -\frac{R_{dcp}}{C_{p(R_{cp}+R_{dcp})}} & 0 & 0 & 0 & -\frac{1}{C_{p(R_{cp}+R_{dcp})}} \end{bmatrix} \quad x=\begin{bmatrix} i_1 \\ i_2 \\ i_{L_2} \\ i_{L_f} \\ V_{C_s} \\ V_{C_p} \end{bmatrix} \quad B=\begin{bmatrix} \frac{1}{L_1} & 0 & \frac{(R_{cp}*R_{dcp})}{L_1(R_{cp}+R_{dcp})} \\ 0 & -\frac{1}{L_g} & -\frac{(R_{cp}*R_{dcp})}{L_g(R_{cp}+R_{dcp})} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{(R_{cp}*R_{dcp})}{C_p(R_{cp}+R_{dcp})} \end{bmatrix} \quad u=\begin{bmatrix} E \\ V_o \\ i_{csi} \end{bmatrix}$$



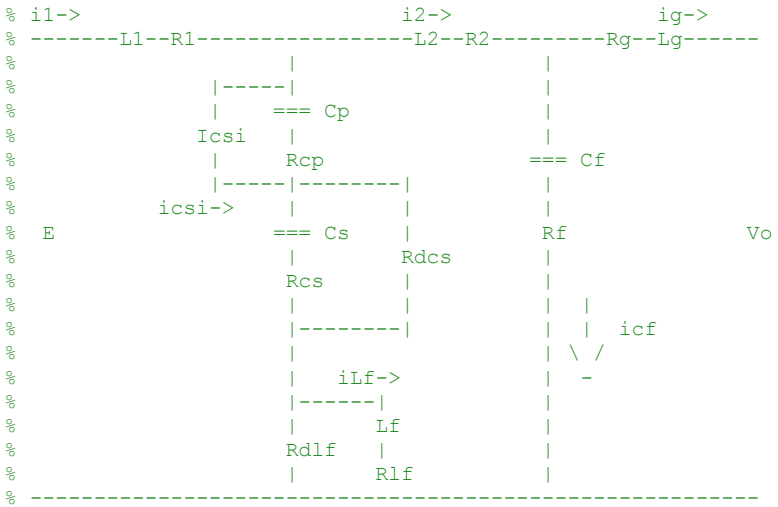
$$A=\begin{bmatrix} -\frac{(R_1+R_{cs}+R_{sd})}{L_1} & \frac{(R_{cs}+R_{sd})}{L_1} & 0 & \frac{R_{sd}}{L_1} & -\frac{1}{L_1} \\ \frac{(R_{cs}+R_{sd})}{L_g} & -\frac{(R_{cs}+R_g+R_{pd}+R_{sd})}{L_g} & \frac{R_{pd}}{L_g} & -\frac{R_{sd}}{L_g} & \frac{1}{L_g} \\ 0 & \frac{R_{pd}}{L_2} & -\frac{(R_2+R_{pd})}{L_2} & 0 & 0 \\ \frac{R_{sd}}{L_f} & -\frac{R_{sd}}{L_f} & 0 & -\frac{(R_{lf}+R_{sd})}{L_f} & 0 \\ \frac{1}{C_s} & -\frac{1}{C_s} & 0 & 0 & 0 \end{bmatrix} \quad x=\begin{bmatrix} i_1 \\ i_2 \\ i_{L_2} \\ i_{L_f} \\ V_{C_s} \end{bmatrix} \quad B=\begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & -\frac{1}{L_g} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad u=\begin{bmatrix} E \\ V_o \end{bmatrix}$$



$$A=\begin{bmatrix} -\frac{(R_1)}{L_1} & 0 & 0 & -\frac{1}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & -\frac{(R_f+R_g)}{L_g} & \frac{R_f}{L_g} & 0 & \frac{1}{L_g} & 0 \\ 0 & 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_s} & 0 & -\frac{1}{C_s} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_f} & \frac{1}{C_f} & 0 & 0 & 0 \\ \frac{1}{C_p} & 0 & -\frac{1}{C_p} & 0 & 0 & 0 \end{bmatrix} \quad x=\begin{bmatrix} i_1 \\ i_g \\ i_2 \\ V_{C_s} \\ V_{C_f} \\ V_{C_p} \end{bmatrix} \quad B=\begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & -\frac{1}{L_g} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_p} \end{bmatrix} \quad u=\begin{bmatrix} E \\ V_o \\ i_{csi} \end{bmatrix}$$



$$A=\begin{bmatrix} -\frac{(R_1+R_s)}{L_1} & 0 & \frac{R_s}{L_1} & -\frac{1}{L_1} & 0 \\ 0 & -\frac{(R_f+R_g)}{L_g} & \frac{R_f}{L_g} & 0 & \frac{1}{L_g} \\ \frac{R_s}{L_2} & \frac{R_f}{L_2} & -\frac{(R_2+R_f+R_s)}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_s} & 0 & -\frac{1}{C_s} & 0 & 0 \\ 0 & -\frac{1}{C_f} & \frac{1}{C_f} & 0 & 0 \end{bmatrix} \quad x=\begin{bmatrix} i_1 \\ i_g \\ i_2 \\ V_{C_s} \\ V_{C_f} \end{bmatrix} \quad B=\begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & -\frac{1}{L_g} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad u=\begin{bmatrix} E \\ V_o \end{bmatrix}$$



$$A=\begin{bmatrix} -\frac{\left(R_1+R_{cp}+R_{dlf}+\frac{(R_{cs}*R_{dcs})}{(R_{cs}+R_{dcs})}\right)}{L_1} & \frac{\left(R_{dlf}+R_{cp}+\frac{(R_{cs}*R_{dcs})}{(R_{cs}+R_{dcs})}\right)}{L_1} & 0 & \frac{R_{dlf}}{L_1} & \frac{\left(\frac{R_{cs}}{(R_{cs}+R_{dcs})}-1\right)}{L_1} & -\frac{1}{L_1} & 0 \\ \frac{\left(R_{dlf}+R_{cp}+\frac{(R_{cs}*R_{dcs})}{(R_{cs}+R_{dcs})}\right)}{L_2} & -\frac{\left(R_2+R_{dlf}+R_{cp}+R_f+\frac{(R_{cs}*R_{dcs})}{(R_{cs}+R_{dcs})}\right)}{L_2} & \frac{R_f}{L_2} & -\frac{R_{dlf}}{L_2} & -\frac{\left(\frac{R_{cs}}{(R_{cs}+R_{dcs})}-1\right)}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & \frac{R_f}{L_g} & -\frac{(R_f+R_g)}{L_g} & 0 & 0 & 0 & \frac{1}{L_g} \\ \frac{R_{dlf}}{L_f} & -\frac{R_{dlf}}{L_f} & 0 & -\frac{(R_{lf}+R_{dlf})}{L_f} & 0 & 0 & 0 \\ \frac{R_{dcs}}{C_s(R_{cs}+R_{dcs})} & -\frac{R_{dcs}}{C_s(R_{cs}+R_{dcs})} & 0 & 0 & -\frac{1}{C_s(R_{cs}+R_{dcs})} & 0 & 0 \\ \frac{1}{C_p} & -\frac{1}{C_p} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 & 0 & 0 \end{bmatrix} \quad x=\begin{bmatrix} i_1 \\ i_2 \\ i_{L_g} \\ i_{L_f} \\ V_{C_s} \\ V_{C_p} \\ V_{C_f} \end{bmatrix} \quad B=\begin{bmatrix} \frac{1}{L_1} & 0 & \frac{R_{cp}}{L_1} \\ 0 & 0 & -\frac{R_{cp}}{L_2} \\ 0 & -\frac{1}{L_g} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_p} \\ 0 & 0 & 0 \end{bmatrix} \quad u=\begin{bmatrix} E \\ V_o \\ i_{csi} \end{bmatrix}$$

Appendix C. Experimental Data

Key measurements for scope waveforms for phase A currents and voltages under different modes of operation for:
Chapter 6: 6.1.2. Operation with electronic AC voltage source

		Vcsi	Vc	Vgrid	Vdc
Before PWM activation	Max	308.887	29.7363	329.736	540.125
	Min	-309.668	-30.4443	-339.0870	532.477
	Mean	-0.7831	-0.7736	-4.1624	535.9962
	RMS	217.87	19.4745	236.2502	535.9969

		Vcsi	Vc	Vgrid	Vdc
Before ripple cancellation	Max	32.8125	340.112	330.859	760.242
	Min	-37.1826	-343.8720	-340.894	745.929
	Mean	-2.6363	0.5896	-4.2425	752.9231
	RMS	16.5193	240.8712	235.8122	752.9246

		Vcsi	Vc	Vgrid	Vdc
Full Hybrid operation	Max	63.5	374.37	332.1	758.6
	Min	-71.5	-368.53	-340.6	745.6
	Mean	-4.6	1.6	-3.8	753.1
	RMS	26.3	236.1	235.7	753.1

		Is	Ic	Igrid	Idc
Before PWM activation	Max	4.8887	0.1712	4.9967	0.1012
	Min	-5.0668	-0.1812	-5.0388	-0.1037
	Mean	-0.0741	-0.0137	0.0018	-0.0043
	RMS	3.1357	0.0707	3.1236	0.0243

		Is	Ic	Igrid	Idc
Before ripple cancellation	Max	12.2254	1.688	12.5134	5.3626*
	Min	-12.4435	-1.688	-12.5554	4.7179*
	Mean	-0.0231	0.0032	0.0236	4.9758
	RMS	5.9307	0.9027	6.0658	4.9761

		Is	Ic	Igrid	Idc
Full Hybrid operation	Max	12.6652	5.2002	9.2748	5.6175*
	Min	-12.0437	-5.0415	-9.3168	4.3218*
	Mean	-0.0416	-0.0029	0.0016	4.9999
	RMS	5.8862	1.8927	5.7891	5.0017

*measurement affected by noise

Chapter 7: 7.1.7. Grid Connected operation using negative sequence voltage compensator K=12%

		Vcsi	Vc	Vgrid	Vdc
Before PWM activation	Max	303.13	31.25	331.25	543.75
	Min	-306.25	-31.25	-328.125	525
	Mean	-1.09	0.3	1.88	532.8
	RMS	217.03	18.9	234.84	532.8

		Vcsi	Vc	Vgrid	Vdc
Before ripple cancellation	Max	37.5000	331.2500	328.1250	756.2500
	Min	-40.6250	-334.3750	-346.8750	731.2500
	Mean	-0.0834	0.9462	2.0176	744.0993
	RMS	15.7844	234.2688	234.0364	744.1054

		Vcsi	Vc	Vgrid	Vdc
Full Hybrid operation	Max	87.5000	378.1250	368.7500*	750.0000
	Min	-87.5000	-381.2500	-328.1250	731.2500
	Mean	-1.4691	1.2904	2.3608	742.2091
	RMS	31.0157	230.0947	234.3670	742.2157

		Is	Ic	Igrid	Idc
Before PWM activation	Max	4.9978	0.2899	4.9278	0.095
	Min	-4.9678	-0.2999	-4.8978	-0.04
	Mean	0.0200	-0.0054	0.0103	0.0281
	RMS	3.0570	0.0770	3.0410	0.0316

		Is	Ic	Igrid	Idc
Before ripple cancellation	Max	11.8547	1.7492	11.9746	5.7124*
	Min	-12.1446	-1.7592	-12.1546	4.2381*
	Mean	0.0382	0.0031	0.0208	4.9130
	RMS	5.9289	0.8648	6.0161	4.9132

		Is	Ic	Igrid	Idc
Full Hybrid operation	Max	11.6548	5.0078	9.1959	5.8574*
	Min	-11.8747	-4.7079	-8.8760	4.0132*
	Mean	0.0265	-0.0089	0.0058	4.9258
	RMS	5.8988	1.9363	5.7454	4.9314

*measurement affected by noise

Chapter 7: 7.2.2. Grid Connected operation with added grid inductance using negative sequence voltage compensator K=12% (Grid connected & filter)

		Vcsi	Vc	Vgrid	Vdc
Before PWM activation	Max	306.2500	31.2500	331.2500	543.7500
	Min	-306.2500	-28.1250	-328.1250	525.0000
	Mean	0.0347	0.5168	2.0523	534.1966
	RMS	217.5134	18.6520	235.3962	534.2061

		Vcsi	Vc	Vgrid	Vdc
Before ripple cancellation	Max	56.2500	328.1250	331.2500	762.5000
	Min	-56.2500	-331.2500	-328.1250	725.0000
	Mean	-0.1897	0.1047	2.6313	744.5874
	RMS	18.9868	231.3085	234.8894	744.5935

		Vcsi	Vc	Vgrid	Vdc
Full Hybrid operation	Max	87.5000	378.1250	328.1250	756.2500
	Min	-87.5000	-378.1250	-325.0000	725.0000
	Mean	-0.5674	0.7723	1.5191	743.7612
	RMS	31.9625	227.7367	234.7997	743.7673

		Is	Ic	Igrid	Idc
Before PWM activation	Max	4.9078	1.9691	12.2545	0.0950
	Min	-4.9178	-2.0091	-12.1346	-0.0450
	Mean	0.0032	-0.0015	0.0202	0.0188
	RMS	3.0431	0.9035	5.9937	0.0239

		Is	Ic	Igrid	Idc
Before ripple cancellation	Max	11.8047	1.9691	12.2545	5.6375*
	Min	-11.7247	-2.0091	-12.1346	4.3381*
	Mean	0.0357	-0.0015	0.0202	4.9460
	RMS	5.8784	0.9035	5.9937	4.9462

		Is	Ic	Igrid	Idc
Full Hybrid operation	Max	11.9546	5.0677	9.1659	5.9173*
	Min	-11.8147	-5.0477	-8.7761	3.9432*
	Mean	0.0487	0.0134	0.0364	4.9304
	RMS	5.8806	1.9281	5.7258	4.9364

*measurement affected by noise

Appendix D. THD Calculations

Ideal grid: THD of Phase A grid currents under full hybrid operation for different CSI switching frequencies

	40 kHz	33kHz	30 kHz	25 kHz	20 kHz
THD40	2.1909	1.8776	2.2320	3.3020	4.1547
THD40*	1.5485	1.0863	1.5318	3.1258	3.9928
THD100	2.7829	2.7440	2.9089	4.3697	5.7135
THD100*	1.5485	1.0863	1.5318	3.3666	4.8892
THD200	3.7623	3.9859	3.9370	5.1317	6.7845
THD200*	1.5485	1.0863	1.5318	3.3666	5.0257
THD1000	4.6899	5.3190	5.4939	6.8785	9.9015
THD1000*	1.5485	1.0863	1.8944	4.2027	7.6887

*ignoring harmonics with amplitude less than 1% of the fundamental harmonic

Ideal grid: THD of Phase A grid side currents prior to current ripple cancellation for different CSI switching frequencies

	40 kHz	33kHz	30 kHz	25 kHz	20 kHz
THD40	28.67	28.689	28.22	28.6173	28.5778
THD40*	28.6552	28.6739	28.2028	28.6026	28.56007
THD100	30.9586	30.972	30.4768	30.8785	30.8409
THD100*	30.9301	30.9414	30.4441	30.8486	30.8083
THD200	31.1003	31.1105	30.6159	31.0187	30.9818
THD200*	30.9489	30.9598	30.4627	30.8676	30.8268
THD1000	31.1197	31.1284	30.6341	31.0382	31.0002
THD1000*	30.9489	30.9598	30.4627	30.8676	30.8268

*ignoring harmonics with amplitude less than 1% of the fundamental harmonic

	Ideal grid		Real grid		Real Grid & filter	
	40kHz Is	40kHz Igrid	40kHz Is	40kHz Igrid	40kHz Is	40kHz Igrid
THD40	28.67	2.1909	28.6998	2.991	28.7956	2.8582
THD40*	28.6552	1.5485	28.666	2.5803	28.7525	2.4054
THD100	30.9586	2.7829	31.1421	3.3857	31.2183	3.4974
THD100*	30.9301	1.5485	31.0834	2.5803	31.1357	2.4054
THD200	31.1003	3.7623	31.2843	4.2614	31.3595	4.6185
THD200*	30.9489	1.5485	31.1061	2.5803	31.1582	2.7070
THD1000	31.1197	4.6899	31.3030	5.1515	31.3773	4.7411
THD1000*	30.9489	1.5485	31.1061	2.5803	31.1582	2.7070

*ignoring harmonics with amplitude less than 1% of the fundamental harmonic

Ideal grid: grid current three phase

	Before cancellation 40kHz			Full operation 40kHz		
	IgA	IgB	IgC	IgA	IgB	IgC
THD40	27.322	27.125	26.9742	2.3401	2.2014	2.2343
THD40*	27.3095	27.118	26.9603	1.9046	1.7772	1.8163
THD100	29.6484	29.4756	29.2699	2.8736	2.7521	2.7880
THD100*	29.6184	29.445	29.2382	1.9046	1.7772	1.8163
THD200	29.8073	29.6382	29.4278	3.7310	3.6488	3.7062
THD200*	29.6605	29.4862	29.2779	1.9046	1.7772	1.8163
THD1000	29.8742	29.7079	29.4933	4.5826	4.5678	4.5687
THD1000*	29.7149	29.544	29.3321	1.9046	1.7772	1.8163

*ignoring harmonics with amplitude less than 1% of the fundamental harmonic

Real grid: grid current three phase

	Before cancellation 40kHz			Full operation 40kHz		
	IgA	IgB	IgC	IgA	IgB	IgC
THD40	27.0048	27.0592	26.3901	2.5952	2.3328	2.3170
THD40*	26.9792	27.0202	26.3436	2.1026	1.5329	1.8920
THD100	29.3724	29.5192	28.7751	3.0344	2.7783	2.7710
THD100*	29.3724	29.4428	28.6919	2.1026	1.5329	1.8920
THD200	29.5882	29.6675	28.9202	3.9686	3.6695	3.7163
THD200*	29.396	29.4653	28.7136	2.1026	1.5329	1.8920
THD1000	29.6508	29.7356	28.9837	4.8168	4.6068	4.6100
THD1000*	29.4425	29.5168	28.7622	2.1026	1.5329	1.8920

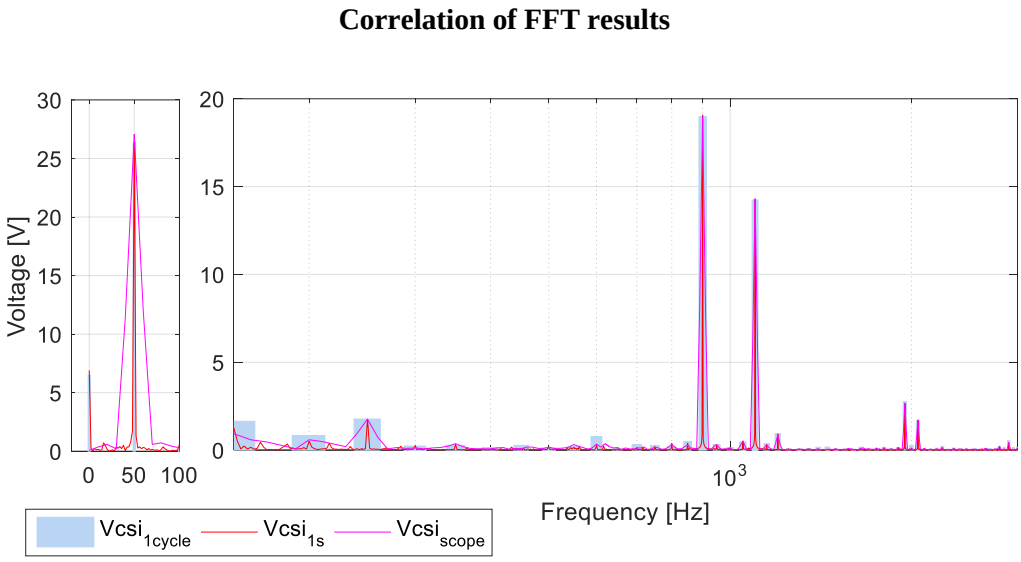
*ignoring harmonics with amplitude less than 1% of the fundamental harmonic

Real grid & filter: grid current three phase

	Before cancellation 40kHz			Full operation 40kHz		
	IgA	IgB	IgC	IgA	IgB	IgC
THD40	26.9684	27.0353	26.3378	2.7593	2.5151	2.4168
THD40*	26.841	26.9846	26.3034	2.4154	1.779	1.974
THD100	29.7994	29.9225	29.1260	3.38	3.1702	3.0702
THD100*	29.7272	29.8336	29.0473	2.4154	1.779	1.974
THD200	30.2680	30.4067	29.5727	4.5756	4.2626	4.2245
THD200*	30.1175	30.2352	29.4141	2.7706	2.0937	2.4491
THD1000	30.2762	30.4150	29.5811	4.6868	4.38700	4.3475
THD1000*	30.1175	30.2352	29.4141	2.7706	2.0937	2.4491

*ignoring harmonics with amplitude less than 1% of the fundamental harmonic

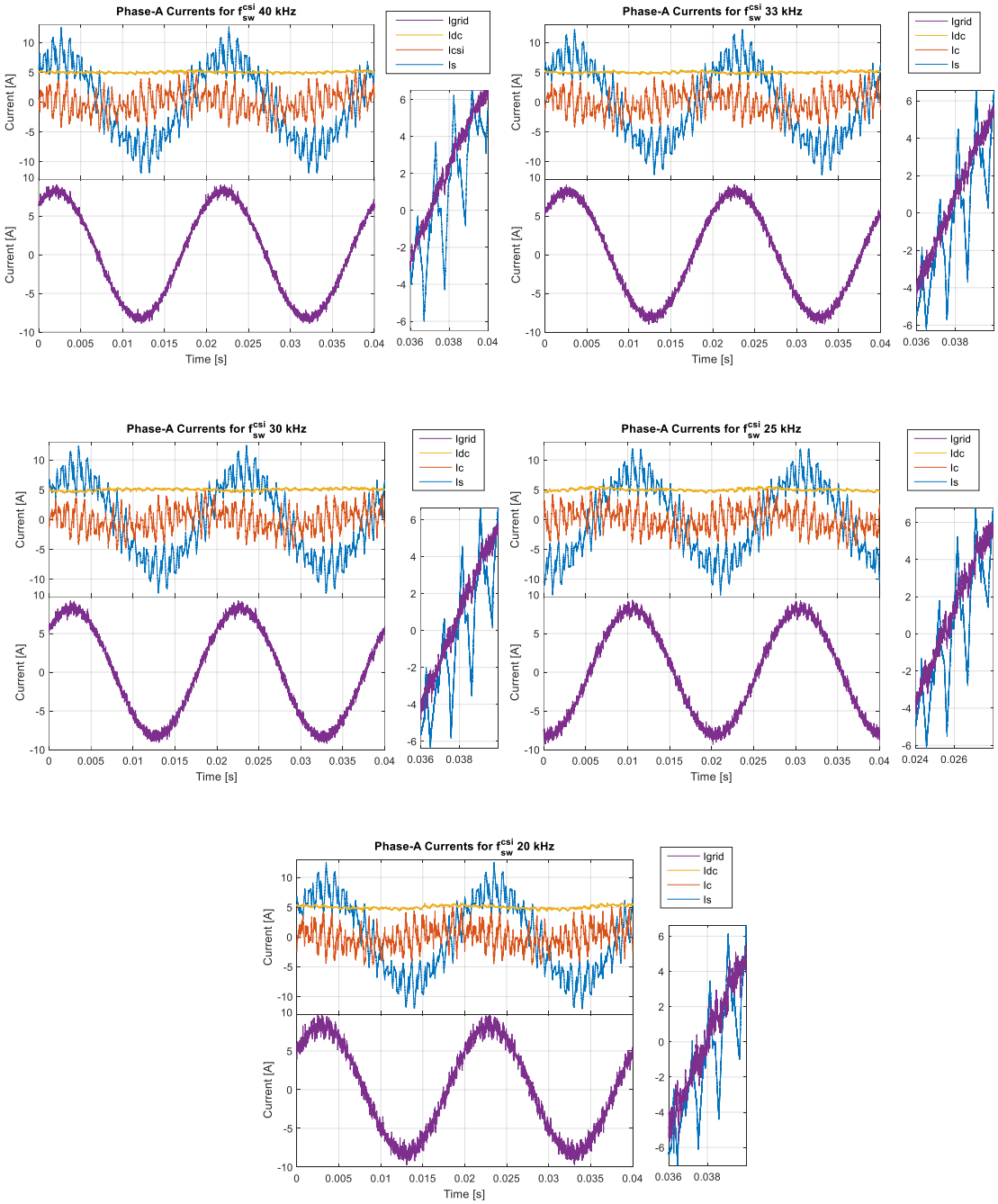
Appendix E. Additional Experimental Plots



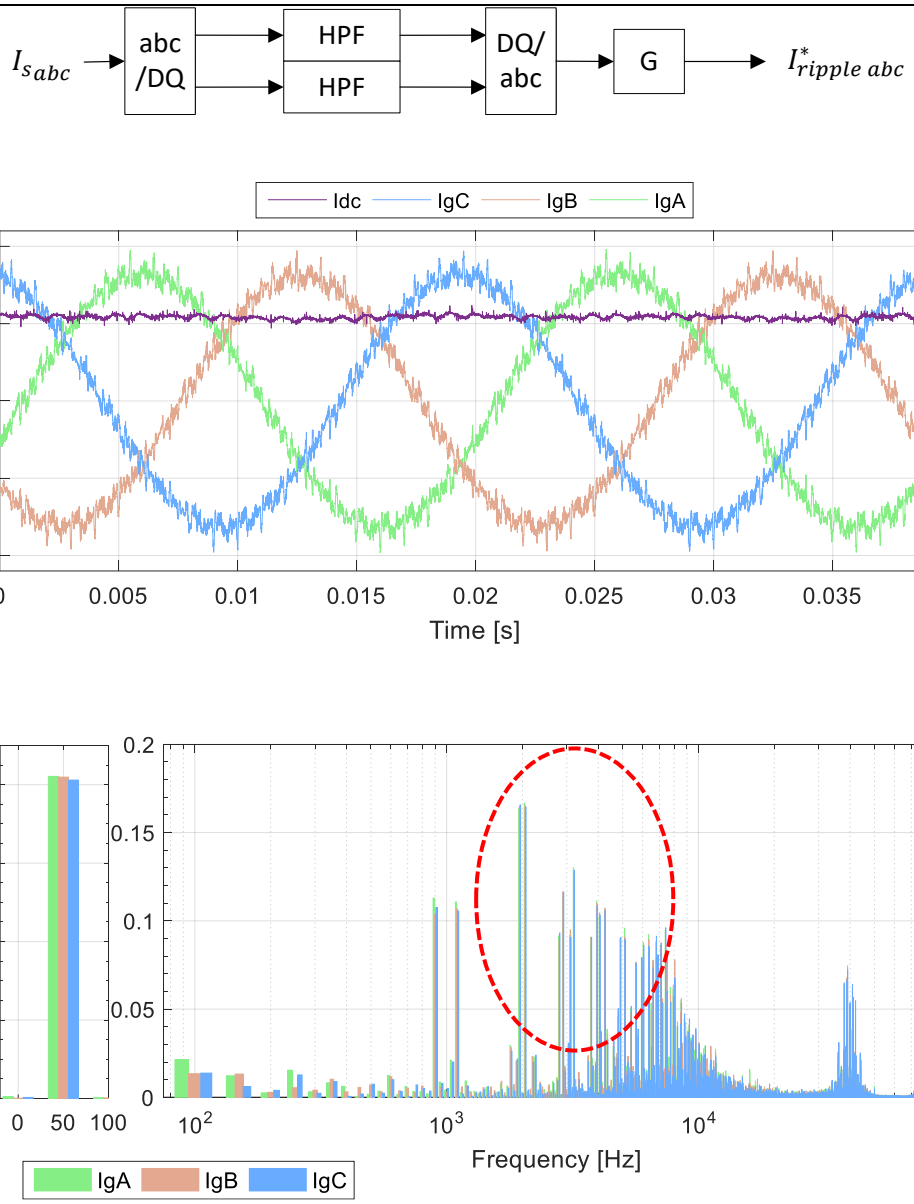
Correlation between FFT methods: Result shows the superimposed FFT waveform of phase A CSI voltage acquired using different methods:

- FFT performed in oscilloscope (using HAMMING window function) for a one second period
- FFT computed using Matlab for one cycle
- FFT computed using Matlab for a one second period.

Phase A currents shown for two cycles of full hybrid system operation for different CSI switching frequencies

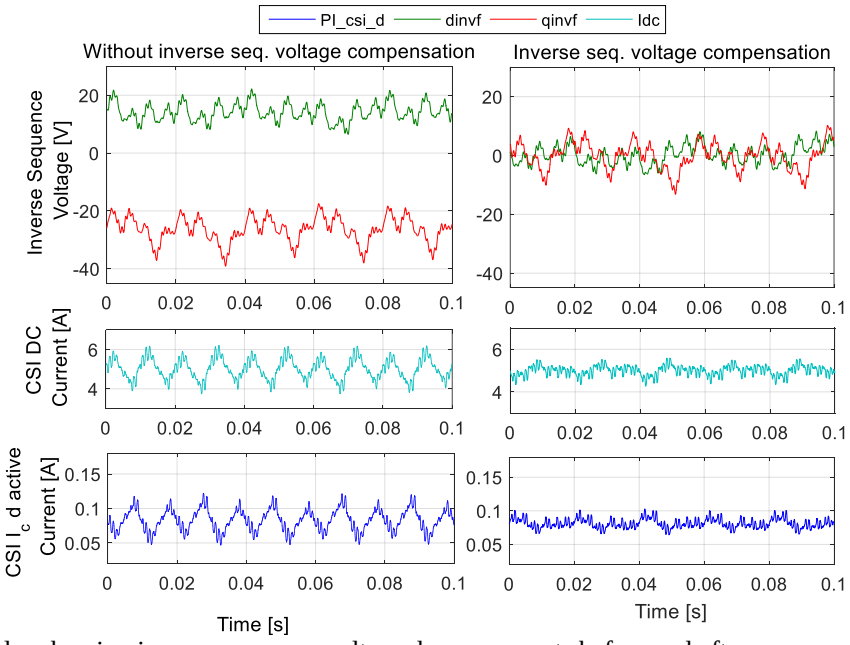


Appendix F. Using HPF for current ripple extraction

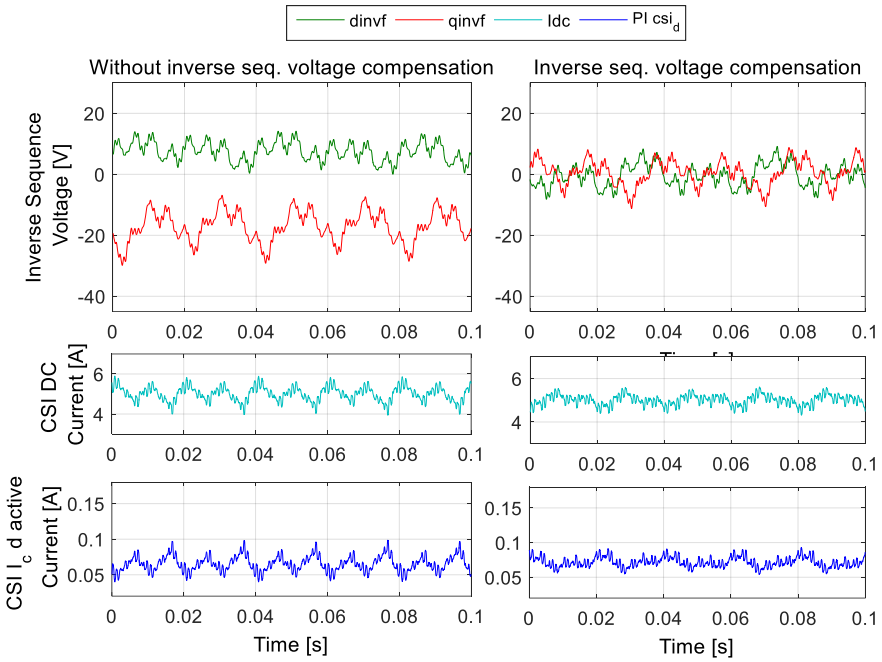


Grid currents using high pass filter for extraction. Prominent remaining periodical notches on the time waveforms can be noticed. Although the main sidebands (900 Hz and 1.1 kHz) are cancelled at comparative levels to ripple extraction using LPF, a noticeable decrease in the reduction of harmonics up to 5 kHz can be seen in the frequency spectrum. This is attributed to a phase shift occurring as the ripple is extracted in the dq reference frame and transformed back to the abc reference values. The cut-off frequency for the HPF had been set at 80Hz.

Appendix G. Validation of negative sequence voltage compensator operation

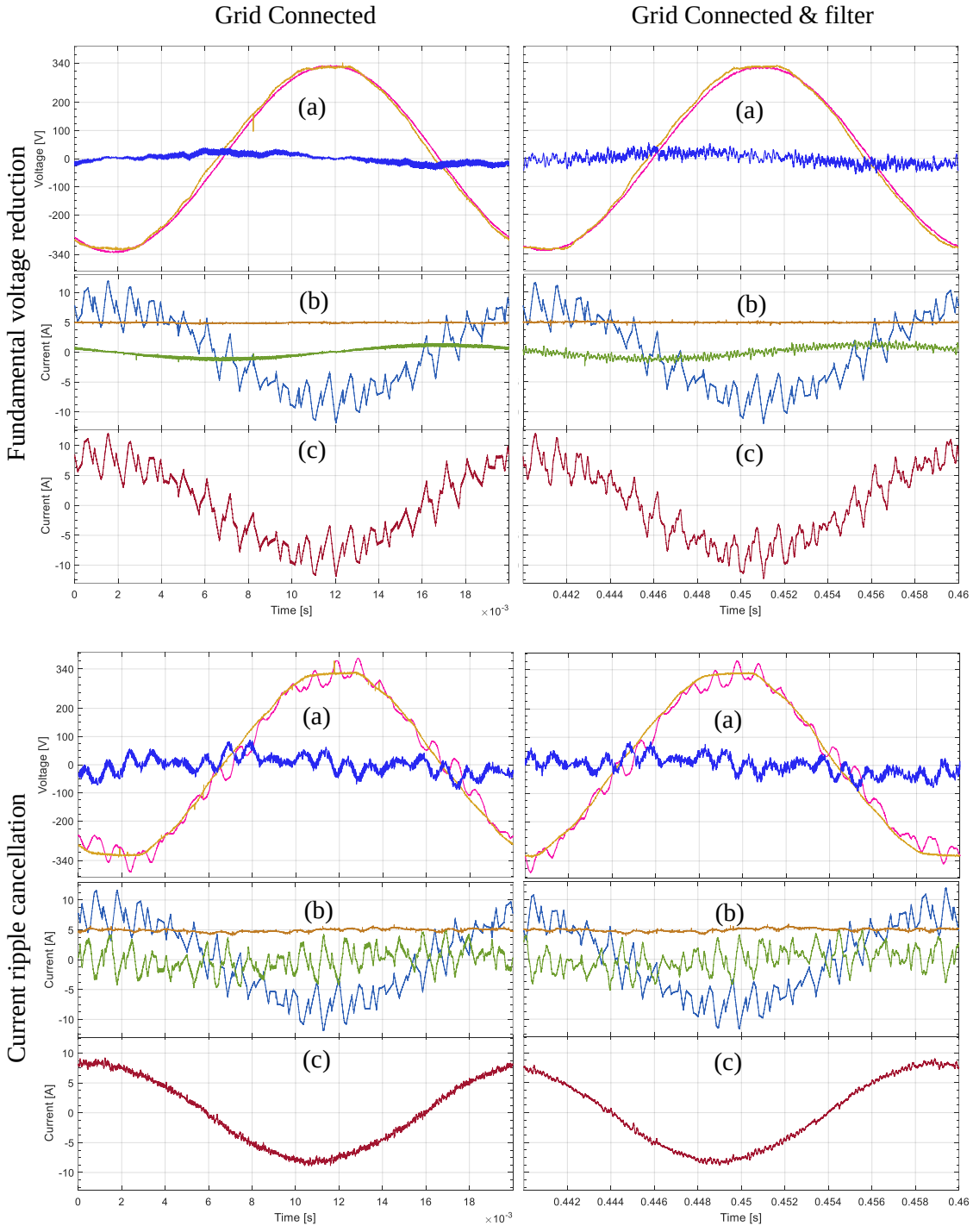


State variables showing inverse sequence voltage dq components before and after compensation while also showing the CSI DC-link current and active current component Ic_d. Both results captured for full hybrid operation. K=0.12.



State variables showing inverse sequence voltage dq components before and after compensation while also showing the CSI DC-link current and active current component Ic_d. Both results captured for full hybrid operation. K=0.12. Using AC filter at the point of PCC.

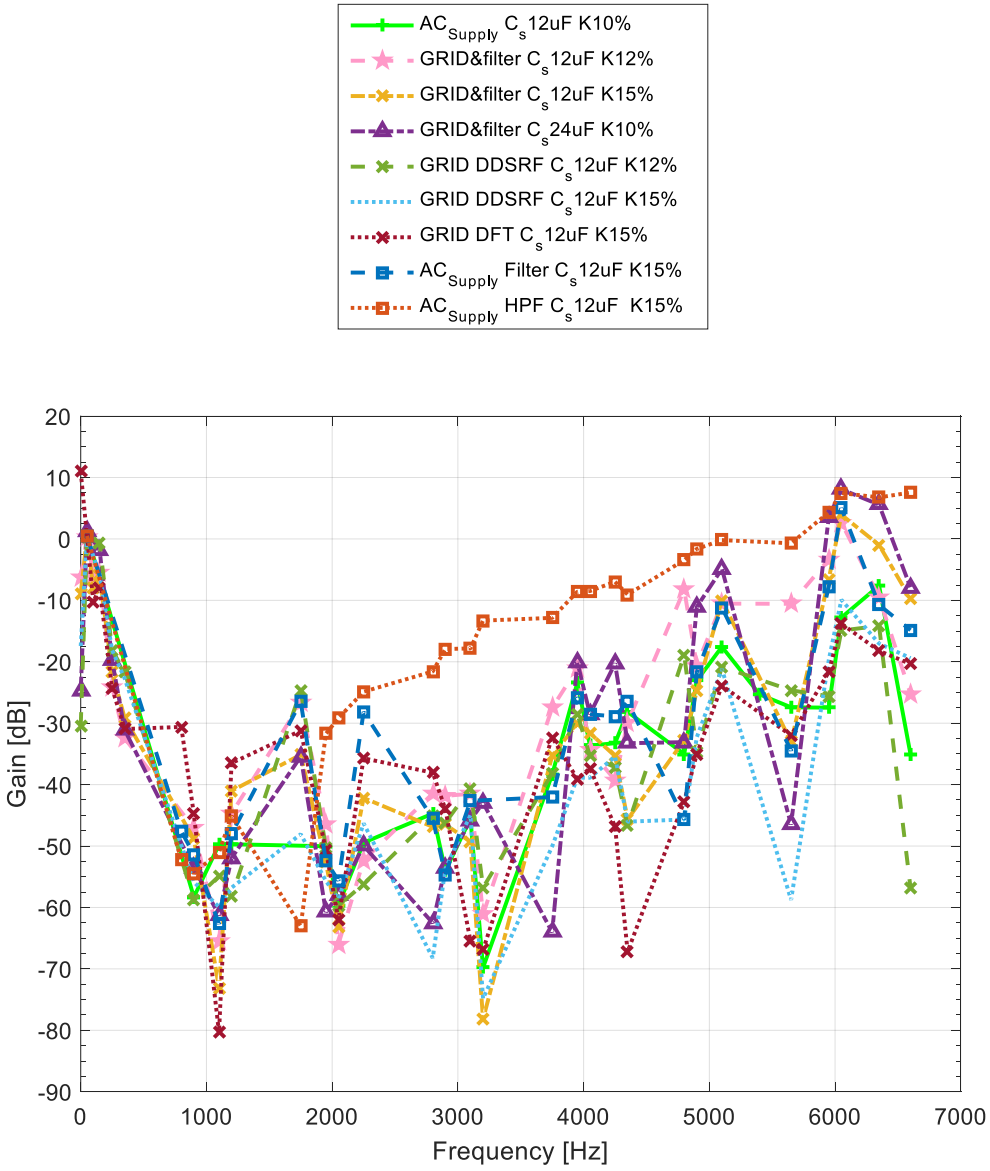
Appendix H. Resonance excitation Phase A results



Experimental results showing: a) Series capacitor (V_c), CSI (V_{csi}) and grid (V_{grid}) phase voltages; b) CSI DC-link current (I_{dc}), Main VSI current (I_s) and series capacitor current (I_c) ; and c) combined grid side current (I_{grid}). The results are shown for one steady state cycle for the following cases: before (top) and after(bottom) ripple cancellation. Without added grid impedance (left) and with added grid impedance showing resonance (right)

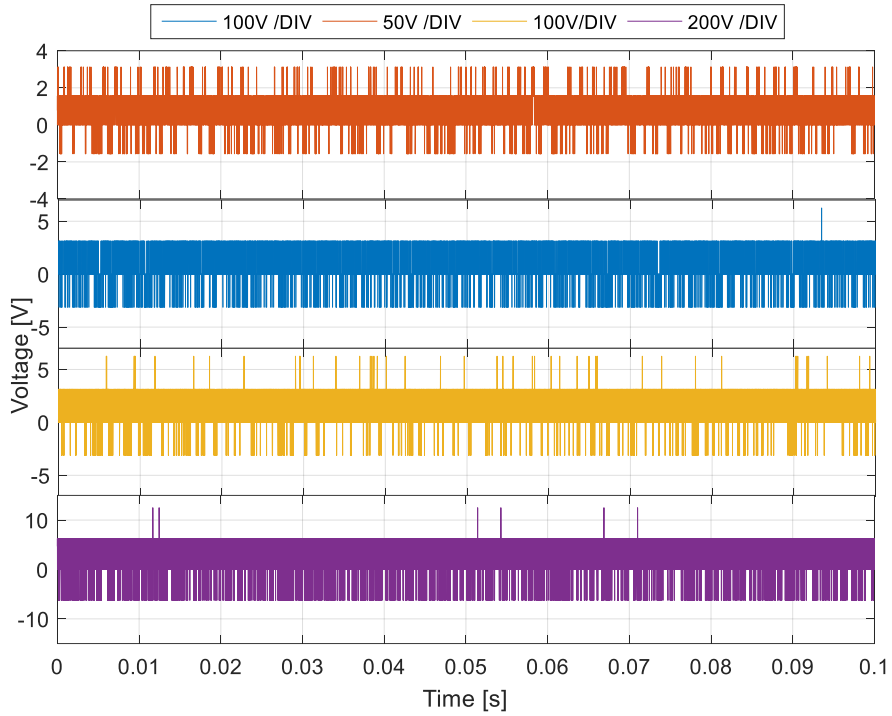
Appendix I. CSI Attenuation: Further Results

Cumulated results showing CSI attenuation for additional tests not included in the thesis:

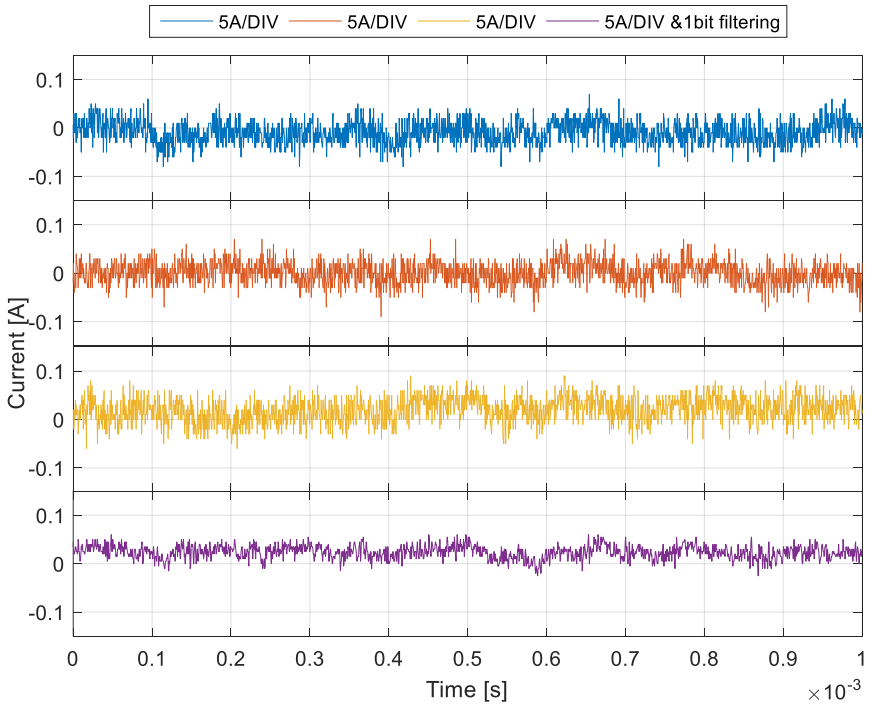


Appendix J. Oscilloscope Measurement Resolution

Minimum measurement resolution and noise for oscilloscope measurements at no load:

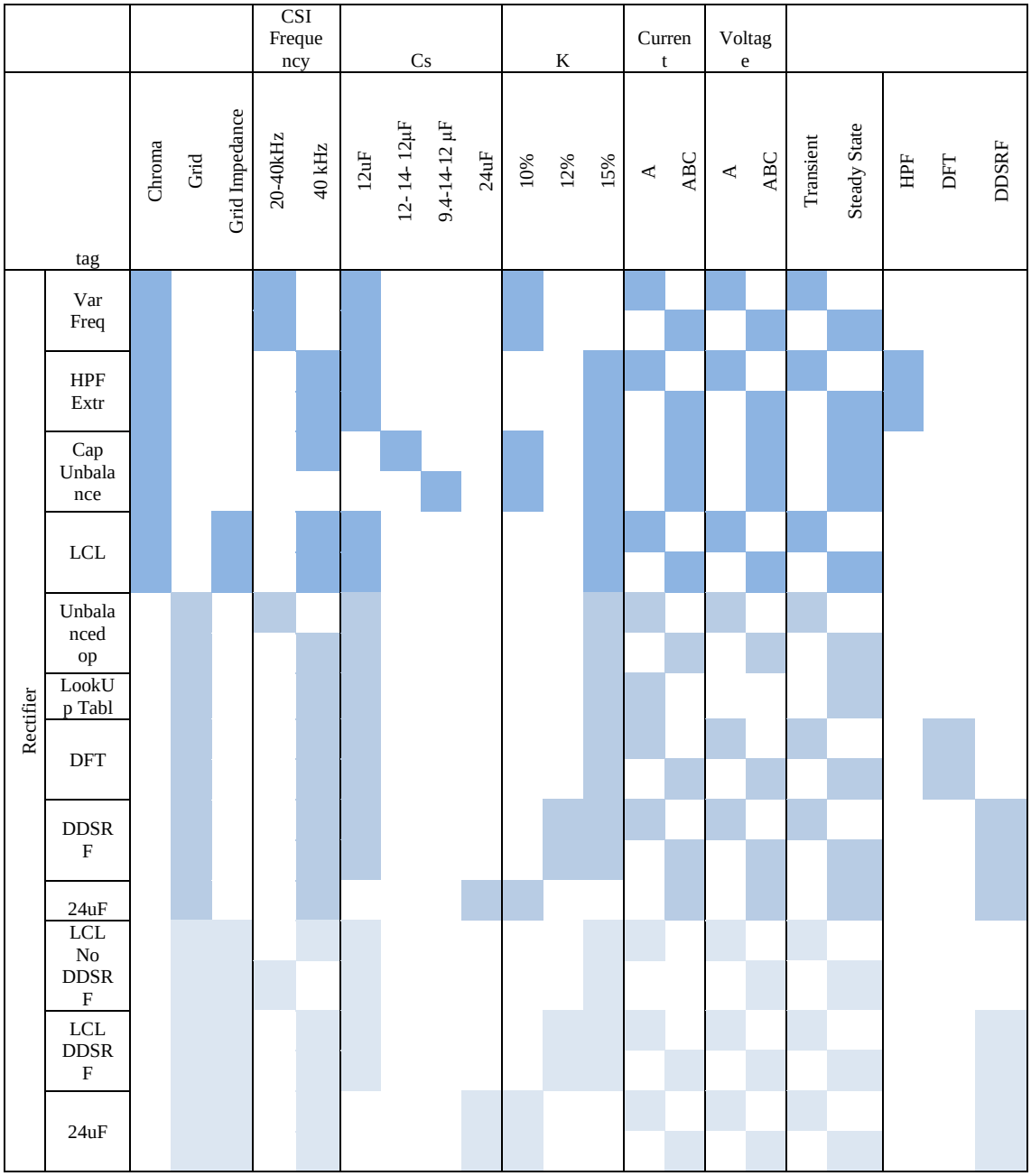


Minimum resolution 1.56V (50V/div) 3.125V (100V/div) and 6.25V (200V/div)



Appendix K. Table of Experimental Tests

Table of experimental configurations tested with results captured at the full grid voltage.



Appendix L. List of Published Papers

The following four conference papers and two journal papers related to the research presented in this thesis have been peer reviewed and published, shown in chronological order:

S. Papadopoulos, M. Rashed, C. Klumpner and P. Wheeler, "A hybrid inverter solution for medium voltage applications using series capacitor and a CSI Active Power Filter (SC-APF)," Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on, Manchester, 2014, pp. 1-6. doi: 10.1049/cp.2014.0456

S. Papadopoulos, M. Rashed, C. Klumpner and P. Wheeler, "A hybrid converter for medium voltage using a low-voltage current source active filter connected via a series capacitor," Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on, Lappeenranta, 2014, pp. 1-10. doi: 10.1109/EPE.2014.6911045

S. Papadopoulos, M. Rashed, C. Klumpner and P. Wheeler, "A hybrid inverter system for medium voltage applications using a low voltage auxiliary CSI," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014, pp. 2809-2816. doi: 10.1109/ECCE.2014.6953779

S. Papadopoulos, M. Rashed, C. Klumpner and P. Wheeler, "Investigations in the Modeling and Control of a Medium-Voltage Hybrid Inverter System That Uses a Low-Voltage/Low-Power Rated Auxiliary Current Source Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 1, pp. 126-140, March 2016. doi: 10.1109/JESTPE.2015.2488631

Papadopoulos, Savvas; Klumpner, Christian; Rashed, Mohamed; Wheeler, Patrick: 'Experimental validation of a hybrid converter with enhanced switching ripple cancellation', IET Power Electronics, 2016, DOI: 10.1049/iet-pel.2015.0984

S. Papadopoulos, M. Rashed, C. Klumpner and P. Wheeler, "Mitigating the Effect of Series Capacitance Unbalance on the Voltage Reduction Capability of an Auxiliary CSI used as Switching Ripple Active Filter," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), doi not yet assigned.