Wide-Bandgap Semiconductor Based Power Converters for Renewable Energy Systems

Emre Gürpınar, MSc

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Abstract

The demand for low carbon economy and limited fossil resources for energy generation drives the research on renewable energy sources and the key technology for utilisation of renewable energy sources: power electronics. Innovative inverter topologies and emerging WBG semiconductor based devices at 600 V blocking class are the enabling technologies for more efficient, reliable and accessible photovoltaic based electricity generation.

This thesis is concerned with the impact of WBG semiconductor based power devices on residential scale PV inverter topologies in terms of efficiency, volume reduction and reliability. The static and dynamic characterisation of the Si and WBG based devices are carried out, gate drive requirements are assessed and experimental performance comparison in a single phase inverter is discussed under wide range of operating conditions. The optimisation of GaN HEMT based single phase inverter is conducted in terms of converter efficiency, switching frequency and converter volume. The long term mission-profile based analysis of GaN and Si based devices is conducted and impact of WBG devices under low and high switching frequency conditions in terms of power loss and thermal loading are presented. Finally, a novel five-level hybrid inverter topology based on WBG devices is proposed, simulated and experimentally verified for higher power applications.

Resume

E-mail: gurpinar.emre@gmail.com

Education

- **MSc in Electrical Energy Conversion Systems**
  University of Manchester, UK, November 2010
- **BSc in Electrical Engineering**
  Istanbul Technical University, Turkey, June 2009

Professional Experience

- **Guest PhD Student**
  CORPE, Aalborg University, Denmark **08/2015 - 11/2015**
- **R&D Power Electronics Engineer**
  GE Power Conversion, UK **10/2011 - 07/2013**
- **R&D Engineer**
  University of Reading, UK **12/2010 - 10/2011**

Scientific Contribution

Emerging wide-bandgap (WBG) power semiconductor devices at 600 V blocking class have been gaining attention from power electronic converter developers with special focus on the application for renewable energy systems. The focus of this thesis is the state-of-the-art inverter topologies and impact of WBG devices at 600 V blocking class on residential scale PV systems.

The first contribution of this thesis is benchmarking of emerging WBG power semiconductor devices at 600 V blocking class, SiC MOSFET and GaN HEMT, and comparison to Si based devices including static and dynamic characterisation, gate drive requirements and performance evaluation in a single phase inverter. The benchmarking of devices has shown that GaN HEMT has excellent switching and conduction properties at low current conditions with negligible temperature dependency, but a relatively higher complex gate driver design is required for safe operation and the design has a strong impact on switching losses. The performance results of WBG devices in single phase inverter shows that SiC and GaN devices provide performance enhancement over Si under wide load, temperature and switching frequency conditions. In terms of switching performance, GaN HEMT has the best performance among three technologies and allows high efficiency at high-frequency applications. The robust performance provides optimisation of system volume and weight by changing switching frequency and heat sink temperature, without compromising system efficiency.

The second contribution is the investigation of impact of the GaN HEMT devices to a PV inverter in terms of power loss, converter efficiency, heat sink and output filter volume, and thermal stress reliability analysis based on a real-field mission profile. The excellent switching and conduction performance of GaN HEMT under different load and heat sink temperature conditions results in very high efficiency and low power cell loss. It is shown that combined heat sink and output filter volume can be reduced by increasing the heat sink temperature from 50 °C to 80 °C, and increasing the switching frequency from 16 kHz to 64 kHz, without compromising the

efficiency of the system. The mission-profile based analysis of the GaN HEMT based inverter shows that GaN HEMT based system has significantly lower thermal stress in comparison to Si IGBT based system at both low and high switching frequency conditions. The reduced thermal stress brought lower junction temperature variation and reduced mean temperature across most stress device throughout the year.

The final contribution of this work is introduction of a novel five-level hybrid inverter topology based on SiC MOSFETs dedicated for renewable energy systems and high power applications, such as variable speed drives or propulsion systems. The results showed that proposed topology provides higher efficiency in comparison to state-of-the-art hybrid topology 5L-ANPC, especially at lighter load conditions. The functionality of the topology was verified experimentally with 650 V SiC MOSFETs in a 12 kW single phase prototype under different load and heat sink temperature conditions.

Journal Papers

First Author

1. **E. Gurpinar** and A. Castellazzi, "Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs, and GaN HEMTs," in *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7148-7160, Oct. 2016.

2. **E. Gurpinar**, Y. Yang, F. Iannuzzo, A. Castellazzi and F. Blaabjerg, "Reliability-Driven Assessment of GaN HEMTs and Si IGBTs in 3L-ANPC PV Inverters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 956-969, Sept. 2016.

Other Author

1. D. Barater, C. Concari, G. Buticchi, **E. Gurpinar**, D. De and A. Castellazzi, "Performance Evaluation of a Three-Level ANPC Photovoltaic Grid-Connected Inverter With 650-V SiC Devices and Optimized PWM," in *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2475-2485, May-June 2016.

Journal Papers under Review

First Author

1. **E. Gurpinar**, F. Iannuzzo, Y. Yang, A. Castellazzi and F. Blaabjerg, "Low Inductance Switching Power Cell Design for GaN HEMT Based Inverter," in *IEEE Transactions on Industry Applications*.
2. **E. Gurpinar** and A. Castellazzi, "GaN HEMT Based Single Phase Inverter Design Optimisation," in *IEEE Transactions on Power Electronics*.

Other Author

1. J. Li, A. Castellazzi, M. A. Eleffendi, **E. Gurpinar**, C. M. Johnson and L. Mills "A Physical RC Network Model for Electro-Thermal Analysis of a Multichip SiC Powe rModule" in *IEEE Transactions on Power Electronics*.

Conference Papers

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1. **E. Gurpinar**, and A. Castellazzi, "600V Normally-Off p-Gate GaN HEMT based 3-Level Inverter" in *IEEE International Future Energy Electronics Conference (IFEEC ECCE-Asia)*, 3-7 June 2017, Kaohsiung, Taiwan (In Press).

2. **E. Gurpinar**, F. Iannuzzo, Y. Yang, A. Castellazzi, F. Blaabjerg, "Ultra-low inductance design for a GaN HEMT Based 3L-ANPC Inverter" in *IEEE Energy Conversion Congress & Expo (ECCE 2016)*, 18-22 Sept 2016, Milwaukee, Wisconsin, pp. 1-8.

3. **E. Gurpinar** and A. Castellazzi, "Novel Multilevel Hybrid Inverter Topology with Power Scalability" in *42nd Annual Conference of IEEE Industrial Electronics Society (IECON 2016)*, 24-27 Oct 2016, Florence (In Press).

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5. **E. Gurpinar**, D. De, A. Castellazzi, D. Barater, G. Buticchi and G. Franceschini, "Performance analysis of SiC MOSFET based 3-level ANPC grid-connected inverter with novel modulation scheme," *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Santander, 2014, pp. 1-7.

6. **E. Gurpinar**, S. Lopez-Arevalo, J. Li, D. De, A. Castellazzi and L. Mills, "Testing of a lightweight SiC power module for avionic applications," *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, Manchester, 2014, pp. 1-6.

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2. J. Garcia, **E. Gurpinar**, and A. Castellazzi , "High-Frequency Modulated Secondary-Side Self-Powered Isolated Gate Driver for Full Range PWM Operation of SiC Power MOSFETs," *2017 IEEE Applied Power Electronics Conference (APEC)*, 26-30 March 2017, Tampa, FL (In Press).

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4. D. Barater, **E. Gurpinar**, G. Buticchi, C. Concari, D. De, A. Castellazzi , "Performance analysis of UniTL-H6 inverter with SiC MOSFETs," *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, Hiroshima, 2014, pp. 433-439.

5. Jianfeng Li, **E. Gurpinar**, S. Lopez-Arevalo, A. Castellazzi and L. Mills, "Built-in reliability design of a high-frequency SiC MOSFET power module," *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, Hiroshima, 2014, pp. 3718-3725.

6. D. Barater, C. Concari, G. Buticchi, **E. Gurpinar**, D. De and A. Castellazzi, "Performance evaluation of a 3-level ANPC photovoltaic grid-connected inverter with 650V SiC devices and optimized PWM," *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, 2014, pp. 2233-2240.

Patents (Pending)

1. **E. Gurpinar**, D. De, A. Castellazzi, "Power Converter", GB Patent App. 1520961.2, 27 November 2015

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Emre Gürpınar

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List of Terms

$2DEG$ - Two-dimensional Electron Gas

AC - Alternating Current

$ANPC$ - Active Neutral Point Clamped

$BFoM$ - Baliga's Figure of Merit

$BSNPC$ - Bi-directional Switched Neutral Point Clamped

BJT - Bipolar Junction Transistor

CM - Common-Mode

CMR - Common-Mode Noise Rejection

DUT - Device Under Test

DC - Direct Current

E_{crit} - Electric Breakdown Field

EU - European Union

E_{on} - Turn-on switching energy

E_{off} - Turn-off switching energy

GaN - Gallium-nitride

$HEMT$ -High Electron Mobility Transistor

$HERIC$ -Highly Efficient and Reliable Inverter Concept

$IEEE$ - Institute of Electrical and Electronic Engineers

IEC - International Electrotechnical Commission

n_i - Intrinsic carrier concentration

$IGBT$ - Insulated-Gate Bipolar Transistor

$JFET$ - Junction Field-Effect Transistor

LFT - Line Frequency Transformer

MPP - Maximum Power Point

$MPPT$ - Maximum Power Point Tracking

$MOSFET$ - Metal-Oxide-Semiconductor Field-Effect Transistor

N_a - Acceptor Doping density

N_d - Donor Doping density

NPC - Neutral Point Clamped

NPP - Neutral Point Piloted

NPT - Non-punch through

PV - Photovoltaic

PT - Punch through

r_{on} - Resistance of Drift Region

RMS - Root Mean Square

q - Elementary charge

Q_{rr} - Reverse recovery charge

Si - Silicon

SiC - Silicon-carbide

SBD - Schottky-barrier Diode

THD - Total Harmonic Distortion

V_{bi} - Built-in potential across pn junction

V_{BR} - Breakdown voltage

UK - United Kingdom

US - United States

WBG - Wide-Bandgap

w_{drift} - Drift region thickness

ε_0 - Permittivity of Vacuum

ε_r - Dielectric Constant

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Chapter 1

Introduction

The ever-increasing demand for energy, limited fossil resources and the need for carbon footprint reduction have raised the awareness for change of the energy production, consumption and management strategies. The aim of creating a low carbon economy with sustainable energy generation and consumption while maintaining energy security has been one of the top priorities for developed and developing countries. The United Kingdom (UK) government, European Union (EU) and United States (US) government have published reports where the importance of low carbon economy and reduction of greenhouses gases have been emphasised, and the increased share of renewable energy sources in electricity generation in the short and long terms has been promised [1], [2].

The renewable energy sources such as wind and photovoltaic (PV) have been at the centre for renewable energy generation. The amount of installed wind power has been increasing rapidly since 1999 and wind power is the major renewable energy source in the world due to increase of wind turbine size and efficiency. In some countries such as Denmark, the aim is to achieve 100 % non fossil-based power generation system by 2050, thanks to large potential of wind along with other renewable sources [3]. In addition to wind power, photovoltaic power has seen strong interest since 2004 and the cumulative installed capacity has increased by factor of 107, from 2000 to

2013 [4]. There are several PV farms in Spain, Germany and Portugal with installed power higher than 40 MW. One of the reasons for increase of PV power penetration to electricity production is the reduction of PV panel price (40 % reduction in 2008) and the other one is advancements in power electronic system, which is the enabling technology for renewable energy systems. Along with high power installations of PV farms, residential scale PV systems have been adopted by the grid users by the subsidies from governments and local authorities in order to reduce the residential electrical energy usage from grid, and potentially feed energy to other users [5].

The share of residential energy generation is increasing rapidly and as mentioned in the previous paragraph, power electronic systems are the enabling technologies for renewable power systems. The power electronic converters provide efficient and flexible connection of residential PV systems to the grid by providing grid synchronisation, maximum power point tracking, anti-islanding and input voltage boosting. As the power generated from a PV panel has to be processed with a power electronic converter, the efficiency and reliability of the converter plays a key role in the overall performance of the system [6]. Therefore, the power electronics research has been focussed on development of systems with higher efficiency and reliability to improve overall performance of the system, reduce cost, increase energy generation and therefore enhance the adoption of PV systems in electrical energy generation.

Two topics have received special attention for residential PV converter development: 1) Converter topologies and 2) Wide-bandgap (WBG) based power semiconductor devices. Innovative converter topologies have been proposed, tailored for PV systems, which provide higher efficiency and lower component count [6]. Moreover, emerging WBG based power semiconductor devices have superior properties in comparison to state-of-the-art Silicon (Si) based power semiconductor devices, and the development of WBG based power devices and penetration to power conversion systems have been announced by US government and European research platforms as one of the priorities in energy research [7], [8]. Hence there is a clear need to assess the impact of emerging WBG power devices in state-of-the-art PV converter topologies to understand the impact of emerging technologies in PV systems.

1.1 Research Objectives

The objective of this work is to investigate the impact of emerging WBG power devices on the design, volume, performance and reliability of highly efficient single phase PV inverters.

In this process the following aspects are considered:

- Comparison of state-of-the-art half-bridge and full-bridge based inverter topologies for residential scale transformerless PV systems.
- Benchmarking of Si and WBG based power devices at 600 V blocking class which are suitable for high efficient single-phase inverters. The benchmarking includes the discussion of devices structures, gate drive requirements, static and dynamic characterisation, and application in PV inverter topologies.
- Experimental performance evaluation of residential scale single phase inverters with Si and WBG devices under wide range of operation conditions (e.g. switching frequency, output power and heat sink temperature).
- Optimisation of WBG device based residential scale single phase inverter in terms of inverter volume, switching frequency and efficiency.
- Mission-profile based reliability-driven assessment of WBG and Si devices in a residential scale PV inverter under long term operating conditions.
- Transfer of knowledge gained about WBG devices to higher power applications, such as multilevel inverters.

1.2 Thesis Outline

The thesis is structured as follows.

Chapter 2 introduces the present status and the background of PV system architectures. PV cell characteristics, and historical background of PV system architectures have been discussed. Grid requirements for the power converters that is used in PV systems have been presented and the impact of these requirements on converter architectures has been discussed in terms of isolation, efficiency and user safety. Review of full-bridge and half-bridge based state-of-the-art PV inverter topologies, which eliminates common-mode current generation, has been presented including inverter operation principles, and comparison in terms of component count and complexity. This chapter ends with simulation based benchmark and analysis of the reviewed topologies in a single phase, grid connected scenario.

In Chapter 3, material properties of Si and WBG materials, and state-of-the art power devices are discussed. The material properties of Si and WBG are compared and the benefits of WBG materials for power devices in terms of blocking and conduction capability are discussed. The material comparison is followed by discussion of power diodes and controlled devices at 600 V blocking class.

In Chapter 4, benchmark of Si and WBG devices in PV inverters is presented. The benchmarking starts with static and dynamic characterisation of 600 V devices under different current and heat sink temperature conditions. Furthermore, gate driver requirements for Si and WBG devices are evaluated. This is followed by performance evaluation of a T-type inverter with Si and WBG devices under different switching frequency, output power and heat sink temperature conditions.

In Chapter 5, a Gallium Nitride (GaN) based PV inverter is analysed to explore the benefits of GaN devices in PV inverters in terms of efficiency, converter volume reduction (heat sink and output filter) and mission-profile based reliability. The discussion starts with the description of the inverter and test setup, followed by experimental

results including efficiency and power loss under different switching frequency, heat sink temperature and load conditions. This is followed by loss breakdown under different temperature and switching frequency conditions to evaluate performance of devices and influence of static and dynamic losses to power cell efficiency. Furthermore, the impact of GaN devices on converter volume is assessed in terms of heat sink and output filter volume. Finally, evaluation of GaN HEMTs and Si IGBTs is presented considering real-field long-term PV mission profiles (e.g., ambient temperature and solar irradiance) to assess the thermal loading and performance of devices in a three-phase grid-connected configuration.

In Chapter 6, potential benefits of WBG devices at higher power applications is explored. The chapter starts with the review of five-level multilevel topologies, with special focus on hybrid topologies. The review is followed by introduction of a new five-level hybrid inverter, which is suitable for WBG based applications with high efficiency. The details of the proposed topology including switching states and commutation scheme are presented and followed by the simulation results including efficiency comparison with respect to state-of-the-art hybrid topology 5L-ANPC. Finally, the experimental results based on 12 kW prototype are presented discussed.

In Chapter 7, conclusions and future works are discussed.

Chapter 2

Review of PV Inverter Topologies

The industrialised economies have been demanding cheap and reliable energy resources in order to produce levels of energy that cannot be achieved by human or animal muscle power since the beginning of industrial revolution. Fossil based natural resources such as coal and petroleum have been widely exploited for this purpose, despite the undesirable side effects such as air pollution and climate change. In 20^{th} century, nuclear based energy production was introduced as an alternative to fossil based resources, but has been recently considered as an unsustainable solution due to safety and political problems. As a result of environmental concerns about fossil fuels, and safety and political concerns about nuclear resources, renewable sources such as photovoltaic, wind and hydro-electric have gained popularity in late 20^{th} century [9]. As 2012, 19% of world's total energy consumption has been provided by renewable sources [10].

Photovoltaic (PV) energy is a key renewable energy resource along with hydro and wind, and as of 2013, the global installed PV capacity has been over 138 GW with a potential of 160 TWh energy generation every year. In addition to the current-installed capacity, the worst case scenario for annual PV installation until 2018 is expected to be around 35 GW [4]. Even with the worst case scenario, there is a strong demand for energy generation with PV systems, where power electronic con-

verters are vital components for realisation of this demand. The intermittent nature of photovoltaic and wind resources require an interface system (e.g. power electronic converter) between the power grid and the source for two reasons: 1) maximum utilization of the source and 2) satisfying the requirements of the power grid. Therefore, renewable power generation is one of the main focus areas of highly efficient and reliable power electronic systems.

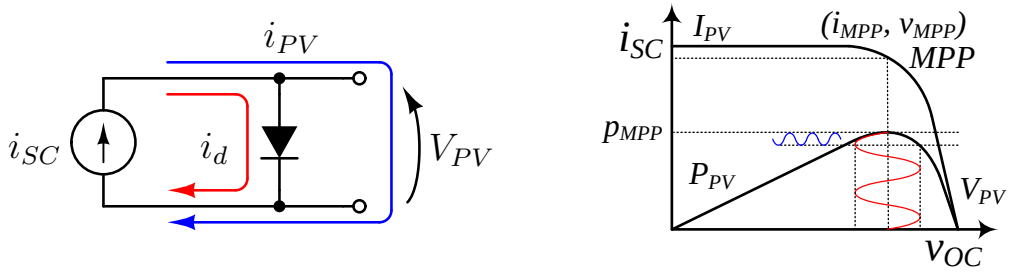
In this chapter, first, single stage and double stage PV converter systems are presented. The main advantages and drawbacks of each configuration are discussed. Then some specific aspects of modern inverter systems such as common-mode (CM) current requirements and transformerless topologies are discussed. The review of single phase transformerless topologies that are designed to eliminate CM current and deliver high efficiency are presented. Finally, efficiency and overall comparison of topologies based on simulation results is presented.

2.1 PV System Architectures

Photovoltaic panels are used in PV based energy generation systems and are formed by series and/or parallel connected PV cells, which are silicon based *pn* junctions with large surface area, depending on output power, voltage and current requirements at specified solar irrandiance and ambient temperature. The output of a PV panel is direct current (DC) and variable in terms of output current, voltage and power. Therefore the output of PV panel has to be controlled for operating at maximum available power and converted to alternating current (AC) for grid connected applications. Within this context,the power electronic converters must cater for two main functionalities: 1) maximisation of energy utilisation by means of Maximum Power Point Tracking (MPPT) control; 2) integration with the AC grid by converting the generated electricity from DC to AC (i.e., using DC-AC inverters) in a grid-friendly manner. That is to say, a certain amount of demands to PV systems should be taken into account in the planning, design, and operation phases such as PV panel

characteristics, ambient operating conditions and grid regulations.

The model and characteristics of most common PV cell technologies are presented in Fig. 2.1a and 2.1b respectively [11]. The model and characteristics show that a PV cell operates as a constant DC current source up to maximum power point (MPP) and the cell has to be operated at MPP in order to maximise the energy generation at any ambient temperature and solar irradiance. The output dependence of a PV cell to solar irradiance and ambient temperature is presented in Fig. 2.2a and 2.2b respectively. During steady state operation, the ripple voltage at the output of the PV cell should be minimised in order to minimise power variation and maximise energy generation. The studies show that ripple voltage at the output of PV cell (V_{PV}) should be below 8.5% for achieving 98% utilization ratio [11].



(a) (b)

Figure 2.1: (a) PV cell model and (b) PV cell characteristics.

According to [12], the relation between output voltage and current of a PV cell presented in Fig. 2.1a can be expressed as:

$$i_{PV} = i_{pv,cell} - i_{0,cell}\left[\exp\left(\frac{q \cdot v_{PV}}{a \cdot k \cdot T}\right) - 1\right] \tag{2.1}$$

where $i_{pv,cell}$ is the current generated by the incident light, $i_{0,cell}$ is the leakage current of the diode, q is the electron charge, k is the Boltzmann constant, T is the temperature of pn junction and a is the diode ideality constant.

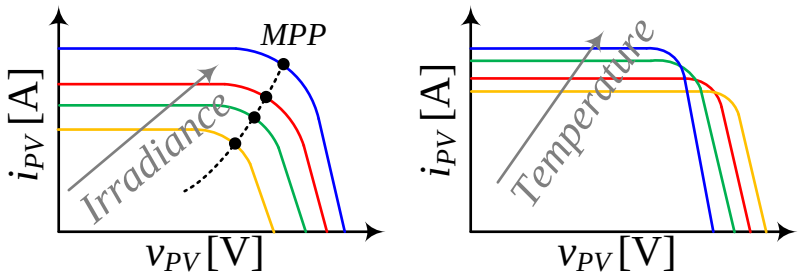


Figure 2.2: PV cell characteristics with respect to (a) solar irradiance and (b) ambient temperature.

On the other hand, integration of the PV system to AC grids is regulated and controlled by grid operators based on national grid legislations. The national grid legislations are based on the international standards set by international bodies such as IEEE (Institute of Electrical and Electronic Engineers) and IEC (International Electrotechnical Commission). Most relevant IEC standards for grid-connected PV systems are IEC 61727 *"Photovoltaic (PV) Systems - Characteristics of the Utility Interface"*, IEC 61000 *Electromagnetic Compatibility (EMC)* and IEC 62116 *"Utility-interconnected photovoltaic inverters - Test procedure of islanding prevention measures"*. IEC 61727 lays down the requirements for interconnection of PV systems to the utility distribution system including power quality, response to abnormal grid conditions such as voltage deviations and frequency deviations [13]. IEC 62116 defines the test procedure for evaluation of the performance of anti-islanding measures for grid-connected PV systems [14]. Finally, IEC 61000 deals with the limitations of harmonic currents injected to the systems where IEC 61000-3-2 covers for devices up to 16 A per phase [15] and IEC 61000-3-3 covers limitations of voltage fluctuations and flickers impressed on the grid [5], [16]. A summary of some standards regarding interconnections of PV systems to the grid is presented in Tables 2.1. In addition to Table 2.1, current harmonic limits for class A devices, such as solar inverters, with less than 16 A output current are presented in Table 2.2. It is clear that the grid has strict harmonic regulations in order to minimise the impact of the inverter to other equipment connected to the grid. It should be noted that the parameters presented

Issue	**IEC 61727 [13]**
Nominal power	10 kW
Harmonic Currents (Order -h) Limits	(3-9) 4% (11-15) 2% (17-21) 1.5% (23-33) 0.6%
Maximum THD	5%
Power factor at 50% rated power	0.90
DC current injection	Less than 1.0% of rated output current
Voltage range for nominal operation	85% - 110% (196 V - 253 V)
Frequency range for nominal operation	50 ± 1 Hz

Table 2.1: Grid requirements for interconnections of PV systems to the grid [11].

IEC 61000-3-2 [15]

Odd Harmonics		Even Harmonics	
Order h	Current [A]	Order h	Current [A]
3	2.30	2	1.08
5	1.14	4	0.43
7	0.77	6	0.30
9	0.40	$8 \leq h \leq 40$	$0.23 \times 8 \,/\, h$
11	0.33		
13	0.21		
$13 \leq h \leq 39$	$0.15 \times 15 \,/\, h$		

Table 2.2: Current harmonic limits for Class A devices.

in Table 2.1 and 2.2 apply to regions where IEC regulations are set as standard. Therefore, performance and design of the PV systems must be compatible with the requirements of installed PV array and also requirements from grid operator in the installed region.

Based on the requirements of PV panels and AC grids, various PV systems have been developed throughout the years. Here four main concepts are considered: centralised, string, multi-string and ac-module technologies shown in Fig. 2.3.

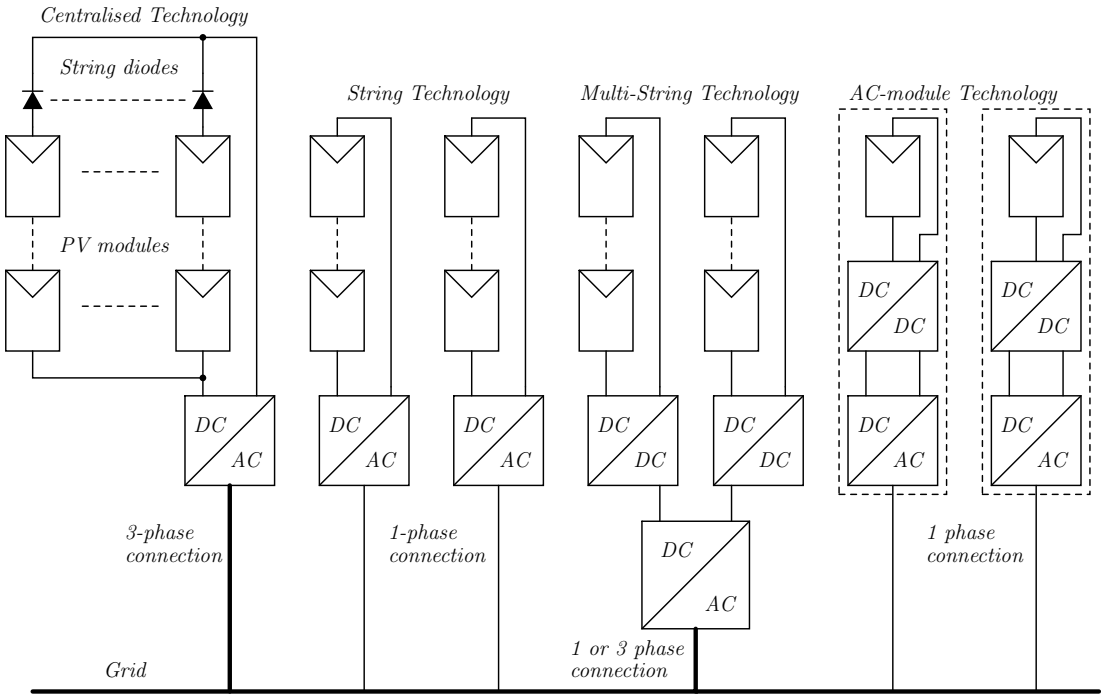


Figure 2.3: Historical overview of PV systems [11].

2.1.1 Centralised Technology

Development of the electricity generation from PV cells started with centralised inverter technology. In centralised technology, large number of PV modules are connected in series and parallel in order to achieve required DC link voltage and power rating. According to required DC link voltage, PV cells are connected in series to form the string with required voltage capacity, and in order to achieve required power level, the strings are connected in parallel with string diodes in series to avoid current flow between strings. The centralised converter has severe limitations such as high voltage cables between strings, maximum power point mismatch between PV modules and losses in string diodes. The centralised converter was generally based on line commutated converter topologies that suffer from high current harmonics and low power quality.

2.1.2 String Technology

With the advancement in Insulated-Gate Bipolar Transistor (IGBT) and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) technologies up to 1000 V blocking class, self-commutated (fully controlled) topologies gained interest in PV systems as string inverters in order to overcome relatively high harmonics generated by line-commutated converters (i.e. thyristor based converters), high voltage cabling between strings, maximum power point mismatch and string diode losses. The number of series connected PV modules can also be reduced with string technology by using a DC-DC converter between PV string and an inverter, or a line-frequency transformer at the output of the inverter. The string approach has higher efficiency and reduced cost due to removal of string diodes, separate MPPT applied to each string and modular production [5], [11].

2.1.3 Multi String and AC-Module Technologies

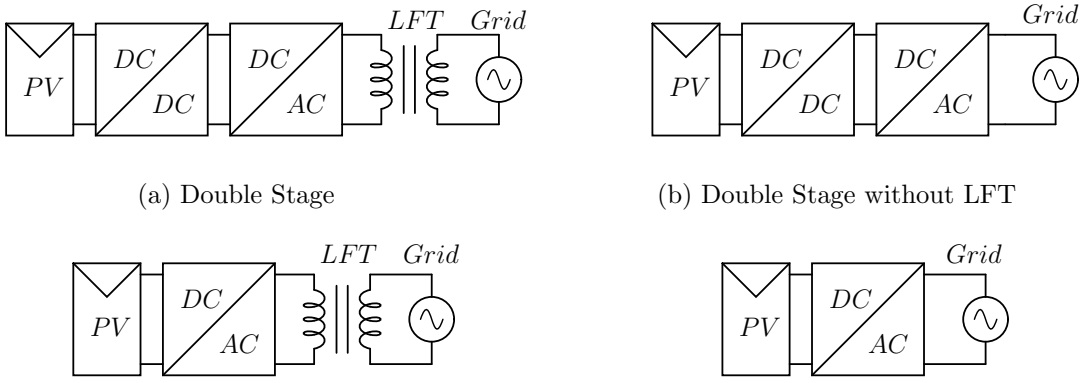
Multi string and AC-module technologies in Fig. 2.3 are considered the next-generation concepts for PV inverter systems that will overcome the challenges of the centralised and the string technologies such as operating point mismatch between PV cells, single point of failure that can disable an entire PV string, and can provide flexible PV voltage and power ratings. In multi string configuration, a DC-DC converter is used for each string for maximum power point control and stepping up the PV string voltage to the main DC bus voltage where as the inverter is responsible for feeding the generated power to the AC grid. This configuration allows further expansion of the system by adding new PV string with a DC-DC converter to the existing PV structure. Therefore it provides a flexible design with high efficiency. On the other hand, AC-module technology is proposed as a plug and play concept where one large PV module is connected to a DC-DC converter and an inverter. This configuration removes the mismatch losses between PV modules since each module is controlled by a single converter and therefore each module can be connected directly to grid. The

system provides simplicity and ease of use for the users that do not have knowledge of electrical installations. The main challenges for AC-module are achieving high voltage amplification ratio with high efficiency in the DC-DC converter due to low output voltage of single PV module (5 V $\sim$ 20 V), and high power density with high efficiency. Therefore, novel converter topologies, power device and passive technologies are required along with mass production of the inverters in order to make the technology viable. In addition to this, the stability of the grid and harmonic content in the grid caused by multiple inverters working in parallel are the challenges with AC module technology [17].

2.1.4 Current Status of String Technology

Although the system structures presented in Fig. 2.3 are different, the architecture is eventually the same, with different power ratings based on PV module configuration. Due to the limitations of multi string and AC-module technologies, and high efficiency and simplicity against centralised technology, string is the most popular technology for PV systems. Different power electronics based systems and converter topologies based on single-staged, double-staged, and with or without galvanic isolation have been proposed in literature for string technology based PV systems in order to comply with grid requirements, which are mentioned earlier while maximising PV energy generation. Different converter topologies and system structures based on single and double-staged conversion systems are published and reviewed in literature [11, 18, 19], whereas the aforementioned power electronics converters are widely utilized. Fundamental structures of single stage and double stage conversion systems with and without isolation transformer are presented in Fig. 2.4. The traditional solution with multiple conversion stages and galvanic isolation as shown in Fig. 2.4a provide flexibility in PV module design and maximum user safety with the penalty of increased system cost and efficiency. Isolation transformer or line frequency transformer (LFT) provide galvanic isolation of PV module from grid and can also provide step-up of generated output voltage at lower PV output voltage. In double-staged conversion, a DC-DC converter is responsible for stepping up the PV output voltage

and maximum power point tracking, where the LFT can be used to provide galvanic isolation and elimination of ground leakage current. The ground leakage current is caused by the voltage variation across the parasitic capacitance between the PV panel and the earth connection, and the source of voltage variation is the common-mode voltage variation at the output of the inverter, which will be explained in detail in Section 2.1.5. Single stage inverter in Fig. 2.4c is the first designs of grid-connected inverters featured a line-frequency transformer for the coupling to the mains. In recent converters, high-frequency transformer coupling or transformerless inverters are preferred, as shown in Fig. 2.4d, due to higher system efficiency and lower system cost.



(a) Double Stage

(b) Double Stage without LFT

(c) Single Stage

(d) Single Stage without LFT

Figure 2.4: Conversion stages for grid-connected PV systems.

2.1.5 Common Mode Current

Single stage transformerless inverters for string technology have gained interest due to mentioned advantages such as high efficiency and simplicity. The main problem that arises with transformerless topologies is due to the photovoltaic panels' parasitic capacitance between the panel and the earth connection , that causes ground leakage current to flow into the grid [20, 21, 22]. This effect is extremely detrimental for the power quality and can cause the disconnection of the inverter due to the residual current device; Figs. 2.5 and 2.6 show the path of the ground leakage cur-

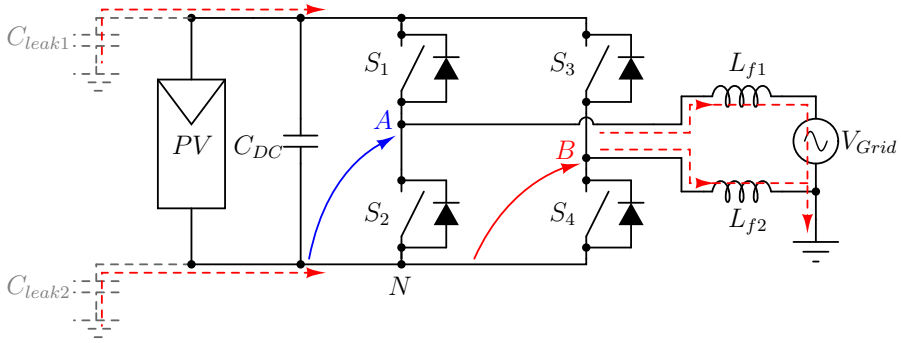


Figure 2.5: Common-mode current path for full-bridge inverter.

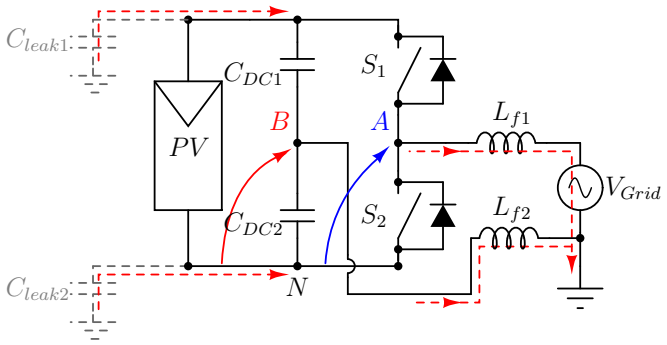


Figure 2.6: Common-mode current path for half-bridge inverter.

rent for well-known full-bridge and half-bridge topologies. The main reason of the ground leakage current is the voltage variation across stray capacitance of PV panel with respect to ground, $C_{leak1-2}$. Voltage variation across $C_{leak1-2}$ is determined by common-mode voltage at the output of the converter and high frequency variation of common-mode voltage can cause large amount of current flowing through the earth connection. The ground current in distribution systems is limited by the grid operators and international standards in order to provide safe operation for end users. As the leakage current circuit is completed via the earth connection of the system, generated leakage current can flow through the users' body in residential systems and can be fatal for users or the people living nearby the PV system. German safety standard VDE 0126-1-1 "Automatic Disconnection Device between a Generator and the Public Low-Voltage Grid" limits maximum permissible leakage RMS current to 300 mA, including active monitoring of fault current with sensitivity down to 30 mA [5, 23]. Leakage current performance of PV inverters has been analysed in detail in the literature and an analytical calculation of leakage current for PV inverters is presented in [21]. The differential voltage V_{DM} and common mode voltage V_{CM_1} at the output of the full-bridge in Fig. 2.5 and half-bridge in Fig. 2.6 topologies can be calculated as follow:

$$V_{DM} = V_{AN} - V_{BN} = V_{AB} \tag{2.2}$$

$$V_{CM_1} = \frac{V_{AN} + V_{BN}}{2} \tag{2.3}$$

and according to [21], total common mode voltage (V_{CM_t}) after the line inductors L_{f1} and L_{f2} can be calculated as:

$$V_{CM_t} = V_{CM_1} + V_{CM_2} \tag{2.4}$$

where

$$V_{CM_2} = V_{DM}\frac{L_{f2} - L_{f1}}{2 \cdot (L_{f2} + L_{f1})} \tag{2.5}$$

Therefore, the total common-mode voltage is:

$$V_{CM_t} = V_{CM_1} + V_{DM}\frac{L_{f2} - L_{f1}}{2 \cdot (L_{f2} + L_{f1})} \tag{2.6}$$

Equation 2.6 can be used to calculate common mode voltage at the output of the inverter for each switching state (e.g. $+V_{DC}$, $-V_{DC}$, 0). By using the variation of common mode voltage between switching states and value of parasitic capacitance C_{leak} in Fig. 2.5 and 2.6, common mode current flowing through the earth can be calculated. Total output inductance is distributed equally among filter inductors L_{f1} and L_{f2} in full-bridge based topologies in order to cancel out the V_{CM_2} in Eq. 2.6. On the other hand, in half-bridge based topologies, the inductance of L_2 is minimised and the total inductance is reflected on L_{f1} in order to minimise the common mode voltage variation at neutral point B. In the literature, it is stated that the parasitic capacitance between PV panel and earth can vary between nano farads and micro farads, depending on installation, weather conditions and panel characteristics [24]. Therefore, large common mode currents can flow to earth with transformerless topologies where the common-mode voltage varies with respect to the switching state.

2.2 Review of Single Phase PV Inverter Topologies

In this section, the most popular single phase PV inverter topologies based on full-bridge and half-bridge architectures are presented. Various topologies have been introduced, specifically for transformerless string inverters for minimising ground leakage current and maximising efficiency. The review begins with introduction of

full-bridge inverter with three different modulation schemes: bipolar, unipolar and hybrid modulations, and continues with full-bridge derived topologies with 3-level voltage output. Furthermore, 3-level half-bridge based topologies are discussed and finally, the efficiency performance of the inverters are compared according to European and American efficiency standards with standard Si IGBTs and Si diodes.

2.2.1 Full-Bridge Derived Topologies

2.2.1.1 Full-Bridge Inverter with Bipolar and Unipolar Modulation

The full-bridge inverter is one of the most popular single phase topologies and has been widely used in various applications where single phase DC-AC or AC-DC conversion is required. The schematic of full-bridge is presented in Fig. 2.7. Devices S_1-S_4 are rated at full DC-link voltage V_{DC} and can be modulated in order to achieve two-level or three-level output voltage by using bipolar, unipolar or hybrid modulation. For full-bridge based topologies, the DC-link voltage V_{DC} can be in the range of 350-400 V for regions such as Europe where RMS grid voltage V_{Grid} is 230 V. Output differential and common mode voltages with respect to each switching state for these three modulation schemes are presented in Table. 2.3. The common-mode voltage at the output of the inverter is calculated with respect to Eq. 2.6 with the equal inductance of L_{f1} and L_{f2}.

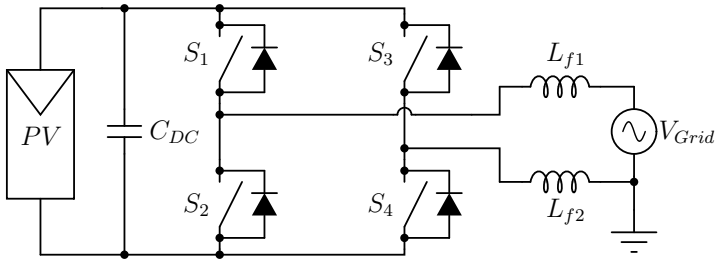


Figure 2.7: Full-bridge inverter.

PWM waveforms for bipolar and unipolar modulation schemes are presented in Fig. 2.8. During bipolar modulation, S_1-S_4 and S_2-S_3 device pairs are switched simultaneously and output voltage is varied between $+V_{DC}$ and $-V_{DC}$. Due to bipolar variation of output voltage across filter inductor and hard switching of two devices at each switching instant, low efficiency with high filtering requirement is expected with this modulation scheme. On the other hand, in unipolar modulation, during positive half of the output voltage, the voltage is varied between $+V_{DC}$ and 0, and during negative half, the output voltage is varied between $-V_{DC}$ and 0. For 0 voltage instants, 0_P or 0_N in Table 2.3 can be used during positive and negative halves of output voltage respectively. In comparison to bipolar modulation, the output voltage has three level rather than two and only one switch is subject to hard switching during change of output voltage. In addition to this, the effective switching frequency at the output of the inverter is twice the switching frequency. In comparison to bipolar modulation, for same switching frequency and output current ripple, the required filter inductance will be four times smaller. Due to these reasons, the expected efficiency with unipolar modulation is higher than bipolar modulation. In hybrid modulation, one of the legs is switched at switching frequency while the other leg is switched at grid frequency in order to achieve three level output voltage. The effective switching frequency at the output of the inverter is equal to switching frequency and provides high efficiency due to lower switching frequency in one leg.

However, from Table 2.3, with unipolar and hybrid modulation, it can be seen that the common mode voltage varies during transition from $+V_{DC}$ and $-V_{DC}$ to 0_P and/or 0_N states, therefore high frequency ground leakage current will flow through the PV system. In conclusion, low efficiency, large filter requirement of bipolar modulation and high ground leakage current of unipolar and hybrid modulation make full-bridge inverter unattractive for transformerless single phase systems and full-bridge based topologies have been derived that combines low filtering requirements, high efficiency along with minimised ground leakage current.

Bipolar Modulation

Output State	S_1	S_2	S_3	S_4	V_{DM}	V_{CM_t}
$+V_{DC}$	1	0	0	1	$+V_{DC}$	$+V_{DC}/2$
$-V_{DC}$	0	1	1	0	$-V_{DC}$	$+V_{DC}/2$

Unipolar Modulation

Output State	S_1	S_2	S_3	S_4	V_{DM}	V_{CM_t}
$+V_{DC}$	1	0	0	1	$+V_{DC}$	$+V_{DC}/2$
0_P	1	0	1	0	0	$+V_{DC}$
0_N	0	1	0	1	0	0
$-V_{DC}$	0	1	1	0	$-V_{DC}$	$+V_{DC}/2$

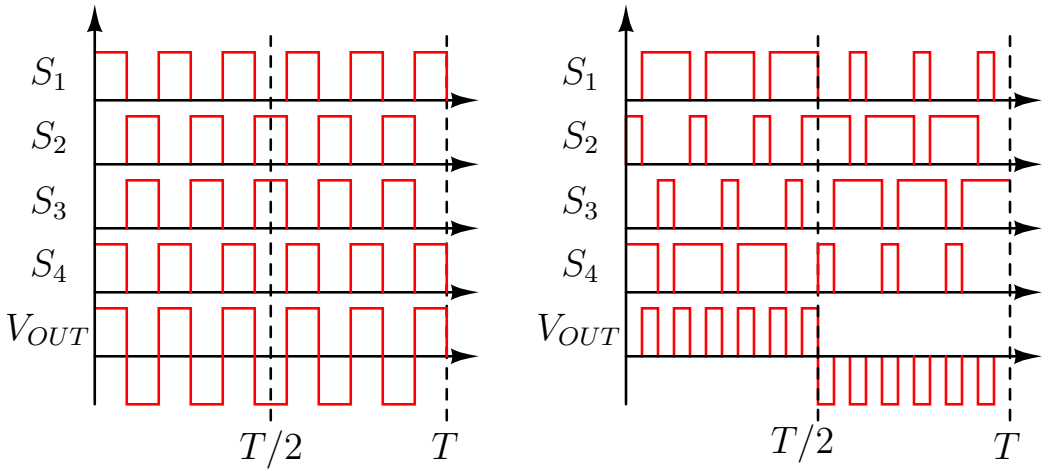
Hybrid Modulation

Output State	S_1	S_2	S_3	S_4	V_{DM}	V_{CM_t}
$+V_{DC}$	1	0	0	1	$+V_{DC}$	$+V_{DC}/2$
0_P	1	0	1	0	0	$+V_{DC}$
0_N	0	1	0	1	0	0
$-V_{DC}$	0	1	1	0	$-V_{DC}$	$+V_{DC}/2$

Table 2.3: Switching states for full-bridge inverter with bipolar and unipolar modulation scheme.

2.2.1.2 H5 Inverter

H5 inverter is one of the first derived topologies from full-bridge inverter for transformerless PV systems and schematic of the inverter is presented in Fig. 2.9. In H5, S_5 switch has been introduced at the high side of DC-link in order to decouple the output of the inverter from PV module when the output state of the inverter is zero. The additional decoupling switch S_5 is rated at full DC-link voltage V_{DC}. It was mentioned that the common mode voltage in a full-bridge inverter with unipolar modulation varies when the output state goes to zero; therefore, by decoupling the output of the inverter from during zero state, the common-mode voltage can be kept constant and ground leakage current can be minimised. S_5 switch also prevents reactive power exchange between C_{DC} and $L_{f1(2)}$.The switching states for H5 inverter are presented in Table 2.4. Hybrid modulation scheme is implemented for this converter where S_1 (S_3) are switched at grid frequency, and S_5 and S_4 (S_2) are switched at inverter switching frequency as shown in Fig. 2.10. Three level voltage is achieved without doubling effective switching frequency at the output, as for unipolar modu-



(a) (b)

Figure 2.8: PWM signals for (a) bipolar modulation and (b) unipolar modulation.

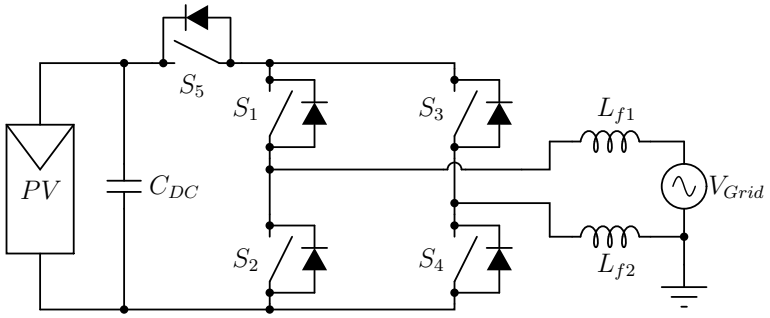


Figure 2.9: H5 inverter.

lation. The major drawbacks of this converter are the addition of S_5 to the system and the fact that three switches are conducting during active states of the inverter, resulting in increase in conduction losses [5]. The topology has been patented and used in commercial PV inverters [25].

Output State	S_1	S_2	S_3	S_4	S_5	V_{DM}	V_{CM_t}
$+V_{DC}$	1	0	0	1	1	$+V_{DC}$	$+V_{DC}/2$
0_P	1	0	0	0	0	0	$+V_{DC}/2$
0_N	0	0	1	0	0	0	$+V_{DC}/2$
$-V_{DC}$	0	1	1	0	1	$-V_{DC}$	$+V_{DC}/2$

Table 2.4: Switching states for H5 inverter.

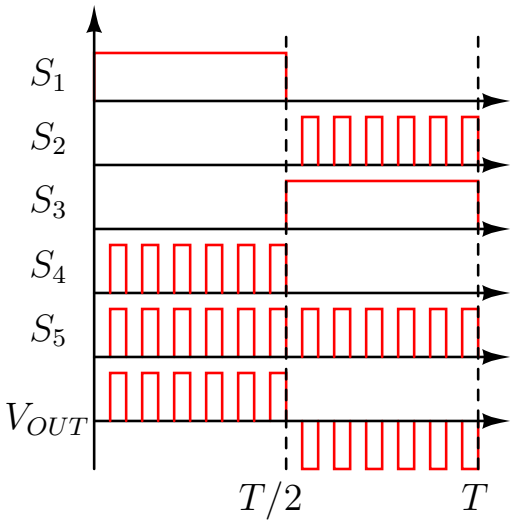


Figure 2.10: PWM Signals for H5 inverter.

2.2.1.3 HERIC Inverter

Highly Efficient and Reliable Inverter Concept (HERIC) in Fig. 2.11 is another full-bridge derived transformerless PV topology. The topology has been patented and also commercialised for string PV systems [26]. In HERIC inverter, elimination of ground leakage current is achieved by decoupling of PV module from the grid with by AC bypass switch, formed by S_5 and S_6 rated at full DC-link voltage V_{DC}. The function of AC bypass switch in HERIC is same as DC bypass switch in H5 inverter. The switching states for HERIC are presented in Table 2.5 and represented in Fig. 2.12. In HERIC, full-bridge switches S_1-S_4 are switched at switching frequency where AC bypass switches $S)5$ and S_6 are switched at grid frequency. Three level output voltage waveform is achieved by two switches switching at switching frequency and one at grid frequency, like in H5 inverter. The effective output switching frequency is equal to switching frequency and two devices are in conduction at any switching

state.

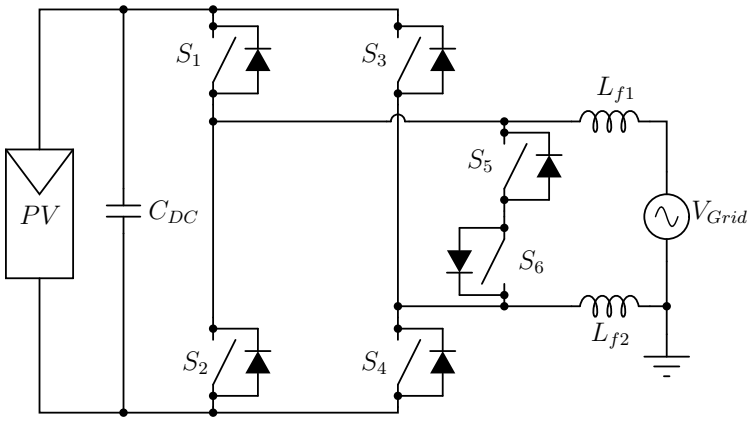


Figure 2.11: HERIC inverter.

Output State	S_1	S_2	S_3	S_4	S_5	S_6	V_{DM}	V_{CM_t}
$+V_{DC}$	1	0	0	1	0	1	$+V_{DC}$	$+V_{DC}/2$
0_P	0	0	0	0	0	1	0	$+V_{DC}/2$
0_N	0	0	0	0	1	0	0	$+V_{DC}/2$
$-V_{DC}$	0	1	1	0	1	0	$+V_{DC}$	$+V_{DC}/2$

Table 2.5: Switching states for HERIC inverter.

2.2.1.4 H6 Inverter

The H6 architecture, shown in Fig. 2.13, was first proposed in [27]. In comparison to the H5 topology, an additional switch S_6 in the lower rail of the DC Link is present. D_1 and D_2 diodes in H6 are optional devices that do not conduct current but ensure fixing common-mode voltage to $V_{DC}/2$ in case of an asymmetric switching behaviour in the full-bridge. In [28], it is mentioned that in topologies such as H5 and HERIC, the V_{AN} and V_{BN} voltages presented in Fig. 2.5 cannot be clamped to $V_{DC}/2$ during freewheeling period and therefore their levels depend on the parasitic parameters of the freewheeling path. If the asymmetrical commutation occurs, the common-mode voltage will not be equal to $V_{DC}/2$ and therefore high common-mode voltage variation will occur at the output. D_1 and D_2 also limit the blocking voltage of S_1 and S_6 to

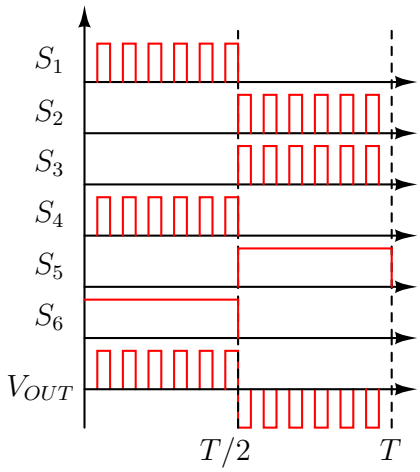


Figure 2.12: PWM Signals for HERIC inverter.

half of DC-link voltage $V_{DC}/2$. The switching states of H6 inverter is presented in Table 2.6 and PWM signals are presented in Fig. 2.14. During the positive half cycle of the output voltage, S_1 and S_4 are on, and S_5-S_6 are switched complementary with S_2-S_3 at switching frequency. During the negative half cycle of the output voltage, S_2 and S_3 are on, and S_5-S_6 are switched complementary with S_1-S_4 at switching frequency. During zero state, the output current is divided into S_1-S_3 and S_2-S_4. With unity power factor operation, only S_1 and S_6 are subject to hard switching at switching frequency and four devices are in conduction during active output states.

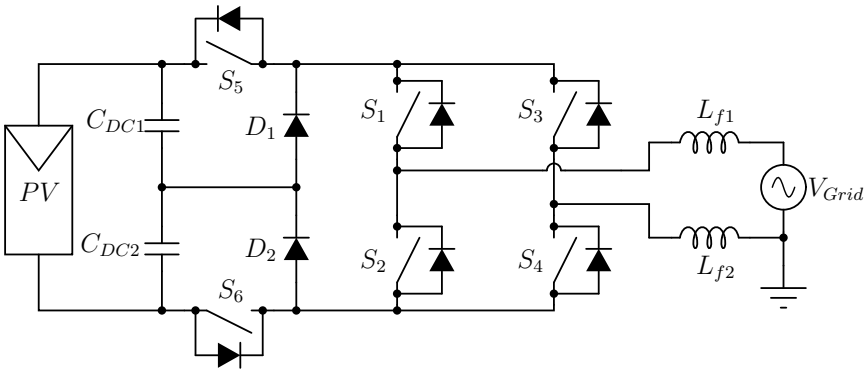


Figure 2.13: H6 inverter.

In [24], an alternative modulation strategy named UniTL was proposed for driving

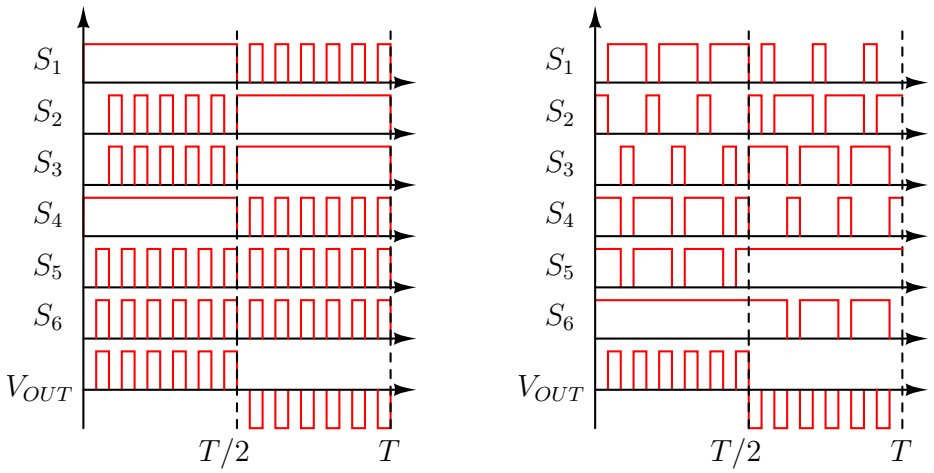
Standard Modulation [27]

Output State	S_1	S_2	S_3	S_4	S_5	S_6	V_{DM}	V_{CM_t}
$+V_{DC}$	1	0	0	1	1	1	$+V_{DC}$	$+V_{DC}/2$
0	1	1	1	1	0	0	0	$+V_{DC}/2$
$-V_{DC}$	0	1	1	0	1	1	$+V_{DC}$	$+V_{DC}/2$

UniTL Modulation [24]

Output State	S_1	S_2	S_3	S_4	S_5	S_6	V_{DM}	V_{CM_t}
$+V_{DC}$	1	0	0	1	1	1	$+V_{DC}$	$+V_{DC}/2$
0_P	1	0	0	1	0	1	0	$+V_{DC}/2$
0_N	0	1	0	1	1	0	0	$+V_{DC}/2$
$-V_{DC}$	0	1	1	0	1	1	$+V_{DC}$	$+V_{DC}/2$

Table 2.6: Switching states for H6 inverter.



(a) (b)

Figure 2.14: PWM signals for (a) standard and (b) UniTL modulation.

this topology. The main advantage of this strategy respect to the one proposed in [27] is that the effective output current ripple is at twice the switching frequency. The H-bridge legs are driven by different duty cycles (S_1 and S_3): this means that the free-wheeling will happen in both the upper and lower parts of the H-bridge, thus effectively doubling the output voltage frequency. A dead time exists between the commutations of the complementary pairs (S_1-S_2 and S_3-S_4). The DC decoupling transistors are switched off at the beginning of each free-wheeling phase. In particular S_5 is switched off when the output current free-wheels in the upper part of the H-bridge, when the current free-wheels in the lower part, S_6 device is to be switched off. As a matter of fact, a lead-lag time between the commutations of the DC decoupling and H-bridge transistors can be adopted to reduce the common mode voltage [28]. Although four devices are conducting in active states, the H6 topology with UniTL PWM scheme promises higher efficiency in comparison to full-bridge with unipolar and bipolar modulations due to lower switching losses. A theoretical loss analysis of these inverter is presented in [24].

2.2.2 Half-Bridge Derived Topologies

2.2.2.1 Neutral Point Clamped (NPC) Inverter

Neutral point clamped (NPC) inverter has been introduced in [29] showing lower dV/dt, switch stress and reduced filter requirements by providing three level output voltage waveform and commutation at half of DC link voltage in comparison to conventional two-level half-bridge inverter, presented in Fig. 2.6. The DC link of the inverter is formed by two series capacitors that equally share DC link voltage. The neutral wire of the grid is connected to the mid-point of the DC voltage source, whereas phase wire is connected to filter inductor L_f. The NPC inverter schematic for single-phase system is presented in Fig. 2.15.

The inverter is formed by four series connected active switches S_1-S_4 and two clamping diodes D_1 and D_2, connected to neutral point of DC link capacitors C_{DC1} and C_{DC2}.

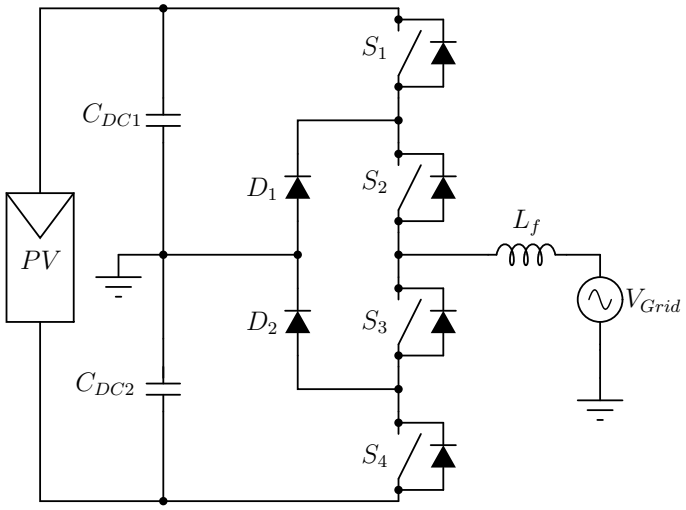


Figure 2.15: Neutral-point-clamped (NPC) inverter.

All of the active switches and diodes are rated at half of DC link voltage $V_{DC}/2$. Consequently, it is possible to use power devices at the 600 V class for grid-connected applications, where the DC link voltage is within a range of 650-1000 V. The switching states of NPC inverter is presented in Table 2.7. The outer switches S_1 and S_4 are switched at switching frequency while inner switches S_2 and S_3 are switched at grid frequency in order to achieve three level output voltage. NPC inverter requires double input voltage in comparison to full bridge topologies and unbalanced switching losses between outer switches $S_{1(4)}$ and inner switches $S_{2(3)}$. The total common mode voltage V_{CM_t} is expressed in Eq. 2.6 as the summation of common mode voltage at the output of the inverter V_{CM_1} and across the filter inductors V_{CM_2}. The value of V_{CM_1} and V_{CM_2} at each switching state for calculation of V_{CM_t} are also presented in Table 2.7. It can be seen that the V_{CM_1} and V_{CM_2} vary with respect to the change output voltage, but the common mode voltage V_{CM_t} is fixed to $+V_{DC}/2$. Therefore it can be concluded that the asymmetrical placement of output filter inductor provides constant V_{CM_t} and any inductance introduced to neutral point connection will lead to variation of common mode voltage and increase in leakage current according to Eq. 2.6.

Output State	S_1	S_2	S_3	S_4	V_{DM}	V_{CM_1}	V_{CM_2}	V_{CM_t}
$+V_{DC}$	1	1	0	0	$+V_{DC}/2$	$+3V_{DC}/4$	$-V_{DC}/4$	$+V_{DC}/2$
0_P	0	1	0	0	0	$+V_{DC}/2$	0	$+V_{DC}/2$
0_N	0	0	1	0	0	$+V_{DC}/2$	0	$+V_{DC}/2$
$-V_{DC}$	0	0	1	1	$-V_{DC}/2$	$+V_{DC}/4$	$+V_{DC}/4$	$+V_{DC}/2$

Table 2.7: Switching states for NPC inverter.

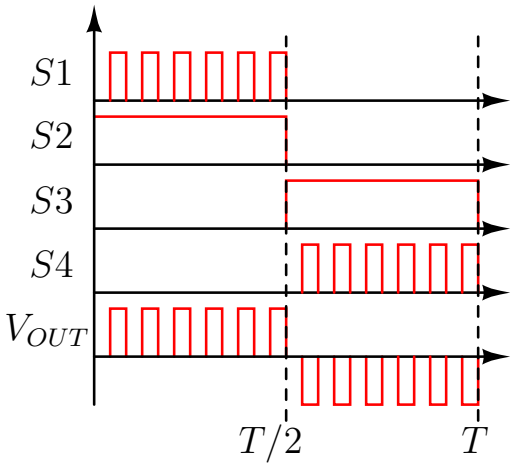


Figure 2.16: PWM signals for NPC inverter.

2.2.2.2 Active Neutral Point Clamped (ANPC) Inverter

Active neutral point clamped (ANPC) inverter is a member of half-bridge neutral point clamped inverter family and it was introduced in [30], [31] as an alternative to the neutral point clamped (NPC) inverter for improved loss balancing and better utilization of semiconductor chip areas in the inverter. Replacing diodes in the NPC inverters with active switches provides additional zero states, and at the same time different modulation strategies can be applied with a flexible utilization of the redundant switching states.

The topology has been discussed thoroughly for industrial drive applications in literature [32, 33, 34, 35]. The schematic of converter is presented in Fig. 2.17. As it can be observed, the ANPC inverter is formed by 6 active switches S_1-S_6 in order to achieve a three-level output voltage, and the power devices are rated at a half of the DC-link voltage $V_{DC}/2$. Same as NPC inverter, it is possible to use power devices at the 600

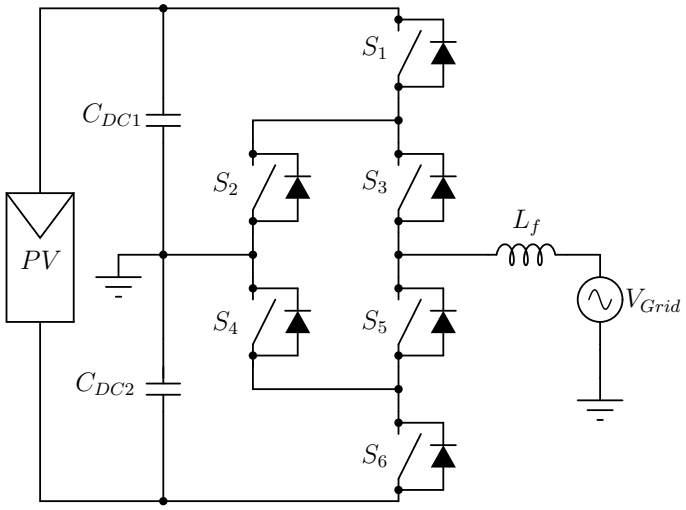


Figure 2.17: Active neutral-point-clamped (ANPC) inverter.

Output State	S_1	S_2	S_3	S_4	S_5	S_6	V_{DM}	V_{CM_t}
$+V_{DC}$	1	0	1	1	0	0	$+V_{DC}/2$	$+V_{DC}/2$
0_P	0	1	1	0	0	0	0	$+V_{DC}/2$
0_N	0	0	0	1	1	0	0	$+V_{DC}/2$
0_{PN}	0	1	1	1	1	0	0	$+V_{DC}/2$
$-V_{DC}$	0	1	0	0	1	1	$-V_{DC}/2$	$+V_{DC}/2$

Table 2.8: Switching states for ANPC inverter.

V class for grid-connected applications. The switching states for ANPC inverter are presented in Table 2.8. The redundant states in zero output voltage can be utilized in PWM schemes in order to balance the switching losses. Same as NPC inverter, the output has three voltage levels, common mode voltage is fixed to $+V_{DC}/2$ and introduction of inductance to neutral point connection can lead to increased ground leakage current.

Different modulation strategies have been discussed for the ANPC inverter in order to achieve a balanced switching loss distribution or doubling of the effective switching frequency at the output [36]. Solutions proposed in [32, 33, 34, 35] are limited to the use of Si devices and were optimised for IGBTs as well as for MOSFETs. A modulation strategy based on reverse conduction capability of SiC MOSFETs has

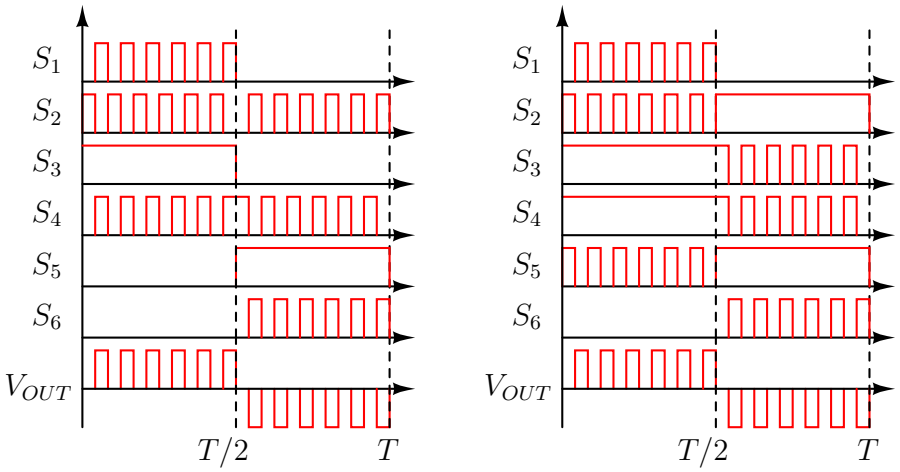


Figure 2.18: PWM signals for (a) conventional modulation and (b) optimised modulation for reverse conduction capability.

been introduced in [37], [38]. The positive voltage is applied to the output by turning-on S_1 and S_3 and the output current flows through the two devices in series. During the positive active-state, S_4 ensures an equal DC-link voltage sharing between S_5 and S_6 without conducting any current. The transition from positive active-state to zero-state is accomplished by switching S_1 off, and then simultaneously switching S_2 and S_5 on, and thus the current is divided in two parallel paths: S_2-S_3 and S_4-S_5. Same commutation scheme is used for complementary switches during the negative active-state and the zero-state. This modulation method ensures low conduction losses at zero-states, with the penalty of asymmetrical switching loss distribution. At unity power factor operation, which is required at steady state operation by standards [5], the outer switches (S_1 and S_6) are subject to switching losses. In other cases where the output voltage and the output current have different polarity, complementary inner switches ($S_{2(3)}$ and $S_{5(4)}$) are subject to switching losses. Therefore the distribution of switching losses are dependent on power factor. The conventional and reverse conduction optimised PWM signals are presented in Fig. 2.18.

2.2.2.3 T-Type Inverter

T-Type inverter, also known as Neutral Point Piloted (NPP) or Bi-directional Switched Neutral Point Clamped (BSNPC) inverter, is a member of neutral-point-clamped inverter topologies with three output voltage levels [39], [40]. It is one of the interesting topologies for single-phase three-level inverter systems and is used in commercial products [5]. The schematic of the converter and switching strategy signals are presented in Fig. 2.19 and Table 2.9 respectively. Switches that are forming the half bridge S_1 and S_4 are rated at V_{DC} and bi-directional switch S_2 and S_3 are rated at $V_{DC}/2$. Control and implementation of T-type converter in various applications such as renewable converters and fault-tolerant systems are discussed in literature [41, 42, 43, 44, 45, 46]. The switching strategy for this topology is published in [47] and PWM signals are presented in Fig. 2.20. The commutation of output current takes place between S_1 and S_2 in the positive half and between S_3 and S_4 in the negative half wave. S_3 is completely on during positive half and S_2 is completely on during negative half of the output current in order to utilize the reverse conduction capability of power devices such as MOSFETs and High Electron Mobility Transistors (HEMTs). In this setup, S_1 and S_4 switches have to withstand full-DC link voltage V_{DC}, S_2 and S_3 switches have to withstand half of DC-link voltage $V_{DC}/2$. Like in NPC and ANPC inverter, same common mode analysis can be carried out and can be seen that common mode voltage at the output of the inverter is fixed to $+V_{DC}/2$.

Output State	S_1	S_2	S_3	S_4	V_{DM}	V_{CM_t}
$+V_{DC}/2$	1	0	1	0	$+V_{DC}/2$	$+V_{DC}/2$
0	0	1	1	0	0	$+V_{DC}/2$
$-V_{DC}/2$	0	1	0	1	$-V_{DC}/2$	$+V_{DC}/2$

Table 2.9: Switching states for T-Type inverter.

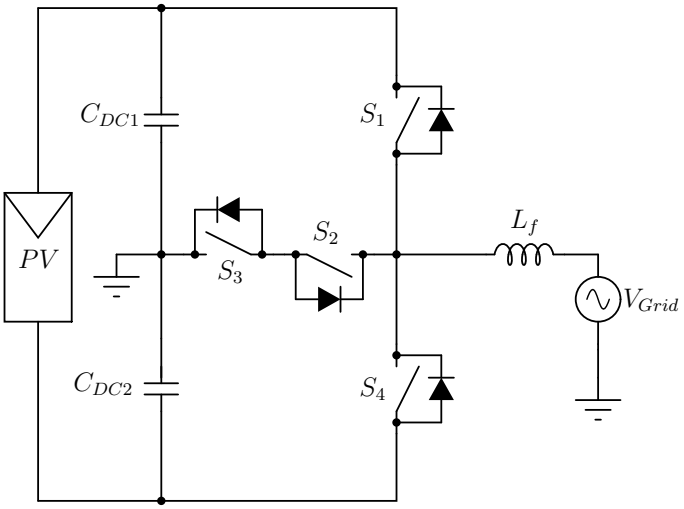


Figure 2.19: T-Type inverter.

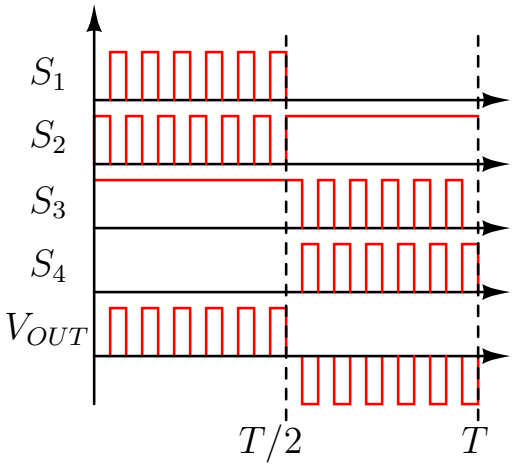


Figure 2.20: PWM signals for T-Type inverter.

2.3 Simulation-Based Benchmark and Analysis

The presented transformerless inverter topologies are simulated in a grid connected system in order to evaluate the efficiency performance under wide load range with state-of-the-art Si IGBT and Si diodes. Infineon 650V IGBT IKP20N60H3 and 1200V IGBT IKW25N120H3 with antiparallel Si diodes have been used for efficiency evaluation [48], [49]. The considered grid connection arrangement is presented in Fig. 2.21, and converter, grid and output filter parameters for the simulation model are presented in Table 2.10. Single stage LC filter has been used in order to keep the Total Harmonic Distortion (THD) less than 5% and comply with grid requirements in Table 2.1. The inductance and capacitance values have been selected in order to set inductor ripple current to 20 % of maximum output current and cut-off frequency of the LC filter to 10 times of output ripple frequency f_{OUT}. According to these assumptions, Filter 2 in Table 2.10 is used for full-bridge inverter with bipolar modulation and Filter 1 is used for the rest of the topologies. Finally, the grid inductance is estimated as 40 μH, which is a reasonable value for low voltage grid systems.

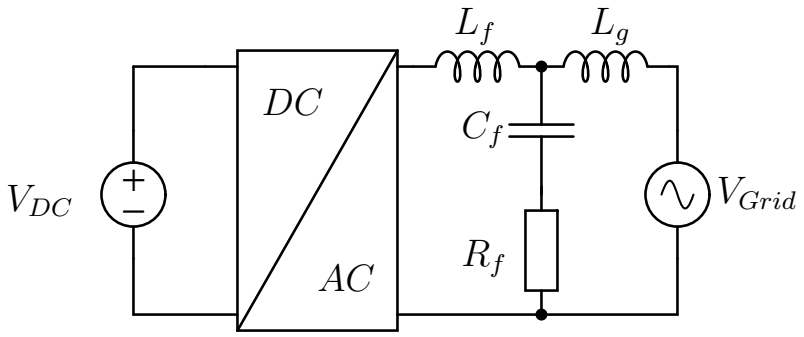


Figure 2.21: Grid connected string inverter.

The maximum output power $P_{OUT_{MAX}}$ for each inverter is 2.5 kW and the input DC link voltage for full bridge and NPC topologies is 400 V and 800 V respectively in order to feed power to 230 V_{rms}, 50 Hz European grid system. The switching frequency is chosen to be 16 kHz or 32 kHz depending on topology in order to provide fixed 32 kHz output ripple current across filter inductor L_f. The dead time between complementary

Converter Parameters

V_{DC} [V]	$P_{OUT_{MAX}}$ [W]	f_{sw} [kHz]	f_{OUT} [kHz]	T_h [°C]	t_{dt} [ns]
400/800	2500	16/32	32	50	500

Grid Parameters			**Filter 1**		**Filter 2**	
L_g [H]	V_{Grid} [V]	f_{Grid} [Hz]	L_f [H]	C_f [F]	L_f [H]	C_f [F]
40μ	230	50	1m	2.7μ	2m	1.5μ

Table 2.10: Simulation conditions for full-bridge and neutral point clamped based inverters.

switching devices is set to 500 ns and the heat sink temperature for power devices is fixed to 50 °C. Power losses across each semiconductor has been measured in order to asses power cell performance for each inverter under same operating conditions. Simulations have been carried out with PLECS® Standalone tool [50], [51]. The acronyms for the topologies are presented in Table 2.11 and the comparison of main parameters of each topology is presented in Table 2.12.

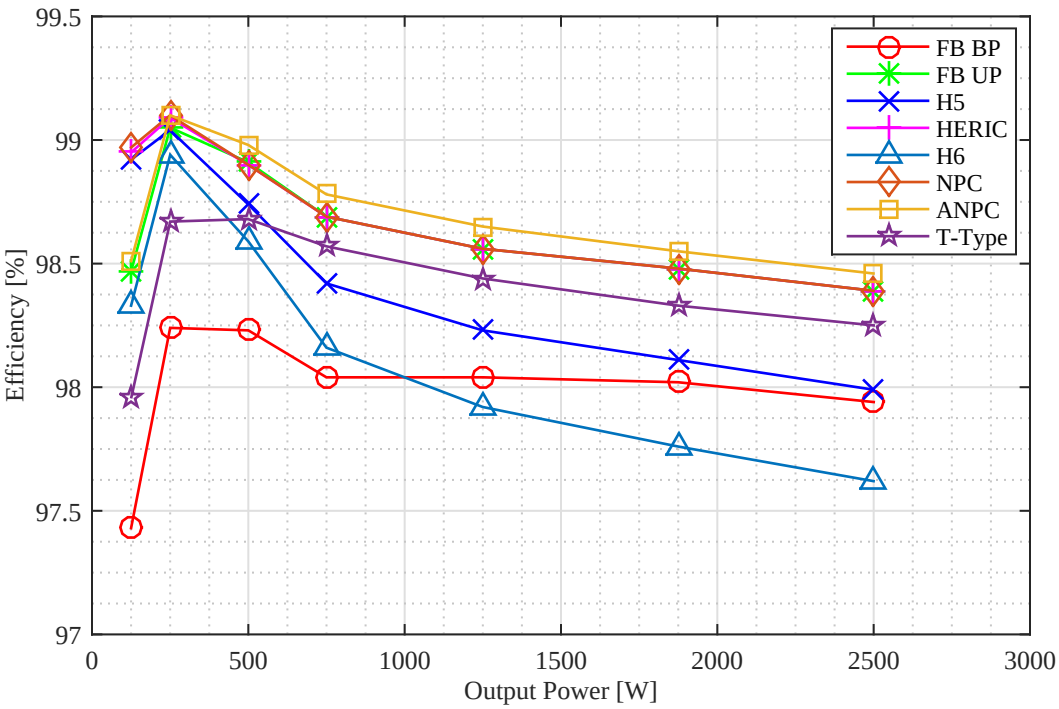


Figure 2.22: Efficiency comparison of full bridge and neutral point clamped based inverters under different load conditions.

Topology	Acronym
Full-bridge inverter with bipolar modulation	FB BP
Full-bridge inverter with unipolar modulation	FB UP
Highly efficiency and reliable inverter concept	HERIC
Neutral point clamped inverter	NPC
Active neutral point clamped inverter	ANPC

Table 2.11: Acronyms for the simulated topologies presented in Table 2.12

	Full-Bridge Derived					Half-Bridge Derived		
Topology	FB BP	FB UP	H5	HERIC	H6	NPC	ANPC	T-Type
DC-Link Voltage	400 V	400 V	400 V	400 V	400 V	800 V	800 V	800 V
Input Capacitor $I_{pk-pk} = 20\%in$ $V_{pk-pk} = 3\%V_{in}$	1500 μF	1500 μF	1500 μF	1500 μF	1500 μF	3000 μF each	3000 μF each	3000 μF each
Input Capacitor Energy	120 J	120 J	120 J	120 J	120 J	480 J	480 J	480 J
Switching Frequency	32 kHz	16 kHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz	32 kHz
Output Inductor L_f	2 mH	1 mH	1 mH	1 mH	1 mH	1 mH	1 mH	1 mH
Output Capacitor C_f	2.7 μF	1.5 μF	1.5 μF	1.5 μF	1.5 μF	1.5 μF	1.5 μF	1.5 μF
Number of Switches	4	4	5	6	6	4	6	4
Number of Diodes	0	0	0	0	2	2	0	0
Switch Voltage Rating	600 V	600 V	600 V	600 V	600 V	600 V	600 V	2×1200 V 2×600 V
Switch Current Rating	6.94 A	7.11 A	2×7.70 A 2×6.47 A 1×9.15 A	2×6.49 A 2×4.14 A	2×7.12 A 2×9.15 A	2×6.4 A 2×7.6 A	2×6.42 A 2×6.5 A 2×2.83 A	2×6.49 A 2×4.16 A
Diode Voltage Rating	600 V	600 V	600 V	600 V	600 V	600 V	600 V	2×1200 V 2×600 V
Diode Current Rating	3.34 A	2.95 A	2×4.17 A	2×4.14 A	2×2.9 A 2×0.3 A	2×4.16 A	2×2.83 A 2×1.4 A	2×4.16 A
Power Cell Efficiency at Full Load	97.94%	98.39%	97.99%	98.39%	97.62%	98.39%	98.46%	98.25%

Table 2.12: Comparison table for different inverter topologies.

The efficiency curves of each inverter under various load conditions excluding gate driver and auxiliary supply losses are presented in Fig. 2.22 and semiconductor loss breakdown of each inverter at 2.5 kW output power is presented in Fig. 2.24. The ANPC topology has the highest efficiency among 8 topologies and is followed by NPC, full-bridge with unipolar modulation (FB UP), HERIC and T-Type topologies. As it is mentioned before, full-bridge inverter with unipolar modulation is not suitable for transformerless applications due to high ground leakage current, but it has been presented in order to compare with other presented topologies. It is clear that number of devices in conduction plays a significant role in the efficiency of the inverter at high output power values. Apart from FB BP, all of the topologies achieve higher than 98 % efficiency under wide load range and show promising performance for string based transformerless inverter systems.

The efficiency of the inverters under partial loads are critical as most of the PV systems operate at partial loads throughout the year due to variation of solar irradiance and ambient temperature. In Europe, the European Union (EU) defined the standard for inverter efficiency considering efficiencies between 5 % and 100 % with different weight factors and is presented in Eq. 2.7 [52]. On the other hand, California Energy Commission (CEC) defined inverter efficiency with different weight factors for loads between 10 % and 100 %, and is presented in Eq. 2.8 [53].

$$\eta_{EURO} = 0.03 \cdot \eta_{5\%} + 0.06 \cdot \eta_{10\%} + 0.13 \cdot \eta_{20\%} + 0.10 \cdot \eta_{30\%} + 0.48 \cdot \eta_{50\%} + 0.20 \cdot \eta_{100\%} \quad (2.7)$$

$$\eta_{CEC} = 0.04 \cdot \eta_{10\%} + 0.05 \cdot \eta_{20\%} + 0.12 \cdot \eta_{30\%} + 0.21 \cdot \eta_{50\%} + 0.53 \cdot \eta_{75\%} + 0.05 \cdot \eta_{100\%} \quad (2.8)$$

Finally, the loss breakdown in Fig. 2.24 provides valuable information about how the semiconductor losses affect efficiency of different topologies. H6 topology suffers from high number of conducting switching during active states and has the highest conduction losses among 8 topologies. On the other hand, T-Type inverter suffers from switching losses of 1200V IGBTs as it is the only topology that uses 1200V switches for grid connected application.

According to Eq. 2.7 and Eq. 2.8, efficiencies of the simulated inverters have been calculated and presented in Fig. 2.23. For all of the simulated inverters, efficiency

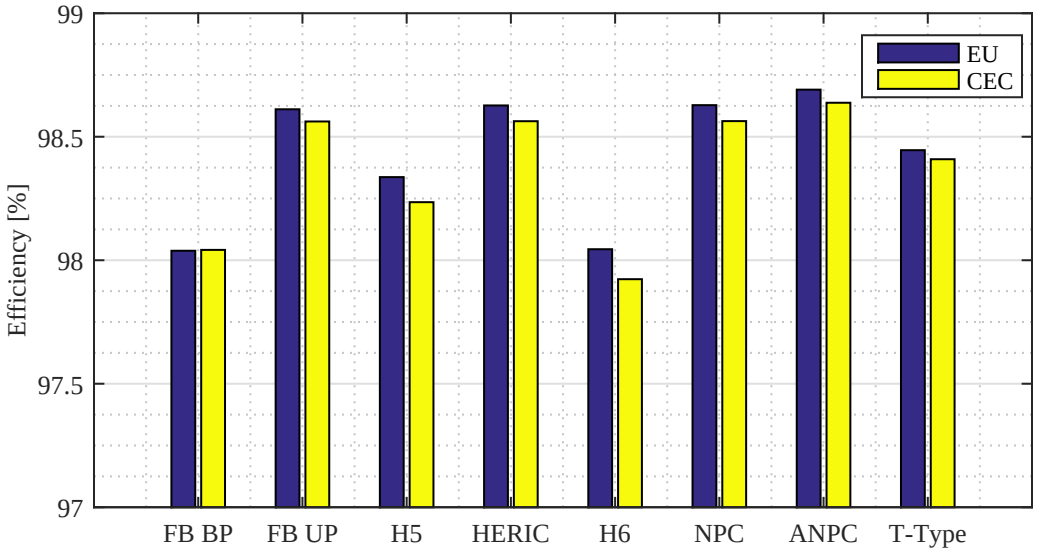


Figure 2.23: Efficiency comparison of full-bridge and half-bridge derived inverters based on EU and CEC efficiency definitions.

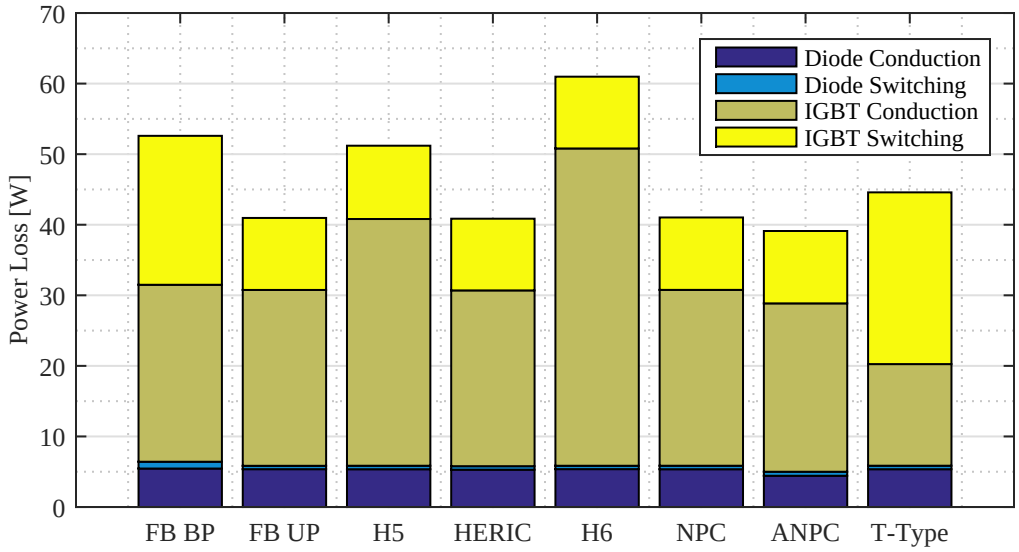


Figure 2.24: Semiconductor loss breakdown for each converter at 2.5 kW output power.

is higher with EU formula but the relative comparison does not change for both EU and CEC cases. ANPC inverter has the highest efficiency among all topologies and is followed by HERIC, NPC, T-Type, H5 and H6.

2.4 Conclusions

In this chapter, historical overview of PV systems, grid requirements for PV inverters, comparison of PV systems with different conversion stages, ground leakage current requirements and challenges for transformerless inverter topologies have been discussed. State-of-the-art transformerless inverters based on full-bridge and NPC topologies for string PV systems have been presented. Presented inverters have been simulated with conventional Si based power devices and single-phase grid connection in order to assess the performance under different load conditions. The results show that transformerless topologies can achieve very high efficiency (> 98 %) and can maximise the energy generation from PV module under wide load conditions. The loss comparison of topologies showed that ANPC topology has the highest efficiency among eight topologies due to high switching and conduction performance under wide load range.

Chapter 3

Wide-Bandgap Power Devices

Wide-bandgap (WBG) materials (e.g. SiC, GaN, diamond) are considered strong candidates to replace silicon (Si) for semiconductor development due to superior material properties. Since the introduction of the first Si based solid-state switches, it took almost half a century for the first wide-bandgap based power device (SiC Schottky-barrier diode) to become commercially available. With SiC based devices, introduction of SiC Schottky-barrier diode is followed by fully-controlled power switches at blocking voltage range above 600 V such as MOSFETs, and normally-on and off Junction Field-Effect Transistors (JFETs). With GaN based devices, 600 V vertical diodes were produced as samples but discontinued due to commercial reasons (expensive substrate and strong competition from SiC Schottky-barrier diode) and the development resources were focused on HEMTs. These devices in SiC and GaN show superior switching and conduction performance over wide temperature range in comparison to Si based IGBTs and therefore have been considered as promising solution for high-efficient inverters for transformerless PV systems. In this chapter, properties of WBG materials, and state-of-the-art WBG power devices are discussed and compared with their counterparts.

3.1 Wide-Bandgap Material Properties

Silicon is the well established material for the fabrication of power semiconductor devices since the introduction of thyristors and diodes in 1950s. Due to device production process improvements and device optimisation over the years, the intrinsic material properties of Si are becoming the limiting factor for the performance of power devices and therefore power converters to further drive evolution according to industrial expectations [54], [55]. Along with work on super junction device development [56], a lot of effort is spent on device development with wide-bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN). In this section, properties of WBG materials with Si is compared and the impact on device properties such as switching, conduction and blocking performances are discussed.

An ideal power switch is desired to perform with zero conduction loss, zero switching loss and infinite voltage blocking capability to achieve high performance in power converters. Therefore, the material that is used to develop power devices should have the properties to satisfy these three requirements as much as possible. In solid materials, electrons are located around the atom at different energy bands. The top energy band and the next lower band are called conduction band and valence band respectively. The current conduction in a material is achieved by electrons in conduction band moving from one atom to another. The break of an electron also creates a hole in the valence band of the atom and leaves it positively charged. The holes can also move in the materials in the opposite direction of of electrons and contribute to current conduction. It should be noted that the mobility of electrons are higher than holes.

Simplified energy bands for metal, semiconductor and insulator are illustrated in Fig. 3.1. The valance and conduction band in semiconductors and insulators are separated by a bandgap E_g. The E_g represents the amount of energy to break the electrons out of the bonds in valence band and move them to conduction band, or vice versa. For metals, the conduction and valence bands are overlapped, thus the E_g does not exist. For semiconductors, the conduction band is almost empty and the bandgap varies de-

Property	**Si**	**4H-SiC**	**GaN**	**Diamond**
Bandgap, E_g [eV]	1.12	3.26	3.39	5.47
Dielectric Constant, ε_r	11.8	9.7	9.0	5.7
Electric Breakdown Field, E_{crit} [MV/cm]	0.23	2.2	3.3	5.6
Electron Mobility, μ_n [cm^2/V·s]	1400	950	1500	1800
Saturated electron drift velocity, v_{sat} [$\times 10^7$ cm/s]	1	2	2.5	2.7
Thermal Conductivity, λ [W/cm·K]	1.5	3.8	1.3	22
Baliga's Figure of Merit [$BFoM$]	1	500	2400	9000

Table 3.1: Material properties of Si and WBG materials [55], [59].

pending on the properties of semiconductor material. Semiconductor materials allow thermal excitation of electrons into their conduction band below their melting point. Therefore the requirements of a power switch (conduction, blocking and switching) can be satisfied with semiconductor materials. [57], [58].

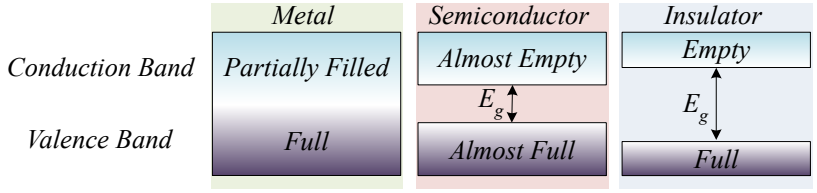


Figure 3.1: Simplified energy diagram of solid metal, semiconductor and insulators.

Within semiconductor materials, the family of materials which require more than 1.7 eV to 2.5 eV bandgap energy to move an electron from valence band to conduction band or vice versa are called wide-bandgap semiconductors. Some key material properties of popular WBG materials SiC (4H-SiC polytype), GaN, diamond, and Si are presented in Table 3.1. It can be seen that the bandgaps of SiC, GaN and Diamond are about 3 to 5 times higher than the bandgap of Si. This means that higher energy temperature is required to break the bond of an electron and move it from one band to another.

Wide-bandgap materials have naturally lower intrinsic carrier concentration n_i in comparison to Si, due to the higher E_g. n_i depends exponentially on E_g and temperature, and, as the leakage current of devices is proportional to n_i and n_i^2, WBG based devices can operate at much higher temperatures with same leakage current in Si based devices or at the same temperature with Si much lower leakage current. The

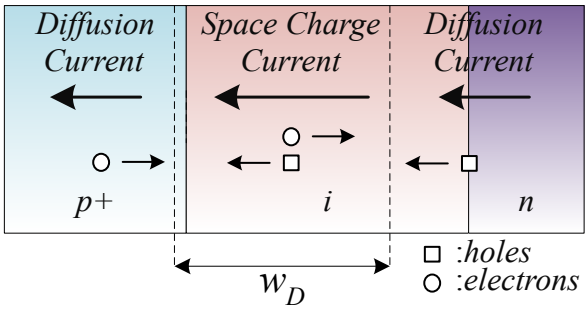


Figure 3.2: Leakage currents in a P-i-N diode under reverse bias voltage [57].

n_i has also an impact on on-state performance of power devices. The built-in potential across the forward biased pn junction caused by space charge region (depletion region) at thermal equilibrium is defined as:

$$V_{bi} = \frac{k \cdot T}{q} \cdot ln(\frac{N_a \cdot N_d}{n_i^2}) \tag{3.1}$$

where N_a and N_d are acceptor and donor densities, k is Boltzmann constant, T is temperature, q is elementary charge. Although the built-in voltage does not represent the total voltage drop, it has a strong contribution in conduction losses. Therefore the built-in potential is important for calculation of on-state performance of power devices [57]. As the pn junction is reverse biased in blocking mode, the depletion region is extended to withstand the reverse bias voltage. In this case, the leakage current for a reverse biased pn junction is formed by two components: 1) space-charge generation current and 2) diffusion current [57]. The leakage current in a P-i-N rectifier where i region is low doped n layer to form the depletion region w_D is illustrated in Fig. 3.2. For space-charge generation current, any electron-hole pairs generated within depletion region are swept out as shown in Fig. 3.2. According to [57], the additional component to the space-charge generation is the diffusion current caused by minority carriers in $p+$ and n regions. Any minority carriers generated in the proximity of the junction can diffuse to the depletion region boundary and get swept to the opposite side of the junction by the electric field across the depletion region.

In this case, the total leakage current per unit area in a P-i-N diode is summation of diffusion current in $p+$ layer $J_{Diff-p+}$, space charge current J_{SC} and diffusion current

in n layer J_{Diff-n}, and is given by:

$$J_{LT} = J_{Diff-p+} + J_{SC} + J_{Diff-n} \tag{3.2}$$

$$J_{LT} = \frac{q \cdot D_n \cdot {n_i}^2}{L_n \cdot N_{AP+}} + \frac{q \cdot (2d) \cdot n_i}{\tau_{SC}} + \frac{q \cdot D_p \cdot {n_i}^2}{L_p \cdot N_{DN+}} \tag{3.3}$$

As it is shown with the built-in voltage drop in Eq. 3.1 and leakage current under reverse bias in Eq. 3.3, the n_i has strong impact on on-state and blocking performance of a power device. While the leakage current is reduced in proportion to n_i and ${n_i}^2$, the built-in voltage is increased.

The second advantage of wider bandgap is a higher electric breakdown field E_{crit}, which is the maximum field that can be applied across the semiconductor before avalanche breakdown. The one-dimensional reverse biased P-i-N diode with non punch through (NPT) and punch through (PT) designs are presented in Fig. 3.3. In NPT based design, the electrical field starts and terminates at the low doped n region with a triangular field distribution. In PT based design, the electrical field is has a trapezoidal shape across low doped i region and terminated at the junction of $p+$ and n layers. The advantage of PT design is reduction of the length depletion region w_D by reducing the doping density and increasing the electrical field across the region for same blocking voltage. With different semiconductor materials, as the E_{crit} increases, it is possible to make thinner devices for same blocking voltage.

The breakdown voltage V_{BR} for a non punch through device in Fig. 3.3 can be calculated as [59]:

$$V_{BR} = 0.5 \cdot w_{drift} \cdot E_{crit} \tag{3.4}$$

where w_{drift} is drift region thickness. The E_{crit} of SiC and GaN is approximately 10 times and 15 times higher than Si respectively. This means the drift region can be 10 and 15 times thinner in comparison to Si. The thickness of the drift region can be expressed as a function of doping density N_d, and E_{crit} with the following equation [60]:

$$w_{drift} = \frac{E_{crit} \cdot \varepsilon_0 \cdot \varepsilon_r}{q \cdot N_d} \tag{3.5}$$

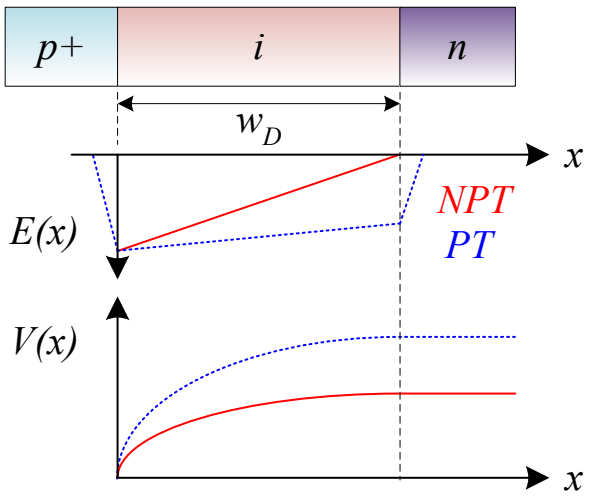


Figure 3.3: Electric field and voltage across depletion region in a P-i-N diode.

where ε_0 is permittivity of vacuum and ε_r is dielectric constant of semiconductor material. It can be seen that with the change from Si to SiC and GaN, the doping density in the drift region has to be increased by 100 and 225 times respectively for same blocking voltage. The increased doping density has a strong impact on on-state resistance of the drift region. By combining Eq. 3.4 and 3.5, the relation between N_a and E_{crit} can be expressed as:

$$N_d = \frac{{E_{crit}}^2 \cdot \varepsilon_0 \cdot \varepsilon_r}{2 \cdot q \cdot V_{BR}} \tag{3.6}$$

The resistance of the drift region r_{on} is defined in [61] as:

$$r_{on} = \frac{w_{drift}}{q \cdot \mu_n \cdot N_d} \tag{3.7}$$

where μ_n is the electron mobility. According to [61], by using Eq. 3.4 and 3.6, Eq. 3.7 can be linked to ε_r, μ_n and E_{crit} and V_{BR} with the following equation:

$$r_{on} = \frac{4 \cdot V_{BR}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot \mu_n \cdot {E_{crit}}^3} \tag{3.8}$$

It is clear that drift region resistance is dependent on material properties presented in Table 3.1 along with required breakdown voltage. Based on Eq. 3.8, in [62], Baliga's

figure of merit $BFoM$ is defined and presented in Table 3.1 for Si and WBG materials:

$$BFoM = \varepsilon_r \cdot \mu_n \cdot E_{crit}^3 \tag{3.9}$$

$BFoM$ provides information about the conduction losses with respect to material properties in unipolar devices. From Table 3.1, it can be seen that $BFoM$ of WBG materials are significantly larger than Si. In other words, if $BFoM$ is taken into account for comparison of materials, on-state resistance of a unipolar device based on GaN and SiC can be decreased by factor of 2400 and 500 in comparison to Si based unipolar device at same blocking voltage. This does not mean that a chip size reduction by factor of 2400 and 500 is realistic due to increased loss density. The same amount of power can not be dissipated in 2400 or 500 times smaller chip due to thermal restriction [59].

3.2 State-of-the-Art WBG Power Devices

In this section, different devices structures at 600 V blocking voltage range are discussed and compared in terms of physical structure. The discussion starts with diodes including Si and SiC based, and continues with state-of-the-art fully controlled discrete switches that are suitable for residential scale PV systems.

3.2.1 P-i-N Diode and Schottky Barrier Diode

3.2.1.1 Si P-i-N Diode

The P-i-N diode is based on the principle of pn junction and is designed to handle large conduction current and blocking voltage in power electronic converters. The structure of a P-i-N power diode is presented in Fig. 3.4. The structure consists of three layers excluding metal contacts: $p+$ layer, $n-$ layer and $n+$ substrate. The $n+$ substrate is a highly doped n layer and $n-$ epitaxial layer is grown with specified

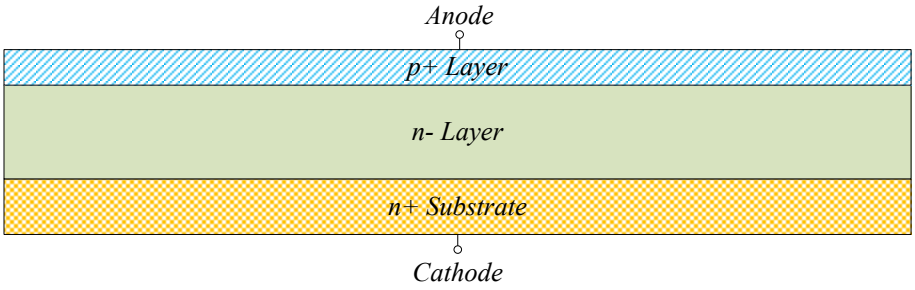


Figure 3.4: P-i-N diode structure

thickness. Then, the pn junction is formed by diffusion of $p+$ on $n-$ to complete the P-i-N structure.

The $n-$ layer provides high voltage capability to P-i-N diode and does not exist in low-power diodes. The depletion layer is formed across $n-$ layer and therefore the thickness of the $n-$ layer (low-doped base region) is determined by the breakdown voltage of the diode. For a specific breakdown voltage, the $n-$ layer can be dimensioned with two different designs: 1) Non-punch through NPT, 2) Punch through PT. The electrical field distribution for these two types are presented earlier in Fig. 3.3. In NPT diodes, the electric field distribution is triangular shaped and the length of $n-$ layer is longer than depletion layer length. Therefore, the depletion layer is contained almost entirely in $n-$ layer. In PT diodes, the thickness of $n-$ layer can be reduced by reducing doping density of the layer and increasing the maximum electric field. In this case, the depletion region is longer than $n-$ layer and is terminated at $n+$ layer with trapezoidal electric field distribution across depletion region. In PT diodes, although $n-$ layer is shorter than in NPT diodes, it has higher ohmic resistivity due to reduced doping. However, high resistivity does not have significant impact on the operation of the diode as the drift region in the diode is shorted by conductivity modulation. Due to short drift region, PT devices have smaller on-state voltage in comparison to NPT diodes [58]. Vertical structure is preferred in power devices as shown in Fig. 3.4 in order to maximise the cross-sectional area for current flow while minimising the junction to case thermal resistance. For high voltage, high current applications, the high voltage capability can be achieved by designing drift region thickness with respect to N_a and E_{crit} and the high current capability can be

achieved by paralleling vertical cells to achieve desired on-state performance.

The on-state performance of P-i-N diode is dominated by the conduction loss across lightly doped drift region. If a forward voltage applied to P-i-N diode, a part of the voltage is used at the junctions to reduce potential steps and also to raise the injected carrier density in the base region. And the remaining part is used to provide an ohmic voltage drop over $n-$ layer. Therefore, the on-state voltage of a P-i-N diode can be expressed by the following equation:

$$V = V_D + R_{on} \cdot I_D \tag{3.10}$$

where V_D is the on-state threshold voltage, R_{on} is on-state resistance and I_D is diode forward voltage [58], [60]. Si is the preferred material as WBG materials (e.g. SiC) has high on-state threshold voltage in P-i-N structure due to lower n_i (Eq. 3.1). With SiC in P-i-N diode, high conduction losses will occur, although the drift region thickness can be reduced due to higher E_{crit}.

The switching performance of P-i-N diode is determined by the turn-off transient that includes reverse recovery charge Q_{rr} and junction capacitance. During conduction of P-i-N diode, excess carrier charges fill the drift region due to conduction modulation, which is explained in the previous paragraphs, and these charges have to be removed before expanding the depletion region for blocking the reverse voltage. After removal of the excess carrier charges in drift region, the voltage across the diode will rapidly rise to the blocking voltage dominated by the DC-link voltage in inverter applications. In a half-bridge application, the reverse recovery charge of a diode will cause switching loss in the blocking diode and also additional turn-on losses across the complementary switch due to increase turn-on current caused by the reverse recovery current. The turn-off energy caused by reverse recovery current E_{rr} is expressed in [58] with the following equation:

$$E_{rr} = \frac{1}{2} \cdot L_\sigma \cdot I_{RRM}^2 + \frac{1}{2} \cdot V_{DC} \cdot I_{RRM} \cdot t_f \tag{3.11}$$

where L_σ is stray inductance in the commutation loop, I_{RRM} is maximum reverse recovery current, V_{DC} is diode blocking voltage and t_f is fall time of reverse recovery

current from I_{RRM} to zero. The L_σ can be rewritten in terms of rate of change of current in the diode and Eq. 3.11 can be rewritten as:

$$E_{rr} = \frac{1}{2} \cdot V_{DC} \cdot I_{RRM} \cdot t_s + \frac{1}{2} \cdot V_{DC} \cdot I_{RRM} \cdot t_f = \frac{1}{2} \cdot I_{RRM} \cdot t_{rr} \cdot V_{DC} \tag{3.12}$$

$$E_{rr} = Q_{rr} \cdot V_{DC} \tag{3.13}$$

where t_s is rise time of recovery current from zero to I_{RRM} and t_{rr} is total recovery time. It can be seen that the recovery losses are directly proportional to Q_{rr} and therefore in high frequency applications it is crucial to have diodes with low Q_{rr} for minimum switching losses. To make the Eqs. 3.11 and 3.12 more meaningful, I_{RRM}, t_s and t_f parameters can be linked to forward current amplitude I_F and rate of fall of forward current $\mathrm{d}I_F/\mathrm{d}t$. The relation between Q_{rr}, t_{rr} and $\mathrm{d}I_F/\mathrm{d}t$ are given in diode datasheets for different ambient temperatures to estimate reverse recovery loss. The physics-based models for turn-off losses in power diodes are discussed thoroughly in literature to link the Q_{rr}, t_{rr} and $\mathrm{d}I_F/\mathrm{d}t$ [63, 64, 65].

3.2.1.2 SiC Schottky Barrier Diode

The alternative structure to P-i-N diode for power diodes is Schottky barrier diode (SBD). SBD is a unipolar device and only one type of carrier is used for current conduction. SBD diodes typically achieve smaller on-state threshold voltage in comparison to P-i-N diodes due to higher reverse saturation current. The drift region thickness and on-state resistance for NPT design are presented in Eqs. 3.5 and 3.8. respectively. It can be seen from Eq. 3.8 that the on-state resistance is proportional to V_{BR}^2 and inversely proportional to E_{crit}^3. The on-state voltage drop across SBD is dominated by on-state threshold voltage across the metal-semiconductor interface and the voltage drop across drift region on-state resistance. Although the on-state threshold voltage is smaller than in P-i-N diode, the absence of conductivity modulation increases the ohmic resistance of drift region during forward conduction. In addition to high on-state resistance, the leakage current under reverse bias is inversely proportional to on-state threshold voltage, which are both functions of Schottky barrier height. In order to avoid large leakage current, high Schottky barrier height is

required which will increase the on-state threshold voltage. Therefore, SBD structure with Si is feasible up to 100-200 V blocking voltage range [57, 58, 60].

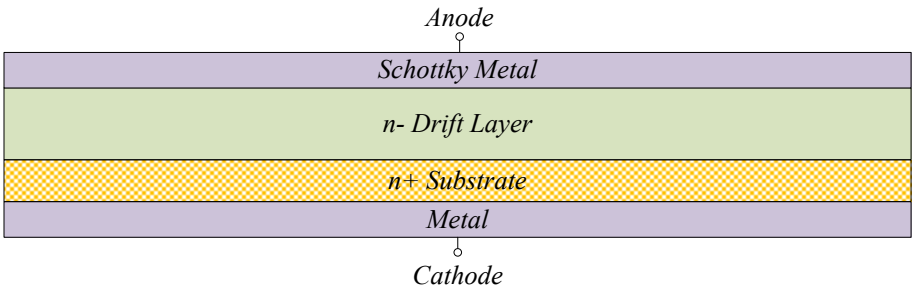


Figure 3.5: SiC based planar Schottky barrier diode structure.

The disadvantage of SiC in P-i-N structure can be avoided with SBD due to lower on-state threshold voltage. In addition to this, it is possible to achieve high voltage SBD with reasonable drift region resistance. There are two main reasons for this: 1) Drift region length with SiC is smaller due to higher E_{crit}, 2) the doping density can be higher due to smaller n_i as shown in Table 3.1. The structure of a SiC based planar SBD is presented in Fig. 3.5. The structure consists of a Schottky metal contact at anode which forms Schottky junction with $n-$ layer. Like in P-i-N diode, $n-$ layer is the drift layer and provides high voltage blocking capability and $n+$ layer is highly doped region. SBD utilises the difference between potential energies of electrons in different materials, in this case between an $n-$ doped semiconductor and the Schottky metal in Fig. 3.5. The depletion region is formed at Schottky junction with negatively charged Schottky metal and positively charged $n-$ layer. Eventually, the depletion region will become large enough that the flow of electrons will reach thermal equilibrium. It should be noted that only majority carriers are involved in this process and due to this reason SBD is a unipolar device. p doped materials can also be used to form SBD but n doped materials are preferred due to higher mobility of electrons in comparison to holes [58], [66].

The SBD has better switching performance in comparison to P-i-N diode due to absence of minority carrier. Therefore, during switch off there will be reverse current due to junction capacitance only. It should be noted that this current may not be negligible due to reduced length of depletion region (e.g., higher capacitance for a

given cross section) in SBD with SiC [60].

3.2.2 SiC MOSFET

The power MOSFET is a unipolar voltage controlled device through a gate terminal and is formed by *npn* and *pnp* structures. Two types of MOSFET can be formed with this alternating structure: enhancement (*npn*) and depletion (*pnp*) mode MOSFETs. The enhancement mode MOSFET uses *p*-type layer as the channel of the device and is formed as *npn* structure. On the other hand, depletion mode MOSFET utilises *n*-type layer as the channel and is formed as *pnp* structure. The enhancement mode devices are normally-off and use electrons as majority carriers. Furthermore, depletion mode devices are normally-on and use holes as majority carriers. As the electrons have almost three times higher mobility in comparison to holes and normally-off devices are preferred in power electronics due to safety and controllability concerns, enhancement mode MOSFETs are preferred over depletion mode MOSFETs for power applications.

Vertical MOSFETs are popular as high power electronics switches, like vertical diodes, for maximum utilisation of semiconductor area. Typical structure of an enhancement mode vertical power MOSFET is presented in Fig. 3.6. The MOSFET is formed by four layers of n-type and p-type materials. $n+$ layer at drain is the highly-doped substrate which is used for growth of other layers. After formation of $n+$ substrate, $n-$ layer is grown epitaxially and then p and $n+$ layers are diffused. The $n-$ layer is the drift region that contains the depletion region to withstand the desired drain-source voltage during off-state. Finally, the device structure is completed by growth of gate oxide and deposition of gate, source and drain metallisation.

The gate oxide insulates the gate from the p and $n-$ layers, therefore there is no minority carrier injection to control the current flow between drain and source of the MOSFET. It can be seen in Fig. 3.6 that the p layer is shorted to the source metallisation at the edges of the device. This connection provides two functions during the normal operation of MOSFET: 1) The *npn* structure forms a parasitic bipolar

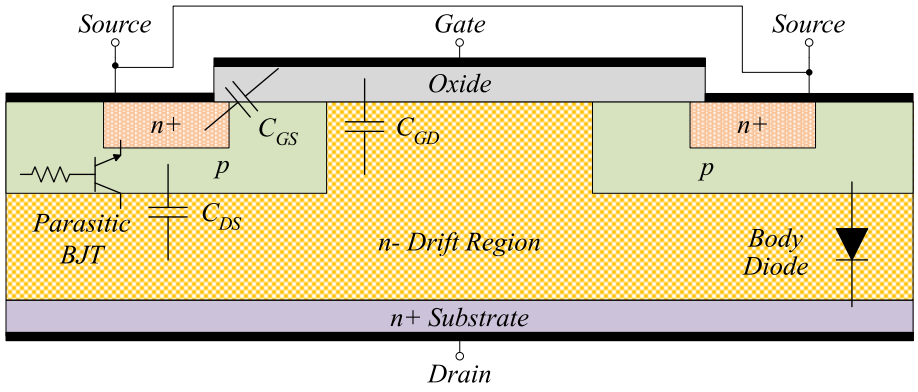


Figure 3.6: Vertical enhancement mode MOSFET structure.

junction transistor (BJT) and the connection of p layer to source shorts the base of BJT to the emitter. This connection ideally prevents any false turn-on during the blocking mode. At the connection, the doping can be increased by $p+$ implantation to reduce BJT base resistance. 2) On the other hand, the direct connection of p layer to the source forms a parasitic P-i-N body diode between the source and the drain of the MOSFET. Moreover, it can be seen that the $n-$ drift layer overlaps with gate oxide. This overlap enhances the conductivity of the $n-$ drift region under the gate during conduction. As the parasitic BJT is kept off by low resistance connection to the source, the breakdown voltage of the MOSFET is defined by the breakdown voltage of the body diode formed by $n+$, $n-$ and p layers. Three major parasitic capacitances C_{GS}, C_{GD} and C_{DS} are formed in a power MOSFET between gate, source and drain pads. The gate-source capacitance can be considered constant while gate-drain and drain-source capacitances are dependent on the drain-source voltage due to move of depletion region, depending on voltage across drain and source .

As it is mentioned earlier, the p layer connection to source metallisation forms a P-i-N diode across drain and source of the MOSFET. The diode has a poor reverse recovery performance in comparison to P-i-N or Schottky barrier diodes for the same blocking voltage, as the p and $n-$ layers are optimised for minimum R_{on} and minimum base resistance for parasitic BJT. Despite this, the diode can be used as an anti-parallel diode during dead time in synchronous rectification applications. The reverse conduction capability of the MOSFET is utilised by turning-on the channel after

certain dead time. Therefore, the body diode of the MOSFET can be used to conduct only during dead time between switching transitions of complementary switches and when body diode is used, the complementary switch will be subject to higher turn-on current due to reverse recovery charge of the the body diode.

The conductivity of the channel in MOSFET, consequently drain-source current, is controlled by gate-source voltage. When a positive gate-source voltage is applied, the positive voltage induces positive charge on the gate oxide. This positive charge on gate oxide repels the majority carrier holes in the p region and exposes the negatively charged acceptors. Further increase of the positive gate-source voltage begins to attract free electrons along with repelling free holes. When the gate-source voltage is large enough, the amount of free electrons in the region will be equal to the holes in the bulk body of p layer. These free electrons form the "inversion" layer which is highly conductive and have the same electrical properties as an n type material. Threshold gate-source voltage of a MOSFET is defined as the beginning of formation of inversion layer in an enhancement mode MOSFET [58], [60].

As no minority carriers are involved in the formation of the inversion layer, MOSFET is a majority carrier device and this brings significant benefits in terms of switching performance. During turn-on and turn-off, the gate does not source or sink minority carriers and this leads to increase in switching speed. The switching speed is determined by C_{GS} and C_{GD} capacitors as they need to be charged and discharged during switching transients by gate drive circuit. In a half-bridge configuration, the switching energy of a MOSFET can be determined by the following equations:

$$E_{Switch} = E_{on} + E_{off} \tag{3.14}$$

$$E_{on} = \frac{1}{2} \cdot V_{DS} \cdot (I_{DS} + I_{RRM}) \cdot t_{ri} + \frac{1}{2} \cdot V_{DS} \cdot (I_{DS} + \frac{2}{3} \cdot I_{RRM}) \cdot t_{fv} \tag{3.15}$$

$$E_{off} = \frac{1}{2} \cdot V_{DS} \cdot I_{DS} \cdot t_{rv} + \frac{1}{2}(V_{DS} + V_{pk}) \cdot I_{DS} \cdot t_{fi} \tag{3.16}$$

where I_{RRM} is the reverse recovery current of complimentary switch, t_{ri} is rise time of device current, t_{fv} is fall time of device voltage, V_{DS} is drain-source voltage and I_{DS} is drain-source current, t_{rv} is rise time of device voltage, t_{fi} is fall time of device current and V_{pk} is the voltage drop caused by commutation loop inductance [58].

On the other hand, the absence of the minority carriers eliminates the offset voltage during conduction but leads to increased channel and drift region resistance at higher currents in comparison to bipolar devices [57]. The on-state voltage drop of a MOSFET can be calculated by the following equation:

$$V_{on} = R_{on} \cdot I_{DS} \tag{3.17}$$

where R_{on} is the on-state resistance of the MOSFET when the device is turned-on. The on-state resistance in a high voltage power MOSFET is dominated by resistance of the low doped $n-$ layer. Similar to Eq. 3.7, the resistance of the low doped $n-$ layer can be calculated with the following equation [58]:

$$R_{n-} = \frac{w_B}{q \cdot \mu_n \cdot N_D \cdot A} \tag{3.18}$$

where A is the cross-section of the region. As the blocking voltage of MOSFET increases, the on-state resistance increases. Due to this reason, MOSFET structure is not viable above 600∼650 V blocking voltage range with Si. Super-junction MOSFETs at 600V class can also be counted as alternative device type due to good on-state performance. However, non-linear behaviour of output capacitance of super-junction devices places large transient load on the complementary switch and extensive reverse recovery charge increases turn-on losses in hard-switching topologies [67], [68].

At this point, WBG materials such as SiC become attractive solutions in comparison to Si in MOSFET structure for high voltage devices due to the benefits explained in Section 3.1. Specifically, SiC based unipolar devices are very attractive due to lower intrinsic carrier density and high electric breakdown field. These two properties allow higher doping density in drift region with thinner drift region thickness. Therefore the limitation of high drift layer resistance with Si above 600 V breakdown voltage can be overcome with SiC. The vertical SiC MOSFET has a similar structure as the Si version in Fig. 3.6. The SiC MOSFETs are currently commercially available between 600 V and 1700 V blocking voltage range and used in various applications, that will be discussed later.

For Si, the bipolar junction transistor (BJT) and MOSFET have complementary characteristics that are desired in power electronics. BJT is a bipolar device and has high

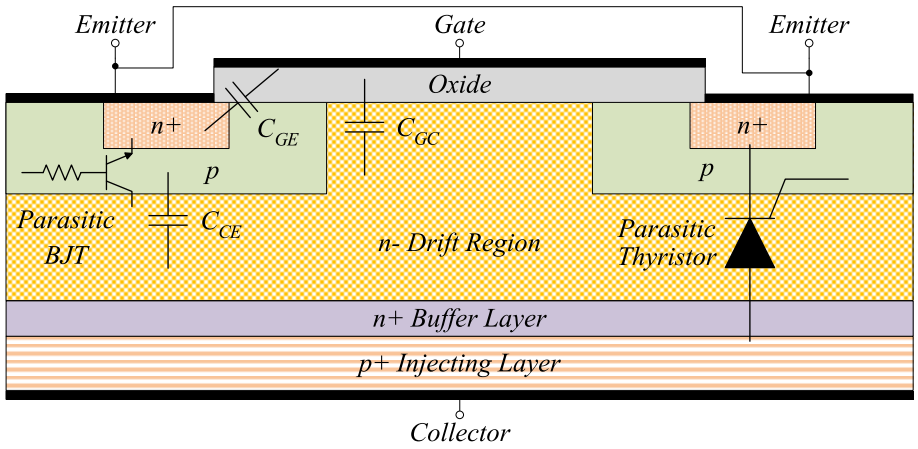


Figure 3.7: Vertical IGBT structure.

conduction performance due to presence minority carriers during device conduction with the penalty of high power driving requirement and low switching speed. On the other hand, MOSFET is a unipolar device which has very high switching speed with low power driving requirement due to absence of minority carriers with the penalty of low conduction performance. The attempts to combine the best properties of BJT and MOSFET structures lead to introduction of Insulated-Gate Bipolar Transistor (IGBT) for high voltage power electronics. The vertical cross section of a generic n-channel IGBT is presented in Fig. 3.7. The structure of a vertical IGBT is very similar to vertical MOSFET presented in Fig. 3.6 apart from the additional $p+$ injecting layer at the collector of IGBT. The $n+$ buffer layer is not essential in the operation of IGBT and is not used in some design. However, The $n+$ buffer layer provides a punch through design in the drift region with trapezoidal electric field distribution and therefore the drift layer with $n+$ can be thinner in comparison to non punch through design without $n+$ buffer layer.

The IGBT is a voltage controlled device with the same configuration as MOSFET. When the gate-emitter voltage exceeds threshold voltage, inversion layer begins to form across p body region and the drain and source are connected through n channel. The channel provides the drift current flow same in MOSFET. At the same time,the current flow through the inversion layer causes hole injection from the $p+$ layer at the collector side to the p layer. The holes move by diffusion and drift through the $n-$

drift layer. As soon as the holes reach p layer, they attract the free electrons at $n+$ layer at the emitter and combine. The minority and majority carriers are involved in current conduction through the $n-$ layer and reduces drift layer resistance. The on-state voltage drop across IGBT can be expressed by the following equation:

$$V = V_{on} + R_{on} \cdot I_{CE} \tag{3.19}$$

where V_{on} is the on-state threshold of the IGBT caused by the pn junction at the collector and R_{on} is the drift layer resistance. During the on-state operation of IGBT, the parasitic thyristor across collector and emitter can be false activated and the controllability of IGBT through the gate can be loss. This process is called "latchup". During injection of holes from $p+$ region, the holes will be attracted to the electrons flowing through the inversion layer and a lateral flow holes through p layer can occur. This lateral flow will create a positive voltage drop at the boundary of p layer and $n+$ layer at the emitter. If the voltage drop is large enough, it will attract substantial amount of electrons from $n+$ region and will turn-on the parasitic thyristor. The thyristor can only be turned-off by removal of charge with reverse current and large conduction time can destroy the IGBT.

The switching performance of the IGBT is affected by minority carriers and during turn-off, these charges have to be extracted from the device which causes tail currents at turn-off. This tail current causes additional power loss across the devices and the turn-off energy can be estimated by the following equation:

$$E_{off} = \frac{1}{2} \cdot V_{CE} \cdot I_C \cdot t_{rv} + \frac{1}{2} \cdot (V_{CE} + V_{pk}) \cdot I_C \cdot t_{fi} + \frac{1}{2} \cdot I_{tail} \cdot V_{CE} \cdot t_{tail} \tag{3.20}$$

where V_{CE} is IGBT collector-emitter voltage, I_C is collector current, t_{rv} is rise time of V_{CE}, V_{pk} is the voltage overshoot caused by stray inductance, t_{fi} is fall time of collector current, I_{tail} is maximum tail current and t_{tail} is the decay time of tail current from maximum to zero. Apart from the tail current loss part, the turn-off loss equation is same as for MOSFET in Eq. 3.16. The turn-on loss can be approximated with the same loss equation for MOSFET Eq. 3.15 [58], [60].

3.2.3 GaN HEMT

GaN is particularly attractive as a WBG material for high frequency, high voltage applications (e.g. grid connected systems where 600 V or 1200 V devices are utilised) due to large critical electric field and high electron mobility, as shown in Table 3.1. Due to lack of high quality free-standing GaN substrates and also high cost of GaN, manufacturers have grown GaN on foreign substrates such as SiC and Si. Particularly Si is the most popular material due to lowest cost technology and GaN on silicon can be processed by standard manufacturing lines. The lack of availability of GaN substrate and non-conductive epitaxial layer between GaN and substrate lead to development of lateral power devices, unlike in Si and SiC based power devices. Among different device structures, high electron mobility transistor (HEMT) is the most popular structure for lateral power devices due to its excellent switching and conduction performance [55, 69, 70]. Recently, due to advancements in material processing technology, vertical GaN devices on GaN and Si substrates have been published by device manufacturers [70]. In [71], vertical GaN P-i-N diode is presented on GaN substrate with 1700 V blocking capability. In addition to this, various MOSFET and JFET based vertical GaN devices are presented in [72, 73, 74, 75] with voltage blocking capability higher than 600 V, but they are still at development stage and the vertical GaN technology is not as advanced as lateral GaN technology at this stage.

In literature, lateral depletion and enhancement mode devices have been presented but due to same reasons as in MOSFETs, enhancement mode devices gained popularity in GaN HEMTs. The structure of a lateral enhancement mode GaN HEMT is presented in Fig. 3.8. The presented structure is proposed by Panasonic in [76] and is currently used in their power devices with 600 V blocking rating. The device is grown on a Si substrate with buffer layer containing GaN/AlN multilayer on the substrate to provide strain relief between GaN and Si. The principal feature of the structure of lateral GaN HEMT is the intrinsic AlGaN and intrinsic GaN heterojunction. The interface between i-AlGaN and i-GaN forms a high-mobility electron layer called "two-dimensional electron gas" (2DEG) [55], [76]. Therefore a natural channel is formed between drain and source terminals of the device. Because of natural formation of the

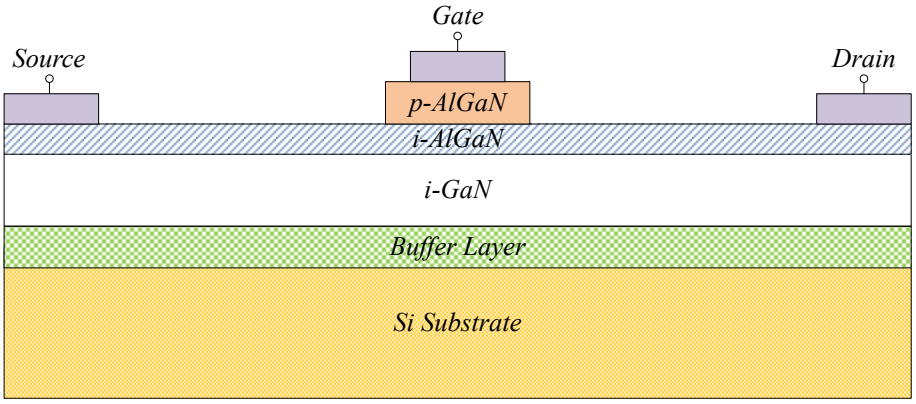


Figure 3.8: Enhancement mode GaN HEMT structure.

2DEG channel, HEMT is a naturally depletion mode device. With the introduction of p-doped AlGaN or GaN beneath the gate terminal, the channel under the gate can be fully depleted at 0 V gate-source voltage and therefore an enhancement mode device can be formed. With the proposed structure in Fig. 3.8, HEMT is operated as a field-effect-transistor when the applied gate-source voltage is between gate-source threshold voltage $V_{gs_{th}}$ and forward built-in voltage V_f of the pn junction formed by p-AlGaN and 2DEG. Above V_f, the holes are injected as minority carriers to the channel from p-AlGaN to enhance on-state performance. During on-state, the number of accumulated holes at the channel is equal to the number of electrons that flow from the source due to charge neutrality at the channel. The drain-source bias moves the accumulated electrons from the channel with high mobility while the injected holes stay beneath the gate pad as the electron mobility is minimum two times higher than hole mobility [70], [76].

Although there is no physical body diode in GaN HEMT, there is a reverse conduction mechanism for enhancement mode and depletion mode HEMT. Due to the symmetry of the device, the reverse conduction will start when gate-drain voltage exceeds the gate-drain threshold voltage $V_{gd_{th}}$. According to [70], the required voltage to activate reverse conduction is:

$$V_{gd} = V_{gs} - V_{ds} > V_{gd_{th}} \tag{3.21}$$

Generally the gate-drain threshold voltage $V_{gd_{th}}$ is equal to gate-source threshold

voltage $V_{gs_{th}}$. Therefore, the voltage drop across source and drain will be:

$$V_{sd} = V_{gd_{th}} - V_{gs} + I_d \cdot R_{sd_{rev}} \tag{3.22}$$

where $R_{sd_{rev}}$ is the effective channel resistance during reverse conduction. The GaN devices have low threshold voltage like SiC MOSFET and due to this, negative voltage during turn-off is recommended for safe operation. Eq. 3.22 shows that negative V_{gs} during turn-off will increase the on-state voltage drop across the device. Additional anti-parallel diode may provide improvement for reverse conduction but will increase the output capacitance of the device and will slow down the switching speed [70]. In synchronous rectification, as discussed in SiC MOSFET, this high conduction loss will only occur during dead time instants and therefore large on-state losses can be minimised by keeping dead time minimum and turning on the channel during reverse conduction. The conduction and switching losses of the device can be calculated using Eqs. 3.14, 3.15, 3.16 and 3.17 which have been presented for MOSFET.

3.3 Conclusion

In this chapter, fundamental properties of wide-bandgap materials are introduced and compared with Si, which has been the dominating material in power semiconductor devices. State-of-the-art WBG and Si power devices including P-i-N diode, SBD, IGBT, MOSFET and HEMT have been presented, operation principles have been explained. The benefits of WBG material properties on device characteristics have been discussed. It is clear that GaN is the promising material for WBG power device development. The maturity of material processing for SiC provided the opportunity to introduce vertical MOSFETs. On the other hand, the lack of availability of conductive substrates for GaN lead to development of lateral power devices, such as HEMTs. Both technologies have superior switching performance in comparison to Si based devices which will be discussed in the next chapter.

Chapter 4

Si, SiC and GaN Device Benchmark in PV Inverters

In this chapter, benchmark of Si, SiC and GaN devices at 600 V blocking class in terms of static, dynamic, gate drive performance and application in a three-level inverter is presented. The chapter starts with static and dynamic characterisation of the devices under different load and temperature conditions. It should be noted that Si MOSFET is not considered due to high on-state resistance at 600 V blocking class. On the other hand, super-junction MOSFETs at 600V class can also be counted as alternative device type due to good on-state performance. However, as mentioned in the previous chapter, non-linear behaviour of output capacitance of super-junction devices places large transient load on the complementary switch and extensive reverse recovery charge increases turn-on losses in hard-switching topologies [67], [68]. The static characterisation begins with on-state comparison Si P-i-N, SiC SBD and SiC P-i-N (body diode of SiC MOSFET) and followed by comparison of Si IGBT, SiC MOSFET and GaN HEMT. The static performance is followed by assessment of gate drive complexity and loss analysis for three device technologies. For dynamic performance analysis, switching performance of Si IGBT, SiC MOSFET and GaN HEMT under different current and temperature conditions are presented. The dy-

namic performance analysis is followed by literature review about application and impact of WBG devices in power electronic systems, including inverters and DC/DC converters. Finally, the benchmark of devices in three level inverter T-type, which was discussed in Chapter 2 is presented. The converter is tested under various temperature, switching frequency and output load conditions in order to assess the impact of performance wide-bandgap devices under different operating conditions. Efficiency results under different load, switching frequency and heat sink temperature are presented for three device technologies.

4.1 Static and Dynamic Characterisation of 600 V Devices

As it is mentioned in the Section 3.2.1, the P-i-N and Schottky diodes are used in half-bridge configurations in PV inverter applications and operated as anti-parallel diodes with fully controlled switches. In this section, the conduction performance of an anti-parallel Si P-i-N diode and a discrete SBD at similar current rating is evaluated. The main parameters of these two devices are presented in Table 4.1. Si P-i-N diode and SiC SBD have 600 V reverse voltage blocking capability and similar pulse current ratings. They are both packaged as discrete devices in TO-220 and SiC SBD has a planar Schottky barrier structure. Although the test conditions are different for reverse recovery charge Q_{rr} measurement, the datasheets show that SiC SBD has approximately 11 times smaller reverse recovery charge in comparison to Si P-i-N diode. This will have significant impact on the turn-on current of the complementary switch, which will be shown in Si IGBT switching performance evaluation.

In terms of controlled switches, three different active devices: Si IGBT, SiC MOSFET and GaN HEMT are compared in terms of conduction and switching performance at different case temperatures. The parameters of these devices are presented in Table 4.2. In order to simplify the comparison, collector and emitter terms used for Si IGBT can be replaced with drain and source terms used for GaN HEMT and SiC MOSFET.

	Infineon Si P-i-N IKP20N60H3	ROHM SiC SBD SCS120AG
V_{ds}	600 V	600 V
I_F	20 A @ $T_{case} = 25^oC$ 10 A @ $T_{case} = 100^oC$	20 A @ $T_{case} = 98^oC$
$I_{F_{puls}}$	80 A	76 A
V_F @ 25°C	1.65 V @ 10 A	1.5 V @ 20 A
Q_{rr}	390 nC @ $V_R = 400$ V @ $di/dt = 1000$ A/μs	35 nC @ $V_R = 400$ V @ $di/dt = 380$ A/μs
$T_{j_{max}}$	175 °C	150 °C
Device Package	TO-220-3	TO-220-2

Table 4.1: Si P-i-N diode and SiC SBD parameters

The SiC MOSFET that is used in this work is commercially available and the only SiC MOSFET device at 600 V blocking class at the time of publication. On the other hand GaN HEMT is available as samples from Panasonic and the only normally-off GaN HEMT device at 600 V blocking class at the time of publication as well. The distributor cost for single purchase in Table 4.2 shows that GaN HEMT and SiC MOSFET are 14 and 4 times more expensive than Si IGBT respectively. It should be noted that the price of WBG devices are dynamic at the time of publication due to ongoing device development, manufacturing volume and limited number of manufacturers. Therefore the cost analysis based on existing device cost may not be conclusive to evaluate the cost impact of WBG devices in renewable energy systems at this stage. It is expected that SiC devices will always be more expensive than Si and GaN based devices, but the benefits of SiC can be derived in other aspects of the system.

Comparison table shows that GaN HEMT has smallest continuous current capability at 25 °C with 15A. One reason for limited current capability of GaN HEMT is the maximum power dissipation capability of the package at 25 °C, which is half of SiC MOSFET and Si IGBT due to insulated tab. In terms of conduction performance, GaN HEMT and SiC MOSFET do not have offset voltage during conduction like Si IGBT and the on-state resistance of GaN-HEMT is approximately half of SiC

MOSFET at room temperature. On the other hand, drain current at 100 °C case temperature is 20 A for SiC MOSFET and Si IGBT, and 11 A for GaN HEMT. It is clear that Si IGBT has to be de-rated significantly in order to operate at high ambient temperatures. At 150 °C case temperature and 20 A device current, the voltage drop of across GaN HEMT, SiC MOSFET and Si IGBT is 3 V, 3.5 V and 2.2 V respectively. On-state voltage drops at different case temperatures show that Si IGBT has the best conduction performance at high case temperature values and GaN HEMT has the best conduction performance at ambient temperature. The device datasheets show that SiC and GaN devices have very stable switching loss performance over different junction temperatures unlike Si IGBT. This property makes wide-bandgap devices interesting at high switching frequencies with high case temperatures. Regarding gate requirements, it is clear that GaN HEMT has the minimum gate drive requirement among these three devices due to smallest gate charge. Gate driver requirements will be discussed in the Section 4.1.2 in detail. The output capacitances C_{oss} are similar for all three devices and the reverse transfer capacitance C_{rss} of GaN HEMT is approximately 8 times and 20 times smaller than SiC MOSFET and Si IGBT respectively.

4.1.1 Static Characterisation

The discussed diode and power switch technologies in Section 3.2 are evaluated in an experimental setup in order to understand switching and conduction performance of each device and potential benefits in PV inverter systems under different load current and ambient temperature conditions.

The test setup for the conduction performance measurement is presented in Fig. 4.1. The devices are in TO-220 package with plastic backside for GaN HEMT and metal backside for Si IGBT, SiC MOSFET and SiC SBD. The device under test (DUT) is placed on a temperature controlled heat sink where the temperature of the heat sink is controlled independently from DUT power dissipation by using power resistors for heating and fans for cooling. At each measurement, a single device is placed in

	Panasonic GaN HEMT PGA26C09DV	ROHM SiC MOSFET SCT2120AF	Infineon Si IGBT IGP20N60H3
V_{ds}	600 V	650 V	600 V
I_{ds} (25 °C)	15 A	29 A	40 A
I_{ds} (100 °C)	11 A	20 A	20 A
R_{DS-on} (25 °C)	71 mΩ @ 8 A	120 mΩ @ 10 A	N/A
V_{CE-sat} (25 °C)	N/A	N/A	1.95 V
C_{iss}	272 pF @ 10 V	1200 pF @ 500 V	1100 pF @ 25 V
C_{oss}	199 pF @ 10 V	90 pF @ 500 V	70 pF @ 25 V
C_{rss}	32 pF @ 10 V	13 pF @ 500 V	32 pF @ 25 V
Q_g	12 nC @ 3.6 V 6.5 nC @ 3.2 V	61 nC @ 18 V	120 nC @ 15 V
V_{th}	1.2 V	1.6 V	4.1 V
V_{gs}	-10 to 4.5 V	-6 to 22 V	±20 V
$T_{j_{max}}$	150 °C	175 °C	175 °C
P_{Diss} (25 °C)	83 W	165 W	170 W
r_{jc}	1.5 °C/W	0.7 °C/W	0.88 °C/W
Device Package	TO-220D	TO-220AB	TO-220-3
Distributor Cost (Single Purchase)	€29.42	€8.55	€2.19

Table 4.2: GaN HEMT, SiC MOSFET and Si IGBT parameters.

the centre of the heat sink to avoid hotspots closer to power resistors and the recommended constant gate-source bias is applied to GaN HEMT, Si IGBT and SiC MOSFET with an auxiliary DC power supply. Controlled current source is used to pass a DC current through device under various case temperature conditions in order to evaluate temperature dependency of the on-state performance. The on-state voltage drop across the device is measured with a precision multimeter. The heat sink temperature is varied between 50 °C and 80 °C as lower heat sink temperature values will increase the heat size and cost significantly, and higher heat sink temperature (> 100 °C) will push the devices to operate closer to recommended maximum junction temperature $T_{j_{max}}$, which is between 150 °C and 175 °C for power devices with conventional packaging.

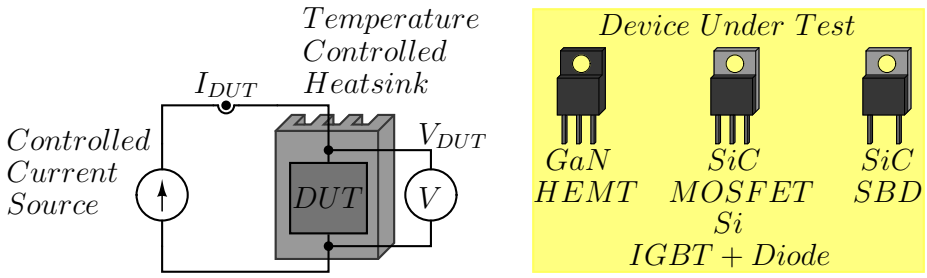


Figure 4.1: Test setup for conduction performance analysis.

4.1.1.1 Si P-i-N, SiC SBD and SiC P-i-N

The static on-state performance of Si P-i-N, SiC SBD and SiC P-i-N diode, which is the body diode of SiC MOSFET in Table 4.2, up to 30 A continuous current are presented in Fig. 4.2. Although SBD structure provides lower on-state threshold voltage V_D in comparison to P-i-N structure in Si, the V_D for Si P-i-N is around 0.61 V and for SiC SBD is around 0.802 V. The V_D decreases to 0.543 V for Si P-i-N and to 0.755 V as the temperature increases from 50 °C to 80 °C. The on-state threshold voltage of SiC P-i-N diode is around 2.63 V and drops down to 2.55 V as temperature increases from 50 °C to 80 °C. It is clear that SiC P-i-N has significantly higher on-state threshold voltage than Si P-i-N and SiC SBD counterparts due to lower n_i in SiC, which was discussed in Chapter 3 and shown in Eq. 3.1. On the other hand, the negative temperature dependency of P-i-N in Si and SiC structure is clear at higher current value with the reduction of on-state voltage while the SiC SBD shows positive temperature dependency. The SiC SBD has smaller voltage drop in comparison to Si P-i-N above 2.5 A device current and this shows that the conduction performance will not be compromised in exchange of lower Q_{rr}. The impact of Q_{rr} with Si P-i-N and SiC SBD will be shown in Si IGBT section, and impact of Q_{rr} with SiC P-i-N will be shown in SiC MOSFET section.

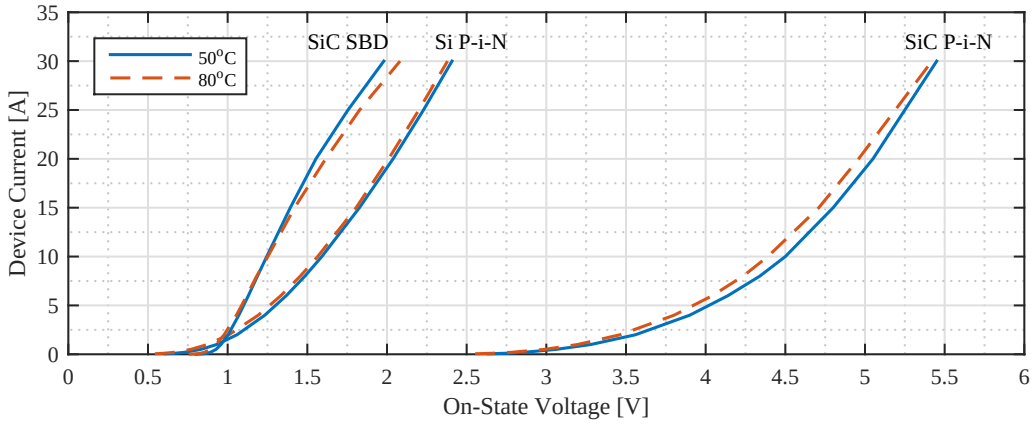


Figure 4.2: On-state characteristic of Si P-i-N diode, SiC SBD and SiC P-i-N diode.

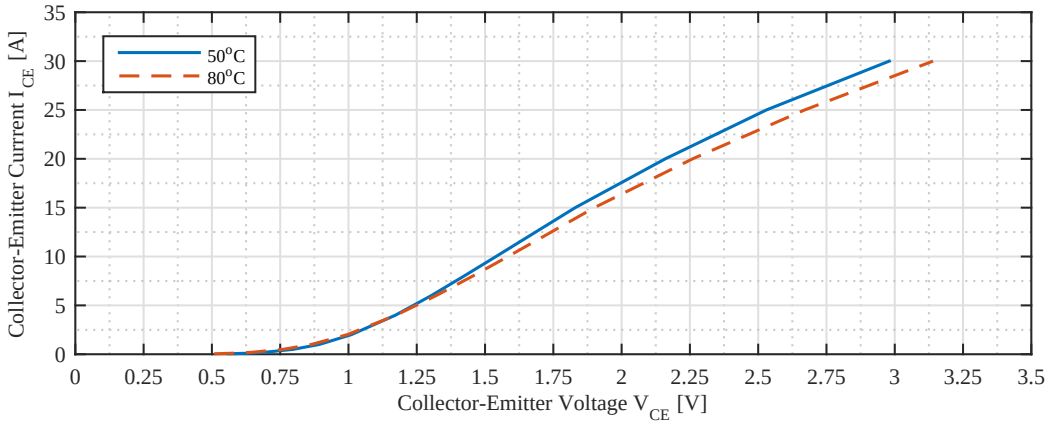


Figure 4.3: On-state characteristic of Si IGBT with 15 V gate-emitter voltage.

4.1.1.2 Si IGBT, SiC MOSFET and GaN HEMT

The static on-state performance of Si IGBT, SiC MOSFET and GaN HEMT are presented for different current and temperature conditions, based on the test setup discussed at the beginning of this section. The gate voltage for Si IGBT is fixed to 15 V as the recommended gate-emitter turn-on voltage. The on-state characteristic is presented in Fig. 4.3. It can be seen that the on-state threshold voltage is around 0.5 V and the device has positive temperature dependency.

SiC MOSFET on-state characteristic is presented in Fig. 4.4 with recommended 20

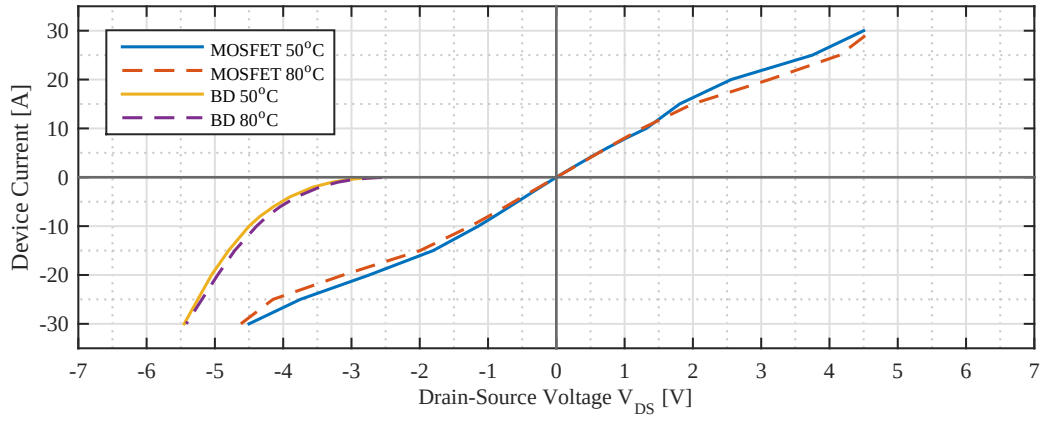


Figure 4.4: On-state and body diode characteristic of SiC MOSFET with 20 V gate-source voltage.

V gate-source turn-on voltage for channel conduction and -3.3 V for body diode conduction. It is shown that the body diode has significant amount of voltage drop in comparison to reverse conduction and the on-state threshold voltage for the body diode is around 3 V. The absence of on-state threshold voltage with MOSFET brings significant benefit at low current values and Fig. 4.4 shows that good reverse conduction capability of SiC MOSFET can provide reduction in component count by eliminating anti-parallel diodes in power converters, which is strictly required for Si IGBTs due to unidirectional current conduction capability.

The on-state and reverse conduction characteristics of GaN HEMT with different gate-source voltages are presented in Fig. 3.8. It should be noted that the V_{th} of GaN HEMT is three times smaller than Si IGBT and 1.33 times smaller than SiC MOSFET with narrower V_{gs} limits, as shown in Table 4.2. The recommended gate-source voltage during turn-on for GaN HEMT is 3.2 V. Same as SiC MOSFET, there is no on-state threshold voltage which brings reduced on-state losses at lower current ratings. The device has positive temperate dependency and the on-state voltage increases from 2.5 V to 3.2 V at 20 A continuous DC current when heat sink temperature is increased from 50 °C to 80 °C. In terms of reverse conduction, the synchronous rectification capability is presented due to symmetry of the device discussed in the previous sections. When the gate voltage is reduced to 0 V, the source-drain voltage

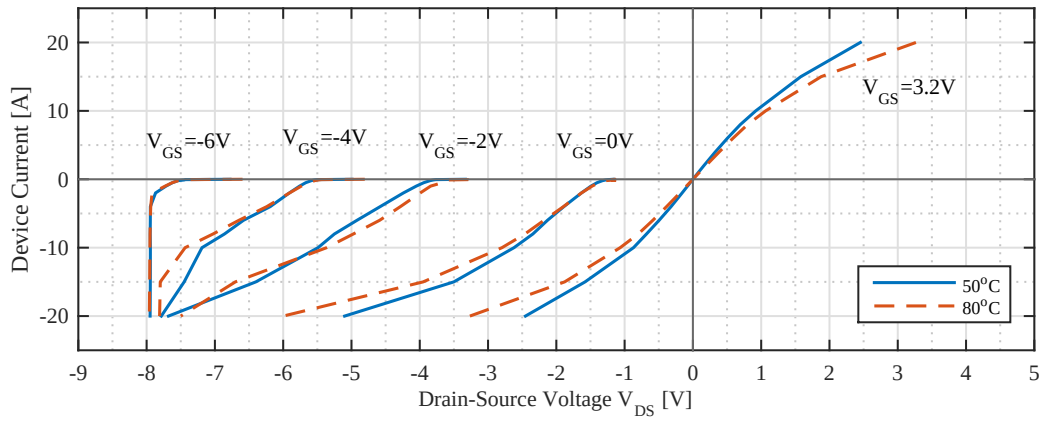


Figure 4.5: On-state and reverse conduction characteristics of GaN HEMT with different gate-source voltages.

has to overcome the threshold voltage for the start of current conduction, which is around 1.2 V in this case. It can be seen that this value is equal to the gate threshold of the device V_{th} in Table 4.2. As the gate-source voltage is brought to negative values, the on-state voltage increases to overcome the negative gate-source voltage and V_{th}. This shows that although negative gate-source is recommended for GaN HEMT due to low V_{th}, it will cause large voltage drop across the device during dead time instants. Therefore, dead time should be kept to minimum to avoid excessive conduction losses, specifically at high switching frequencies where dead time can become a significant portion of the switching period.

Finally, the on-state characteristic of Si IGBT, SiC MOSFET and GaN HEMT at 80 °C are plotted in Fig. 4.6 in order to compare the device forward conduction performance. It is clear that SiC MOSFET and GaN HEMT have better on-state performance up to 15 A due to on-state threshold voltage of Si IGBT. The smaller on-state resistance R_{on} of Si IGBT brings benefit above 15 A and at 20 A, the on-state voltage drop of SiC MOSFET and GaN HEMT is approximately 1.5 times higher than on-state voltage drop of Si IGBT.

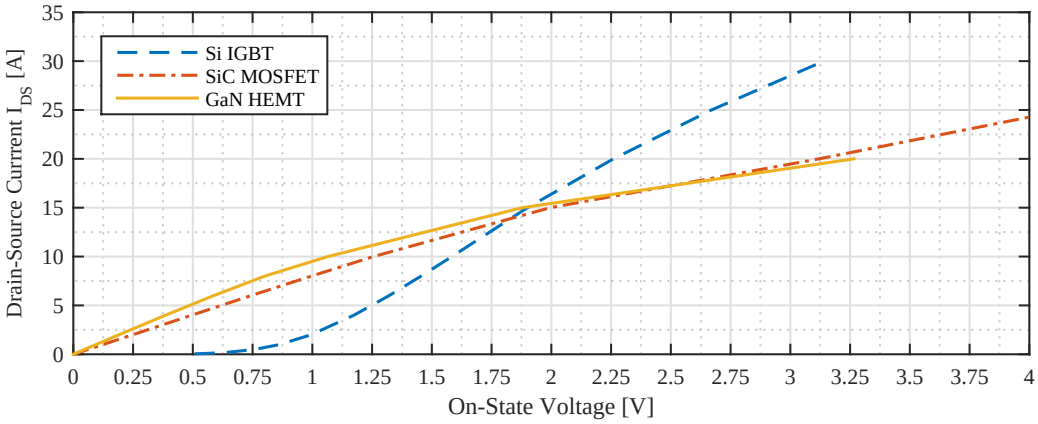


Figure 4.6: Comparison of on-state characteristic of Si IGBT, SiC MOSFET and GaN HEMT at 80 °C case temperature.

4.1.2 Gate Driver Requirements

The devices presented in the previous section require different gate-source voltages for turn-on and turn-off. In addition to this, they also have different dynamic characteristics; therefore bespoke gate-drivers have to be designed for each device technology. The schematics and gate waveforms for each device are presented in Fig. 4.7. The gate driver loss P_g for SiC MOSFET and Si IGBT can be calculated as:

$$P_g = V_g \cdot Q_g \cdot f_s \tag{4.1}$$

Where V_g is rail-to-rail gate driver voltage, Q_g is cumulative gate charge and f_s is switching frequency. SiC MOSFET and Si IGBT are easy to drive in terms of gate configuration but both devices are generally operated with positive and negative voltages for safety reasons and faster switching. SiC MOSFET requires around +19V to +21V for fast turn-on and minimum conduction loss; and -3V to -5V for better noise immunity during turn-off. On the other hand, Si IGBT is driven with symmetrical voltage such as ±15V or ±18V for similar reasons with SiC MOSFET. For these two devices, two isolated power supplies or an isolated power supply with two outputs are required. The turn-on and turn-off paths for these devices can be separated with

$R_{gate(turn-off)}$, optional external gate-source capacitance $C_{gs(ext)}$ can be included as it can be seen in Fig. 4.7c, in order to achieve optimum switching speed and avoid false turn-on due to reverse transfer capacitance [77].

GaN HEMT from Panasonic requires continuous gate current during conduction in order to enhance the conduction performance by injecting minority carriers to the channel, as discussed in Chapter 3. Therefore the gate driver losses can be calculated as follow:

$$P_g = V_g \cdot (Q_{C_s} + Q_{C_g}) \cdot f_s + R_{gate} \cdot {I_g}^2 \cdot D \tag{4.2}$$

Where Q_{C_s} is the total charge across series connected capacitor C_s in GaN gate driver, Q_{C_g} is total charge across gate capacitance C_g including reverse transfer capacitance, R_{gate} is the gate resistor that provides continuous gate current I_g and D is duty cycle in a switching period. Series connected capacitance C_s provides inrush current during switching and also negative voltage during turn-off in order to prevent false turn-on due to low threshold voltage of GaN HEMT. The accumulated charge across C_s should be larger than Q_{C_g} in order to reach required voltage level across GaN HEMT during turn-on and the capacitance value of C_s will determine the turn-off negative voltage. R_{gate} resistor is defined by continuous gate current, which is 2 mA (manufacturer recommendation) at 3.2 V gate-source voltage, and supply voltage. $R_{gate(turn-on)}$ is determined according to maximum gate driver current, supply voltage and recommended limits (300 mA in this case). The maximum gate current should not exceed 2 A according to manufacturer application note and 300 mA is the recommended peak gate current to achieve adequate switching performance.

In GaN HEMT gate driver, R_{gate} is selected as 4.5 kΩ in order to limit continuous gate current to 2 mA with 12 V rail-to-rail gate driver voltage and 3.2 V gate-source voltage. For determining $R_{gate(turn-on)}$ and C_s values, at first, $R_{gate(turn-on)}$ is selected as 47Ω in order to provide 300mA gate charging current along with R_{gate}. Then, the series capacitor C_s is selected as 3.84 nF according to following equation in order to

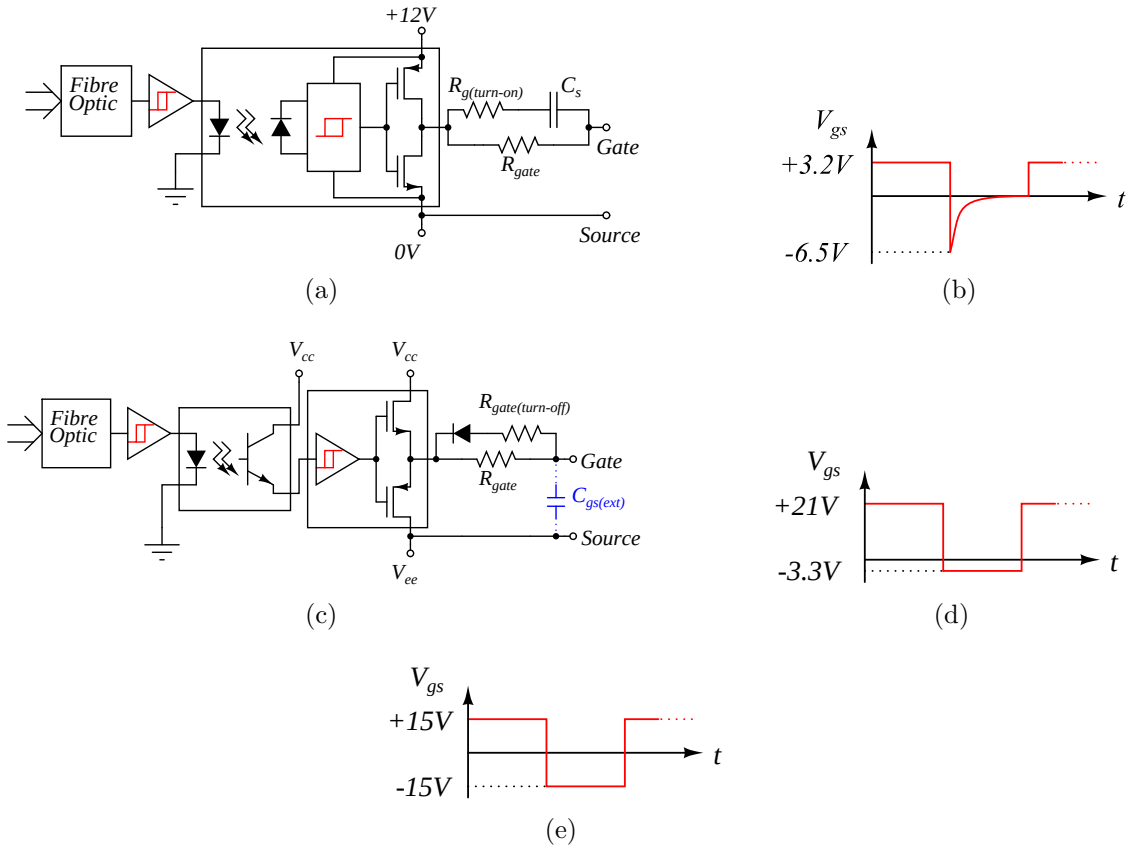


Figure 4.7: Gate driver schematics and waveforms: (a) GaN HEMT gate driver, (b) GaN HEMT gate waveform, (c) SiC MOSFET and Si IGBT gate driver, (d) SiC MOSFET gate waveform, (e) Si IGBT gate waveform.

provide approximately -6.5 V ($\triangle V_{(neg)}$) during turn-off for safe operation and speed up turn-on transient:

$$C_s = \frac{Q_g}{V_g - V_{gs} - \triangle V_{(neg)}} \tag{4.3}$$

By using datasheet values, the gate drive loss for each device at different switching frequencies can be calculated. The comparison of gate drive loss with respect to switching frequency is presented in Fig 4.8. For GaN HEMT, the duty cycle is taken as 0.64 and the gate-source (emitter) voltage, gate charge for all devices are taken as shown in Table 4.2. The comparison in Fig. 4.8 shows that GaN HEMT has

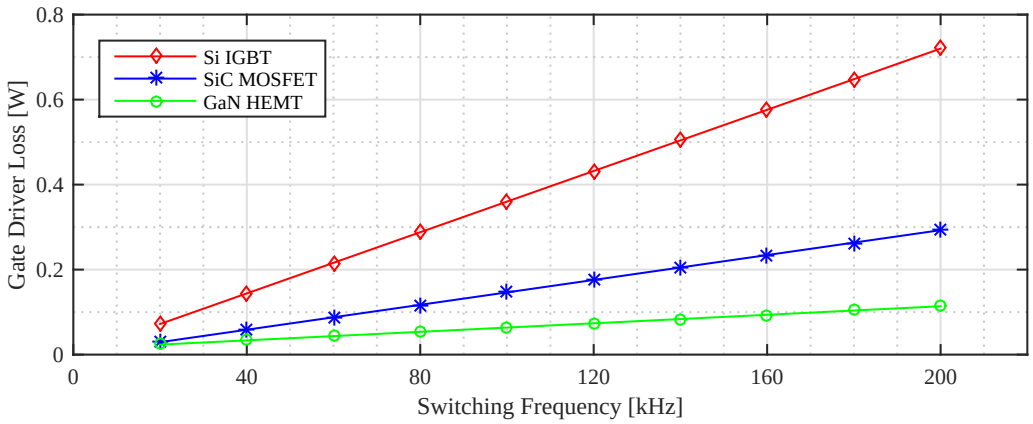


Figure 4.8: Gate loss comparison of single Si IGBT, SiC MOSFET and GaN HEMT.

minimum gate loss among three device technologies. With GaN HEMT, the static losses dominate at low switching frequencies and has clear advantage in high switching frequencies in comparison to both SiC MOSFET and Si IGBT.

The gate current requirement and noise immunity are important factors for selection of gate driver IC and therefore size of the IC package. High speed switching for SiC MOSFET and Si IGBT requires small gate resistance and therefore high peak current. Two different gate drive ICs are presented in Fig. 4.7a and 4.7c. Gate drive optocoupler (ACPL-P346) in Fig. 4.7a provides isolation with 70kV/s common-mode noise rejection (CMR) and totem pole arrangement in the same package but the continuous peak current capability is limited to 3A. The main advantage of this IC is the isolation with single package, minimum external component requirement and small footprint in the printed circuit board. On the other hand, limited current capability means it is not suitable for high speed switching devices with large gate charge. For SiC MOSFET and Si IGBT, in Fig. 4.7c, a gate drive interface optocoupler with high CMR has to be used for signal isolation and a high current non-isolated gate driver IC is used for driving the power switch. In this configuration, ACPL-4800 interface IC with 30kV/s CMR is used for signal isolation and IXDN609SI with 9A current capability is used for gate drive circuit. Although this configuration provides higher peak current with commercial ICs, the footprint of gate driver circuit increases significantly and component count on the board also increases in comparison to the option in Fig. 4.7a.

Moreover, isolated gate drive supply for both configurations is provided by isolated DC/DC converters with minimum 1kV isolation rating and low isolation capacitance (e.g. IH0512S-H for +12V supply) in order to minimize common-mode current circulation. The complexity of gate driver is an important factor, which significantly impacts both manufacturing and testing, especially in large volume applications, from a cost point of view.

4.1.3 Dynamic Characterisation

The switching test setup for evaluation of Si IGBT with Si P-i-N and SiC SBD, SiC MOSFET and GaN HEMT at different current ratings and heat sink temperature is presented in Fig. 4.10. The setup is configured as the well known double pulse test circuit, discussed in [78], which is formed by a half-bridge leg, output inductor and a DC-link formed by a DC power supply, electrolytic capacitors C_{ele} for keeping the DC link voltage fixed at 350 V and decoupling capacitors C_{film} for minimisation of commutation loop stray inductance L_{stray} and delivering pulsed power. Like in static characterisation, the same temperature controlled heat sink is used for evaluation at different heat sink temperatures. To begin the switching loss analysis, the DC link is charged to 350 V, which is the nominal voltage for devices at 600 V blocking voltage range with 700 V DC link in three-level half bridge based and 350 V DC link in full bridge topologies, discussed in Chapter 2. After charging DC link to 350 V, DUT_1 is turned-on to charge the load inductor L_{Load} to the desired current value where turn-on and turn-off switching energies will be calculated. When inductor current reaches desired value, DUT_1 is turned-off and the L_{Load} current begins to free-wheel through DUT_2. After certain time (around 10 μs), DUT_1 is turned-on again to calculate the turn-on switching loss at the same current value with the assumption of negligible current reduction in L_{Load} during free-wheeling. Main waveforms for double pulse test are presented in Fig. 4.9. As it can be seen from Fig. 4.9, the switching energy for a specific device can be obtained with this configuration at desired output current and heat sink temperature with double pulse applied to a single switch. During free-wheeling of L_{Load} current, the DUT_2 can be turned on after certain dead time

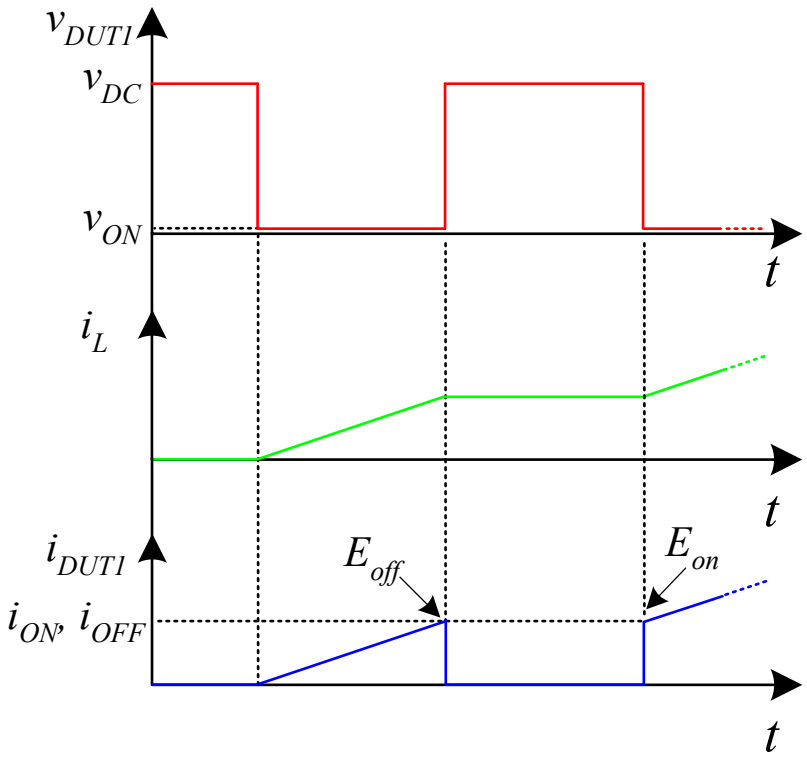


Figure 4.9: Double pulse test waveforms for switching loss calculation.

for devices with reverse conduction capability in order to reduce the voltage drop across the inductor and also losses in the free-wheeling device. For the high voltage measurement, high bandwidth (400 MHz) different probes have been used in order to capture fast switching transients. The device current is measured at the source pin of DUT_1 with a 30 MHz Rogowski current probe in order not to add extra stray inductance to the commutation loop. The temperature of the heat sink is measured with a thermocouple.

The switching performance analysis is based on the double test setup presented in Fig. 4.10. Four different experiments have been conducted for the analysis of switching performance of Si, SiC and GaN devices. During the experiments, the measurement system and test layout are kept constant in order to avoid inconsistency between results. The gate drives that have been used for Si IGBT, SiC MOSFET and GaN HEMT are discussed in detail in Section 4.1.2, which is the previous section in this chapter.

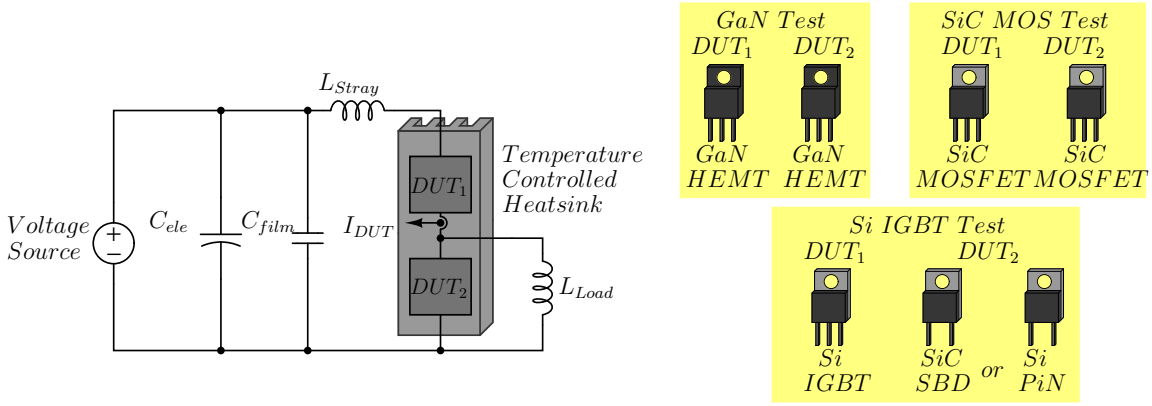
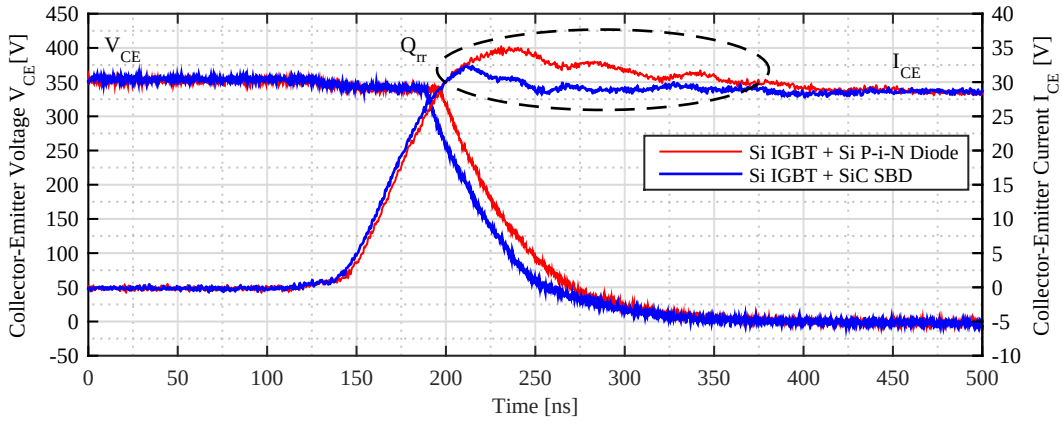


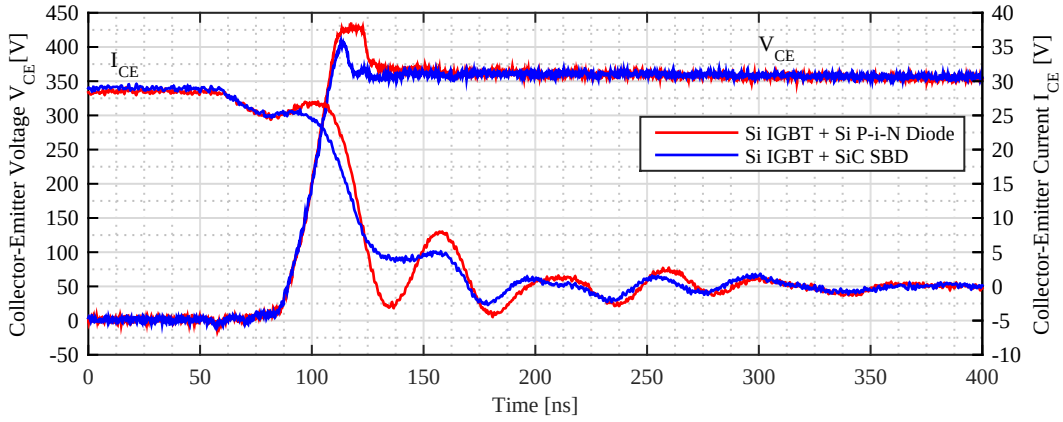
Figure 4.10: Double pulse test configuration for switching analysis of Si, SiC and GaN devices.

Dynamic characterisation begins with Si IGBT. The collector-emitter voltage V_{CE} and current I_{CE} waveforms of Si IGBT for turn-on and turn-off transitions at 350 V DC link, 30 A load current and 60 °C heat sink temperature are presented in Figs. 4.11a and 4.11b respectively. The switching results are presented with Si P-i-N diode and SiC SBD to show the impact of the anti-parallel diode on the losses of the complementary switch. The results in Fig. 4.11a shows that the smaller Q_{rr} of SiC SBD leads to smaller peak current in Si IGBT during turn-on with approximately 2.5 A peak current difference. In addition to reduction in peak current, the amount of time for Si IGBT reaching from peak current to steady state load current is significantly reduced with SiC SBD, which is also a result of reduced Q_{rr} in the anti-parallel diode. During turn-off in Fig. 4.11b, there is not a significant difference between two configurations in terms of voltage overshoot caused by rate of change of current dI_{CE}/dt and commutation loop stray inductance L_{Stray}. With SiC SBD, it is clear that the ringing at I_{CE} is smaller. It should be noted that with Si P-i-N diode at turn-off in Fig. 4.11b, the clamp of voltage overshoot to 425 V with slightly higher dI_{CE}/dt can be due to dynamic avalanche at the P-body junction of the IGBT [79]. Based on the switching waveforms, the switching energy of Si IGBT with Si P-i-N diode and SiC SBD are calculated and plotted with respect to collector-emitter current at 60 °C heat sink temperature, heat sink temperature at 30 A collector-emitter current

and heat sink temperature at 16 A collector-emitter current in Figs. 4.12a, 4.12b and 4.12c respectively. It can be seen in Fig. 4.12a that at high current values, SiC SBD reduces turn-on losses of Si IGBT by factor 1.2. In terms of temperature dependency, the turn-on losses increase by 1.12 times as the heat sink temperature is increased from 50 °C to 80 °C with Si P-i-N diode. On the other hand, with SiC SBD, the loss increase only by 1.034 times under same operating conditions. As the turn-off loss is independent from diode performance, the increase in power loss with temperature increase is 1.12 times for both conditions.



(a)



(b)

Figure 4.11: Switching waveforms for Si IGBT with Si Diode and SiC SBD: a) Turn-on transition b) Turn-off transition.

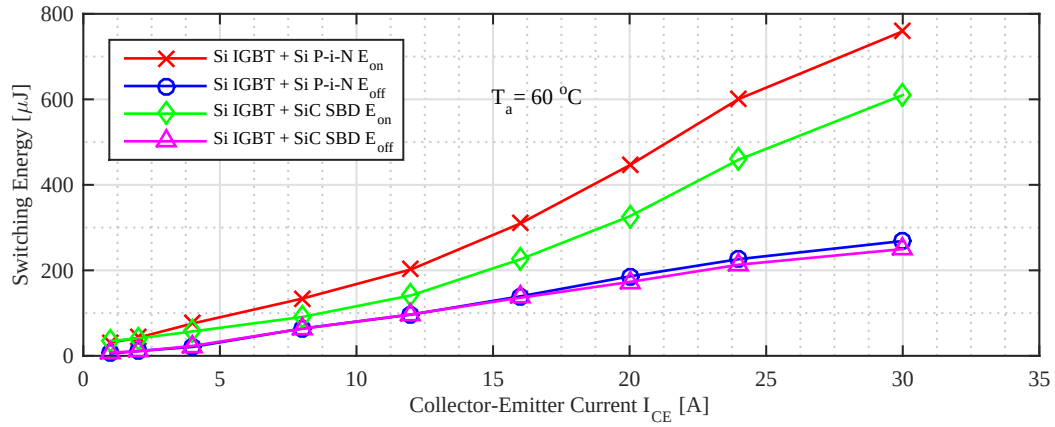
The next device to be evaluated is SiC MOSFET. The drain-source voltage V_{DS} and

current I_{DS} waveforms for turn-on and turn-off transitions at 350 V DC link, 30 A load current and 60 °C heat sink temperature are presented in Figs. 4.13a and 4.13b respectively. As it is mentioned earlier, the synchronous rectification capability of the MOSFET is utilised and no external SiC SBD diode is used. The turn on I_{DS} in Fig. 4.13a shows the impact of Q_{rr} of SiC MOSFET body diode and at turn-off instant in Fig. 4.13b, there is no sign of tail current which can be seen in Si IGBT in Fig. 4.11b. Based on the switching waveforms, the switching energy of SiC MOSFET is calculated and plotted with respect to drain-source current at 60 °C heat sink temperature and heat sink temperature at 30 A and 16 A drain-source current in Figs. 4.14a and 4.14b respectively. It is clear that the turn-on and turn-off switching energies increase linearly with load current but Fig. 4.14b shows one of the interesting aspects: temperature in-dependency of switching performance of SiC MOSFET. As the heat sink temperature is increased from 50 °C to 80 °C, the turn-on energy is reduced by a factor of 1.056 where turn-off energy stayed constant.

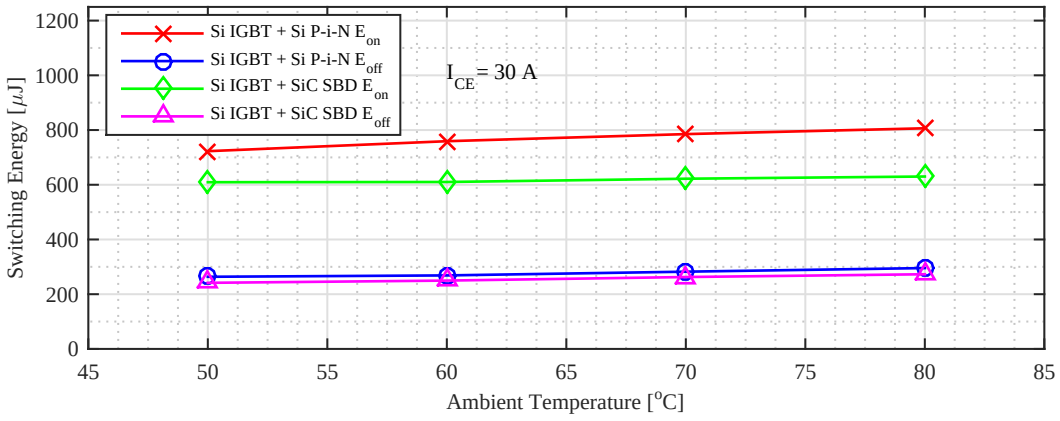
Finally, switching performance of the GaN HEMT is presented in the same structure with Si IGBT and SiC MOSFET before comparison of these three technologies. The drain-source voltage V_{DS} and current I_{DS} waveforms for turn-on and turn-off transitions at 350 V DC link, 30 A load current and 60 °C heat sink temperature are presented in Figs. 4.16a and 4.16b respectively. Same as SiC MOSFET, reverse conduction capability of GaN HEMT is utilised in the double pulse configuration and no external diode is used. As it is mentioned earlier, the negative voltage during turn-off is recommended for GaN HEMTs due to low gate-source threshold voltage and this increases the required charge to be delivered during turn-on to the input capacitance C_{iss} along with the increased conduction loss during dead time. Therefore, the turn-on loss will be influenced by the applied negative gate-source voltage. The switching waveforms in 4.16a and 4.16b are presented for two conditions: 1) Normal operation where the device is turned-off with -6 V voltage and turned-on when gate-source voltage is equal to -4 V (labelled as "GaN HEMT"), 2) Zero voltage turn-on operation where the device is turned-off with -6 V but turned on when gate-source voltage is equal to 0 V (labelled as "GaN HEMT-z"). The gate-source voltage waveform illustration is presented in Fig. 4.15 to clarify these two conditions. It can be seen

from Fig. 4.16a that the applied negative voltage slows down the turn-on transition and during turn-off due to same operating conditions, the V_{DS} and I_{DS} waveforms overlap for both cases. The impact of the negative voltage becomes more apparent with the calculation of switching energies with respect to drain-source current and heat sink temperature. The switching energy results are presented in Figs. 4.17a and 4.17b with respect to drain-source current at 60 °C heat sink temperature and heat sink temperature at 16 A drain-source current respectively. Fig. 4.17a shows that turn-on switching energy can increase up to three times with negative voltage at high I_{DS} conditions. On the other hand, regarding temperature dependency in Fig. 4.17b, the turn-on energy increases by a factor of 1.06 for both conditions and the turn-off energy decreases by a factor of 1.03 with the temperature increase from 50 °C to 80 °C.

To give an overall dynamic performance comparison, the turn-on and turn-off switching performance of Si IGBT, SiC MOSFET and GaN HEMT are plotted together in order to give an overall comparison with respect to device current and heat sink temperature. The turn-on and turn-off switching energies for three devices are presented in Figs. 4.18a and 4.18b with respect to device current at 60 °C heat sink temperature respectively. The temperature dependency of the turn-on and turn-off switching energies at 16 A device current for three devices are presented in Figs 4.19a and 4.19b respectively. It is clear that GaN has the lowest turn-on and turn-off losses independent from heat sink temperature unless high negative voltage is maintained before turn-on transition. The temperature in-dependency of SiC MOSFET and GaN HEMT provides the possibility of reduction of heat sink volume without compromising device performance.



(a)



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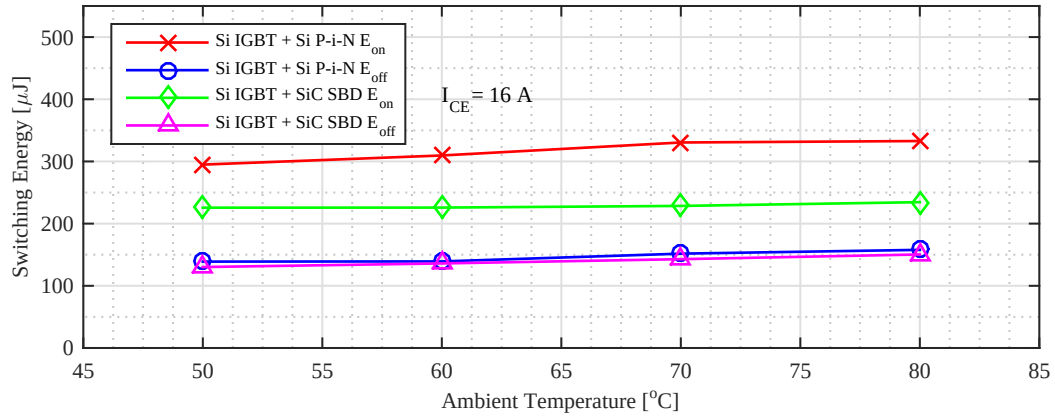
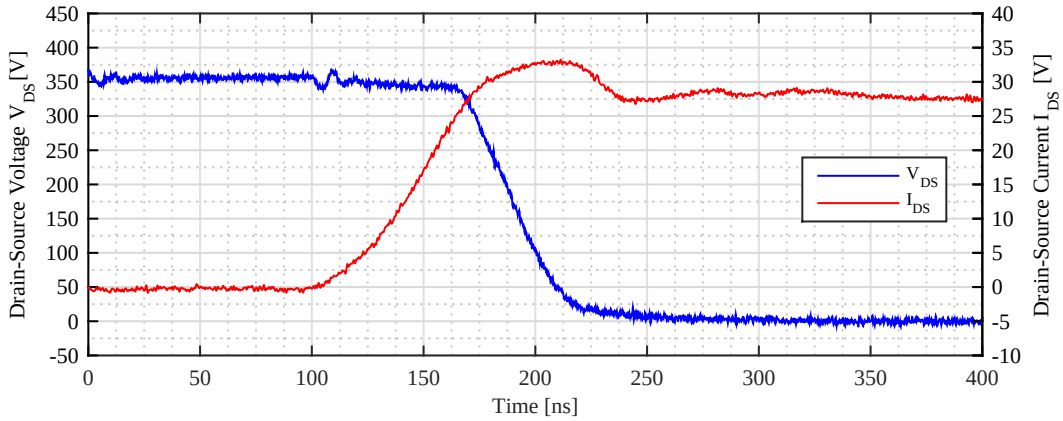
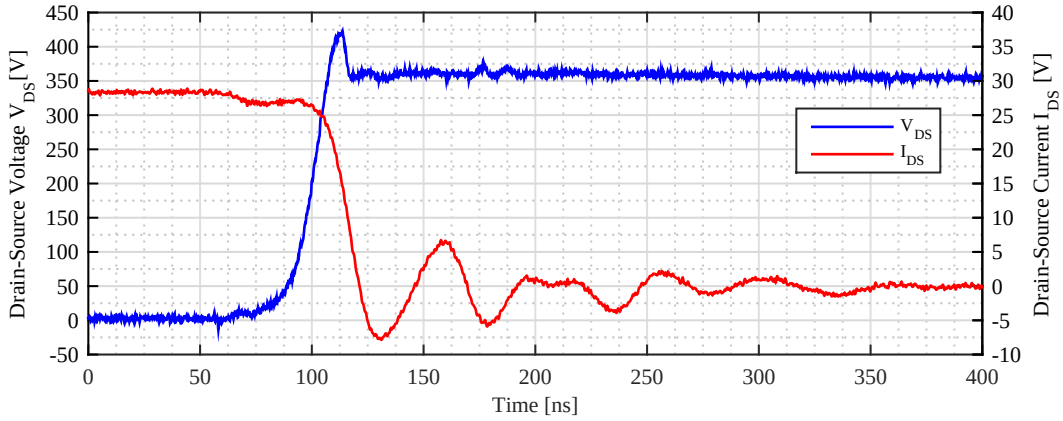


(c)

Figure 4.12: Turn-on and turn-off switching loss of Si IGBT with Si Diode and SiC SBD: a) 60 °C ambient temperature, b) 30 A collector-emitter current and c) 16 A collector-emitter current

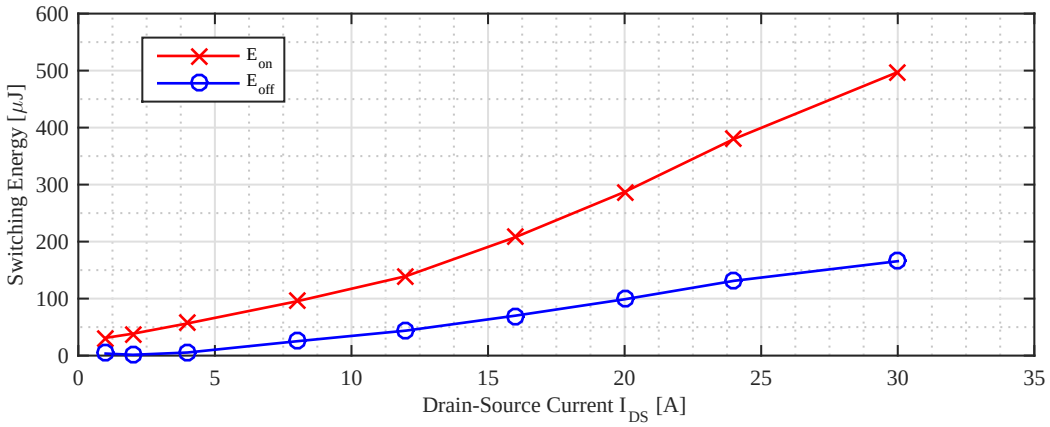


(a)

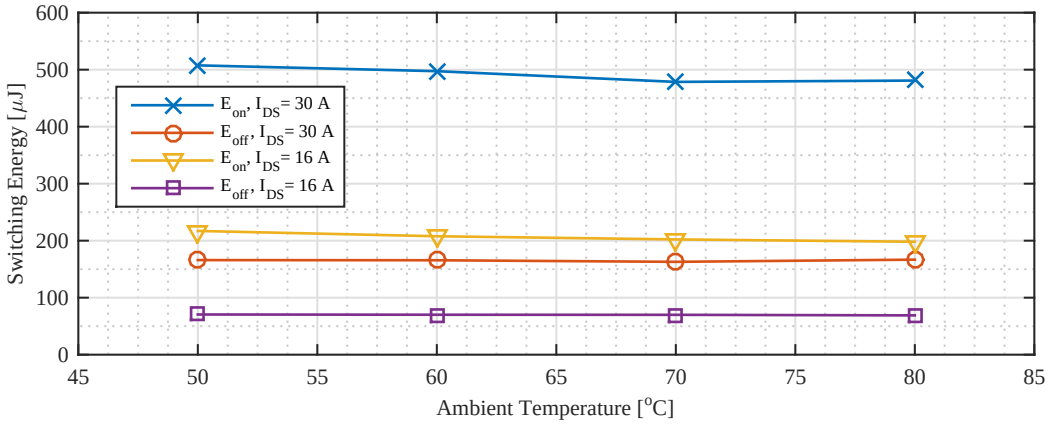


(b)

Figure 4.13: Switching waveforms for SiC MOSFET: a) Turn-on transition b) Turn-off transition.



(a)



(b)

Figure 4.14: Turn-on and turn-off switching loss of SiC MOSFET: a) 60 °C ambient temperature b) 30 A and 16 A drain-source current.

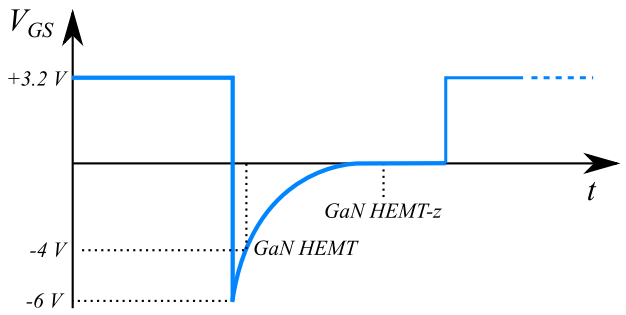
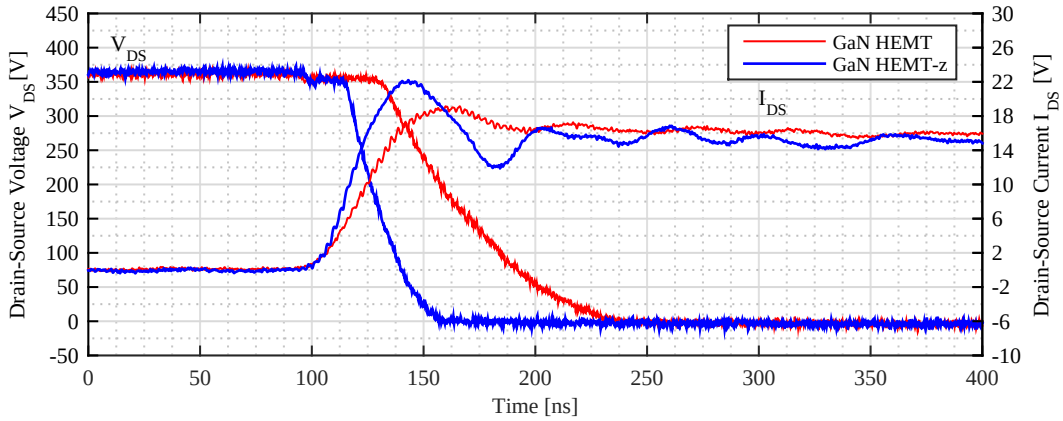
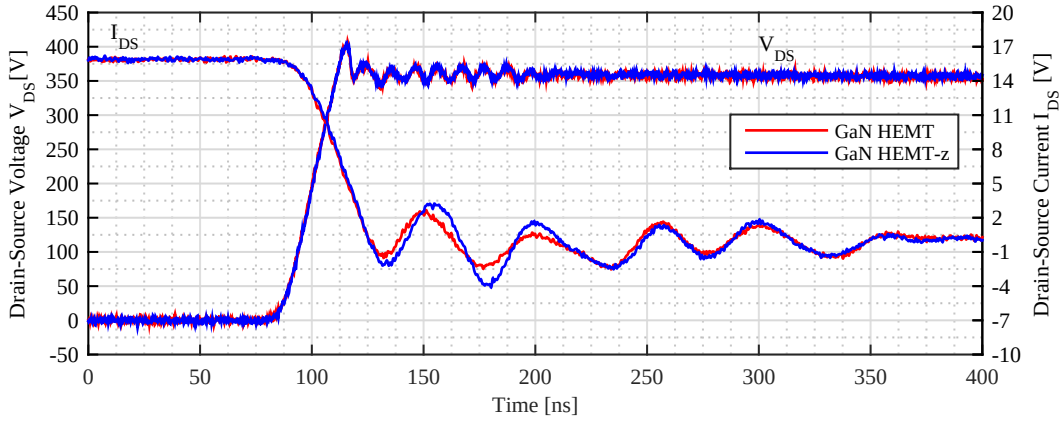


Figure 4.15: Illustration of applied gate-source drive voltage waveform for GaN HEMT.

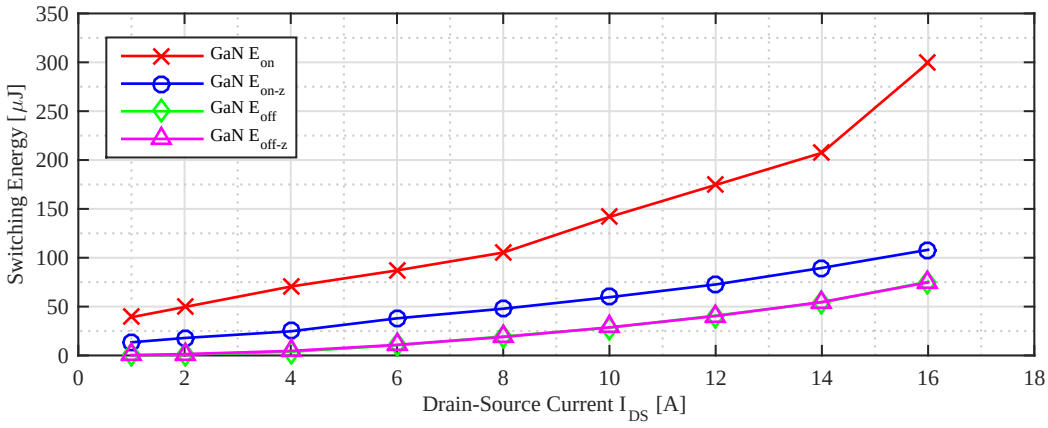


(a)

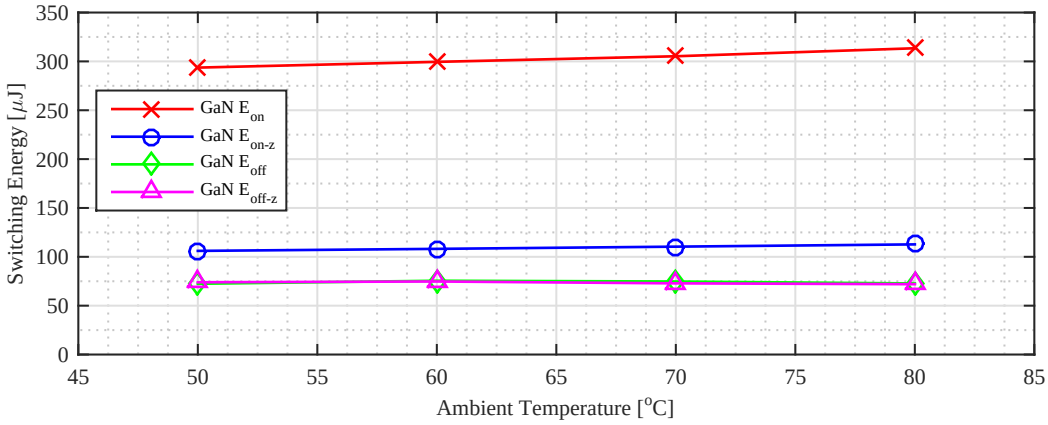


(b)

Figure 4.16: Switching waveforms for GaN HEMT: a) Turn-on transition b) Turn-off transition.

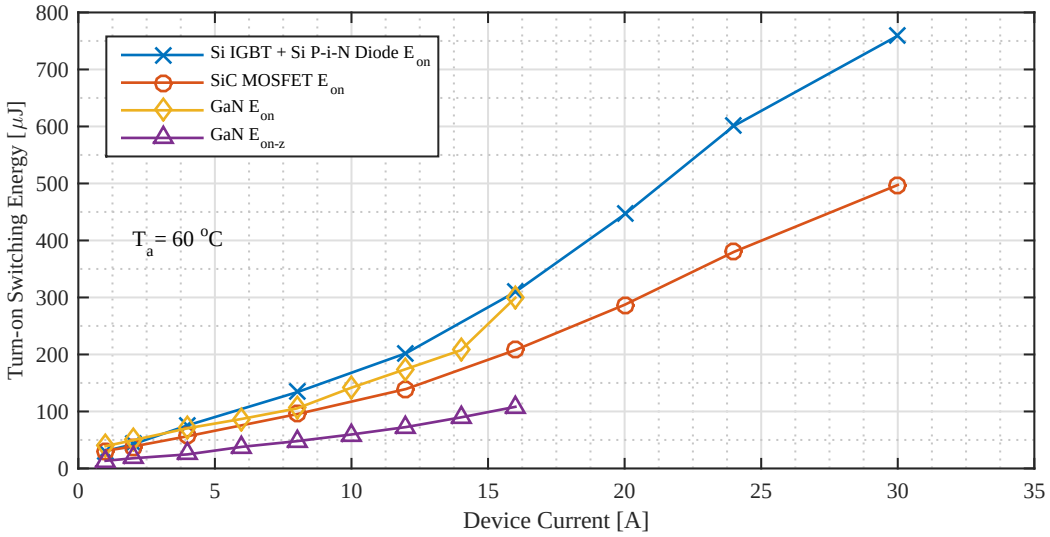


(a)

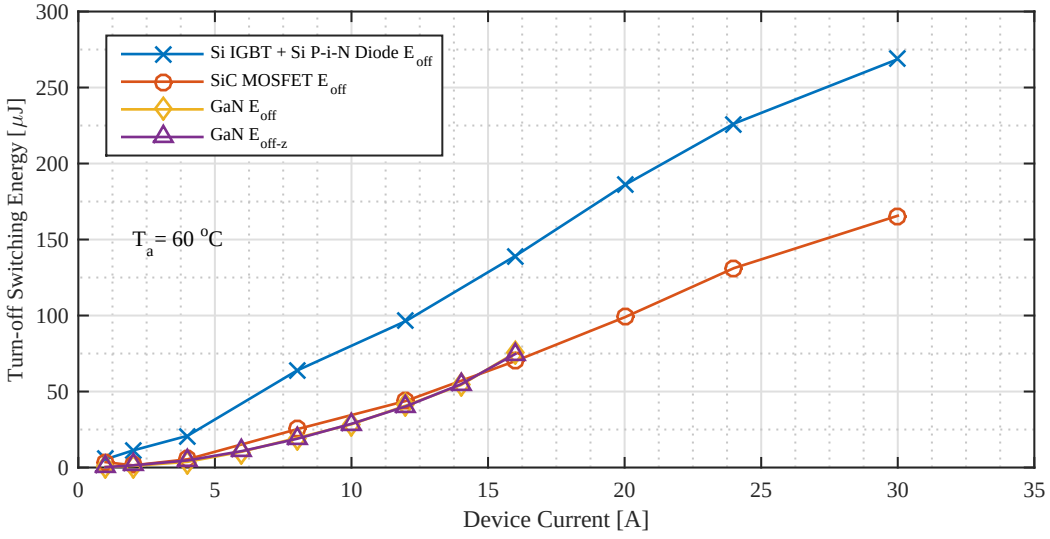


(b)

Figure 4.17: Turn-on and turn-off switching loss of GaN HEMT: a) 60 °C ambient temperature b) 16 A collector-emitter current.

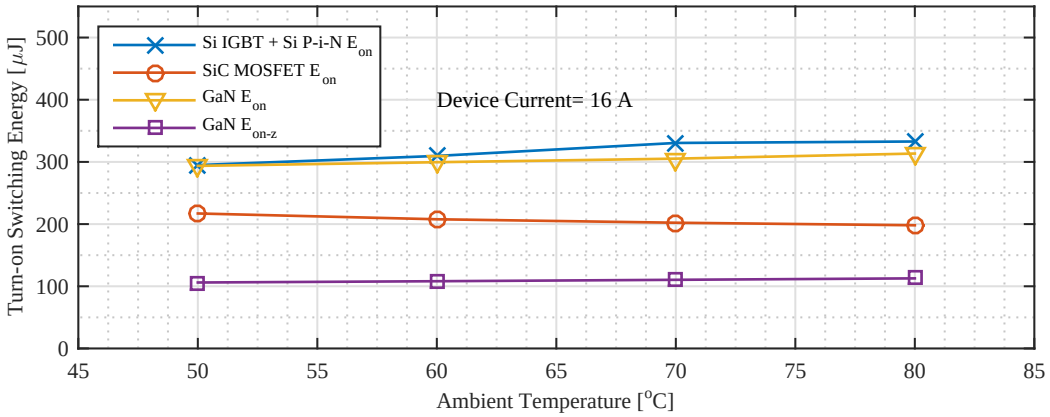


(a)

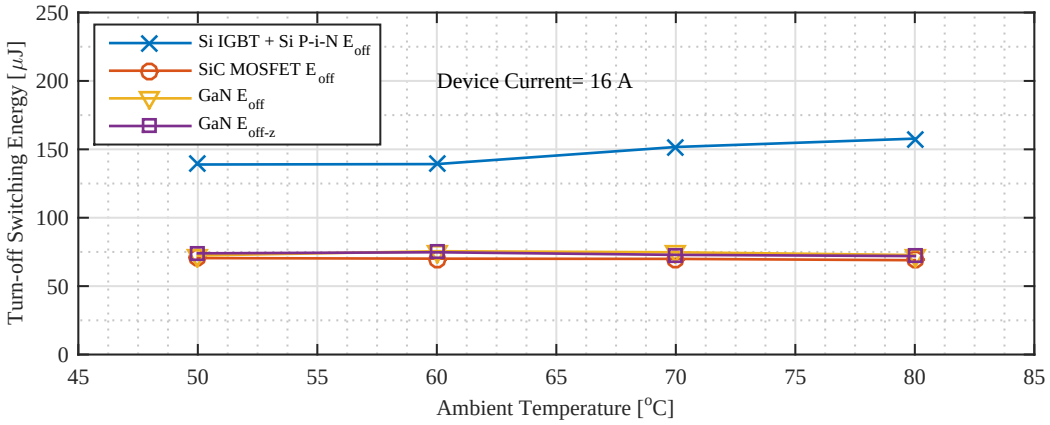


(b)

Figure 4.18: Switching loss comparison of Si IGBT, SiC MOSFET and GaN HEMT: a) Turn-on at 60 °C ambient temperature b) Turn-off at 60 °C ambient temperature.



(a)



(b)

Figure 4.19: Switching loss comparison of Si IGBT, SiC MOSFET and GaN HEMT: a) Turn-on at 16 A device current b) Turn-off at 16 A device current.

4.2 Overall Comparison

The static and dynamic performance of Si, SiC and GaN based devices under different current and temperature conditions has been presented. Finally, gate drive design and loss analysis for Si IGBT, SiC MOSFET and GaN HEMT are presented and discussed. The results of the comparison is summarised in Table 4.3. The GaN HEMT has excellent switching and conduction properties at low current conditions with negligible temperature dependency, but a complicated gate driver design is required for safe operation and the design has a strong impact on switching losses. On the other hand, SiC MOSFET has similar on-state performance in comparison to GaN HEMT below 15 A device current and shows significantly better switching performance than Si IGBT without any temperature dependency. The gate driver design is simpler in comparison to GaN HEMT but the required driving voltage is different from conventional Si devices, therefore additional effort is required in the design process. Finally, Si IGBT has the best conduction performance at high current ratings as expected but suffer from high switching losses due to intrinsic properties of Si and minority carrier charges. WBG devices can be used in reverse conduction mode with careful design in terms of dead time duration and applied negative gate voltage, and anti-parallel diodes can be therefore eliminated in inverter designs which are required in Si IGBT based designs.

	Panasonic GaN HEMT PGA26C09DS	ROHM SiC MOSFET SCT2120AF	Infineon Si IGBT IGP20N60H3
On-State Performance at low current	+++	++	- - -
On-State Performance at high current	- - -	+	+++
Switching Performance Performance	+++	++	- - -
Temperature Dependency	+++	+++	-
Gate Drive Complexity	- - -	- -	+++
Reverse Conduction	+	+++	- - -

Table 4.3: Overall Comparison of Si IGBT, SiC MOSFET and GaN HEMT.

4.3 WBG Devices in Power Electronic Converters

WBG devices gain immediate attention in power electronic community due to superior switching and conduction properties in comparison to Si as shown in the first section of this chapter. In this section, a brief literature review of applications of WBG devices and their benefit in in power converters are presented.

The literature review clearly shows that SiC and GaN devices are promising advancements in power semiconductor technology that can enable very high efficiencies and very high power density by increased switching frequencies [80]. Application of SiC devices in renewable energy converters has been widely discussed in literature and papers show the potential of achieving very high efficiency figures with SiC devices for photovoltaic applications specifically. Performance of SiC JFET devices for PV applications is discussed in detail in [81, 82, 83]. In [81], designed converter achieved 98.8 % peak efficiency and in [82], HERIC converter with SiC devices achieved 99 % peak efficiency. According to [83], overall losses in a PV inverter can be halved by just replacing Si IGBTs with SiC JFETs.

Normally-off GaN HEMTs have been introduced by Panasonic at 600V. In [84], GaN HEMTs are implemented in a DC/DC converter for maximum power point tracking for PV applications and converter operated with 98.59 % peak efficiency at 48 kHz switching frequency. Same devices have been used in different applications such as resonant LLC DC/DC converter, three phase inverter and synchronous buck converter that show the high switching and conduction performance of the devices in different operating conditions [85, 86, 87]. In [85], GaN devices are operated at 1MHz switching frequency in LLC resonant converter and achieved 96.4 % efficiency at 1 kW output power. In [86], GaN devices are used at low frequency three phase inverter and the inverter achieved 99.3% efficiency at 900 W output power and 16kHz switching frequency. Normally-on GaN HEMTs at 600V voltage class with and without cascode structure are discussed in [88] and [89] for hard-switching topologies. Performance improvement in a synchronous buck topology is presented in [88] and it is shown that smaller reverse recovery charge and output capacitance of GaN HEMT lead to

reduction in turn-on losses and up to 2 % efficiency improvement in comparison to Si MOSFET. The current collapse phenomena for 600V normally-on GaN HEMT is presented in [89] and although the device is statically rated at 600 V, the experimental results are presented up to 50-60 V due to increase in on-state voltage drop during dynamic testing.

The GaN and SiC devices at 600 V blocking class gained more attention from researches with the announcement of Little Box Challenge [90] in 2015, sponsored by Google and IEEE Power Electronics Society where the aim of the challenge is to design a 2 kVA, single phase inverter with more than 3 kW per litre power density and 95 % efficiency based on weighted CEC weighted efficiency in Eq. 2.8. The developed converter is expected to comply with EMI regulations as well. Various full-bridge topologies have been compared including soft-switching and hard switching topologies based on enhancement mode GaN HEMT and SiC MOSFET [91], [92]. The switching frequency of the converters range between 100 kHz to 200 kHz to reduce output filter size while keeping the inverter efficiency above 95 %. A multilevel inverter topology based on 200 V GaN devices and achieving MHz effective switching frequency at the output of the inverter is presented in [93]. In addition to inverter applications, active power decoupling converters to eliminate electrolytic capacitors in single phase inverters have been also discussed and realised with these WBG devices. The comparison of various topologies based on high frequency switching WBG devices is presented in [94] and [95].

4.4 Benchmark of 600 V Devices in T-Type Inverter

In order to evaluate the performance of the devices in a converter system, the T-Type topology is selected as the application. T-Type is an inverter topology based on half-bridge configuration and presented in Section 2.2.2.3. The topology is attractive as a three-level inverter solution with low conduction losses, low component count and

high efficiency. It is shown in Chapter 2 that T-Type has high efficiency in comparison to full-bridge derived topologies and currently used commercial residential scale PV systems. The topology requires 4 active switches where two of them S_1 and S_4 are used as half bridge and S_2 and S_3 are used as a bi-directional switch. In this study, the bi-directional switch formed by S_2 and S_3 in Fig. 2.19 is tested with Si, SiC and GaN devices at 600 V blocking class, presented in the previous sections. The test setup for the evaluation of the devices is explained in the next section, followed by presentation and discussion efficiency performance and switching performance under different conditions. Similar results have been obtained in H6 inverter, which is a full-bridge topology and discussed in Chapter 2, and presented in Appendix A.

4.4.1 Test Setup

The converter parameters are listed in Table 4.4 and a schematic of the test setup is shown in Fig. 4.20. Converter parameters are based on single phase grid connected inverters. PPA 5530 precision power analyser from N4L is used to measure voltage, current and power factor at the input and output of the converter and overall efficiency. The efficiency measurements exclude gate driver losses. The voltage at the output is measured before the filter inductor L_f in order to exclude winding and core losses of output filter inductors from performance analysis. The accuracy of the analyser reduces with respect to signal frequency and is around 2% at 200 kHz. Therefore the measurements as carried out inevitably characterized by some degree of inaccuracy, but as the inaccuracy is the same for all type of devices, it is expected that the error should always be in the same direction and should not affect the comparative analysis.

Two heating resistors are mounted to the heat sink with equal distance to power devices and a cooling fan is placed directly at the cooling fins of heat sink for control of case temperature of devices. The resistors generate additional heat at light load and cooling fan cools down power devices at heavy load conditions. By properly setting the required amount of heat generation including device losses and heat removal,

the heat sink temperature can be controlled independently from converter operation point. For each load and switching frequency condition, the heat sink temperature is independently set between 50 °C and 80 °C in order to evaluate the performance of the devices under different load, frequency and temperature conditions. By this arrangement, temperature of the heat sink can be made independent from load and switching frequency.

Gate driver board and power cell are shown in Fig. 4.21a and 4.21b respectively. High frequency film capacitors are placed closed to switches in parallel with electrolytic capacitors in order to provide minimum voltage overshoot across devices and output inductor L_f is formed by two off the shelf 500 μH inductors connected in series and mounted on power plane PCB. The DC link capacitance is selected to ensure the voltage variation across DC link is less than 5%. The gate driver is designed according to requirements in the previous section to provide high switching speed performance for SiC, Si and GaN devices. The board is directly soldered on the device pins in order to minimize the gate loop stray inductance and the gate signals are provided through a fibre optic link by FPGA board that can provide high frequency sinusoidal PWM modulation.

Parameter	Value
P_{MAX}	2.5 kW
V_{DC}	700 V
V_{OUT}	230 V
L_f	1 mH
C_{DC}	4 mF
f_s	16 kHz to 160 kHz
$Dead-time$	400 ns
S_1, S_4	CREE CMF2120D
	Panasonic PGA26A10DV
S_2, S_3	ROHM SCT2120AF
	Infineon IGP20N60H3
600 V SiC SBD	CREE C3D20060
T_h	50 °C to 80 °C

Table 4.4: Converter Parameters and Test Conditions

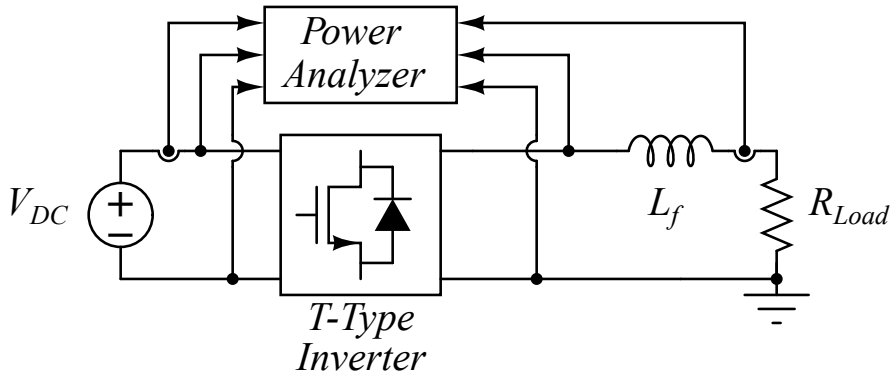


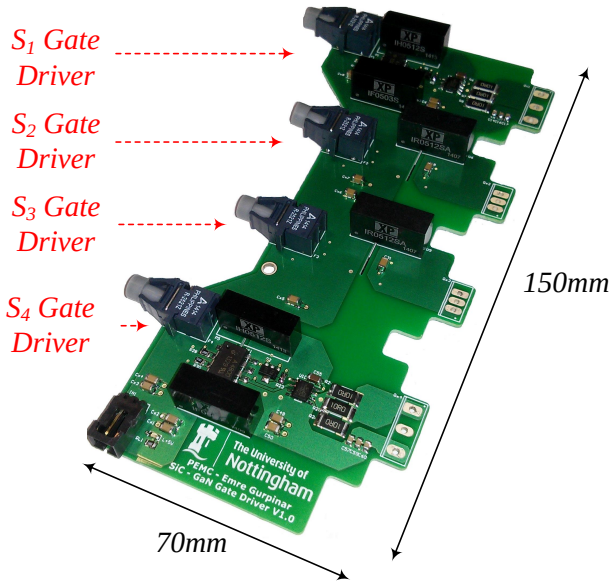
Figure 4.20: Test setup for T-Type inverter.

4.4.2 Experimental Results

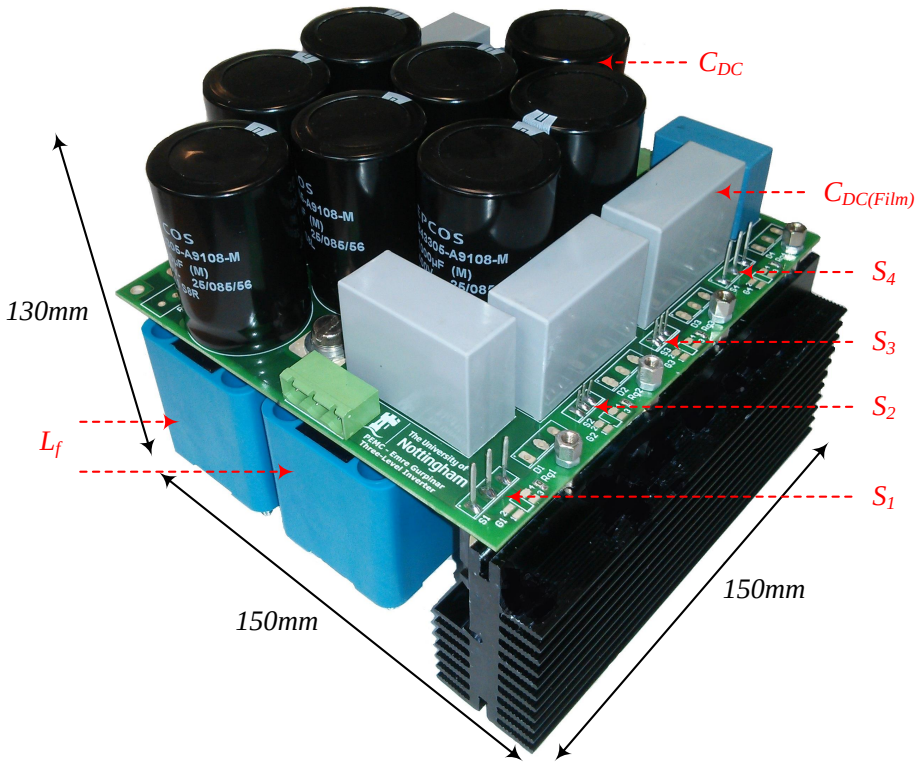
4.4.2.1 Efficiency Performance

The power cell efficiency with three different semiconductor technologies is presented in this section. The efficiency analysis at 16 kHz and 32 kHz at 50 °C heat sink temperature is presented in Fig. 4.22 for Si IGBT, SiC MOSFET and GaN HEMT. It is clear that by just replacing Si IGBT with GaN HEMT or SiC MOSFET, significant improvements in efficiency can be achieved due to superior switching properties of wide-bandgap devices. The performance difference between silicon and wide-bandgap devices becomes clearer at 32 kHz. The converter achieved peak efficiency 99.2 % with GaN HEMTs at 16 kHz switching frequency and 50 °C heat sink temperature. At 16kHz, SiC MOSFET and GaN HEMT brings up to 0.6 % and 1.45 % efficiency improvement respectively and at 32 kHz, these values increase to 0.75 % and 1.6 % due to poor switching performance of Si IGBT in comparison to wide-bandgap technologies.

The performance of the devices at different switching frequencies and heat sink temperatures are presented in Fig. 4.23a and 4.23b. Fig 4.23a shows the comparison of SiC and GaN solutions up to 64 kHz switching frequency and between 60 °C and 80 °C heatsink temperatures at 2.5 kW output power. The results show that GaN solution proves a robust performance under different temperature conditions and complete

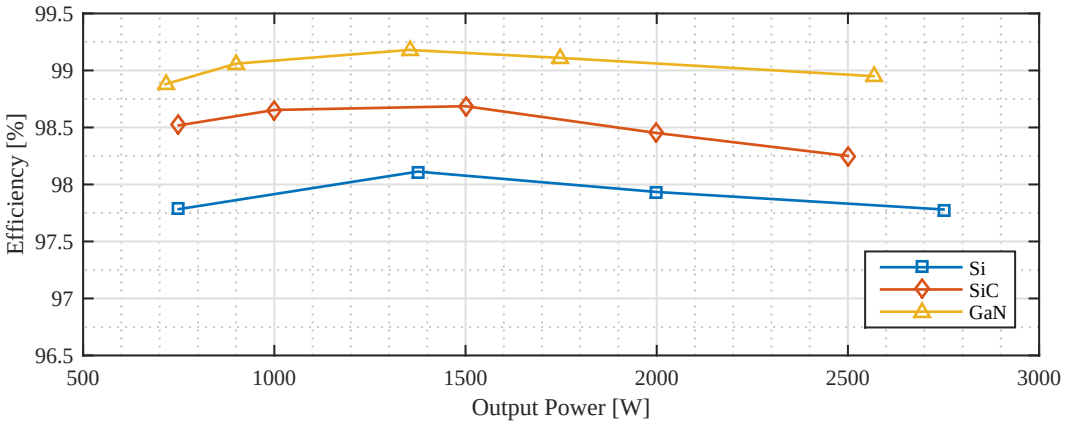


(a)

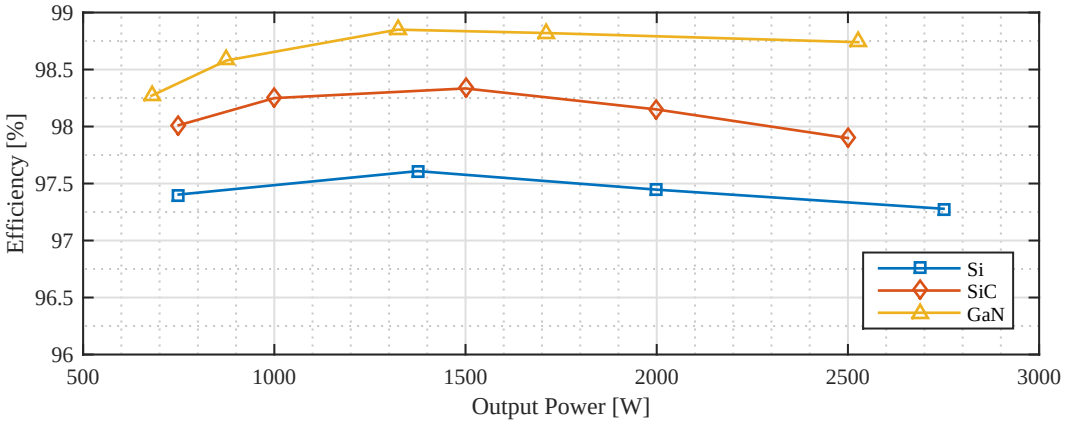


(b)

Figure 4.21: Single phase T-type inverter: (a) gate driver and (b) power cell.



(a)



(b)

Figure 4.22: Efficiency comparison at: (a) 16 kHz and (b) 32 kHz switching frequencies at 50 °C heatsink temperature.

SiC solution has less than 0.5 % efficiency variation at 64kHz switching frequency. Fig. 4.23b shows a similar efficiency comparison versus heatsink temperature at 16 kHz and 32 kHz switching frequencies at 2.5 kW output power for three different device technologies. It is clear that SiC and GaN devices show good performance under different ambient temperatures due to wide-bandgap device properties [80].

Finally, due to best performance among all three devices, inverter based on GaN is tested up to 160kHz at various load conditions in order to evaluate switching performance of the inverter. The results are presented in Fig. 4.24. The efficiency results show that SiC and GaN based T-type inverter can perform with high efficiency up to 2.5 kW output power and up to 160 kHz switching frequency. The efficiency remains above 97 % above 2.2 kW output power. In order to fully understand the trend of efficiency curves at different switching frequencies, the main contributors to power cell losses should be discussed. According to [96], there are three main loss components occurring in a power electronic system and the total loss P_{Loss_t} can be expressed as follow:

$$P_{Loss_t} = k_0 + k_1 \cdot P_{OUT} + k_2 \cdot {P_{OUT}}^2 \tag{4.4}$$

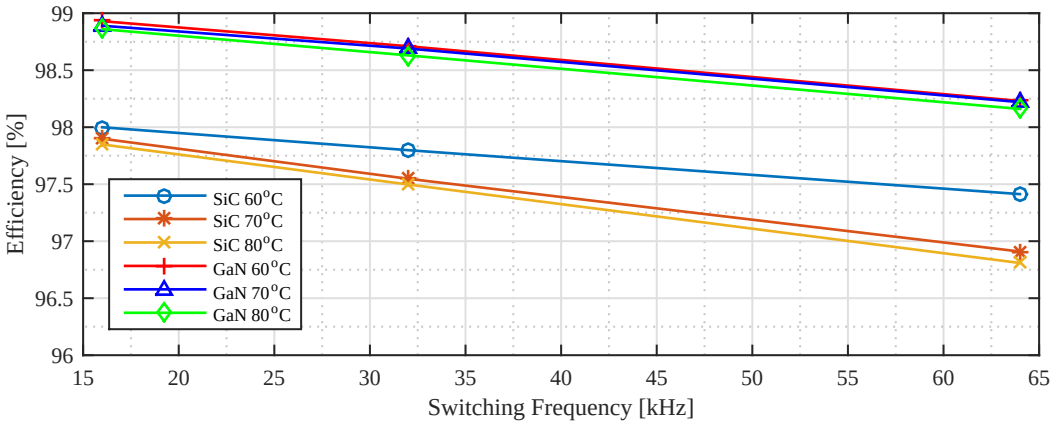
where k_o is the component that represents losses that are independent of the output power such as auxiliary systems, drive circuits for the power transistors, capacitive switching losses, etc. The $k_1 \cdot P_{OUT}$ term represents the losses that increase linearly with output power such as conduction losses due to forward voltage drop of power semiconductors (e.g. bipolar devices) and linearly current dependent switching losses. The last term $k_2 \cdot {P_{OUT}}^2$ in Eq. 4.4 corresponds to ohmic losses such as conduction losses of unipolar devices and losses in capacitors due to equivalent series resistance. Therefore, in a power electronic system with only k_0 losses, the efficiency will increase gradually with increase of output power. With only $k_1 \cdot P_{OUT}$ term, the efficiency will be constant at any load condition as the losses change linearly with output power. Finally with only $k_2 \cdot {P_{OUT}}^2$ term, the efficiency will reduce gradually with the increase of P_{OUT} due to quadratic relation between losses and output power.

It can be seen from Fig. 4.24 that at low switching frequencies such as 16 kHz and 32 kHz, the efficiency increases gradually up to 1500 W and then reduces slightly with

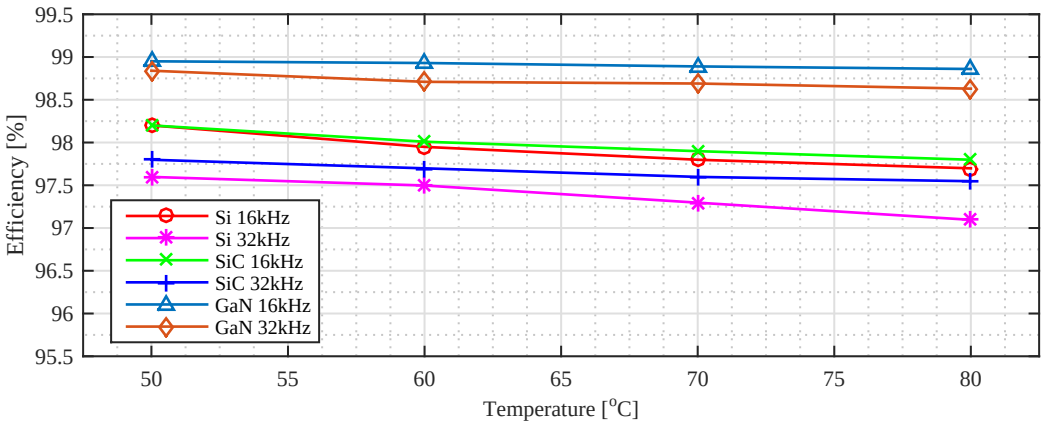
respect to increase of output power. From these two curves, it can be concluded that at low switching frequencies and light load conditions, the k_0 and $k_1 \cdot P_{OUT}$ terms in Eq. 4.4 dominate the efficiency performance. As the output power increases, the quadratic term $k_2 \cdot {P_{OUT}}^2$ begins to dominate the efficiency curves. At higher switching frequencies such as 128 kHz and 160 kHz, it can be seen that the efficiency of the power cell reduces drastically at light load conditions (below 1500 W). The reason for the reduction of this efficiency drop can be linked to increased share of mainly k_0, and $k_1 \cdot P_{OUT}$ terms in the total loss of the inverter. As the capacitive switching losses increase linearly with switching frequency and power loss P_{Loss_t} is dominated by k_0 at light load conditions. On the other hand, beyond 1500 W, the $k_1 \cdot P_{OUT}$ term, which is linked to switching losses, dominates the performance of the power cell instead of ohmic losses, unlike in low switching frequency conditions. Therefore, the efficiency of the power cell continues to increase to a steady level with increased output power.

4.4.2.2 Switching Performance

The theoretical conduction loss analysis of T-type inverter has been discussed thoroughly in [97] and equations can be found in Eqs. 4.5, 4.6, 4.7 and 4.8. The theoretical conduction loss can be calculated with respect to experimental conditions (e.g. temperature, modulation index, output power) in order to extract switching losses from experimental efficiency results. Therefore switching and conduction performance of Si, SiC and GaN can be compared at different switching frequency and heat sink temperature cases. The converter total, theoretical conduction and switching loss comparisons at 2.5 kW output power, different heat sink temperatures, and 32 kHz switching frequency for Si, SiC and GaN based configurations are presented in Fig. 4.25. Switching losses dominate the total losses for SiC and Si based configurations. On the other hand, GaN based configuration shows significant reduction in total loss due to high switching performance of GaN devices at different heat sink temperature values.



(a)



(b)

Figure 4.23: Efficiency vs switching frequency comparison at different heatsink temperatures for (a) SiC and GaN , and (b) efficiency vs temperature comparison for SiC, GaN and Si at 16 kHz and 32 kHz switching frequencies.

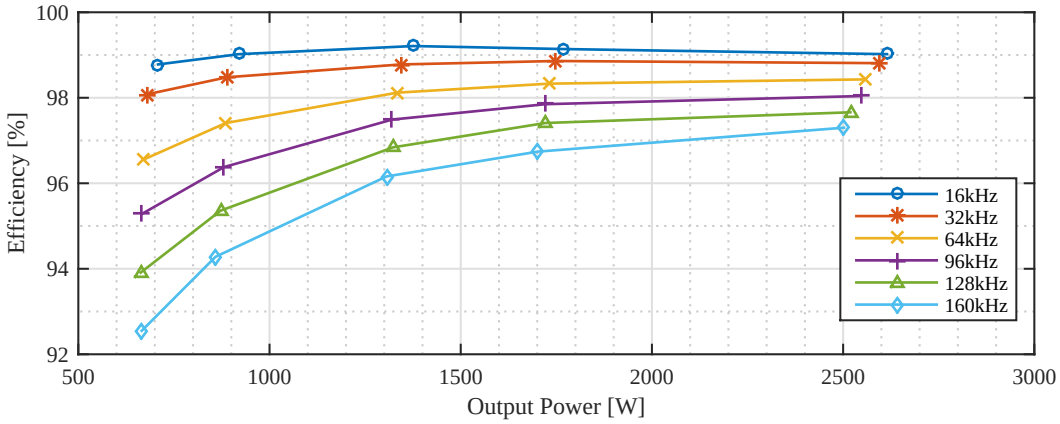


Figure 4.24: Efficiency versus output power of SiC + GaN inverter at 50 °C heatsink temperature and between 16 kHz and 160 kHz switching frequencies.

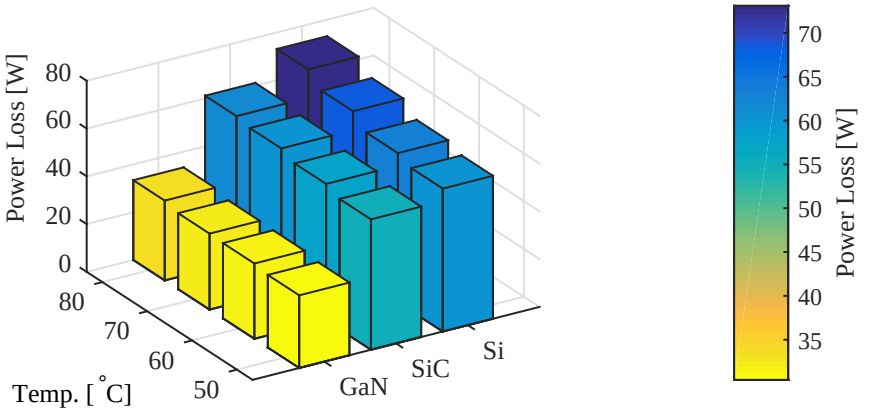
Theoretical conduction loss analysis of the T-type converter is as follow [97]:

$$P_{c-S_{1,4}} = \frac{v_{o,S}M\widehat{I}_{OUT}}{4\pi}\left[sin\left(\phi\right) + \left(\pi - \phi\right)cos\left(\phi\right)\right] + \frac{r_{o,S}M\widehat{I^2}_{OUT}}{4\pi}\left[\frac{8}{3}cos^4\left(\frac{\phi}{2}\right)\right] \tag{4.5}$$

$$P_{c-D_{1,4}} = \frac{v_{o,D}M\widehat{I}_{OUT}}{4\pi}\left[sin\left(\phi\right) + \phi cos\left(\phi\right)\right] - \frac{r_{o,D}M\widehat{I^2}_{OUT}}{2}\left[\frac{4}{3\pi}sin^4\left(\frac{\phi}{2}\right)\right] \tag{4.6}$$

$$P_{c-S_{2,3}} = \frac{v_{o,S}\widehat{I}_{OUT}}{\pi}\left[1 - \frac{M}{4}\left(2sin\left(\phi\right) - \left(2\phi - \pi\right)cos\left(\phi\right)\right)\right] + \frac{r_{o,S}\widehat{I^2}_{OUT}}{4}\left[1 - \frac{4M}{3\pi}\left(1 + cos^2\left(\phi\right)\right)\right] \tag{4.7}$$

$$P_{c-D_{2,3}} = \frac{v_{o,D}\widehat{I}_{OUT}}{\pi}\left[1 - \frac{M}{4}\left(2sin\left(\phi\right) - \left(2\phi - \pi\right)cos\left(\phi\right)\right)\right] + \frac{r_{o,D}\widehat{I^2}_{OUT}}{4}\left[1 - \frac{4M}{3\pi}\left(1 + cos^2\left(\phi\right)\right)\right] \tag{4.8}$$



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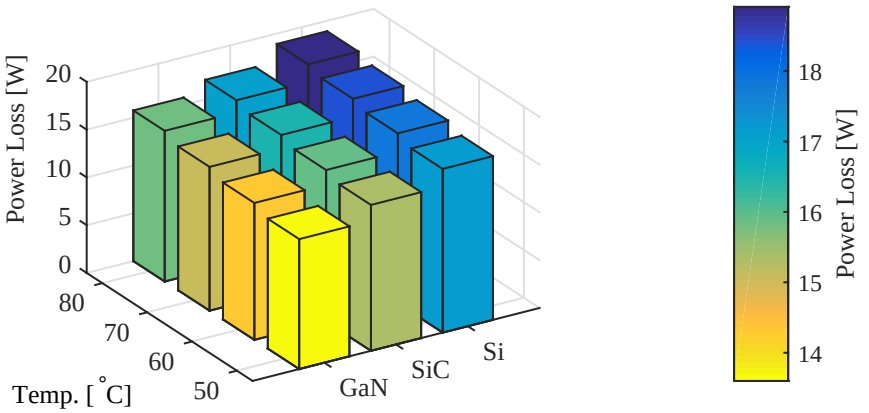

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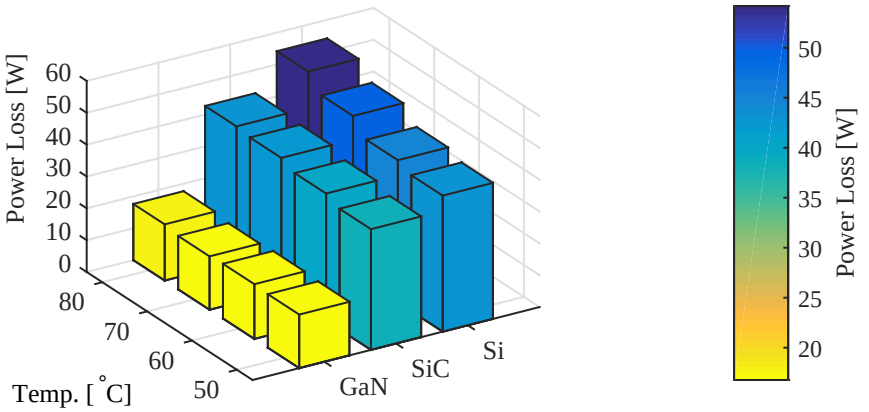


(c)

Figure 4.25: Loss breakdown for GaN, SiC and Si based converter at 1.3 kW output, 32 kHz switching frequency: (a) total power device loss, (b) conduction loss, (c) switching loss.

4.5 Conclusion

In this chapter, the benchmark of state-of-the-art Si, SiC and GaN devices is presented in terms of static, dynamic, gate drive and converter efficiency. With static, dynamic and gate driver analysis, it is shown that GaN HEMT has excellent switching and conduction properties at low current conditions with negligible temperature dependency, but relatively higher complex gate driver design is required for safe operation and the design has a strong impact on switching losses. The results with T-Type inverter show that SiC and GaN devices provide performance enhancement over Si under wide load, temperature and switching frequency conditions. In terms of switching performance, GaN HEMT has the best performance among three technologies and allows high efficiency at high-frequency applications. Performance evaluation of three device technologies show that WBG devices, specifically GaN HEMT provide robust performance under wide temperature, switching frequency conditions.

Chapter 5

GaN HEMT Based ANPC Inverter

The dynamic, static, gate drive and application benchmarking of WBG devices in Chapter 4 showed that GaN HEMT is the most promising device despite the relatively higher complex gate drive circuitry. The on-state performance of GaN HEMT is better than Si IGBT and SiC MOSFET and the switching performance is the best among three devices, independent from case temperature. The efficiency results with T-Type inverter also were aligned the dynamic and static characterisation results with achieving highest power cell efficiency when GaN HEMT is used in the system. Due to these reasons, ANPC topology, which is a member of half-bridge topologies presented in Chapter 2, is selected as the topology to explore benefits of GaN HEMT in PV inverters.

In this chapter, a fully GaN HEMT based ANPC inverter is analysed to explore the benefits of GaN HEMT devices in PV inverters in terms of efficiency, converter volume reduction (heat sink and output filter) and mission-profile based reliability. The discussion starts with the description of the inverter and test setup, followed by experimental results including efficiency and power loss under different switching frequency, heat sink temperature and output load conditions. This is followed by loss breakdown under different temperature and switching frequency conditions to evaluate performance of devices and influence of static and dynamic losses to power cell

efficiency. Furthermore, the impact of GaN devices on converter volume is assessed in terms of heat sink and output filter volume. Finally, evaluation of GaN HEMTs and Si IGBTs is presented considering real-field long-term PV mission profiles (e.g., ambient temperature and solar irradiance) to assess the thermal loading and performance of devices in a three-phase grid-connected configuration.

5.1 ANPC Inverter and Test Setup

The operation principle of ANPC inverter has been discussed in detail in Chapter 2. The selected PWM scheme for the GaN HEMT based ANPC prototype is presented in 2.18b where the synchronous rectification capability is utilised during zero state conduction. The topology provides six different switching states (two for active-states $+V_{DC}/2$ and $-V_{DC}/2$, four for zero-states) for IGBT-based applications. The schematic of the single phase topology with possible commutation loops that can be used for commutating the output current between positive state and upper and lower neutral states formed by $S_2 - S_5$ are presented in Fig. 5.1. The switching states and commutation schemes are discussed thoroughly for loss balancing and better utilisation of Si IGBTs. In literature, parallel conduction of S_2, S_3, S_4 and S_5 has not been considered as a switching state due to difficulty of the parallel conduction of IGBTs [31]. With respect to any selected switching strategy, S_1 or S_3 may be subject to switching losses for positive output voltage and positive output current. In the selected switching strategy presented in Fig. 2.18b, S_1 and S_6 switches will be subject to switching losses at positive and negative halves of the output waveform respectively with unity power factor operation. The total commutation inductance formed by the commutation loop stray inductance L_σ and the DC-link capacitor self-inductance L_{DC1} has to be minimised for reducing voltage overshoots and switching losses. The self-inductance of DC-link capacitor can be minimised by paralleling high frequency capacitors (e.g., ceramic, film) and commutation loop inductance by placing conductors that carry opposing currents in adjacent layers to induce magnetic field self-cancellation.

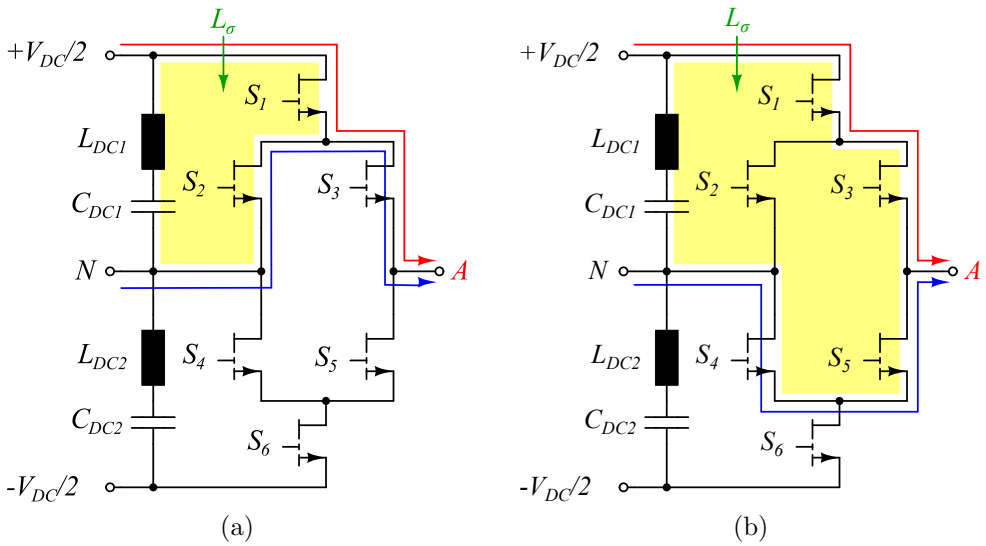


Figure 5.1: Commutation loops in ANPC from positive to neutral states: (a) positive state to upper neutral state (b) positive state to lower neutral state.

Based on these principles, the prototype PCB has been designed in order to minimise the commutation loop between commutating switches S_1-S_5, S_1-S_2, and S_6-S_3, S_6-S_4. The PCB consists of four layers with 0.2 mm FR4 insulation between layers and 1 μF, 400 V CeraLink capacitors from TDK as decoupling capacitors C_{DC1} and C_{DC2}, shown in Fig. 5.1 [98]. The constructed single phase prototype is shown in Fig. 5.2. and the PCB layer layouts are presented in Figs. B.1 - B.4 in Appendix B. The prototype is housing the fibre optic receivers for transfer of PWM signals from FPGA board, individual isolated gate drivers for each switch with the same structure presented in Fig. 4.7a, film decoupling capacitors and temperature controlled heat sink which consists of two heating resistors mounted at the sides of the heat sink and two cooling fans for independent control of device case temperature from switching frequency and output load.

The setup for the converter evaluation is illustrated in 5.3 and test parameters are presented in Table 5.1. The inverter is powered by a DC power supply with electrolytic DC link decoupling capacitors. An RL load configuration is used for evaluation of performance under different load conditions. Efficiency and losses of power cell is measured by Yokogawa WT3000E precision power analyser, which has 0.01% power

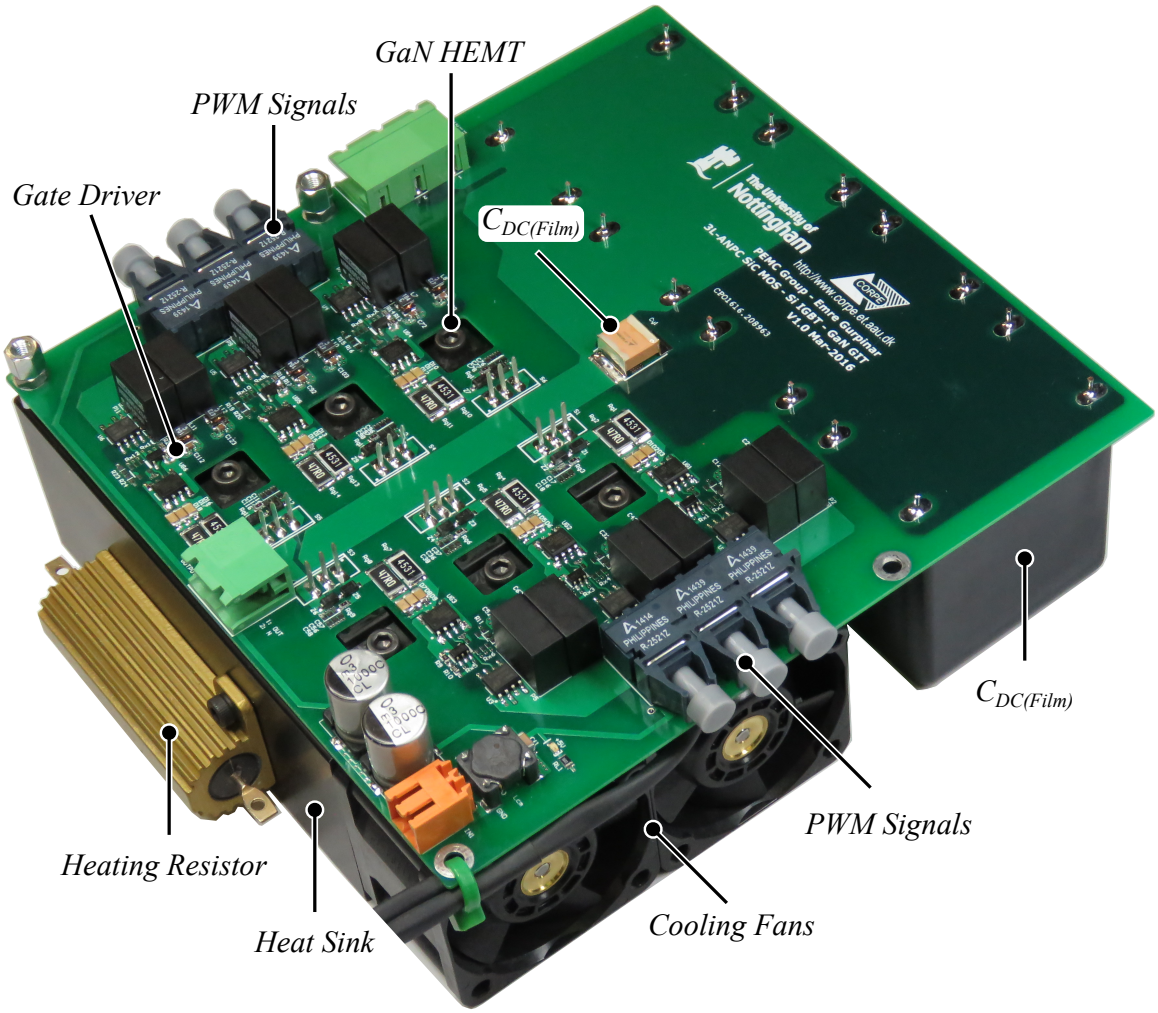


Figure 5.2: Single phase GaN HEMT based ANPC inverter.

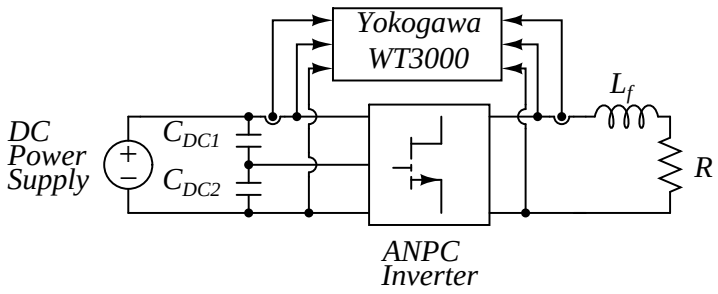


Figure 5.3: Test setup for GaN HEMT based ANPC inverter.

Parameter	Value
P_{MAX}	2 kW
V_{DC}	700 V
V_{OUT}	230 V
L_f	1.6 mH
C_{DC}	4 mF
f_s	16 kHz to 160 kHz
$Dead-time$	400 ns
$S_1 - S_6$	Panasonic PGA26C09DV
T_h	50 °C to 80 °C

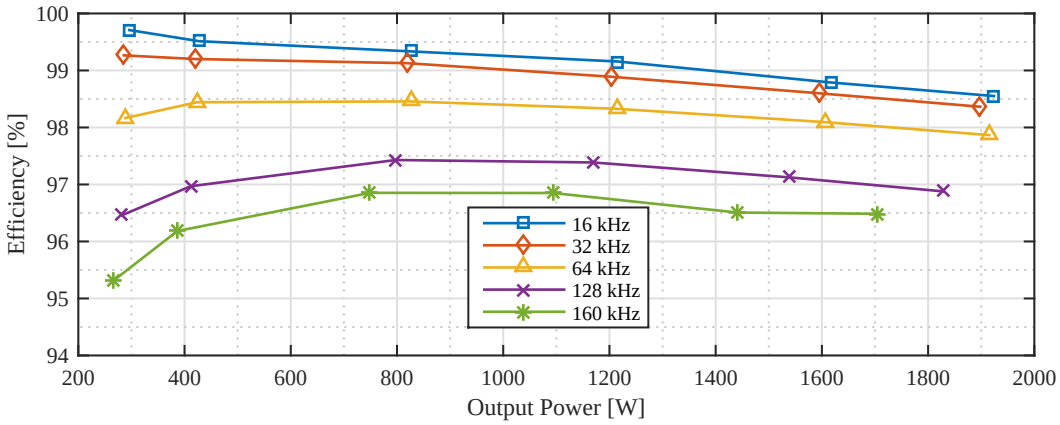
Table 5.1: Converter Parameters and Test Conditions

accuracy [99]. The PWM signals are generated by an FPGA development platform and transferred to the board via fibre optic cables. The modulation index is kept fixed and the load is changed through the resistive load bank.

5.2 Experimental Results and Loss Analysis

The inverter is tested at 120 different operating points to evaluate the performance with 4 different heat sink temperatures (50 ^{o}C, 60 ^{o}C, 70 ^{o}C and 80 ^{o}C), 5 switching frequencies (16 kHz, 32 kHz, 64 kHz, 128 kHz and 160 kHz) and 6 output load conditions (300 W to 2 kW). The efficiency and power loss of the inverter at 50 ^{o}C heat sink temperature under various load and switching frequency conditions are presented in Fig. 5.4. The superior switching performance of GaN HEMTs provide very high efficiencies (above 99 %) at low switching frequencies. The efficiency of the power cell reduces gradually due to increase in switching loss as the switching frequency is increased, and the efficiency stays above 97 % under wide load region at 128 kHz. In terms of power loss, as the switching frequency of the inverter is increased by a factor of 4 (16 kHz to 64 kHz), the power loss increases only by a factor of 1.5. If the switching frequency is increased 128 kHz (increase by factor of 8), the losses increase by a factor of 2.

The efficiency and power loss curves with respect to switching frequency at 2 kW output power are presented in Figs. 5.5a and 5.5b respectively. The efficiency decreases linearly with increase of switching frequency from 98.5 % to 96.5 % at 50 ^{o}C case temperature. The temperature dependency of the efficiency is presented in Fig. 5.6 at 2 kW output power and 5 different switching frequencies. The results in Figs. 5.5a and 5.5b show that the performance of the power cell has minimum dependency to heat sink temperature within the test conditions and high efficiency can be maintained with increased switching frequency. The increase of switching frequency and heat sink temperature allows the designer to reduce the output filter and heat sink volume, which will be discussed in the following sections.



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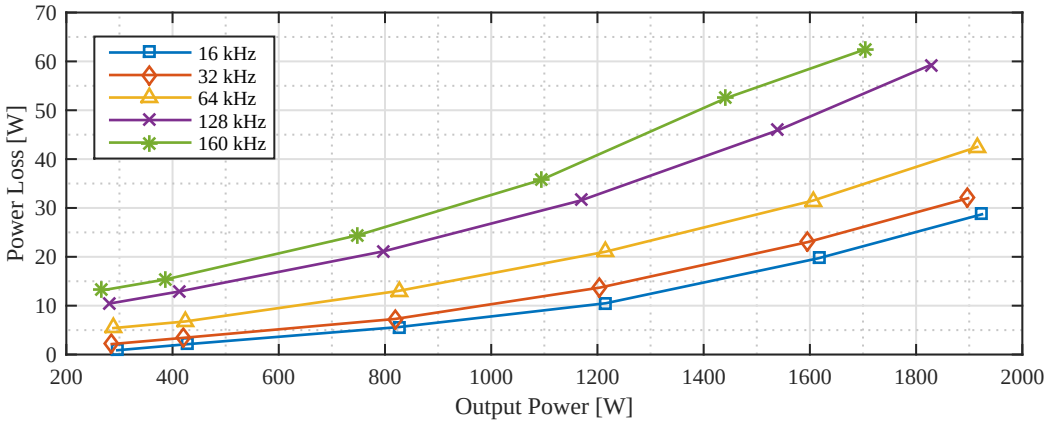
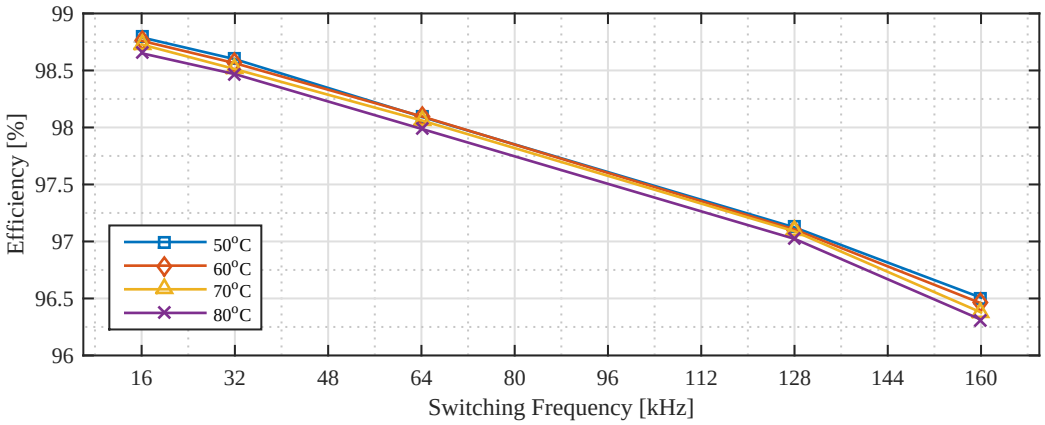


(b)

Figure 5.4: Performance of GaN HEMT based ANPC power cell versus output power at 50 ^{o}C heat sink temperature: a) efficiency, b) power loss.



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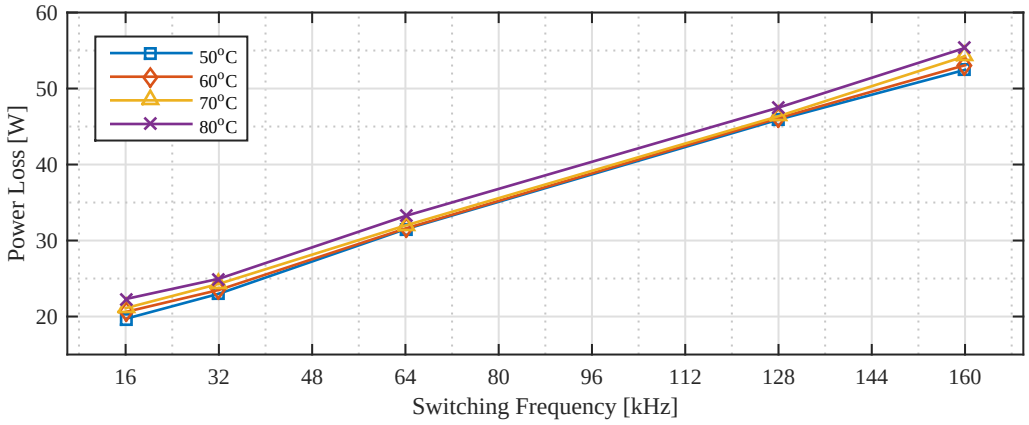
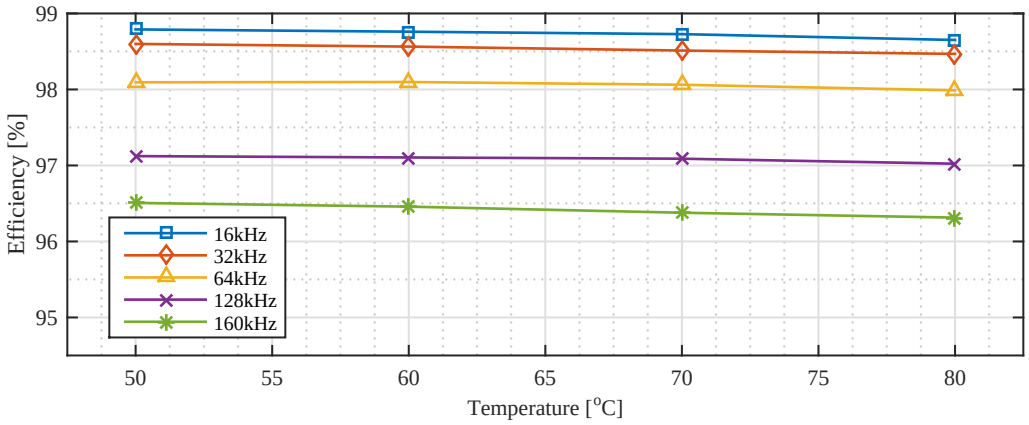
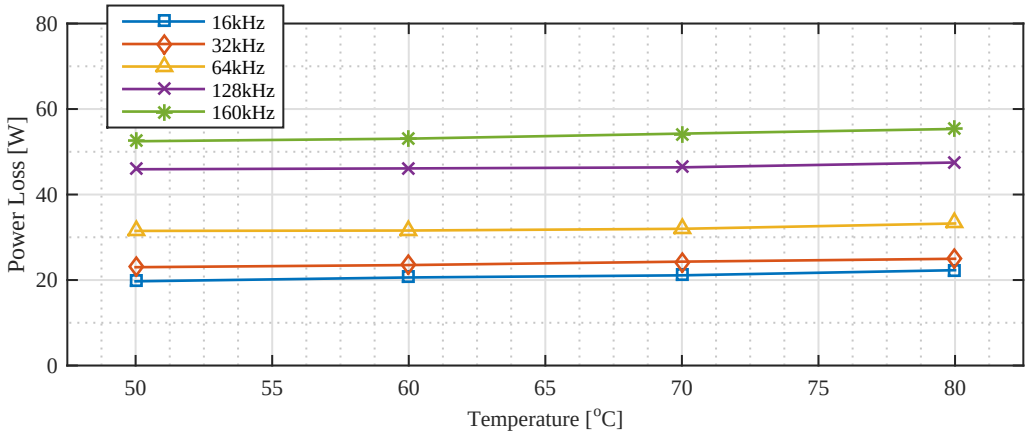


(b)

Figure 5.5: Performance of GaN HEMT based ANPC power cell versus switching frequency at 2 kW output power: a) efficiency, b) power loss.



(a)



(b)

Figure 5.6: Performance of GaN HEMT based ANPC power cell versus heat sink temperature at 2 kW output power: a) efficiency, b) power loss.

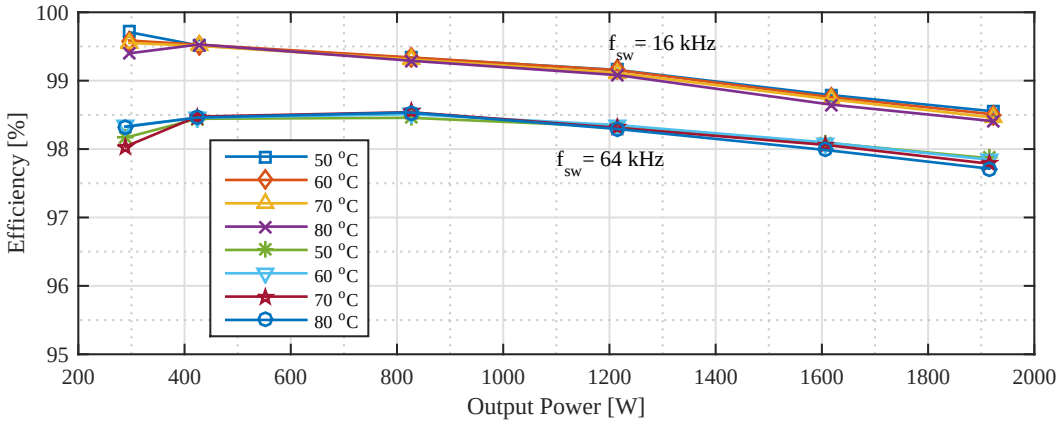


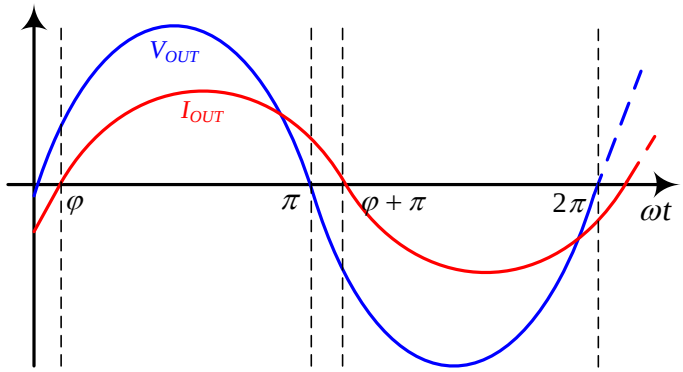
Figure 5.7: Efficiency of GaN based ANPC power cell versus output power for 16 kHz and 64 kHz switching frequencies at different heat sink temperatures.

5.2.1 Loss Breakdown

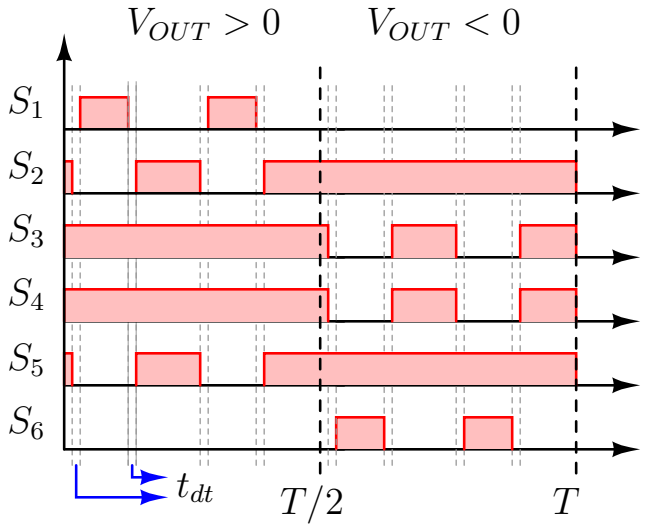
The breakdown of overall power cell loss in terms of conduction and switching losses is conducted to evaluate the dominant loss component at different switching frequency and heat sink temperature conditions. In order to separate conduction and switching losses for each operating point, conduction losses with respect to output load, dead-time and heat sink temperature are calculated based on the on-state performance of GaN HEMT, which was discussed in Chapter 4. Then, the calculated conduction loss value is subtracted from experimental power cell loss value for each operating point, which is presented in the previous section, to obtain the total switching loss.

The conduction losses are calculated based on sinusoidal approximated output voltage and current, excluding switching ripple current and harmonics. The approximated output voltage and current waveforms for this analysis are illustrated in Fig. 5.8a. The PWM switching waveforms for the selected modulation scheme (see Fig. 2.18b) including dead-time t_{dt} between complimentary devices are presented in Fig. 5.8b. An arbitrary phase shift ϕ between output voltage and current is shown to derive conduction loss equations for any power factor condition. The output current in Fig. 5.8a can be expressed as:

$$i(t) = \widehat{I}_{OUT} \cdot sin(\omega t - \phi) \tag{5.1}$$



(a)



(b)

Figure 5.8: a) Approximated output voltage and current waveforms for loss analysis and b) PWM signals for ANPC inverter with dead time.

where $\widehat{I}_{OUT}$ is the output current amplitude. The conduction time of each device can be expressed by duty cycle D. The duty cycle for active states ($+V_{DC}/2$ or $-V_{DC}/2$) D_{active} can be expressed as [38]:

$$D_{active}(t) = M \cdot sin(\omega t) \tag{5.2}$$

where M is the modulation index varying between 0 and 1. Therefore the duty cycle for zero states D_{zero} can be calculated as follow:

$$D_{zero}(t) = 1 - M \cdot sin(\omega t) \tag{5.3}$$

The on-state voltage drop across and therefore conduction loss at active state can be calculated as follow:

$$v_{on}(t) = R_{DS} \cdot i(t) \tag{5.4}$$

$$P_{cond_a} = \frac{1}{2\pi} \int_0^{\pi} i(t) \cdot v_{on}(t) \cdot D_{active}(t) \cdot \mathrm{d}(\omega t) \tag{5.5}$$

$$P_{cond_a} = \frac{\widehat{I}_{OUT}^2 \cdot R_{DS} \cdot M}{2\pi} \cdot \left(1 + \frac{cos(2\phi)}{3}\right) \tag{5.6}$$

where R_{DS} is on-state resistance at given temperature. Similarly the conduction loss at zero state can be calculated:

$$P_{cond_z} = \frac{1}{2\pi} \int_0^{\pi} i(t) \cdot v_{on}(t) \cdot D_{zero}(t) \cdot \mathrm{d}(\omega t) \tag{5.7}$$

$$P_{cond_z} = \frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{2\pi} \cdot \left(\frac{\pi}{2} + M \cdot \left(1 + \frac{cos(2\phi)}{3}\right)\right) \tag{5.8}$$

As it is shown in Fig. 5.8b, there is dead time between complementary switches S_1-$S_{2,5}$ and S_6-$S_{3,4}$ to avoid shoot through. After the conducting device is turned off, the complementary device will start conducting the output current in reverse conduction mode with higher on-state losses during dead-time. As shown in Chapter 4, GaN HEMT devices have diode like conduction characteristic in reverse conduction mode when gate-source voltage is below threshold of the device. Therefore, the on-state voltage drop across GaN HEMT, v_{dt}, during dead time can be expressed with the following equation:

$$v_{dt}(t) = V_f + \widehat{I}_{OUT} \cdot R_{DS} \cdot sin(\omega t - \phi) \tag{5.9}$$

where V_f is on-state threshold voltage and can be neglected when the device is turned-on. Based on Eq. 5.9, the dead time conduction loss for 0 to ϕ region in Fig. 5.8a is:

$$P_{dt_{1-bp}} = \frac{1}{2\pi}\int_0^{\phi} v_{dt}(t)\cdot i(t)\cdot t_{dt}\cdot 2\cdot f_{sw}\cdot \mathrm{d}(\omega t) \tag{5.10}$$

$$P_{dt_{1-bp}} = \tfrac{t_{dt}\cdot f_{sw}}{\pi}\left[V_f\cdot \widehat{I}_{OUT} - V_f\cdot \widehat{I}_{OUT}\cdot cos(-\phi) + \widehat{I}^2_{OUT}\cdot R_{DS}\left(\tfrac{\phi}{2} - \tfrac{1}{4}sin(2\phi)\right)\right] \tag{5.11}$$

$$P_{dt_{1-up}} = \frac{1}{2\pi}\int_0^{\phi} v_{dt}(t)\cdot i(t)\cdot t_{dt}\cdot 2\cdot f_{sw}\cdot \mathrm{d}(\omega t) \tag{5.12}$$

$$P_{dt_{1-up}} = \frac{t_{dt}\cdot f_{sw}}{\pi}\left[\widehat{I}^2_{OUT}\cdot R_{DS}\left(\frac{\phi}{2} - \frac{1}{4}sin(2\phi)\right)\right] \tag{5.13}$$

where $P_{dt_{1-bp}}$ corresponds to dead time conduction loss when the gate-source voltage is below threshold and $P_{dt_{1-up}}$ corresponds to dead time conduction loss when the device is turned-on. Similarly, the dead time conduction loss for ϕ to π region in Fig. 5.8a is:

$$P_{dt_{2-bp}} = \frac{1}{2\pi}\int_{\phi}^{\pi} v_{dt}(t)\cdot i(t)\cdot t_{dt}\cdot 2\cdot f_{sw}\cdot \mathrm{d}(\omega t) \tag{5.14}$$

$$P_{dt_{2-bp}} = \tfrac{t_{dt}\cdot f_{sw}}{\pi}\left[\tfrac{-V_f\cdot \widehat{I}_{OUT}}{2}\left(cos(\pi-\phi)-1\right) + \tfrac{\widehat{I}^2_{OUT}\cdot R_{DS}}{4}\left(\tfrac{\pi-\phi}{2} + \tfrac{1}{4}sin(2\phi)\right)\right] \tag{5.15}$$

$$P_{dt_{2-up}} = \frac{1}{2\pi}\int_{\phi}^{\pi} 2\cdot v_{dt}(t)\cdot i(t)\cdot t_{dt}\cdot 2\cdot f_{sw}\cdot \mathrm{d}(\omega t) \tag{5.16}$$

$$P_{dt_{2-up}} = \frac{t_{dt}\cdot f_{sw}}{\pi}\left[\frac{\widehat{I}^2_{OUT}\cdot R_{DS}}{4}\left(\frac{\pi-\phi}{2} + \frac{1}{4}sin(2\phi)\right)\right] \tag{5.17}$$

Dead time t_{dt} also means reduction of conduction time as the applied total gate pulse time is reduced by dead time duration. The reduction of power loss in a switch can be calculated as follow:

$$P_{dt_{red}} = \frac{1}{2\pi}\int_0^{\pi} R_{DS}\cdot \widehat{I}^2_{OUT}\cdot sin^2(\omega t-\phi)\cdot t_{dt}\cdot f_{sw}\cdot \mathrm{d}(\omega t) \tag{5.18}$$

$$P_{dt_{red}} = \frac{t_{dt}\cdot f_{sw}\cdot R_{DS}\cdot \widehat{I}^2_{OUT}}{4} \tag{5.19}$$

The absence of V_f can be seen in Eqs. 5.18 and 5.19 as the reduction occurs when the device is turned-on. The conduction cases for switches S_1, S_2 and S_3 for unity and zero power factor cases are presented in Fig. 5.9 based on Fig. 5.8b. The *Control Signal* represents the PWM signal before applying dead time to the gate signal, $P_{dt_{red}}$ is the

reduction in conduction loss expressed in Eq. 5.19, $P_{cond_{S_x}}$ is the total conduction loss across specified switch, $P_{cond_{ON}}$ is the conduction loss when the specified device is turned-on and $P_{dt_{x-bp}}$ is the dead-time loss when gate voltage is below threshold as presented in Eqs. 5.11 and 5.15. It can be seen from Figs. 5.9a and 5.9b that S_1 only conducts during the positive voltage output in ANPC inverter. The actual control signal is reduced by introduction of dead-time and the total loss $P_{cond_{S1}}$ is equal to $P_{cond_{ON}}$ at unity power factor as the output voltage V_{OUT} is clamped to zero state during dead-time and no current flows through S_1. At 0 power factor, during dead time, the output current I_{OUT} flows through S_1 and V_{OUT} is clamped to $V_{DC}/2$. Therefore the $P_{cond_{S1}}$ is equal to sum of $P_{cond_{ON}}$ and $P_{dt_{1-bp}}$. For arbitrary power factor, the total conduction loss across S_1 $P_{cond_{S1}}$ can be expressed by using Eq. 5.6, 5.11 and 5.19, as:

$$P_{cond_{S_1}} = P_{cond_a} + P_{dt_{1-bp}} - P_{dt_{red}} \tag{5.20}$$

With similar approach, the conduction loss of S_2 for arbitrary power factor can be calculated. As the S_2 conducts at both positive half and negative half of output voltage, the total conduction loss of S_2 can be calculated as the sum of positive half conduction loss P_{S_2+} and negative half conduction loss P_{S_2-}:

$$P_{cond_{S_2}} = P_{S_2+} + P_{S_2-} \tag{5.21}$$

where P_{S_2+} and P_{S_2-} are defined as follow:

$$P_{S_2+} = \frac{P_{cond_z}}{4} + P_{dt_{2-bp}} - \frac{P_{dt_{red}}}{4} \tag{5.22}$$

$$P_{S_2-} = \frac{P_{cond_z}}{4} + P_{dt_{2-up}} - \frac{P_{dt_{red}}}{4} \tag{5.23}$$

The only difference between P_{S_2+} and P_{S_2-} is the dead-time conduction losses $P_{dt_{2-bp}}$ and $P_{dt_{2-bp}}$. As it can be seen from Figs. 5.9c and 5.9d, $P_{dt_{2-bp}}$ corresponds to reverse conduction dead time losses at the positive half of the output when the device is turned-off, and $P_{dt_{2-up}}$ corresponds to increased conduction time in $P_{cond_{ON}}$ at the negative half of the output voltage. It should be noted that P_{cond_z} and $P_{dt_{red}}$ are divided by 4 as the output current is divided into two parallel conduction paths: S_2-S_3 and S_4-S_5. Similarly, according to Figs. 5.9e and 5.9f, the conduction loss of S_3

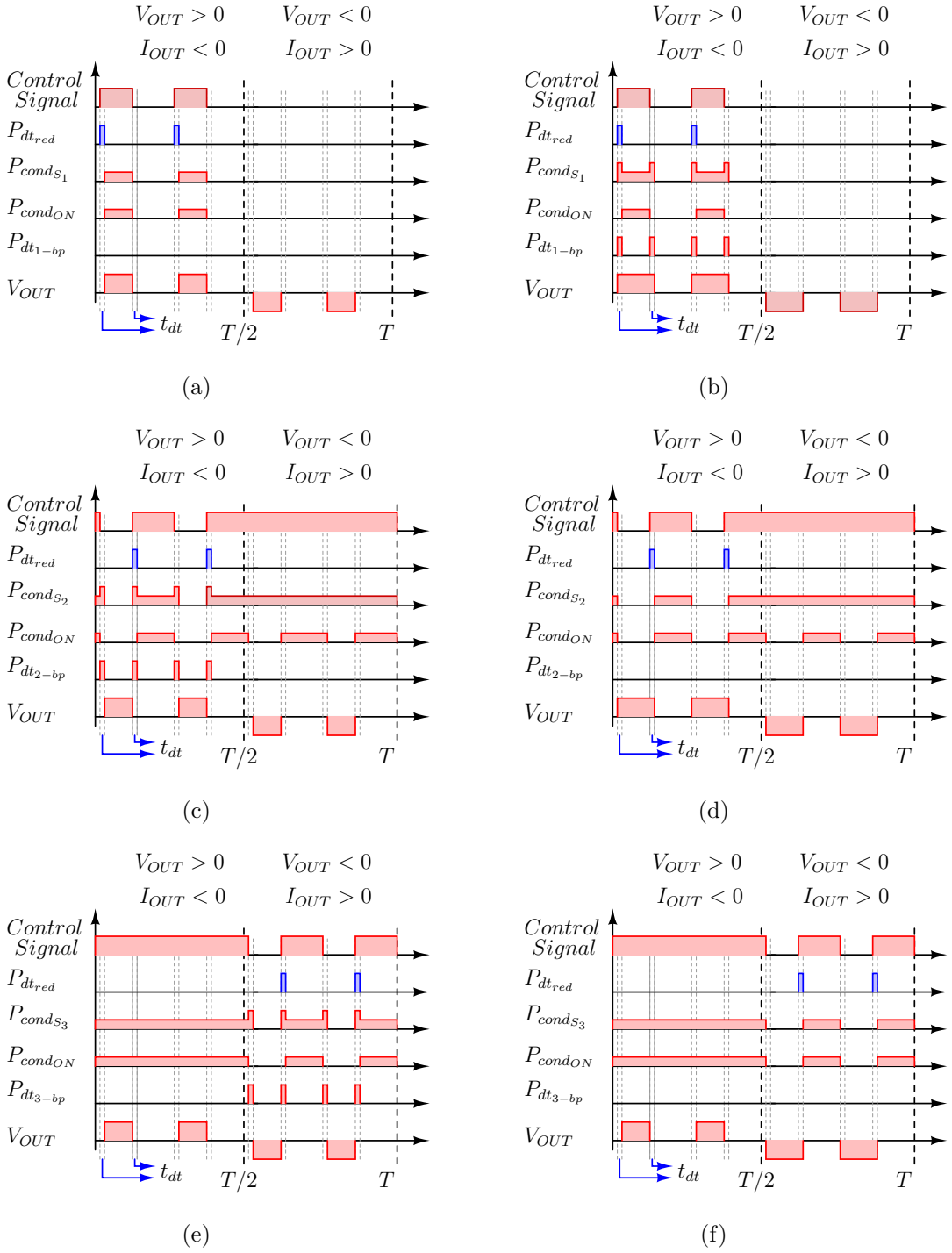


Figure 5.9: Conduction instants of switches in ANPC inverter: a) S_1 switch when power factor is equal to 1, b) S_1 switch when power factor is equal to 0, c) S_2 switch when power factor is equal to 1, d) S_2 switch when power factor is equal to 0, e) S_3 switch when power factor is equal to 1, f) S_3 switch when power factor is equal to 0.

for arbitrary power factor can be calculated as:

$$P_{cond_{S_3}} = P_{S_3+} + P_{S_3-} \tag{5.24}$$

where P_{S_3+} and P_{S_3-} are conduction losses at positive half and negative half of output voltage respectively. At positive half of the output voltage, S_3 is completely on and therefore will at both active and zero states. Based on $P_{cond_{S_1}}$ in Eq. 5.20 and P_{S_2+} in Eq. 5.22 and considering that S_3 is turned-on at dead time instants, the conduction loss of S_3, P_{S_3+}, can be expressed as:

$$P_{S_3+} = P_{cond_a} + \frac{P_{cond_z}}{4} + P_{dt_{1-up}} + P_{dt_{1-up}} - \frac{5 \cdot P_{dt_{red}}}{4} \tag{5.25}$$

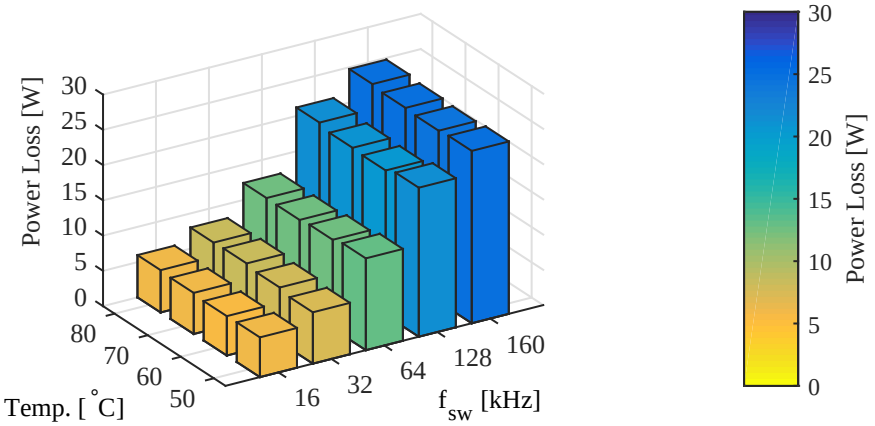
At the negative half of output voltage, as shown in Figs. 5.9c, 5.9d, 5.9e and 5.9f, the loss profile of S_3 is same as the loss profile of S_2 at the positive half of output voltage. Therefore, based on Eq. 5.22, P_{S_3-} is:

$$P_{S_3-} = \frac{P_{cond_z}}{4} + P_{dt_{2-bp}} - \frac{P_{dt_{red}}}{4} \tag{5.26}$$

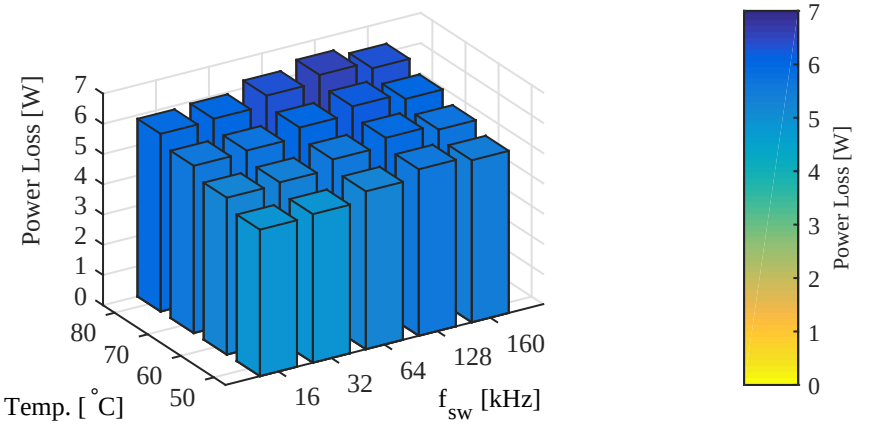
With symmetrical output current and voltage waveforms (e.g. no DC offset, no overmodulation), the total conduction loss P_{cond_t} in one fundamental cycle can be calculated as:

$$P_{cond_t} = 2 \cdot \left(P_{cond_{S_1}} + P_{cond_{S_2}} + P_{cond_{S_3}}\right) \tag{5.27}$$

The loss figures for five different switching frequencies and four different heat sink temperatures at 1.3 kW output power in terms of total, switching and conduction losses are presented in Figs. 5.10a, 5.10b and 5.10c respectively. As it is shown in previous section, the total loss increases with respect to increase in switching frequency, and it can be seen in Fig. 5.10c that main contributor to this is the increase in switching loss. At low switching frequencies such as 16 kHz and 32 kHz, the total power cell loss is dominated by conduction loss. At 64 kHz, the switching loss is at the same range with conduction loss and dominates the total power cell loss at 128 kHz and 160 kHz switching frequencies. The switching loss is independent from heat sink temperature and the conduction loss increase gradually with the increase of R_{DS}. One thing to note in Fig. 5.10b is the increase of conduction loss with the increase of switching frequency. This is due to the increase of proportion of dead time in a switching period which increases the dead-time losses linearly in Eqs. 5.11, 5.13, 5.15 and 5.17 with $t_{dt} \cdot f_{sw}$ term.



(a)



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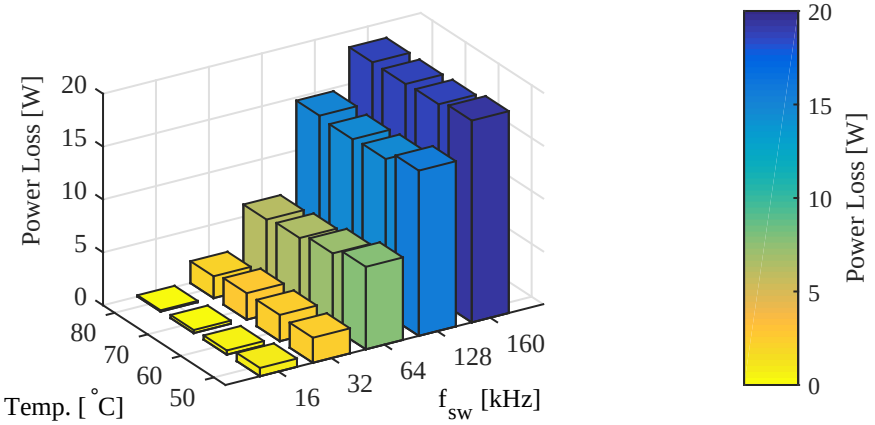


(c)

Figure 5.10: Loss breakdown for GaN based ANPC converter at 1.3 kW output: (a) total power device loss, (b) conduction loss, (c) switching loss.

5.3 Impact on Converter Volume

The overall efficiency analysis under various output power, switching frequency and heat sink temperature conditions shows that GaN HEMTs can be used to design inverters at high frequency, high heat sink temperature in order to reduce heat sink volume and output inductor volume without compromising the efficiency. In this section, the impact of high performance of GaN HEMTs on heat sink volume and output filter volume is investigated. The impact analysis is based on following assumptions:

- Cooling system is based on natural air convection.
- Single stage LC output filter is used.
- Converter output power is rated at 2000W.

5.3.1 Heat Sink Design

The heat sink volume analysis is based on calculation of required thermal resistance r_{h_r} for heat sink at maximum output power, between 16 kHz and 160 kHz switching frequencies, and between 50°C and 80 °C heat sink temperatures. The maximum heat sink temperature is limited to 80 °C, as the higher heat sink temperature condition may lead to exceeding maximum allowed junction temperature, which is 150 °C for GaN HEMT devices. The thermal network for ANPC inverter is illustrated in Fig. 5.11 where T_j is junction temperature, T_h is heat sink temperature, T_a is room temperature (chosen as 25 °C), P_{loss} is power loss across a single device, r_{jc} is junction-to-case thermal resistance, r_{ch} is chase-to-heat sink thermal resistance and r_{h_r} is required thermal resistance of the heat sink. The junction temperature for a device T_{j_x} and required heat sink thermal resistance r_{h_r} can be calculated as follow:

$$S_x : T_{j_x} = P_{loss_x} \cdot \left(r_{jc_{loss_x}} + r_{ch_{loss_x}}\right) + T_h \tag{5.28}$$

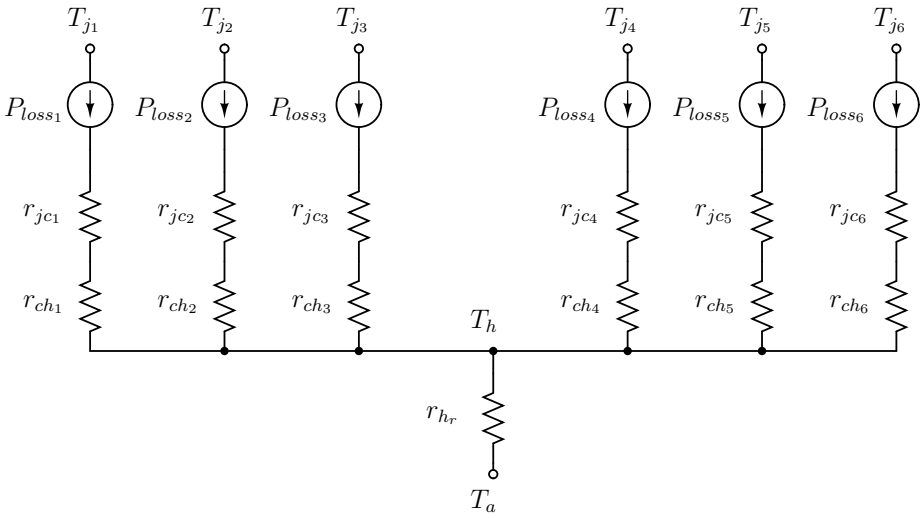


Figure 5.11: Thermal network for ANPC inverter.

$$r_{h_r} = \frac{T_h - T_a}{P_t} \tag{5.29}$$

where P_t is total power device loss and x can be replaced with device number 1 to 6. Calculated r_{h_r} then can be used to calculate volume of heat sink based on natural air convection. The volume of various extruded naturally cooled heat sinks against heat sink thermal resistance are presented in Fig. 5.12 [100]. Based on the results, curve fitting is applied to minimum heat sink volume available at given r_{h_r} value and presented in Eq. 5.30. By using r_{h_r} from Eq. 5.29 in Eq. 5.30, volume of extruded naturally cooled heat sink can be calculated for different device case temperature, ambient temperature and power loss.

$$Vol_{heatsink} = 286.71 \cdot r_{h_r}^{-1.468} \tag{5.30}$$

Based on Eqs. 5.29 and 5.30, the calculated heat sink volume with respect to switching frequency for different heat sink temperatures is presented in Fig. 5.13. It can be seen that the heat sink volume increases with the increase of switching frequency. The heat sink volumes at 16 kHz for 50 ^{o}C and 80 ^{o}C are 202 cm^3 and 76 cm^3 respectively. As the switching frequency is increased to 160 kHz, the heat sink volume goes up to

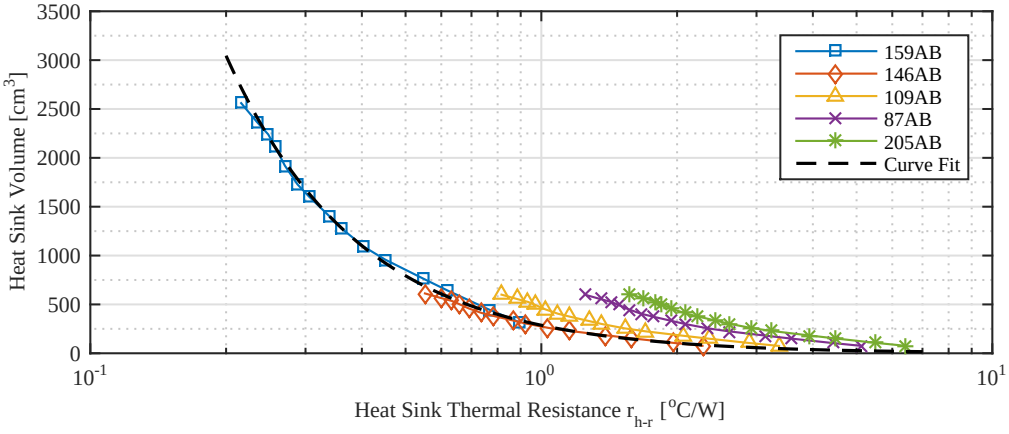


Figure 5.12: Commercial naturally cooled heat sink volumes [100].

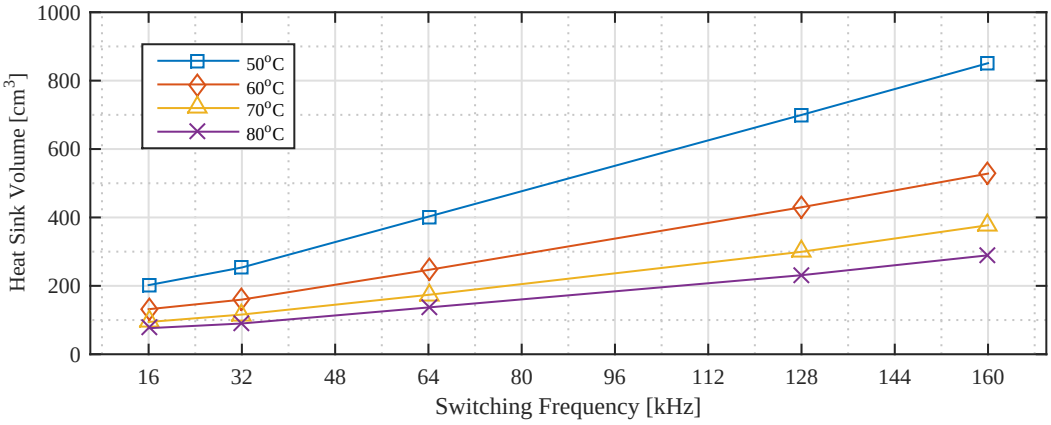


Figure 5.13: Heat sink volume versus switching frequency at different heat sink temperatures.

851 cm^3 (increase by factor of 4.21) and 290 cm^3 (increase by factor of 3.81) for these two temperature conditions. The increase in heat sink temperature from 50 ^{o}C to 80 ^{o}C provides heat sink volume reduction by factor of 2.66 at 16 kHz, and by factor of 2.93 at 160 kHz switching frequencies. The impact of heat sink volume reduction in overall volume will be discussed after output filter design.

5.3.2 Output Filter Design

Grid connected power inverters must have an output filter in order to minimize the injected harmonics to the grid that are caused by high switching frequency. Passive filters are usually chosen in grid connected applications due to its simplicity and high performance. The size of the filter depends on number of stages and order of the filter. One of the most common type of filter is second order single stage LC filter at considered power range and presented in Fig. 5.14 [101]. L_{grid} in Fig. 5.14 is the impedance of the grid after point of common coupling and can depend on the length of grid cables, connected loads and sources to the grid. In addition to the output filter, EMI filter should be included in the final inverter design to comply with grid operator requirements. However, it is shown in previous results with GaN HEMT and SiC MOSFET that the variation in switching frequencies that can be achieved with WBG devices is very broad based on the experimental results. Therefore even if an optimum value has been suggested, a number of consideration on the control would have to be entered to finalise the study. EMI filter re-design appears meaningful mainly after evaluating the impact of WBG device on output filter and heat sink volume.

Passive component and output filter volume is inversely related to switching frequency. Therefore, it is interesting to analyse the trade-off between increased power losses due to increased switching frequency and reduction in filter volume. To begin the analysis, based on Fig. 5.5b, the expression that defines loss of the power cell $P_{Loss_{GaN}}$ with respect to switching frequency f_{sw} at 2000W output power and variable heat sink temperature can be written as:

$$P_{Loss_{GaN}} = k_{t_{GaN}} \left(0.23015 f_{sw} + 15.6352\right) \tag{5.31}$$

where $k_{t_{GaN}}$ is:

$$k_{t_{GaN}} = 0.002855 \cdot T_h + 0.85725 \tag{5.32}$$

and f_{sw} is in kHz.

In this study, single stage LC filter, which is the common type differential output

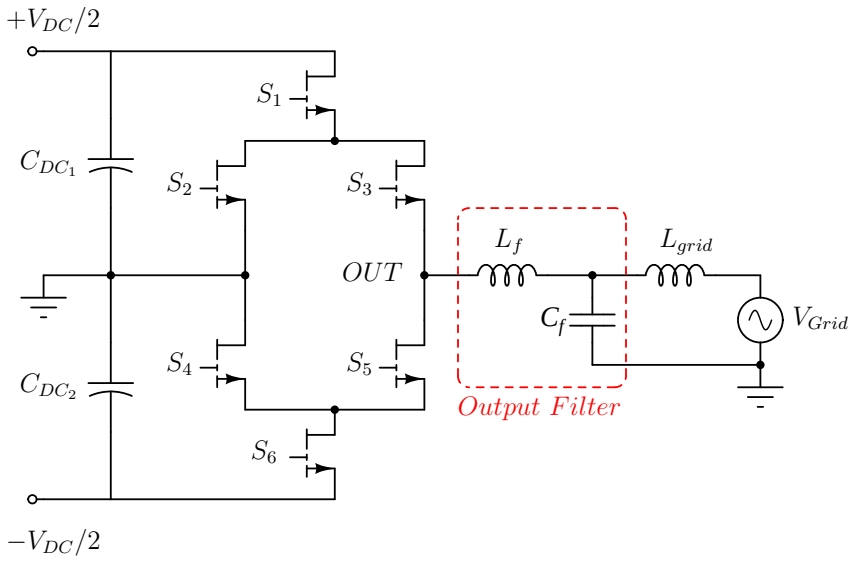


Figure 5.14: Grid connected single-phase T-type inverter.

filter for power converters at this power range, is considered [101]. The design of LC filter starts with calculation of filter inductance L_f for defined maximum output ripple current by using 5.33. Calculated L_f is then used in 5.34 in order to calculate output capacitance:

$$L_f = \frac{V_{DC}}{8 \cdot \Delta I_{OUT} \cdot f_s} \tag{5.33}$$

$$C_f = \frac{1}{(2\pi \cdot f_s)^2 \cdot L_f \cdot Att_{req}} \tag{5.34}$$

Where V_{DC} is DC link voltage, ΔI_{OUT} is output current ripple, f_s is switching frequency and Att_{req} is required attenuation of the filter [101], [102]. The required attenuation is chosen as 0.01 in order to provide adequate damping at switching frequency and keep the resonance frequency far away from inverter switching frequency. Output current ripple ΔI_{OUT} is chosen as 20% of peak output current for limiting maximum power device switching current and keeping inverter output current ripple in reasonable level. Based on Eqs. 5.33 and 5.34, calculated inductance and capacitance values for different switching frequencies are presented in Table 5.2.

By using inductance and capacitance values in Table 5.2, volume of the LC filter can be calculated with area-product approach for inductor, and capacitor volume constant

Switching Frequency	**16 kHz**	**32 kHz**	**64 kHz**	**128 kHz**	**160 kHz**
Inductance L_f [mH]	2.2	1.1	0.556	0.278	0.222
Capacitance C_f [μF]	4.45	2.225	1.11	0.556	0.445

Table 5.2: Inductance and capacitance values for output filter at different switching frequencies.

for capacitor. After [103], the area-product A_p and volume of a power inductor can be calculated as:

$$A_p = \left[\frac{\sqrt{1+\gamma} \cdot K_i \cdot L_f \cdot \widehat{I}^2}{B_{max} \cdot K_t \cdot \sqrt{k_u \cdot \Delta T}} \right]^{\frac{8}{7}} \tag{5.35}$$

$$Vol_L = k_L \cdot {A_p}^{\frac{3}{4}} \tag{5.36}$$

where γ is ratio of iron loss to copper loss (is taken to be 0.03 or less for AC inductors with small high frequency flux ripple), B_{max} is maximum flux density in inductor core, K_i is current waveform factor ($I_{rms}/\widehat{I}$), K_t is 48.2×103, $\widehat{I}$ is peak inductor current, k_u window utilization factor (based on window fill factor, proximity and skin effects) and k_L is inductor volume constant. Maximum flux density is based on performance factor of ferrite material ($f \times B_{max}$) N87 in [104]. In this case flux density is kept at the level to achieve fixed core losses at different switching frequencies. Maximum temperature rise ΔT is chosen as 60 °C with natural cooling and without any heat sink in order to keep current density in the windings high enough while keeping maximum core temperature within recommended operating temperature limits. The maximum flux density for fixed core losses is approximated with the following equation:

$$B_{max} = \begin{cases} 0.35 \text{ mT} & f_{sw} < 25 \text{ kHz} \\ |1.111 \cdot 10^4 \cdot f_{sw}^{-0.3104} - 132.3| \cdot 10^{-3} \text{ mT} & 25 \text{ kHz} < f_{sw} < 200 \text{ kHz} \end{cases} \tag{5.37}$$

Based on the calculated area-product value, the core with the higher closest area-product value to the calculated is selected for each switching frequency condition. After selection of the core from manufacturer data book in [104], the required air-gap in the magnetic flux path can be calculated as follow:

$$l_g = \frac{E_{stored} \cdot \mu_0}{B_{max}^2 \cdot A_e} \tag{5.38}$$

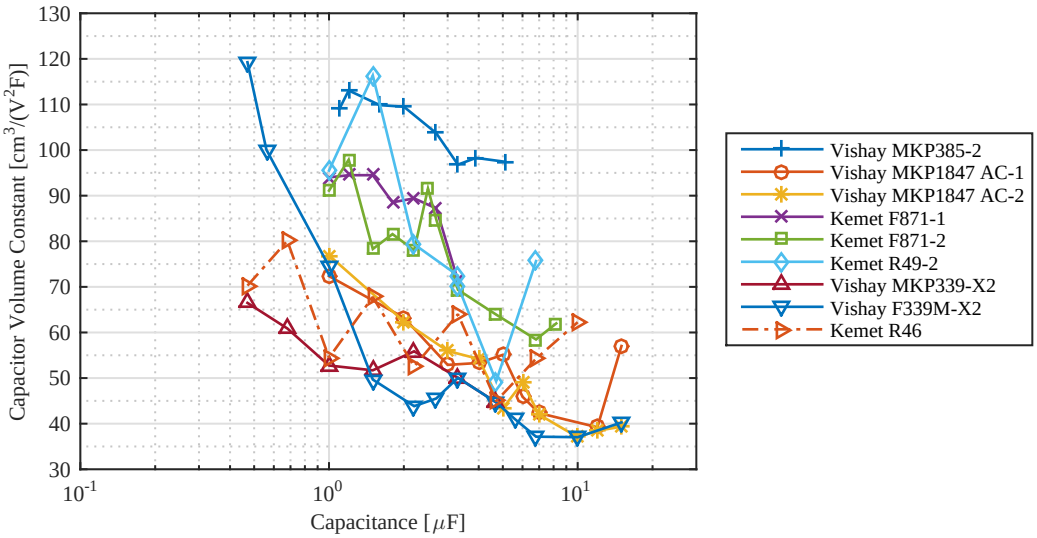


Figure 5.15: Capacitor volume constant for various filter capacitors for grid connected applications.

where A_e is effective core area, which is specified by the core manufacturer, and E_{stored} is the maximum stored energy in the core:

$$E_{stored} = 0.5 \cdot L_f \cdot \widehat{I}^2 \tag{5.39}$$

The reluctance of the magnetic path R is then calculated with the assumtion that the permability of the core is much higher than vacuum ($\mu_r >> \mu_0$):

$$R = \frac{l_g}{A_e \cdot \mu_0} \tag{5.40}$$

With the calculation of the reluctance, the required number of turns for required filter inductance can be calculated as follow:

$$N = \sqrt{L_f \cdot R} \tag{5.41}$$

Based on the calculated of window utilisation factor from [103], number of turns and skin effect in the windings, number of litz wires can be calculated and the appropriate wire thickness can be selected.

The next step in volume analysis of LC filter is the selection of filter capacitor. The

Switching Frequency	**16 kHz**	**64 kHz**	**128 kHz**
Inductor Volume [cm^3]	266.3	141.7	96.4
Capacitor Volume [cm^3]	20.2	5.1	4
Total Volume [cm^3]	286.5	146.8	100.4

Table 5.3: Inductor, capacitor and total volume for output filter at 16, 64 and 128 kHz switching frequencies.

volume of filter capacitor can be calculated by the following equation:

$$Vol_C = k_c \cdot C_f \cdot {V_{nom}}^2 \tag{5.42}$$

Where V_{nom} is nominal voltage of capacitor and k_c is capacitor volume constant in $cm^3/(V^2F)$. A survey is conducted to evaluate the volume of capacitors for grid connected output filter applications (X2 type) and the capacitor volume constant of different capacitors from different manufacturers are presented in Fig. 5.15. It can be seen that the k_c varies for different manufacturers and also capacitance values. The MKP339-X2 series is selected as it has the lowest k_c over wide range of capacitance [105]. The k_c for MKP339-X2 series is approximated as 60.

The inductor and capacitor volumes for each switching frequency case in Table 5.2 are calculated using Eqs. 5.33 - 5.42. Based on the calculation results, three filter cases have been realised for 16 kHz, 64 kHz and 128 kHz switching frequencies. The realised filters are presented in Fig. 5.16 and the inductor volume, capacitor volume and total filter volume values are presented in Table 5.3. It should be noted that the calculated exact capacitance value according to Eq. 5.34 cannot be purchased, therefore the closest values to the ones presented in Table 5.2 (4.7 μF for 16 kHz, 1 μF for 64 kHz and 680 μF for 128 kHz) are used.

The comparison of the calculated and realised volumes for the inductor, capacitor and total filter are presented in Fig. 5.18. It can be seen that the calculated values for inductor and capacitor are well matched with the realised filter. In Fig. 5.18, it is also shown that the total filter volume is dominated by the inductor volume and the rate of volume reduction for inductor reduces beyond 64 kHz. The total filter volume can be reduced by factor of 2 with the increase of switching frequency from 16 kHz

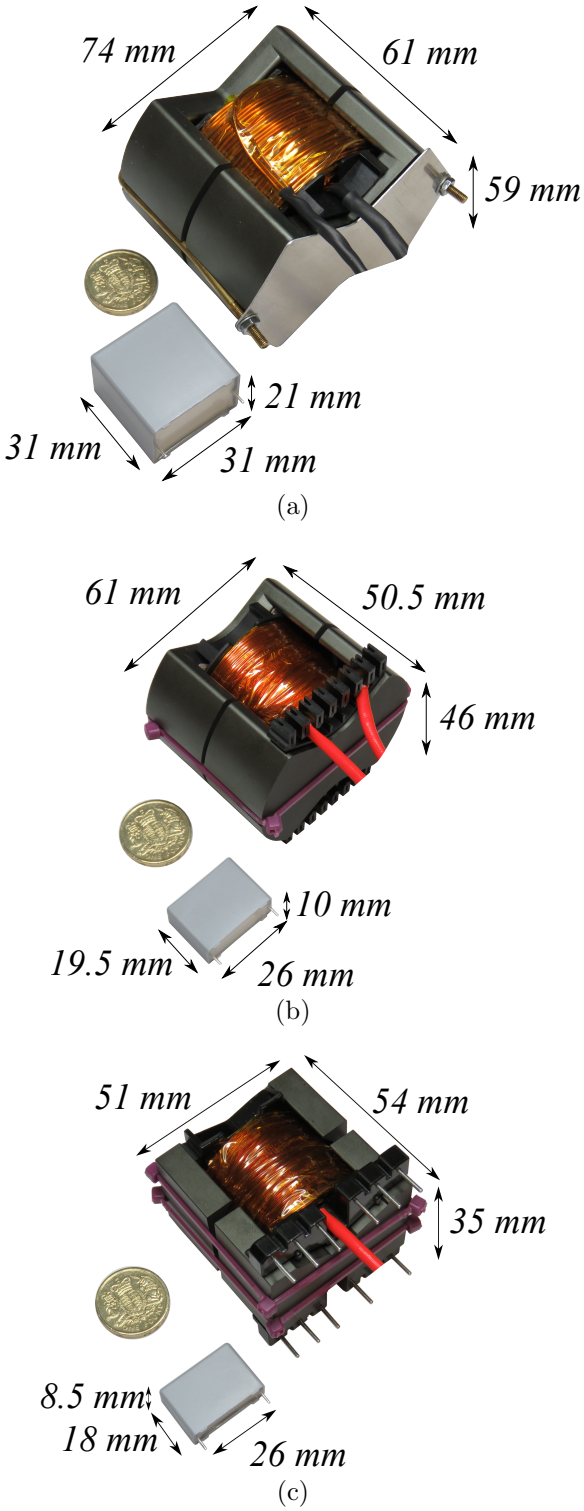
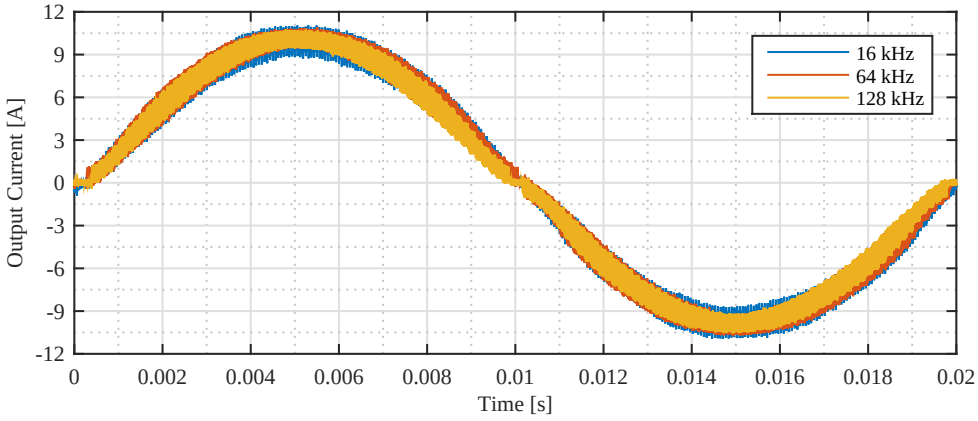


Figure 5.16: Designed LC filters for three different switching frequencies: a) 16 kHz b) 64 kHz and c) 128 kHz.

to 64 kHz. The factor of reduction increases to 2.86 as the switching frequency is increased to 128 kHz. There are two reasons for reduction in rate of reduction beyond 64 kHz: 1) The increase of core size as the core losses is aimed to be kept constant, 2) The reduction of fill factor in winding area due to increase of skin effect. The skin effect causes increase in number of wires in parallel and reduction in wire diameter to achieve low AC resistance at given switching frequency with desired current density in the winding.

The performance of the designed filter inductors are evaluated at 1.6 kW output power at their designed switching frequencies: 16 kHz, 64 kHz and 128 kHz. The output power is kept constant for each test condition by slight increase in modulation index due to fixed dead time and the heat sink temperature is kept at 30 ^{o}C. The fundamental output current waveform, switching ripple and the loss results for three operating cases are presented in Figs. 5.17a, 5.17b and 5.17c respectively. It can be seen that the peak to peak ripple current at the output is almost constant for three operating conditions and below the design limit (ΔI_{OUT}). The loss results in Fig. 5.17c shows that the efficiency of the power cell or the filter is not compromised with reduction of output filter size. The filter inductor loss is almost constant at 64 kHz and 128 kHz, and smaller than at 16 kHz due to reduced number of turns.

In order to include the temperature and power cell loss impact to the volume reduction analysis, the filter volume, heat sink volume and the total volume of filter and heat sink volume are presented with respect to switching frequency at different heat sink temperatures in Figs. 5.19a, 5.19b and 5.19c. It can be seen that heat sink volume is almost equal to filter volume at 32 kHz, 50 ^{o}C and dominates the total volume beyond 32 kHz in Fig. 5.19a. When the heat sink temperature is increased to 80 ^{o}C, as shown in Fig. 5.19b, the filter and heat sink volume crosses around 64 kHz. The overall comparison in Fig. 5.19c shows that the increased heat sink temperature can bring significant volume reduction at switching frequencies above 64 kHz and low heat sink temperatures such as 50 ^{o}C and 60 ^{o}C can lead to increase in overall volume as the heat sink dominates the total volume.



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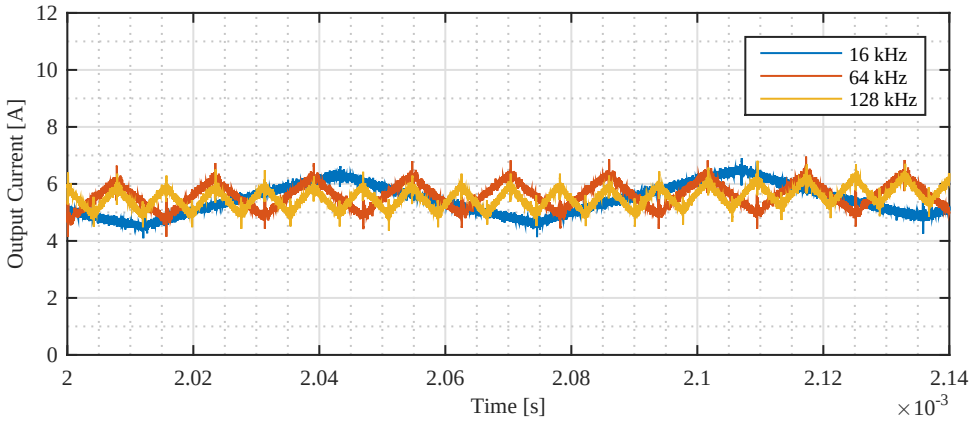

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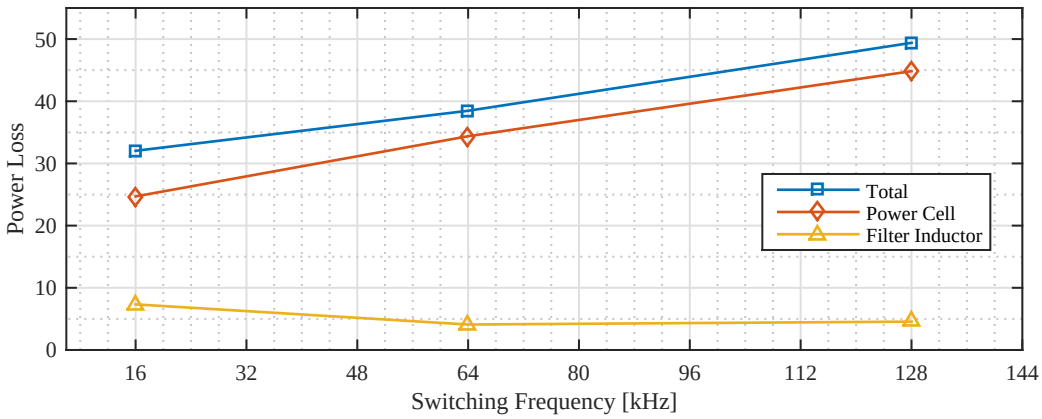


(c)

Figure 5.17: Output current waveform with designed inductor at 1.6 kW output power and 16 kHz, 64 kHz and 128 kHz switching frequencies: a) fundamental waveform, b) switching ripple, c) total, power cell and inductor loss.

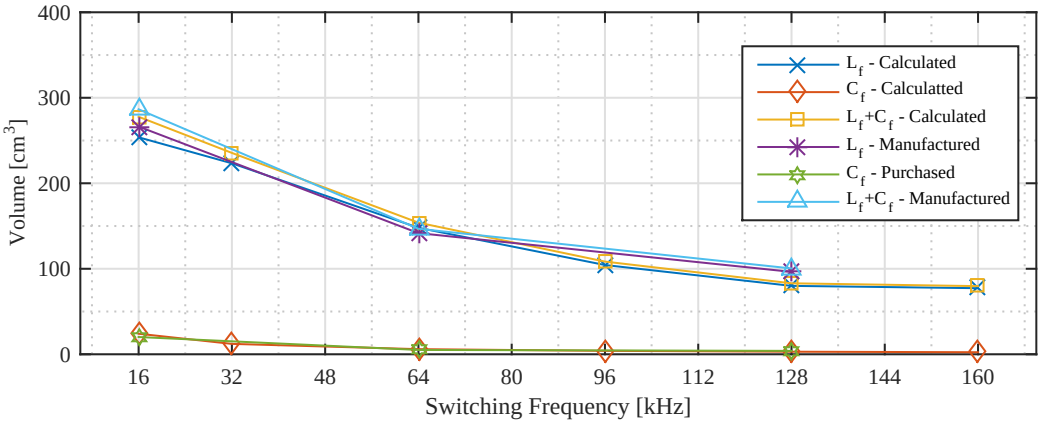
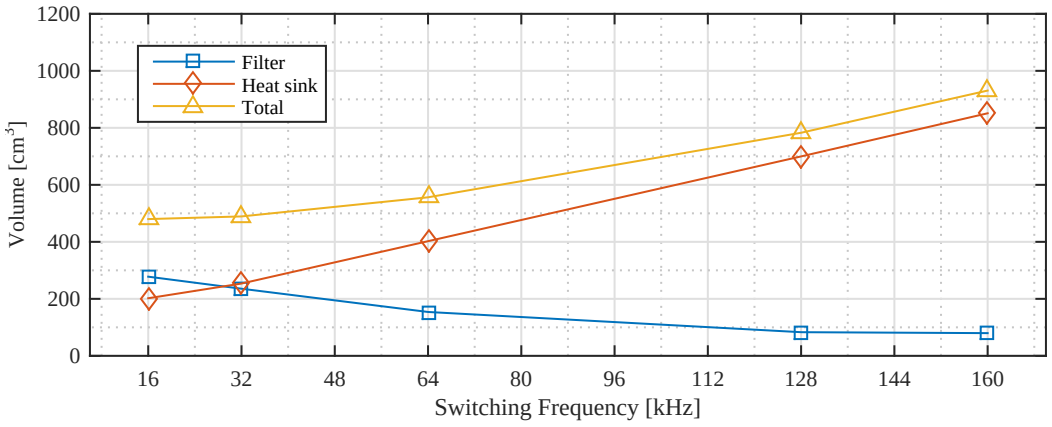
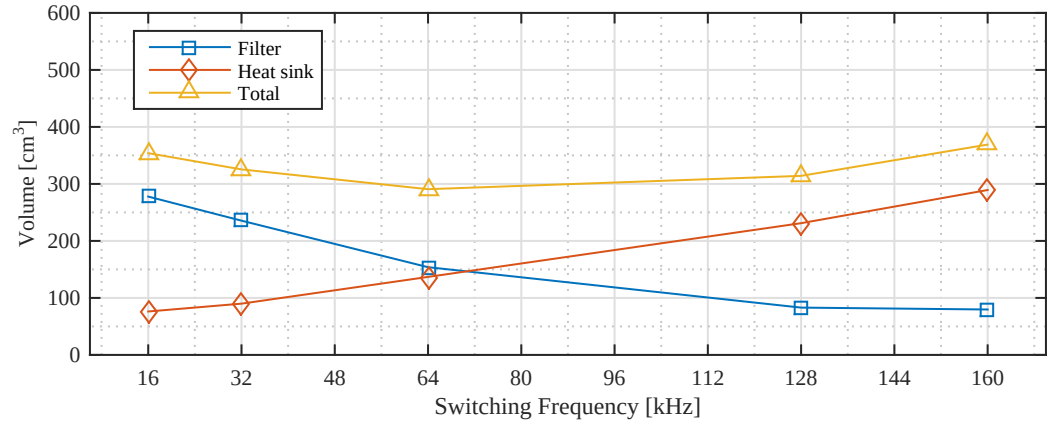


Figure 5.18: Calculated and realised inductor, capacitor and total filter volume versus switching frequency.

Finally total volume is plotted with respect to switching frequency and heat sink temperature in Fig. 5.20a, and with respect to power cell loss at different heat sink temperatures in Fig. 5.20b to give an overall summary of impact of GaN HEMT performance in heat sink and output filter volume. It can be seen in Fig. 5.20a that the increase of switching frequency leads to increase of total volume at low heat sink temperatures due to increase in heat sink size, and at high heat sink temperatures, increase of switching frequency beyond 64 kHz does not lead to significant decrease in total volume. Contrary, above 128 kHz the total volume starts to increase again due to heat sink volume. In terms of the comparison of total volume and power loss, Fig. 5.20b shows that at 50 °C, increase of power loss by factor of 1.6 times (16 kHz to 64 kHz) leads to increase in total volume by 1.16 times. On the other hand, at 80 °C, increase of power loss by factor of 1.5 times (16 kHz to 64 kHz) leads to decrease in total volume by 1.22 times. Therefore, it can be seen that the optimum operating point to minimise the total volume with minimum impact on inverter efficiency is 64 kHz switching frequency with 80 °C heat sink temperature.



(a)



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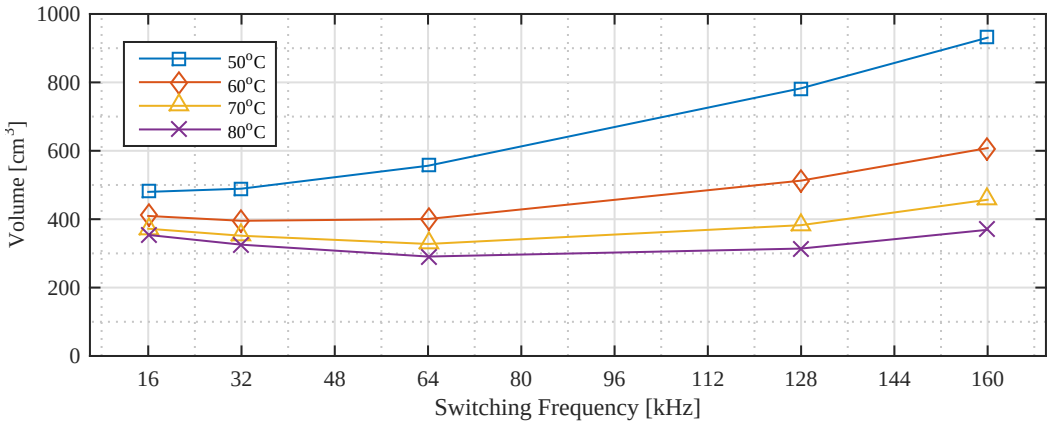
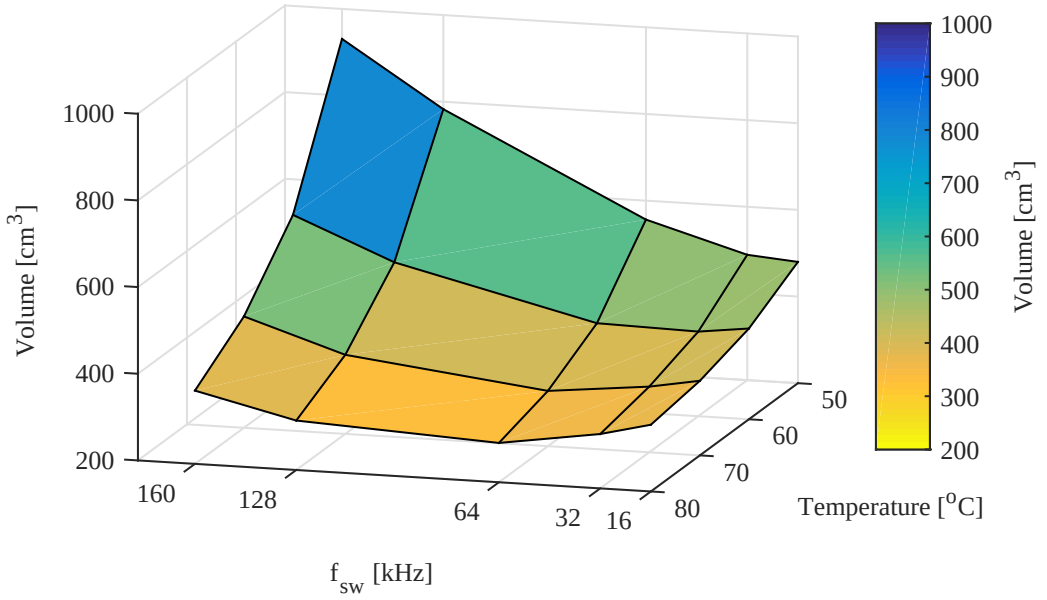
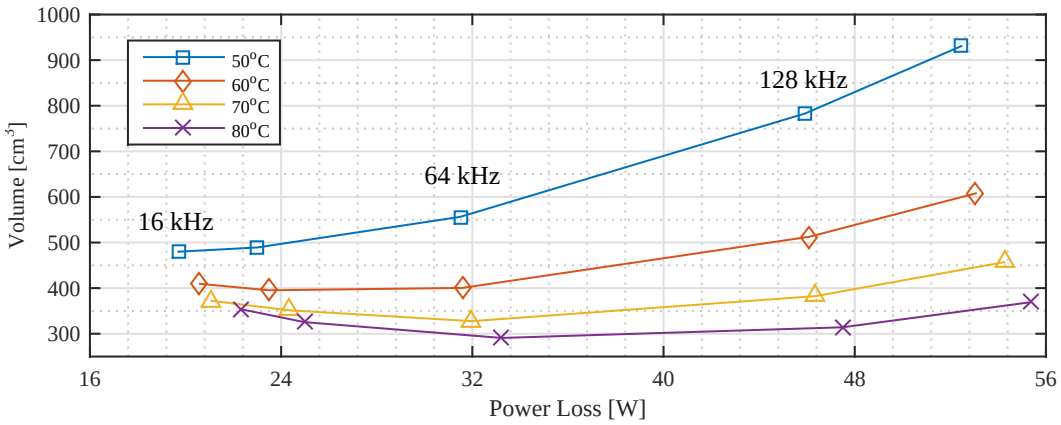


(c)

Figure 5.19: Filter, heat sink and total volume versus switching frequency: a) at 50 °C heat sink temperature, b) at 80 °C heat sink temperature and c) total volume versus switching frequency at four different heat sink temperature.



(a)



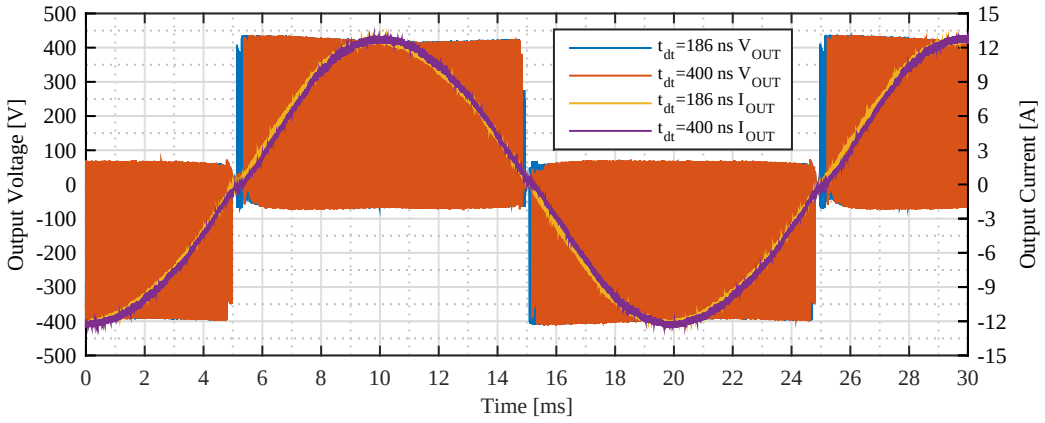
(b)

Figure 5.20: a) Total volume versus switching frequency and heat sink temperature, b) total volume versus power cell loss.

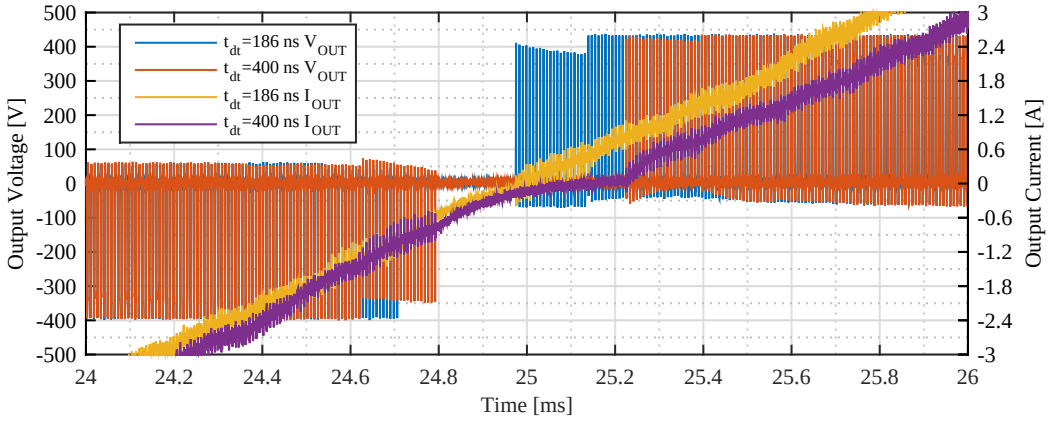
5.3.3 Dead Time Impact

Dead time between commutating switches S_1-$S_{2,5}$ and S_6-$S_{3,4}$, where both switches are turned-off, is introduced in order to avoid shoot through. During dead-time, the control of output voltage is lost and the output voltage can be clamped to $+V_{DC}/2$, $-V_{DC}/2$ or 0 depending on the direction of current. The effect of dead-time becomes severe at higher switching frequencies and lower modulation index values. The harmonic analysis and compensation of dead-time effect for voltage source converters have been studied in [106] ,[107]. In this work, it is defined as 400 ns but the switching results of SiC and GaN in Chapter 4 show that the dead-time for wide-bandgap devices can be as small as 100 ns due to high switching speeds.

In order to evaluate the effect of dead-time in ANPC inverter with GaN HEMT, the inverter is run at 128 kHz switching frequency at three different dead time values: 186 ns, 300 ns and 400 ns. The output voltage and current waveforms for 186 ns and 400 ns at maximum output power for 1.5 fundamental cycle is presented in Fig. 5.21a. The zoomed section of the zero-crossing of the output waveforms in Fig. 5.21a is presented in Fig. 5.21b and it can be seen that increase in dead time increases the distortion in current waveform increases. The reason for this distortion is due to elimination of output voltage pulses in Fig. 5.21b with duty ratio of less than 0.0512 and 0.0238 for 400 ns and 186 ns dead-times respectively. The blanking in the output current increases the THD and therefore output filter requirements. The variation of output current THD with respect to dead-time is presented in Fig. 5.22a. It is clear that minimum dead-time value has to be used with SiC and GaN devices regardless efficiency concerns in order to utilize high switching performance that allows reduction in filter volume. Finally, the impact of dead time to overall power cell loss is presented in Fig. 5.22b for three different dead time conditions. It can be seen that the additional power loss due to increased dead time is negligible in light load conditions. However, above 1200 W output power, the power loss starts to differentiate for different dead time values and the difference in power loss can be up to 3.7 W at 1830 W output power, which corresponds to approximately 0.2 % efficiency difference.

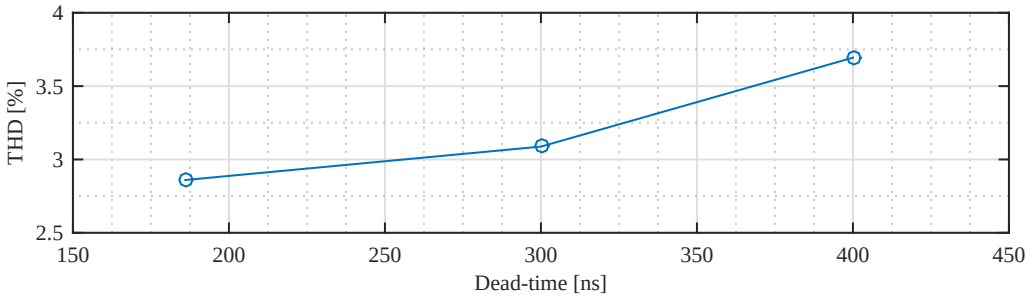


(a)



(b)

Figure 5.21: Effect of different dead time values a) fundamental period, b) zoomed at zero crossing.



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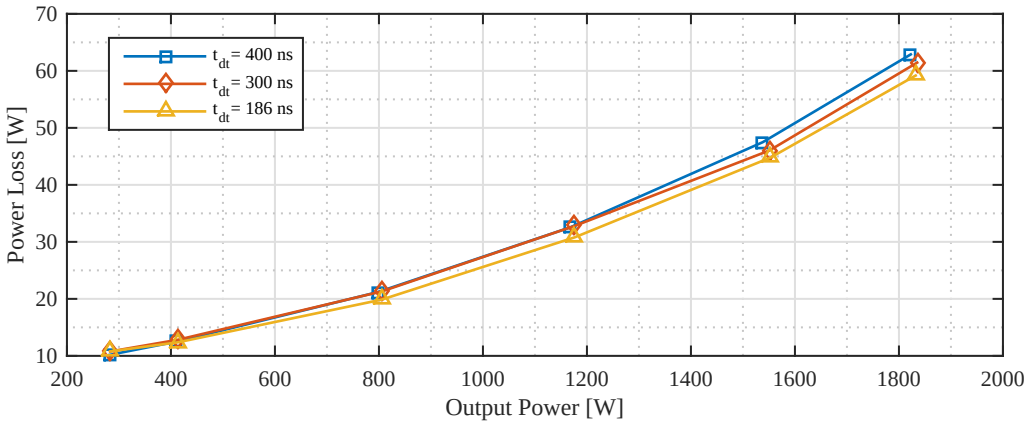


(b)

Figure 5.22: Effect of different dead time values to a) output current total harmonic distortion, b) power cell loss.

5.4 Mission Profile Based Analysis

In addition to high efficiency of WBG devices presented in Chapter 4 and previous section of this chapter, high reliability is required for PV inverters in order to extend lifetime of the system and therefore energy generation [108], and as a consequence to reduce the cost of energy. Commercial PV inverters are generally offered with a 25 year performance warranty, and also considered as the most vulnerable components in a PV system [109]. It is known from field data that a majority of the failure mechanisms for PV inverters are related to mean temperature variations and temperature swings [110]; therefore long-term mission-profile plays a key role in reliability and assessment of thermal performance of the inverter [111], [112]. During design process, real-field operating conditions (e.g., ambient temperature and solar irradiance) have to be considered for reliability-oriented approaches, as different conditions may unevenly stress the components within the system. As shown in Chapters 3 and 4, emerging SiC and GaN power devices have different electrical and thermal properties from Si devices due to inherent differences in material, chip size and packaging properties [113]. Therefore, it is essential to evaluate the long-term performance of the system for better understanding the benefits as well as the drawbacks of using WBG devices in PV systems. In such a way, the applications of WBG devices can further be paved away.

In this section, a reliability-oriented comparison of the Si IGBT with GaN HEMT for ANPC based PV system is thus presented. The dynamic and static comparison of Si IGBT and GaN HEMT have been discussed in Chapter 4. First, the converter topology and overall system are presented, followed by a mission-profile oriented analysis in terms of thermal loading and reliability estimation of the considered power electronic converters. Simulation results of the converter based on GaN and Si devices are presented in Section 5.4.1 regarding efficiency, annual energy generation, loss distribution and thermal loading.

The schematic of the studied converter for a double-stage three-phase grid-connected PV system is presented in Fig. 5.23. As it can be observed, each leg of the 3L-ANPC

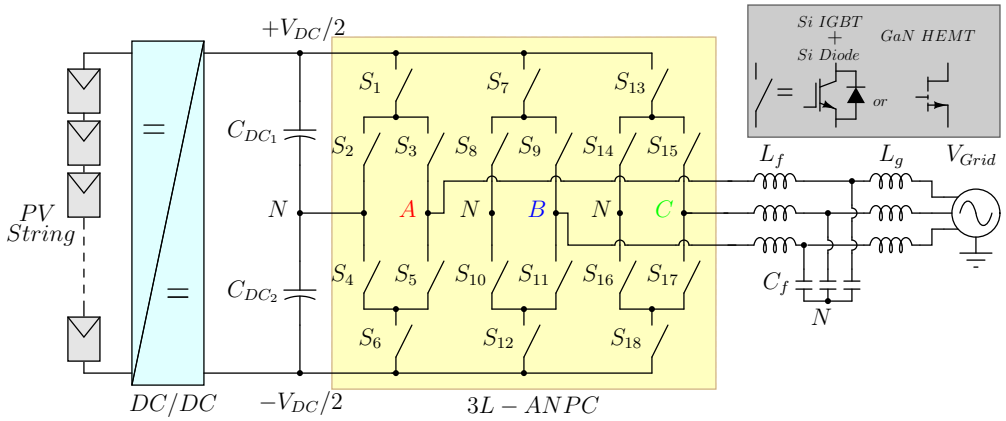


Figure 5.23: Grid-connected three-phase double-stage 3L-ANPC inverter with an LCL filter in PV applications

inverter is formed by 6 active switches (S_1-S_{18} of three legs) in order to achieve a three-level phase output voltage with respect to the neutral point N, and the power devices (S_1-S_{18}) are rated at half of the DC link voltage V_{DC}. Consequently, as discussed earlier, it is possible to use GaN HEMT devices at 600 V class for three-phase grid-connected applications, where the DC link voltage is within a range of 650-1000 V. In this configuration, a DC-DC converter between the PV strings and the 3L-ANPC inverter is adopted in order to flexibly maximize the energy production (i.e., MPPT control) as well as to extend the operating hours of the PV systems (e.g., in the case of weak solar irradiance). The power delivered by the DC/DC converter is then fed to the 3L-ANPC inverter, while the DC-link voltage is usually maintained as constant by controlling the output current of the inverter. Normally, for the PV system, it should inject high-quality grid currents at unity power factor operation, and thus the modulation schemes applied to the 3L-ANPC inverter should be specially designed. In this study, same modulation scheme presented in Fig. 5.8b is used.

The PV system and converter parameters considered in this study are presented in Table 5.4. As the DC/DC converter between PV strings and the 3L-ANPC inverter that is shown in Fig. 5.23 is responsible from the MPPT control, it is assumed that the conversion efficiency of 99 % can be achieved by the MPPT control of the converter in the following. Recent advances in SiC MOSFETs show that efficiency

Table 5.4: Converter and System Parameters

Parameter	Value
Input DC Link Voltage (V_{DC})	800 V
Input Power (P_{in}) @ 25 °C, 1000 W/m^2	3 kW
Switching Frequency (f_{sw})	16 kHz & 128 kHz
DC Link Capacitor ($C_{DC_1} - C_{DC_2}$)	1500 μF
Output Filter Inductor (L_f)	3.6 mH
Output Filter Capacitor (C_f)	2.35 μF
Output Filter Capacitor (L_g)	4 mH
Grid Phase-to-Phase Voltage (V_{ph-ph})	400 Vrms
PV Module	BP 365
PV String Configuration	46 module in series
DC/DC (MPPT) Efficiency (η_{MPPT})	99 %
Evaluated Devices	PGA26C09DS IGP20N60H3

higher than 99 % is feasible for DC/DC converters in PV applications [114]. A single PV string, formed by 23 PV modules, is considered to deliver 3 kW power at the standard test conditions (i.e., 25 °C ambient temperature and 1000 W/m^2 solar irradiance). The power of the PV panel with respect to solar irradiance at different ambient temperatures is presented in Fig. 5.24. It can be seen from Fig. 5.24 that the input power P_{in} can go up to 5.5 kW at -25 °C and 1500 W/m^2 theoretically, and therefore maximum total rating of the converter is selected as 6 kW in order to operate at a wide range of ambient temperature and solar irradiance. The inverter is operated at 16 kHz switching frequency for Si IGBTs; while at 16 kHz and 128 kHz for GaN HEMT devices for evaluation of the performance of GaN HEMT based inverter at low and high switching frequencies in comparison to the Si IGBT based inverter. Selection of 128 kHz for high frequency application of the GaN HEMTs is determined by the experimental performance of GaN HEMTs shown in Section 5.2, where the junction temperature of most stressed devices is close to their limits, and the efficiency is still above 97 %. Additionally, it is shown in [115] that by moving to very high switching frequencies (e.g. beyond 100 kHz), 70 % reduction in EMC filter volume can be achieved for GaN HEMTs.

The thermal loading of the power electronic devices, which is the combination of

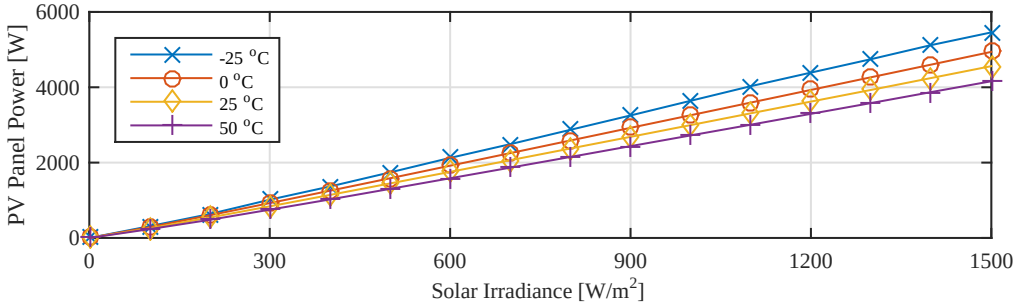


Figure 5.24: PV panel output power with respect to solar irradiance and ambient temperature.

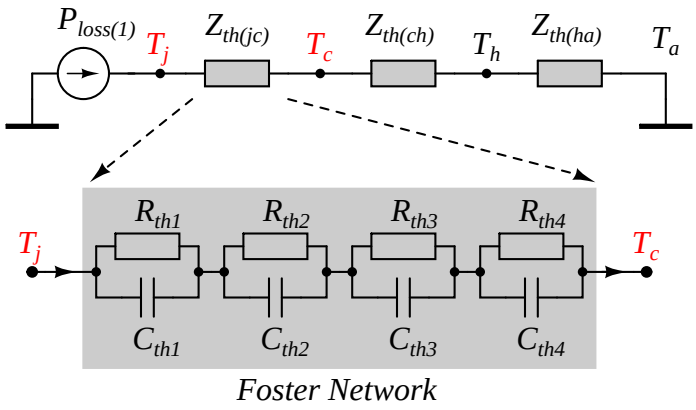


Figure 5.25: Thermal model of a single power device, where the RC layer number is related to the device packaging technology as indicated in Table 5.5.

dynamic and static temperature variation across power device, is still the major lifetime affecting factor, which is an essential part for reliability analysis. Hence, a thermal model of a single device is presented in Fig. 5.25. The device thermal network consists of thermal impedances between device junction and device case ($Z_{th(jc)}$), case and heat sink ($Z_{th(ch)}$), and heat sink and ambient ($Z_{th(ha)}$). As the thermal parameters of GaN HEMT are not clearly indicated in the device datasheet, thermal characterisation has been conducted to calculate the thermal impedance of the device. The thermal impedance of the device and the curve fit based on the Foster equation is presented in Fig. 5.26. The Foster network is formed by 5 series connected RC networks to model the experimentally measured thermal impedance.

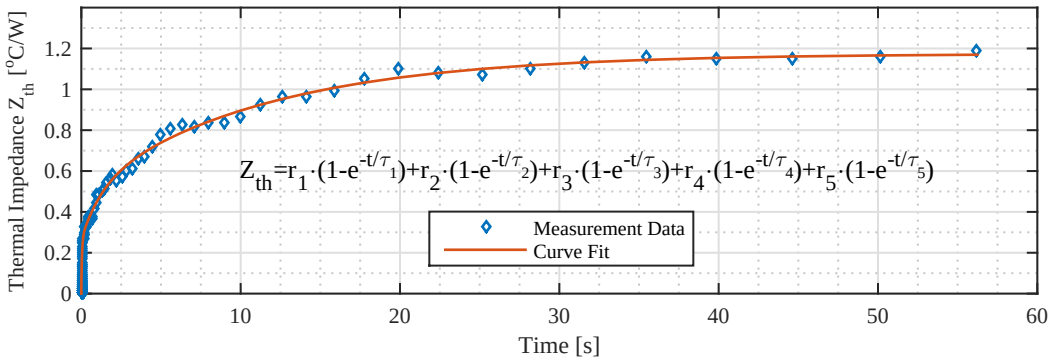


Figure 5.26: Thermal impedance of GaN HEMT and applied curve fit for derivation of Foster network.

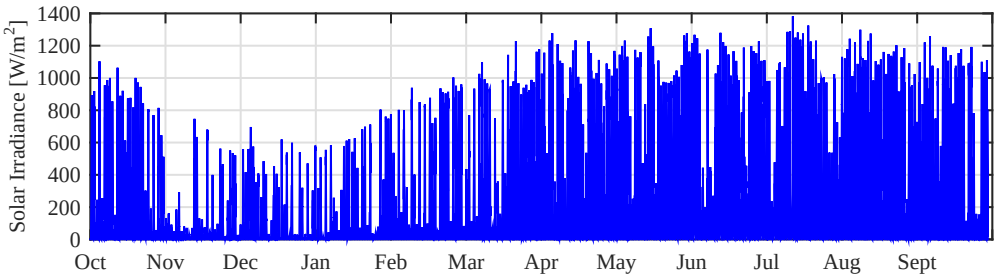
Based on manufacturer datasheet of the Si IGBT and thermal measurement results for the GaN HEMT in Fig. 5.26, Foster network parameters for junction-to-case impedance are presented in Table 5.5. Obtained Foster network parameters are transferred to the Cauer network in the simulation environment for accurate thermal modelling. Notably, the device thermal model is implemented along with the electrical model (see Fig. 5.23) in order to obtain the thermal performance with respect to converter instantaneous loading conditions, which are highly dependent on the solar and ambient temperature profiles and in return affect the semiconductor switch properties. As mentioned in Chapter 4, the package of GaN HEMT is fully insulated and due to this reason there is no need for additional insulation between the backside of the package and the heat sink. However for Si IGBTs, thermally-conductive insulator with 0.57 °K/W thermal resistance and 4 kV breakdown voltage is considered for isolation of discrete devices from common heat sink [116]. The common heat sink for the devices is modelled as a simple RC circuit. There are two reasons for this simplification: 1) The analysis in this study focuses on the thermal profile analysis of steady-state device junction temperature and the heat sink will not have significant effect on thermal loading comparison, 2) Simplification of heat sink model leads to acceleration of long-term mission profile simulations. Junction temperature comparisons will be presented over an annual mission profile by simulations in Section 5.4.1.

Table 5.5: Thermal parameters for Si IGBT, Si Diode and GaN HEMT.

Impedance		$Z_{th(j-c)}$				
i		1	2	3	4	5
Si IGBT	R_{thi} [°K/W]	0.07041042	0.3070851	0.3198984	0.1871538	-
	τ_i [s]	0.000096	0.00068	0.01084623	0.06925485	-
Si Diode	R_{thi} [°K/W]	0.4398	0.6662	0.4734	0.3169	-
	τ_i [s]	0.00013	0.0011	0.0071	0.04629	-
GaN HEMT	R_{thi} [°K/W]	0.01167	0.03065	0.2246	0.2413	0.6661
	τ_i [s]	0.00009676	0.002868	0.04835	1.284	11.46

It is necessary to evaluate the performance of power electronic systems in long-term operation along with short-term operation, as the long-term operation profiles can have significant impact on efficiency, reliability and lifetime of the entire system [110]. For short-term evaluation, time-based simulation tools or prototype based experiments can be conducted to assess the performance but both of these approaches are not suitable for long-term evaluation due to constraints of time, computational and financial resources. Therefore an efficient method is required to evaluate the long-term performance (see Figs. 5.28 and 5.29) [110], [111]. The long term PV mission profile consists of solar irradiance level (S_i) and ambient temperature (T_a). In this study, a real-field annual PV mission profile data (i.e., solar irradiance level and ambient temperature) in Aalborg, Denmark is considered. The measured annual solar irradiance and ambient temperature data are presented in Fig. 5.27.

Realisation of the long-term mission profile based analysis is presented in Fig. 5.28. The first step of this analysis is to obtain the maximum power (P_m) operation points with respect to the PV module output voltage (v_{pv}) for the PV string specified in Table 5.4, based on the measured different solar irradiance (S_i) and ambient temperature (T_a). Then maximum power and operation voltage is fed into the short-term simulation model in order to obtain power loss (P_{tot}) and temperature profile (T_j) for each switching device in correspondence to an individual operation point (e.g., P_m = 3 kW, V_{pv} = 400 V for the case of 25 °C and 1000 W/m^2). The maximum output power of the PV panel with respect to solar irradiance and ambient temperature is presented in Fig. 5.24. The losses and temperature performance are finally curve-fitted with respect to the entire solar irradiance and ambient temperature spectrum



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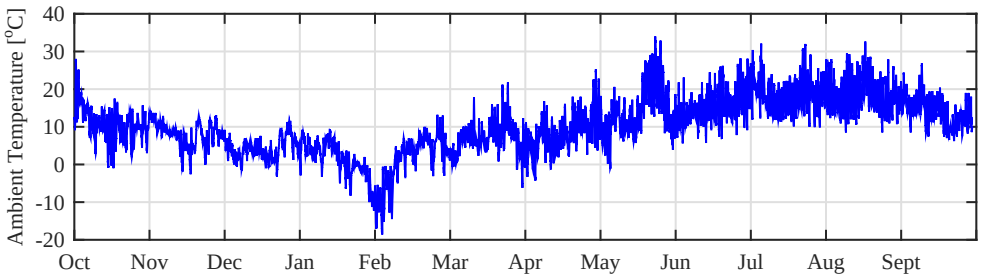


(b)

Figure 5.27: An annual mission profile used in this thesis: (a) solar irradiance and (b) ambient temperature profile in Aalborg.

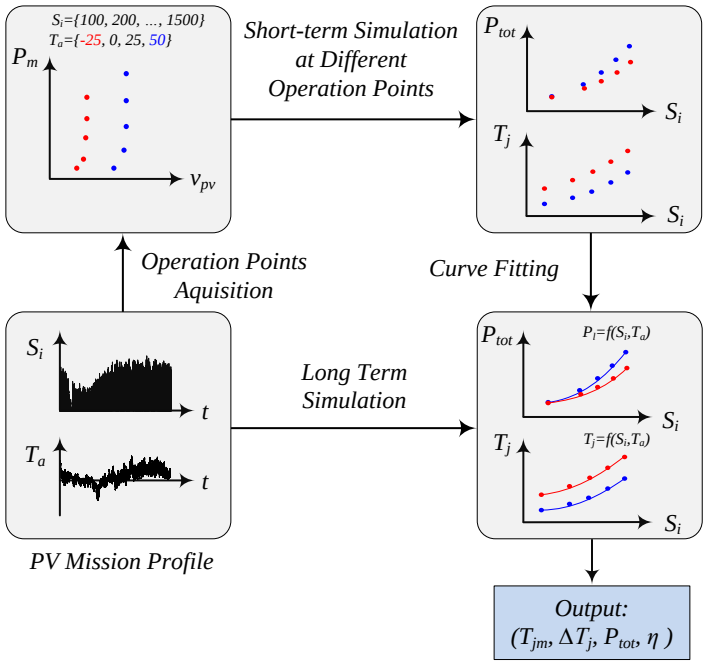


Figure 5.28: Realisation of the long-term mission profile based analysis approach.

in such a way to link a specific mission profile with the power electronic converter (electrical behaviour). It should be pointed out here that the MPPT control (dc-dc converter) efficiency has been assumed to 99%, since the focus of the work is not on the MPPT control.

The detailed structure of the multi-disciplinary analysis method can be seen in Fig. 5.29. Short-term simulation model consists of two domains: thermal model and electrical model, which are linked via the power device model. In the electrical model, device blocking voltage V_{off} and on-state current I_{on} are calculated based on the operating point P_{in} and then transferred to the power device model in order to calculate switching and conduction losses. The calculated loss data then fed to thermal model along with ambient temperature T_a from mission profile to calculate the junction temperature T_j and to the electrical model for calculation of the total converter losses. In addition to electrical parameters, the thermal model also feeds the device junction temperature T_j to the power device data in order to calculate the device losses with respect to device temperature. The calculated device loss P_{loss} is then used in the electrical model to evaluate converter efficiency and in the thermal model to recalculate junction temperature T_j. This bidirectional data exchange between different simulation domains provide results that can be used for better understanding the thermal and electrical performance, enabling the multi-disciplinary evaluation of the implemented modulation scheme, power devices and converter topologies. The conduction and switching data of Si IGBT and GaN HEMT are obtained from the performed static and dynamic benchmarking of the devices at different heat sink temperatures in Chapter 4.

5.4.1 Simulation Results

The simulations based on the approach explained in details in the previous section are carried out on a single phase 3L-ANPC inverter with the assumption of a balanced three phase grid system and operation. In this case, the analysis results can be extended to the three-phase 3L-ANPC converter shown in Fig. 5.23. Input power,

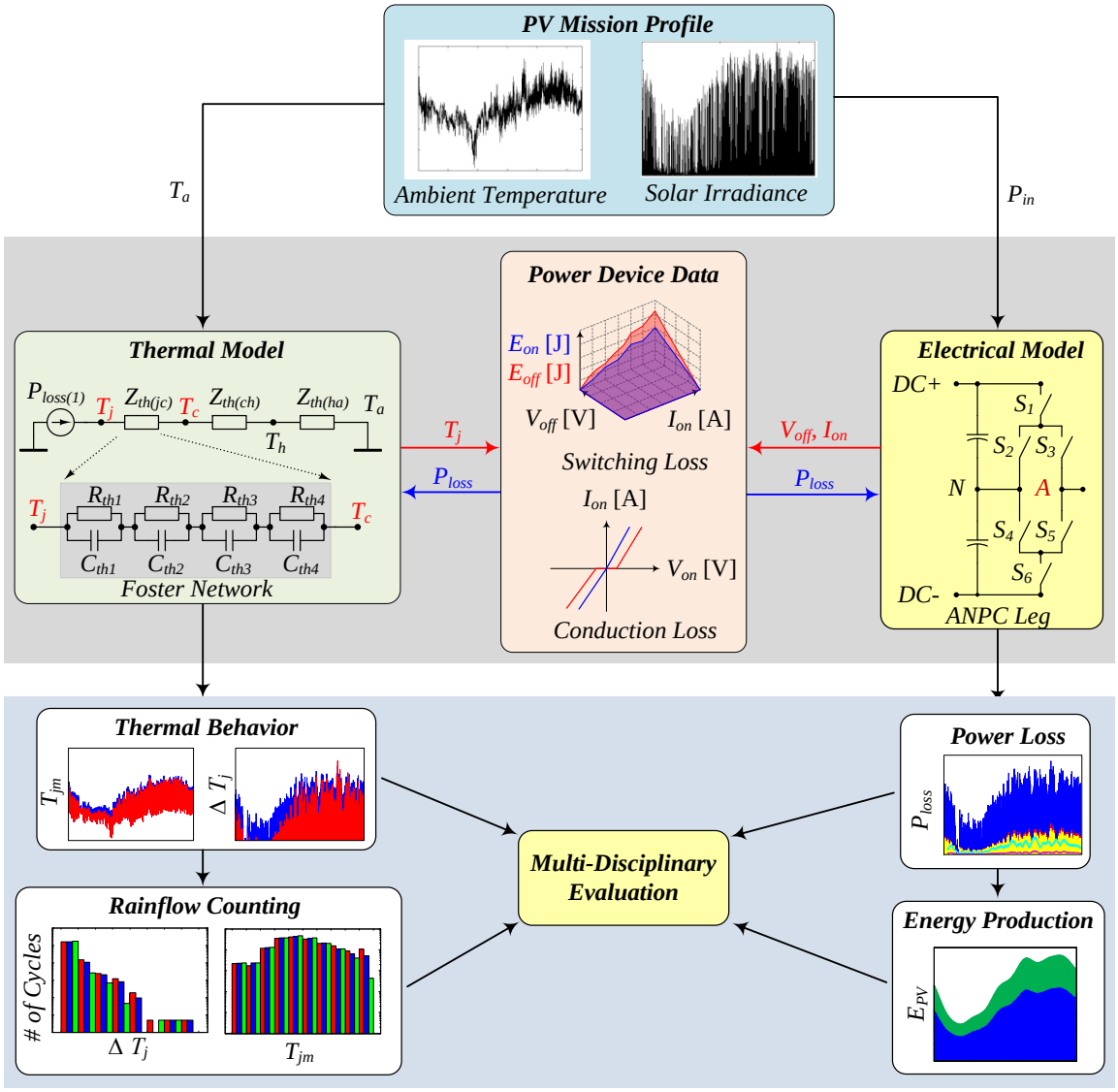
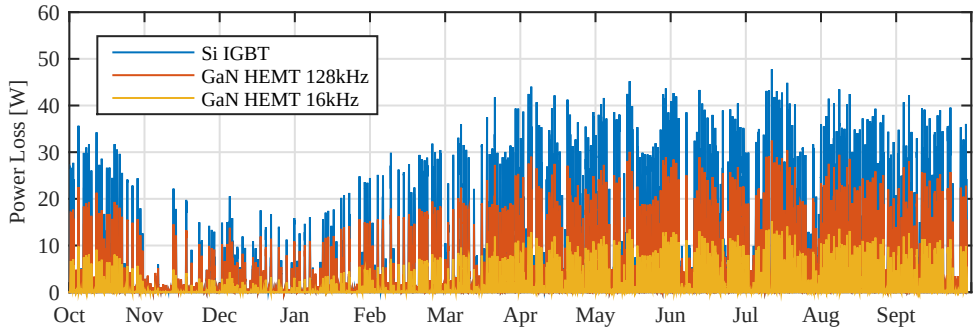


Figure 5.29: Multi-disciplinary analysis method.

total conduction losses and total switching losses are recorded for converter performance evaluation according to the multi-disciplinary approach. In addition to this, power losses, mean and maximum junction temperatures for each device are recorded for device in order to evaluate the loss distribution, thermal stress and behaviour of each power switch in a single 3L-ANPC leg. In the beginning of this section, overall inverter performance is presented including inverter loss breakdown, annual power loss and cumulative energy loss for Si IGBT and GaN HEMT based scenarios. These results are followed by the thermal stress comparison of each power device including the power loss distribution, mean junction temperature and junction temperature variation for most stressed devices in the specific configuration.

5.4.1.1 Overall Power Loss and Energy Generation

The annual power loss and cumulative energy loss of three-phase 3L-ANPC inverter with Si IGBTs at 16 kHz, and with GaN HEMTs at 16 kHz and 128 kHz are presented in Fig. 5.30. As it is expected from the results presented in Chapter 4 and previous sections of this chapter, the GaN-based 3L-ANPC inverter has higher efficiency, and therefore less power losses throughout the year in comparison to those of the Si IGBT based 3L-ANPC inverter. The cumulative energy loss for the Si IGBT based inverter is around 29.51 kWh, and in contrast, for the GaN-based inverter at 16 kHz and 128 kHz is 6.05 kWh and 21.87 kWh, respectively. At the switching frequency of 128 kHz, although the GaN HEMTs are switched 8 times more than Si IGBTs, the associated additional energy losses due to the increased switching frequency is 54% of the total energy losses of the Si IGBT based inverter. The average electricity price in Denmark in 2014 for household consumers is 0.304 €/kWh [117]. Without considering thermal benefits of reduced converter losses, if the feed-in tariff is assumed to be same as the utility tariff, it can be concluded that the GaN HEMT based inverter at 16 kHz will bring additional €7.13 to the owner in comparison to the Si IGBT based inverter. At 128 kHz, the GaN HEMT based inverter will not bring significant operation income to the owner, whereas will provide reduction in initial system cost saving due to the reduction in cooling and output filtering requirements, as shown in Chapter 4 and



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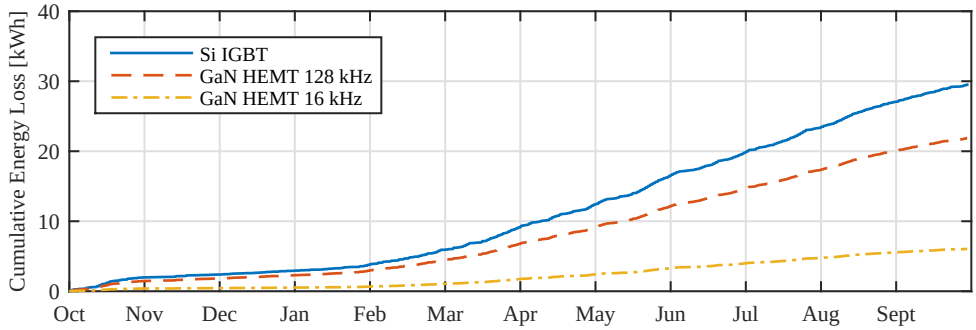


(b)

Figure 5.30: Estimated annual power losses and cumulative energy loss of the ANPC inverter based on different technologies using the mission-profile analysis approach: (a) annual power losses and (b) cumulative energy losses.

previous sections of this chapter.

Conduction and switching loss breakdown of the Si and GaN based inverter phase leg are presented in Fig. 5.31. With respect to four different ambient temperatures and at maximum solar irradiance for the given ambient temperature profile. At 16 kHz switching frequency, the conduction losses are dominating the overall converter losses for the Si IGBTs. Meanwhile, the losses reduce with respect to the temperature increase due to the reduction in the input power and relatively small temperature dependence of conduction performance of Si IGBTs at low collector current levels as presented in Chapter 4, despite the fact that switching losses increase according to ambient temperature. On the other hand, the switching losses of the GaN HEMT

based inverter leg is negligible at 16 kHz and the total losses are dominated by the conduction losses. The switching losses increase as the switching frequency is moved from 16 kHz to 128 kHz in Fig. 5.31b and 5.31c, but the overall loss of the phase leg is still less than Si IGBT based inverters, as it is shown in Fig. 5.31a. As the size of heat sink volume is inversely proportional to required thermal resistance r_{h_r} as shown in Eq. 5.29, the heat sink volume of the GaN HEMT based inverter at 128 kHz will still be smaller than that in the case of the Si based inverter. Therefore, heat sink can still contribute to system level cost saving for the GaN based inverter at a very high switching frequency.

5.4.1.2 Thermal Stress Comparison

The applied modulation scheme, which is used in this work and presented earlier in Fig. 5.8b, provides low conduction losses with the penalty of uneven loss distribution in the 3L-ANPC phase leg at unity power factor operation. During the positive half cycle of the output voltage, S_1 is subject to hard switching and also conducts during active state, while S_3 conducts during positive and zero states, and S_2 only conducts during zero states. Therefore, it is expected to see highest power losses across S_1 or S_3 switches depending on the device switching, conduction performance and inverter switching frequency. The loss distributions for upper devices in the 3L-ANPC - phase leg-A in Fig. 5.23 are presented in Fig. 5.32 for Si and GaN. In the Si-based inverter, due to the unity power factor operation, antiparallel diodes D_2 and D_3 only conduct during positive and negative zero states. Although S_3 has higher conduction losses than S_1, S_1 has the highest losses in the inverter leg due to the switching loss contribution presented in Fig. 5.31 (a). On the other side, for the GaN based inverter at 16 kHz and 128 kHz in Fig. 5.32b and 5.32c, the loss distributions among S_1 and S_3 vary with respect to the selected switching frequency. High switching performance of the GaN HEMTs shows the impact at 16 kHz by keeping power losses of S_1 almost same with S_3. By increasing the switching frequency to 128 kHz, switching losses become significant in overall losses (Fig. 5.31c), resulting in that S_1 has the highest power loss in the inverter leg.

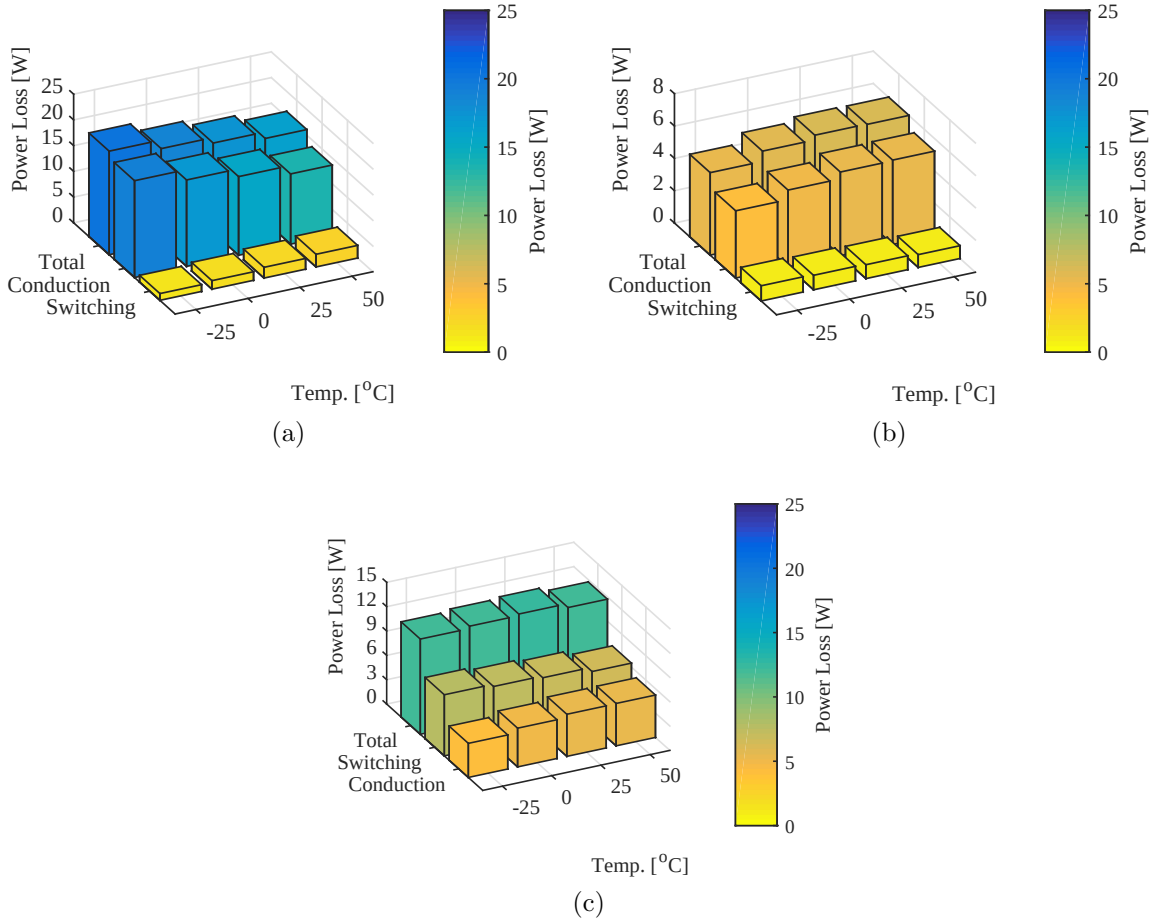


Figure 5.31: Semiconductor total, conduction, and switching losses per phase leg of the ANPC inverter based on: (a) Si IGBT technology with a switching frequency of 16 kHz, (b) GaN HEMT technology with a switching frequency of 16 kHz, and (c) GaN HEMT technology with a switching frequency of 128 kHz, where different ambient temperatures with the maximum solar irradiance level are considered.

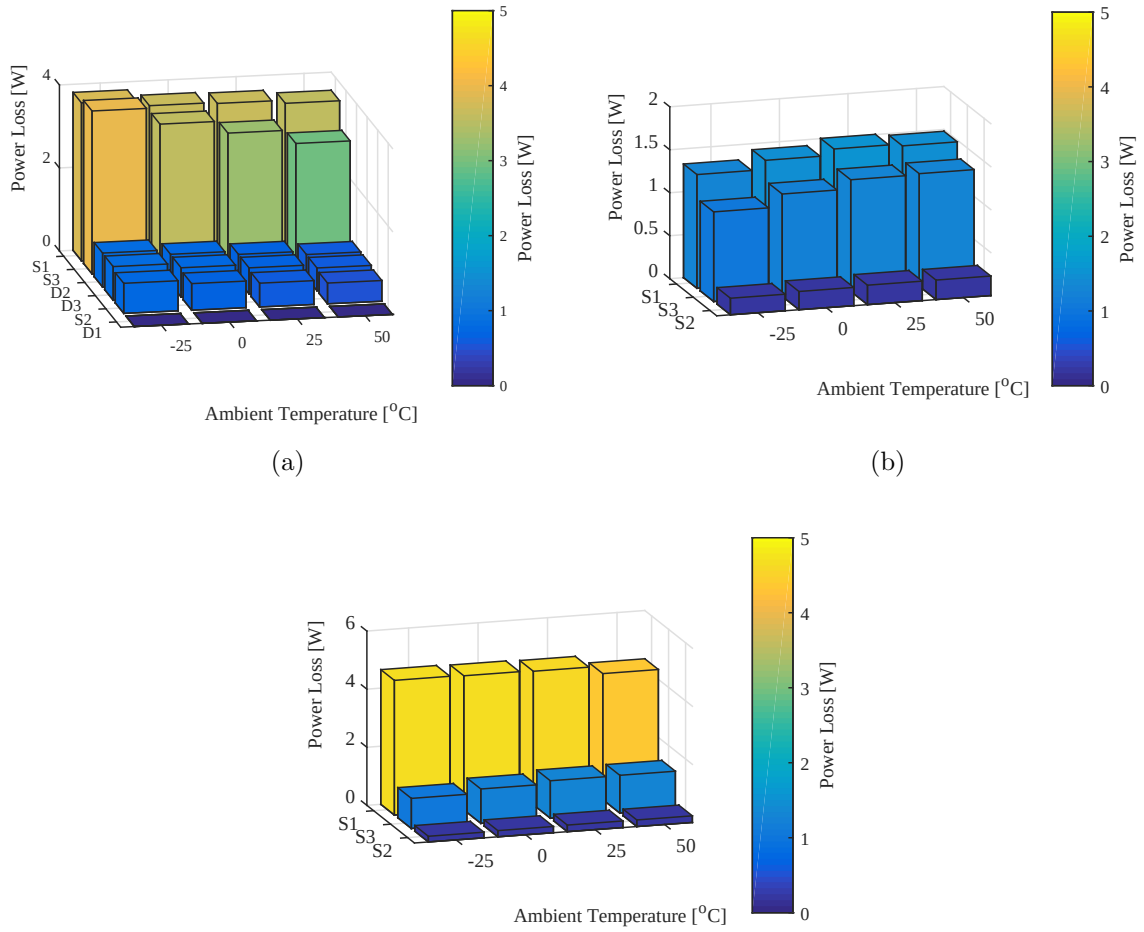
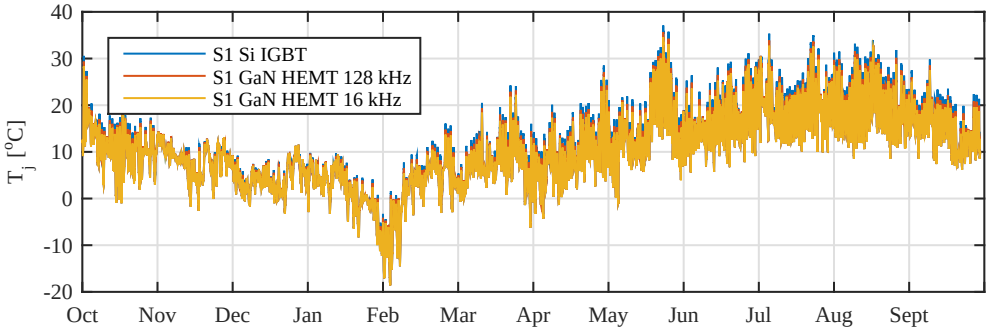


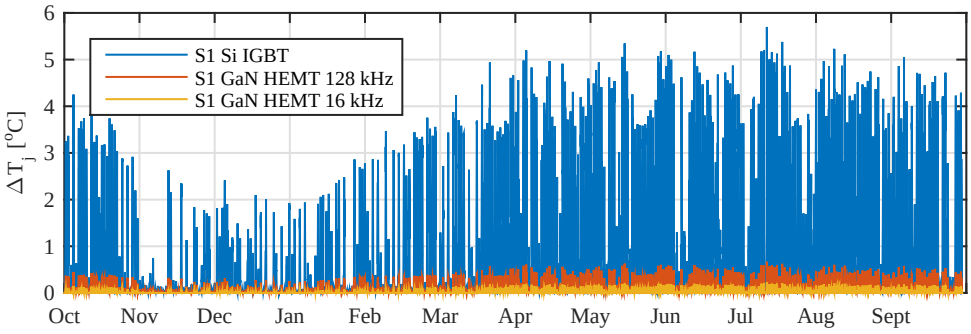
Figure 5.32: Loss distribution of the ANPC inverter based on: (a) Si IGBT technology with a switching frequency of 16 kHz, (b) GaN technology with a switching frequency of 16 kHz, and (c) GaN technology with a switching frequency of 300 kHz, where different ambient temperatures with the maximum solar irradiance level are considered.

As the devices with highest power losses and therefore the thermal stress in each configuration are identified, further thermal performance analysis can be conducted on these devices based on the annual mission profile. Mean junction temperature (T_j) and junction temperature variation (ΔT_j) for devices with the highest thermal stress are presented in Fig. 5.33a and 5.33b, respectively. The mean junction temperature of S_1 in a Si IGBT based inverter is the highest among three configurations, while the mean junction temperature of S_1 in the GaN HEMT based inverter with 16 kHz switching frequency is lowest. The mean junction temperature is affected by the ambient temperature, shown in Fig. 5.27. The mean junction temperature follows the ambient temperature trend throughout the year and can show significant variations based on the solar irradiance and ambient temperature. Regarding the junction temperature variations, S_1 in a Si IGBT based inverter with 16 kHz has the highest temperature variation across the junction of the device. On the other hand, the junction temperature variation across S_1 in a GaN HEMT based inverter at 16 kHz and 128 kHz is very small during winter, and has a similar performance during warm months to that of S1 in a Si IGBT inverter due to the increased conduction losses. It should be noted that the light loading of the inverter throughout the year, due to solar irradiance profile in Fig. 5.27 lead to low junction temperature variations.

It can be seen from Fig. 5.33 that the long term mean junction temperature and junction temperature fluctuations are irregular profiles with varying frequencies and amplitudes. In order to make the results more meaningful, cycling counting methods can be applied to the mean junction temperature and junction temperature variation data. The number of cycles at each temperature level is dependent to mission profile, thermal and electrical models as it is explained in the previous sections. Rainflow is one of the cycle-counting methods to identify full and half cycles within irregular profiles, and is chosen in this study. It has been used in calculation of lifetime of power modules based on device solder temperature profiles [118]. The histograms of mean junction temperature (T_j) and junction temperature variations (ΔT_j) are presented for the most stressed devices are presented in Fig. 5.34a and 5.34b, respectively. Replacing Si IGBTs with GaN HEMTs at 16 kHz switching frequency reduces the number of cycles of at higher mean junction temperatures. On the other hand, the



(a)

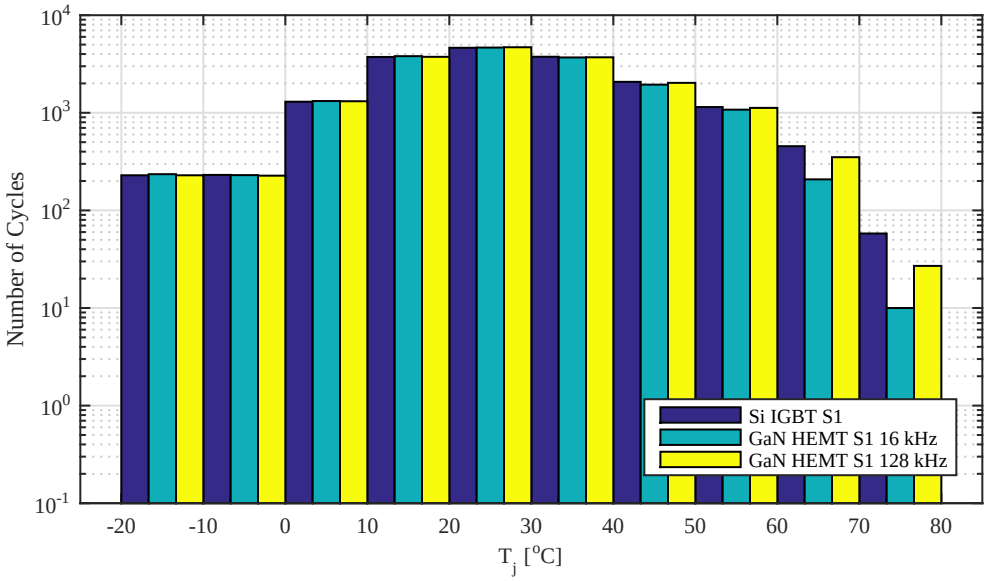


(b)

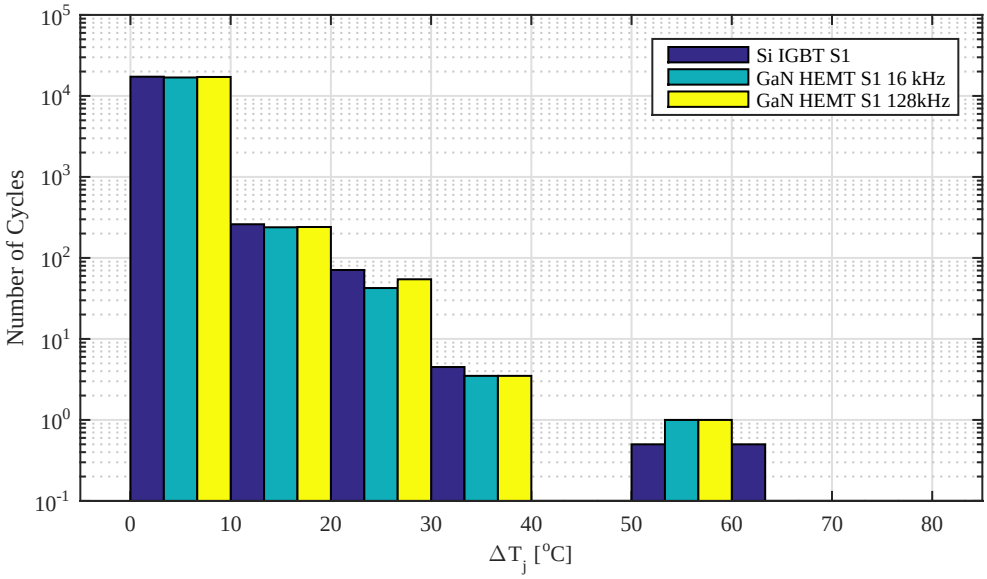
Figure 5.33: Thermal loading profiles for the most stressed devices in 3L-ANPC inverter through a year: (a) mean junction temperature and (b) junction temperature variation.

GaN HEMTs with 128 kHz switching frequency have increased T_j in comparison to GaN HEMT at 16 kHz and Si IGBT. In terms of ΔT_j, at higher temperatures, the number of cycles is higher at 20 °C but the number of cycles at higher temperatures is still lower than Si IGBT.

The Coffin-Manson model for conventional power modules indicates that number of failures in a power module is only dependent on the temperature cycles, cycle amplitude ΔT_j and mean junction temperature T_j [119]. Therefore, with adequate device packaging models for the GaN HEMTs and Si IGBTs, lifetime consumption of the power devices at different switching frequencies can be calculated and then an optimisation between reliability, efficiency and system volume can be achieved. Despite the fact that the lifetime of the devices is not calculated in this work, it is clear that GaN HEMT based inverter has lower thermal stress in comparison to Si IGBT based inverter. Although the replacement of Si with GaN does not bring significant energy savings to the user with given grid tariff, it can bring system level savings from heat sink and output filter, and reduced thermal stress.



(a)



(b)

Figure 5.34: Rainflow counting results for the thermal loading profiles shown in Fig. 5.33 under a yearly mission profile: (a) mean junction temperature and (b) cycle amplitude.

5.5 Conclusions

In this chapter, the impact of GaN HEMT to a PV inverter in terms of power loss, converter efficiency, heat sink and output filter volume, and thermal stress based on a mission profile is discussed. It is shown that the GaN HEMT has excellent switching and conduction performance under different load and heat sink temperature conditions that results in very high efficiency and low power cell loss. Therefore, the combined heat sink and output filter volume can be reduced by increasing the heat sink temperature from 50 °C to 80 °C and increasing the switching frequency from 16 kHz to 64 kHz, without compromising the efficiency of the system. In addition to this, the mission-profile based analysis of the inverter with real field annual solar data from Aalborg, Denmark showed that GaN HEMT based system has significantly lower thermal stress in comparison to Si IGBT based system at both low and high switching frequency conditions. Although the replacement of Si IGBT with GaN HEMT in the system does not bring significant operational income due to low grid tariff and operating conditions (solar irradiance and loading of the system throughout the year), it brings lower junction temperature variation and reduced mean temperature across most stress device throughout the year. Regarding the power semiconductor devices cost and impact on overall cost of the system, the reduction in device cost for WBG devices has taken place over the last few years and the final cost will be to a large extent decided by market acceptance (i.e, volume of sales).

Chapter 6

WBG in Higher Power Applications

The evaluation and benchmarking of WBG devices in Chapters 4 and 5 showed that conduction performance and switching performance of devices at 600 V blocking class provide excellent performance under wide output load, switching frequency and heat sink temperature conditions at residential scale applications. The analysis of GaN HEMT based inverter in Chapter 5 showed that heat sink and output filter volume reduction is possible with WBG based power cell design by operating at higher heat sink temperature and switching frequency conditions without compromising power semiconductor performance. Due to these reasons, specifically SiC MOSFETs are considered to be excellent solution for high power ($>$ 1 MW) applications due to higher thermal conductivity of SiC in comparison to Si and GaN. Higher thermal conductivity allows higher power dissipation for same temperature difference between junction and case, or lower temperature difference between junction and case for same power dissipation. At high power applications such as marine, drive or drilling applications, multilevel topologies are preferred due to lower output voltage harmonics, lower voltage stress across power semiconductor devices and reduced filtering requirements. Various applications of SiC MOSFETs have been presented in literature for

high power, high voltage applications [120], [121]. In this chapter, a new five-level hybrid inverter, which is suitable for WBG based applications with high efficiency, is presented. The chapter starts with the review of five-level multilevel topologies, with special focus on hybrid topologies. Then, the details of the proposed topology including derivation of the topology, available switching states and commutation scheme are presented in Section 6.2. The simulation results including efficiency comparison with respect to state-of-the-art hybrid topology 5L-ANPC is presented in Section 6.3. Finally, the experimental results based on 12 kW prototype are presented in Section 6.4 and discussed.

6.1 Review of Five-Level Inverter Topologies

Multilevel inverters have been discussed in literature as good candidates for high power conversion systems ($>$ 1 MW), such as marine propulsion systems, variable speed drives and HVDC systems, due to improved output voltage distortion, reduced voltage stress across power semiconductors and reduced filtering requirements [122], [123]. The first multilevel converter designs were based on neutral point clamped (NPC) and flying capacitor (FC) oriented topologies. These two approaches have been proposed for three and higher number of voltage levels. At high number of voltage levels (five and more), NPC based inverters suffer from high semiconductor count, high conduction losses and asymmetrical semiconductor switching loss. On the other hand, FC based topologies require complex control schemes for balancing flying capacitors and high energy storage in floating capacitors [122], [124]. Due to the limitations of NPC and FC based topologies for high number voltage levels (five and above), various hybrid topologies have been introduced [125]. The aim of hybrid topologies is minimisation of number devices and energy storage while maximising number of output voltage levels and maintaining high efficiency.

One of the most popular hybrid topologies is five-level active neutral point clamped (ANPC) inverter that has been discussed and analysed in depth in the previous

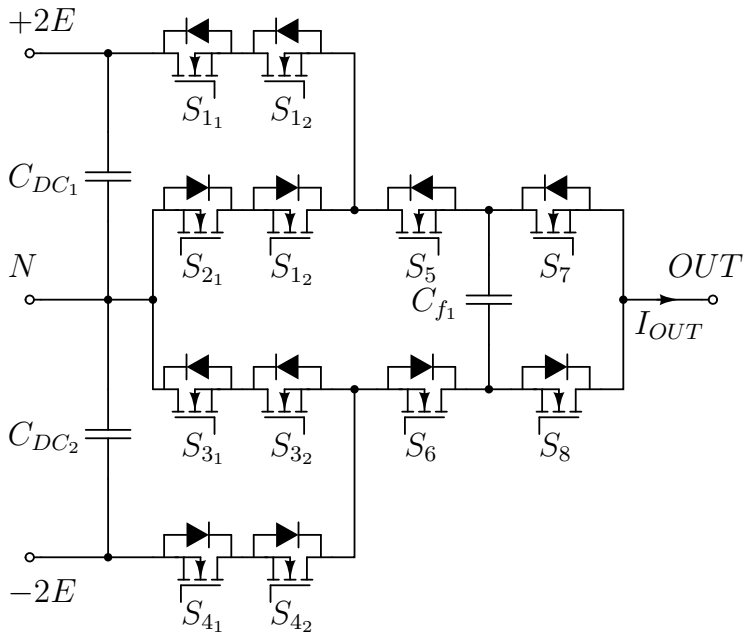


Figure 6.1: 5L-ANPC inverter.

chapters of this thesis. The analysed three-level ANPC topology is extended to five-level ANPC (5L-ANPC) in [126, 127, 128] and presented in Fig. 6.1. 5L-ANPC is formed by 12 active switches and a floating capacitor C_{f_1}, where C_{f_1} voltage is fixed to E. By using the floating capacitor and neutral point, five voltage levels (+2E, +E, 0, -E, -2E) can be achieved between the output (OUT) and neutral point (N). Similar hybrid five-level topology based on two floating capacitors $C_{f_{1-2}}$ and 14 active switches has been introduced in literature [129]. The topology is presented in Fig. 6.2. The floating capacitor voltages are kept at one fourth of DC link voltage and the inductor L_{f_1} is used for limiting inrush current between DC link capacitors and floating capacitors due to voltage variation across floating capacitors. Another hybrid multilevel inverter concept called "Stacked Multicell Converter" (SMC) is discussed in [130], [131]. The concept is based on increasing number of voltage levels at the output of the converter by introducing floating capacitor and active switch based cells. Five-level inverter based on SMC approach is presented in Fig. 6.3. In all three inverters presented in Fig. 6.1, 6.2 and 6.3, active devices are rated at one fourth of DC link voltage E.

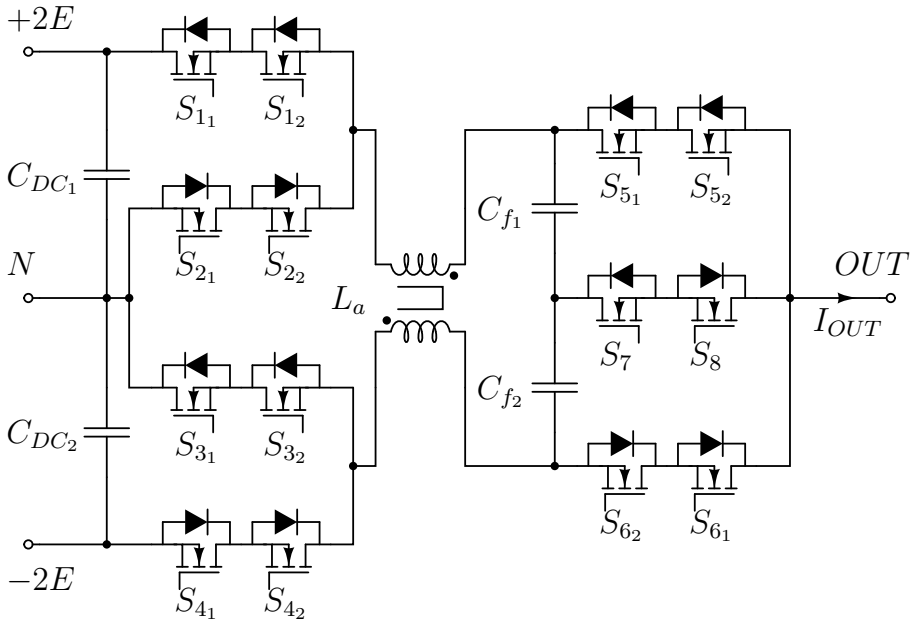


Figure 6.2: FUJI five-level inverter.

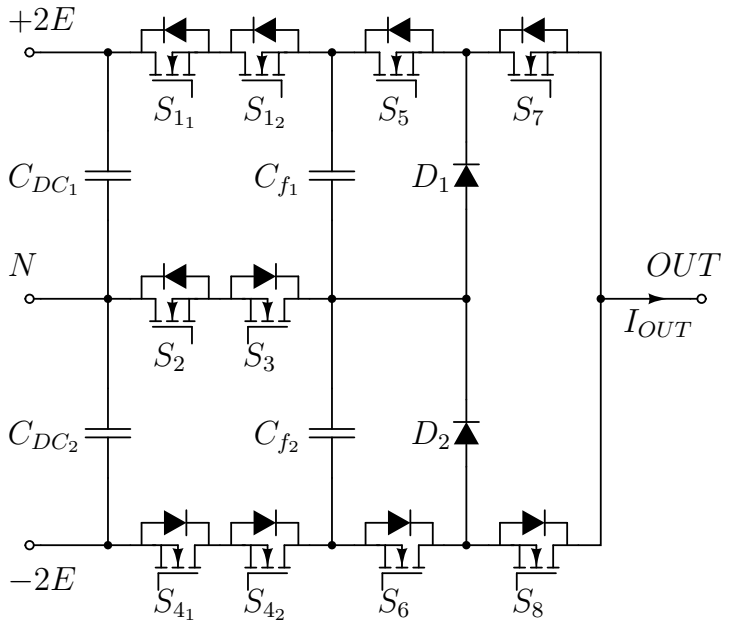


Figure 6.3: Five-level stacked multicell inverter.

6.2 Proposed Inverter Topology

The static characterisation results of SiC MOSFET and GaN HEMT in Figs. 4.4 and 4.5 in Chapter 4 show that the on-state characteristic of WBG devices have positive temperature dependency. Positive temperature dependency provides the opportunity for conduction of devices in parallel with equal current sharing. The benefit of parallel conduction of WBG devices have been presented in Chapter 5 where high efficiency in ANPC topology is presented with parallel conduction of GaN HEMTs at zero states. In addition to this, the loss breakdown of power cell in Fig. 5.10 clearly indicates that the conduction losses dominate the power cell loss in a WBG based inverter up to high switching frequencies (64 kHz in this case). Therefore it is beneficial to reduce the conduction losses in WBG based high power multilevel topologies where switching frequency is usually low due to high power output and increased number of output voltage levels. The presented five-level topologies in the previous section do not utilise parallel conduction of devices due to their nature and the motivation in this work is to utilise low switching loss performance of WBG devices in multilevel topologies while reducing the conduction losses.

The proposed five-level inverter topology is based on a hybrid configuration of neutral-point-clamp and floating capacitors. The topology is named as "Efficient and Dense Architecture: EDA5" and filed for patent application [132]. The topology is formed by 16 active switches S_1-S_{10}, two floating capacitors $C_{f_{1-2}}$ and two DC-link capacitors $C_{DC_{1-2}}$. The schematic of EDA5 is presented in Fig. 6.4. Each switch in the converter is rated at E, one-fourth of the total DC link voltage $4E$. The charge state of floating capacitors $C_{f_{1-2}}$ is controlled by utilizing redundant states in order to keep capacitor voltages at E for five-level voltage waveform ($2E$, E, 0, $-E$ and $-2E$) between output of the converter (OUT) and neutral point (N) of input DC-link capacitors $C_{DC_{1-2}}$.

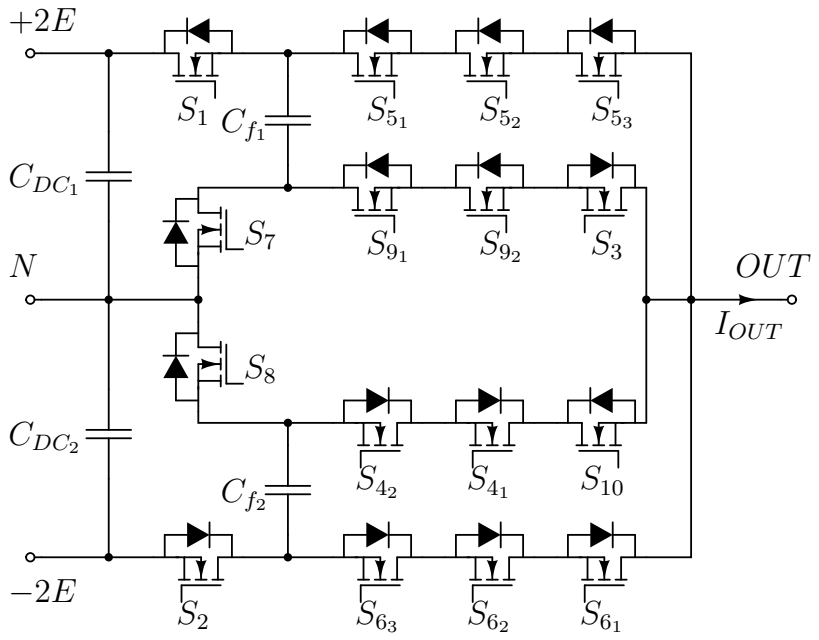


Figure 6.4: Proposed five-level inverter topology: EDA5

6.2.1 Switching States

The switching states of the converter are presented in Table 6.1. Series connected switches such as S_{X_1} and S_{X_2} are switched on and off simultaneously, and therefore are represented as a single switch S_X in the switching state table. Single state is available for $+2E$ and $-2E$ output voltage levels while two states are available for $+E$ and $-E$ output voltage levels and three states are available for zero output state. The two switching states for $+E$ and $-E$ levels are achieved by introducing floating capacitors to the path of output current I_{OUT}. Depending on the polarity of output current and voltage, the floating capacitors are charged or discharged. In Table 6.1, the switching states E_C and E_D define the charging and discharging states respectively for floating capacitors at unity power factor operation and inverter mode. For zero output voltage, three possible paths can be used: 1) upper path 0_P formed by S_3, S_7 and S_9, 2) lower path 0_N formed by S_4, S_8 and S_{10}, 3) parallel path 0_X formed by simultaneous conduction of upper path 0_P and lower path 0_N. The main benefit of parallel zero state path 0_X is the reduction of conduction losses in the

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
$+2E$	1	0	0	0	1	0	0	0	0	0
$+E_C$	1	0	1	0	0	0	0	0	1	0
$+E_D$	0	0	0	0	1	0	1	0	0	0
0_P	0	0	1	0	0	0	1	0	1	0
0_N	0	0	0	1	0	0	0	1	0	1
0_X	0	0	1	1	0	0	1	1	1	1
$-E_D$	0	0	0	0	0	1	0	1	0	0
$-E_C$	0	1	0	1	0	0	0	0	0	1
$-2E$	0	1	0	0	0	1	0	0	0	0

Table 6.1: Switching States

power cell during low modulation indexes or higher DC link voltages, where zero state conduction is dominant.

The current paths for four different switching states during positive half of output voltage for inverter mode are presented in Fig. 6.5. It can be seen from Figs. 6.4 and 6.5 that four devices are in conduction during all switching states except zero state 0_X where the output current is divided into two zero state branches. Charge or discharge state can be selected during $+E$ and $-E$ states in order to fix the floating capacitor voltage to the half of DC link capacitor voltage. For example, during unity power factor operation for inverter mode, at $+E_C$ state, switches S_1, S_3 and S_9 are turned-on in order to apply $+E$ state to the output by subtracting floating capacitor voltage E from DC link capacitor voltage $+2E$ while charging the floating capacitor. During $+E_D$ state, the voltage across floating capacitor is applied to the output of the converter by turning-on S_5 and S_7 switches. The "*charging*" or "*discharging*" status of a switching state can be defined by polarity of output voltage and direction of output current.

6.2.2 Commutation Scheme

The commutation procedure between switching states, which are presented in Table 6.1, has to be determined for transition of continuous output current from one state to

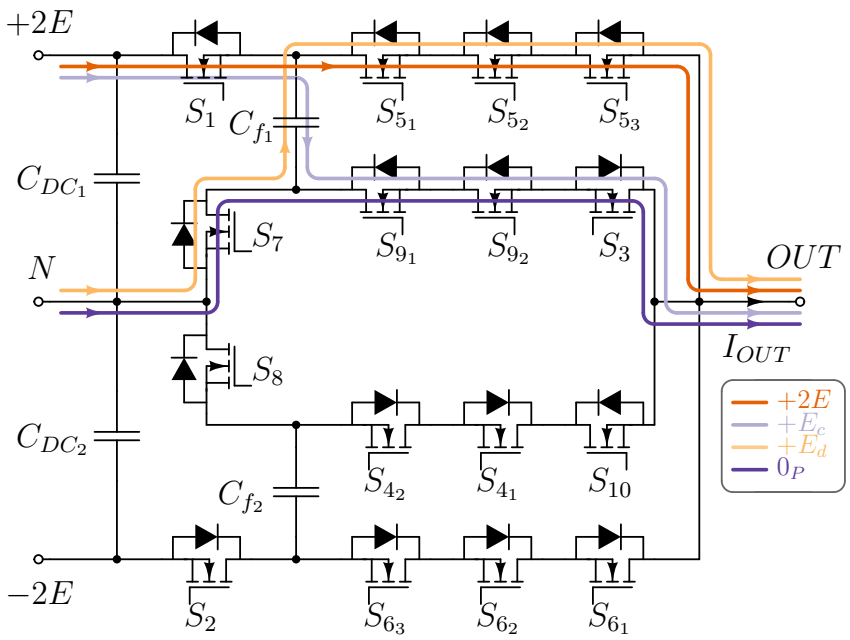
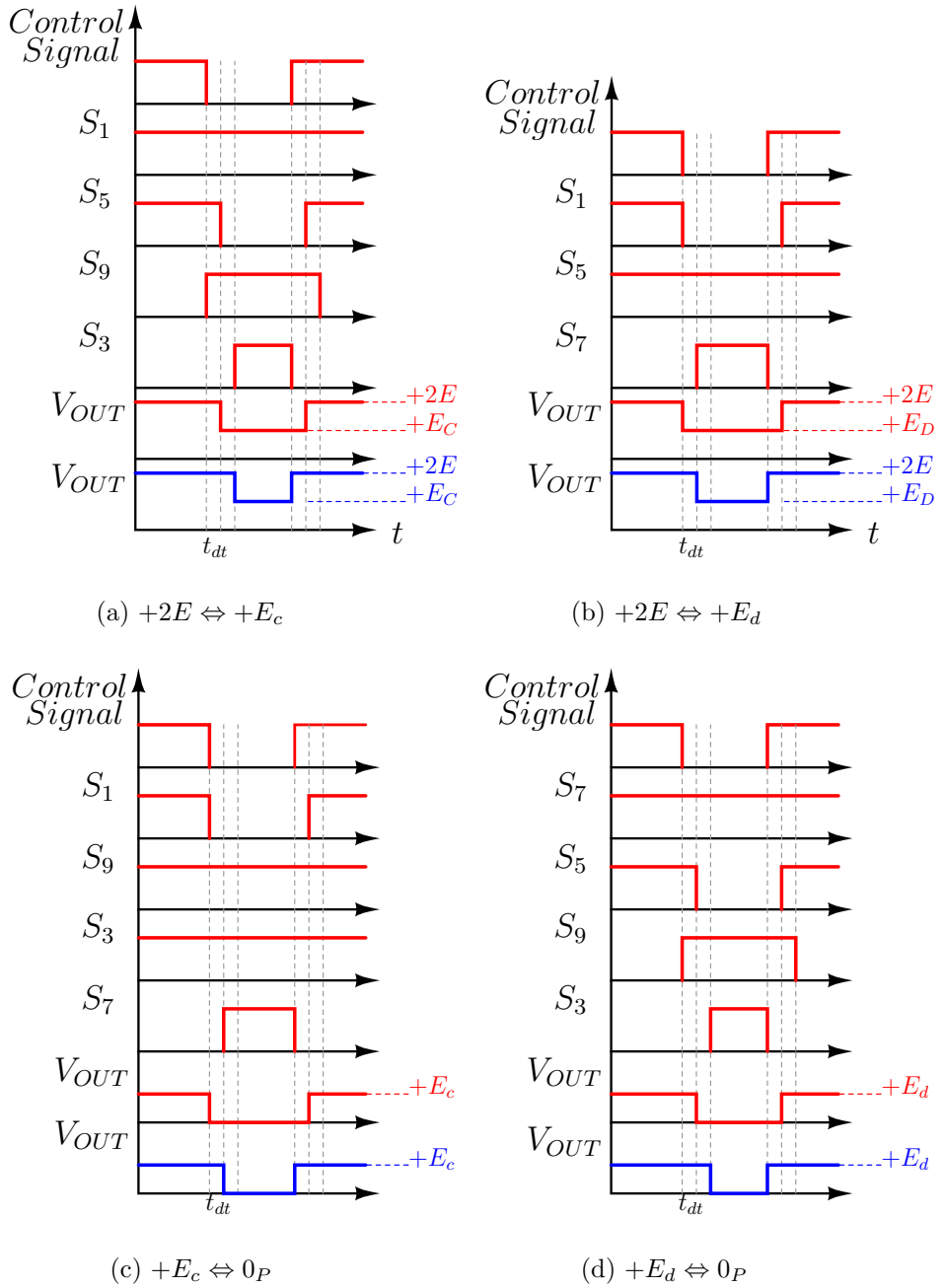


Figure 6.5: Current paths for $+2E$, $+E_C$, $+E_D$ and 0_P states during positive half of output voltage.

another. The possible commutation schemes for the positive half of the output voltage for positive and negative output current are presented in Fig. 6.6. The blue and red curves for V_{OUT} represents output voltage with positive and negative output currents respectively. Due to the nature of the topology, suitable commutations can be realised between $+2E$ and $+E_{C-D}$ or $+E_{C-D}$ and 0_P states. The commutation between $+E_C$ and $+E_D$ is not possible without clamping the output to another voltage state. In the first commutation scenario from $+2E$ to $+E_C$ in Fig. 6.6 (a), $S9$ switch is turned-on first, and after the dead-time period t_{dt}, S_5 is switched-off and finally S_3 switch is turned-on. Depending on the direction of output current, the output voltage changes from $+2E$ to $+E_C$ state after t_{dt} or $2t_{dt}$. Commutation schemes in Fig. 6.6 (b), (c) and (d) have similar structure with Fig. 6.6 (a), and all of the schemes can be realised by applying logic gates to PWM signals coming from the controller. With WBG devices, the antiparallel diodes can be eliminated and reverse condcution capability can be utilised to reduce the component count without compromising system efficiency.



(a) $+2E \Leftrightarrow +E_c$

(b) $+2E \Leftrightarrow +E_d$

(c) $+E_c \Leftrightarrow 0_P$

(d) $+E_d \Leftrightarrow 0_P$

Figure 6.6: Commutation schemes for the positive half of the output voltage.

6.3 Simulation Results

The proposed topology is simulated in PLECS at inverter mode for evaluation of functionality and efficiency comparison with 5L-ANPC topology. The simulation conditions and converter parameters are presented in Table 6.2. Medium voltage drive systems have been considered as the case study for the evaluation of the topology. Higher power and DC link voltage have been chosen to show the functionality and suitability for these systems. Due to limited current rating of WBG devices at 600 V and below blocking class, commercial 650 V, 70 A SiC MOSFET with trench structure from ROHM has been used in order to achieve 1 kV DC link voltage with 12 kW output power [133]. Switching and conduction losses of switches at various operating conditions are calculated based on datasheet parameters at 60 °C junction temperature. Switching frequency is fixed to 10 kHz, and RL load with fixed 1.5 mH filter inductance is used to achieve continuous load current. The output voltage and current waveforms at 7 kW output power are presented in Fig. 6.7. Modulation index is set to 0.72. It is proven that the converter can achieve five-level output waveform successfully by controlling floating capacitor voltages.

Under same operating conditions, floating capacitor voltages for C_{f_1} and C_{f_2} capacitors are presented in Fig. 6.4. The floating capacitor voltages are controlled by individual charge/discharge controllers for each capacitor where main DC link and floating capacitor voltages are measured and compared. Schematic of the imple-

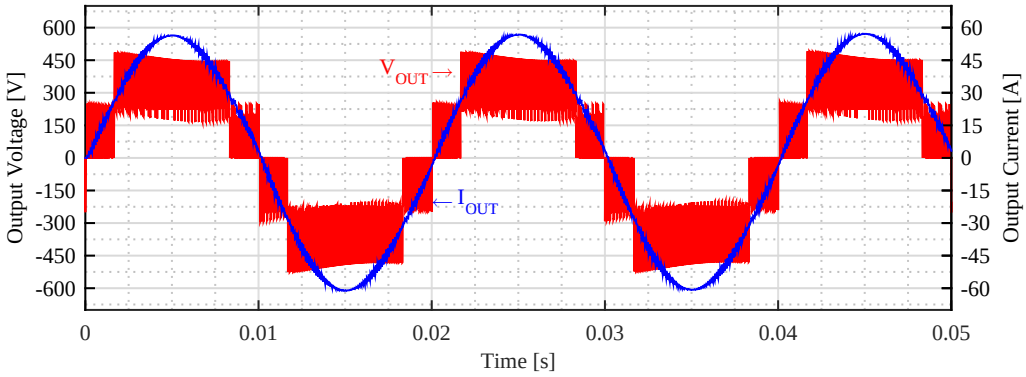


Figure 6.7: Simulated output voltage and current waveforms.

Table 6.2: Simulation and Converter Parameters

Parameter	Symbol	Value
Input Voltage	V_{DC}	1 kV
Output Power	P_{OUT}	12 kW
Output Inductor	L_f	1.5 mH
Output Voltage	V_{OUT}	1.5 kV
Switching Frequency	f_{sw}	10 kHz
Switching Device	S_{1-10}	SiC MOSFET 650 V, 70 A SCT3030AL
Junction Temperature	T_j	60 °C
Total Floating Capacitance	C_f	200 μF

mented control system is presented in Fig. 6.8. Each floating capacitor $C_{f_{1-2}}$ is charged or discharged depending on whether the voltage across the floating capacitor is higher than half of the corresponding DC link capacitor $C_{DC_{1-2}}$. Floating capacitor voltages with respect to DC link capacitor voltages are presented in Fig. 6.9. It can be seen that the capacitor voltages are exceeding limits excessively at certain time of operation. The reason for that is the floating voltage controller is forcing the output control signal, which determines charge or discharge state for each capacitor, to be changed during $2E$, 0 or opposite half of output signal with respect to each floating capacitor by using the OR gate and DQ flip-flop presented in Fig. 6.8. As it is mentioned in commutation scheme section, the commutation of output current cannot happen between charging and discharging states and this approach prevents commutation between these two E states. The state of charge of each floating capacitor is dependent on load current and switching frequency. Therefore, the control of floating capacitor voltage with the implemented controller can be improved by increasing switching frequency and increase of capacitance for same load conditions. It can also be seen from Fig. 6.9 that the main DC link capacitors have 50 Hz ripple at steady state. The low frequency voltage variation in NPC based topologies is investigated in the literature, specifically for three phase systems and DC link voltage control can also be implemented to overcome this problem [134].

In order to evaluate efficiency performance of proposed topology, 5L-ANPC is simu-

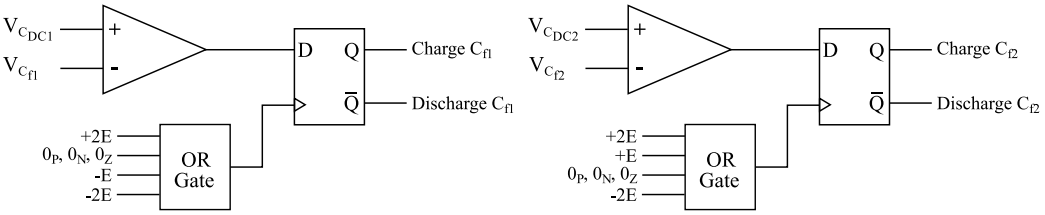


Figure 6.8: Floating capacitor voltage control scheme used in simulation and experimental validation.

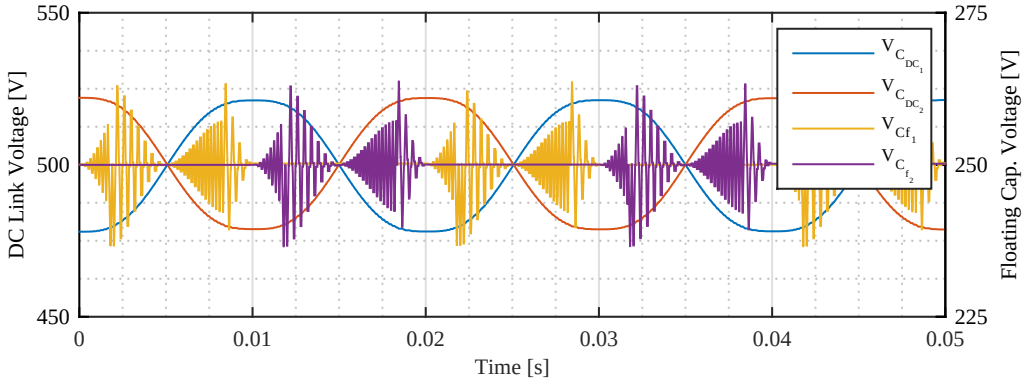


Figure 6.9: Simulated C_{f_1} and C_{f_2} floating capacitor voltages.

lated under same operating conditions in Table 6.2. Two operation scenarios for the converters are considered: 1) Voltage controlled mode operation where modulation index is fixed and output current is varied, 2) Current controlled mode where output current is fixed and modulation index is varied. The efficiency results of single phase power cells for voltage source and current source operation are presented in Figs. 6.10 and 6.11 respectively. The results in Fig. 6.10 for voltage source operation show that proposed topology has approximately the same efficiency with 5L-ANPC under wide load range. As presented in Fig. 6.11, during current source operation, the performance gap between proposed topology and 5L-ANPC is increased at light load conditions due to reduced conduction and switching losses at lower modulation index.

The power cell losses for both operation modes have been analysed and presented in Figs. 6.12 and 6.13 for voltage source and current source operation respectively. With voltage source mode, the switching and conduction losses increase linearly and exponentially with respect to output power for both topologies. Although the con-

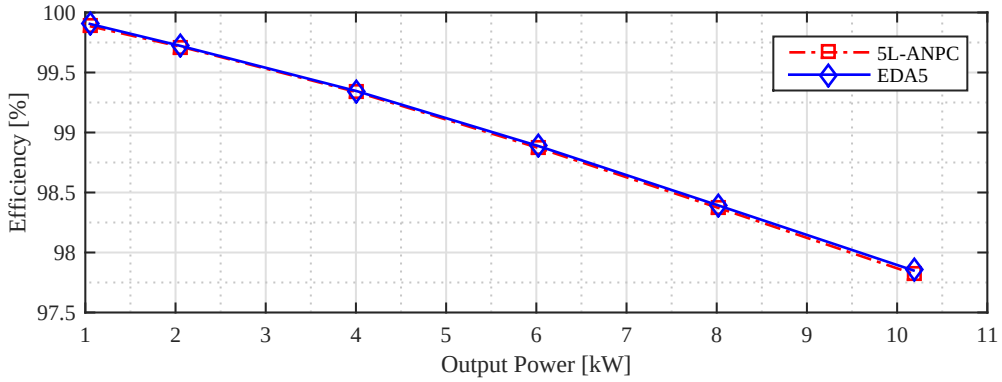


Figure 6.10: Efficiency comparison with voltage controlled mode operation.

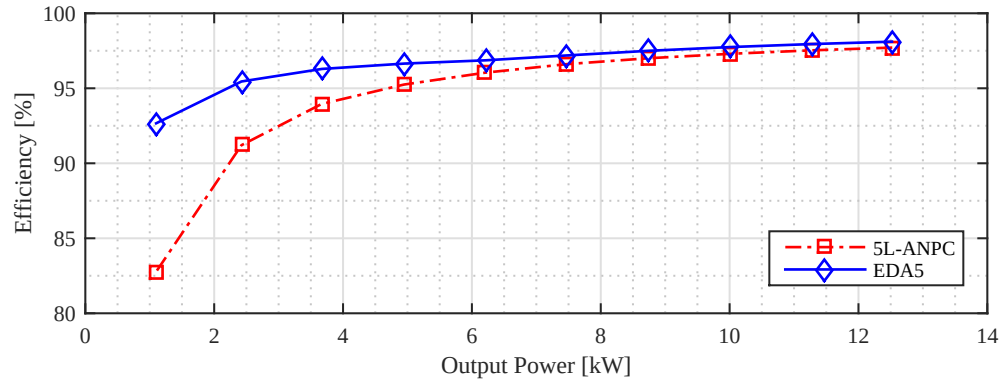


Figure 6.11: Efficiency comparison with current controlled mode operation.

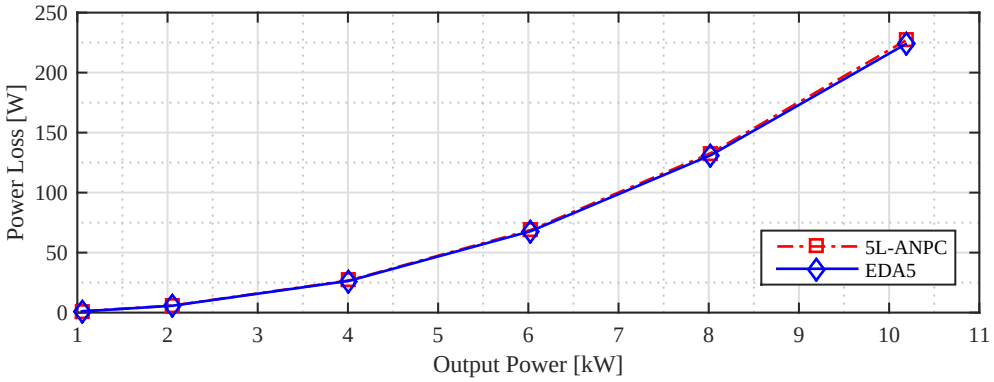


Figure 6.12: Power cell loss comparison with voltage controlled mode operation.

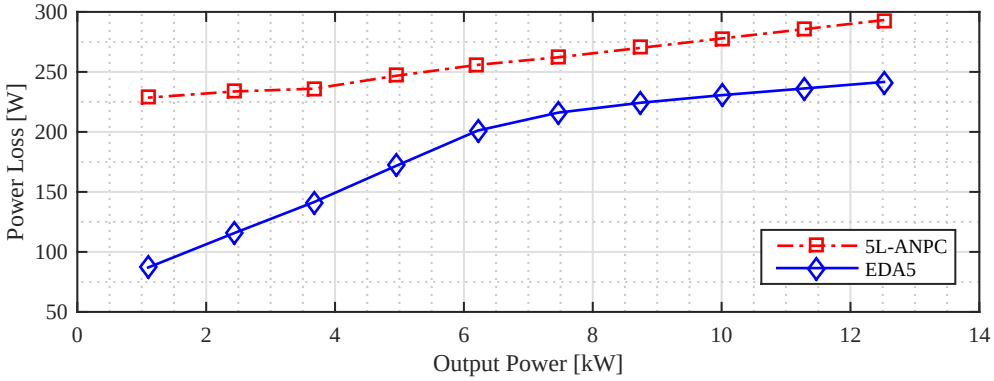


Figure 6.13: Power cell loss comparison with current controlled mode operation.

duction losses are similar, the proposed topology has better switching performance in comparison to 5L-ANPC. The difference between switching losses is the reason for the efficiency difference between two topologies shown in Fig. 6.10. In current source mode, the proposed topology has a significant advantage over 5L-ANPC under light load conditions due to reduced conduction and switching losses. This shows that proposed topology can operate with higher efficiency at higher DC link voltage and lower modulation index conditions.

Table 6.3: Prototype Parameters

Parameter	Symbol	Value
Input Voltage	V_{DC}	1 kV
Output Power	P_{OUT}	12 kW
Switching Frequency	f_{sw}	10 kHz
Switching Device	S_{1-10}	ROHM SiC MOSFET 600 V, 70 A SCT3030AL
Output Filter Inductor	L_f	1.5 mH

6.4 Experimental Results

Experimental validation of the proposed hybrid inverter topology is completed by a 12 kW single phase prototype. The prototype test parameters are presented in Table 6.3 and photo of the prototype can be seen in Fig. 6.14. The system can be extended to three phase by stacking single phase building blocks. Single phase building block consist of DC link film capacitors, floating capacitors, DC link and floating capacitor voltage sensors, gate drivers, switches and turn-off snubbers. DC link voltage sensors are used to control the floating capacitor voltage by charge/discharge control implemented in DSP+FPGA control platform. Discrete SiC MOSFETs without anti-parallel diodes are implemented with RC snubbers in order to achieve dynamic and static voltage sharing between series connected MOSFETs presented in Fig. 6.4. Power plane is formed by 6-layer PCB with 140 μm copper on each layer for minimum parasitic inductance between commutating switches and minimum conduction losses.

The voltage sharing across the devices S_1, S_{5_1}, S_{5_2} and S_{5_3} at 1 kV DC link voltage is presented in Fig. 6.15. It can be seen that each devices is subject to 300 V including the voltage overshoots due to parasitics and the voltage sharing among the devices is successful.

The inverter output voltage and current waveforms at 7 kW output power conditions are presented in Fig 6.16. The experimental results show that proposed topology successfully operates with an inductive load up to 7 kW output power. At 7 kW

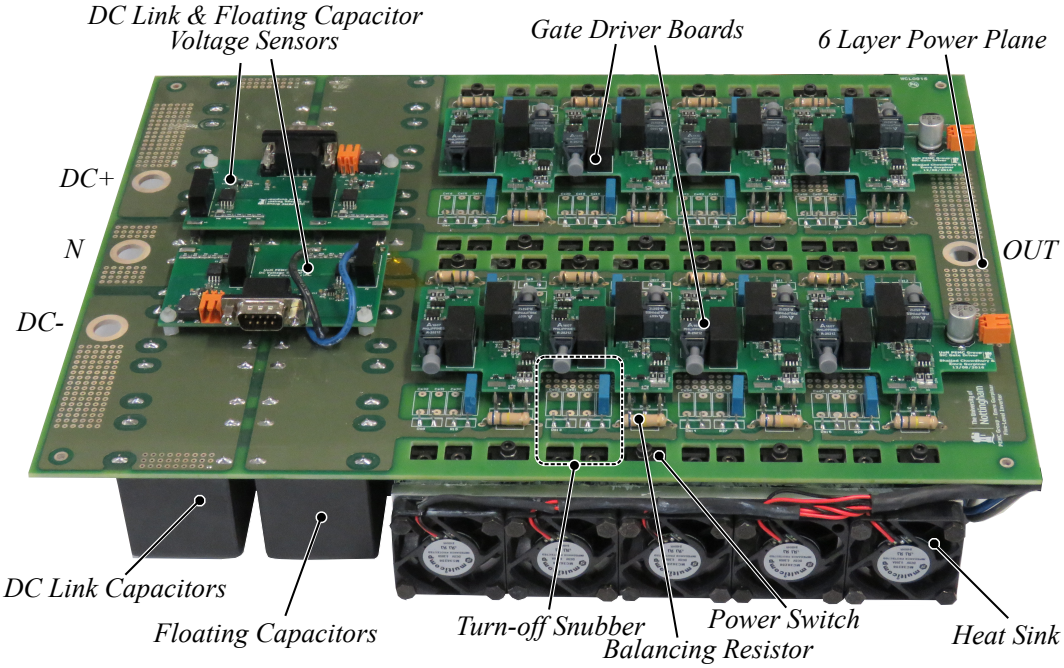


Figure 6.14: Single phase 12 kW prototype of proposed five-level hybrid topology: EDA5.

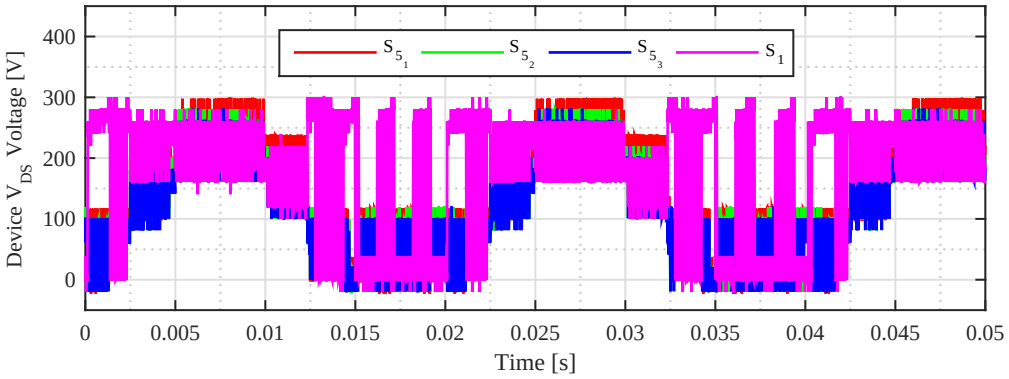


Figure 6.15: Voltage across S_1, S_{5_1}, S_{5_2} and S_{5_3} at 1 kV DC link voltage.

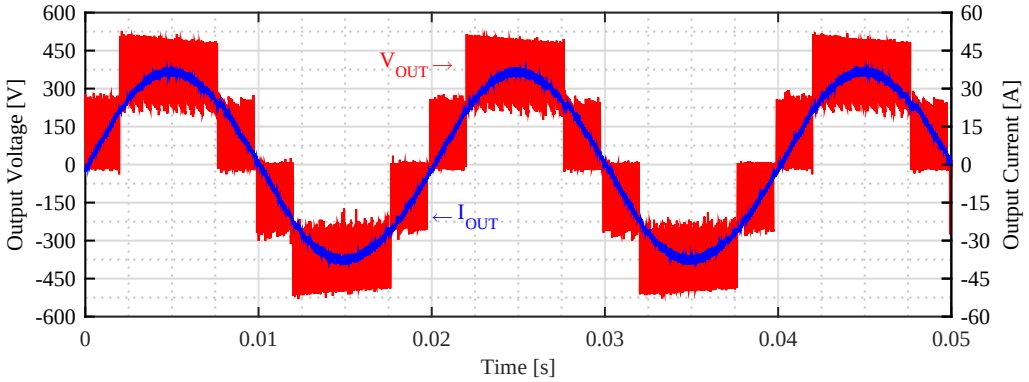


Figure 6.16: Experimental output voltage and current waveforms at 7 kW output power.

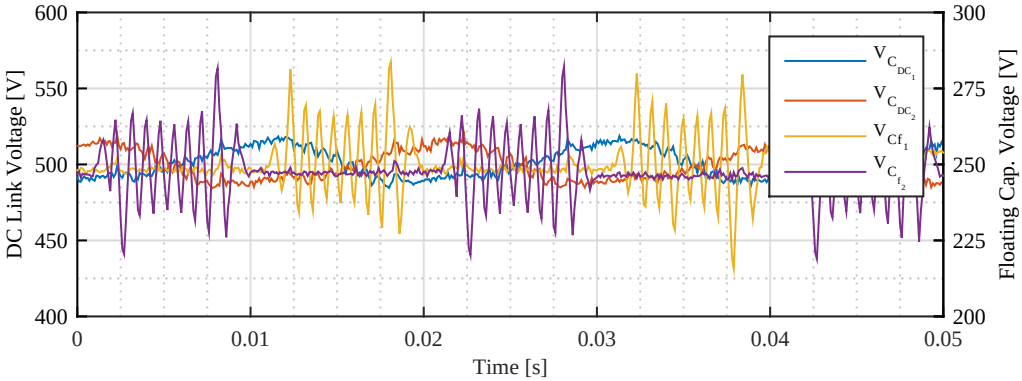


Figure 6.17: DC link and floating capacitor voltages at 7 kW output power.

output power, it can be seen that output current is distorted slightly due to voltage variation across floating capacitors C_{f_1} and C_{f_2}. The floating capacitor voltage with respect to DC link capacitor voltage is presented in Fig 6.17 at 7 kW output power condition. Although the average voltage of floating capacitor is fixed to half of DC link capacitor voltage 250 V for both load conditions, the peak-to-peak voltage variation across floating capacitor is increased to with the increase of output current. The reason for the large variation at high output power is the sensor accuracy and limitations of control board. Due to control board limitations (sample, hold and processing delays), the update rate for floating capacitor control is limited to 1 kHz and the effect of low update frequency makes voltage fluctuation more severe at higher output current conditions. This can be solved by implementing the capacitor voltage control in the FPGA rather than DSP.

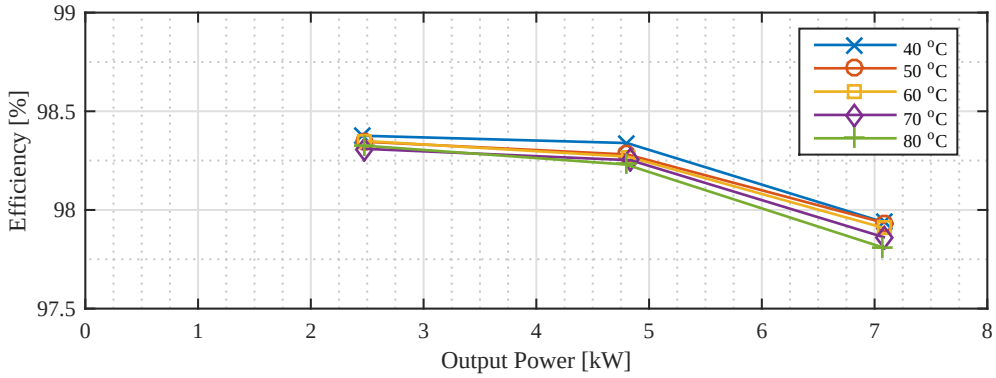


Figure 6.18: Efficiency of the prototype at 1 kV DC link voltage and 0.8 modulation index.

Finally, efficiency figure of the prototype power cell at 1 kV DC link voltage, 0.8 modulation index and different heat sink temperatures is presented in Fig. 6.18. The power cell efficiency curve includes DC link capacitor and power switch losses; and total efficiency curve includes power cell losses and output inductor losses. It can be seen that the prototype power cell can achieve 98.38 % peak efficiency with SiC MOSFETs. The main objective of the prototype is demonstration of the functionality of EDA5 topology at high voltage and high power conditions. The efficiency of the prototype can be further improved by optimising RC snubbers to minimise switching loss.

6.5 Conclusion

In this chapter, a novel five-level hybrid inverter topology for renewable energy systems and high power applications has been presented including description switching states and commutation scheme. The proposed topology is compared with state-of-the-art hybrid multilevel topologies in simulation. Simulation results show that EDA5 provides higher efficiency in comparison to 5L-ANPC, especially at lighter load conditions. The functionality of the topology has been verified experimentally with a 12 kW single phase prototype.

Chapter 7

Conclusion and Future Works

7.1 Conclusion

The demand for low carbon economy and limited fossil resources for energy generation drive the research on renewable energy sources and the key technology for utilisation of renewable energy sources: power electronics. Innovative inverter topologies and emerging WBG based semiconductor devices at 600 V blocking class are the enabling technologies for more efficient, reliable and accessible renewable energy sources for electricity generation.

This thesis has investigated the state-of-the-art inverter topologies and WBG devices at 600 V blocking class for residential scale PV systems. The review of the inverter topologies and current status of PV systems were presented in Chapter 2. The WBG material properties and state-of-the-art WBG devices were discussed in Chapter 3. The benchmarking of WBG devices including static and dynamic characterisation, gate drive requirements and performance evaluation in T-Type inverter were presented in Chapter 4. The benchmarking of devices has shown that GaN HEMT has excellent switching and conduction properties at low current conditions with negligible temperature dependency, but a relatively higher complex gate driver design is

required for safe operation and the design has a strong impact on switching losses. The performance results of WBG devices in T-Type inverter shows that SiC and GaN devices provide performance enhancement over Si under wide load, temperature and switching frequency conditions. In terms of switching performance, GaN HEMT has the best performance among three technologies and allows high efficiency at high-frequency applications. Performance evaluation of three device technologies show that WBG devices, specifically GaN HEMT provide robust performance under wide temperature, switching frequency conditions.

The impact of GaN HEMT to a PV inverter in terms of power loss, converter efficiency, heat sink and output filter volume, and thermal stress based on a mission profile was discussed in Chapter 5. The switching and conduction performance of GaN HEMT under different load and heat sink temperature conditions resulted in very high efficiency and low power cell loss. It was shown that combined heat sink and output filter volume can be reduced by increasing the heat sink temperature from 50 ^{o}C to 80 ^{o}C, and increasing the switching frequency from 16 kHz to 64 kHz, without compromising the efficiency of the system. The mission-profile based analysis of the GaN HEMT based inverter showed that GaN HEMT based system has significantly lower thermal stress in comparison to Si IGBT based system at both low and high switching frequency conditions. The reduced thermal stress brought lower junction temperature variation and reduced mean temperature across most stress device throughout the year.

In Chapter 6, a novel five-level hybrid inverter topology for renewable energy systems and high power applications based on SiC MOSFET was presented. The proposed topology was compared with state-of-the-art hybrid multilevel topologies in simulation. Simulation results showed that proposed topology provides higher efficiency in comparison to 5L-ANPC, especially at lighter load conditions. The functionality of the topology was verified experimentally with 650 V SiC MOSFETs in a 12 kW single phase prototype under different load and heat sink temperature conditions.

7.2 Future Works

There are a few points which can be investigated further:

- The recently introduced GaN devices in low inductance packages from GaN Systems and Infineon can be included to the benchmarking of WBG devices. These devices were not available at the time of this research project but should be considered as the competitors of the evaluated devices in this thesis. The semiconductor manufacturing and packaging technology is constantly evolving with introduction of WBG materials and the emerging devices to the market come with their own challenges (e.g. cooling, design of PCB layout, gate circuitry) and benefits (e.g. better static and dynamic performance, improved reliability).

- The GaN HEMT based optimisation based in Chapter 5 is based on conventional output inductor design and naturally cooled heat sink. The optimisation can be extended further with planar inductors, which have higher power density and performance at higher switching frequencies, and forced cooled heat sink designs to maximise the volume reduction.

- EMI filter design is an important aspect of high switching frequency inverters and EMI filter volume can be a significant portion of the total inverter volume. Therefore EMI filter should be considered in the final volume optimisation.

- Loss balancing techniques can be applied to GaN HEMT based ANPC inverter in order to reduce the thermal stress across S_1 and S_6 switches, and therefore improve the reliability of the system.

- This thesis has taken into account hard switching topologies for WBG devices. The results with GaN HEMT showed that the switching losses dominate the overall power loss beyond 100 kHz. The switching frequency of the power cell can be pushed beyond 160 kHz with soft switching topologies where the contribution of switching losses to the overall power cell loss can be minimised.

- The dynamic and static voltage balancing across series connected SiC MOSFETs in Chapter 6 was achieved with RC snubbers. The balancing can be also achieved with gate drive circuitries, which are introduced for Si IGBTs to eliminate the use of RC snubbers.

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Appendix A

Performance Benchmark in H6 Inverter

The second inverter that is used to evaluate the device performance is H6, presented in Section 2.2.1.4. H6 is a member of full-bridge inverter family and provides high efficiency as a transformerless PV inverter topology and requires 6 active devices where S_1 to S_4 are used to form a full-bridge inverter, and S_5 and S_6 are used to decouple the grid from PV panel at zero states for minimisation of CM current. In this study, Si IGBT, SiC MOSFET and GaN HEMT has been used in all devices $S_1 - S_6$ to evaluate the performance of the converter under different test conditions and assess the benefits of WBG devices in full-bridge based topologies. Same as the analysis in T-Type inverter, the study starts with description of the test setup, followed by the efficiency performance under different load and heat sink temperature conditions and concluded with the loss breakdown at 40 kHz with three different devices.

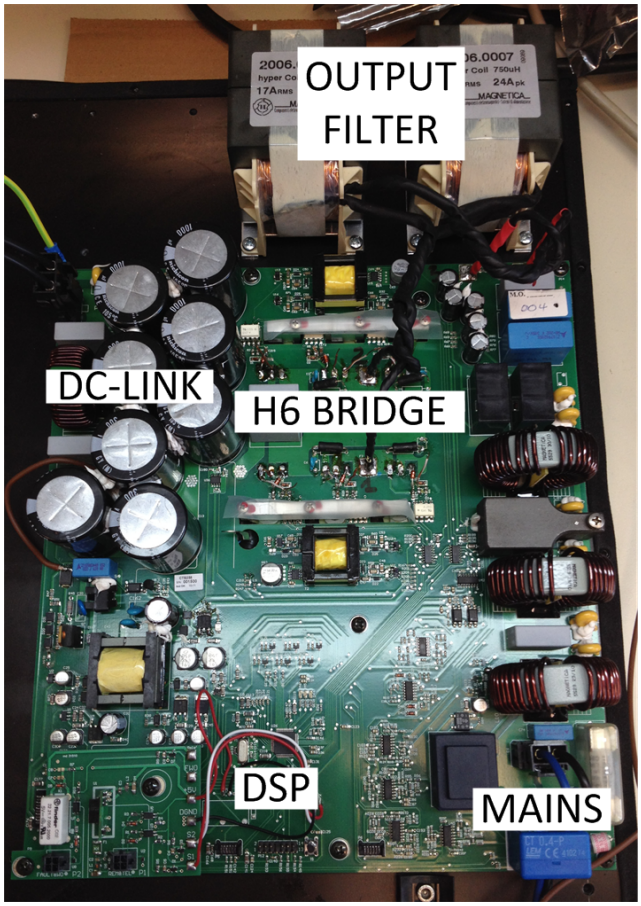
A.0.1 Test Setup

A commercial converter [135] in Fig. A.1a embedding the H6 bridge with UniTL PWM modulation is used to evaluate the performance of the 650 V SiC MOSFET

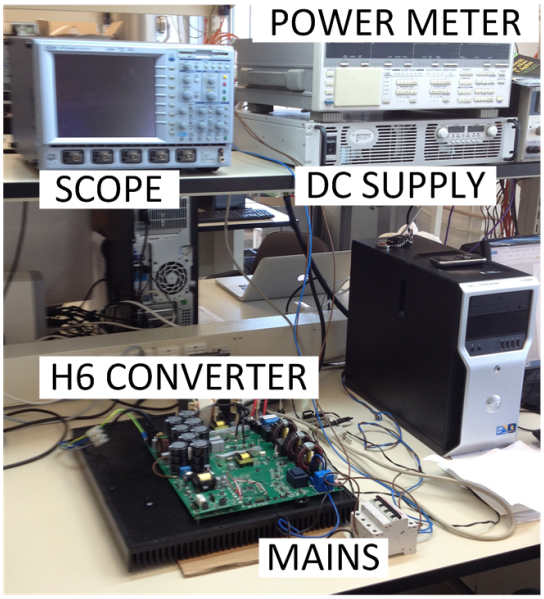
Parameter	Value
P_{MAX}	1.5 kW
V_{DC}	400 V
V_{OUT}	230 V
L_f	750 μH each
C_f	5 μF
C_{DC}	1.5 mF
f_{sw}	10 to 40 kHz
Si IGBT *Deadtime*	1 μs
SiC MOSFET *Deadtime*	250 ns
GaN HEMT *Deadtime*	266 ns
$S_1 - S_6$	ST STGW35HF60WD ROHM SCT2120AF Panasonic PGA26A10DS
T_h	60 to 100 °C

Table A.1: Converter Parameters and Test Conditions

and 600 V GaN HEMT devices in comparison to 600 V Si IGBTs. This converter features a Freescale MC56F8323 DSP for grid connected control of the converter. The output LC filter is composed of two inductors $L_f = 750$ μH and a $C_f = 5$ μF capacitor. The converter parameters are presented in Table A.1. The experimental setup is shown in Fig. A.1b, corresponding to the schematic of Fig. 2.13, where converter is powered through a controlled DC power supply. The schematic of test setup is presented in Fig. A.2. Same in T-Type test, power analyser is used to extract power cell losses which correspond to semiconductor losses in the system. The isolated gate drives provide 0-18 V gate signal for SiC devices and 0-15 V for Si IGBTs. Input DC link voltage of the converter is fixed to 400 V and output grid voltage is 230 V_{rms} with 50 Hz grid frequency. In order to decouple the device case temperature from the load, a full controllable heat sink is used where the temperature of the heat sink can be controlled independently from the load by cooling fans and heating resistors.



(a)



(b)

Figure A.1: Single phase H6 inverter: (a) prototype and (b) test bed.

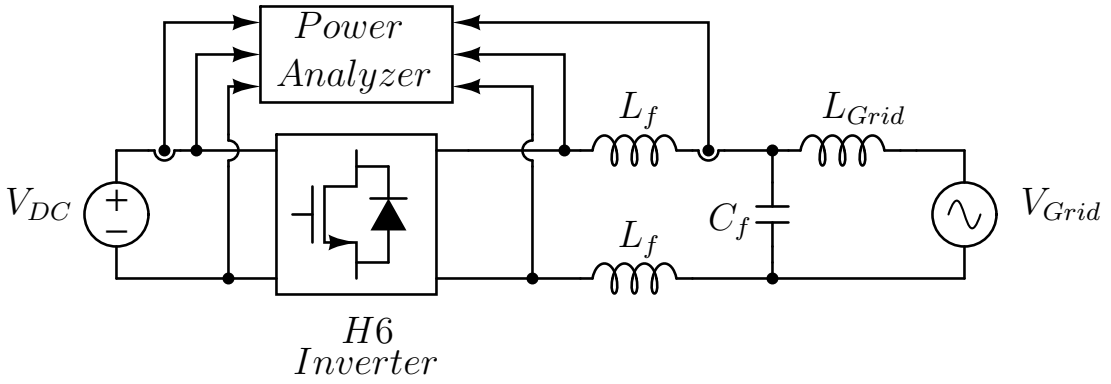


Figure A.2: Test setup for H6 inverter.

A.0.2 Experimental Results

A.0.2.1 Efficiency Performance

The efficiency of the converter is assessed with three semiconductor technologies: Si IGBT, SiC MOSFET and GaN HEMT. During the assessment, heat sink, switching frequency and output load are varied for evaluation of device performance under different conditions independent from each other. The Si and SiC and GaN based configurations are tested up to 1.5 kW input power. Total converter efficiency including relay, auxiliary power supply and filter losses; and power cell efficiency which includes only DC link and semiconductor losses at 60 °C heat sink temperature for Si, SiC and GaN devices are presented in Fig. A.3 for 10, 20 and 40 kHz switching frequencies.

The total efficiency results for Si, SiC and GaN based configurations in Fig. A.3a show that SiC and GaN based configurations have up to 1 % higher efficiency in comparison to Si based configuration. The efficiency gap between Si and wide-bandgap devices increases as the switching frequency is increased from 10 kHz to 20 kHz and 40 kHz, especially at higher load conditions. At 40 kHz and 1 kW output power, GaN and SiC based H6 inverters achieved 96.5 % total efficiency where Si based H6 inverter has 95.4 % total efficiency. From Fig. A.3, the total efficiency difference between

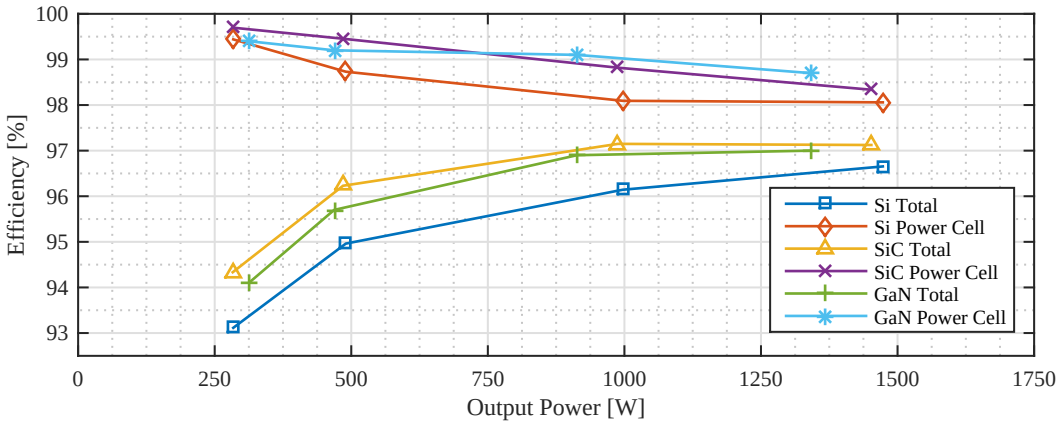
wide-bandgap based inverters and Si based inverter is due to superior performance of power cell with GaN HEMT and SiC MOSFET in comparison to Si IGBT. GaN and SiC devices provide 98.5 % power cell efficiency at 40 kHz, 1 kW output power where Si based power cell can reach 97.2 % power cell efficiency.

The performance of the devices at different switching frequencies and heat sink temperatures are presented in Fig. A.4 and A.5. Fig A.4 shows the comparison of Si, SiC and GaN solutions up to 40 kHz switching frequency and between 60 °C and 100 °C heat sink temperatures at 1.5 kW output power. The results show that GaN solution proves a robust performance with power cell efficiency higher than 98 % under different temperature and switching frequency conditions. SiC based solution provides more than 97.8% efficiency under different temperature and switching frequency conditions. Both solutions provide robust performance with respect to increased switching frequency. On the other hand, in Fig. A.4a, it can be seen that increased switching frequency and ambient temperature has significant impact on inverter performance with Si IGBTs. Fig. A.5 shows a similar efficiency comparison versus heat sink temperature at 10, 20 and 40 kHz switching frequencies at 1.5 kW output power for three different device technologies. It is clear that SiC and GaN device show good performance under different ambient temperatures due to wide-bandgap device properties discussed in Chapter 3.

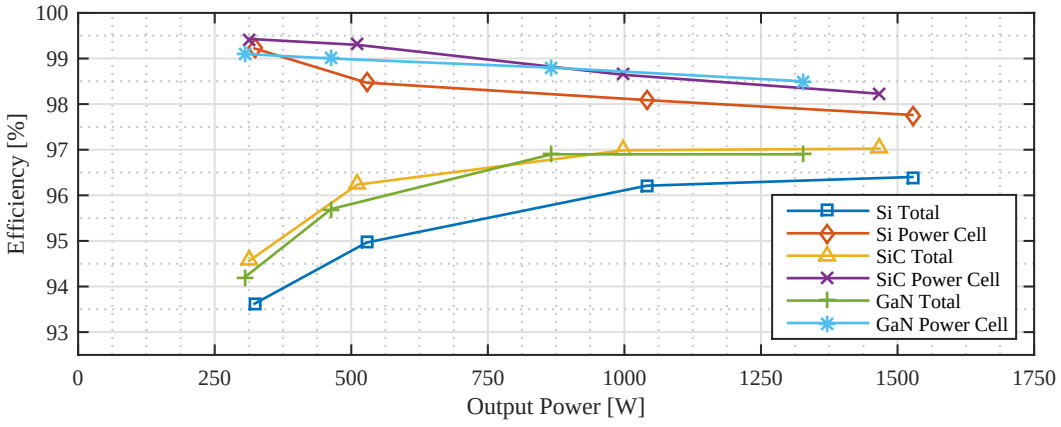
A.0.2.2 Switching Performance

Based on the power cell efficiency curves presented in previous section, the breakdown of semiconductor losses in terms of switching and conduction can be conducted on the inverter with respect to different heat sink temperature conductions. The conduction loss of each switch in H6 inverter with respect to modulation index M and the load angle θ are can be calculated based on active and zero state conduction equations for bipolar and unipolar devices:

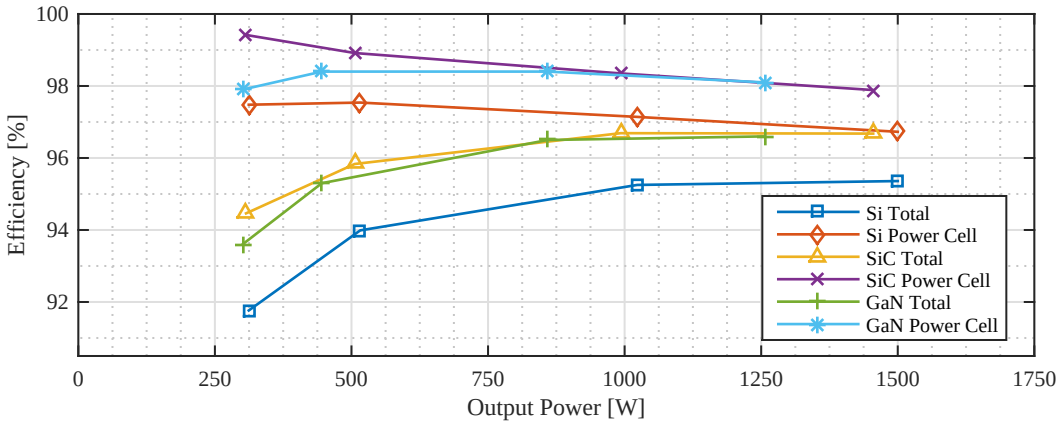
$$P_{c-act_{bp}} = I_m \cdot V_f \cdot \frac{M}{4} \cdot cos(\theta) + \frac{I_m^2 \cdot R_{ce} \cdot M}{2\pi} \cdot (1 + cos(2\theta)) \tag{A.1}$$



(a)

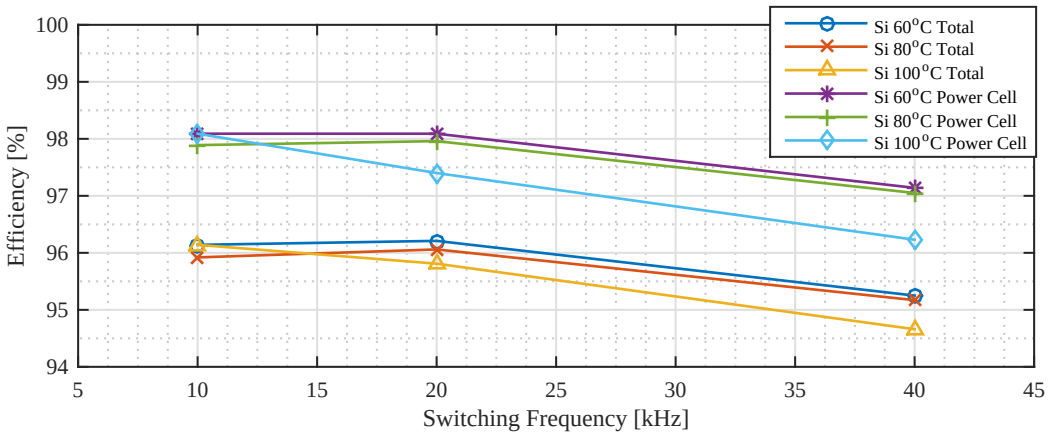


(b)

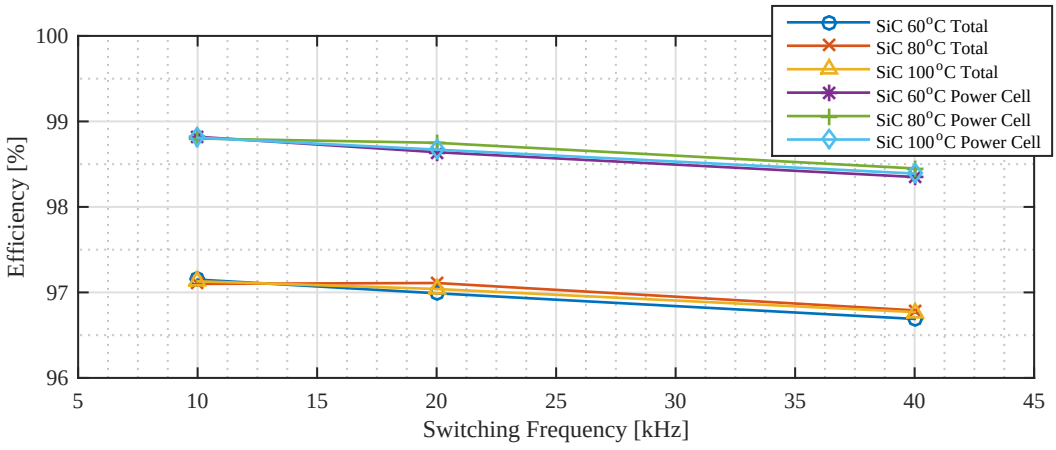


(c)

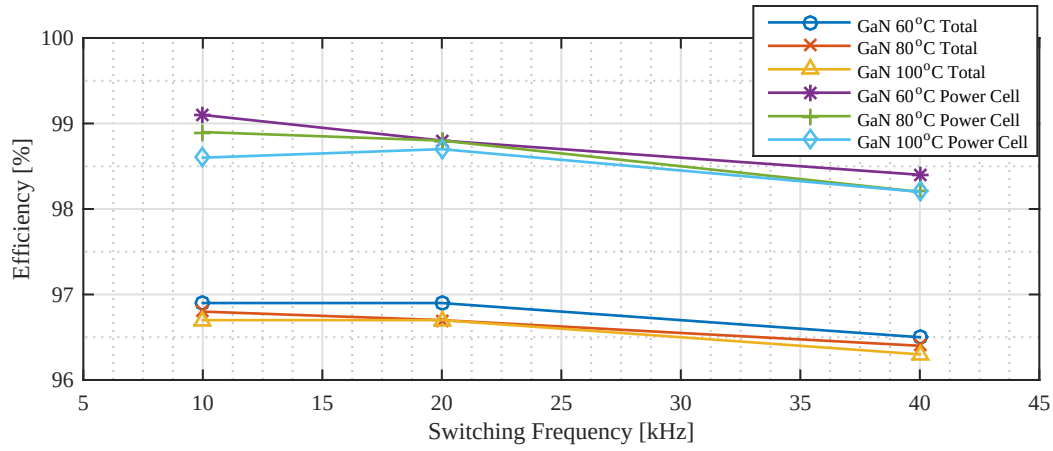
Figure A.3: Efficiency comparison at: (a) 10 kHz, (b) 20 kHz and (c) 40 kHz switching frequencies at 60 ^{o}C heatsink temperature.



(a)

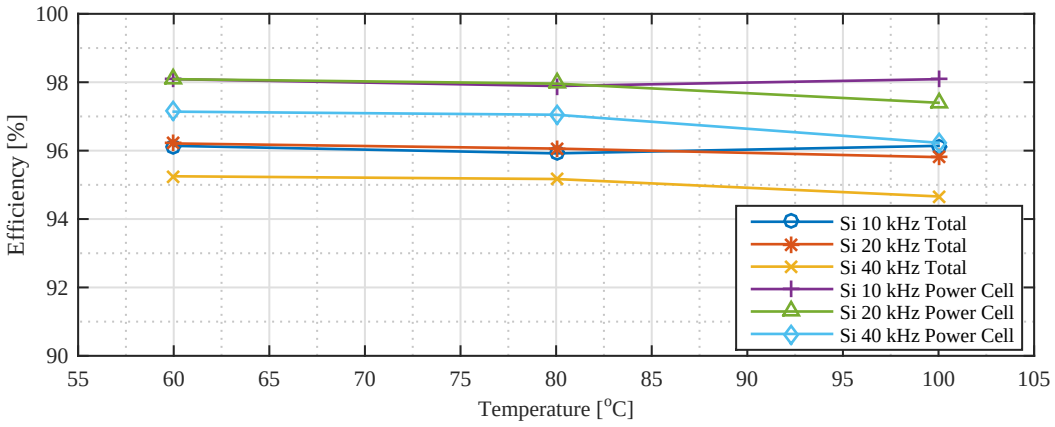


(b)

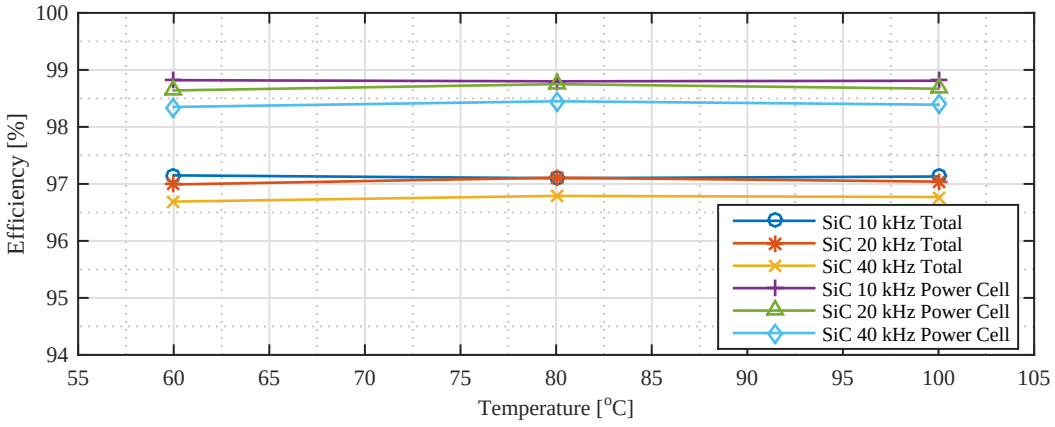


(c)

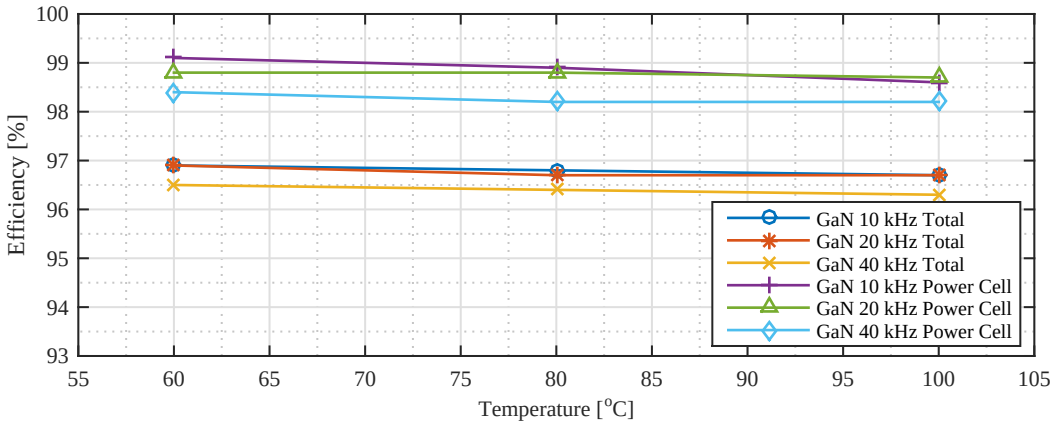
Figure A.4: Efficiency comparison of (a) Si IGBT, (b) SiC MOSFET and (c) GaN HEMT based H6 inverter at 1 kW output power and different switching frequencies.



(a)



(b)



(c)

Figure A.5: Efficiency comparison of (a) Si IGBT, (b) SiC MOSFET and (c) GaN HEMT based H6 inverter at 1.5 kW output power and different heatsink temperatures.

$$P_{c-zero_{bp}} = I_m \cdot V_f \cdot (\frac{1}{\pi} - \frac{M}{4} \cdot cos(\theta)) + I_m^2 \cdot R_{ce} \cdot \left(\frac{1}{4} - \frac{M \cdot \left(1 + \frac{1}{3} \cdot cos(2\theta)\right)}{2\pi} \right) \quad \text{(A.2)}$$

$$P_{c-act_{up}} = \frac{I_m^2 \cdot R_{ds} \cdot M}{2\pi} \cdot (1 + cos(2\theta)) \quad \text{(A.3)}$$

$$P_{c-zero_{up}} = I_m^2 \cdot R_{ds} \cdot \left(\frac{1}{4} - \frac{M \cdot \left(1 + \frac{1}{3} \cdot cos(2\theta)\right)}{2\pi} \right) \quad \text{(A.4)}$$

where I_m is peak value of output current, M is modulation index and θ is load angle, which can be approximated as 0 for grid connected single phase PV inveters. For SiC MOSFET and GaN HEMT based configurations where reverse conduction capability of devices is utilised, the conduction losses for the devices are:

$$P_{c-S_{5,6}} = 2 \cdot P_{c-act_{up}} \quad \text{(A.5)}$$

$$P_{c-S_{1,2,3,4}} = P_{c-act_{up}} + P_{c-zero_{up}} \quad \text{(A.6)}$$

Therefore, total conduction losses in H6 inverter based on WBG devices can calculated as:

$$P_{c-total_{up}} = 4 \cdot P_{c-S_{1,2,3,4}} + 2 \cdot P_{c-S_{5,6}} \quad \text{(A.7)}$$

For Si IGBT based configuration, the conduction losses for the devices are:

$$P_{c-S_{5,6}} = 2 \cdot P_{c-act_{bp}} \quad \text{(A.8)}$$

$$P_{c-S_{1,2}} = P_{c-act_{bp}} + P_{c-zero_{bp}} \quad \text{(A.9)}$$

$$P_{c-S_{3,4}} = P_{c-act_{bp}} \quad \text{(A.10)}$$

$$P_{c-D_{3,4}} = P_{c-zero_{bp}} \quad \text{(A.11)}$$

The total conduction loss for Si IGBT based H6 inverter can be calculated as:

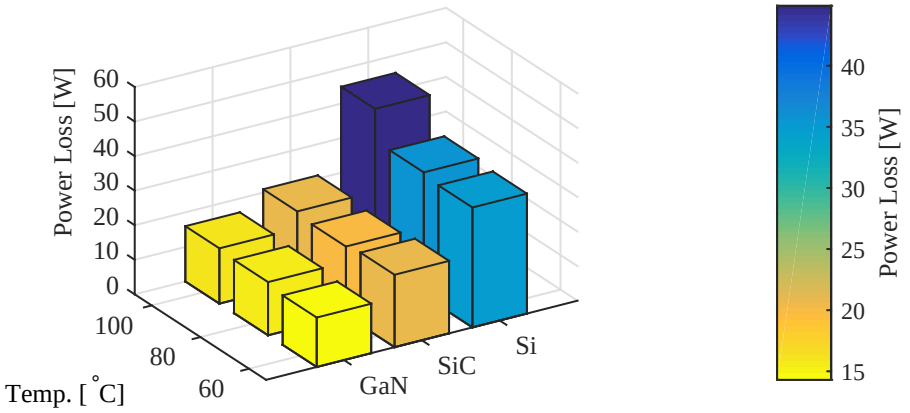
$$P_{c-total_{bp}} = 2 \cdot P_{c-S_{1,2}} + 2 \cdot P_{c-S_{3,4}} + 2 \cdot P_{c-D_{3,4}} + 2 \cdot P_{c-S_{5,6}} \quad \text{(A.12)}$$

The on-state parameters of the devices such as on-state resistance R_{ds}, R_{ce} or R_{ak} and threshold voltage V_f are linked to heat sink temperature based on device datasheet

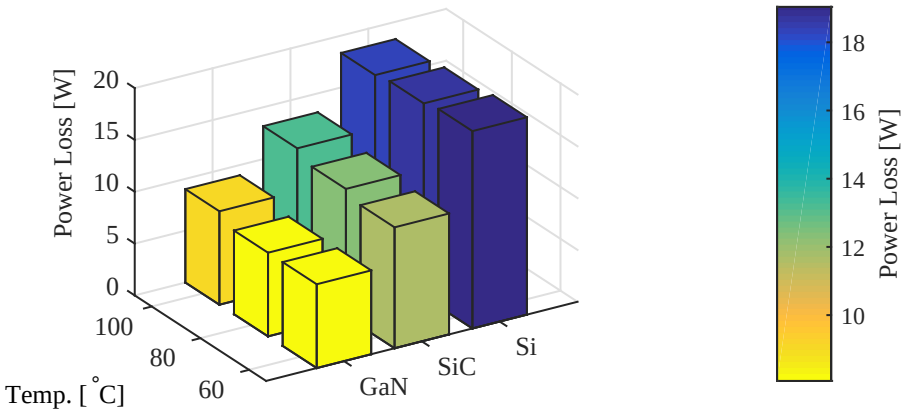
parameters in order to calculate the conduction losses. The modulation index can be calculated with respect to RMS value of output voltage and input DC link voltage. Based on the experimental results, the devices total, conduction and switching losses at 1.3 kW output power and 40 kHz switching frequency for Si, SiC and GaN based converter are presented in Figs. A.6a, A.6b and A.6c respectively. The total is lowest in GaN based inverter as presented in the efficiency curves and the conduction loss in Fig. A.6b. The results show the advantage of WBG devices at low current rating due to absence of on-state threshold voltage discussed in Chapter 3. With 230 V output RMS voltage, the peak current is approximately 8 A. When the conduction loss is subtracted from total loss, the switching loss data for each technology under different heat sink temperature values is obtained. Although the conduction loss of SiC and GaN devices increase with the increase of heat sink temperature, the switching losses remain constant and due to this reason, the converter performance with GaN and SiC is not affected by heat sink temperature increase as much as the case with Si IGBT.

A.0.3 Grid Connection

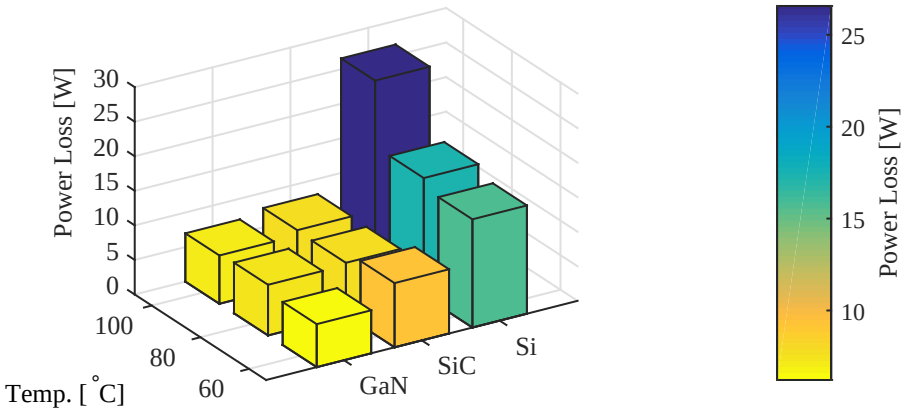
The dead-time between complementary switches in order to avoid shoot through in a half-bridge configuration introduces additional harmonics when the total dead-time becomes significant in a switching period, in other words with high switching frequency. In this setup, the dead-time is set as 1 μs for Si IGBT and 250 ns for SiC MOSFETs. The output current and voltage waveforms for both cases are presented in Fig. A.7. The results in Fig. A.7a show that with Si IGBT, output current is distorted at zero-crossings due to low modulation index and large dead-time. On the other hand, for SiC MOSFET based inverter with the same load and switching frequency conditions in Fig. A.7b, the distortion at the zero-crossing is minimised due to reduced dead-time between complementary switches.



(a)

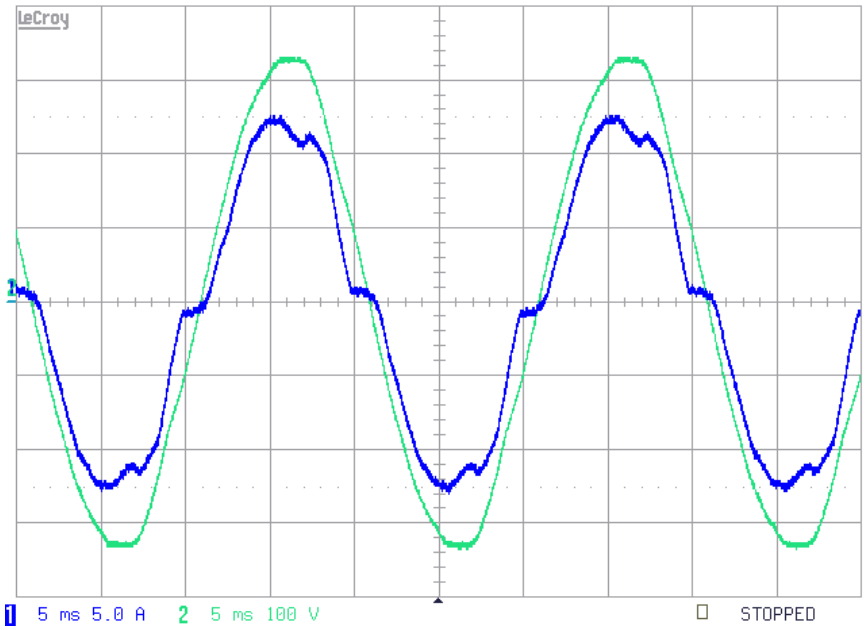


(b)

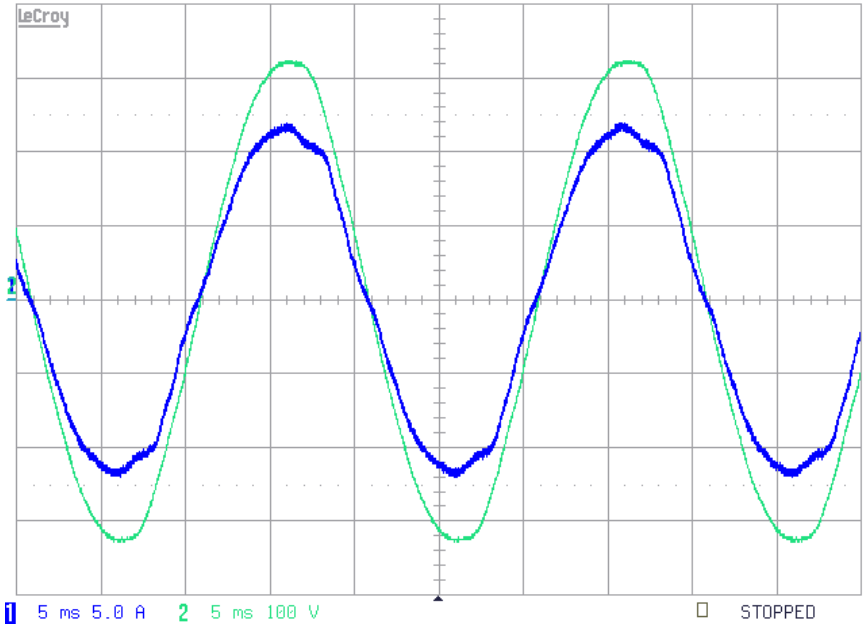


(c)

Figure A.6: Loss breakdown for GaN, SiC and Si based converter at 1.3 kW output, 40 kHz switching frequency: (a) total power device loss, (b) conduction loss, (c) switching loss.



(a)



(b)

Figure A.7: Grid voltage and current waveforms with (a) Si IGBTs and (b) SiC MOSFETs at 40 kHz switching frequency (CH_1: Grid current 5 A\div, CH_1: Grid voltage 100 V\div).

Appendix B

PCB Design for GaN HEMT Based ANPC Inverter

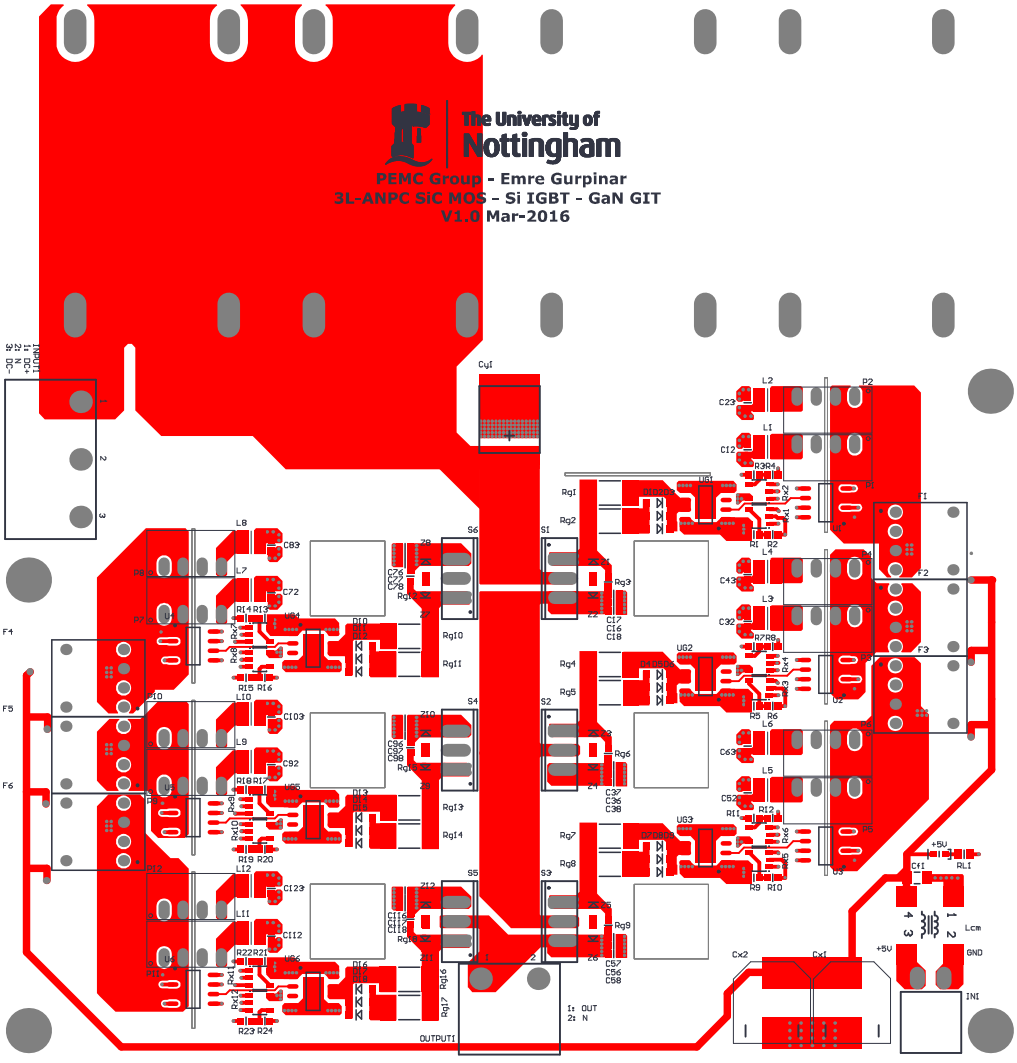


Figure B.1: Top layer layout for GaN HEMT based ANPC power cell.

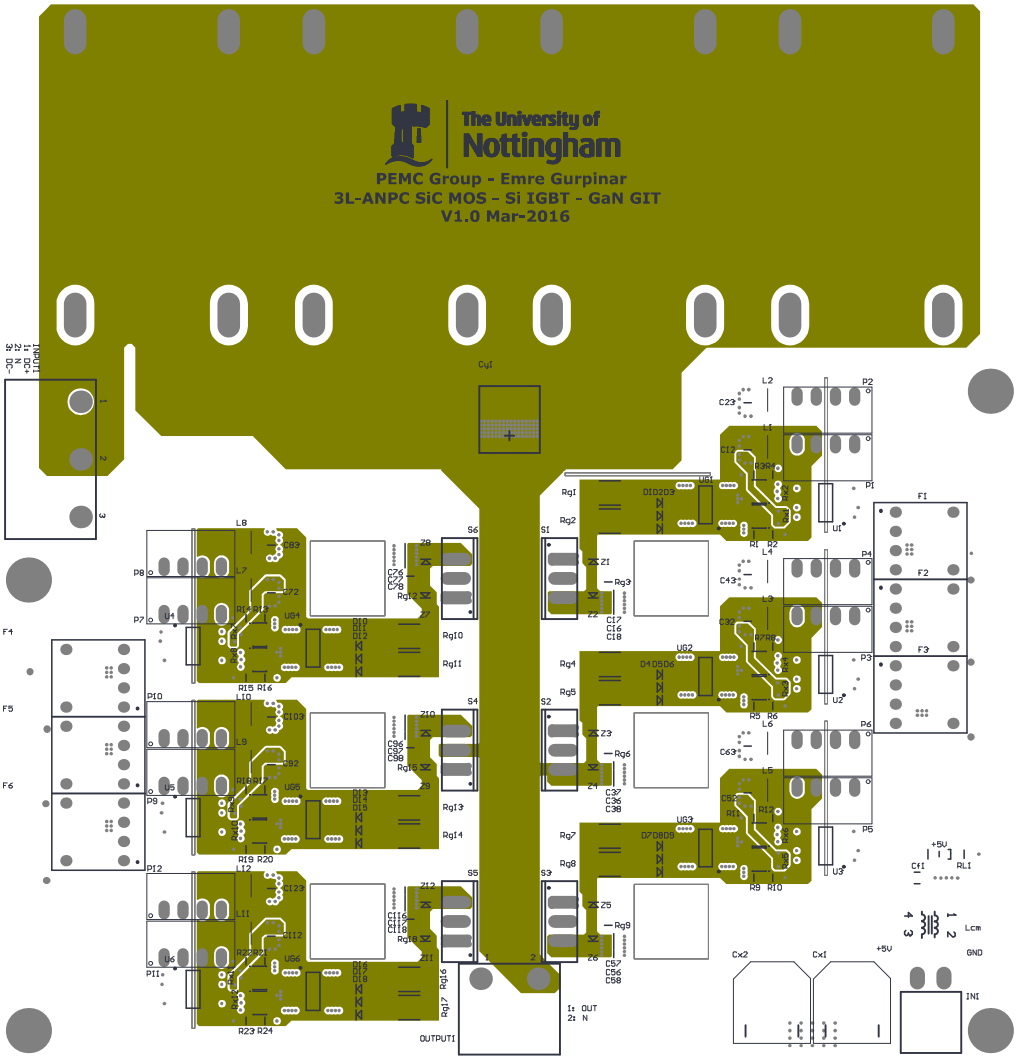


Figure B.2: Inner Layer 1 layout for GaN HEMT based ANPC power cell.

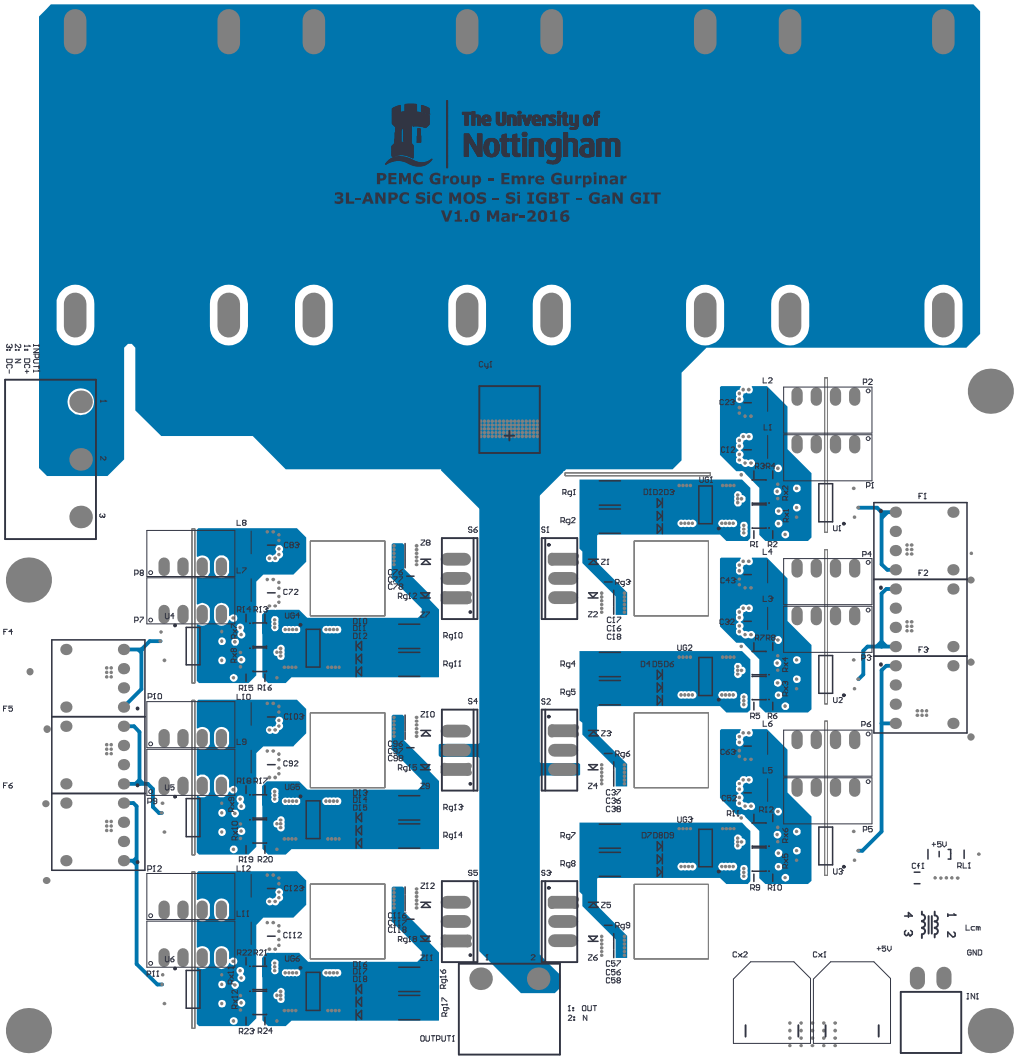


Figure B.3: Inner Layer 2 layout for GaN HEMT based ANPC power cell.

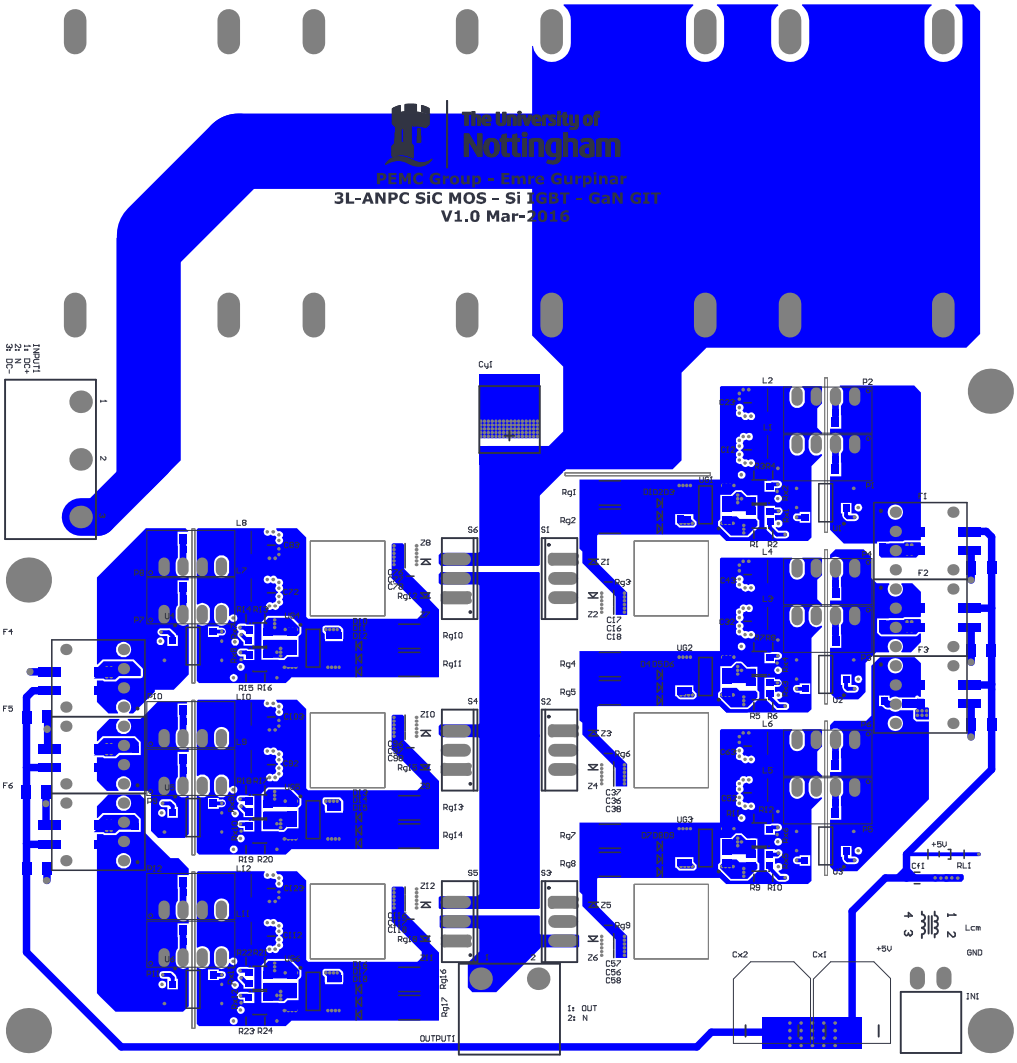


Figure B.4: Bottom Layer layout for GaN HEMT based ANPC power cell.