Department of Electrical and Electronic Engineering

A Multilevel Converter with a Floating Bridge for Open-Ended Winding Motor Drive Application

by

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To

My respected parents,

and

My beloved Wife, Pritha

Abstract

In this thesis, a dual inverter topology is considered as an alternative to a multilevel converter for the control of high speed machines. Instead of feeding to one end of the stator with a single power converter, this topology feeds from both sides of the stator winding using two converters, thus achieving multilevel output voltage waveforms across the load. A large amount of published work in the area of open end winding power converter topologies are focused on symmetrical voltage sources. This published research recognises the advantages of the converter system in terms of increased reliability, improved power sharing capability and elimination of common mode voltages when compared to traditional single sided three phase converter solutions. However isolated DC supplies come with the price of additional components thus increase size, weight and losses of the converter system.

The aim of this project is, therefore, to investigate on reducing size, weight and losses of the open end winding motor drive by eliminating the need for isolated supply as well to achieve multilevel output voltage waveform. A traditional open-end winding induction motor drive has been analysed in terms of weight and losses and it has been clearly identified that the isolation transformer not only increases the size and weight of a drive system but also includes additional losses.

A modified dual inverter system has then been proposed where one of the bridge inverters is floating, thus eliminated the need for isolated supplies. An asymmetric DC voltage sources ratio of 2:1 is utilised to achieve multilevel output voltage waveform across the load. The switching sequences are also analysed to identify the charging and discharging sequences to achieve control over floating capacitor voltage. This thesis describes the theoretical derivation of the modified converter model and algorithms as well as experimental results from an 11kW laboratory prototype.

Thesis contribution

The work presented in this thesis has resulted in two conferences and three journal publications. The published papers are as listed:

- S. Chowdhury, P. W. Wheeler, C. Gerada, and C. Patel, "Model Predictive Control for a Dual Active Bridge Inverter with a Floating Bridge," *IEEE Transactions on Industrial Electronics,* vol. 63, pp. 5558-5568, 2016.
- S. Chowdhury, P. Wheeler, C. Patel, and C. Gerada, "A Multilevel Converter with a Floating Bridge for Open-ended Winding Motor Drive Applications," *IEEE Transactions on Industrial Electronics,* vol. 63, pp. 5366-5375, 2016.
- S. Chowdhury, P. Wheeler, C. Gerada, and C. Patel, "A dual two-level inverter with a single source for open end winding induction motor drive application," *17th European Conference on* in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015*, 2015, pp. 1-9.
- S. Chowdhury, P. Wheeler, C. Gerada, and S. Lopez Arevalo, "A dual-inverter for an open end winding induction motor drive without an isolation transformer," IEEE *Applied Power Electronics Conference and Exposition (APEC),* 2015, pp. 283-289.

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Contents

LIST OF SYMBOLS AND ACRONYMS

Symbols	Definitions
S_x	Switching state
m	modulation index for carrier based modulation
V_m	Amplitude of the modulating signal
V_{cr}	Amplitude of the carrier signal
V_{DC}	DC link voltage
V_{DC_m}	Main inverters DC link voltage
V_{DC_f}	Floating inverters DC link voltage
V_α, V_β	Fictitious two phase voltage after using Clarke's transformation
T_s	Sampling time
T_a, T_b, T_c	Duty cycle time
m_a	modulation index for space vector modulation
k	Current time instant
$k+1$	Future time instant
g	Cost function for predictive control
G	Cost function for modulated model predictive control
V_{abc_s}	Three phase stator voltage
V_{abc_r}	Three phase rotor voltage
i_{abc_s}	Three phase stator current
i_{abc_r}	Three phase rotor current
Ψ_{abc_s}	Three phase stator flux
Ψ_{abc_r}	Three phase rotor flux
R	Resistance
L	Inductance
r_s	Three phase stator resistance matrix
r_r	Three phase rotor resistance matrix

R_s	Stator per phase resistance
R_r	Rotor per phase resistance
l_{ls}	Stator per phase leakage inductance
l_{lr}	Rotor per phase leakage inductance
l_{sr}	Stator to rotor mutual inductance
l_m	Magnetising inductance
θ_r	Rotor angular position
T_e	Electromagnetic torque
P	pole pair
ω_r	Rotor speed in rad/sec
ω_{rpm}	Rotor speed in rotation per minute
B_m	Frictional coefficient
T_L	Load torque
j	Rotor inertia
i_{abc_r5}	Three phase stator current for MMF distribution of 5^{th} harmonics
i_{abc_r7}	Three phase stator current for MMF distribution of 7^{th} harmonics
V_{ds}, V_{qs}, V_{os}	Stator voltages after rotational transformation is applied
V_{dr}, V_{qr}, V_{or}	Rotor voltages after rotational transformation is applied
i_{ds}, i_{qs}, i_{os}	Stator currents after rotational transformation is applied
i_{dr}, i_{qr}, i_{or}	Rotor currents after rotational transformation is applied
Ψ_{ds}, Ψ_{qs}, Ψ_{os}	Stator flux after rotational transformation is applied
Ψ_{dr}, Ψ_{qr}, Ψ_{or}	Rotor flux after rotational transformation is applied
$C_{v/f}$	v/f constant to achieve constant flux
P_{iron}	Iron loss
k_h	Hysteresis loss coefficient
k_e	eddy current loss coefficient
k_u	Window utilisation factor
f	Fundamental frequency

V_d	Diode voltage drop
J	Current density
A_p	Area product
W_a	Window utilisation factor
A_c	Iron area
B_{ac}	Maximum flux density
K_g	Core geometry
A_t	Surface area
N_p	Number of primary winding turn
A_w	Bare copper area
ρ	Resistivity
$I_{a,b,c}$	Three phase load currents
$V_{an,bn,cn}$	Main converter leg voltages
$V_{an',bn',cn'}$	Floating converter leg voltages
$V_{aa',bb',cc'}$	Voltages across the load
dt	Dead time
$V_{nn'}$	Voltage across the isolated neutral points
$V_{\alpha,\beta}$	Voltages after using Clarke's (stationary) transformation
$i_{\alpha,\beta}$	Currents after using Clarke's (stationary) transformation
i_{mrd}	Magnetising current
ω_{sl}	Slip speed
$\theta_{\psi r}$	Rotor flux angle
$S_{m1,m2,m3}$	Switching pulses for main inverter
$S_{f1,f2,f3}$	Switching pulses for floating inverter
T_s	Sampling time
I_{dc_f}	Floating inverters DC link current
g	Cost function for predictive control
G	Cost function for modulated model predictive control
λ	Weighting factor
f_s	Switching frequency

Abbreviations

MLT	Mean Length Turn
SVM	Space Vector Modulation
IM	Induction Machine
FS-MPC	Finite Set – Model Predictive Control
MPC	Model Predictive Control
MMPC	Modulated Model Predictive Control
PI	Proportional Integral
DC	Direct Current
AC	Alternating Current
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
THD	Total Harmonic Distortion
POD	Phase Opposition Disposition
APOD	Alternate Phase Opposition Disposition
IGBT	Insulated Gate Bipolar Transistor
PWM	Pulse Width Modulation
VSI	Voltage Source Inverter

General

*	When in superscript, denotes the reference value
[]	Square brackets identify matrices
α-β	When in subscript, denotes transformation of three phase symmetrical system into two phase system using Clarke's transformation
d-q	When in subscript, denotes transformation of three phase symmetrical system into two phase system using rotational transformation.

List of Tables

List of Figures

Chapter 1

Background and Motivation

This chapter presents a brief introduction about the background and motivation of the research work presented in this thesis; highlighting the emergence of multilevel converter systems in the recent past and specifically the dual inverter topology to supply an open phase load. This chapter also mentions the limitations associated with such systems, as well the objective of the presented research work. This chapter concludes with the thesis outline.

1.1 Background

Power Electronics inherited from the history of signal amplifier technologies which were then industrialised for high power applications. There are lots of advantages which power electronics brought, but the most significant one is the possibility to control electrical motor drives and to manage the power flow. During the Eighties and Nineties, the developments of power electronics allowed the implementation of revolutionary systems to improve existing technologies, as can be seen from the patent applications [1-4]. Nowadays power converters can connect systems with different electrical characteristics, for example, choppers connect two DC systems with different voltage level and inverters transform voltage (current) from DC to AC with variable amplitude and frequency. Furthermore, AC-AC converters transform ac voltage (current) with variable amplitude and frequency. Unfortunately, during the eighties and nineties, existing converter topologies allowed only a small margin for further improvements due to the intrinsic limits of semiconductor switching devices. For example, only the slowest devices can withstand a higher voltage.

Multilevel converters were developed with the specific aim to overcome the voltage limit of semiconductor devices. The main idea at the basis of multilevel

converters is to connect more devices in series and clamp the voltages between their pins to achieve the level of voltage with multiple steps. The concept of utilising multiple small voltage steps for power converter topologies was patented about forty years ago [5]. In the last two decades, multilevel inverter topologies have emerged as a very important alternative in the area of high-power, medium-voltage (MV) applications. This field of high-power drives has become one of the most attractive areas in the research and development of power converters. The classical two-level Voltage Source Converter (VSC) is limited to low and medium power applications due to the semiconductor blocking voltage limits. Multilevel converters use series connected switches and can share the blocking voltage thus enabling the realisation of high power VSIs. With the increase of the number of voltage levels the harmonic distortion is reduced as well as the blocking voltage that the components have to withstand. Unfortunately, the control complexity increases due to the incremental number of switches as well as for commutation techniques.

High power converters and MV drives were first developed in the mid-1980s [6]. The MV drives converter voltage ranges from 2.3kV – 7.2kV and the output power ranges from 200kW to as high as 12MW. The introduction of high-power insulated-gate bipolar transistors (IGBTs) and integrated gate commutated thyristors (IGCTs) in the late 1990s [7, 8] made a new standard for the MV drives. These devices are now extensively used due to their superior switching characteristics, reduced power losses, and ease of gate control. The advantages of multilevel converters include [9]:

- good power quality (low voltage distortion and dv/dt),
- good electromagnetic compatibility,
- operation with a lower switching frequency,
- high voltage capability,
- smaller common mode voltage steps (reducing the stress in the motor bearings),
- possibility for fault tolerant operation,
- additional degrees of freedom for control and
- higher efficiency.

The main disadvantages are described in [10-12]:

- a larger number of switching semiconductors are required, which for low-voltage systems causes a higher implementation cost,
- difficulties with capacitor voltage balancing,
- unequal current stresses on semiconductors and
- control complexity increases.

The applications of multilevel converters are now widely spread across industry, for example pumps in the petrochemical industry [13], water pumping stations [14], grid integration of renewable energy sources [15], reactive power compensators [16], steel rolling mills in metal industry [17], traction applications [17], fans in cement industry [18], laminators, conveyors, blowers, compressors and others.

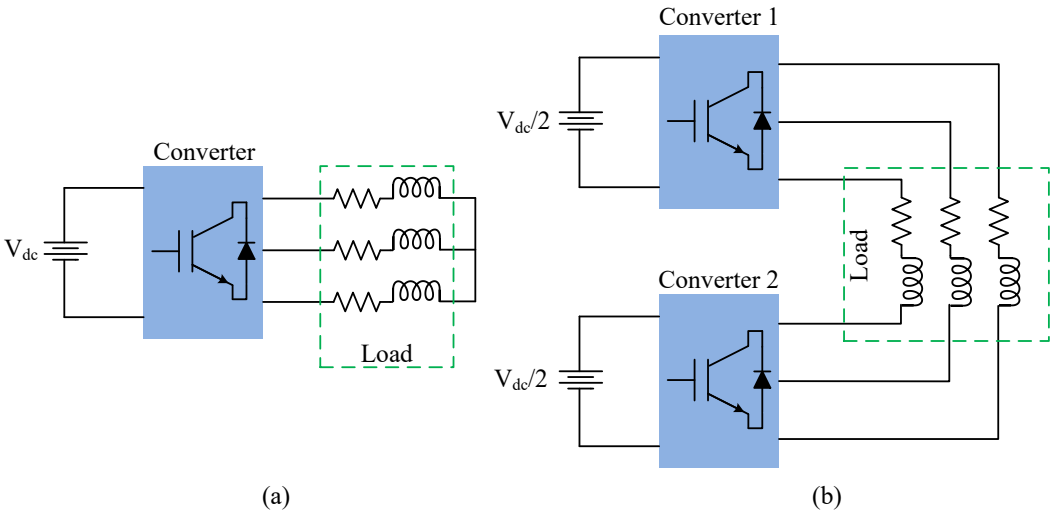


Figure 1.1 Converter topologies depending on supply techniques (a) single sided converter (b) dual converter.

The converter systems can be divided into two parts depending on the supply techniques. The conventional technique uses a single sided supply and the load can be configured as star or delta connected systems, shown in Figure 1.1(a). The other type uses two supplies across the load, known as dual inverter system shown in Figure 1.1(b). Two VSIs are used for this topology, with one connected at each side of the phase, leading to dual inverter supply. It is possible to achieve multilevel voltage waveforms across phases similar to single ended multilevel converter even

using dual two-level converter topology. However, the required number of isolated voltage sources are higher than the single ended multilevel converters.

The dual inverters are expected to retain most or even all of the advantages of multilevel converter. The topology shows further benefits such as redundancy due to the arrangement of the topology itself. There is a considerable amount of work published recently with regard to the three-phase open-end winding topology with symmetric voltage sources. On the basis of the attention given to the three-phase topology, the dual two-level inverter with symmetrical voltage sources can be considered mature. However, the dual inverter with asymmetric sources is not analysed in depth. Moreover, previous research has shown that the asymmetric converter system was not considered with advanced control techniques. For example, there is no research on dual inverter system controlled utilising predictive control algorithm. Thus the dual inverter with asymmetric voltage sources is considered for this research work.

1.2 Objectives of the project

The project investigates a cascade multilevel converter topology known as the dual inverter system to reduce size and weight as well as increasing system efficiency of the existing dual inverter topology. Like all other cascaded inverter topologies, the dual inverter topology requires isolated supplies to eliminate the path of common mode current flow, thus increase size, weight and losses of the system compared to traditional single sided multilevel converters.

The work presented in this thesis has multiple objectives. The first objective of this project is to eliminate the need for isolated supplies for the dual inverter system to increase efficiency and power to weight ratio of the converter system. The second objective is to introduce a predictive control algorithm for the dual inverter topology and modification of traditional predictive control algorithm to improve waveform quality. The aims have been met by achieving a number of research objectives, which are as follows:

- Modelling of three phase voltage source inverters.
- Modelling of more accurate three phase Induction Motor (IM) incorporating space harmonics.

- Investigation of losses for the open end winding IM drive system.
- Investigation of available switching states of dual two-level three phase inverter with symmetric and asymmetric voltage sources.
- Investigation of dual inverter system with one of the bridges is floating, where charging and discharging switching sequences are identified to control the floating capacitor. In addition, a limitation on charging is identified.
- Implementation of a Space Vector Modulation (SVM) scheme to control the floating bridge converter.
- Implementation of a Model Predictive Control (MPC) algorithm to control the load current and floating inverter voltage.
- Identification of challenges related to the predictive control algorithm.
- Implementing a predictive control algorithm to eliminate the challenges of the MPC
  algorithm.
- Creation of simulations of the proposed topology and control schemes using Matlab/Simulink and PLECS software.
- Experimental validation

Although the dual inverter topology can be considered mature for symmetric voltage sources, the amount of research regarding asymmetric sources is limited. The research also considers predictive control algorithms for an open end winding IM drive for the first time. This research presents a significant contribution to the existing knowledge regarding open-end winding topology. The originality of the research is shown by the publications listed under the title 'Thesis contribution' as shown in page iii.

1.3 Thesis structure

The thesis is organised as follows:

- **Chapter 1** gives background, motivation and objective of the research emphasising on challenges associated with cascade multilevel converters, specifically dual inverter system. The chapter also gives the thesis structure.

- **Chapter 2** gives an overview of the multilevel inverter topologies. The chapter describes the operating principle of popular multilevel converter topologies, such as the diode clamped, flying capacitor, cascaded, modular and hybrid converter topologies. This chapter also provides the modulation strategies for multilevel converter topologies as well as provides a brief description of a predictive control algorithm for multilevel converters.

- **Chapter 3** provides a detailed topological description of a specific cascade converter topology, known as the dual inverter system. This chapter gives a detailed analysis of the inverter system and modulation strategies. Chapter 3 also discusses the popular control strategies for this system.

- **Chapter 4** provides the mathematical model of the open-end winding motor drive fed by a dual inverter system. A modulation scheme is presented to simulate the drive system and losses of the individual components are estimated. A modification of the traditional dual inverter system is proposed in this chapter to minimise losses, size and weight of the drive.

- **Chapter 5** presents the modulation scheme to control the proposed converter along with modification of pulses to avoid the dead-time voltage spike. This chapter also shows simulation results with a Proportional-Integral (PI) controller along with Space Vector Modulation (SVM) as a modulation scheme, to support the analysis.

- **Chapter 6** presents a predictive control algorithm to control load current using the proposed converter topology, simulation results are shown to support the analysis. This chapter also presents a modified model predictive control algorithm to improve the waveform quality.

- **Chapter 7** gives a description of the experimental setup that uses a dual inverter system with one of the bridges is floating. This chapter presents all the experimental results using methods presented in Chapter 5 and Chapter 6.

- **Chapter 8** provides detailed discussion and concluding remarks for the thesis. Suggestions on areas where improvements can be made along with future work on the proposed topic are also provided.

1.4 Summary

This chapter gave an introduction about the project motivations and objectives by highlighting the advancement of multilevel converter topologies and the challenges associated with them. The chapter also presents the thesis structure.

Chapter2

Multilevel Voltage Source Converters

Multilevel converters are a family of power converters that produce more than two-levels in the output pole voltage waveform. The commutation of the switches in such converter topologies permits the addition of the capacitor voltages to achieve high voltage, multilevel output waveforms. The power semiconductor has to withstand only the associated capacitor voltage, which is usually smaller than the total output voltage magnitude. A generalised form of a two-level, three-level and n-level converter is shown in Figure 2.1.

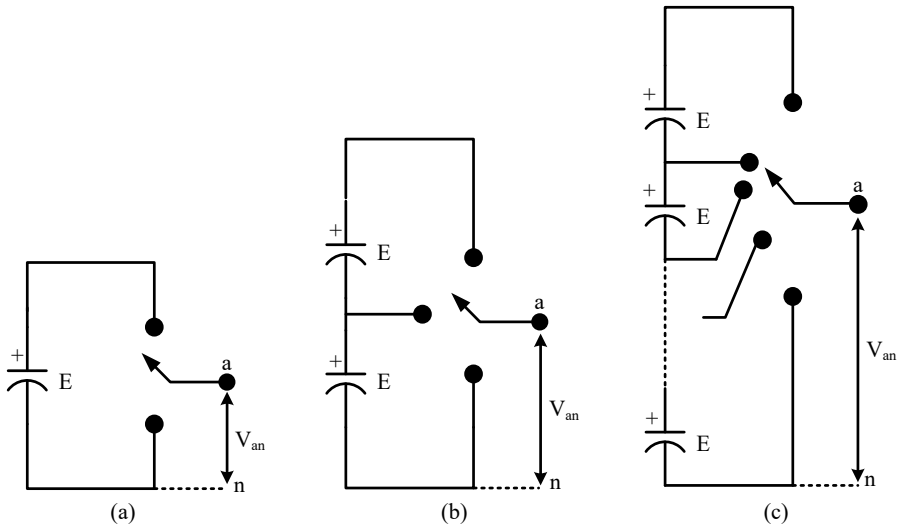


Figure 2.1 One phase leg of an inverter (a) two-level, (b) three-level and (c) n-level inverter.

An example of two, three, five and seven-level output voltage waveforms are shown in Figure 2.2. The use of multilevel power converter topologies improves output quality for a given switching frequency by tracking the sinusoidal reference more closely. Reductions in blocking voltage rating along with the switching losses for the same reference waveforms are usually the main advantages of multilevel converters. All these advantages come, however, at the expense of increased

converter size, and control complexity. The main disadvantages of multilevel converters are the increased number of semiconductor switching devices compare to two-level converters as well as more capacitors and the need for multiple isolated voltage supplies in some cases.

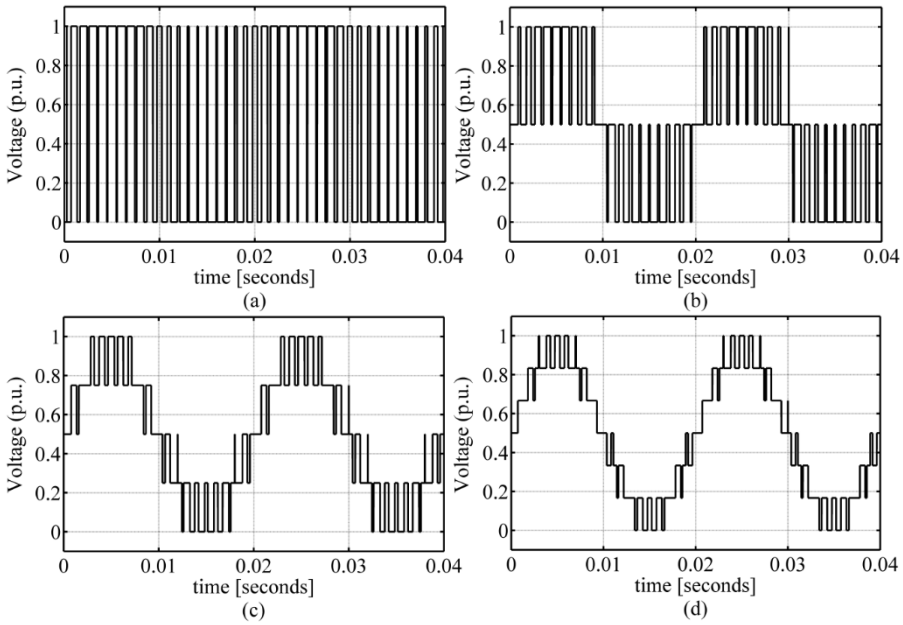


Figure 2.2 Per-unit output pole voltage waveform of power converters (a) two-level converter (b) three-level converter (c) five-level converter (d) seven-level converter.

This chapter presents an introduction to the well-known multilevel converter topologies along with their principles of operation. A few established modulation techniques are also presented focusing on their application to multilevel converters. Finally, a brief theory and background for model predictive control are presented.

2.1 Multilevel converter topologies

The following multilevel converter topologies are described in this section

- Diode clamped converter
- Flying capacitor converter
- Cascade converters
- Modular multilevel converters
- Hybrid converter topologies.

The diode clamped, flying capacitor and cascade converters are the most used multilevel converters [19, 20]. The modular multilevel converter is advantageous compared to multilevel converter topologies[21, 22] and has generated a lot of research interest in recent years. The hybrid converters [23], which are a mixture of different converter cells, are also receiving research attention due to their higher output voltage levels with lower device count compared to Neutral Point Clamped (NPC) and flying capacitor topologies. Brief descriptions of all these topologies are presented in the following sections.

2.1.1 Diode clamped converter

The diode clamped converter splits the DC bus into several equal steps using series capacitors. A single phase leg of the three-level and the five-level converter topology is shown in Figure 2.3. The DC bus is split into two and four equal voltage levels for the three-level and five-level converters respectively. The switching states of the converter circuit will act to connect the output terminal to one of the DC voltage levels and therefore generate multilevel output voltage waveform. The switching states and the output voltage levels for a five-level converter are shown in Table 2.1. In the table, the state of the switch S_x is always a compliment of S_x'. The three-level form of the diode clamp converter also known as Neutral Point Clamped (NPC) converter [24], which is one of the widely adopted multilevel converters [25]. This topology has been used in many industrial applications such as pumps, fans and compressors at high power levels [25]. Research has been conducted to overcome the problem of maintaining an equal split in the DC link voltage ratio. The split DC link voltages can become unbalanced due to load current flow especially during transients or unbalanced operation. The balancing of the neutral point was first modelled in [26] for a full operating range of the converter. In the paper, authors investigate the control of neutral point currents for each smaller triangle for a three level converter, controllable and uncontrollable current components were identified and a new current modulation index is defined. This control scheme utilises the controllable currents to balance the neutral point. To control the neutral point, measurement of unbalanced voltage and phase current amplitude is required. The benefit of this scheme is there is no ripple at half of the switching frequency. The drawback of this controller is the switching losses due to the introduction of

additional switching instances. A method of using a back to back converter to balance the capacitor voltage for a neutral point clamped converter is presented in [27]. The control strategy was derived using minimum energy principle suitable for practical implementation. The minimum energy principle states that the energy assumes to be minimum when all the capacitor voltages are balanced. To control the capacitor an energy function is defined and an online controller is set to minimise the energy. There are other different methods to balance the capacitor such as using redundant voltage states or to include the balancing requirement in a model predictive control algorithm [28]. There is another type of diode clamped converter which utilises fewer semiconductor devices than the traditional NPC converter, the T-type diode clamped converter [29]. Instead of using extra clamping diodes, this topology utilises only four semiconductor switches to achieve three-level output voltage waveform. One phase leg of the three-level T-type NPC converter is shown in Figure 2.4 along with the corresponding switching states in Table 2.2.

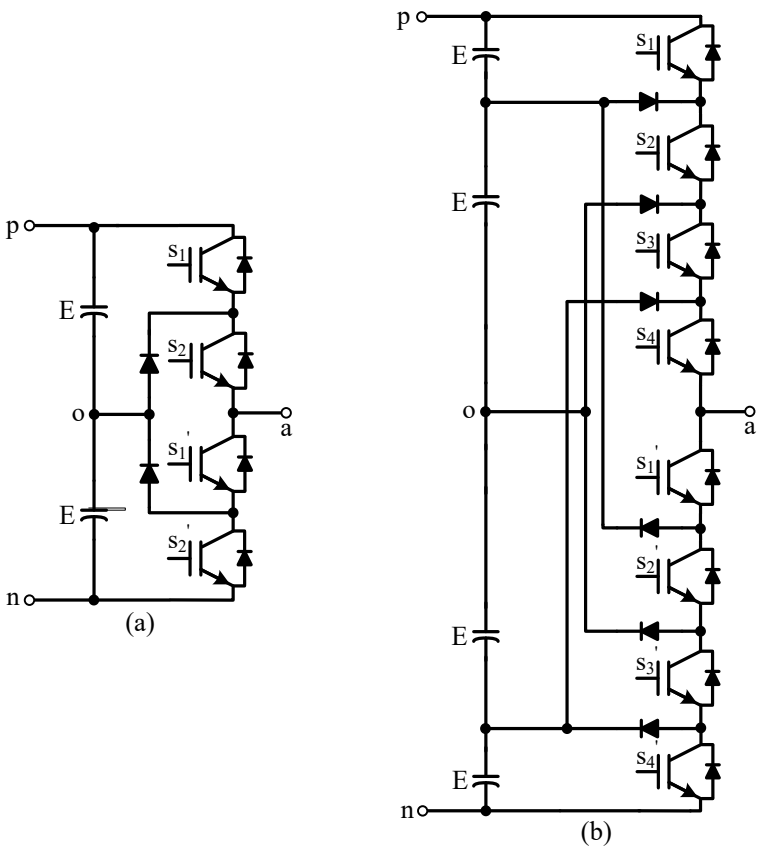


Figure 2.3 Single phase leg of diode clamped multilevel converter topology (a) three-level converter (b) five-level converter.

Table 2.1 Relationship between switching states and output voltage of five-level diode clamped converter.

Switching states								Output voltage
S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	V_{an}
1	1	1	1	0	0	0	0	4E
0	1	1	1	1	0	0	0	3E
0	0	1	1	1	1	0	0	2E
0	0	0	1	1	1	1	0	E
0	0	0	0	1	1	1	1	0

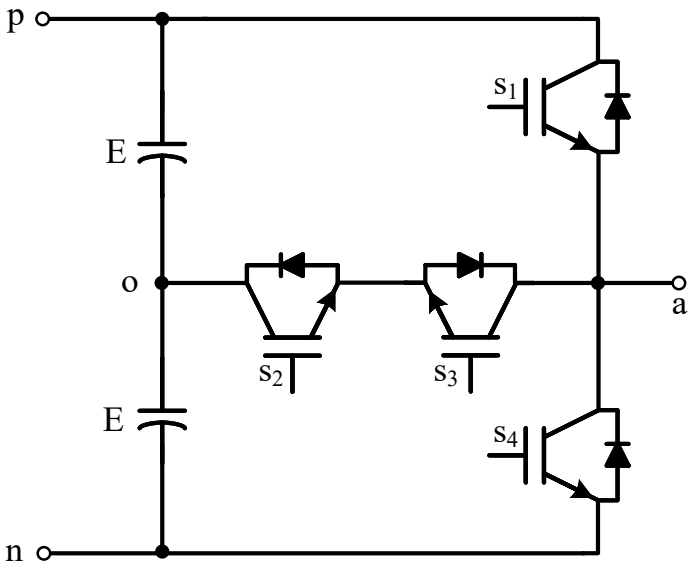


Figure 2.4 Three-level T-type NPC converter.

Table 2.2 Relationship between switching states and output voltage of three-level T-NPC converter.

Switching states				Output voltage
S_1	S_2	S_3	S_4	V_{an}
1	1	0	0	2E
0	1	1	0	E
0	0	1	1	0

The main disadvantage of the diode clamped topology is unequal loss distribution among semiconductor switching devices [30, 31]. Therefore different devices reach different operating temperatures and the most used devices are more prone to failure.

To avoid this effect, a modified converter topology has been introduced, the Active Neutral Point Clamped (ANPC) converter [29, 32, 33]. This topology uses two switching devices instead of clamping diodes to distribute losses equally between semiconductor switches [30]. One phase leg of the ANPC three-level converters along with the switching states is shown in Figure 2.5 and in Table 2.3 respectively.

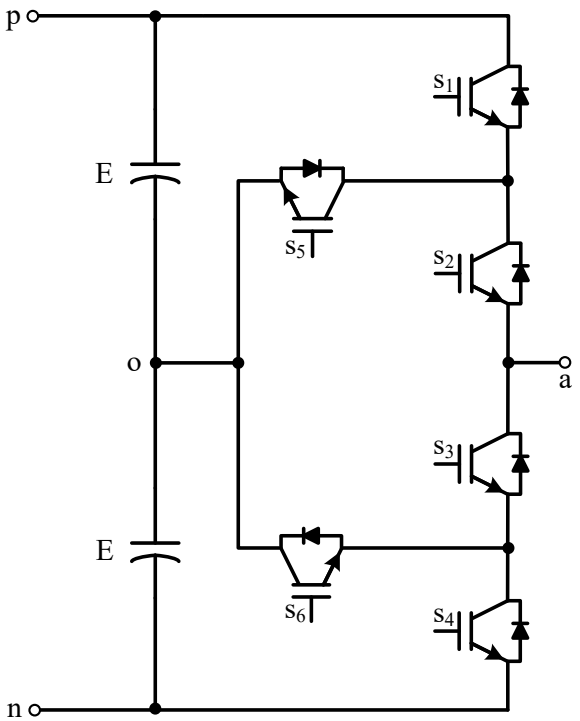


Figure 2.5 Three-level Active-NPC converter.

Table 2.3 Relationship between switching states and output voltage of three-level Active-NPC converter.

Switching states						Output voltage
S_1	S_2	S_3	S_4	S_5	S_6	V_{an}
1	1	0	0	0	1	2E
0	0	1	1	1	0	0
0	1	0	0	1	0	E
0	1	0	1	1	0	E
0	0	1	0	0	1	E
1	0	1	0	0	1	E

2.1.2 Flying capacitor converter

The circuit for a flying capacitor multilevel converter phase leg for the three-level and five-level converters are shown in Figure 2.6. The topology has similarity with diode clamped converters, the switching states for capacitor clamped converters determines which capacitors will contribute to the output voltage. These converters are also used for high power industrial applications [34]. The extension of the converter to more than five-levels is easy to implement, just like with diode clamp converters. The output leg voltage will be clamped to the negative DC rail if all the lower switches are closed and then closing any upper switches will contribute one of the capacitor voltages. A switching state table for the five-level flying capacitor topology is shown in Table 2.4.

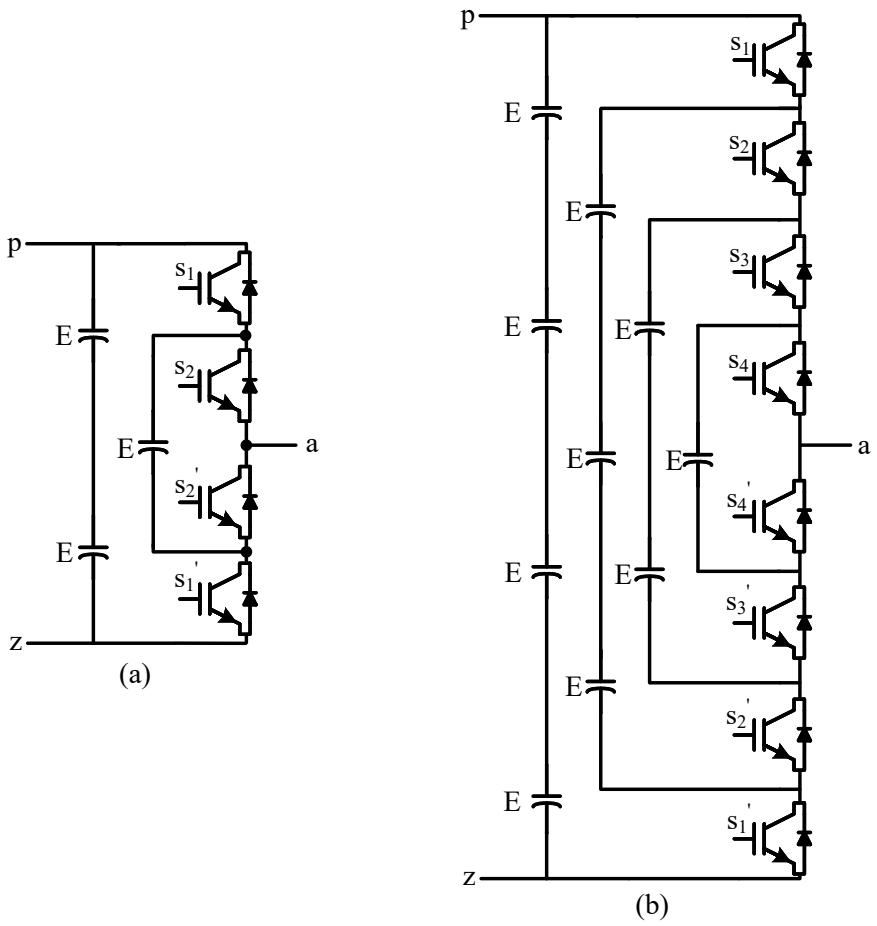


Figure 2.6 Single phase leg of flying capacitor multilevel converter topology (a) three-level converter (b) five-level converter.

Table 2.4 Relationship between switching states and output voltage of five-level flying capacitor converter.

Switching states								Output voltage
S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	V_{an}
1	1	1	1	0	0	0	0	4E
1	1	1	0	0	0	0	1	3E
1	1	0	1	0	0	1	0	3E
1	0	1	1	0	1	0	0	3E
0	1	1	1	1	0	0	0	3E
1	1	0	0	0	0	1	1	2E
1	0	1	0	0	1	0	0	2E
1	0	0	1	0	1	1	0	2E
0	1	1	0	1	0	0	1	2E
0	1	0	1	1	0	1	0	2E
0	0	1	1	1	1	0	0	2E
1	0	0	0	0	1	1	1	E
0	1	0	0	1	0	1	1	E
0	0	1	0	1	1	0	1	E
0	0	0	1	1	1	1	0	E
0	0	0	0	1	1	1	1	0

The main disadvantage of flying capacitor topology is the need for balancing the capacitor voltages. In the case of the three-level converters one has to control only one capacitor voltage, thus makes this control easier. However, increasing the number of levels makes it more difficult to control as a number of clamping capacitors increases. Unlike the diode clamped converter any combinations of upper switches are permitted and there are a lot of redundant switching states which can be used to balance switching losses [35]. Much research into flying capacitor topology has been focused on understanding the natural balancing behaviour that maintains the correct capacitor voltages [36-38].

2.1.3 Cascade converters

Two types of cascade converters are described in this section, one is the cascade H-bridge converter and the second is the dual inverter. A diagram of the cascade three-level and five-level H-bridge converters are shown in Figure 2.7. The H-bridge converter was first developed in the 1990s for medium voltage drives applications [39]. A single phase full-bridge converter will produce three distinct voltage levels. More than three voltage levels can be achieved by cascading more H-bridge cells. This is one of the simplest cascade converter solutions and provides modularity which reduces the cost of commissioning and maintenance as well as introducing some fault tolerant capacity [40, 41]. The possible switching states along with output voltages are shown in Table 2.5. The advantage of these converters depend on the applications; the circuit being best suited to applications such as STATCOM [42] and applications where independent voltage sources are inherent such as photovoltaic power applications and grid connected battery storage systems [43, 44].

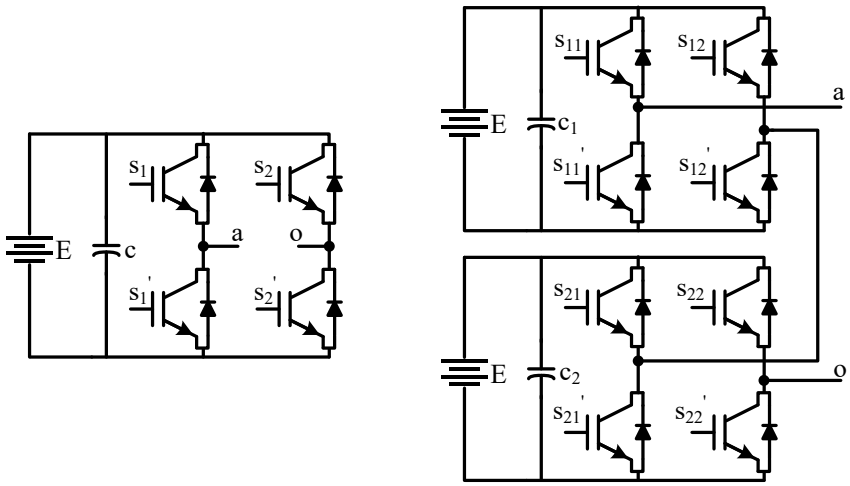


Figure 2.7 H-bridge converter topology (a) three-level full bridge converter (b) five-level cascade H-bridge converter.

The main disadvantage of cascade H-bridge converters is that each H-bridge (full bridge) cells require an isolated voltage source. As an example, for a three phase induction motor drive application using a full H-bridge converter, three isolated DC sources are required, which are costly and will increase the weight and losses in the drive system. However, a dual converter system [45] needs one less isolated supply than a three phase H-bridge system. A diagram of dual two-level inverter supplying a

three phase load is shown in Figure 2.8. The converter is composed of commercialised and reliable parts making implementation easier [46].

Table 2.5 Relationship between switching states and output voltage of five-level cascade H-bridge converter.

Switching states								Pole voltage
S_{11}	S_{12}	S_{21}	S_{22}	S_{11}'	S_{12}'	S_{21}'	S_{22}'	V_{ao}
1	0	1	0	0	1	0	1	2E
1	1	1	0	0	0	0	1	E
1	0	0	0	0	1	1	1	E
1	0	1	1	0	1	0	0	E
0	0	1	0	1	1	0	1	E
1	1	1	1	0	0	0	0	0
1	1	0	0	0	0	1	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	0	1	1	1	1	0	0	0
0	0	0	0	1	1	1	1	0
0	1	1	1	1	0	0	0	-E
0	0	0	1	1	1	1	0	-E
0	1	0	0	1	0	1	1	-E
1	1	0	1	0	0	1	0	-E
0	1	0	1	1	0	1	0	-2E

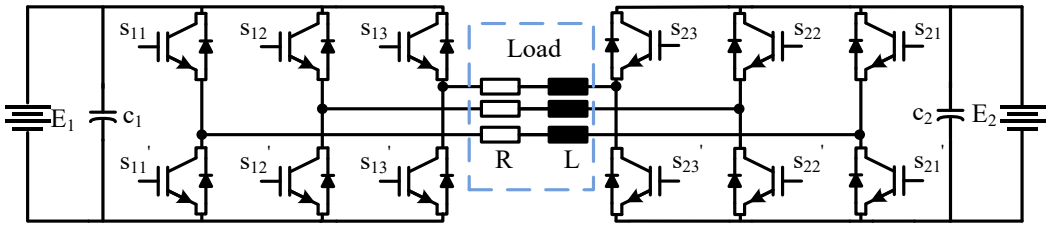


Figure 2.8 Cascade dual two-level three phase inverter topology with equal DC link voltage ratio.

The dual inverter topologies are widely used for motor drive applications due to its redundancy and multilevel characteristics [47, 48]. The dual two-level inverter shown here comprises of two equal DC sources and can mimic the three-level

converters output voltage with a lower device count than traditional three-level single sided converters [49]. Deviation of the DC link capacitor voltage can be avoided in dual inverter system by using an equal DC link voltage ratio. More levels can be achieved by splitting the voltage ratio, for instance with a DC link voltage ratio of 2:1 the same dual two-level converter can achieve four-level output voltage waveform [50]. One disadvantage of using an asymmetric DC link voltage ratio for the dual inverter system is that it can introduce DC link voltage deviation. The lower DC link voltage will charge to a higher voltage than required unless controlled. One simple solution is to avoid the charging switching sequences to balance the lower DC link voltage [50].

2.1.4 Modular multilevel converter

The modular multilevel converter is one of the recent additions to the multilevel converter family, first proposed in 2003[51]. Modularity is a way to make a larger system by adding smaller subsystems to achieve high power and to improve waveform quality. The structure of this converter is made in a way that each phase will have two arms and each arm will have several subsystems. A diagram of the modular multilevel converter is shown in Figure 2.9. The most used subsystems are half-bridge modules, other subsystem modules which are used is a full bridge, clamped double, neutral point clamped and flying capacitor topologies [52].

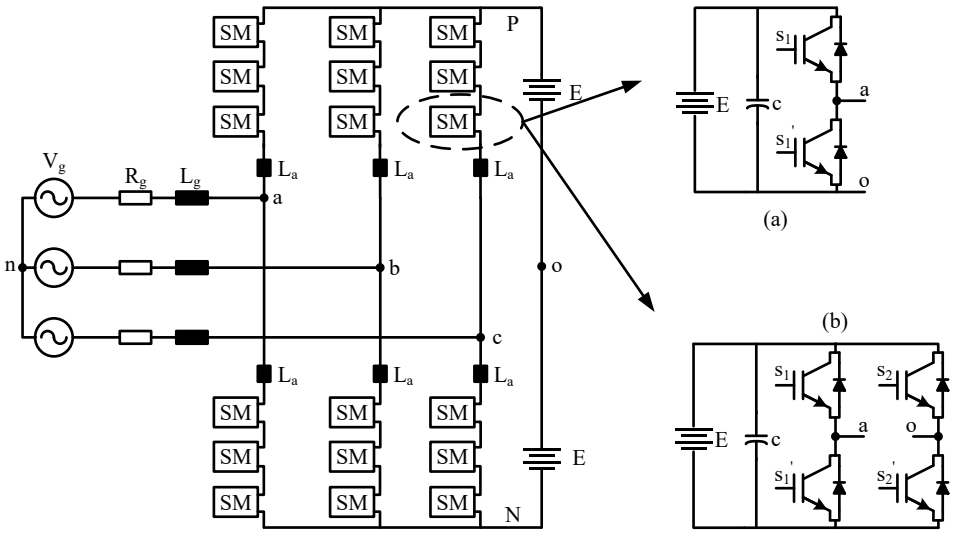


Figure 2.9 Modular multilevel converter topology (a) single modules with half bridge converters (b) single modules with full bridge converters.

Modular multilevel converters are gaining interest for applications such as HVDC and STATCOM as well as in multi megawatt motor drives due to the reduced need for voltage blocking properties in the semiconductor switching devices and more voltage levels [21, 52]. Due to more voltage levels each device has low switching frequency to approximate sine wave at the converter output, hence a reduced heat sink size is possible and in some cases it is possible to remove some of the passive filtering components [21, 53]. The recent focus of the MMC topology is on understanding the dynamics of the circuit topology and deriving suitable control methods. It has also been identified that the output voltages can be controlled independently so the same circuit can achieve ac to ac power conversion [22].

2.1.5 Hybrid converters

Hybrid multilevel converters are derived from the basic converter topologies, with one or more converters connected in series [54]. This type of converter can be a mixture of different converter topologies or can be of same types with different modulation for the stages. The simplest of the hybrid converter type is a cascaded H-bridge with different cell voltage levels. Due to differences in the cell voltage levels, they are also known as asymmetric cascade H-bridge converters [55].

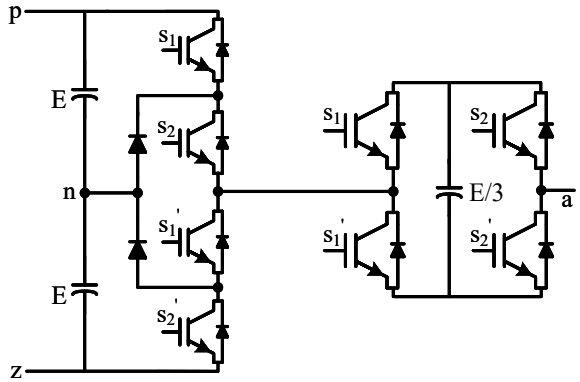


Figure 2.10 Hybrid nine-level converter topology, three-level NPC converter is series connected with three-level H-bridge converter

A hybrid converter such as mongrel between the three-level NPC with a series connected floating H-bridge converter is shown in Figure 2.10. This particular topology can produce nine different voltage levels [56, 57]. Another multilevel converter using two three-level NPC converters is shown in Figure 2.11. This type of

topology is suitable for high-voltage, high power applications due to the lower blocking voltage requirement and lower device switching frequency for the semiconductor devices. The output voltage waveform which consists of more levels to emulate a sinusoidal reference will improve current and voltage harmonic distortions[19].

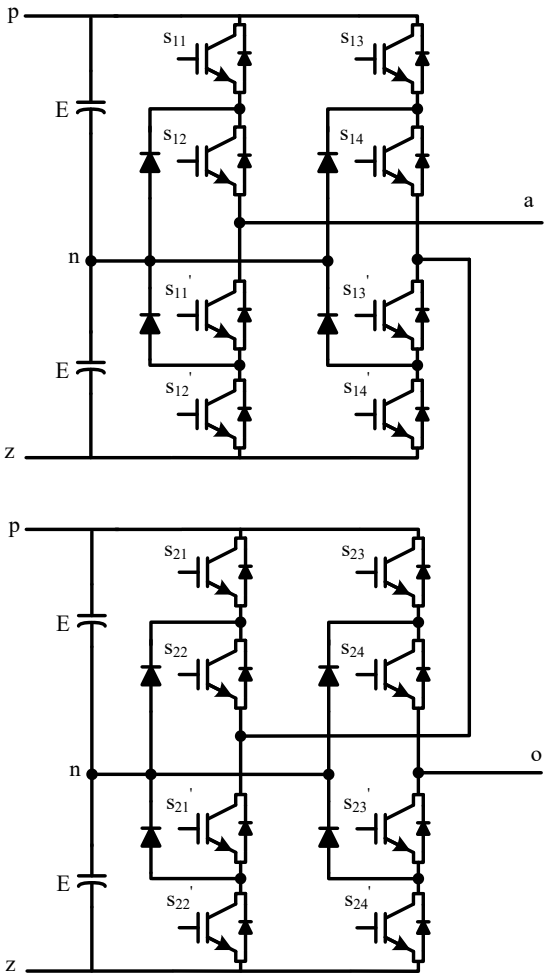


Figure 2.11 Hybrid multilevel converter topology, three-level NPC converter series connected with another three-level NPC converter.

2.2 Modulation strategies

Modulation is the technique to control the power converter's switches to produce the desired waveform. A classification of multilevel modulation technique is shown in Figure 2.12. Multilevel modulation techniques are subdivided into three divisions depending on switching frequency: fundamental, mixed and high switching frequency modulation. The selected harmonic elimination is a fundamental switching

frequency modulation techniques which can be used to eliminate specific low frequency harmonics. The mixed switching frequency modulation is used to commutate different devices with different switching frequency. This type of modulation is often used to modulate hybrid converter cells.

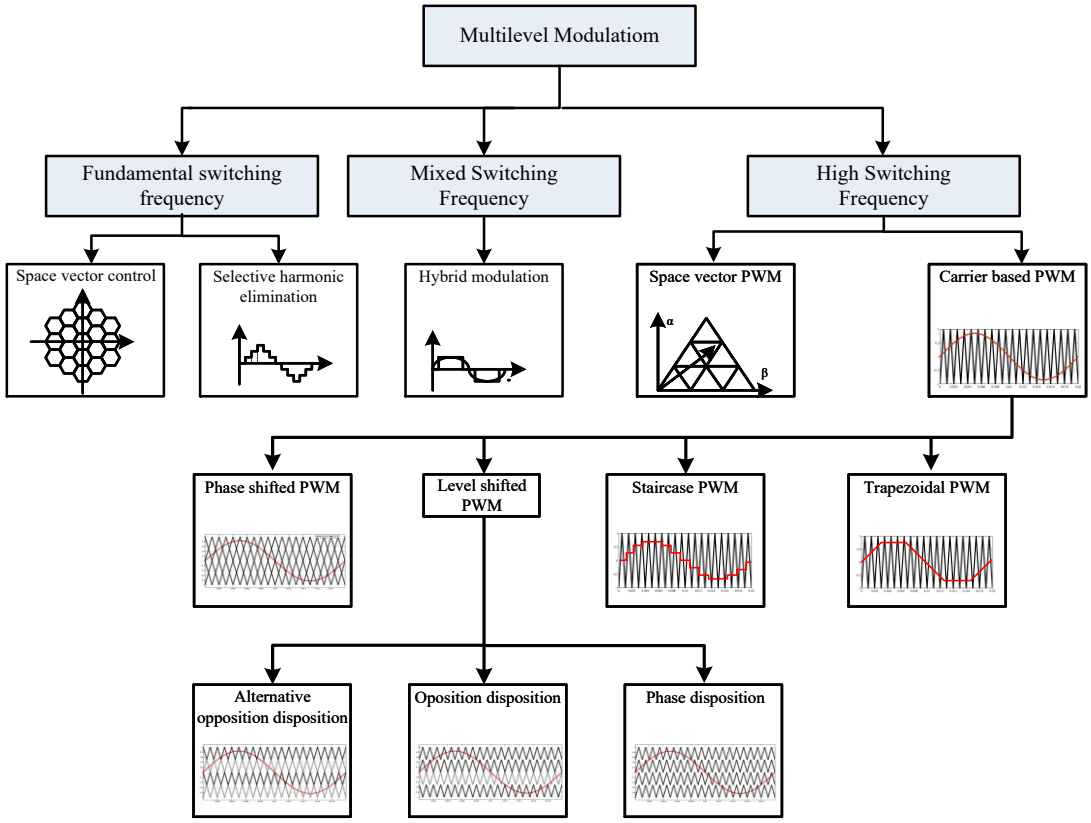


Figure 2.12 Classification of multilevel modulation technique.

The space vector, phase shifted and level shifted PWM techniques are widely used multilevel modulation methods and they are classified as high switching frequency modulation techniques. This higher switching frequency modulation techniques will be described in the next sections.

2.2.1 Carrier based modulation

Carrier based modulation originates from analogue control systems. In this type of modulation, a modulating wave is compared with a high frequency triangular carrier signal to generate the pulses for the switching devices. This is one of the easiest forms of modulation to understand. To modulate a multilevel converter,

multiple carrier signals are required, for example, for an N level converter N-1 carrier signals are required. The fundamental output voltage component can be controlled using a modulation index m_a as defined in equation 2.1.

$$m_a = \frac{V_m}{V_{cr}} \tag{2.1}$$

In this equation, V_m is the amplitude of the modulating signal and V_{cr} is the amplitude of carrier signal. A simple carrier based modulation scheme is shown in Figure 2.13. The utilisation for DC link voltage is $0.621 V_{DC}$for a simple carrier based modulation when modulation index m_a is '1' but this utilisation factor can be increased to $0.78 V_{DC}$by pushing the limit of the modulation by going into over modulating region (m_a = 3.24) [58]. This will add lower order harmonics to the output waveform which requires larger passive components for filtering. The way to increase the DC bus utilisation without going into the over-modulation region is by adding third harmonics to the modulating waveform. In this way, the actual modulating wave goes into over modulating region and therefore the DC bus voltage utilisation factor increases.

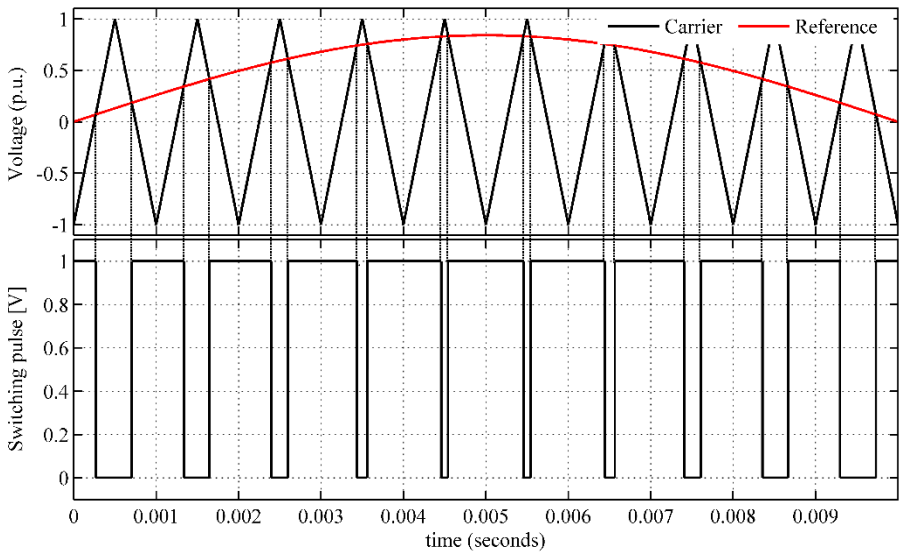


Figure 2.13 Carrier based modulation of two-level converter.

There are different types of carrier based modulation techniques, among them third harmonic injection (THI-PWM) [58], phase shifted [59] and level shifted [60]modulation techniques are described in the following sections.

2.2.1.1 Third harmonic injection PWM

The fundamental output voltage of a converter can be increased by adding third harmonics to the modulating signal, without causing over-modulation. The modulation method, shown in Figure 2.14, is generally known as third harmonic injection PWM [58]. The figure shows the concept of third harmonic injection where V_{m2} is composed of the signals $V_{m1}$and third harmonic component. Adding these two signals produces a flat topped modulating signal. As a result, the peak modulating waveform V_{m1}can go for higher amplitude than carrier wave, but due to third harmonics, the final complex modulating wave V_{m2}amplitude remains under the carrier waveform and thus avoids over-modulation [61, 62].

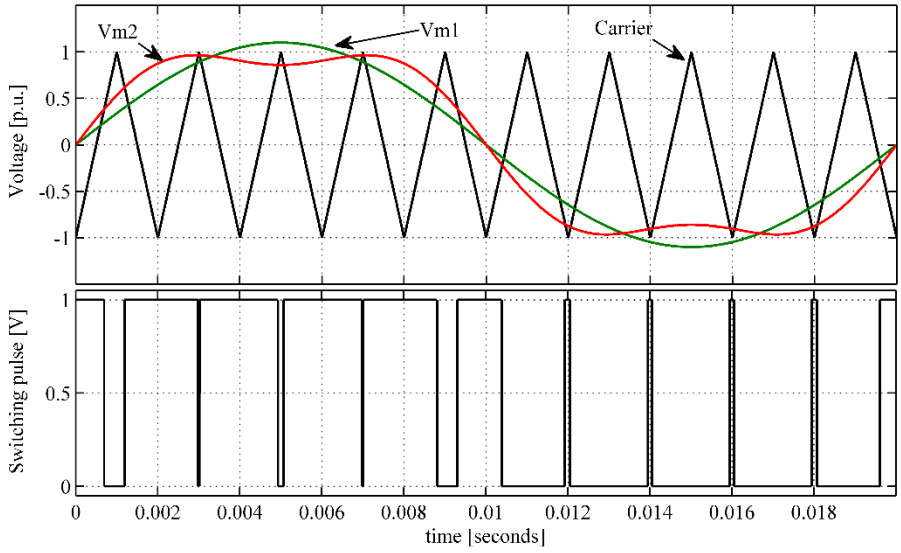


Figure 2.14 Third harmonic injection carrier based modulation for two-level converter.

The third harmonic component will also be modulated and will be present in the output pole voltage waveforms. In a three phase system these co-phasor third harmonics will cancel out in the line to line voltage waveform and therefore the third harmonic will have no effect on the load.

2.2.1.2 Phase shifted PWM

The phase shifted PWM follows the same standard principle as the standard carrier based modulation scheme. In this modulation scheme the modulating signal is compared with a triangular carrier signal to generate gating pulses for the switches,

but instead of one carrier, it utilises multiple carrier signals to modulate multilevel converters. The number of carriers depends on the number of output voltage levels that the power converter can achieve [59, 63]. As an example, a converter with *n*-levels output voltage will require *n-1* numbers of carrier signals. The carrier waveforms have to be displaced by shifting their phases. The phase shifts can be achieved by adding a delay for example, to achieve minimum harmonic distortion the carriers are shifted by a quarter of switching frequency for a five-level converter [64]. Figure 2.15 shows the carrier and reference voltages for a five-level converter along with the associated output voltage waveform.

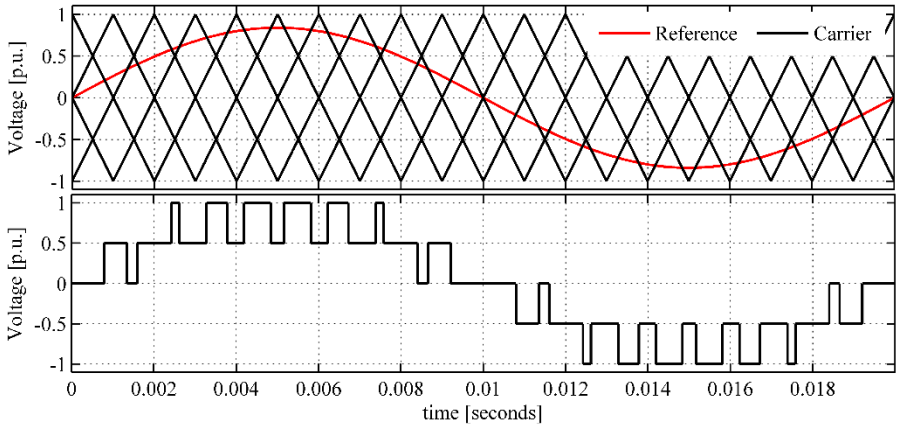


Figure 2.15 Phase shifted PWM for five-level converter

It can be seen that the output voltage is achieved by comparing all four carriers with the reference voltage, thus the effective switching frequency of output voltage waveform is four times higher than conventional carrier based modulation scheme for a five-level converter topology.

2.2.1.3 Level shifted PWM

The level shifted PWM also utilises multiple carriers to modulate the reference signal. The interval of possible voltage reference is subdivided into zones. Each zone has its own carrier signal to modulate the reference in that zone when the reference is not in a specific zone the associated power semiconductor switch will be turned on or off. The number of carriers needed to modulate is the same as PS-PWM, the most common type of level shifted PWM is called Phase Disposition (PD) [35, 63]. The PD-PWM technique for a five-level NPC converter is shown in Figure 2.16. There

are two other types of level shifted PWM techniques, one is Phase Opposition Disposition (POD) and the other is Alternate Phase Opposition Disposition (APOD).

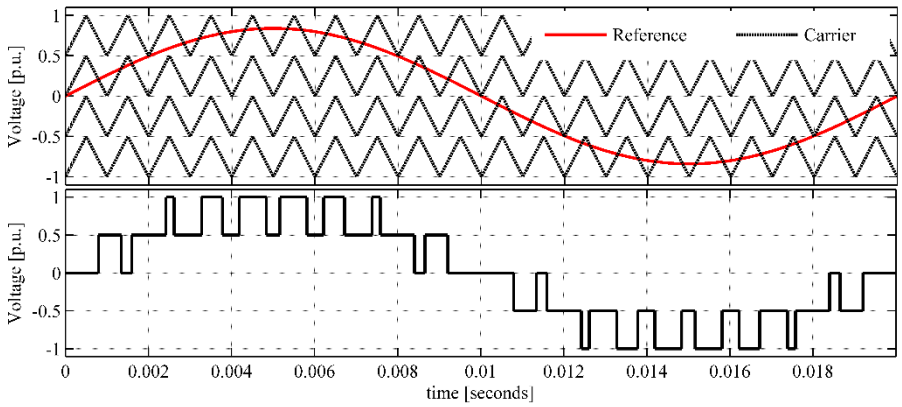


Figure 2.16 PD-PWM of five-level converter.

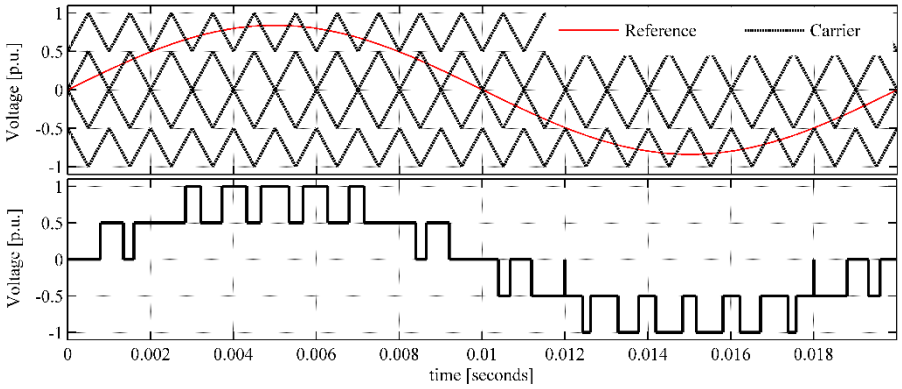


Figure 2.17 POD-PWM of five-level converter.

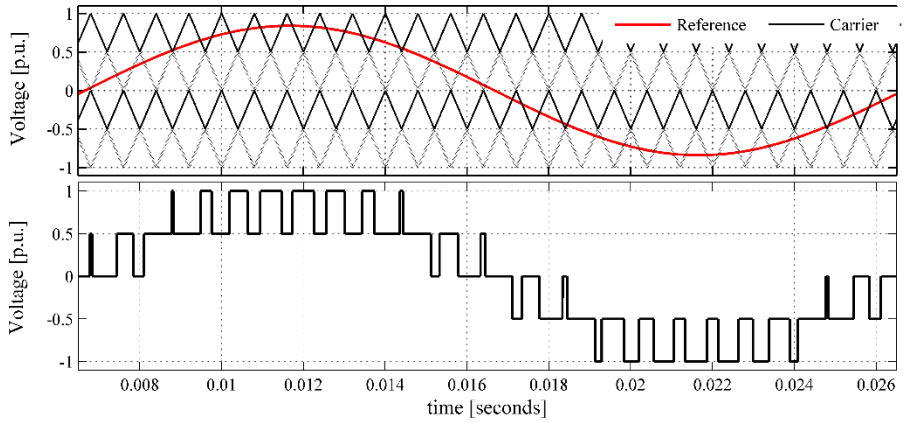


Figure 2.18 APOD-PWM of five-level converter.

In the POD level shifted PWM technique the carriers associated with the lower switches are in opposition to the carrier for the upper switches [65], as shown in Figure 2.17. In Alternative Phase Opposition Disposition (APOD) PWM the carriers are alternatively in phase or in opposition [66, 67], as shown in Figure 2.18.The difference between these three types of the level shifted PWM's is the output voltage symmetry. The POD-PWM and the APOD-PWM show asymmetrical output waveform of positive and negative half cycle in one fundamental period, while the PD-PWM shows symmetry in the output waveform.

2.2.2 Space Vector Modulation

Space vector modulation is one of the preferred digital modulation schemes to control voltage source converters. Space vector modulation chooses the switching states of the entire converter based on a mathematical transformation of reference voltage waveform [68, 69]. The space vector of symmetrical three phase current and voltages can be defined as

$$\begin{aligned} \vec{V} &= \frac{2}{3}(V_a + \bar{a}V_b + \bar{a}^2 V_c) \\ \vec{i} &= \frac{2}{3}(i_a + \bar{a}i_b + \bar{a}^2 i_c) \end{aligned} \quad \text{where, } \bar{a} = e^{j\frac{2\pi}{3}}, \bar{a}^2 = e^{-j\frac{2\pi}{3}} \tag{2.2}$$

where, $\vec{V}$ and $\vec{i}$ are the space vector of current and voltage respectively and ā is the vector rotator. Space vector can also be defined for stationary reference frame in real and complex quantities as shown in equation 2.3

$$\begin{aligned} \vec{V} &= (V_\alpha + jV_\beta) = Ve^{j\theta_v} \\ \vec{i} &= (i_\alpha + ji_\beta) = ie^{j\theta_i} \end{aligned} \tag{2.3}$$

Where, $e^{j\theta}$ is the vector rotator, it rotates the space vector in the stationary reference frame by an angle θ in two dimensional plane. The space vectors defined in equation 2.3 is illustrated in a complex plane shown in Figure 2.19.

2.2.2.1 Space vector and switching states

A space vector for a three-phase system can be generated utilising the *α-β* components of the waveforms. To relate between space vector and the switching states, a diode clamped converter is considered, shown in Figure 2.20. The figure represents a simplified diagram of a three-phase five-level converter connected to a star connected *R-L* load. Considering the converter, a space vector is constructed shown in figure 2.21. The vectors can be subdivided into six triangular sectors (*I - VI*). The identification of the sector is easier and can be classified in terms of reference voltage angle [62, 70]. If the reference voltage angle is $0 < \theta \leq 60^o$ then the reference is in sector *I* and then for each 60° the sector number will change.

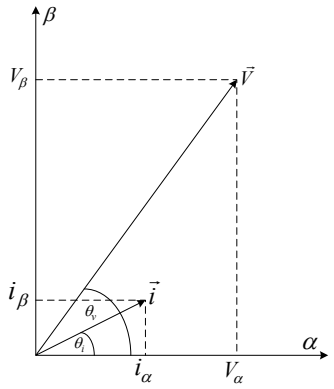


Figure 2.19 Voltage and current space vector in a two dimensional complex plane.

The relationship between switching states and space vector can be derived assuming that the three phase output of the inverter is balanced.

$$V_{ao}(t) + V_{bo}(t) + V_{co}(t) = 0 \tag{2.4}$$

Here V_{ao}, V_{bo} and V_{co} are the output phase voltages of the converter where *a, b,c* are three phases and '*o*' referred to the neutral point of a three phase star connected load.

$$\begin{bmatrix} V_\alpha(t) \\ V_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{ao}(t) \\ V_{bo}(t) \\ V_{co}(t) \end{bmatrix} \tag{2.5}$$

As these three voltages are balanced, the three phase system can be translated into two phase system using Clarke's transformation [62, 70, 71] as shown in equation 2.5. There are four types of Clarke's transformation among them the 2/3 scaling factor method is chosen to keep the input and output voltage magnitude equal. A space vector can be expressed in terms of real and imaginary α-β plane, as shown in equation 2.6

$$\vec{V}(t) = V_{\alpha}(t) + jV_{\beta}(t) \tag{2.6}$$

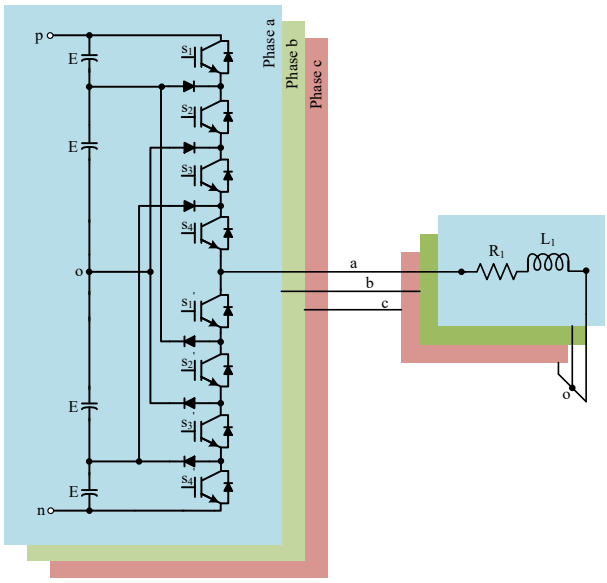


Figure 2.20 A three-phase five-level diode clamped converter topology.

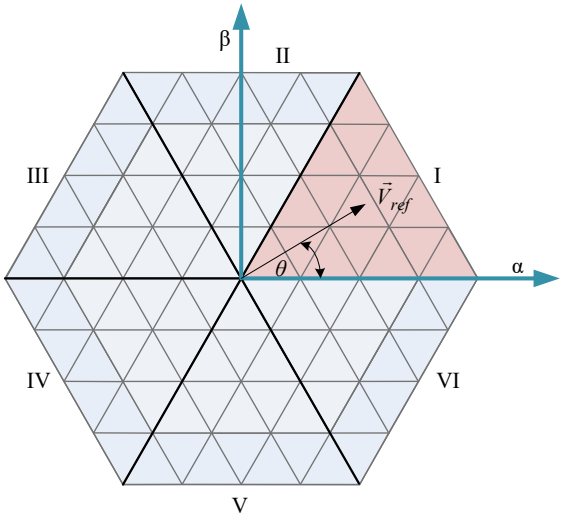


Figure 2.21 Space vector diagram of five-level converter.

Substituting equation 2.5 into equation 2.6

$$\vec{V}(t) = \frac{2}{3}\left[V_{ao}(t)e^{j0} + V_{bo}(t)e^{j2\pi/3} + V_{co}(t)e^{-j2\pi/3}\right] \tag{2.7}$$

Where, $e^{jx} = \cos x + j\sin x$ and x = 0, $2\pi/3$ or $-2\pi/3$. Equation 2.7 can be used to relate the voltage vector with the switching states by identifying the magnitude of phase voltages for each switching state.

2.2.2.2 Dwell time calculation

The reference voltage $\vec{V}_{ref}$ can be synthesised using the three nearest stationary voltage vectors [72, 73]. The dwell time is simply the duty cycle of the switching pulses during a sampling period T_s. The dwell time can be calculated using equation 2.8, where voltage multiplied by the sampling period T_s is equal to the sum of the three duty cycle multiplied by the adjacent stationary voltage vectors.

$$\begin{aligned} &\vec{V}_{ref}T_s = V_1T_a + V_2T_b + V_3T_c \\ &T_a + T_b + T_c = T_s \end{aligned} \tag{2.8}$$

Where T_a, T_b and T_c are the duty-cycles for the voltage vectors V_1, V_2 and V_3 used to synthesise the reference voltage vector, as shown in Figure 2.22. If the voltage vector resides in the red triangular small subsector then:

$$\vec{V}_1 = (\frac{2}{4} + j\frac{\sqrt{3}}{4}) * V_{dc} \tag{2.9}$$

$$\vec{V}_2 = (\frac{5}{8} + j\frac{\sqrt{3}}{8}) * V_{dc} \tag{2.10}$$

$$\vec{V}_3 = (\frac{3}{8} + j\frac{\sqrt{3}}{4}) * V_{dc} \tag{2.11}$$

By substituting equation 2.9-2.11 into equation 2.8:

$$V_{ref}(\cos\theta + j\sin\theta)T_s = (\frac{2}{4} + j\frac{\sqrt{3}}{4})V_{dc}T_a + (\frac{5}{8} + j\frac{\sqrt{3}}{8})V_{dc}T_b + (\frac{3}{8} + j\frac{\sqrt{3}}{4})V_{dc}T_c \quad (2.12)$$

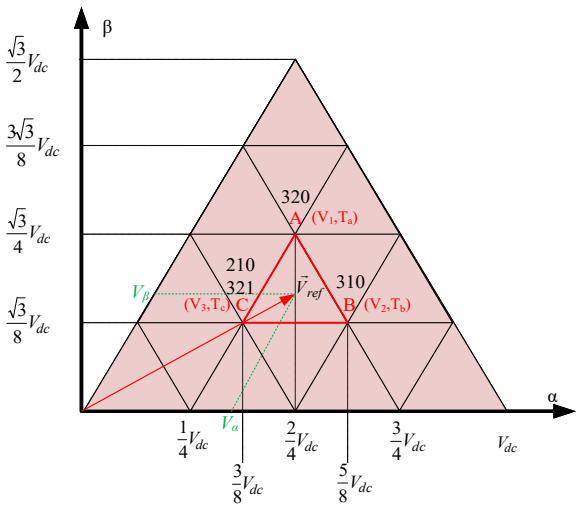


Figure 2.22 Sector I of five-level converter.

Real and imaginary parts of the equation 2.12 are:

$$\begin{aligned} &\text{Re}: \ 2T_a + \frac{5}{2}T_b + \frac{3}{2}T_c = \frac{4}{\sqrt{3}}\frac{\sqrt{3}V_{ref}}{V_{dc}}T_s\cos(\theta) \\ &\text{Im}: \ T_a + \frac{1}{2}T_b + \frac{1}{2}T_c = \frac{4}{3}\frac{\sqrt{3}V_{ref}}{V_{dc}}T_s\sin(\theta) \end{aligned} \quad (2.13)$$

By solving the equations together the dwell time can be found:

$$\begin{aligned} T_a &= T_s[1-2m\sin\theta] \\ T_b &= T_s\left[m\sin\left(\frac{\pi}{3}+\theta\right)-1\right] \quad \text{for } 0 \le \theta \le \frac{\pi}{3} \\ T_c &= T_s\left[1-2m\sin\left(\frac{\pi}{3}-\theta\right)\right] \end{aligned} \quad (2.14)$$

Where m is the modulation index and can be defined as

$$m = \frac{\sqrt{3}V_{ref}}{V_{dc}} \quad (2.15)$$

2.2.2.3 Switching sequence design

The final stage of the SVM algorithm is to design the switching sequence. There is no specific design rule for the switching sequence, but there are some requirements to minimise the device switching frequency [70], which are

- The transition from one switching state to the next should involve only two switches in the same leg.
- The transition from one sector to another in space vector diagram should take a minimum number of switching.

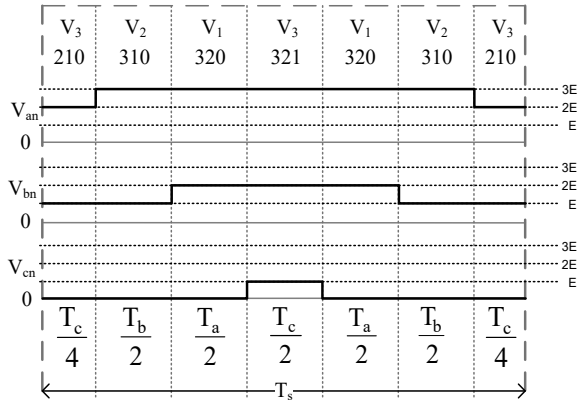


Figure 2.23 Seven segment switching sequence.

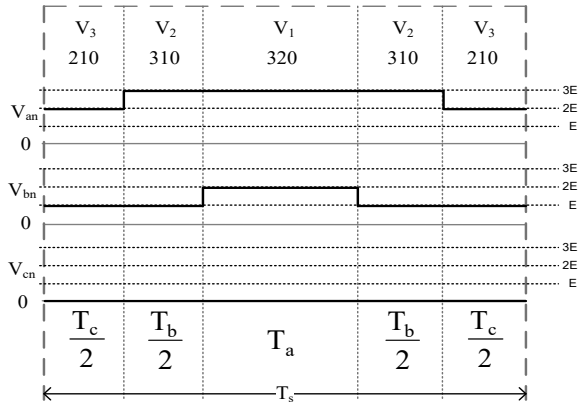


Figure 2.24 Five segments (discontinuous) switching sequence.

A seven segment switching sequence is shown in Figure 2.23 for when the reference voltage resides in the red triangle, shown in Figure 2.22. It can be seen that in one sample period the voltage states change seven times and the transition from

one state to other requires only two switches. The redundant zero vectors are utilised to minimise the switching losses and each of the switches turns on and off once in one sample period, therefore the device switching frequency is equal to the sampling frequency.

There is another type of switching sequence called the five segment switching sequence. This switching sequence considers the same principle as the seven segment switching sequence, but the switching states change five times in one sample period. In the five segment switching sequence, one of the three phases is clamped to either the positive or negative terminal of the DC bus, as shown in Figure 2.24. This can be true for a period of $(2\pi/3)$ per cycle of the fundamental frequency. Due to the switching discontinuity, the five segment switching sequence is also known as discontinuous switching sequence [70].

2.3 Model predictive control for multilevel converters

The model predictive control has been widely used for different power electronics applications [74, 75]. The advantage of model predictive control for power electronic applications is its ability to include constrains and nonlinearities. Model predictive control algorithms typically have faster dynamics, which can be advantageous for faulty conditions. The other advantageous features are, control of multiple variables in a single control loop and model predictive control does not require complex time calculations and switching sequence design.

The model predictive control algorithm can be achieved by predicting the future behaviour of the control parameter(s) for all the converter's possible switching states and then choosing the optimum state. To achieve proper control an accurate model of the load and converter is necessary [76]. A generalised block diagram for model predictive control is shown in Figure 2.25. The control algorithm measures the control variables *x(k) and* calculates the future prediction *x(k+1)* of the control variables for all available converter switching states. Then the minimum error of the predicted value is selected in the cost function optimisation block. The converter states are selected according to the minimum cost function values. The cost function can simply be presented as

$$g = \lambda_1 \left| parameter_1^{*} - parameter_1^{(k+1)} \right| + \lambda_2 \left| parameter_2^{*} - parameter_2^{(k+1)} \right| \qquad (2.16)$$

Here g is the cost function, '$parameter_1$ and $parameter_2$' are the control constrains superscript '*' represents the reference value and $k+1$refers to the predicted value and λ is the weighting factor to normalise the error value. The general concept of the MPC algorithm principle is based on sample time and switching sequence selection as shown in Figure 2.26. Where, $k-1$, k, $k+1$, $k+2$, $k+3$ and T_s refers to the previous, current, one sample ahead, two sample, three sample ahead predicted values and sampling time respectively. The measurement of the control parameter is taken at current sample period, then these values are used to predict the $k+1$ future reference by utilising all available switching states offered by the converter.

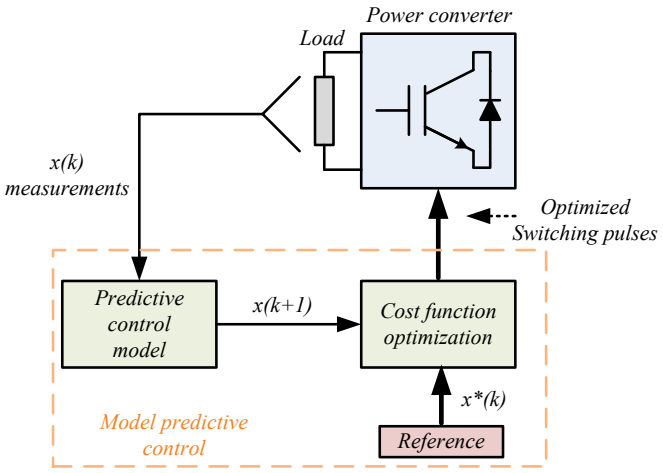


Figure 2.25 Block diagram of predictive control algorithm.

After achieving all available predicted control variable values these are then compared with reference values as shown in equation 2.16. Then the minimum cost function value is identified and the switching sequence that achieved minimum cost function will be selected for the next sampling interval. There are few drawbacks of model based predictive control algorithm, as the name suggests the controller use the model of the load and the converter to predict the current. The challenge is to define an accurate model and estimation of load parameters. It has been shown in [77, 78] that any variation in the model inaccuracy will produce errors between the measured variable and the prediction as well as more ripple in the control signal. Authors in [79] have demonstrated a model free predictive control to avoid the challenges of model based predictive control. The control method requires to measure the control variable twice in a single sampling period and then the amplitude difference (ΔC) of

this two values are calculated. The future control variable is predicted using ΔC values and thus avoid using the discrete load model compared to model based predictive control. Authors claim that these controllers achieve better tracking than model based predictive control algorithm. Both the model free or model based predictive control can select the same optimal switching state for two or more successive sampling intervals, resulting in a variable switching frequency [76]. Due to variable switching frequency harmonics of the control variable will spread all over the frequency plane thus output filter design become difficult as well as harmonic distortion will be higher.

Several solutions have been proposed in the literature, including improved vector sequences achieved by modifying the pulse patterns [80], the introduction of modulation schemes within FS-MPC as well as increasing the prediction horizon to improve waveform quality [80-83]. An analytical calculation to identify duty cycle time was shown in [82] and an SVM technique has been applied to the FS-MPC current controller for a six-phase inverter [84]. In such approaches, the duty cycles are calculated by solving an optimisation problem. However, multi-objective control becomes rather complex since it requires a solution for a multi-dimensional optimisation problem to be derived [85].

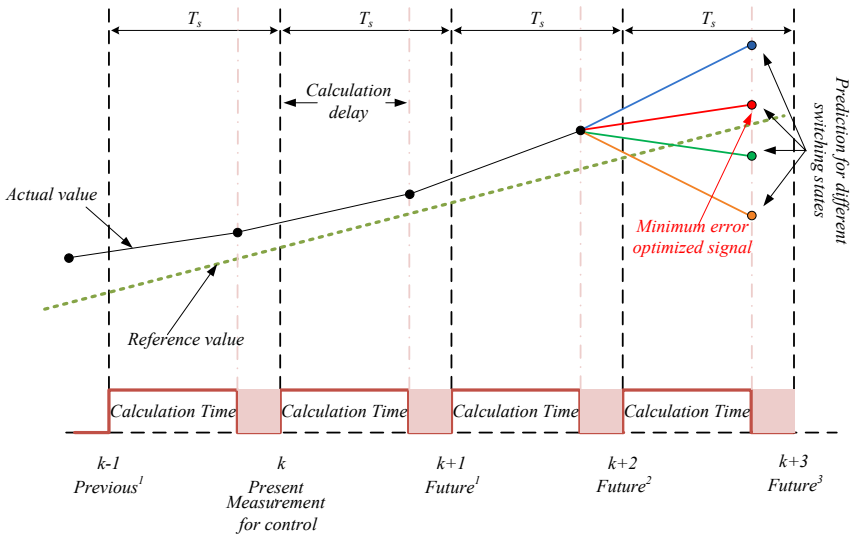


Figure 2.26 Sampling interval and switching state selection for predictive control.

Other methods of achieving fixed switching frequency at the output are shown in [86-90] wherein [87, 90] authors introduce a modulation scheme similar to SVM

algorithm inside cost function algorithm thus achieves fixed switching frequency at the output. In [88] authors achieved fixed switching frequency by limiting the switching choice to predetermined sequences that are based on regular sampled PWM. To achieve desired output the controllers needs to be sampled much higher than the expected switching frequency and can be challenging for low level control platforms.

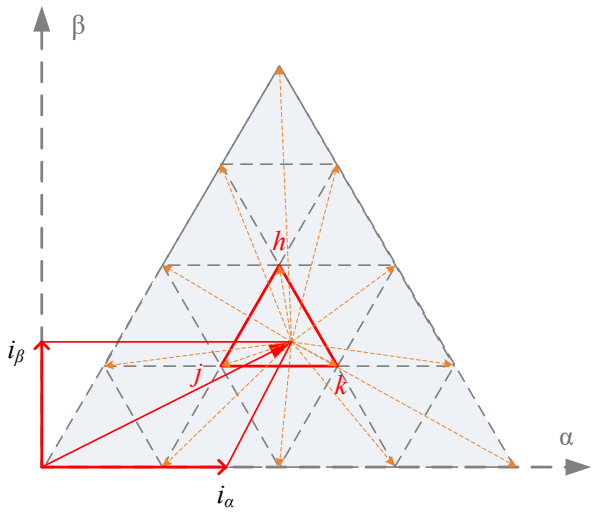


Figure 2.27 Current space vector diagram for MMPC algorithm.

There are several methods described in the literature to achieve fixed switching frequency modulation but the one will be discussed in this section is Modulated Model Predictive Control (MMPC) [91] due to its similarity with SVM algorithm. The controller could also be considered as an alternative to traditional controllers for its simplicity and intuitive implementation.

MMPC allows the retention of all the available characteristics of Finite Set Model Predictive Control (FS-MPC) as well as increasing the performance in terms of power quality. MMPC is designed to mimic the SVM algorithm [90]. This algorithm uses a suitable modulation scheme in the cost function minimisation[87, 91, 92]. To understand the process of cost function minimization, a multilevel converter space vector diagram is considered for the MMPC load current control algorithm, as shown in Figure 2.27. To reduce the calculation time and control complexity the controllers are designed in α-β coordinates. The controller will have predefined switching vectors for each small triangle (sub-sectors), in this case, the resultant voltage vector is in the red triangle. The controller will calculate currents for each switching states

of the specific triangle using the load model and will calculate the cost function for each state, shown in equations 2.17 – 2.19. The timing will be calculated incorporating these cost functions for each switching vector. Finally, the total cost function of that particular triangle will be calculated using the following equations:

$$g_h = \sqrt{(i_{h-\alpha} - i^*_{h-\alpha})^2 + (i_{h-\beta} - i^*_{h-\beta})^2} \tag{2.17}$$

$$g_j = \sqrt{(i_{j-\alpha} - i^*_{j-\alpha})^2 + (i_{j-\beta} - i^*_{j-\beta})^2} \tag{2.18}$$

$$g_k = \sqrt{(i_{k-\alpha} - i^*_{k-\alpha})^2 + (i_{k-\beta} - i^*_{k-\beta})^2} \tag{2.19}$$

Here, g_h, g_j, g_k are the cost functions for the switching sequences of *h, j* and *k*. $i_{(h,j,k)-\alpha}$ and $i_{(h,j,k)-\beta}$, are theα-β currents for the switching sequences *h, j* and *k*. In this equation (*) mean the reference values. The duty cycles to achieve these currents are then calculated using these cost functions. The higher the cost function value the lower will be the duty cycle for that specific switching sequence. The duty cycles of the active vectors are calculated by solving equation 2.20 for *k* and the duty cycles can be expressed as shown in equations 2.21-2.23.

$$\begin{aligned} t_h &= k / g_h \\ t_j &= k / g_j \\ t_k &= k / g_k \\ t_h + t_j + t_k &= T_s \end{aligned} \tag{2.20}$$

$$t_h = \frac{g_j g_k}{g_h g_j + g_h g_k + g_j g_k} T_s \tag{2.21}$$

$$t_j = \frac{g_h g_k}{g_h g_j + g_h g_k + g_j g_k} T_s \tag{2.22}$$

$$t_k = \frac{g_h g_j}{g_h g_j + g_h g_k + g_j g_k} T_s \tag{2.23}$$

Where t_h, t_j and t_k are the duty cycles for the switching vector *h, j* and *k* as shown in Figure 2.27. The total duty cycle for this triangle is then calculated using:

$$G = t_h g_h + t_j g_j + t_k g_k \tag{2.24}$$

Where G is the total duty cycle for this specific sub sector. To achieve the minimum cost function the total cost functions for each available subsector are deduced. Then all the cost functions are compared with the previously achieved cost functions and the lowest one will be selected to achieve minimum error in the next sampling interval [87, 91, 92]. A suitable switching sequence is then designed in accordance with the SVM algorithm to have minimum switching losses. Using this algorithm the variable switching frequency problem of the model predictive control algorithm can be eliminated. Therefore the power quality for a given sampling time will significantly improve. The harmonics spectrum will cluster around the sampling frequency so it becomes easier to design passive filters.

2.4 Conclusion

This chapter has presented an introduction to multilevel converter topologies and a few popular multilevel modulation techniques. Three primary multilevel converters, diode clamped, flying capacitor and cascaded topologies are described in brief. A few emerging topologies such as modular multilevel converter along with the hybrid converters have also been reported in this chapter.

A few popular multilevel modulation techniques have also been discussed to control the output voltage of multilevel voltage source converters. Finally, a model predictive control algorithm is described along with the challenges due to the variable switching frequency of the classic predictive control. A solution to the variable switching frequency is also discussed in this section.

Among all the topologies and modulation schemes the cascade dual two-level inverter will be discussed further in this thesis as this converter shows redundancy as well as can achieve multilevel output voltage without DC link voltage deviation, compared to NPC topologies. A space vector modulation scheme, as well as predictive controller, will be used to modulate and control the dual inverter system as these schemes will allow control over the selection of redundant switching states.

Chapter 3

Dual Two-Level Inverter

This chapter introduces a class of three phase inverter topologies known as dual inverters. The converter topology supplies both ends of the load thus the converter can achieve multilevel output voltage waveforms. A power stage diagram of dual two-level three phase inverter is shown in Figure 3.1. The dual inverter topology provides some redundancy due to the arrangement of the topology. The converter arrangement also has good DC link voltage utilisation and therefore reduces the blocking voltage requirement for the power semiconductor devices in a similar way to a multilevel converter.

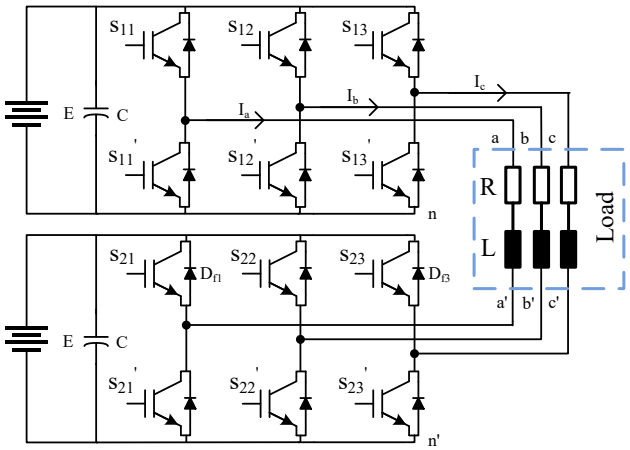
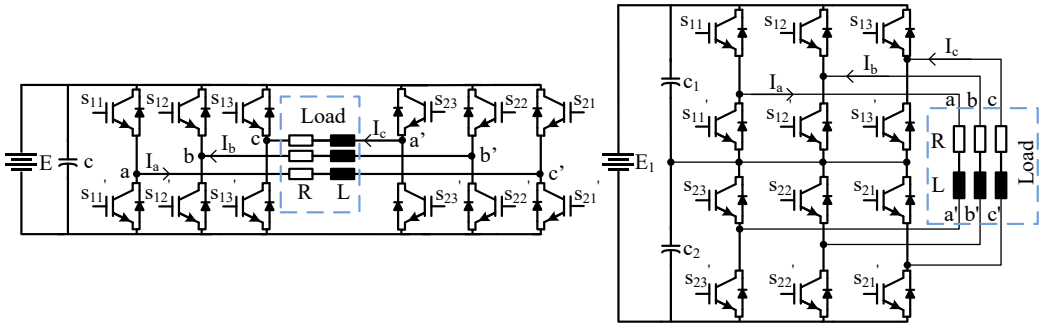


Figure 3.1 Dual two-level inverter with isolated sources.

3.1 Topology description

The dual two-level inverter consists of two standard 2-level inverters, each with isolated DC sources. The isolation of the sources is required to eliminate the path of common mode current flow through the system [50, 93]. The dual two-level inverter can also be supplied with a single source where series and parallel configurations are available. In Figure 3.2(b) the series configuration is obtained by splitting the DC

bus using two series capacitors [94]. Series connected topologies suffer from unbalanced DC voltages due to common mode current flow through the midpoint of the DC bus capacitors. Figure 3.2(a) shows the parallel configuration utilising single DC source. The parallel connected systems suffer from the huge common mode current flow, therefore the RMS current amplitude will increase without contributing toward the output power. For these reasons dual two-level inverters usually require isolated DC supplies.



(a) (b)

Figure 3.2 Dual two-level inverter with single source (a) series configuration (b) parallel configuration.

3.2 Applications of dual inverter

The application of dual inverter is advantageous where independent voltage sources are inherent. Such applications include Electric Vehicles (EV) and Hybrid Electric Vehicles (HEV)[95]. In battery powered electric vehicles the battery stack can be divided into two parts to supply both the converters and for HEV both the converters can be supplied with two separate generators, thus no isolation transformer will be required [95]. The other advantageous applications are grid connected photovoltaic applications. The converter topology for a grid connected application is shown in Figure 3.3. The converters can be supplied with two separate PV arrays or a battery bank can be connected to one of the bridges to store the energy[96-99]. In both cases, the converter topology is connected to an open phase transformer and the secondary of the transformer is connected to the grid. The dual converter topology is also used for electric ship propulsion, where one of the bridge converters is connected to a capacitor bank and other bridge is supplying all the required power. The power supplying converter is modulated to work as six step mode thus switching losses are reduced [100, 101].

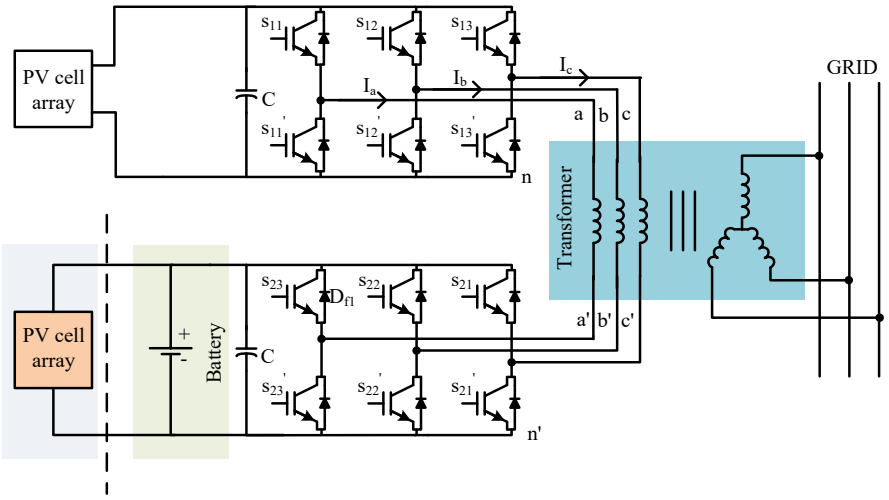


Figure 3.3 Dual inverter for PV applications.

3.3 Analysis of the system

The dual two-level inverter utilises twelve switching semiconductor devices (usually IGBTs or MOSFETs) and twelve antiparallel diodes. There are eight switching states produced by each of the two-level converters. Using two of them increases the number of switching states to 64:

$$N_{states} = 2^3 * 2^3 = 64 \tag{3.1}$$

Among the 64 vector states generated by the converter topology, there are 8 null vectors, and rest of them are active vectors. To identify the voltages across the load the dual inverter circuit can be analysed[94], as shown in Figure 3.4. *Ea* and *Eb* are the DC link voltages of the converters, both are equal in this example:

$$E_a = E_b \tag{3.2}$$

The voltages labelled as V_{12a}, V_{23a}, V_{31a} and V_{12b}, V_{23b}, V_{31b} in Figure 3.4 are the line voltages produced by '*Inverter a*' and '*Inverter b*' respectively, as shown in Figure 3.4. The voltages across the load V_1, V_2 and V_3 can be calculated as

$$\begin{aligned} V_1 - V_2 &= V_{12a} - V_{12b} \\ V_2 - V_3 &= V_{23a} - V_{23b} \\ V_3 - V_1 &= V_{31a} - V_{31b} \end{aligned} \tag{3.3}$$

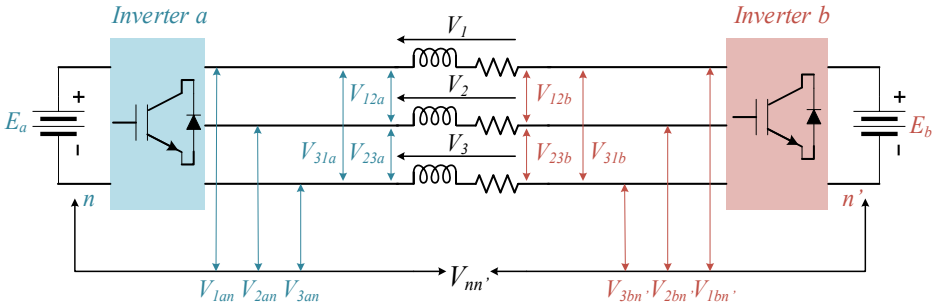


Figure 3.4 Dual inverter voltage states.

If the sources are isolated and the converter is supplying a balanced three phase load, then the sum of the three phase voltages will become zero.

$$V_1 + V_2 + V_3 = 0 \tag{3.4}$$

Considering a balanced three phase load the equation 3.3 can be rearranged as:

$$\begin{aligned} V_1 &= \frac{V_{12a} - V_{31a}}{3} - \frac{V_{12b} - V_{31b}}{3} \\ V_2 &= \frac{V_{23a} - V_{12a}}{3} - \frac{V_{23b} - V_{12b}}{3} \\ V_3 &= \frac{V_{31a} - V_{23a}}{3} - \frac{V_{31b} - V_{23b}}{3} \end{aligned} \tag{3.5}$$

The phase voltages generated by each converter can be given in terms of the line voltages produced by the associated converters.

$$\begin{aligned} V_{1a} &= \frac{V_{12a} - V_{31a}}{3} \\ V_{2a} &= \frac{V_{23a} - V_{12a}}{3} \\ V_{3a} &= \frac{V_{31a} - V_{23a}}{3} \end{aligned} \tag{3.6}$$

$$\begin{aligned} V_{1b} &= \frac{V_{12b} - V_{31b}}{3} \\ V_{2b} &= \frac{V_{23b} - V_{12b}}{3} \\ V_{3b} &= \frac{V_{31b} - V_{23b}}{3} \end{aligned} \tag{3.7}$$

In equations 3.6 – 3.7V_{1a}, V_{2a}, V_{3a} and V_{1b}, V_{2b}, V_{3b} are the phase voltages for '*Inverter a*' and '*Inverter b*' respectively. Substituting equations 3.6 – 3.7 into equation 3.5:

$$\begin{aligned} V_1 &= V_{1a} - V_{1b} \\ V_2 &= V_{2a} - V_{2b} \\ V_3 &= V_{3a} - V_{3b} \end{aligned} \tag{3.8}$$

It is evident from equation 3.8 that the voltage across the load or the phase voltage of dual inverter topology is the difference between the phase voltages produced by each of the converters. To achieve the maximum available voltage across the load the converter switching combinations are selected in such a way that the average generated voltages across the load are completely out of phase so that they sum across the load.

The common mode voltage has not yet been considered in this section. The common mode voltage for each of the converters and the total common mode voltage of the converter can be calculated as:

$$\begin{aligned} V_{0a} &= \frac{V_{1an} + V_{2an} + V_{3an}}{3} \\ V_{0b} &= \frac{V_{1bn'} + V_{2bn'} + V_{3bn'}}{3} \\ V_0 &= \frac{V_1 + V_2 + V_3}{3} \end{aligned} \tag{3.9}$$

Where, V_{0a}, V_{0b} and V_0 are the common mode voltages of the individual inverters and the load combined common mode voltage. By applying Kirchhoff's voltage law to the close path of each phase, the leg voltages of the *Inverter a* can be written as

$$\begin{aligned} V_{1an} &= V_1 + V_{1bn'} + V_{nn'} \\ V_{2an} &= V_2 + V_{2bn'} + V_{nn'} \\ V_{3an} &= V_3 + V_{3bn'} + V_{nn'} \end{aligned} \tag{3.10}$$

Where $V_{nn'}$ is the total common mode voltage produced by the converter system. The expression in equation 3.10 can be rearranged and presented in terms of the total common mode voltage:

$$V_{nn'} = \frac{V_{1an} + V_{2an} + V_{3an}}{3} - \frac{V_{1bn'} + V_{2bn'} + V_{3bn'}}{3} - \frac{V_1 + V_2 + V_3}{3} \tag{3.11}$$

To simplify equation 3.11 it can be assumed that the load is symmetrical and linear. Therefore the sum of load voltages and load currents will become zero. The common mode equation can, therefore, be written as:

$$V_{nn'} = \frac{V_{1an} + V_{2an} + V_{3an}}{3} - \frac{V_{1bn'} + V_{2bn'} + V_{3bn'}}{3} = V_{0a} - V_{0b} \tag{3.12}$$

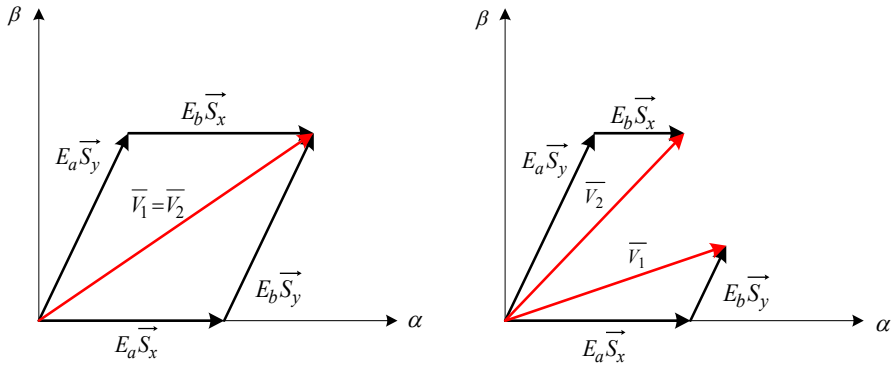
The expression shown in equation 3.12 suggests that the common mode voltage produced by the converter is the difference between the common mode voltages of each converter[94].

3.4 Dual inverter with asymmetric voltage sources

The dual inverter described in this thesis so far is realising with both the converters are supplied from equal voltage sources. Using unequal voltage sources the converter operation changes significantly. A vector diagram is shown in Figure 3.5 comparing the voltage vector generation for equal and unequal ($E_a = 2E_b$) voltage sources. The voltage vector diagrams are drawn by considering the complex switching sequence $\overline{S}_{1x}$ and $\overline{S}_{2x}$, these complex switching sequences are described for the first converter as $\overline{S}_{11} = 1, \overline{S}_{12} = 0, \overline{S}_{13} = 0;$ and for the second converter as $\overline{S}_{21} = 1, \overline{S}_{22} = 1, \overline{S}_{23} = 0;$ shown in Figure 3.1. The output voltages are given by equation 3.13 and representative diagrams are shown in Figure 3.5.

$$\begin{aligned} \overline{V}_1 &= E_a \overline{S}_x + E_b \overline{S}_y \\ \overline{V}_2 &= E_a \overline{S}_y + E_b \overline{S}_x \end{aligned} \tag{3.13}$$

The complex vectors associated with the switching combinations shows the direction of the complex voltage vector positions. In this case, the voltage vectors are superimposed on the *d*-axis and the other one is leading 60^o from the *d*-axis. The amplitude of the voltage vectors is defined by the source value. It can be seen that if both the sources are equal then the voltage vectors are equal in magnitude and angle. If the voltages are unequal, for example, a ratio of 2:1, then additional vectors can be seen, as shown in Figure 3.5 (b). It is evident from the analysis that some of these vectors can be considered as redundant vectors and these can be decoupled using asymmetric voltage sources to increase the available number of output voltage vectors.

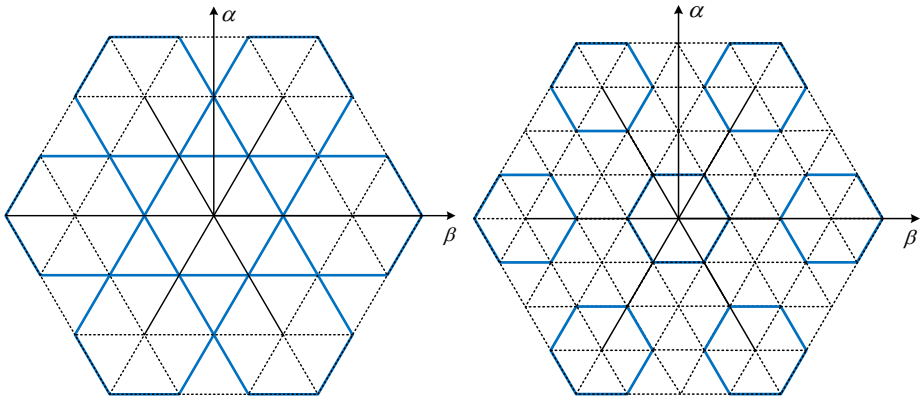


(a) (b)

Figure 3.5 Voltage vector compositions (a) equal voltage sources (b) asymmetrical sources ratio of (2:1).

A space vector diagrams for the dual two-level inverter with unequal voltage sources with a ratio of 2:1 is shown in Figure 3.6 (a). The converter system with unequal voltage sources with a ratio of 2:1 produces 37 voltage vectors which are symmetrical and evenly distributed in the α-β plane.

The vector diagram is shown in Figure 3.6 (b) is drawn considering the use of asymmetrical sources with a ratio of 3:1. This converter topology can produce 48 voltage vectors which are symmetrical but unevenly distributed among the α-β plane. In this particular configuration, there are some regions where choosing the nearest three vectors are challenging and this may introduce some additional harmonics into the output waveform. Moreover, there will be a minimum number of redundant states and therefore at lower modulation index, the inverter will overcharge the lower voltage capacitors in some regions. This converter has some challenges which lay outside the scope of the work described in this thesis.



(a) (b)

Figure 3.6 Space vector diagram of dual two-level inverter with asymmetric sources (a) sources ratio of 2:1 (b) sources ratio of 3:1.

3.5 Modulation strategies

A dual two-level inverter can be modulated using sine triangular modulation scheme [102] or traditional Space Vector Modulation (SVM) [45, 50, 93, 103, 104]. This section will present commonly used modulation schemes to control the fundamental output voltage of the converter.

3.5.1 Carrier based modulation

The simplest way to modulate a dual inverter is to use a single carrier with two references. Each reference is equal to half of the desired output voltage and has 180^{o} phase shift from the other. In this way, the output waveforms from each converter will add up across the load to give the desired voltage waveform. This modulation scheme is shown in Figure 3.7.

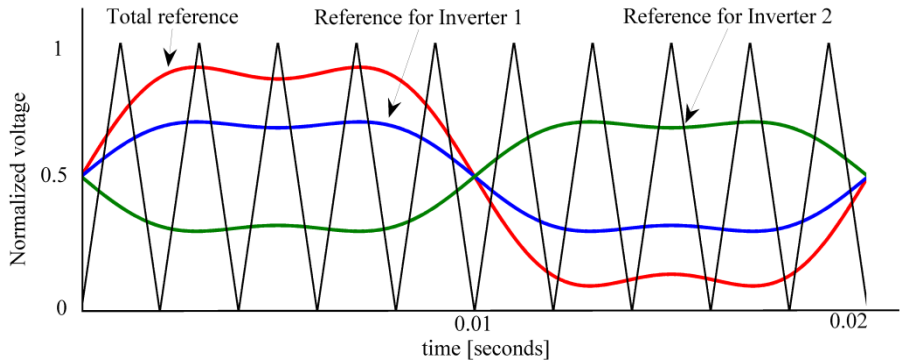


Figure 3.7 Carrier based modulation scheme where two references are used to modulate dual inverter with equal voltage sources.

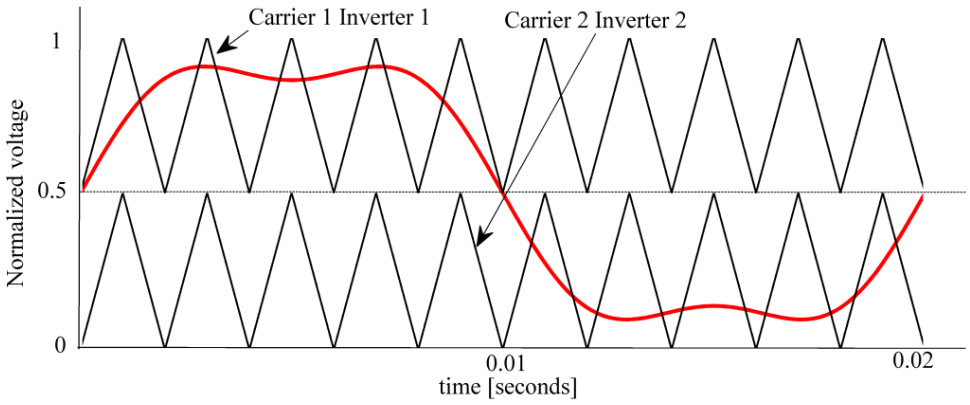


Figure 3.8 Carrier based modulation scheme where two carrier signals are used to modulate dual inverter with equal voltage sources.

Other ways of modulating the converter include utilising level shifted multi-carrier techniques [105]. Two carriers are used to form the three-level output for a dual inverter with equal sources, as shown in Figure 3.8. In this example, the two carriers will control the two converters independently. The dual inverter with asymmetric voltage sources (source ratio of 2:1) can produce four distinct voltage levels and therefore needs three carrier signals. This modulation method is known to overcharge the DC link of the lower voltage inverter. This overcharging can be prevented by using controlled DC link supplies; using additional hardware or by excluding the switching sequences that cause overcharging.

A multi-carrier modulation technique has been defined [102, 105]in which the switching states are defined using simple mathematical terms applied to a logical variable A. Variable A is a function of the reference and carrier signals corresponding to zone k and phase i, as shown in equation 3.14 and in Figure 3.9.

$$A_{ki} = \begin{cases} if\ v_i^* > C_k & then\ 1 \\ if\ v_i^* < C_k & then\ 0 \end{cases} \tag{3.14}$$

Where v_i^* is the reference voltage for i^{th} phase, C_k is carrier signals corresponds to the zone k, where k = 1, 2, 3. The relation between switching signals and logical variables can be written as

$$s_{1i} = A_{2i}$$
$$s_{2i} = NOT(A_{1i}) + A_{2i}NOT(A_{3i}) \quad (3.15)$$

Where, s_{1i} and s_{2i} are the switching signals for the i^{th} phases for *Inverter a* and *Inverter b* respectively.

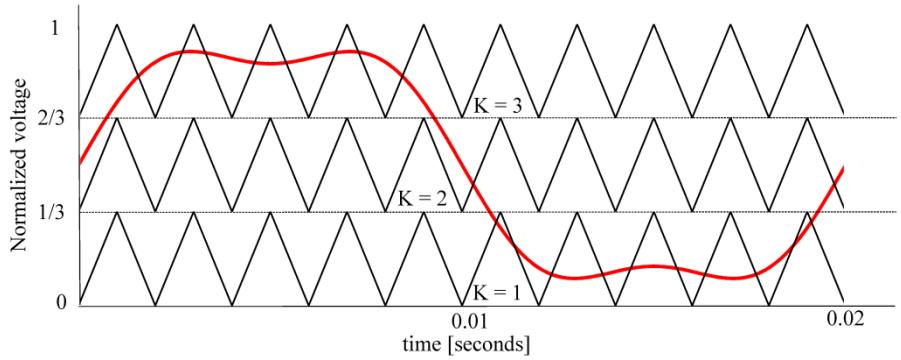


Figure 3.9 Carrier based modulation scheme where three references are used to modulate dual inverter with unequal voltage sources.

Table 3.1 Relationship between converter operation and reference zone.

Zone (k)	Range	VSI-1	VSI-2
1	0 to 1/3 V_{dc}	Holds 0	PWM
2	1/3 V_{dc} to 2/3 V_{dc}	PWM	PWM
3	2/3 V_{dc} to V_{dc}	Holds E_a	PWM

A table is constructed to show the relation between the converter states and the reference zones, Table 3.1. It can be seen that the second (lower voltage) converter is switching faster than the higher voltage converter to reduce overall losses. Figure 3.9 shows the level shifted modulation scheme and the associated reference zones.

3.5.2 Space vector modulation

The dual three phase inverter topology can be modulated using Space Vector Modulation scheme (SVM). In SVM schemes one has the freedom to select specific switching sequences [45, 50, 93, 103, 106-110]. In this section, a brief introduction to space vector modulation for the dual inverter topology is provided.

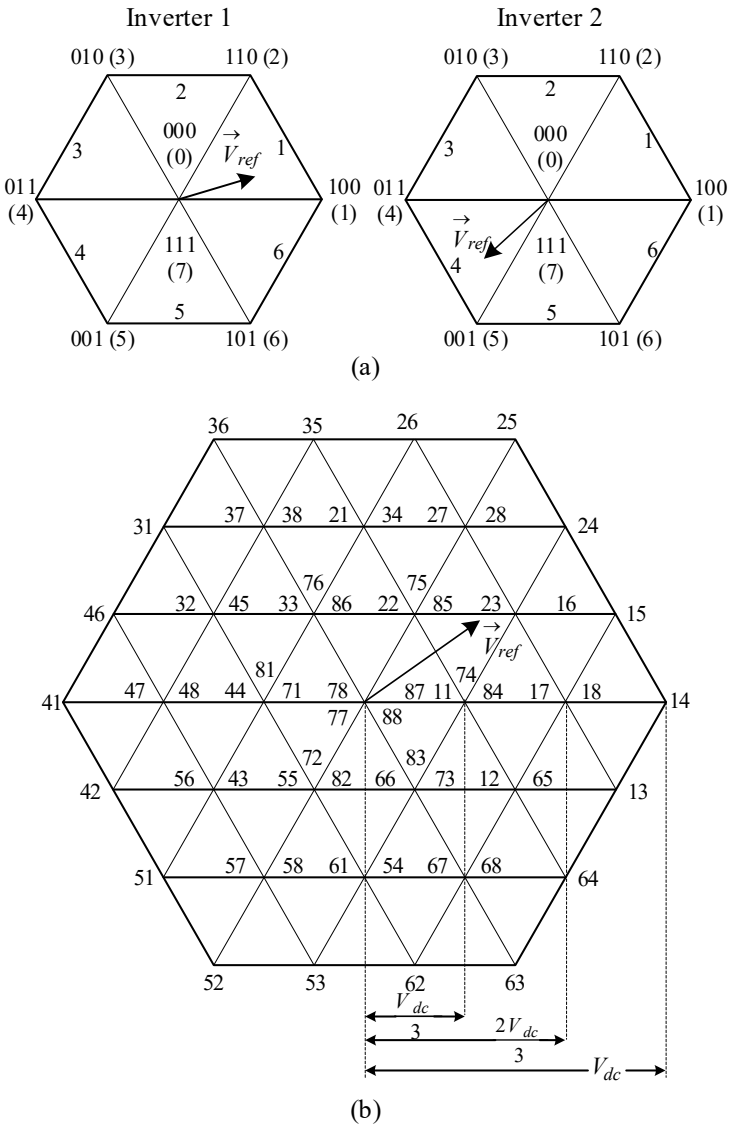


Figure 3.10 Space vector diagram of dual inverter with voltage ratio of 2:1 (a) individual inverters (b) dual inverter system.

A space vector diagram of for the individual inverters and the total space vector diagram of the dual inverter system for a source ratio of 2:1 are shown in Figure 3.10. As an example, a decoupled space vector modulation strategy is described for the dual inverter topology. Switching combinations are selected in such a way that the generated voltages for each of the converters are 180-degree phase shifted from the other, as shown in Figure 3.10 (a). The voltages will add across the load to match the overall reference, as shown in Figure 3.10 (b). The reference voltage location inside the vector diagram is identified using the angle of the reference voltage as described in Chapter 2. The process of identifying reference voltage subsector location is shown in equations 3.16 to 3.17 and is tabulated in Table 3.2. The associated equations are

derived using Figure 3.11. In the figure, the reference voltage (V_{ref}) or the modulation index (m) is divided into two components k_1 and k_2 which are 60^o apart from the other. These values are then compared to find the location of the subsector where the reference voltage resides, shown in Table 3.2.

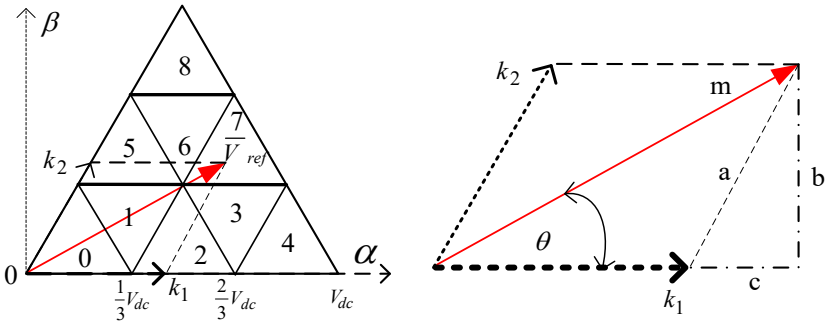


Figure 3.11 Subsector identification diagram.

$$a = k_2 = \frac{b}{\sin(\pi/3)} = \frac{2}{\sqrt{3}}b = \frac{2}{\sqrt{3}}m\sin(\theta) \tag{3.16}$$

$$k_1 = m\cos(\theta) - \left(\frac{2}{\sqrt{3}}m\sin(\theta)\right)\cos\left(\frac{\pi}{3}\right)$$
$$k_1 = m\left(\cos(\theta) - \frac{\sin(\theta)}{\sqrt{3}}\right) \tag{3.17}$$

where k_1 and k_2 are the components of the reference voltage and m refers to the modulation index:

$$m = \frac{\sqrt{3}V_{ref}}{V_{dc}} \tag{3.18}$$

The switching time is calculated using the volt second balancing principle. An example of how to calculate dwell time is shown in Chapter 2 in equations 2.8 to 2.15. The final stage of the SVM algorithm is to design a switching sequence; in this case, a seven segment switching sequence is used, as shown in Figure 3.12.

Table 3.2 Subsector identification.

Subsector	Identification criteria
0	$if\,(k_1, k_2) < \frac{1}{3}\ \&\ (k_1 + k_2) \le \frac{1}{3})$
1	$if\,(k_1, k_2) < \frac{1}{3}\ \&\ (k_1 + k_2) > \frac{1}{3})$
2	$if\,(k_1 < \frac{2}{3}\ \&\ k_2 < \frac{1}{3}\ \&\ (k_1 + k_2) < \frac{2}{3})$
3	$if\,(k_1 < \frac{2}{3}\ \&\ k_2 < \frac{1}{3}\ \&\ (k_1 + k_2) > \frac{2}{3})$
4	$if\,(k_1 > \frac{2}{3})$
5	$if\,(k_1 < \frac{1}{3}\ \&\ k_2 > \frac{1}{3}\ \&\ (k_1 + k_2) < \frac{2}{3})$
6	$if\,(k_1 < \frac{1}{3}\ \&\ k_2 < \frac{2}{3}\ \&\ (k_1 + k_2) > \frac{2}{3})$
7	$if\,(k_1 < \frac{2}{3}\ \&\ k_2 < \frac{2}{3}\ \&\ (k_1 + k_2) > \frac{2}{3})$
8	$if\,(k_1 > \frac{2}{3})$

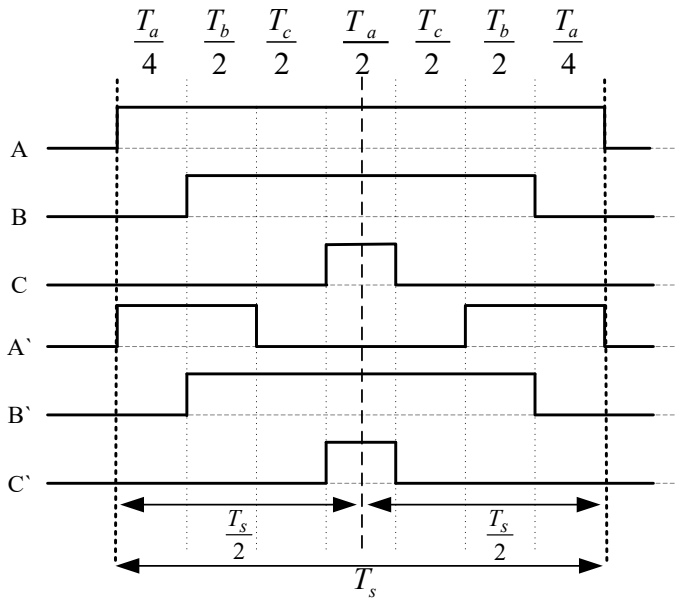


Figure 3.12 Seven segment switching sequence.

3.6 Control Strategies for dual inverter

Traditional dual inverter topologies using isolated DC sources have been analysed with various modulation schemes to achieve multilevel output voltage waveform [45, 50, 93, 94, 102-107, 109-116]. An improved PWM switching strategy was proposed to achieve a minimum number of switching commutations [45]. A method was also presented to eliminate common mode voltage [113], sharing of power between two converters and to boost the voltage for drive operation [95, 109, 117, 118]. There are other advantageous techniques, such as modulating one converter to operate as six step mode and use the other converter for signal conditioning [100]. All these techniques show advantages depending on their applications. In this section, some of these control strategies are briefly introduced.

3.6.1 Dual inverter to eliminate common mode voltage

The dual two-level inverter has 64 switching states. Using equal DC link voltage the converter can be modelled using 19 switching states, the rest of them are redundant states.

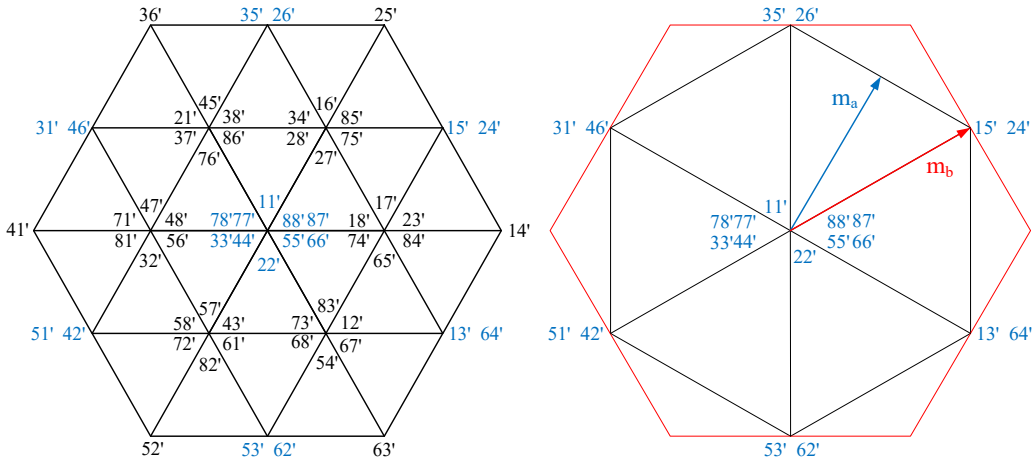


Figure 3.13 Space vector diagram of (a) dual inverter with equal source ratio (b) dual inverter for common mode elimination.

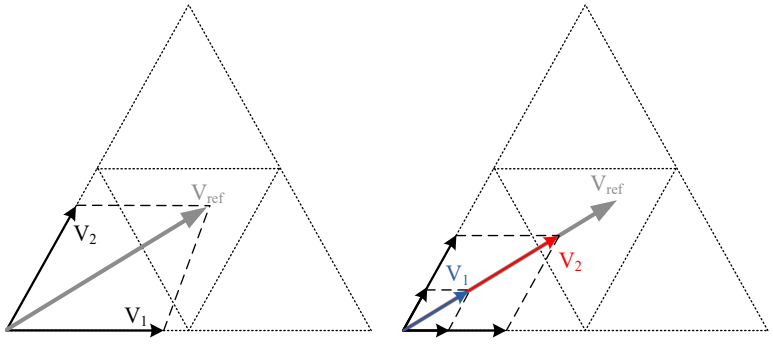
In [107, 110]is has been shown that some of the switching combinations produce equal common mode voltages in both the converters. Due to the arrangement of the converters connections the equal common mode voltages will cancel at load terminal. A vector diagram of the dual inverter with equal voltage sources is shown

in Figure3.13(a), where the switching states with zero common mode voltages are marked in blue. Using these switching states the converter system can be operated with a single source.

It can also be seen from the figure that if only the common mode elimination switching sequences are used then the system can only achieve two-level output voltage waveform, as shown in Figure 3.13 (b). The other drawback of this converter is the lower than ideal DC link utilisation.

3.6.2 Dual inverter with power sharing capability

The dual inverter topology can be used to regulate power flow between two sources. This requirement can be used to equalise the state of charge of two batteries or can be used to exploit the characteristics of two sources[95].The traditional modulation technique for the symmetrical dual inverter system have symmetrical power sharing capabilities, asymmetrical sharing of power can be achieved by decomposing the reference vectors into distinctive collinear vectors [95, 109, 117, 119].



(a) (b)

Figure 3.14 Vector diagram (a) traditional modulation (b) modified modulation to achieve power sharing.

Figure 3.14(a) shows the reference vector generation using conventional modulation and Figure 3.14(b) show the collinear voltage vectors for power sharing. It is shown in [95, 119] that the asymmetric power sharing capability is high at low modulation index and low at higher modulation index. This is because each inverter generates a part of the total output voltage, if the modulation index is less than 0.5 then one of the converters can produce all the required voltage (power) or both

inverters can share the voltage (power). In this case, the ratio of voltage sharing can be between0 to 1.If the modulation index is higher than 0.5 then only one inverter is not enough to produce the required voltage (power), thus the other inverter is required to share a part of the voltage to match the overall reference voltage. This is because the power sharing capability reduces with the increase of modulation index.

3.6.3 Dual inverter with one bridge floating

The floating bridge capacitor for the dual inverter can be used for various purposes. For example, the floating capacitor has been used to supply reactive voltage to distribute the voltage requirement for high speed machines [118] and to achieve multilevel voltage waveforms. The use of the floating bridge inverter to supply reactive voltage components arise due to the voltage limitation for high speed drives. In high speed operation, the back Electromotive Force (EMF) is dominant and therefore requires higher voltage than the traditional 50Hz machine. In [114, 115] a dual inverter with a floating bridge was utilised to share the voltage required for the drive operation. The floating converter was used to supply reactive voltage and the capacitor voltage was regulated using a PI controller which controls the power flow in and out of the floating capacitor.

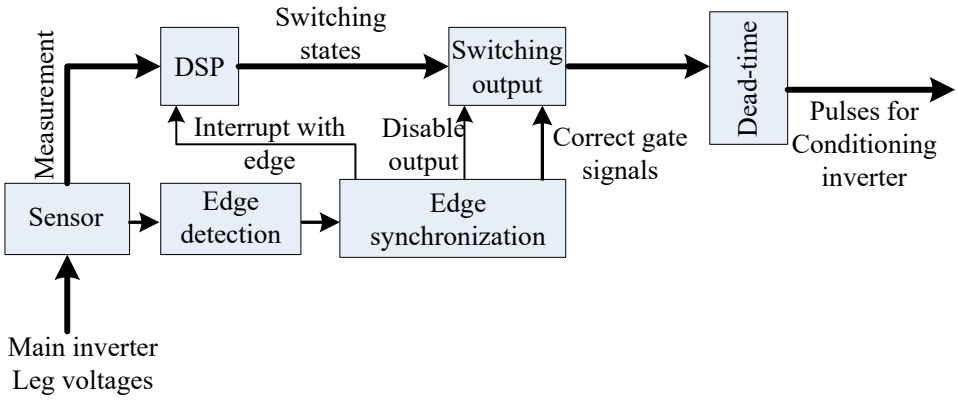


Figure 3.15 Hardware implementation block diagram of the conditioning inverter.

The multilevel operation with the dual inverter with one bridge floating was presented in [100, 101], where a commercial off the shelf converter was used to supply all the power and the floating inverter was used to enhance the output using a PWM waveform. The main converter worked in a six step mode of operation and the

secondary converter voltage was controlled using a PI based controller. A block diagram of the hardware implementation of the floating inverter shown in Figure 3.15.

It can be seen from Figure 3.15 that to control the converter the leg voltages of the primary converter is measured and the primary converter voltage edges are detected using additional hardware. The floating (conditioning) converter then applies switching pulses which modify the output waveform. The system includes additional measurement boards, an edge detection circuit and requires complex calculations in order to have proper control over the converter.

3.6.4 Dual inverter with asymmetric sources

The dual inverter with asymmetric sources can be challenging to implement and there are only a few research papers on this topic. In one paper, the authors show that the converter overcharges the lower voltage source for a voltage ratio of 2:1[50]. The authors also presented a method to overcome the overcharging of the lower voltage source by introducing three isolation transformers and associated voltage sources to maintain the voltage ratio of 1:2:1, as shown in Figure 3.16.

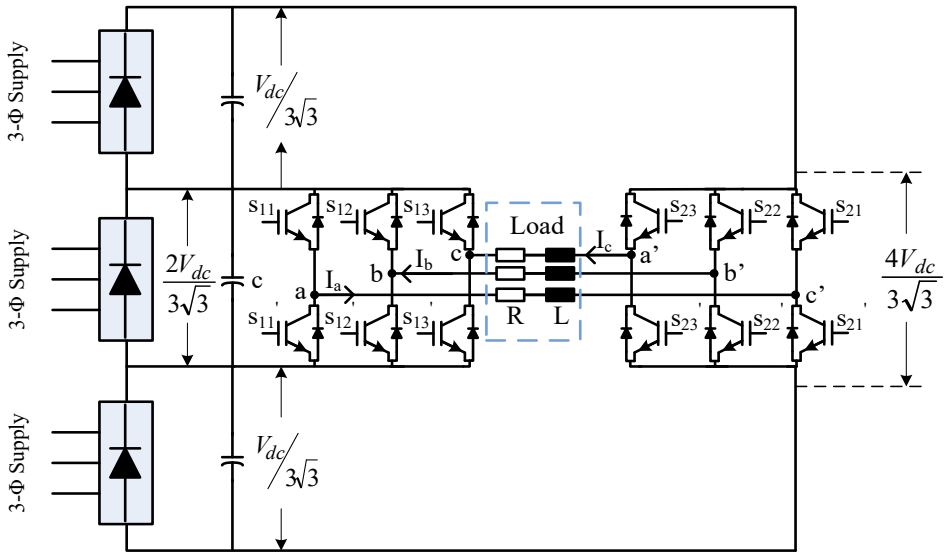


Figure 3.16 Dual inverter with asymmetric voltage sources with three isolated supplies.

This modified topology can achieve four-level output voltage waveforms and the capacitor overcharging problem was eliminated with the expense of additional

isolation transformers. It has also been claimed that dual inverter with asymmetric voltage sources can also be used to suppress and even eliminate specific harmonic content in motor drive applications [120]. The DC link voltage ratio used for this topology was 1:0.366 and the modulation scheme can remove 5^{th} and 7^{th} order harmonics as well as suppressing the $11^{th}$and 13^{th} order harmonics. A vector diagram of this modulation process is shown in Figure 3.17.

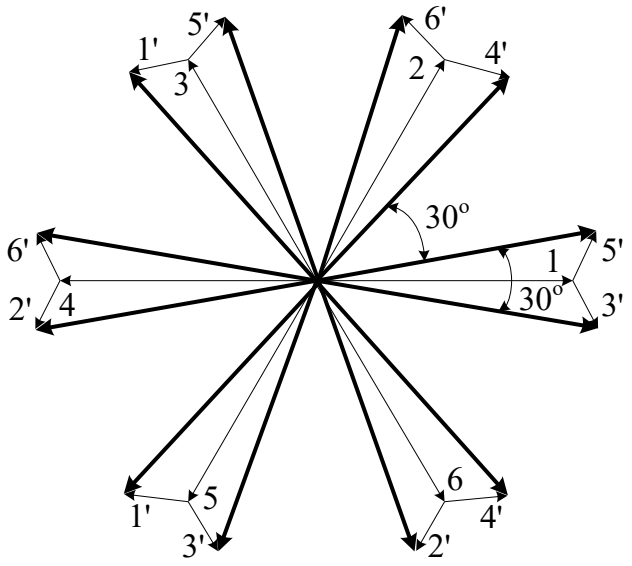


Figure 3.17 Selected switching combinations of the vector positions for both the inverters for a voltage ratio of 1:0.366.

3.7 Advantages and disadvantages of dual inverter system

The dual three phase two-level inverter topology utilises two three phase inverter to achieve multilevel output voltage waveforms. The dual inverter topology can produce nine distinct voltage levels across the load, similar to a three-level converter and has received research attention due to the simplicity of power stage. The circuit implementation requires fewer capacitors than the flying capacitor topology [121], fewer isolated supply than a three phase H-bridge converter [43] and require fewer diodes than the three-level NPC converter [122].

The dual inverter with a DC link voltage ratio of 2:1 can achieve 13 voltage levels across the load, similar to a traditional four-level converter topology[50]. This topology, however, suffers from the overcharging of the lower DC link voltage, this issue can be avoided by selecting some specific switching sequences. The voltage

levels can be increased by increasing the DC link voltage ratio to 3:1, but this will increase the complexity of modulation techniques due to uneven distribution of voltage vectors.

Although the dual inverter shows advantages over the single sided converter topologies, there are major drawbacks of this system. Due to the arrangement of the topology, the common mode current will flow through the system. To avoid common mode current flow isolated supplies are used, thereby increasing size, weight and losses of the system. The other challenge occurs during asymmetric voltage source operation, the lower voltage converter will again overcharge.

3.8 Conclusion

This chapter has presented a brief review of the dual two-level inverter topology. A few traditional modulation schemes have been presented for converter topologies with both symmetric and asymmetric voltage sources. Popular control strategies including common mode voltage elimination, power sharing, floating bridge topology as well as control techniques for a dual inverter with asymmetric voltage sources are described in brief. Finally, the advantage and disadvantages of the dual two-level inverters have been presented. The converter has advantages in applications where isolated supplies are available, such applications are electric and more electric vehicles [95] as well as photovoltaic applications [96-99, 123].

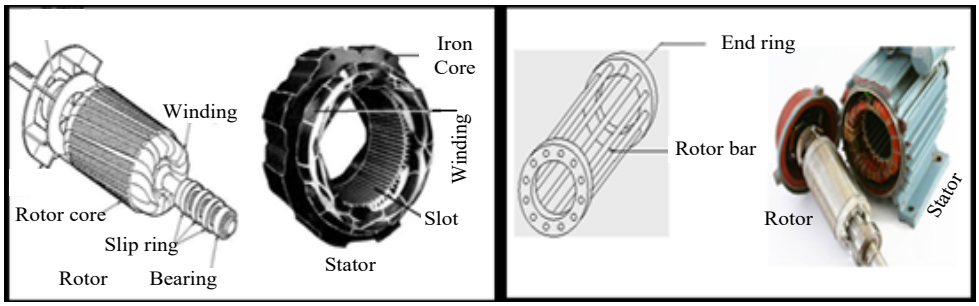
Chapter 4

Open End Winding Induction Motor Drive

This chapter presents a detailed analysis of traditional open end winding Induction Motor (IM) drive. This analysis will be essential to focus on the losses in different parts of the drive system and can lead to the improvement in the existing topology. To determine the losses an induction motor drive was modelled incorporating space harmonics using a simulation platform (Matlab & SimuLink). The losses of the converter were determined using the component manufacturer's data. The machine and transformer losses were calculated using Finite Element (FE) software (Infolytica MagNet).

4.1 Induction machine

Three phase AC machines operate using the principle of rotating field which is developed by spatially shifted individual phases along the circumference of the machine. This is true for any machine with three or more phases regardless of the size of the machine [124, 125]. For a three phase machine, the individual phases are placed 120^{o} apart from the other. This section deals with the modelling and simulation of three phase Squirrel Cage Induction Machine (SCIM).



(a) (b)

Figure 4.1 Rotor and stator construction (a) wound rotor induction motor (b) SCIM

The stator of a Wound Rotor Induction Motor (WRIM) is same as the SCIM, but instead of shorted rotor bars, it has copper winding connected through slip rings. Structures of both machines are shown in Figure 4.1.

4.1.1 Modelling of three phase induction motor

In this section, a mathematical model of a three phase induction machine is developed. The goal is to find a set of differential equation to map the dynamics of the induction machine in order to analyse it. An equivalent circuit of a squirrel cage induction motor is shown in Figure 4.2.

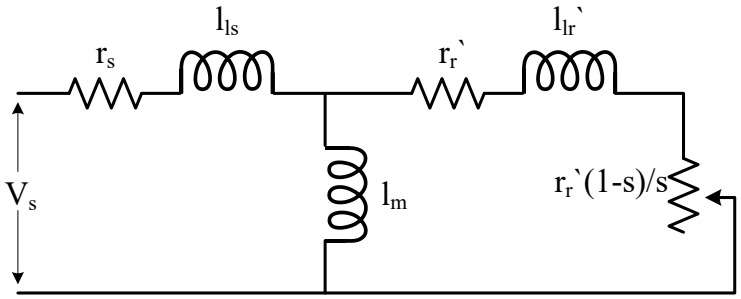


Figure 4.2 Equivalent circuit of squirrel cage induction motor.

An ideal machine model is subject to a number of simplifying assumptions [125]. They are:

- All individual phase windings are identical and symmetrical. This means that spatial displacement of two consecutive phases is exactly 120 degrees.
- All the spatial Magnetomotive Force (MMF) harmonics, except the fundamental is neglected.
- Impact of slotting of stator (rotor) is neglected as a uniform airgap is assumed.
- Stator and rotor resistance, leakage reactance are considered constant with no effect of temperature and frequency variation.
- Ferromagnetic and Eddy current losses are ignored.
- Frictional losses can be ignored.
- Stator and rotor turn ratio is assumed to be 1:1.

Since all the windings of a machine are resistive and inductive in nature, the voltage equilibrium equation of rotor and stator [126] can be written as:

$$\begin{bmatrix} V_{abc\_s} \\ V_{abc\_r} \end{bmatrix} = \begin{bmatrix} r_s & 0 \\ 0 & r_r \end{bmatrix} \cdot \begin{bmatrix} i_{abc\_s} \\ i_{abc\_r} \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \psi_{abc\_s} \\ \psi_{abc\_r} \end{bmatrix} \tag{4.1}$$

$$\begin{bmatrix} V_{abc\_s} \\ V_{abc\_r} \end{bmatrix} = \begin{bmatrix} r_s & 0 \\ 0 & r_r \end{bmatrix} \cdot \begin{bmatrix} i_{abc\_s} \\ i_{abc\_r} \end{bmatrix} + \frac{d}{dt} \left(\begin{bmatrix} l_s & l_{sr} \\ l_{sr}^T & l_r \end{bmatrix} \cdot \begin{bmatrix} i_{abc\_s} \\ i_{abc\_r} \end{bmatrix} \right) \tag{4.2}$$

Where, V_{abc_s}, V_{abc_r}, i_{abc_s} and i_{abc_r} are three phase stator voltage, rotor voltage stator current and rotor current respectively. The terms ψ_{abc_s} and ψ_{abc_r} specify three phase stator and rotor flux linkages. The rotor voltages will be zero '0' for SCIM due to the shorted rotor bars. The stator resistance, rotor resistance, stator inductance and rotor inductance matrices are denoted as r_s, r_r, l_s and l_r in equations 4.1 – 4.2, and the terms can be elaborated using equations 4.3 – 4.6. The term l_{sr} specify the stator to rotor mutual inductance and can be described using equation 4.11.

$$[r_s] = \begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix} \tag{4.3}$$

$$[r_r] = \begin{bmatrix} R_r & 0 & 0 \\ 0 & R_r & 0 \\ 0 & 0 & R_r \end{bmatrix} \tag{4.4}$$

$$[l_s] = \begin{bmatrix} L_{aa\_s} & L_{ab\_s} & L_{ac\_s} \\ L_{ba\_s} & L_{bb\_s} & L_{bc\_s} \\ L_{ca\_s} & L_{cb\_s} & l_{cc\_s} \end{bmatrix} \tag{4.5}$$

$$[l_r] = \begin{bmatrix} L_{aa\_r} & L_{ab\_r} & L_{ac\_r} \\ L_{ba\_r} & L_{bb\_r} & L_{bc\_r} \\ L_{ca\_r} & L_{cb\_r} & l_{cc\_r} \end{bmatrix} \tag{4.6}$$

Where L_{xx_s} and L_{xy_s} are the stator self and mutual inductance, whereas L_{xx_r} and L_{xy_r} are the rotor self and mutual inductances, here $xx = aa, bb, cc$ and $xy = ab, bc$ and ca. The windings in a three phase machine are equally displaced along the circumference of the machine, thus all three winding has equal mutual inductance. As all the phases are 120^o shifted from the other, the mutual inductances can be calculated using equations 4.7 – 4.8.

$$L_{ab\_s} = L_{bc\_s} = L_{ca\_s} = l_m \cos\left(\frac{2\pi}{3}\right) = -\frac{1}{2} l_m \tag{4.7}$$

$$L_{ab\_r} = L_{bc\_r} = L_{ca\_r} = l_m \cos\left(\frac{2\pi}{3}\right) = -\frac{1}{2} l_m \tag{4.8}$$

Where, l_m is the magnetising inductance. The self-inductances defined in equations 4.5 and in 4.6 are the addition of leakage inductance and magnetising inductance, hence the equations 4.5 - 4.6 can be rewritten as shown in equations 4.9 and 4.10.

$$[l_s] = \begin{bmatrix} l_{ls} + l_m & -\frac{1}{2} l_m & -\frac{1}{2} l_m \\ -\frac{1}{2} l_m & l_{ls} + l_m & -\frac{1}{2} l_m \\ -\frac{1}{2} l_m & -\frac{1}{2} l_m & l_{ls} + l_m \end{bmatrix} \tag{4.9}$$

$$[l_r] = \begin{bmatrix} l_{lr} + l_m & -\frac{1}{2} l_m & -\frac{1}{2} l_m \\ -\frac{1}{2} l_m & l_{lr} + l_m & -\frac{1}{2} l_m \\ -\frac{1}{2} l_m & -\frac{1}{2} l_m & l_{lr} + l_m \end{bmatrix} \tag{4.10}$$

$$[l_{sr}] = l_m \begin{bmatrix} \cos\theta_r & \cos\left(\theta_r + \frac{2\pi}{3}\right) & \cos\left(\theta_r - \frac{2\pi}{3}\right) \\ \cos\left(\theta_r - \frac{2\pi}{3}\right) & \cos\theta_r & \cos\left(\theta_r + \frac{2\pi}{3}\right) \\ \cos\left(\theta_r + \frac{2\pi}{3}\right) & \cos\left(\theta_r - \frac{2\pi}{3}\right) & \cos\theta_r \end{bmatrix} \tag{4.11}$$

The flux linkage of the machine can be defined as

$$\begin{bmatrix} \psi_{abcs} \\ \psi_{abcr} \end{bmatrix} = \begin{bmatrix} l_s & l_{\text{sr}} \\ l_{sr}^T & l_r \end{bmatrix} \begin{bmatrix} i_{abcs} \\ i_{abcr} \end{bmatrix} \tag{4.12}$$

$$\begin{bmatrix}\psi_{as}\\ \psi_{bs}\\ \psi_{cs}\\ \psi_{ar}\\ \psi_{br}\\ \psi_{cr}\end{bmatrix}=\begin{bmatrix} l_{ls}+l_m & -\frac{1}{2}l_m & -\frac{1}{2}l_m & l_m\cos\theta_r & l_m\cos\theta_{r+} & l_m\cos\theta_{r-}\\ -\frac{1}{2}l_m & l_{ls}+l_m & -\frac{1}{2}l_m & l_m\cos\theta_{r-} & l_m\cos\theta_r & l_m\cos\theta_{r+}\\ -\frac{1}{2}l_m & -\frac{1}{2}l_m & l_{ls}+l_m & l_m\cos\theta_{r+} & l_m\cos\theta_{r-} & l_m\cos\theta_r\\ l_m\cos\theta_r & l_m\cos\theta_{r-} & l_m\cos\theta_{r+} & l_{ls}+l_m & -\frac{1}{2}l_m & -\frac{1}{2}l_m\\ l_m\cos\theta_{r+} & l_m\cos\theta_r & l_m\cos\theta_{r-} & -\frac{1}{2}l_m & l_{ls}+l_m & -\frac{1}{2}l_m\\ l_m\cos\theta_{r-} & l_m\cos\theta_{r+} & l_m\cos\theta_r & -\frac{1}{2}l_m & -\frac{1}{2}l_m & l_{ls}+l_m \end{bmatrix}\times\begin{bmatrix}i_{as}\\ i_{bs}\\ i_{cs}\\ i_{ar}\\ i_{br}\\ i_{cr}\end{bmatrix} \tag{4.13}$$

In equation 4.13,

$$\theta_{r+}=\theta_r+\frac{2\pi}{3}\text{ and }\theta_{r-}=\theta_r-\frac{2\pi}{3}$$

The electromagnetic torque of the machine can be defined as [126]

$$T_e=\frac{p}{2}\begin{bmatrix}i_{abcs} & i_{abcr}\end{bmatrix}\frac{\Delta\begin{bmatrix}l_s & l_{\mathrm{sr}}\\ l_{sr}^T & l_r\end{bmatrix}}{\Delta\theta_r}\begin{bmatrix}i_{abcs}\\ i_{abcr}\end{bmatrix} \tag{4.14}$$

The stator and rotor inductances, l_s and l_r contain only constant elements, so the electromagnetic equation 4.14 can be simplified to:

$$T_e=\frac{p}{2}i_{abcs}^T\frac{\Delta l_{sr}(\theta_r)}{\Delta\theta_r}i_{abcr} \tag{4.15}$$

$$=-\frac{p}{2}l_m\begin{bmatrix}i_{as} & i_{bs} & i_{cs}\end{bmatrix}\begin{bmatrix}\sin\theta_r & \sin\left(\theta_r+\frac{2\pi}{3}\right) & \sin\left(\theta_r-\frac{2\pi}{3}\right)\\ \sin\left(\theta_r-\frac{2\pi}{3}\right) & \sin\theta_r & \sin\left(\theta_r+\frac{2\pi}{3}\right)\\ \sin\left(\theta_r+\frac{2\pi}{3}\right) & \sin\left(\theta_r-\frac{2\pi}{3}\right) & \sin\theta_r\end{bmatrix}\begin{bmatrix}i_{ar}\\ i_{br}\\ i_{cr}\end{bmatrix} \tag{4.16}$$

In addition, the mechanical equations of the machine must be considered [126]:

$$\frac{d\omega_r}{dt} = \frac{p}{2j}T_e - \frac{B_m}{j}\omega_r - \frac{p}{2j}T_L$$
$$\frac{d\theta_r}{dt} = \omega_r \tag{4.17}$$

Where T_L is the load torque and T_e is the electromagnetic torque produced by the machine,ω_r *and* θ_r are the electrical speed and angular position of the rotor. The rotor bearing friction and the inertia of the machine is denoted as B_m and j.

4.1.2 Induction machine model incorporating space harmonics

Stator windings are usually distributed over a few stator slots along the periphery of the stator, this type of winding is known as distributed winding. As there are a limited number of slots along the periphery of the stator the distribution is not perfectly sinusoidal, instead a staircase type of MMF distribution can be seen [125, 127], as shown in Figure 4.3. An ideal sinusoidal distribution is only possible if an infinite number of slots can be introduced, which is not practical. The harmonics in the flux density waveform of an induction machine are a result of the combination of the spatial distribution of the air gap MMF harmonics, (due to the discrete placement of the winding in slots) and the non-uniform permanence seen by these fields [128]. The existence of space harmonics is known to have a significant detrimental effect on the steady state and transient characteristics of the machine [129].

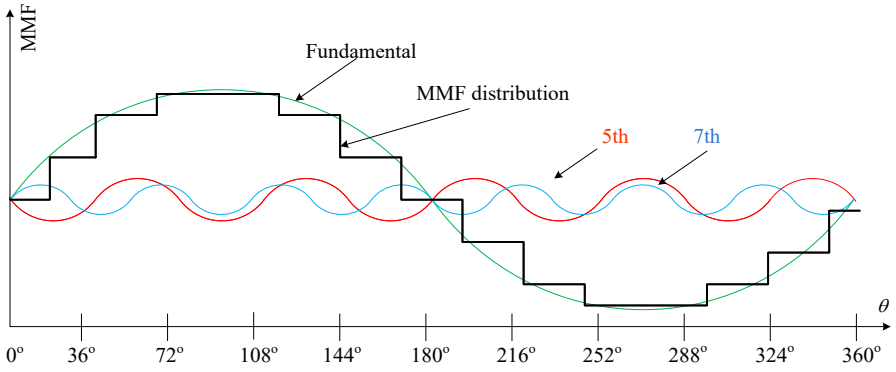


Figure 4.3 Ideal MMF distribution in the air gap.

For a balanced machine, the MMF distribution contains the fundamental and a family of space harmonics of order $h = 6k \pm 1$, where k is a positive integer. In a three phase machine, when sinusoidal currents flow through the windings, the resultant space harmonic fluxes will rotate at $(1/h)$ times the speed of the

fundamental wave. The space harmonic fluxes rotate in the same direction as the fundamental wave if $h = 6k + 1$ and in the opposite direction if $h = 6k - 1$ [128]. Heller [130] indicate that any induction motor may be represented by a series of mechanically connected induction motors which have different numbers of poles, whose stator windings are connected in series. This means that a space harmonic flux of order (h) is equivalent to the flux created in a machine with ($h \times p$) poles, here p is the number of poles. Therefore, more than one rotor circuit should be considered, one for each harmonic, and each with different numbers of poles. This type of approach can be used to model the space harmonic by adding to the equivalent circuit [125].

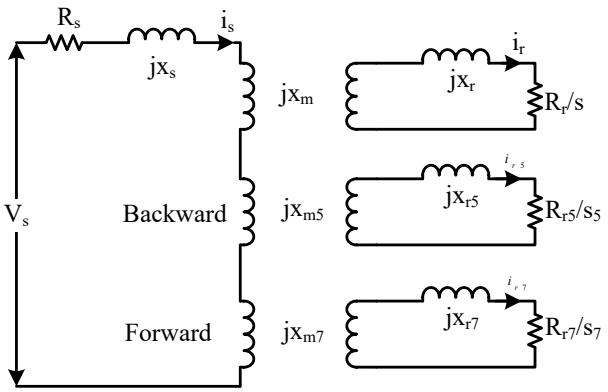


Figure 4.4 Conventional per-phase equivalent circuit (left) and modified equivalent circuit (right).

The standard equivalent circuit of the IM is modified in order to include two principal space harmonics 5^{th} and 7^{th}, shown in Figure 4.4. According to the new equivalent circuit shown in Figure 4.4 the equation 4.2 is modified as:

$$\begin{bmatrix} V_{abcs} \\ V_{abcr} \\ V_{abcr5} \\ V_{abcr7} \end{bmatrix} = \begin{bmatrix} r_s & 0 & 0 & 0 \\ 0 & r_r & 0 & 0 \\ 0 & 0 & r_{r5} & 0 \\ 0 & 0 & 0 & r_{r7} \end{bmatrix} \cdot \begin{bmatrix} i_{abcs} \\ i_{abcr} \\ i_{abcr5} \\ i_{abcr7} \end{bmatrix} + \frac{d}{dt} \left(\begin{bmatrix} l_s & l_{sr} & 0 & 0 \\ l_{sr}^T & l_r & 0 & 0 \\ l_{sr5}^T & 0 & l_{r5} & 0 \\ l_{sr7}^T & 0 & 0 & l_{r7} \end{bmatrix} \cdot \begin{bmatrix} i_{abcs} \\ i_{abcr} \\ i_{abcr5} \\ i_{abcr7} \end{bmatrix} \right) \tag{4.18}$$

Here $V_{abcr5,7}$ and $i_{abcr5,7}$ are the rotor voltage and currents for 5^{th} and 7^{th} harmonics components. The mutual inductance between rotor and stator total inductance due to 5^{th} and 7^{th} harmonics are:

$$l_{srh} = l_{mh}\begin{bmatrix} \cos\theta_{rh} & \cos\left(\theta_{rh}+\frac{2\pi}{3}\right) & \cos\left(\theta_{rh}-\frac{2\pi}{3}\right) \\ \cos\left(\theta_{rh}-\frac{2\pi}{3}\right) & \cos\theta_{rh} & \cos\left(\theta_{rh}+\frac{2\pi}{3}\right) \\ \cos\left(\theta_{rh}+\frac{2\pi}{3}\right) & \cos\left(\theta_{rh}-\frac{2\pi}{3}\right) & \cos\theta_{rh} \end{bmatrix} \tag{4.19}$$

$$l_{rh} = \begin{bmatrix} l_{lr}+l_{mh} & -\frac{1}{2}l_{mh} & -\frac{1}{2}l_{mh} \\ -\frac{1}{2}l_{mh} & l_{lr}+l_{mh} & -\frac{1}{2}l_{mh} \\ -\frac{1}{2}l_{mh} & -\frac{1}{2}l_{mh} & l_{lr}+l_{mh} \end{bmatrix} \tag{4.20}$$

where h is the harmonic order, and $l_{mh} = l_m / h^2$ [125, 131], θ_{rh} is rotor position for different harmonics order. If 5^{th} harmonic is considered the $\theta_{rh} = -5\theta_r$ and for 7^{th}harmonics $\theta_{rh} = 7\theta_r$ here positive and negative sign indicates the positive and negative sequence of the harmonics. Now, the torque equation will become

$$T_e = \frac{p}{2}\left[\frac{1}{2}\left[\begin{bmatrix} i_{abcs} & i_{abcr} & i_{abcr5} & i_{abcr7} \end{bmatrix} \Delta \frac{\begin{bmatrix} l_s & l_{sr} & 0 & 0 \\ l_{sr}^T & l_r & 0 & 0 \\ l_{sr5} & 0 & l_{r5} & 0 \\ l_{sr7} & 0 & 0 & l_{r7} \end{bmatrix}}{\Delta\theta_r} \begin{bmatrix} i_{abcs} \\ i_{abcr} \\ i_{abcr5} \\ i_{abcr7} \end{bmatrix}\right]\right] \tag{4.21}$$

$$T_e = \frac{p}{2}\left[\left(i_{abcs}^T \frac{\Delta l_{sr}(\theta_r)}{\Delta\theta_r} i_{abcr}\right) + \frac{1}{2}\left(i_{abcs}^T \frac{\Delta l_{sr}(\theta_r)}{\Delta\theta_r} i_{abcr5}\right) + \frac{1}{2}\left(i_{abcs}^T \frac{\Delta l_{sr}(\theta_r)}{\Delta\theta_r} i_{abcr7}\right)\right] \tag{4.22}$$

According to the new equations, another machine model is created which takes space harmonics into account. The final induction motor model is an extension to the well-known approximate equivalent circuit and the model will achieve more realistic results.

4.2 Transformation of IM model into a common reference frame

The mathematical model of an induction motor expressed in terms of phase variables and can be transformed into a corresponding model in the common

reference frame by the mean of appropriate mathematical transformation [126]. Park's transformation matrix is used to transform the phase variable model [126] as shown in equations 4.23 – 4.24.

$$X_s = \frac{2}{3}\begin{bmatrix} \cos\theta_s & \cos\left(\theta_s - \frac{2\pi}{3}\right) & \cos\left(\theta_s + \frac{2\pi}{3}\right) \\ -\sin\theta_s & -\sin\left(\theta_s - \frac{2\pi}{3}\right) & -\sin\left(\theta_s + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4.23}$$

$$X_r = \frac{2}{3}\begin{bmatrix} \cos\theta_r & \cos\left(\theta_r - \frac{2\pi}{3}\right) & \cos\left(\theta_r + \frac{2\pi}{3}\right) \\ -\sin\theta_r & -\sin\left(\theta_r - \frac{2\pi}{3}\right) & -\sin\left(\theta_r + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4.24}$$

In the transformation matrices, the rotor and stator utilise two different equations in terms of angles. The angle in the equation shows the stator angle θ_s for the common coordinate system and the rotor has an instantaneous angular position θ_{inst} with respect to the stator and can be defined as:

$$\theta_r = \theta_s - \theta_{inst} \tag{4.25}$$

The procedure of transforming the phase variable model into a rotational fictitious winding can be found in [126]. The model obtained after the application of the transformation can be given as:

$$\begin{aligned} V_{ds} &= r_s i_{ds} + \frac{d\psi_{ds}}{dt} - \omega_s \psi_{qs} \\ V_{qs} &= r_s i_{qs} + \frac{d\psi_{qs}}{dt} + \omega_s \psi_{ds} \\ V_{os} &= r_s i_{os} + \frac{d\psi_{os}}{dt} \end{aligned} \tag{4.26}$$

$$
\begin{aligned}
V_{dr} &= r_r i_{dr} + \frac{d\psi_{dr}}{dt} - (\omega_s - \omega_r)\psi_{qr} \\
V_{qr} &= r_r i_{qr} + \frac{d\psi_{qr}}{dt} + (\omega_s - \omega_r)\psi_{dr} \\
V_{or} &= r_r i_{or} + \frac{d\psi_{or}}{dt}
\end{aligned}
\tag{4.27}
$$

where *ds, qs ,os* are the fictitious stator components and *dr, qr*, *or* are the fictitious rotor components after the transformations are applied. The component ω_s is the arbitrary angular speed of the common coordinate system and ω_r is the rotor angular speed. The flux linkages are given by:

$$
\begin{aligned}
\psi_{ds} &= l_s i_{ds} + l_m i_{dr} \\
\psi_{qs} &= l_s i_{qs} + l_m i_{qr} \\
\psi_{os} &= l_{os} i_{os}
\end{aligned}
\tag{4.28}
$$

$$
\begin{aligned}
\psi_{dr} &= l_r i_{dr} + l_m i_{ds} \\
\psi_{qr} &= l_r i_{qr} + l_m i_{qs} \\
\psi_{or} &= l_{or} i_{or}
\end{aligned}
\tag{4.29}
$$

where the stator and rotor inductances can be described as

$$
\begin{aligned}
l_s &= l_{ls} + l_m \\
l_r &= l_{lr} + l_m
\end{aligned}
\tag{4.30}
$$

where l_s and l_r are the stator and rotor self-inductance. l_{ls}, l_{lr} and l_m are the leakage inductances of the stator, rotor and the magnetising inductance respectively. In the equations each set of three phase windings is substituted with a new set of three windings, the new sets are labelled as *d, q* and *o*. If the machine is fed from three phase symmetrical supply the *o* component cannot exist, for this reason, the fictitious *o* winding is omitted for further considerations. The electromagnetic torque of the IM rotating at an arbitrary speed can be achieved:

$$
T_e = \frac{p}{2}(K_s^{-1} i_{abcs}^T)\frac{\Delta l_{sr}(\theta_r)}{\Delta \theta_r}(K_r^{-1} i_{abcr}) \tag{4.31}
$$

Where K_s^{-1} and K_r^{-1} are the inverse Parks transformation for stator and rotor quantities. By performing the multiplication of matrices shown in [126] the following formula of the electromagnetic torque results

$$T_e = \frac{3}{2}\frac{p}{2} l_m (i_{qs} i_{dr} - i_{ds} i_{qr}) \tag{4.32}$$

The mechanical equations remain the same as equation 4.17. The necessity of converting the three phase machine winding to fictitious two phase winding rotating at an arbitrary speed arise due to the simpler controller design. The controller design became much easier using these equations as the controller has to deal with two sets of differential equations.

4.3 Loss calculation for open end winding IM drive

The open end winding IM drive considered in this section consists of an isolation transformer, an open phase induction motor, dual two-level converters and a rectifier [113]. To calculate the losses the drive system was modelled using the Simulink and PLECS simulation platform. An induction machine was selected along with a dual two-level inverter with equal voltage sources. Equal sources ratio will allow achieving three-level output voltage waveform across the load.

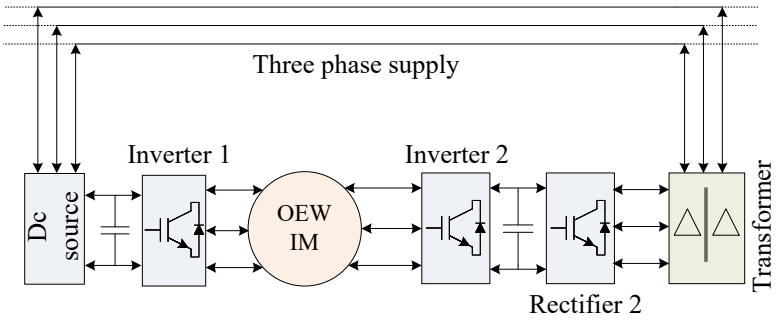


Figure 4.5 Open end winding IM drive with an isolation transformer.

A circuit diagram of the dual inverter system is shown in Figure 4.5. A dc voltage source is used to supply one of the converters the other is supplied with a bridge rectifier which is isolated using an isolation transformer. The machine used for this analysis is designed for aerospace application and requires peak phase voltage of 155Volts and the rated peak phase current is 340Amps. The total DC link voltage was set to 270Volts to modulate the peak reference voltage of 155Volts with a

modulation index of 1 using space vector modulation scheme. The drive system was operated using a *v/f* control method and fully loaded after the machine reaches steady state, a block diagram is shown in Figure 4.6. This is one of the simplest control methods where the ratio of rated voltage to the rated fundamental frequency is kept constant to achieve constant flux throughout the machines operating range [132]. The *v/f* constant is denoted as $C_{v/f}$ in equation 4.33.

$$C_{v/f} = \frac{V_{rated}}{f_{rated}} \tag{4.33}$$

The speed of the machine was controlled by injecting the reference frequency and the reference voltage was calculated by manipulating the equation 4.33. To achieve results the fundamental frequency was set to 266.667Hz to achieve a rotor speed of 8000 rpm. After the speed reaches steady-state a reference torque of 60Nm was set in the controller. The current and voltage waveforms were observed by varying the converter's switching frequency from 5–20kHz.

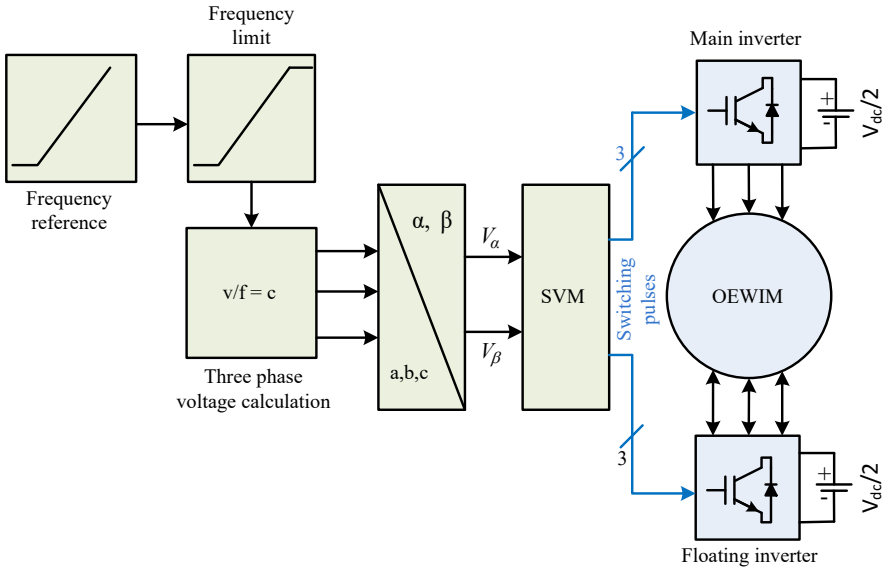


Figure 4.6 Block diagram of v/f controlled open end winding induction motor drive.

The losses in the power converters were then calculated using PLECS and SIMULINK platform using the component manufacturer's data. Losses in the IM were calculated using Finite Element (FE) software (MagNet) by injecting the currents acquired from *v/f* controlled drive. Finally, an isolation transformer was designed and losses were determined, again using FE software.

4.3.1 Loss estimation of the converter system

The power converter semiconductor devices were selected to withstand half of the DC link voltage and the rated load current. The IGBT switches selected for this analysis is designed by Infineon, FF600R07ME4_B11 [133]. The switches selected for this analysis is one of the IGBT switches available in the market which is the closest to the required rating for this particular drive operation. The conduction and switching losses for the power semiconductor devices were calculated and all other losses were ignored as they are relatively small in comparison.

To calculate the switching losses the semiconductor device manufacturer's data was used; the switching energy loss is provided in relation to the voltage, collector current and the junction temperature. The switching loss profile can be seen in Figure 4.7. In PLECS simulation platform this data can be inserted for each switching devices as a 4D table where the energy loss will be selected depending on the collector-emitter voltage, collector current and the device temperature [134].

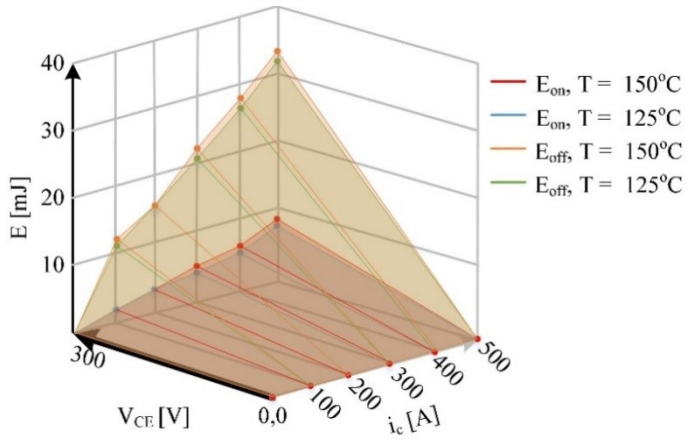


Figure 4.7 Switching loss profile for IGBT switch FF600R07ME4_B11.

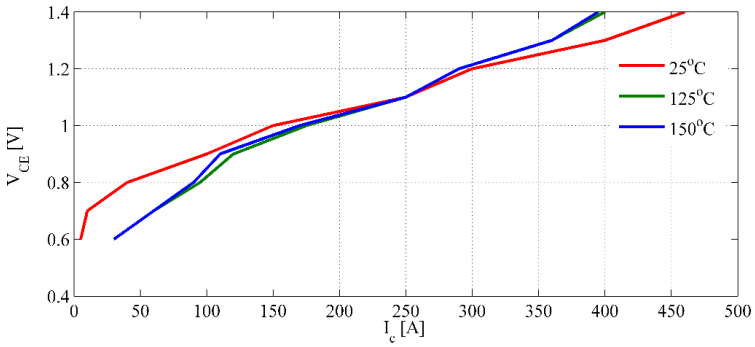


Figure 4.8 Conduction loss profile for IGBT switch FF600R07ME4_B11.

The conduction loss profile is also shown in Figure 4.8. The conduction loss profile was also defined inside the PLECS simulation platform as a 2D graph and the loss is calculated multiplying the turn on voltage drop by the collector current. The converter losses were calculated for a 50kW motor by varying switching frequency from 5-20kHz and are shown in Table 4.1. In the table, it can be seen that the converters conduction losses are essentially constant because the fundamental output voltage/current of the converter is constant regardless of the switching frequency. The switching losses were increased with the switching frequency as the number of switching instances increase in each fundamental period.

Table 4.1 Losses for the dual inverter system.

Frequency (kHz)	Conduction loss (W)	Switching loss (W)	Total loss (W)
5	1048	152	1200
10	1050	263	1313
15	1050	369	1419
20	1050	480	1530

4.3.2 Loss calculation of the induction motor

To calculate machine losses, a suitable slip is injected to the rotor to achieve 60 N-m torque, which is rated for this machine. Simulation has been carried out for a current fed, velocity driven combination. The machine parameters are shown in Table 4.2.The losses were calculated by injecting the full load currents achieved from the *v/f* controlled drive, as shown in Figure 4.9.The losses are divided into two parts iron losses and copper loss. The method used for calculation of iron losses in FE software (MagNet) is based on Epstein frame loss measurement but uses the Steinmetz equation augmented with an eddy current term to split the total iron losses into two components; hysteresis with anomalous losses and eddy current losses [135], shown in equation 4.34. The Loss curve data from the manufacturer at several frequencies is used to get the coefficients for the Steinmetz and eddy current loss terms. This way, both loss quantities can be calculated individually. The DC copper losses were estimated using the FE software where the losses were calculated using I^2Requation, where I is the RMS phase current and R is DC resistance. A figure of

the simulated motor using MagNet is shown in Figure 4.10.In the figure, a flux function view is shown when the motor reaches steady-state at 7940rpm with an electromagnetic torque of 60Nm due to the slip.

$$P = \underbrace{k_h f^{\alpha} B^{\beta}}_{Hysteresis} + \underbrace{k_e (sfB)^2}_{Eddy\,current} \tag{4.34}$$

Where k_h is hysteresis loss coefficient, f is the fundamental frequency, B is the peak flux density, k_e is the eddy current loss coefficient and s is the lamination thickness ratio. The losses were calculated injecting the PWM currents achieved from the *v/f* controlled drive with varying switching frequency from 5-20kHz.

Table 4.2 Induction motor parameter.

Fundamental frequency	f	266.667 Hz
Phase current (RMS)	i	155 Amps
Phase voltage (RMS)	V	110 Volts
Rated slip speed	s	60 rpm
Rated torque	Te	60 Nm
Stator resistance	r_s	0.00206 Ω
Rotor resistance	r_r	0.00276 Ω
Stator leakage inductance	l_{ls}	$0.0207e^{-3}$ H
Rotor leakage inductance	l_{lr}	$0.047e^{-3}$ H
Magnetising inductance	l_m	$0.69e^{-3}$ H
Pole pair	P	2
Machine weight		8 kg

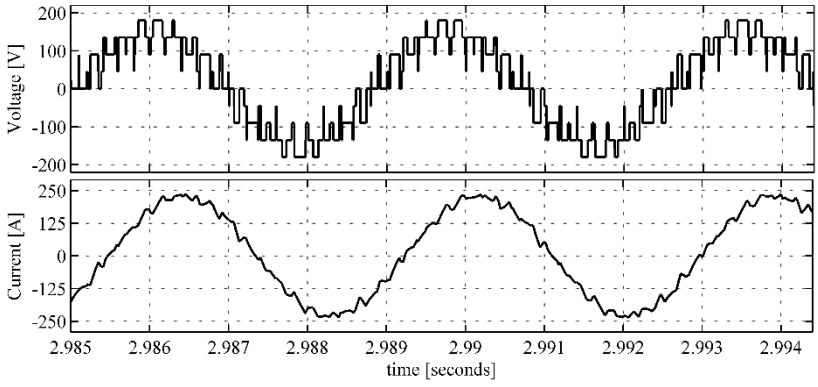


Figure 4.9 Phase voltage and current for the IM when the machine was fully loaded.

Table 4.3 Materials used for loss calculations.

Stator back iron and tooth	CoFe VACOFLUX 50
Stator winding	Copper: 100% IACS
Rotor back iron and tooth	CoFe VACOFDOR s plus
Rotor bars	Copper:80% IACS (CuCrZr)

Table 4.4 Losses in the stator of the IM.

Switching	Stator losses			
	Eddy current loss (w)	Hysteresis loss (W)	Copper loss (W)	Total loss (W)
5kHz	29.57	145.47	587	762.04
10kHz	32.37	151.5	585	768.87
15kHz	30.24	147.31	585	762.55
20kHz	30.66	148.19	585	763.85

Table 4.5 Losses in the rotor of the IM.

Switching	Rotor losses			
	Eddy current loss (w)	Hysteresis loss (W)	Copper loss (W)	Total loss (W)
5kHz	9.23	28.36	487	524.59
10kHz	12.1	31.59	476	519.69
15kHz	10.66	30.28	451	491.94
20kHz	11.05	30.76	446	487.81

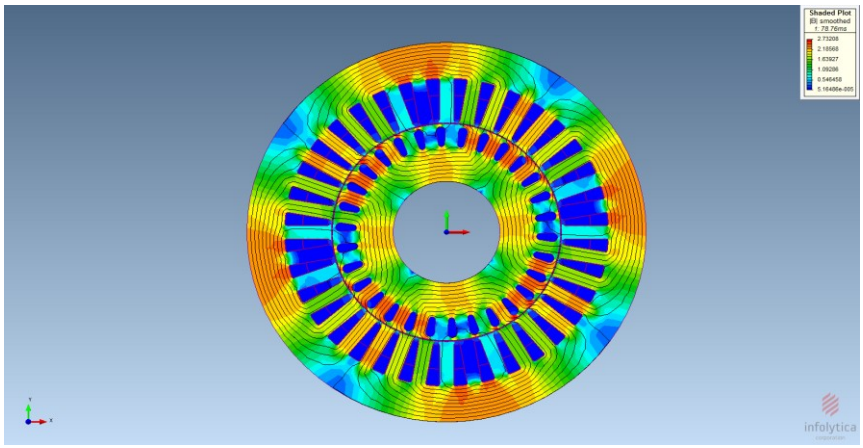


Figure 4.10 Flux density distribution and flux plot of IM.

The losses of the rotor and stator can be seen in Table 4.4 and 4.5. The material properties can be found in [136-138]. It can be seen from the Tables 4.4 – 4.5 that after 10kHz switching the machine losses decrease, this is due to the machine inductance filtering out the higher frequency switching components.

4.3.3 Design and losses of isolation transformer

To calculate losses a three phase isolation transformer was designed using area product approach [139]. The transformer was designed considering aircraft power system where the grid operates on 230*Volts* and 400*Hz*, a diagram of the transformer is shown in Figure 4.11. The magnetic materials were selected to achieve low loss, low mass density and to achieve flux density around 1.5T. The design specification is shown in table 4.6. A comprehensive design process for the isolation transformer is shown in Appendix A in detail.

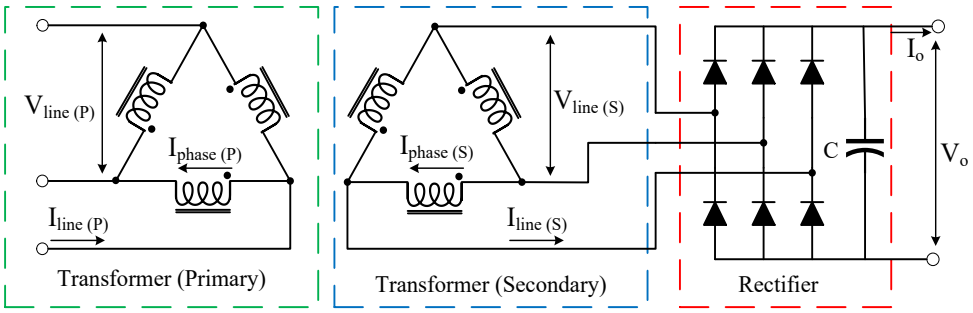


Figure 4.11 Three phase delta connected isolation transformer with a bridge rectifier.

Table 4.6 Design parameter of isolation transformer

Primary voltage	$V_{line(P)}$	230 V
Output voltage	V_o	135 V
Secondary current	I_o	190 A
Fundamental frequency	f	400 Hz
Power output	P_0	25 kW
Efficiency	n	95%
Window utilisation factor	K_u	0.4

According to the calculation, the iron area is 19.858cm^2 and window area is 52.26cm^2. To design the transformer using CAD tool (MagNet) iron depth and width is kept the same and width of the window is 4.57cm and height is taken as 11.43cm.

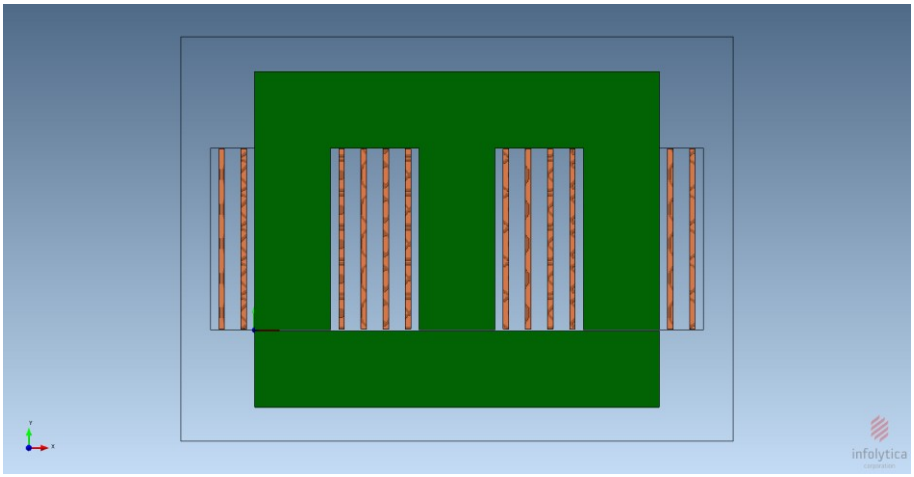


Figure 4.12 Isolation transformer designed in MagNet.

According to the calculation an FE model was created using Magnet shown in Figure 4.12. The winding and core material is shown in Table 4.7. The secondary of the transformer was connected to a bridge rectifier and the output DC link voltage was kept constant at 135Volts, shown in Figure 4.11. A load resistance is connected to the output of the rectifier and the resistance value was selected to achieve 25kW power output from the rectifier, as the drive operation isolated inverter will supply 25kW power to the load. The primary of the transformer is supplied with an AC voltage source of 230Volts with a fundamental frequency of 400Hz. The flux in the transformer is shown in Figure 4.13for the situation when the transformer was loaded.

Table 4.7 Used materials and losses for isolation transformer.

Materials	
E-I core	Arnon 5
Windings	Copper: 100% IACS
Losses and weight	
Iron loss (W)	304
Copper loss (W)	112.5
Total loss (W)	200
System weight (kg)	16.25

The losses of the transformer were calculated considering sinusoidal supply, the losses for PWM waveforms were not considered for this analysis. The core losses

were calculated using the same Steinmetz equation used for machine loss calculation[equation 4.34]. The copper losses considered here are due to DC resistance and the calculation is shown in Appendix A. The losses for the transformer are shown in Table 4.7 along with the core and winding material used. The properties of the core material can be found in [136] and the winding material in [140].

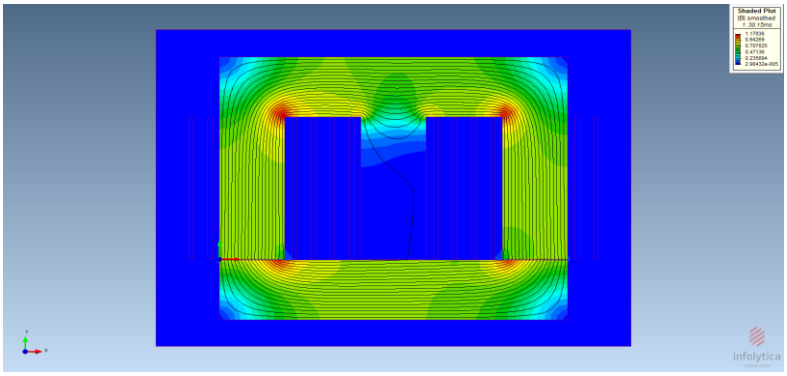


Figure 4.13 Flux function view of the transformer when it is loaded.

4.4 Reduction of losses size and weight of OEW-IM drive

The open end winding IM drive was analysed in terms of losses. The losses for an induction motor and power converters are unavoidable, the only component that can be removed from the system is the isolation transformer. If the transformer can be removed then the system volume and weight will reduce as well losses in the isolation transformer and in the bridge rectifier.

Table 4.8 Loss and weight comparison for IM drive components.

Component	Weight (Kg)	Total loss (W)
HSIM	8	1288
Transformer	16.8	417
Power converter	30 (without cooling system)	1313
Total	54.52	3018
Efficiency	94.31%	
Power to weight ratio	917.09 W/Kg	

To calculate total system weight a two-level converter designed by Semikron is selected, the converter is known as SKAI module and are designed for automotive application [141]. The converter system is capable of supplying more than 200kW of load. The weight of each converter is 15kg and the 50kW motor weighs 8kg. In contrast with the motor and power converter, the isolation transformer is heavy and weight of the transformer is 16.52kg, as shown in Appendix A. The loss and weight comparison of the drive system are shown in Table 4.8 for a switching frequency of 10kHz. It can be noted from the table that if the isolation transformer can be removed from the system, then the system efficiency will increase by 1% and power to weight ratio will increase by more than 30% along with the decrement of system volume.

4.5 Conclusion

A detailed loss analysis of traditional dual inverter topology is presented in this chapter. A three phase induction machine was model incorporating space harmonics to achieve more realistic simulation results. The drive system was simulated using PLECS and Simulink simulation platforms and the converter losses were calculated from the simulation platform using component manufacturer's data. An isolation transformer was designed and an induction machine model was used to calculate losses using an FE software named MagNet. The drive analysis suggests that the system volume will reduce by 30% as well as the efficiency will increase by 1% if the requirement of the isolation transformer is eliminated from the drive system.

Chapter 5

Analysis of Dual Inverter with one Bridge Floating

This chapter investigates a dual two-level inverter, where one of the bridge inverters is floating. This floating bridge will provide isolation and will eliminate the need for any isolation transformer in systems where two bridges are used for a single, open-ended load. This is achieved by employing just a capacitor instead of an isolated DC voltage source to supply the floating end of the converter. The capacitor voltage will be charged to half of the main inverters DC link voltage. This DC link voltage ratio will allow the proposed converter to achieve a three-level output pole voltage waveform.

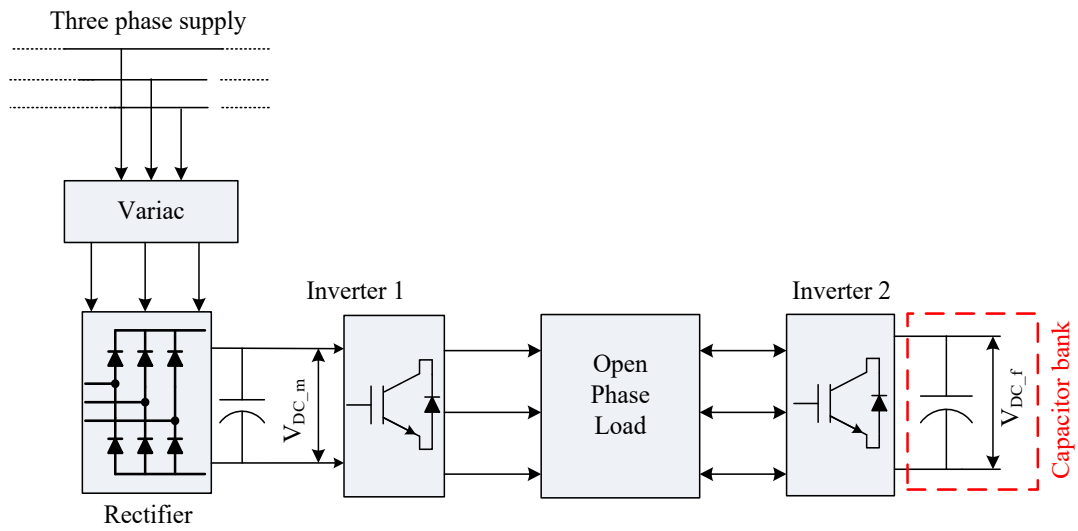


Figure 5.1 Block diagram of dual inverter with an open phase load.

A block diagram of the proposed dual two-level inverter is shown in Figure 5.1. The DC link voltage of the floating inverter is controlled and kept constant to the required voltage value using redundant switching states.

This chapter presents detailed simulation results to show that the proposed converter can achieve multilevel output voltage waveforms and that the floating capacitor voltage can be controlled.

5.1 Analysis of the proposed system

This section presents a detailed analysis of the proposed floating bridge topology. To justify the selection of this particular voltage ratio the dual inverter with equal voltage sources is compared to the proposed topology. The comparisons are in term of output voltage level and DC bus utilisation. A detailed analysis is presented for the proposed system along with the identification of the achievable voltage levels and the limit of the modulation index. A modification of switching pulses is also presented to avoid phase voltage spike during the dead-time interval and to improve waveform quality.

5.1.1 Floating capacitor voltage control

The floating bridge capacitor voltage can be controlled by directing the load current through the floating capacitor in either direction. To consider the direction of the load current through the floating capacitor, switching combinations produced by the dual two-level inverter have been analysed.

Table 5.1 Relation between switching number and switching states.

Switching number	Switching states (Top switches)		
	Leg a	Leg b	Leg c
1	on	off	off
2	on	on	off
3	off	on	off
4	off	on	on
5	off	off	on
6	on	off	on
7	on	on	on
8	off	off	off

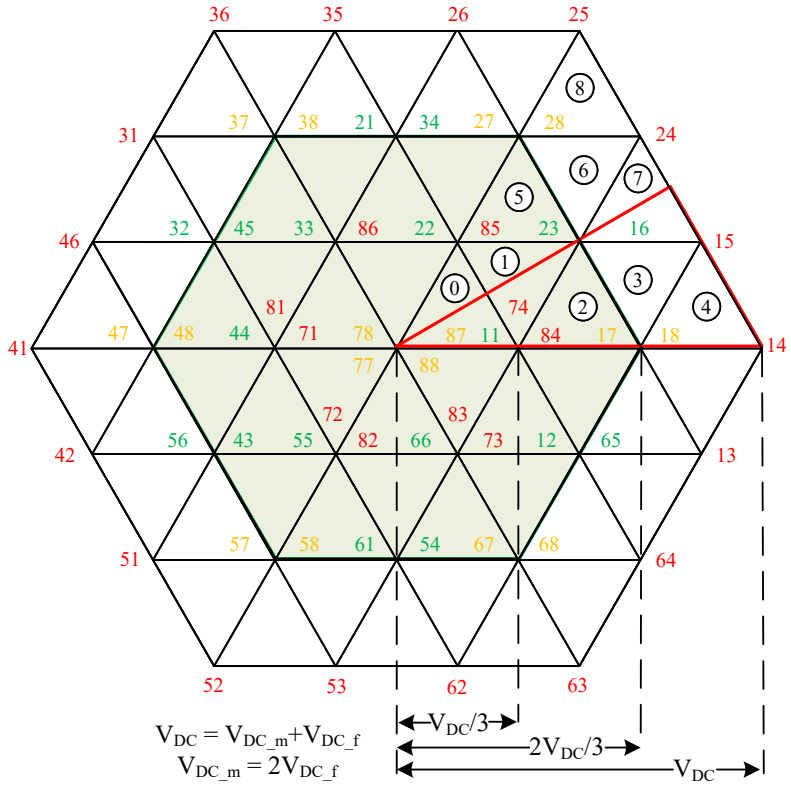


Figure 5.2 Space vector of dual two-level inverter (source ratio 2:1).

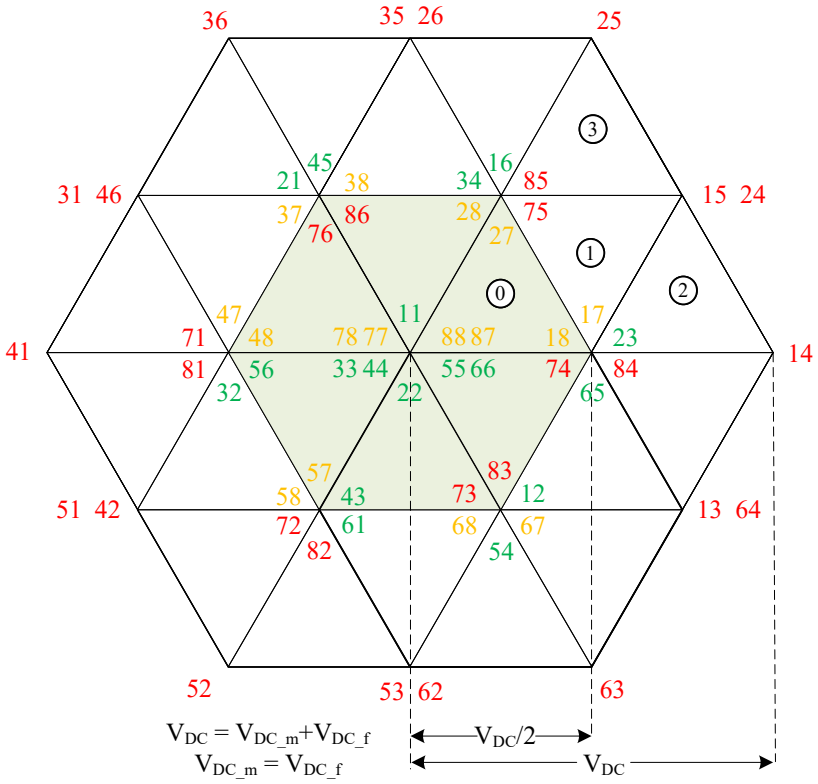


Figure 5.3 Space vector of dual two-level inverter (source ratio 1:1).

The dual two-level inverter produces 64 switching states and can be represented using space vector diagram, which is a representation of three phase quantity utilising a single vector in the α-β co-ordinates. A space vector diagram along with the switching sequences for the dual two-level inverter with unequal and equal voltage sources are shown in Figure 5.2 and in Figure 5.3. In the figures, the number inside the circles specify the subsector.

The vector diagrams are obtained by assuming that both the converters are fed by isolated voltage sources. In the vector diagram the switching combinations are represented with two numbers, as an example consider the switching state (16). The number on the left hand side considers the switching sequence of the first converter, the numbers can be decomposed as 1(+ - -) where '+' refers to the on state of the top switch of the converters first leg and '-' refers to the off state of the top switches of the converts second and third leg. The number on the right hand side is the switching states of the second inverter legs where the number can be decomposed as 6(+ - +).

Table 5.1 presents the relationship between all the switching numbers and the converter states. In the state diagrams, Figures 5.2 – 5.3 the red numbered switching combinations discharge the floating capacitor while the green numbered switching combinations charge the floating capacitor. The yellow numbered switching combinations hold the last state of capacitor voltage and are therefore neutral in terms of the state of charge of the floating capacitor.

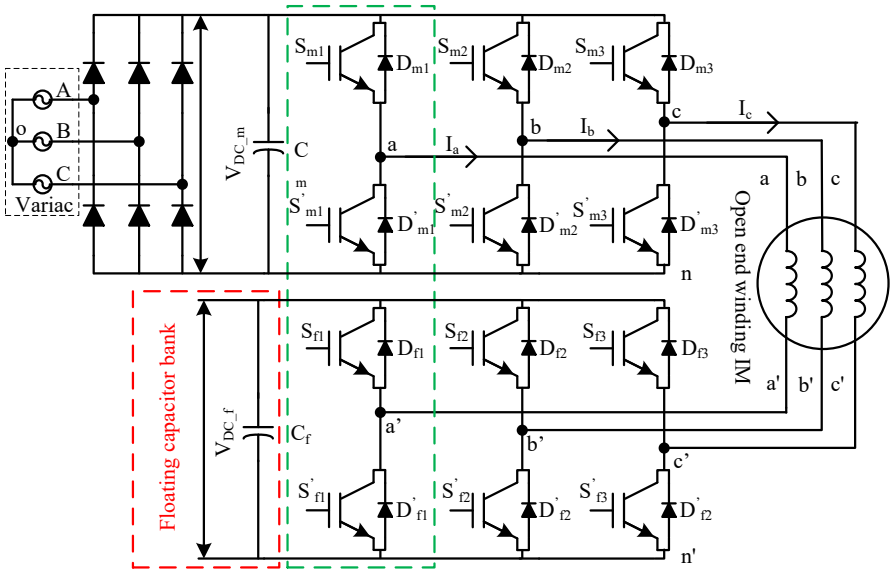


Figure 5.4 Power stage diagram of dual inverter with an open phase load.

To access how these switching states charge or discharge the floating capacitor a set of current flow diagrams of the different switching combinations are shown in Figure 5.5. These diagrams are derived from the power stage diagram of the proposed system shown in Figure 5.4. In the figure, a variac is used to charge the main inverter's capacitor voltage slowly to the rated voltage and the three phase supply is considered to be 415V with 50Hz fundamental. In the current flow diagram, solid lines represent the current flowing paths and the dotted lines signify open circuits.

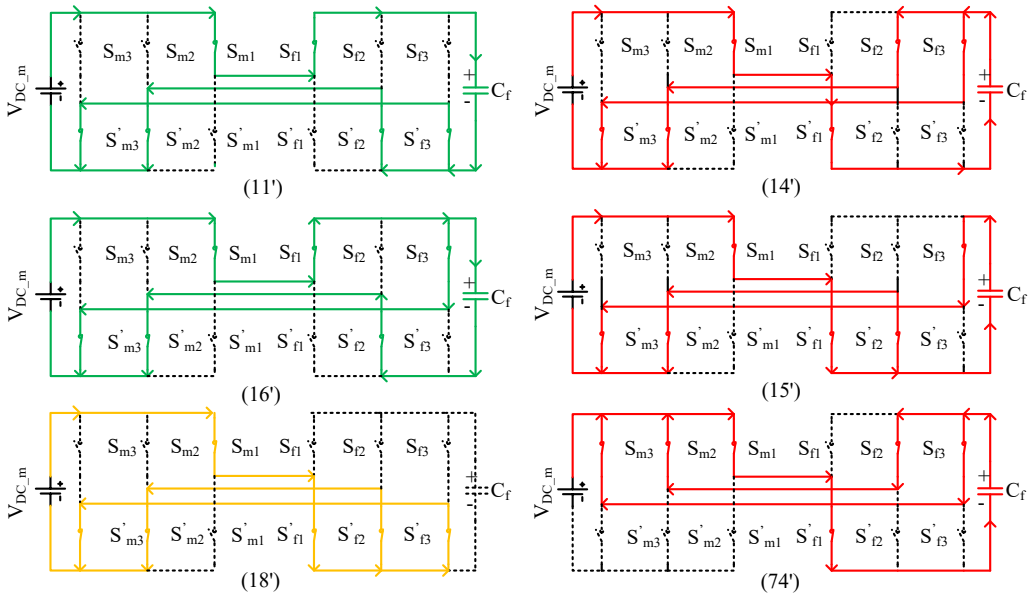


Figure 5.5 Current flow for different switching states.

It can be seen from the current flow diagrams that combinations (11) and (16) will result in a current path through the capacitor from the positive to the negative terminal, thus charging the capacitor. Combinations (14), (15) and (74) will result in a current in the opposite direction and will, therefore, act to discharge the capacitor. Combinations ending with 7 (111) or 8 (000) are zero states and will, therefore, have no impact on floating capacitor's voltage.

To understand which combinations can charge the capacitor to the required value a simplified circuit diagram of the dual inverter system for switching states (11) and (16) are analysed, as shown in Figure 5.6 and in Figure 5.7 respectively. The circuit is drawn assuming that the switches and capacitors are ideal and the load is a simple three phase resistive load. All other parasitic components and non-linearity are ignored for this analysis.

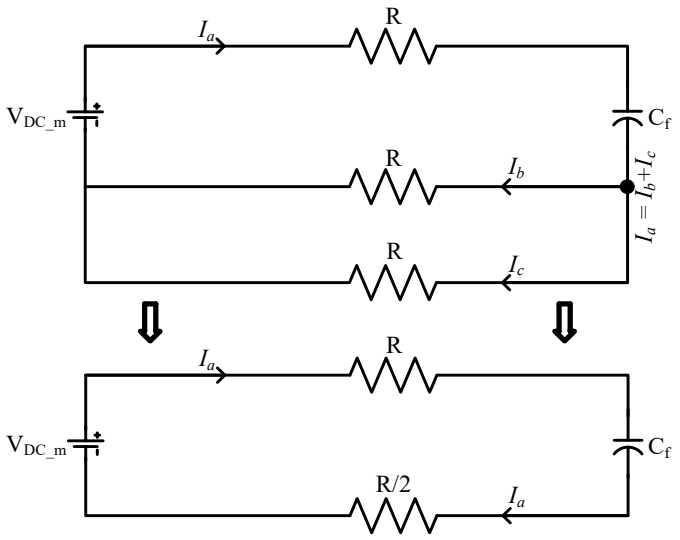


Figure 5.6 Circuit diagram of dual inverter when the switching state (11) is applied.

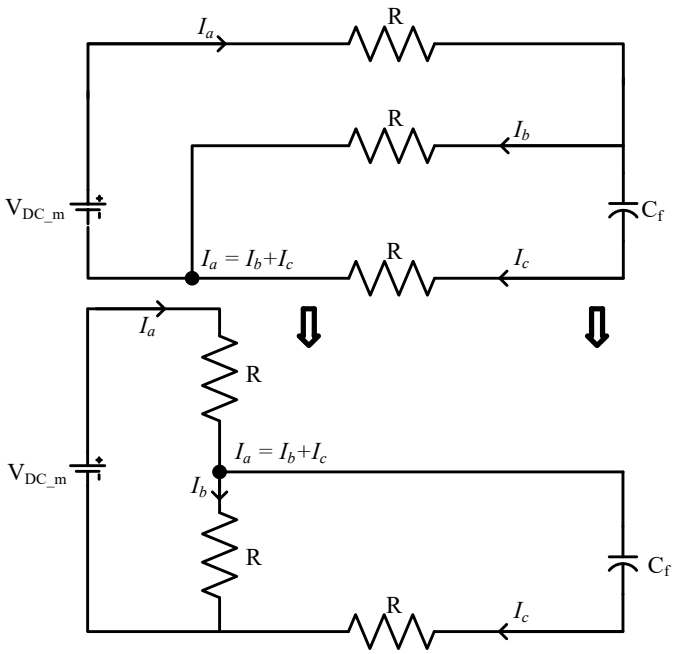


Figure 5.7 Circuit diagram of dual inverter when the switching state (16) is applied.

It can be seen from the Figure 5.6 that for the switching combination (11) the formation of the total circuit is such that floating capacitor can be charged equal to the main inverters DC link voltage level. On the other hand from Figure 5.7 it can be seen that due to the formation of voltage divider the floating capacitor cannot be charged more than half of the main inverter's DC link voltage level. It is evident from both the circuit diagrams that the converter can charge the floating capacitor

equal to the main inverter's DC link voltage if the states (11, 22, 33, 44, 55 and 66) are applied. The other charging combinations will act to charge the capacitor to half of the main inverters DC link voltage level.

The state diagram of the dual inverter with equal voltage [Figure 5.3] has all its full charging sequences concentrated on the zero voltage vectors. Therefore it is not possible to charge the floating capacitor and maintain its value if the inverter is operating at the outer hexagon. If this topology is used the number of achievable voltage levels will be two and the modulation index has to be restricted to 0.5. However, if unequal voltage sources are used then the charging sequences are spread across the vector diagram, shown in Figure 5.2. It is also evident from the vector diagram shown in Figure 5.2 that there are only two charging states if the converter is operating at outer hexagon, therefore charging the capacitor voltage to the required value is not possible in this outer hexagon. The capacitor voltage can only be charged and maintained at the required voltage level if the modulation index is kept below 0.67. This is 16% better DC bus utilisation than the dual inverter with equal voltage sources. Moreover, the dual inverter with unequal DC link voltage sources (with a floating bridge) can achieve multilevel (three-level) output voltage waveforms. Therefore the dual inverter with unequal voltage sources is selected for further analysis in this work.

5.1.2 SVM to control the floating capacitor voltage

A space vector modulation technique is adopted in this section to modulate the dual inverter system with one bridge floating. This is one of the high frequency modulation techniques which utilise the space vector diagram to locate the reference voltage and to calculate the duty cycles to modulate a three phase power converter system [70].The process of deriving the SVM algorithm for the proposed topology can be summarised as:

- Two switching tables are constructed utilising the redundant switching states for capacitor charging and discharging.
- The reference voltage location inside space vector diagram is identified.

- The duty cycle for each switch used to modulate the reference voltage is calculated using the three nearest voltage vectors and by solving the volt-second balancing equations.
- The floating DC link voltage is measured and according to voltage values redundant switching states are selected to charge or discharge the capacitor appropriately.

The control of the capacitor voltage is a bang-bang control where the charging and discharging switching states will be selected at every sample time depending on the capacitor voltage at that time. In this way, the need for a PI based controller for the capacitor voltage is avoided. A charging and discharging switching sequences are shown in Table 5.2.

Table 5.2 Charging and discharging switching sequences.

Sub Sector	**Charging**			**Discharging**		
	T_a	T_b	T_c	T_a	T_b	T_c
0	88	11	22	88	84	85
1	11	22	16	84	85	16
2	11	16	17	84	16	17
5	22	16	27	85	16	27

5.1.3 Dead-time effect

The dead-time refers to the turn on delay time of top and bottom switches of an inverter leg to avoid short circuit of the DC link voltage source. During the dead-time interval, the output voltage state of the converter is governed by load current direction and the voltage state is equal to one of the voltage levels before or after the dead-time interval. The dual two-level inverter with unequal voltage sources shows different characteristics to traditional inverters, instead of clamping the output voltage to one of the voltage levels before or after the dead-time interval voltage levels, the load current clamps the output voltage to some other voltage levels. This is true for simultaneous switching for each phase legs of the converters.

In order to understand the phenomenon only one phase leg of the dual inverter is analysed, the phase leg inside the green dotted rectangle shown in Figure 5.4. A circuit diagram is presented in Figure 5.8 for a single phase leg of the dual two-level inverter with a positive load current direction (current flowing from main to secondary converter). The switching states for both the converters are the same and the transition is from (11) both the converters legs top devices are on to (00) both the converters bottom devices are on. The output leg voltage for each converter is analysed for the transition and the total voltage is shown in equation 5.1 to equation 5.3. It can be seen that when both the converters top switches are on Figure 5.8 (a) the total voltage is '$V_{dc}/3$'. During dead-time interval [Figure 5.8 (b)], the load current passes through different devices thus the total voltage becomes '- $V_{dc}/3$'. The circuit diagram of the converters phase legs are shown in Figure 5.8 (c) when the converter legs both the bottom switches are on and the total voltage is '*0*'.

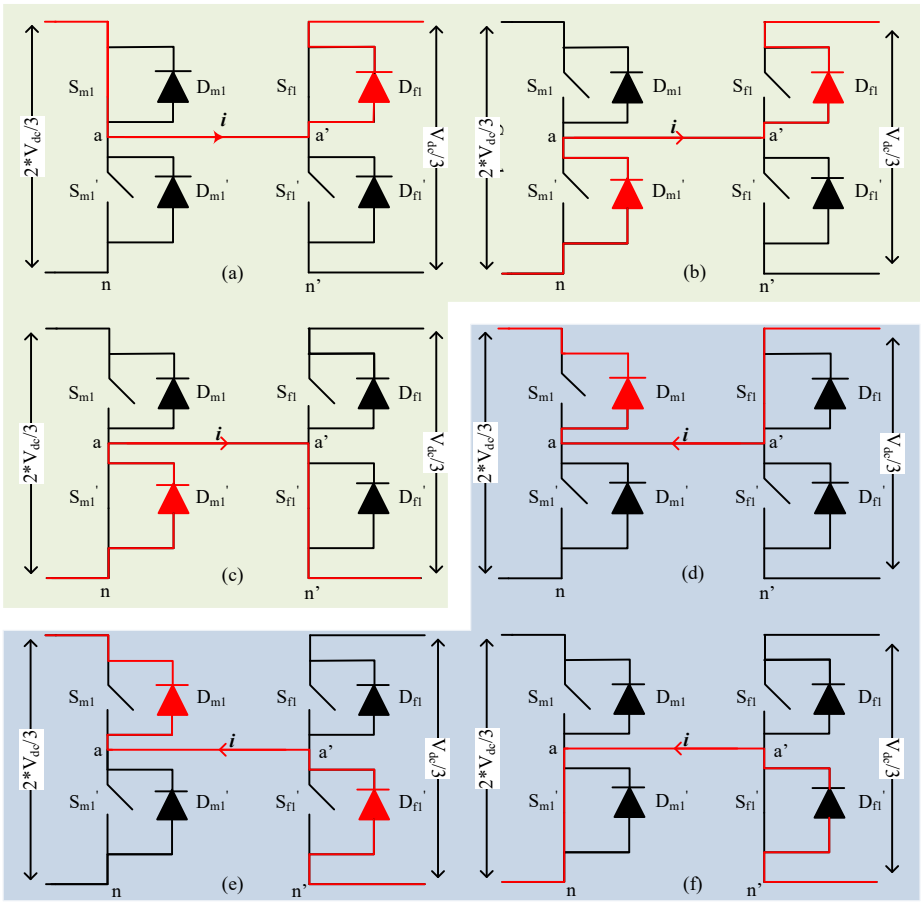


Figure 5.8 Dead-time effect for positive load current (a) current direction before dead-time (b) current direction during dead-time (c) current direction after dead-time and the dead time effect for negative load current (d) current direction before dead-time (e) current direction during dead-time (f) current direction after dead-time.

$$V_{an} = \frac{2V_{dc}}{3}$$
$$V_{a'n'} = \frac{V_{dc}}{3} \quad (5.1)$$
$$V_{total} = \frac{2V_{dc}}{3} - \frac{V_{dc}}{3} = \frac{V_{dc}}{3}$$

$$V_{an} = 0$$
$$V_{a'n'} = \frac{V_{dc}}{3} \quad (5.2)$$
$$V_{total} = 0 - \frac{V_{dc}}{3} = -\frac{V_{dc}}{3}$$

$$V_{an} = 0$$
$$V_{a'n'} = 0 \quad (5.3)$$
$$V_{total} = 0 - 0 = 0$$

Circuit diagrams are also presented in Figure 5.8 (d -f) to show how the converter behaves during the dead-time interval when the load current is negative (load current flowing from floating inverter to the main inverter). It is evident from the analysis that the current conducting devices change during dead-time interval and thus a different voltage level can be seen across the load. This change in voltage level can be detrimental to the output voltage waveform quality and it is, therefore, desirable to avoid this situation.

5.1.4 Avoiding voltage spike during dead-time interval

The phase voltage spike during the dead-time interval will increase distortion in the output voltage as well as to the load current. To eliminate the dead-time spike for the dual inverter system one solution is to avoid the switching sequence which clamps the phase voltage to an unwanted voltage level during the dead-time interval. However, not all the voltage spike producing switching sequences can be avoided for the proposed topology. Another method is to delay the dead-time interval in both converters individually to make sure both the converter phase legs do not go into the dead-time interval at the same time. To understand how much delay is needed between the two converters and which converter will be delayed the diagrams in Figure 5.8 are analysed again. In Figure 5.8 (a) when the current direction is positive and if the converter switching state is (11) then switch (Sm1) and diode (Df1) are

conducting. It can be seen from the figure that if the floating converter goes to its dead-time first then current will still go through the same devices. The main converter will go to its dead-time as soon as the floating converter recovers from its dead-time interval and the current conducting devices will change to the diode (Dm1') and switch (Sf1'). Therefore the phase voltage during the dead-time interval will have exactly the same voltage level as before the dead time interval. If the current direction is negative [Figure 5.8 (d)] then the current will go through the switch (Sf1) and diode (Dm1) when the converter state is (11). If the main converter goes to its dead-time first, then the current conducting devices remain the same. The floating converter will go to its dead-time as soon as the main converter finishes its dead-time interval, therefore avoiding the voltage spike. Table 5.3 presents the relationship between the current direction and the dead-time intervals in each phase legs.

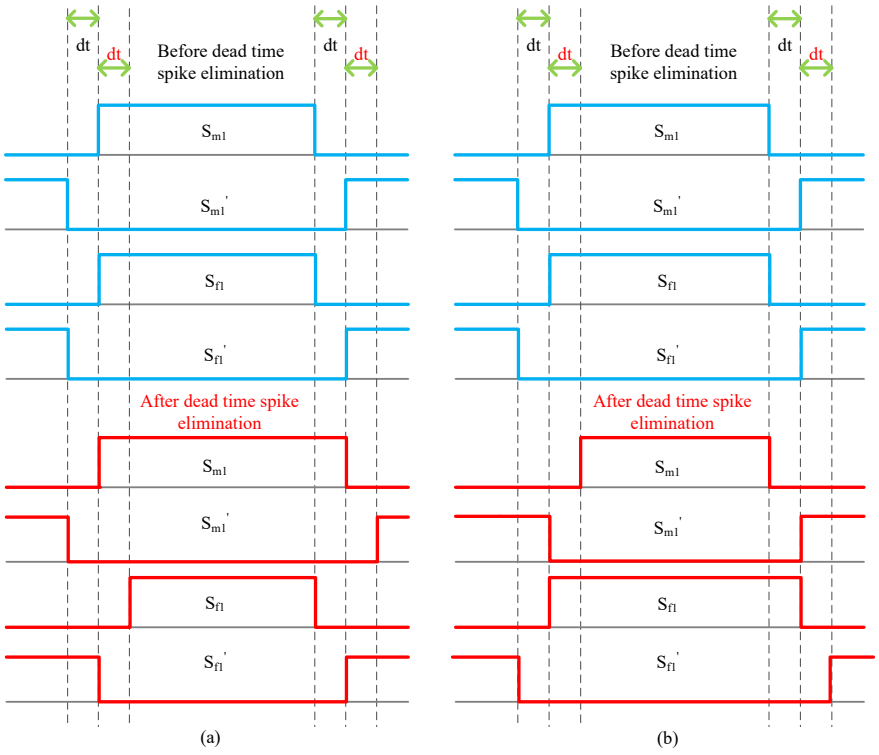


Figure 5.9 Delayed dead-time intervals in both converters (a) load current is positive (b) load current is negative.

Table 5.3 Delay time depending on current direction.

	Inv-1 Top	**Inv-1 Bot**	**Inv-2 Top**	**Inv-2 Bot**
I > 0	Turn off delay	Turn on delay	Turn on delay	Turn off delay
I < 0	Turn on delay	Turn off delay	Turn off delay	Turn on delay

The switching sequences before and after the alteration of the pulses is shown in Figure 5.9 for both positive and negative current directions. To implement the delays in the switching pulses identification of the output current direction is required. To achieve this current direction identification using simulation platform a simple comparator was used, which outputs either 0 or 1 to identify negative and positive current direction for each phase. The output pulses are then altered depending on the current direction.

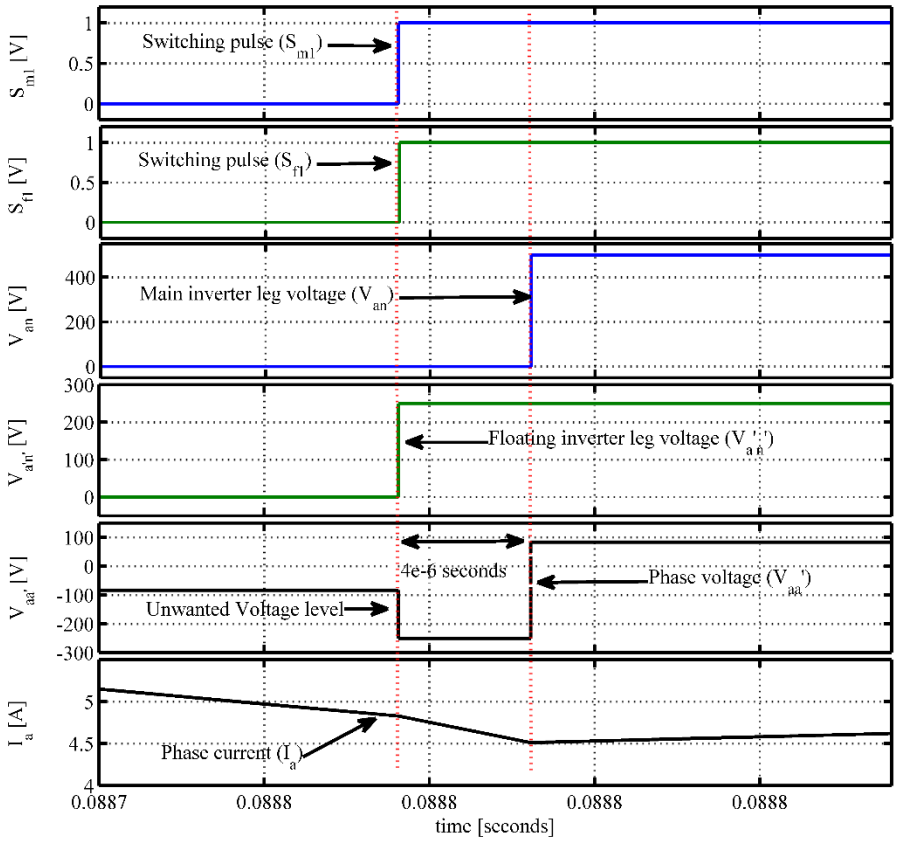


Figure 5.10 Switching pulses, leg voltages, phase voltage and current before dead-time spike elimination.

The results are shown in Figure 5.10 and in Figure 5.11 without and with modification of the output pulses respectively. The results without alteration of pulses show that the phase voltage clamps to some other voltage levels during the dead-time intervals. It is also evident from the simulation results that the output current slope has changed, which will introduce losses to the system. The converter output voltages and current are shown in Figure 5.11 for the case after introducing delays in switching pulses. It can be seen that the spike is no longer visible in the output phase voltage waveform and the load current show no unexpected deviation

during the dead-time interval. To ensure that the modification of the pulses is necessary for this topology the THD of load current and voltage was analysed before and after the modified pulses were applied to the converters. To achieve the results the converter was operated as an open loop *v/f* controlled IM drive and the converter switching frequency was set to 2 kHz. The drive parameters are shown in Appendix F.

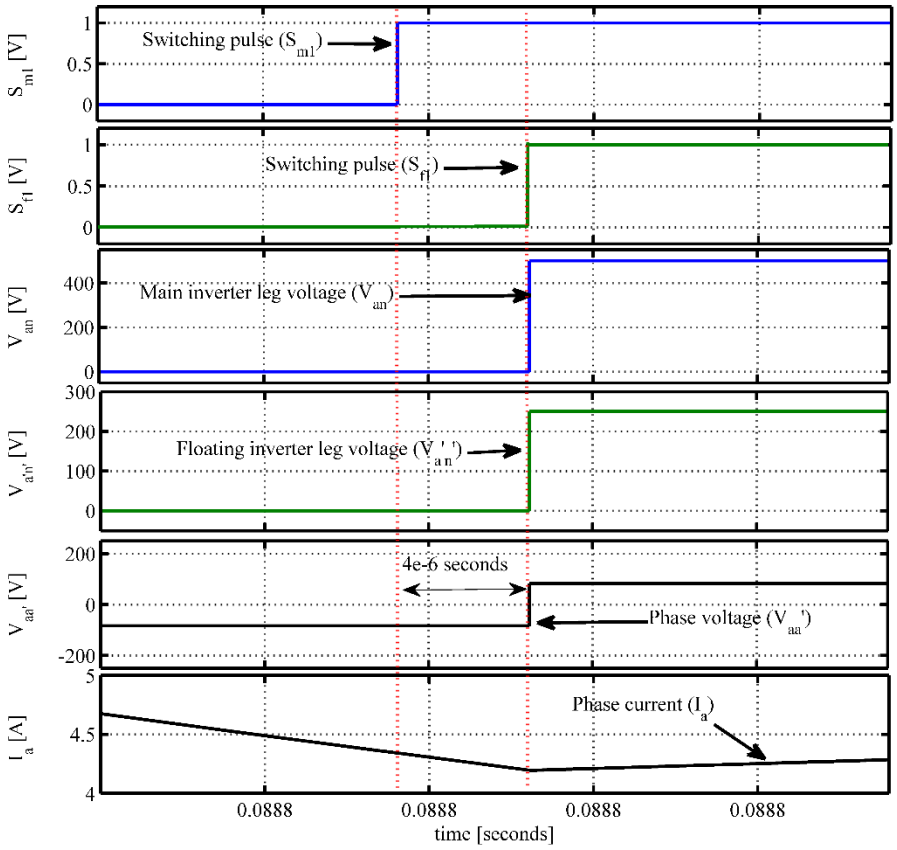


Figure 5.11 Switching pulses, leg voltages, phase voltage and current after dead-time elimination.

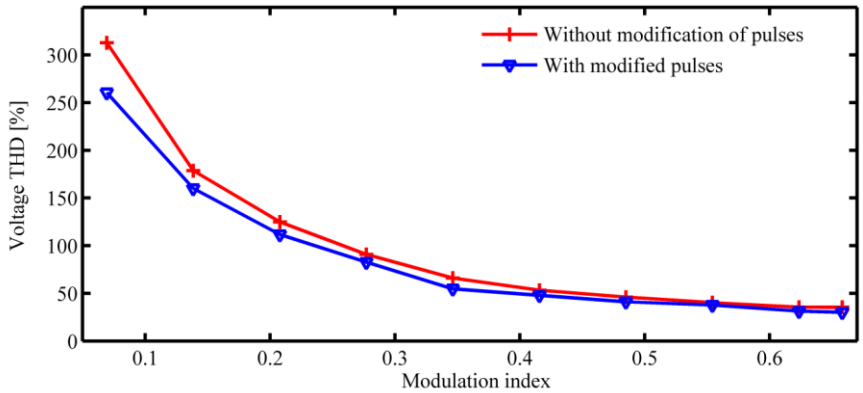


Figure 5.12 Voltage harmonic distortions with or without modification of output pulses.

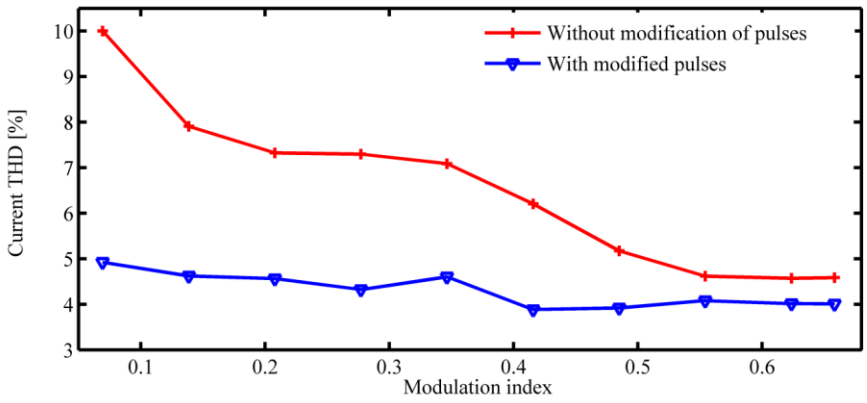


Figure 5.13 Current harmonic distortions with or without modification of output pulses.

The results for the current and voltage THD are shown in Figure 5.12 and in Figure 5.13, with the modulation index varying from 0.05 to 0.66, which is the operating range for proposed topology. The THD of both waveforms has reduced after the modified pulses were implemented. The difference between modified and non-modified pulses decreases with the increase of modulation index, which is due to the utilisation of a lower number of dead-time spike producing switching combinations when operating with a higher modulation index.

5.1.5 Common mode voltage reduction

The common mode voltage appears in the output of power converters and can be dependent on the modulation techniques used. The common mode voltage can be represented as the average sum of three phase voltage at a particular switching state. Due to common mode voltage common mode current can flow through parasitically coupled components and can interfere with other systems [142]. Research has also revealed that the common mode current can flow through machine bearings and cause premature failures [143, 144]. In this section, the common mode voltage of the proposed dual inverter system is identified and the switching combinations which produce lower or zero common mode voltage are selected and utilised for the converter. The dual inverter system has 64 switching states, among them the converter can be modelled with 37 active switching states, the remainder is redundant states. The proposed floating bridge converter can be modelled using only 19 switching states along with 27 redundant states as the outer hexagon is not considered.

Table 5.4 Common mode voltage for all available switching combinations.

States	1 (+ - -)	2 (+ + -)	3 (- + -)	4 (- + +)	5 (- - +)	6 (+ - +)	8 (- - -)	7 (+ + +)
1 (+ - -)	$V_{dc}/9$	0	$V_{dc}/9$	0	$V_{dc}/9$	0	$2V_{dc}/9$	$-V_{dc}/9$
2 (+ + -)	$V_{dc}3$	$2V_{dc}/9$	$V_{dc}3$	$2V_{dc}/9$	$V_{dc}3$	$2V_{dc}/9$	$4V_{dc}/9$	$V_{dc}/9$
3 (- + -)	$V_{dc}/9$	0	$V_{dc}/9$	0	$V_{dc}/9$	0	$2V_{dc}/9$	$-V_{dc}/9$
4(- + +)	$V_{dc}3$	$2V_{dc}/9$	$V_{dc}3$	$2V_{dc}/9$	$V_{dc}3$	$2V_{dc}/9$	$4V_{dc}/9$	$V_{dc}/9$
5(- - +)	$V_{dc}/9$	0	$V_{dc}/9$	0	$V_{dc}/9$	0	$2V_{dc}/9$	$-V_{dc}/9$
6(+ - +)	$V_{dc}3$	$2V_{dc}/9$	$V_{dc}3$	$2V_{dc}/9$	$V_{dc}3$	$2V_{dc}/9$	$4V_{dc}/9$	$V_{dc}/9$
8(- - -)	$-V_{dc}/9$	$-2V_{dc}/9$	$-V_{dc}/9$	$-V_{dc}/9$	$-V_{dc}/9$	$-V_{dc}/9$	0	$-V_{dc}/9$
7(+ + +)	$5V_{dc}/9$	$4V_{dc}/9$	$5V_{dc}/9$	$4V_{dc}/9$	$5V_{dc}/9$	$4V_{dc}/9$	$2V_{dc}/3$	$V_{dc}3$

Table 5.5 Common mode voltage for redundant switching states.

States	Common mode voltage	Redundant States	Common mode voltage
23	$V_{dc}3$	16	0
21	$V_{dc}3$	34	0
45	$V_{dc}3$	32	0
43	$V_{dc}3$	56	0
61	$V_{dc}3$	54	0
65	$V_{dc}3$	12	0
77	$V_{dc}3$		
78	$2V_{dc}/3$	88	0
87	$-V_{dc}/9$		

Among all these 64 states, 57 of them produce common mode voltages of different values. The rest of the switching sequences produce zero '0' common mode voltage across the load. The Common mode voltages related to the switching states are shown in Table 5.4 and can be calculated using equation 5.4.

$$V_{nn'} = ((V_{an} - V_{a'n'}) + (V_{bn} - V_{b'n'}) + (V_{cn} - V_{c'n'}))/3 \tag{5.4}$$

In equation 5.4 V_{xn} and $V_{x'n'}$ are the leg voltages of the main and the floating converter respectively where, x (x = a,b,c) represents the three phase system. A comparison of the common mode voltages for the redundant charging sequences which can charge the floating capacitor to half of the main DC link voltage is shown in Table 5.5. It can be seen from the table that these combinations have redundant states with zero common mode voltage. The switching sequences for the floating bridge converter topology can be selected to hold the charge of floating capacitor voltage as well as to reduce the common mode voltage across the load. The switching combinations which produce lower or no common mode voltage are therefore selected to achieve the output of proposed converter topology.

5.2 Loss comparison

The identification of losses and blocking voltage requirements for the proposed converter are an important part, as reduction of blocking voltage and losses in power semiconductor devices are some of the significant advantages of multilevel converter topologies. In this section, the proposed converter is compared with the dual inverter system with equal voltage levels supplied with isolated sources along and with a single sided three-level NPC converter topology. The selection of these three converters is based on the same output voltage levels. The comparisons shown in this section are in terms of the number of semiconductor devices and associated blocking voltage requirements as well as the number of isolated supplies along with the losses in power semiconductor devices.

Table 5.6shown a comparison of the device voltage ratings along with the number of devices utilised by these three converter topologies. It can be seen that the three-level NPC converter utilises 36 semiconductor devices including antiparallel diodes along with diodes for the rectifier unit, the traditional dual two level inverter topology utilises the same number of devices as the topology requires additional rectifier unit for the secondary supply. The proposed topology does not require an additional isolated supply compared to traditional dual inverter topology and thus utilises only 30 semiconductor devices making this converter superior over the other two converter topologies in terms of device number along with the size and weight of the system.

Finally, switching and conduction losses are calculated for these topologies and compared. The losses were calculated for the 12kW drive used for experimental

validation. The device losses were calculated using semiconductor device characteristics selected according to blocking voltage and current requirements of the topology as shown in Table 5.6. A 1200Volts module was used for the main bridge of the floating bridge topology, the module is designed by Infineon named as F12-25R12KT4G and for the rest of the converters a 600Volts module was used named as FS20R06VE3. The loss calculations are in terms of switching and conduction losses for the power semiconductor devices and in this comparison all other circuit losses were ignored. The losses were calculated using PLECS simulation platform, the loss profile of the power semiconductor are defined inside the simulation platform as stated in the datasheet.

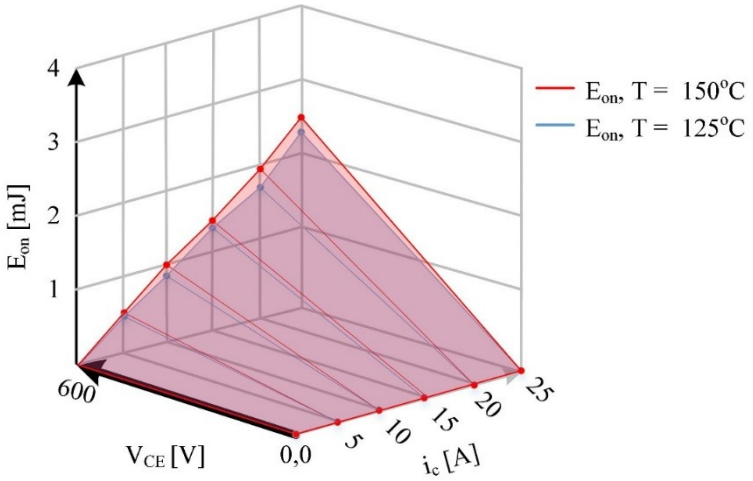


Figure 5.14 Turn-on switching loss profile for Infineon F12-25R12KT4G IGBT switches.

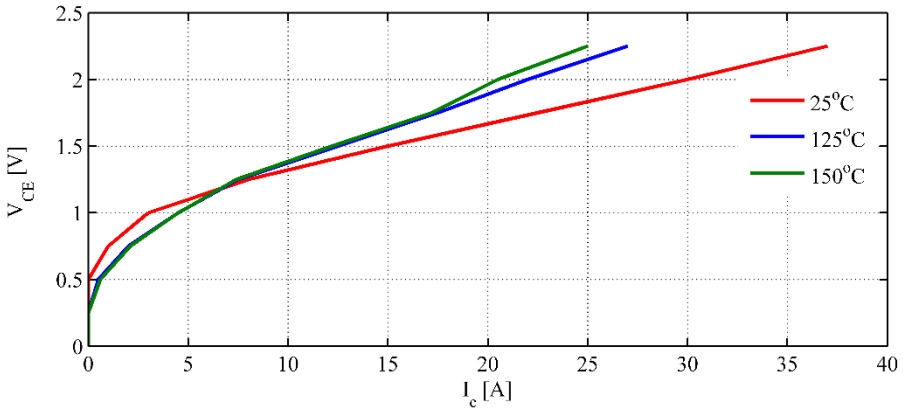


Figure 5.15 Conduction loss profile for Infineon F12-25R12KT4G IGBT switches.

The switching loss profile can be seen in the Figure 5.14. The conduction loss profile is also defined and shown in Figure 5.15. Using these graphs the simulation software determines the energy depending on the collector-emitter voltage (V_{CE}) and collector current (I_c). To achieve results, the machine was operated using *v/f* control method and was fully loaded when the machine reached steady-state. The loss data are taken by varying switching frequency from 5 – 20kHz and are shown in Figure 5.16.

Table 5.6 Device voltage rating comparison.

		Number of IGBT (voltage rating)	**Number of diode (voltage rating)**	**Number of diodes in rectifier (voltage rating)**	**Capacitor Voltage**
3-L NPC		12 (485 V)	18 (485 V)	6 (970 V)	485 V
Dual equal voltage		12 (485 V)	12 (485 V)	12 (485 V)	485 V
Dual Floating bridge	***Main***	6 (970 V)	6 (970 V)	6 (970 V)	970 V
	Floating	6 (485 V)	6 (485 V)	n/a	485 V

Figure 5.16 shows the converter efficiency at full load (12kW) with varying switching frequencies. It can be seen from the figure, for this particular load, the dual inverter with equal DC link voltage ratio has better efficiency than the other two topologies. The three-level NPC has six extra clamping diodes, thus the losses are higher. The proposed floating bridge topology has slightly better efficiency than three-level NPC converter but is less efficient than dual inverter with the equal DC link voltage ratio. The proposed floating bridge converter has two distinct switching patterns, one is for charging and the other is for discharging, therefore it is difficult to maintain the minimum switch involvement for switching transitions which increase the switching losses.

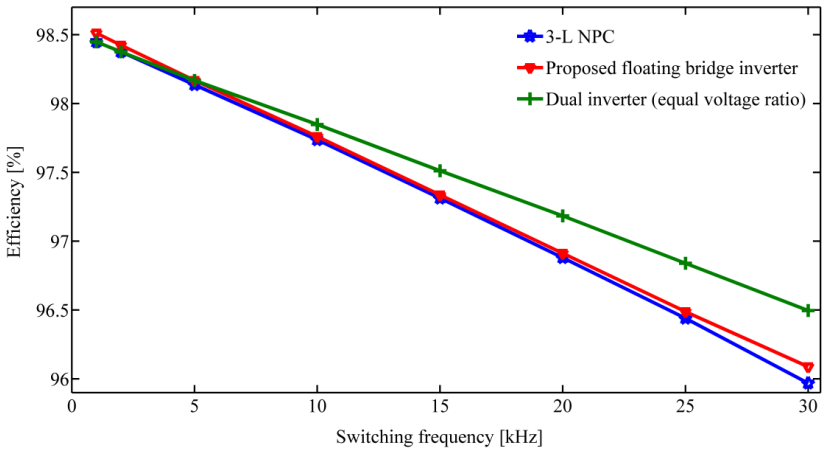


Figure 5.16 Loss comparison in different power converter topologies.

The other disadvantage of the proposed topology is the lower than ideal DC bus utilization which means that the main inverter's devices have to withstand twice the voltage compared to other two topologies described in this section. The reason for using a dual inverter compared to single sided inverters is redundancy for safety critical applications. The proposed converter has advantages where size, weight and redundancy play a crucial role, for example, aerospace, Electric Vehicle (EV) and Hybrid Electric Vehicle (HEV) applications.

5.3 Simulation results

The proposed converter was simulated with closed loop control of an R-L load using PI controllers to achieve control over the load current. A block diagram of the current controlled dual inverter with an R-L load is shown in Figure 5.17. The references are in *d-q* coordinates and achieved using constant block. The three phases to two phase transformation of the load current is achieved using Clarke's transformation [equation 5.6]; the transformation angle is calculated using equation 5.5 and the stationary to rotational reference frame transformation is achieved using equation 5.7.

$$\theta = \int 2\pi f \tag{5.5}$$

Where f is the fundamental frequency set by the designer.

$$X_\alpha = \frac{1}{3}\left[2X_a - (X_b + X_c)\right]$$
$$X_\beta = \frac{1}{\sqrt{3}}\left[X_b - X_c\right] \tag{5.6}$$

$$X_d = X_\alpha \cos(\theta) + X_\beta \sin(\theta)$$
$$X_q = X_\beta \cos(\theta) - X_\alpha \sin(\theta) \tag{5.7}$$

Here, θ is the transformation angle, X represents either the current or the voltage. The subscripts α-β represents the real and imaginary component of the three phase system and d-q represents the component after rotational transformation, which are DC quantities.

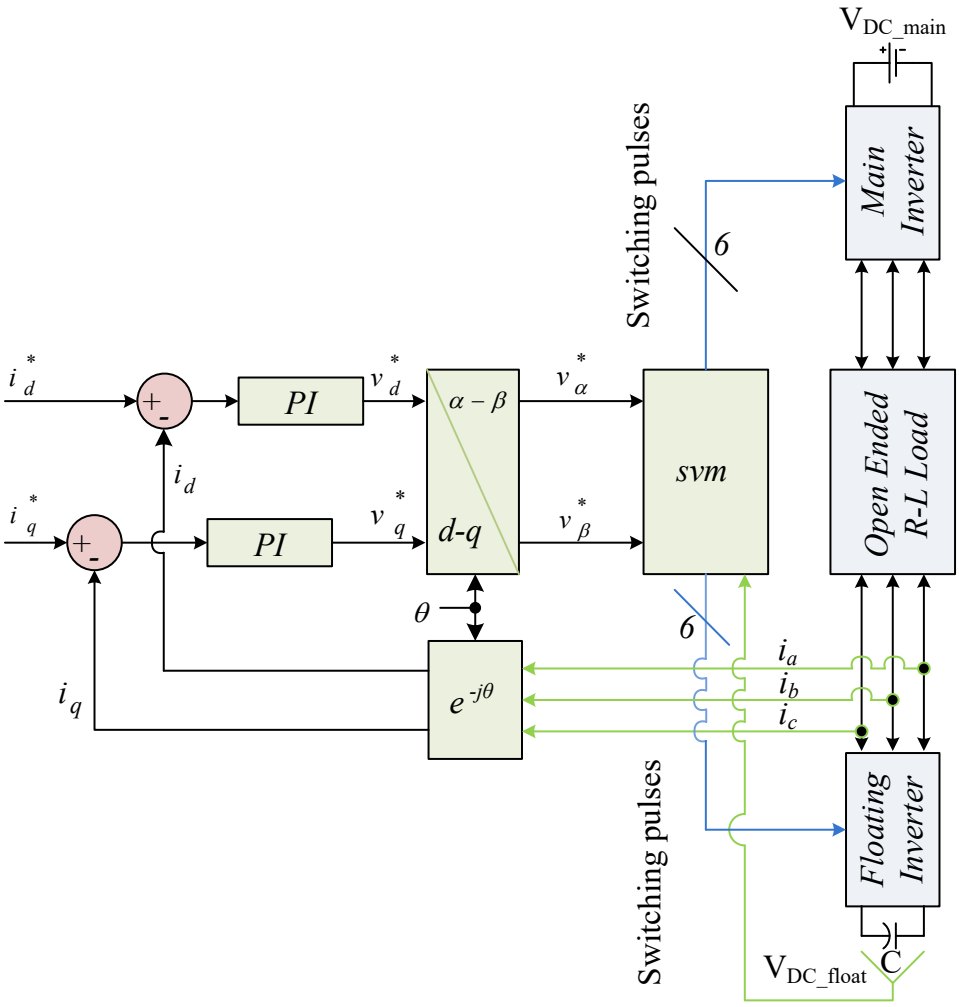


Figure 5.17 Block diagram of current controlled open phase R-L load.

To obtain simulation results with a static R-L load, the main converter was supplied with a constant DC voltage source of 200Volts. The dead-time was set to match the experimental system, 4µs. The floating bridge converter was initially charged to half of the main DC link voltage. The sampling frequency was set to 5kHz and the current direction was identified using a comparator. A current reference of 4Amps was set to show the operation in two-level mode.

Figure 5.18 shows the floating DC link capacitor voltage, output voltage and output current. It can be seen that the converter can control the floating capacitor voltage at the required value and the floating DC link voltage closely follows the reference. A reference current of 9 Amps was set to show the multilevel operation of the converter. It can be seen from Figure 5.19 that the converter can achieve 9 output voltage levels across the load (similar to three-level converters). The converter can control the floating DC link voltage to the required value. Finally, a step change in the reference current was applied from 4Amps to 9Amps to see the dynamic response of the system as shown in Figure 5.20. It can be seen from the figure that load current changes quickly to match the overall reference and these does not have any effect on the floating inverter's average DC link voltage.

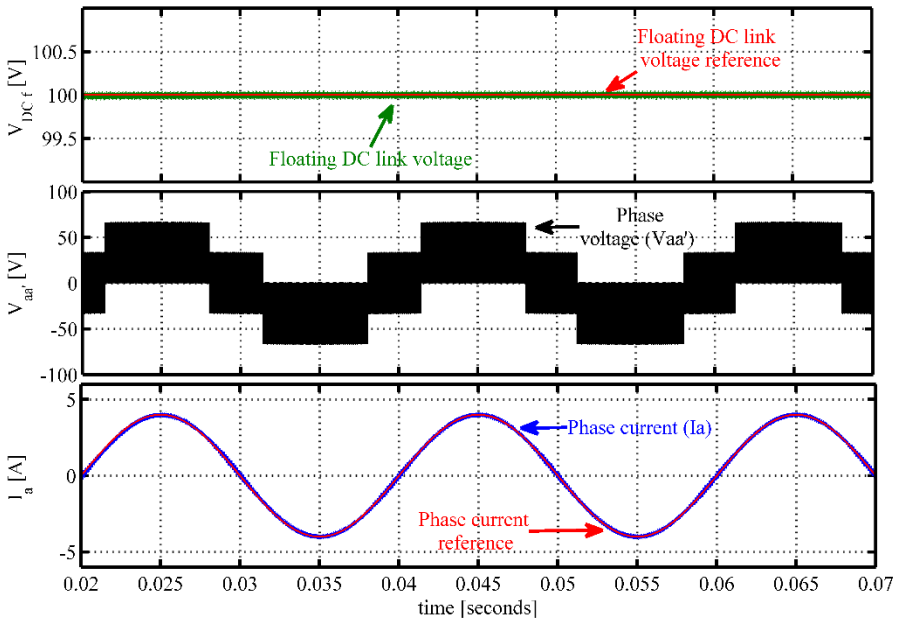


Figure 5.18 Floating DC link voltage, phase voltage and current for R-L load when the reference was set to 4 Amps.

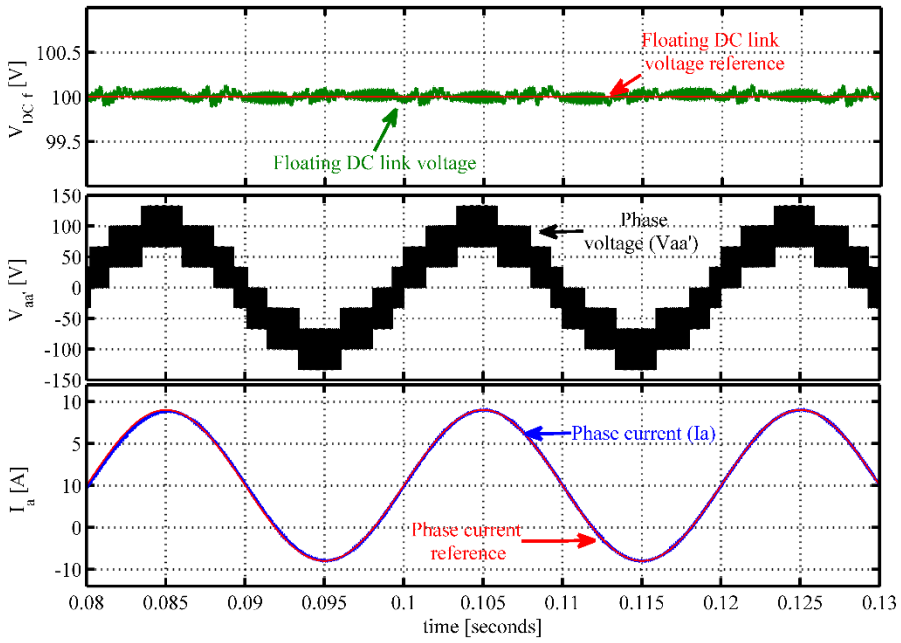


Figure 5.19 Floating DC link voltage, phase voltage and current for R-L when the reference was set to 9Amps.

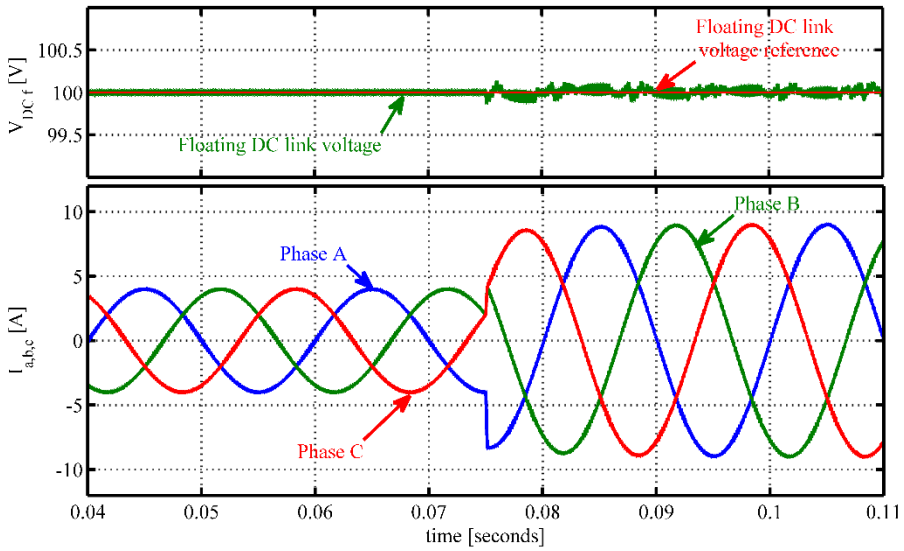


Figure 5.20 Step response of the controller (R-L load) from top to bottom: Floating DC link voltage, three phase currents.

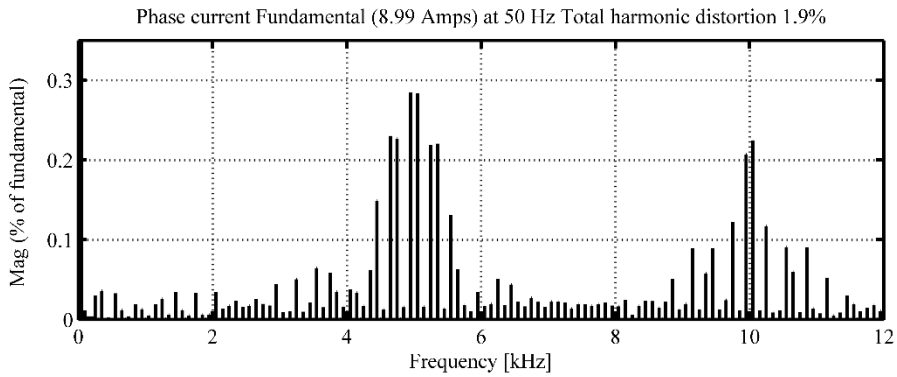


Figure 5.21 FFT of current when the converter was running at three-level mode.

A frequency spectrum of the output voltage and current is shown in Figure 5.21 when the converter was operating at three-level mode. It can be seen from the frequency spectrum that the converter is switching around 5kHz.

To further validate the performance of the proposed inverter an induction motor load was used. The motor drive performance was analysed by running the motor as an open loop *v/f* controlled drive. The *v/f* method is used to maintain the constant flux of the machine by keeping the *v/f* ratio constant under all operating conditions. A block diagram of the *v/f* controlled drive is shown in Figure 5.22.

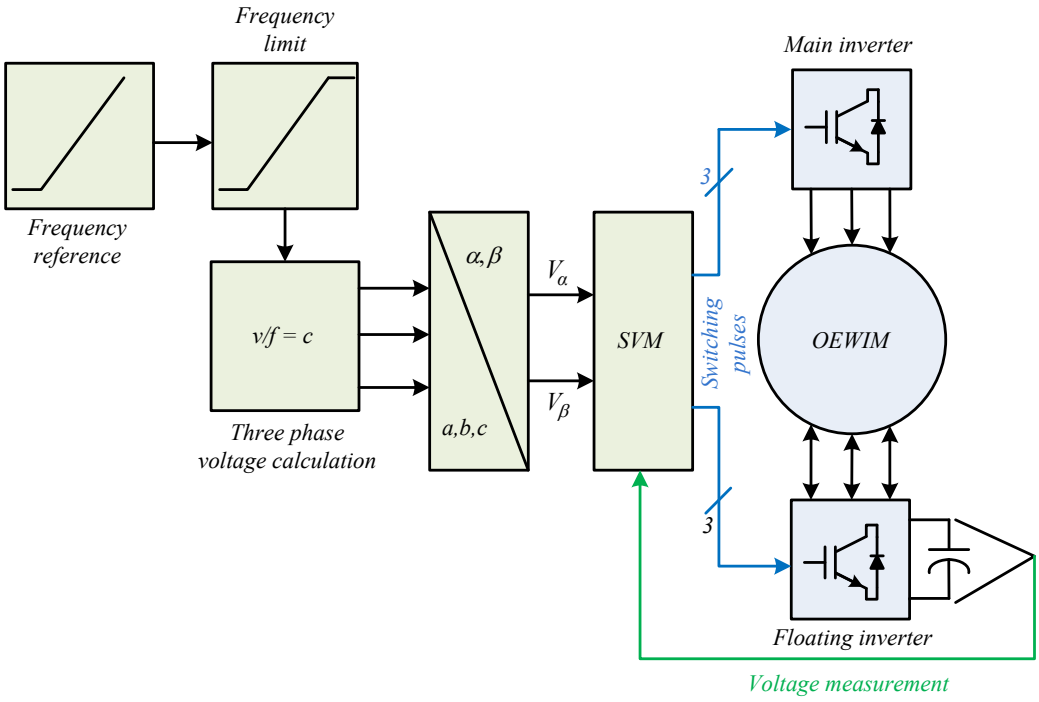


Figure 5.22 Block diagram of open loop *v/f* controlled induction motor drive.

To achieve the results using an induction motor as a load, the main converter was supplied with a constant DC voltage source of 500Volts the aim of the capacitor control was to charge the floating bridge capacitor to 250Volts and to maintain charge under all operating conditions. The switching frequency was set to 5kHz. The results for the open loop *v/f* controlled drive were achieved using MATLAB and PLECS simulation platform as shown in Figures 5.23 and 5.24.

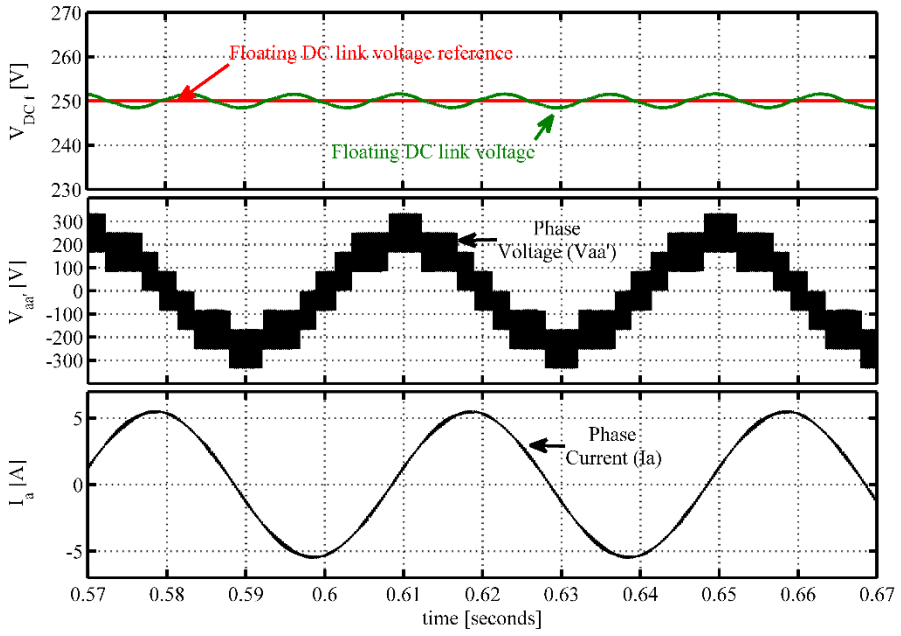


Figure 5.23 Floating DC link voltage, phase voltage and current for open loop *v/f* IM drive when the reference frequency was set to 25Hz.

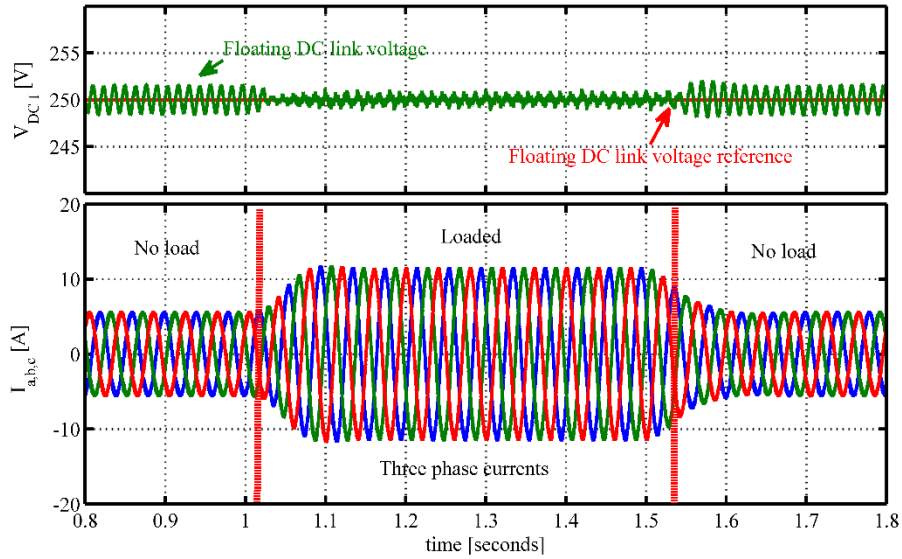


Figure 5.24 Floating DC link voltage and three phase currents for open loop *v/f* IM drive when a load torque was applied to the machine.

Figure 5.23 shows the phase voltage, current and floating DC link voltage when the machine was running at 750 RPM. It is evident from the waveforms that the converter achieves multilevel output voltage waveform and can control the floating capacitor voltage. A step load was applied to the machine after the speed reached steady-state at $t = 1$ second and removed at $t = 1.5$ seconds, shown in Figure 5.24. It can be seen from the figure that the loading has no effect on the average floating capacitor voltage. The floating capacitor voltage ripple increase for no-load operation due to high reactive power demand from the machine. It is difficult to control the floating capacitor voltage with a small real power flow.

Finally, a close loop controller is selected for IM drive to control torque and flux independently. There are two basic and robust controller which are mostly used for industrial applications known as Field Oriented Control (FOC)and the other one is Direct Torque Control (DTC). The DTC is basically a hysteresis type controller where a hysteresis band is defined for rotor flux and torque. The switching sequences are generated to maintain the actual torque and flux value inside the hysteresis band. This type of controller experience torque ripple and has variable output switching frequency [145, 146]. On the other hand, field oriented controllers use machine equations in *d-q* reference frame along with PI based controllers to control the flux and torque of the machine independently. This type of controllers requires a direct or indirect method to calculate the slip angle and susceptible to parameter variations. The advantages of this controller compared to a DTC based controller are the fixed switching frequency and much less torque ripple. Thus an Indirect Rotor Flux Orientation (IRFO) based closed loop control [71]was used to validate the performance of the proposed converter. The voltage values for both the converters kept the same as for the open loop *v/f* control drive. The IRFO based control is one of the standard control techniques for motor drives and widely used. The objective of this controller is to control the induction machine in the same way as a DC machine where the torque and field producing currents have no coupling as well as maintaining constant *v/f* ratio [147]. To decouple torque and flux producing current the rotor flux vector is aligned with the reference *d*-axis component. Therefore the rotor flux q-axis component will become zero. A phasor diagram of rotor flux orientation is shown in Figure 5.25.

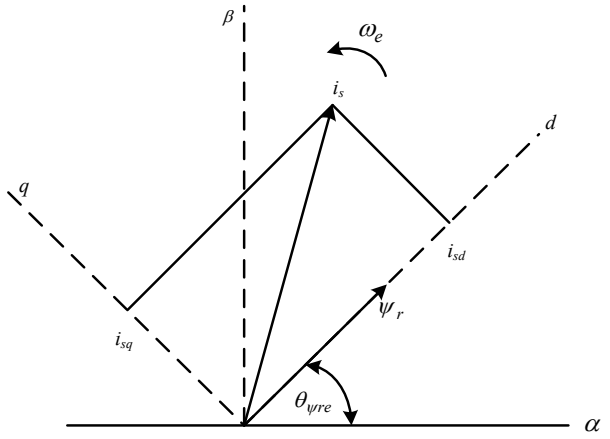


Figure 5.25 Phasor diagram of rotor flux orientation for IRFO based drives.

The rotor flux then can be controlled using stator *d*-axis current component and torque can be controlled independently using stator *q*-axis current. The stator voltage equations for the rotor flux oriented machine can be written as:

$$\begin{aligned} V_{sd}^{*} &= R_s i_{sd} + \sigma L_s \frac{d}{dt} i_{sd} + \left\{ -\omega_e \sigma L_s i_{qs} + \frac{L_m}{L_r} \frac{d}{dt} \psi_{rd} - \omega_e \frac{L_m}{L_r} \psi_{rq} \right\} \\ V_{sq}^{*} &= R_s i_{sq} + \sigma L_s \frac{d}{dt} i_{sq} + \left\{ +\omega_e \sigma L_s i_{ds} + \omega_e \frac{L_m}{L_r} \psi_{rd} + \frac{L_m}{L_r} \frac{d}{dt} \psi_{rq} \right\} \end{aligned} \tag{5.8}$$

The rotor dynamic equations can be written as,

$$\begin{aligned} V_{rd}^{*} &= 0 = \frac{R_r}{L_r} \psi_{rd} - \frac{L_m}{L_r} R_r i_{sd} + \frac{d}{dt} \psi_{rd} - \omega_{sl} \psi_{rq} \\ V_{rq}^{*} &= 0 = \frac{R_r}{L_r} \psi_{rq} - \frac{L_m}{L_r} R_r i_{sq} + \frac{d}{dt} \psi_{rq} + \omega_{sl} \psi_{rd} \end{aligned} \tag{5.9}$$

Here, *V, I, ψ, L, R* and *ω* represent the voltage, current, flux, inductance, resistance and electrical speed. Subscript *sd, sq, rd, rq, e,* and *m* represents the stator and rotor *d-q* axis components, electrical quantity and magnetising quantities respectively. The superscript '*' represents the reference values. The flux linkage equations for the machine in *d-q* reference frame can be written as shown in equation 5.10. The rotor *q*-axis flux component is initially set to zero.

$$\begin{aligned}\psi_{sd} &= L_s i_{sd} + L_m i_{rd} \\ \psi_{sq} &= L_s i_{sq} + L_m i_{rq} \\ \psi_{rd} &= L_r i_{rd} + L_m i_{sd} \\ \psi_{rq} &= 0 = L_r i_{rq} + L_m i_{sq}\end{aligned} \tag{5.10}$$

The magnetising current (i_{mrd}) can be defined as:

$$\psi_{rd} = L_m i_{mrd} \tag{5.11}$$

Substituting equation 5.11 into equation 5.9 the decoupled vector equations can be achieved.

$$\begin{aligned}i_{sd} &= \frac{L_r}{R_r}\frac{d}{dt} i_{mrd} + i_{mrd} \\ \omega_{sl} &= \frac{R_r}{L_r i_{mrd}} i_{sq}\end{aligned} \tag{5.12}$$

Here, subscript '*sl*' represents the slip values. It can be seen from the equation 5.12 that the machine flux can be controlled using the stator *d*-axis current component and the slip of the machine (torque) can be controlled using the stator *q*-axis current and that they are independent of each other. These equations are called the vector controlled equations, derivations of these equations are shown in Appendix D. If the machine is operating in the base speed region then the rotor flux current component is equal to the stator *d*-axis current component, as shown in equation 5.13. The transformation angle to align the rotor flux *q* component to the rotor *q*-axis reference frame is calculated using equation 5.14.

$$i_{sd} = i_{mrd} \tag{5.13}$$

$$\theta^e_{\psi r} = \int \left[\frac{\omega^e_r}{2} + \omega_{sl} \right] dt \tag{5.14}$$

The IRFO based IM dynamic control equations are given in equation 5.8 to equation 5.14. Using these equations a model is created using the MATLAB and PLECS simulation platform. A block diagram of the complete drive system is shown in Figure 5.26. The design of the PI controllers are shown in Appendix E. In the simulation the floating capacitor is initially charged to 200 Volts and the reference for the floating DC link voltage is set to 250 Volts. The machine is initially supplied with rated d-axis (magnetising) current. The results are shown in Figure 5.27. It can be seen that floating capacitor voltage reaches the reference voltage value in 0.7 seconds and this control has no effect on stator *q*-axis current component. A step speed command from 0 to 700 rpm was applied to the controller after the floating capacitor voltage reaches steady-state, the results are shown in Figure 5.28. It can be seen that the *q*-axis (torque-producing) current steps up immediately to provide the maximum available torque to overcome the inertia of the machine. The speed transient is fast and speed reaches steady state in 0.1 seconds.

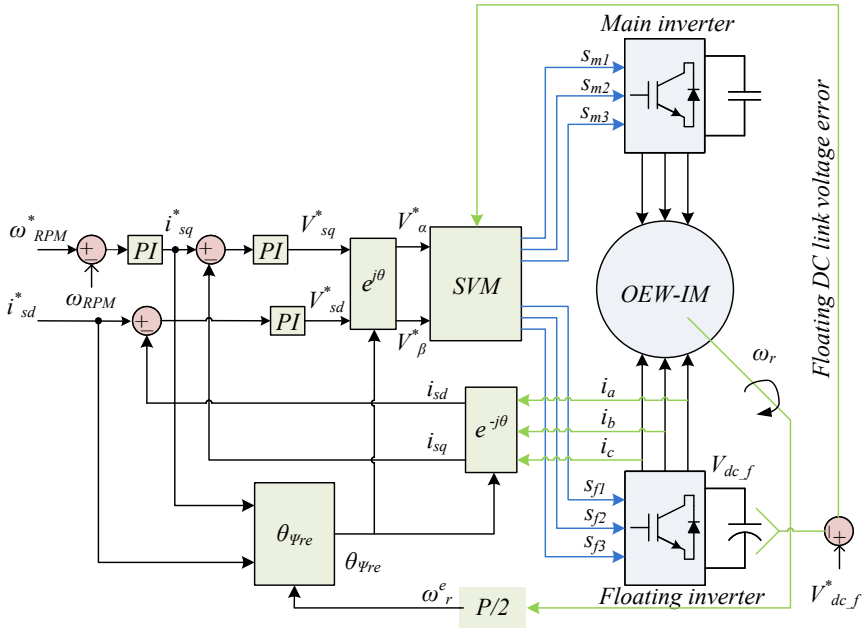


Figure 5.26 A block diagram of IRFO based OEWIM drive.

The capacitor voltage fluctuates after speed reaches steady state as there is not enough real power flowing through the system to charge or discharge the capacitor quickly due to the no-load condition. A step load was applied to the machine after the speed reaches steady state speed of 700 rpm. A step load of 25 Nm was applied to the machine and the results are shown in Figure 5.29. It can be seen that the q-axis

current steps up immediately to counter load torque and control the motor speed. The rotor speed does decreases momentarily when the load torque was applied to the machine but recovers in 0.1 seconds. The capacitor voltage fluctuates during the no load operation of the motor drive but the capacitor voltage control improves under load due to real power flow through the power converter.

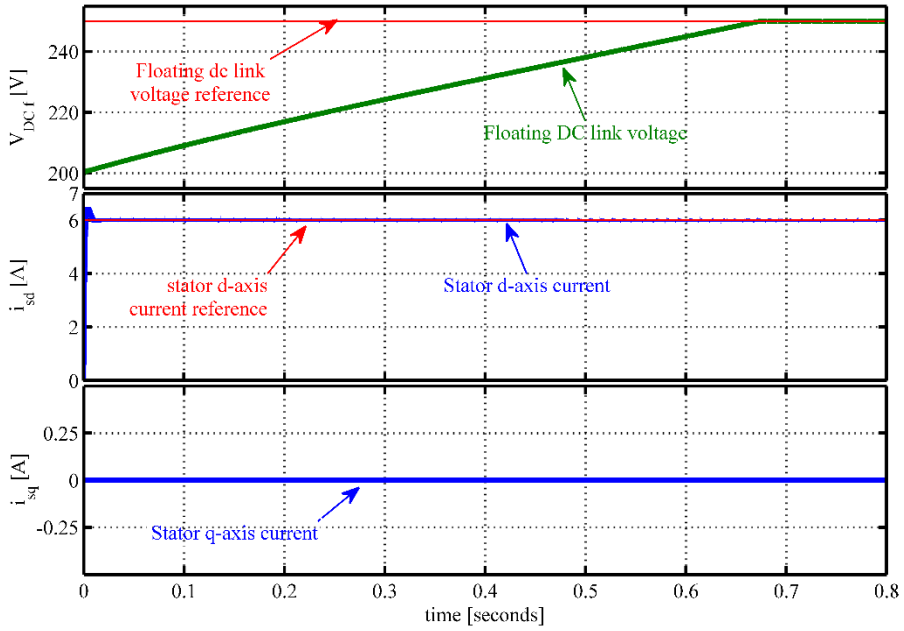


Figure 5.27 Initial charging of floating capacitor after machine was magnetised.

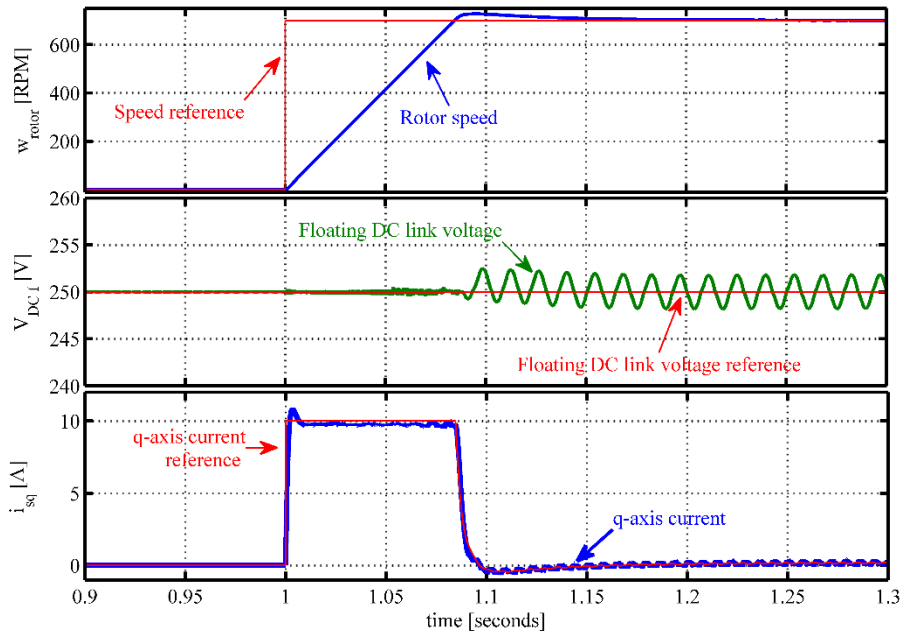


Figure 5.28 FOC response of no load speed to a step reference speed command.

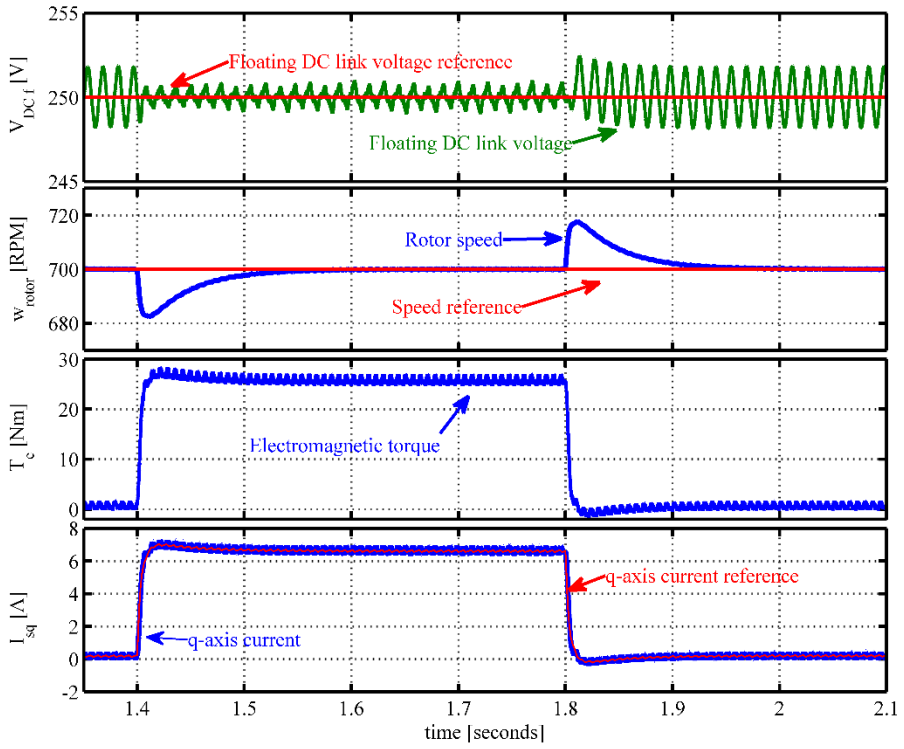


Figure 5.29 FOC response to a step load applied after the speed reaches steady-state.

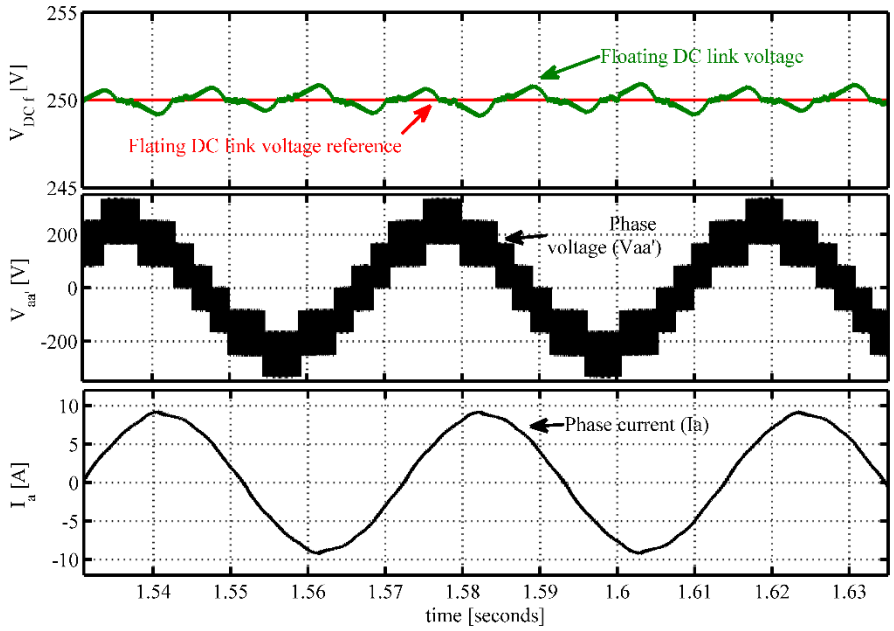


Figure 5.30 Floating DC link voltage, phase voltage (V_{aa}') and phase current (I_a) when the machine was loaded.

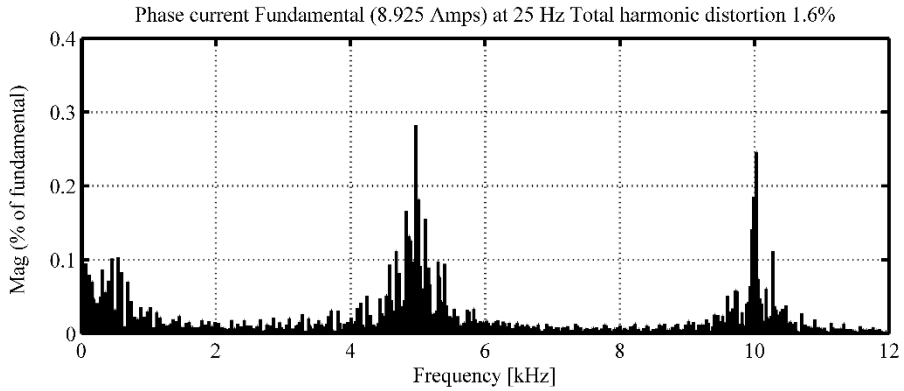


Figure 5.31 FFT of phase current when the machine was loaded.

The output voltage and current of the machine are shown in Figure5.30 for the loaded condition. It can be seen that the converter can achieve a multilevel output voltage waveform and is able to control the floating capacitor voltage under any operating conditions. A frequency spectrum for the voltage and current is shown in Figure 5.31 and it can be seen that the harmonic spectrums are clustering around the harmonics of the switching frequency.

5.4 Conclusion

This chapter has presented a dual inverter topology where one of the bridges is floating. The conventional dual inverter topology requires isolation transformer and additional rectifier which can increase the weight of the system. The proposed converter does not require any isolation transformer and eliminates the need for rectifier thus the power to weight ratio for the system improves. A detailed analysis is presented to identify the charging and discharging switching states along with limits to the modulation index. The dead-time spike due to simultaneous switching of the two converters is also avoided by altering the switching pulses. A loss calculation is presented to compare the converter losses with two other topologies (the dual inverter with isolated DC sources and the single ended NPC converter). Finally, a space vector modulation scheme is used for the converter and results are shown for a static R-L load along with the converter being used as an open and a closed loop induction motor drive. In all cases, the proposed converter achieves multilevel output voltage waveforms and can control the floating capacitor voltage.

Chapter6

Predictive Control of Dual Inverter with one Bridge Floating

This chapter presents the use of model predictive control algorithms in the modulation and control of the proposed dual bridge inverter topology. Predictive control will be used to control the load current and floating capacitor voltage. The advantages of predictive control strategies for the proposed power converter topologies are the faster dynamic response and the control of load currents and DC link voltage in a single, relatively simple control loop than a PI based controller. A method of introducing a fixed modulation frequency in a predictive control algorithm will also be presented, this method overcomes the variable switching behaviour of the traditional model predictive control algorithm which can improve the waveform quality as well as simplify filter design.

6.1 Model Predictive Control

A model predictive control scheme can be used to control the load current and the floating capacitor voltage of the proposed topology. Predictive control uses the finite number of possible switching states generated by the converter [76] and in this case, predicts the load current and floating capacitor voltage which would result from the application of each state. The predicted values are then compared with the reference values at each sample time and the control selects the next switching states to minimise the predicted error [148]. The process in each sampling period for the predictive control algorithm applied to the proposed topology can be summarised as:

- The values of current and floating DC link voltage reference are defined and the actual values are measured.

- The load currents and floating DC link voltage for the next sampling instant are predicted for each valid switching state of the converter.
- A cost function is used to evaluate the cumulative error between references and the predicted values for each switching state, a weighting factor is applied to the floating capacitor voltage term in the cost function to match the error magnitude with current error reference.
- The switching state that generates the minimum value of the cost function is selected and applied to the converter during the next sampling period.

To achieve results a good quality model of the load and converter is necessary for the predictive control algorithm. An ill-defined model will result in the selection of unwanted switching states and the waveform quality will then be lower. The next section will provide a detailed analytical model of the load and the proposed power converter topology. The derived equations will then be applied to the control of the converter and used to provide both simulation and experimental results.

6.1.1 Modelling of the converter

In dual inverter systems, the converter state combinations are selected in such a way that the average generated voltages across the load are 180 degrees phase shifted from the other. Thus the voltages add up across the load terminal to provide, when needed, the maximum available voltage. The leg voltages of each of the converters can be described in terms of switching states and converters DC link voltages using equation 6.1 and 6.2.

$$\begin{aligned} V_{an} &= S_{m1} V_{DC\_m} \\ V_{bn} &= S_{m2} V_{DC\_m} \\ V_{cn} &= S_{m3} V_{DC\_m} \end{aligned} \tag{6.1}$$

$$\begin{aligned} V_{a'n'} &= S_{f1} V_{DC\_f} \\ V_{b'n'} &= S_{f2} V_{DC\_f} \\ V_{c'n'} &= S_{f3} V_{DC\_f} \end{aligned} \tag{6.2}$$

Using Clarke's transformations [149]a balanced three phase system can be represented as two phase *α-β* system using equation 6.3. In equation 6.3 *X* represents either the current or the voltage.

$$X_\alpha = \frac{1}{3}\left[2X_a - \left(X_b + X_c\right)\right]$$
$$X_\beta = \frac{1}{\sqrt{3}}\left[X_b - X_c\right] \tag{6.3}$$

In equation 6.3 subscripts *a, b, c* represents the three phase system, *α-β* represents the two phase system after the application of Clarke's transformations. The output voltage of the converter can, therefore, be synthesized as a function of DC link voltage and the state of the switching devices S_α and S_β in *α-β* coordinate as shown in equations 6.4 to 6.6.

$$V_{\alpha\_m} = S_{\alpha\_m} V_{DC\_m}$$
$$V_{\beta\_m} = S_{\beta\_m} V_{DC\_m} \tag{6.4}$$

$$V_{\alpha\_f} = S_{\alpha\_f} V_{DC\_f}$$
$$V_{\beta\_f} = S_{\beta\_f} V_{DC\_f} \tag{6.5}$$

$$V_\alpha = V_{\alpha\_m} - V_{\alpha\_f}$$
$$V_\beta = V_{\beta\_m} - V_{\beta\_f} \tag{6.6}$$

Here, the components of the main inverter and floating inverters are denoted by subscript '*m*' and '*f*'. The voltages produced by the converter for each switching state are calculated using equations 6.1 – 6.6.

6.1.2 Load modelling

The operation of the proposed converter topology was validated with both a static *R-L* load and with an open end winding induction motor whilst controlling the load current and the floating DC link voltage. To achieve good tracking of the reference current and floating DC link voltage an accurate model of both types of load are required.

$$V_{\alpha\beta} = Ri_{\alpha\beta} + L\frac{di_{\alpha\beta}}{dt} \tag{6.7}$$

The analytical model of an *R-L* load is straight forward as shown in equation 6.7 in *α-β* coordinates. Equation 6.7 can then be used to calculate the predicted current value by decomposing the differential equation in a similar way as for discrete control systems, as shown in equations 6.8 to 6.10.

$$\frac{di_{\alpha\beta}}{dt} = \frac{V_{\alpha\beta}}{L} - \frac{Ri_{\alpha\beta}}{L} \tag{6.8}$$

$$\frac{i_{\alpha\beta}^{k+1} - i_{\alpha\beta}^{k}}{Ts} = \frac{V_{\alpha\beta}^{k}}{L} - \frac{Ri_{\alpha\beta}^{k}}{L} \tag{6.9}$$

$$i_{\alpha\beta}^{k+1} = \left(1 - \frac{RTs}{L}\right)i_{\alpha\beta}^{k} + \frac{Ts}{L}V_{\alpha\beta}^{k} \tag{6.10}$$

Here, *R* and *L* are the load resistance and inductance $i_{\alpha\beta}^{k}$ and $V_{\alpha\beta}^{k}$ are the load current and voltage at current sample time in *α-β* coordinates. The sample time is defined as *Ts* and $i_{\alpha\beta}^{k+1}$ is one sample ahead predicted current values. To control the capacitor voltage the charging and discharging switching combinations are identified the green and red switching sequences as shown in Figure 5.2. The DC link current for the floating DC link is calculated using equation 6.11, which is related to the phase current in *α-β* coordinates and the floating inverters switching state.

$$i_{DC\_f} = S_{\alpha\_f}i_{\alpha} + S_{\beta\_f}i_{\beta} \tag{6.11}$$

The floating DC link current equation can be represented in terms of the floating DC link voltage as shown in equation 6.12. The floating DC link voltage prediction can be found by decomposing equation 6.12 as shown in equation 6.13.

$$i_{DC\_f} = C\frac{dV_{DC\_f}}{dt} \tag{6.12}$$

$$V_{DC\_f}^{k+1} = \frac{Ts * i^{k}_{DC\_f}}{C} + V_{DC\_f}^{k} \tag{6.13}$$

Where i_{DC_f} is the floating inverter's DC link current, C is the floating DC link capacitance, $V_{DC\_f}^{k}$ and $V_{DC\_f}^{k+1}$ are current and predicted capacitor voltages respectively. The calculation time for the control is high and the control action will be delayed in the application by one sample period. To compensate for these time delays the prediction of current and capacitor voltage will simply be two samples ahead of the current values[150]. This is achieved by first calculating the one sample ahead current values using the currently applied voltage vectors as shown in equations 6.10 and 6.13. Then these one sample ahead current predictions are used to calculate the two sample ahead current predictions by utilizing all the available converter voltage vectors to minimise the predicted error, as shown in equation 6.14. The same technique is used to predict the value of floating capacitor voltage at two samples ahead, as shown in equation 6.15.

$$i_{\alpha\beta}^{k+2} = \left(1 - \frac{RTs}{L}\right) i_{\alpha\beta}^{k+1} + \frac{Ts}{L} V_{\alpha\beta}^{k+1} \tag{6.14}$$

$$V_{DC\_f}^{k+2} = \frac{Ts * i^{k+1}_{DC\_f}}{C} + V_{DC\_f}^{k+1} \tag{6.15}$$

where *(k+2)* refers to the predicted value at two sample periods ahead. As the floating DC link voltage does not change by a large amount during one sample period $v_{dc\_float}^{k+1}$ is assumed to be the current floating DC link value. The reference *α-β* currents for *R-L* load are sine and cosine functions which are 90^{o} phase shifted from the other. The converter output current is now predicted two steps ahead but the reference is at present sampling instant. To predict the reference current value at two sample periods ahead a vector angle compensation method is used, as shown in equation 6.16[150]. The reference current value therefore becomes:

$$i^{*k+2} = i^{*k} e^{2j\omega T_s} \tag{6.16}$$

where $k+2$ is two step ahead predicted value, k is the present reference value and ω is the angular frequency of the reference quantities. Cost functions can be calculated using equations 6.17 – 6.19.

$$g_i = \left|\left(i_\alpha^{*k+2} - i_\alpha^{k+2}\right)\right| + \left|\left(i_\beta^{*k+2} - i_\beta^{k+2}\right)\right| \tag{6.17}$$

$$g_{v\_f} = \lambda\left|\left(V_{DC\_f}^{*} - V_{DC\_f}^{k+2}\right)\right| \tag{6.18}$$

$$g = g_i + g_{v\_f} \tag{6.19}$$

$$\lambda = \frac{\left|i^*\right|}{V_{DC\_f}^{*}} \tag{6.20}$$

Where, g_i is the load current cost function, g_{v_f} is the floating capacitor voltage cost function, g is the total cost function and λ is the weighted factor to normalise the floating voltage error in contrast with the current errors.

Finally, an induction motor is modelled to simulate and validate the performance of the converter and the predictive control scheme for a motor drive application. The predictive control chosen to control the IM is a hybrid controller based on PI and predictive control algorithm. The outer speed control loop is slow and using PI based controller will save calculation time without compromising the control dynamics. The predictive current control used for the motor drive is replacing the fast inner current control loop in the IRFO based control shown in Figure5.26. The reference torque producing current, i_{sq} is produced by the PI controller as shown for the IFRO based drive. The control equations are calculated from the stator voltage equations for the rotor flux oriented machine, as shown in equation 5.8. The equations are in rotational d-q reference frame under rotor flux orientation. The transformation from stationary to the rotational frame is achieved using equation 6.21.

$$\begin{aligned} X_d &= X_\alpha \cos(\theta) + X_\beta \sin(\theta) \\ X_q &= V_\beta \cos(\theta) - X_\alpha \sin(\theta) \end{aligned} \tag{6.21}$$

Where subscript d,q and θ represents the d-q axis components and transformation angle respectively. In the equation 6.21, the angle θ will be replaced with $\theta_{\psi r}^{e(k+1)}$ for motor drive application which is the predicted rotor flux angle, shown in equation

6.27. The differential parts of the equation 5.8 are decomposed and the current prediction equations can be derived as is shown in equation 6.22 and in equation 6.23.

$$i_{sd}^{k+1} = i_{sd}^{k} + T_s\left(\frac{V_{sd}^{k} - R_s i_{sd}^{k}}{\sigma L_s} + \omega_e i_{sq}^{k}\right) \tag{6.22}$$

$$i_{sq}^{k+1} = i_{sq}^{k} + T_s\left(\frac{V_{sq}^{k} - R_s i_{sq}^{k}}{\sigma L_s} - \omega_e i_{sd}^{k} - \frac{\omega_e L_m^2 i_{sd}^{k}}{\sigma L_r L_s}\right) \tag{6.23}$$

To calculate the two steps ahead current values the one step ahead values are first calculated using the previously applied voltage vector along with present current (i_{sd} and i_{sq}) values. These one step ahead values are then used to calculate the two step ahead current values, as shown in equations 6.24 and in equation 6.25.

$$i_{sd}^{k+2} = i_{sd}^{k+1} + T_s\left(\frac{V_{sd}^{k+1} - R_s i_{sd}^{k+1}}{\sigma L_s} + \omega_e i_{sq}^{k+1}\right) \tag{6.24}$$

$$i_{sq}^{k+2} = i_{sq}^{k+1} + T_s\left(\frac{V_{sq}^{k+1} - R_s i_{sq}^{k+1}}{\sigma L_s} - \omega_e i_{sd}^{k+1} - \frac{\omega_e L_m^2 i_{sd}^{k+1}}{\sigma L_r L_s}\right) \tag{6.25}$$

The rotor slip angle calculation is based on the magnitude of the *d-q* axis currents and rotor time constant, to predict the accurate currents the slip angle has to be predicted using the one sample ahead current values, shown in equation 6.26. The rotor speed cannot change quickly in a standard 50Hz machine and thus the present value of the rotor speed is used to calculate the predicted rotor flux angle, as shown in equation 6.27. The rotor speed needs to be predicted for high frequency supply machines.

$$\omega_{sl}^{k+1} = \frac{R_r}{L_r i_{sd}^{k+1}} i_{sq}^{k+1} \tag{6.26}$$

$$\theta_{\psi r}^{e(k+1)} = \int\left[\frac{\omega_r^e}{2} + \omega_{sl}^{k+1}\right]dt \tag{6.27}$$

The motor drive control variables are in the *d-q* plane to achieve separate control over the field and torque producing currents. As the controller is in *d-q* plane the converter voltages shown in equations 6.4 to 6.6 can be transferred to *d-q* plane, using equation 6.21. To achieve proper capacitor control a weighting factor is multiplied by the capacitor control cost function term. The resulting cost functions are shown in equations6.28 – 6.30.

$$g_i = \left|\left(i_{sd}^{*k+2} - i_{sd}^{k+2}\right)\right| + \left|\left(i_{sq}^{*k+2} - i_{sq}^{k+2}\right)\right| \tag{6.28}$$

$$g_{v\_f} = \lambda_{dc}\left|\left(V_{DC\_f}^{*} - V_{DC\_f}^{k+2}\right)\right| \tag{6.29}$$

$$g = g_i + g_{v\_f} \tag{6.30}$$

where λ_{dc} is the weighting factor for floating DC link voltage. The calculation of the weighting factor is shown in equation 6.31.

$$\lambda_{dc} = \frac{\sqrt{\left(i_{sd}^{*}\right)^2 + \left(i_{sq}^{*}\right)^2}}{V_{DC\_f}^{*}} \tag{6.31}$$

In equation 6.31 the superscript '*' refers to the reference values, subscript *d-q* represents the rotational *d* and *q* axis quantities and *'DC_f'* represent the floating DC link voltage.

6.1.3 Simulation results

The predictive control algorithm for the proposed converter was simulated using the PLECS and SIMULINK modelling platforms. The control algorithm for the *R-L* load was modelled using equations 6.4 - 6.20, the load parameter values were the same values used in Chapter 5. The main inverter was supplied with a constant DC voltage source of 200Volts and the floating capacitor was initially charged to 100Volts. The reference *α-β* currents were generated using sine and cosine blocks. The dead-time was set to 4μs, similar to the experimental setup.

A block diagram of the control platform is shown in Figure 6.1. A reference current of 4Amps was set to show the converter operation in two-level mode. Figure 6.2 shows the floating DC link capacitor voltage, output voltage and output current. It

can be seen that the converter can control the floating capacitor voltage at the required value and the load current closely follows the reference.

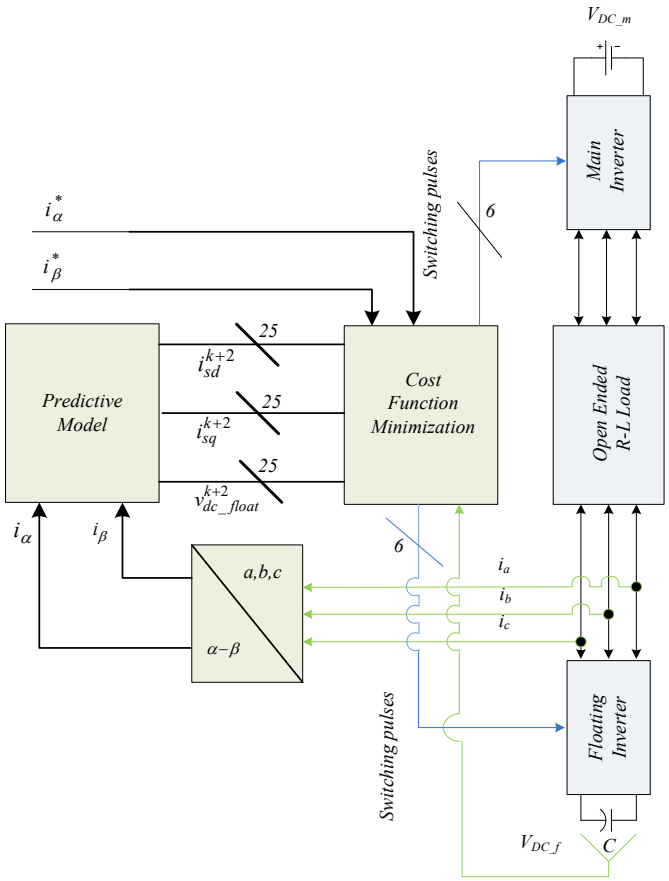


Figure 6.1 Block diagram of predictive current controlled open phase R-L load.

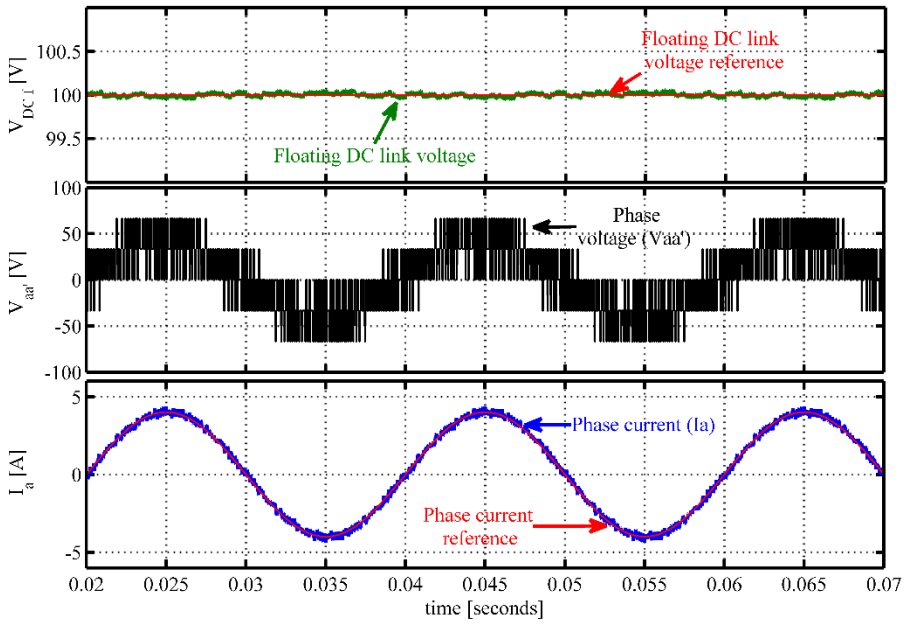


Figure 6.2 Floating DC link voltage, phase voltage and current for R-L load when the reference was set to 4 Amps.

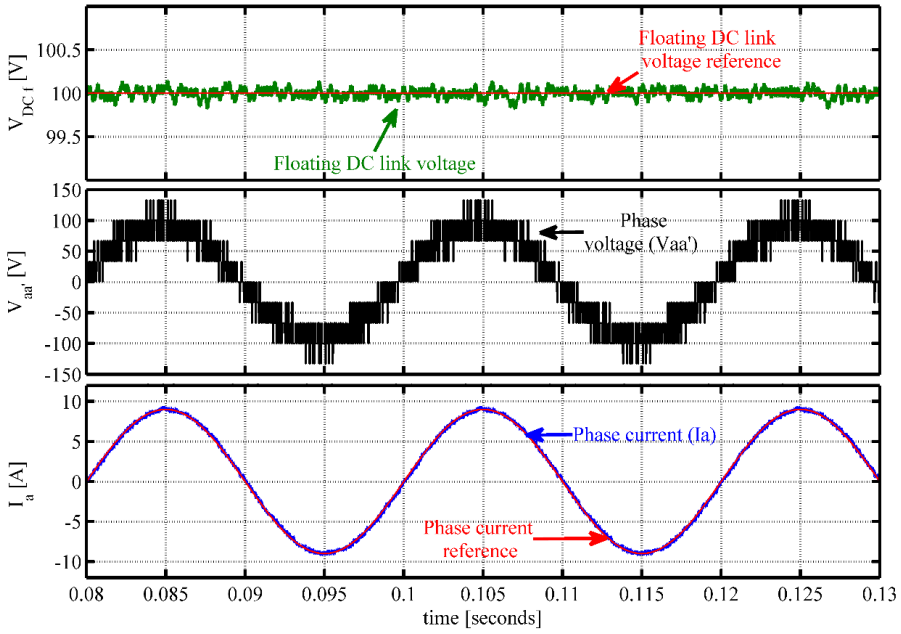


Figure 6.3 Floating DC link voltage, phase voltage and current for R-L load when the reference was set to 9 Amps.

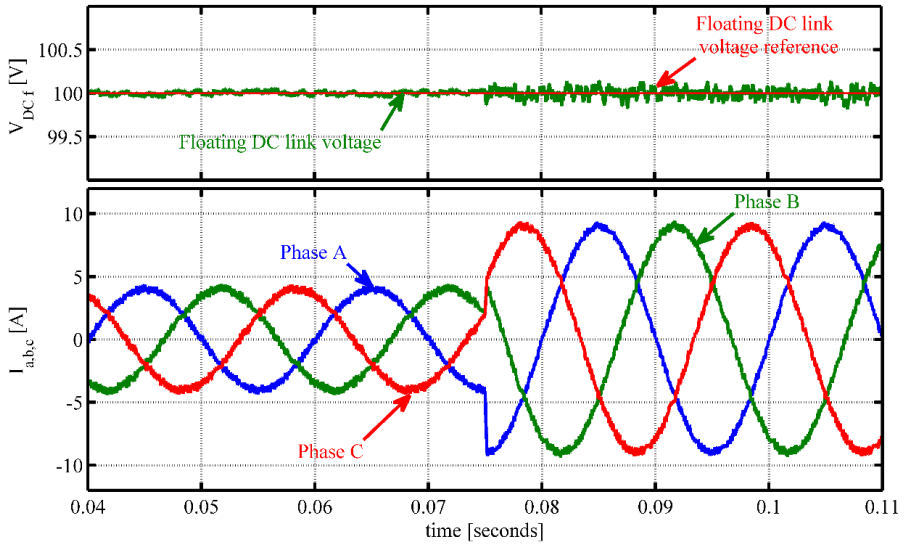


Figure 6.4 Step response of the controller (R-L load) from top to bottom: Floating DC link voltage, three phase currents.

Figure 6.3 shows the converter waveforms for operation with a reference current with a peak value of 9Amps. It can be seen that the load current is following the reference value closely and the converter achieves nine distinct DC voltage levels across the load, similar to a three-level converter. To show the dynamic performance of the controller a step change in the reference current was applied from 4Amps to 9Amps, the resulting controller response is shown in Figure 6.4. It can be seen that

the load current changes quickly to match the overall reference and this transient does not have any effect on floating inverter's average DC link voltage. A frequency spectrum of the load current is also shown in Figure 6.5. The harmonics are spread all over the frequency plane due to variable frequency nature of the controller.

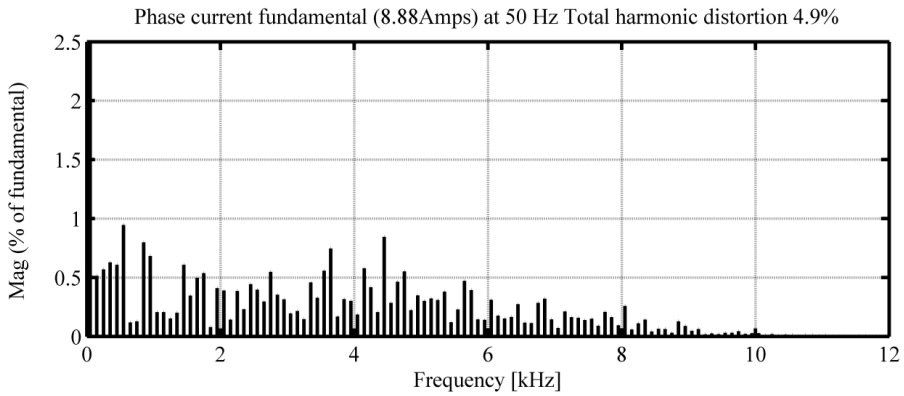


Figure 6.5 FFT of phase current when the when the converter was operating at three-level mode.

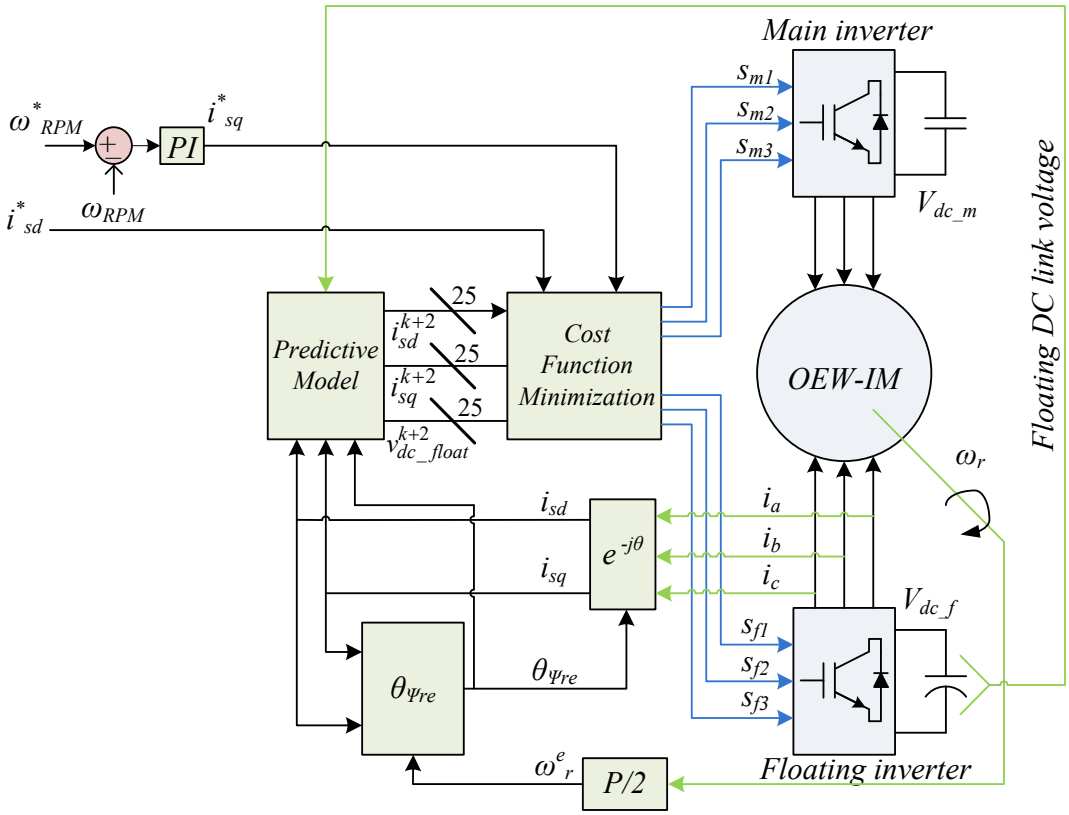


Figure 6.6 Block diagram of induction motor drive using predictive current control of dual two-level inverter with one bridge floating.

To obtain results with an IM the main inverter was supplied with a constant DC voltage source of 500Volts and the floating inverter was initialized with 200Volts.A block diagram of the motor controller is shown in Figure 6.6. A reference for the floating DC link voltage of 250Volts was set after the machine was magnetised. The converter waveforms are shown in Figure 6.7. It can be seen that the floating capacitor voltage charges from 200Volts to 250Volts quickly and can hold its value when the rotor of the machine was at stand-still.

After the capacitor voltage reaches steady-state a step reference speed command of 700 rpm was applied to the controller. It can be seen from Figure 6.8 that the controller provides the maximum available torque to overcome the inertia of the machine. The floating DC link voltage ripple increases after the speed reach steady state, this is due to no load operation of the machine as described in Chapter 5. A step load of 25Nm was also applied to the machine to observe the controller dynamics, as shown in Figure 6.9. It is evident from Figure 6.9 that the hybrid predictive control algorithm can hold the capacitor charge to the required value under all operating conditions. The output voltage and current are shown in Figure 6.10 for operation when the machine was loaded. It can be seen that the proposed system produces multilevel output voltage waveforms and is able to control the capacitor voltage for this electrical machine drive application using predictive current control algorithm.

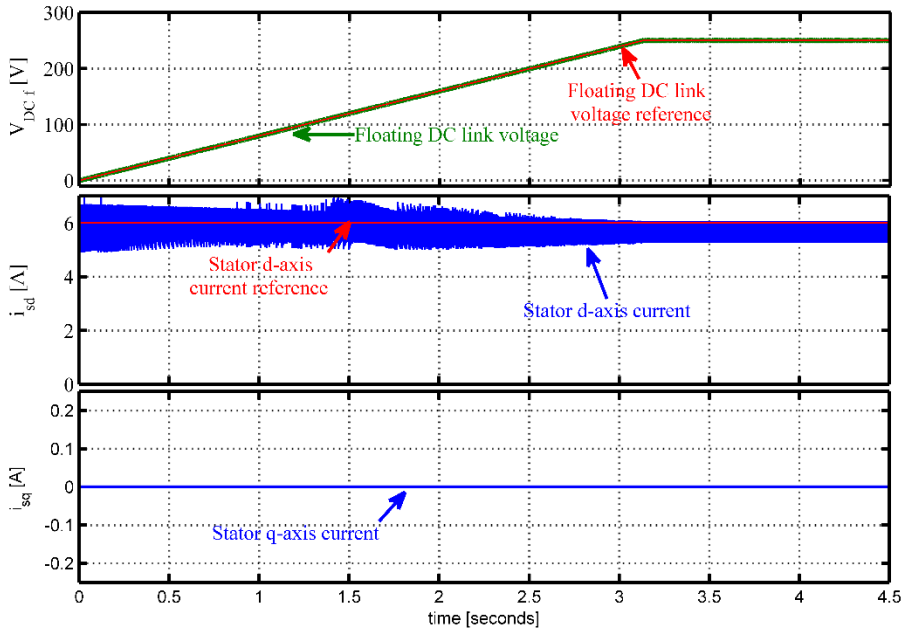


Figure 6.7 Initial charging of floating capacitor after machine was magnetised.

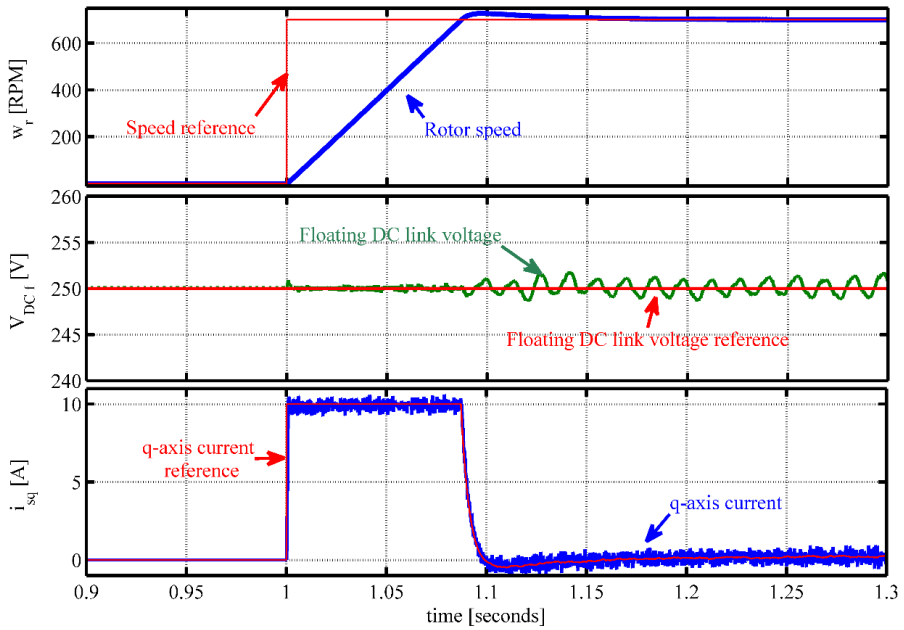


Figure 6.8 Predictive control response of no load speed to a step reference speed command.

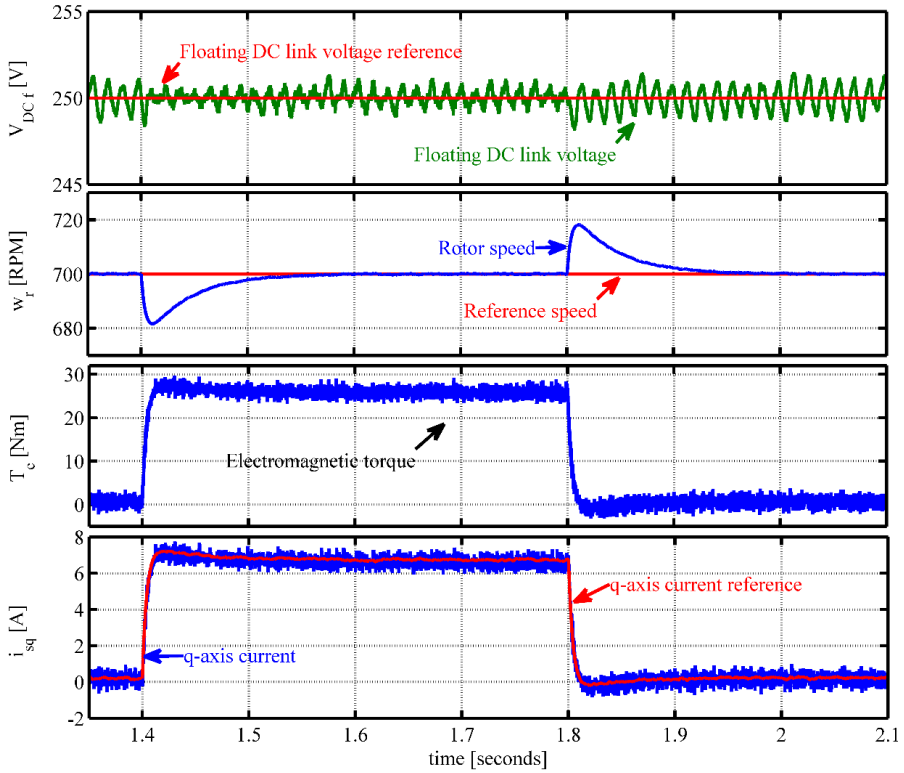


Figure 6.9 MPC response to a step load applied after the speed reaches steady-state

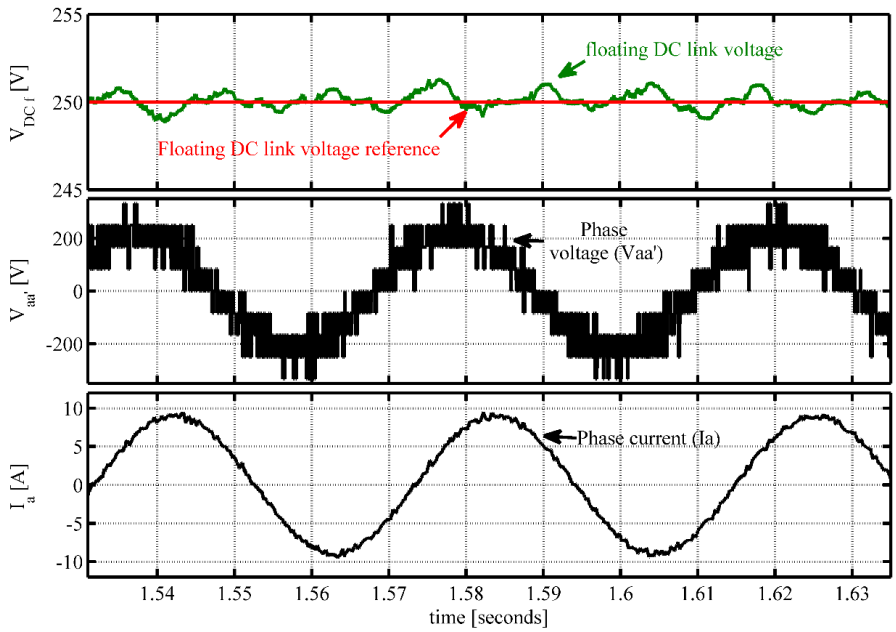


Figure 6.10 Floating DC link voltage, phase voltage (V_{aa}') and phase current (I_a) when the machine was loaded.

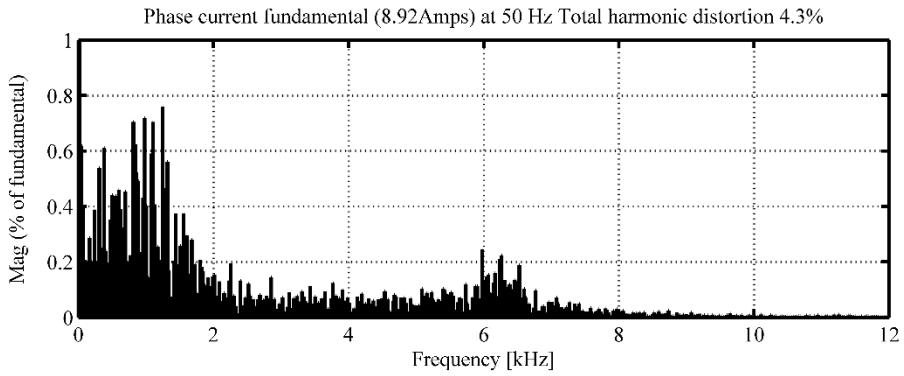


Figure 6.11 FFT of phase current when the when the machine was loaded.

A frequency spectrum for one phase of the output current is shown in Figure 6.11 for the condition when the machine was loaded. The harmonics are spread across the frequency plane, which is expected from predictive control algorithm.

A model predictive control algorithm has been presented in this section along with a selection of results. The results suggest that it is possible to control the proposed system with a predictive control algorithm for both a static R-L load and an IM load. The only challenge is the variable switching behaviour of predictive control algorithm which increases harmonic distortion in the load current. To improve the waveform quality, a modified predictive control algorithm is analysed, named as modulated model predictive control. This analysis is presented in the next section.

6.2 Modulated model predictive control

Modulated model predictive control introduces a modulation scheme in the cost function minimization algorithm to improve waveform quality of a converter [87, 90-92, 151]. This control inherently has all the advantages of the FS-MPC algorithm and avoids increasing the complexity for multi-objective control [86].The control algorithm can be summarised as:

- The values of current and floating DC link voltage reference are defined and the actual values are measured.
- The load currents and floating DC link voltage for the next sampling instant are predicted for all the converter's valid switching states.
- The cost function is calculated for every possible switching state, as shown in equations 6.32 – 6.34.
- The duty cycles are calculated in relation to the calculated cost function values, shown in equations 6.35 – 6.37.
- A Single cost function for each subsector utilising three cost function values multiplied with their subsequent duty cycles is calculated, as shown in equation 6.38.
- A switching sequence similar to an SVM algorithm sequence is used in the modulation.
- The switching sequences which produce the minimum error during the next sampling interval are applied.

To achieve results with the MMPC algorithm two methods are used. The first method is to introduce capacitor control in the cost function minimization algorithm. In this way, the control has to predict the load currents and floating capacitor voltage. The other method is exactly the same as the SVM algorithm, where the charging and discharging switching sequences are identified and the charging algorithm is introduced as a bang-bang control inside the modulation scheme. In this way, the need for capacitor voltage prediction is eliminated and the calculation time will be reduced. Reduction of computational time is always one of the challenges for the practical implementation of predictive control due to the nature of the control design.

Using a simulation study both algorithms were analysed to validate the controller performance and the best algorithm is then used in the practical implementation.

6.2.1Cost function and duty cycle calculation

The space vector diagram for the control of the converter is shown in Figure 6.12. In this figure, the reference voltage resides in sector 1, subsector I. For this case the cost function for the specific sub-sector will be minimised. Sector 1, subsector II will be selected to achieve minimum error in the next sampling interval.

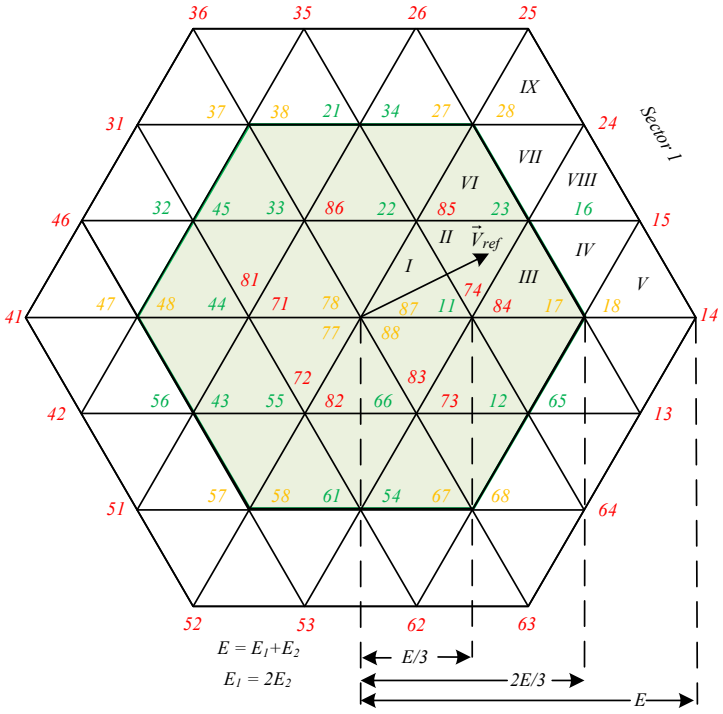


Figure 6.12 Space vector diagram of the proposed system.

The calculation of the cost functions for this particular subsector is shown in equation 6.32 to 6.34, for the case where the capacitor voltage control is integrated into cost function algorithm. The voltage terms inside the cost function equations and the prediction of the capacitor voltage will not be required if the capacitor control is incorporated within modulation scheme.

$$g_{85} = \sqrt{(i_\alpha^* - i_\alpha^{85})^2 + (i_\beta^* - i_\beta^{85})^2 + (V_{DC\_f}^* - V_{DC\_f}^{85})^2} \tag{6.32}$$

$$g_{23} = \sqrt{(i_\alpha^* - i_\alpha^{23})^2 + (i_\beta^* - i_\beta^{23})^2 + (V_{DC\_f}^* - V_{DC\_f}^{23})^2} \tag{6.33}$$

$$g_{84} = \sqrt{(i_\alpha^* - i_\alpha^{84})^2 + (i_\beta^* - i_\beta^{84})^2 + (V_{DC\_f}^* - V_{DC\_f}^{84})^2} \tag{6.34}$$

where, g_{85}, g_{23} and g_{84} are the cost functions for the individual switching combinations *85*, *23* and *84* respectively. The duty cycle is calculated using the cost function values, the larger the cost function the lower the duty cycle. The calculation of the duty cycle for each switching instance is shown in equations 6.35 – 6.37. The complete cost function calculation for this particular triangle is shown in equation 6.38. This is the cost function of the subsector where the reference voltage resides and this cost function needs to be minimised to achieve minimum error in the next sampling interval. A switching sequence is designed after the subsector is selected, as shown in Figure 6.13. Finally, the output voltage of the converter is calculated in order to increase the prediction horizon.

$$t_{85} = \frac{g_{23}g_{84}}{g_{85}g_{23} + g_{85}g_{84} + g_{23}g_{84}} \tag{6.35}$$

$$t_{23} = \frac{g_{85}g_{84}}{g_{85}g_{23} + g_{85}g_{84} + g_{23}g_{84}} \tag{6.36}$$

$$t_{84} = \frac{g_{23}g_{85}}{g_{85}g_{23} + g_{85}g_{84} + g_{23}g_{84}} \tag{6.37}$$

$$G = g_{85}t_{85} + g_{23}t_{23} + g_{84}t_{84} \tag{6.38}$$

The output voltage can be calculated by multiplying the duty cycle with the voltage vector for that particular switching state. The calculation of the output voltage vector in the *α-β* plane is shown in equations 6.39 and 6.40.

$$V_\alpha(k) = [t_{85}V_{\alpha\_85} + t_{23}V_{\alpha\_23} + t_{84}V_{\alpha\_84}] \tag{6.39}$$

$$V_\beta(k) = [t_{85}V_{\beta\_85} + t_{23}V_{\beta\_23} + t_{84}V_{\beta\_84}] \tag{6.40}$$

Where *α-β* represents the real and imaginary axis voltage components produced by the converter. The numbers in the subscript signify the switching sequences. These voltages are calculated to predict one sample ahead current values.

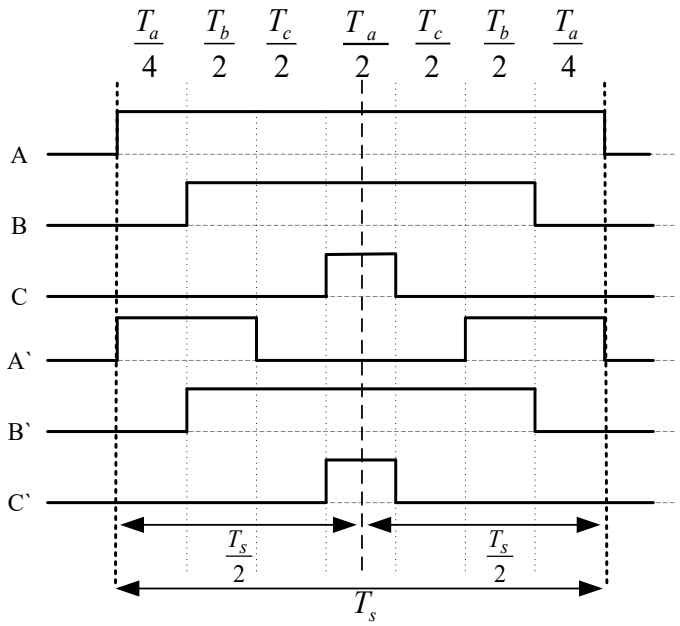


Figure 6.13 Seven segment switching sequence for MMPC algorithm.

These one sample ahead current predictions are used to calculate two samples ahead current predictions utilising all the available voltage vectors to compensate for delays in the close loop system. Using equations 6.32 - 6.40 the modulated model predictive control algorithm can be modelled.

6.2.2 Simulation results

Some results for the converter operating with modulated model predictive current control are described in this section. The control system was designed with the floating capacitor voltage control in the cost function minimization algorithm and with the capacitor voltage control inside modulation scheme. The converter was simulated with an R-L load and the main converter was supplied with a 200Volts DC voltage source, the floating capacitor voltage was kept constant at 100Volts. The sampling frequency was set to 5kHz and the dead time was set to 4μs. The reference α-β currents were generated using sine and cosine functions.

A 4Amps reference current was set to the controller to show the converter operation in two-level mode, the results are shown in Figures 6.14 and 6.15 for capacitor control is incorporated within modulation index and in the cost function algorithm respectively. The results show that for both cases the average floating capacitor voltage is equal to the reference voltage and the load currents are following their reference values closely.

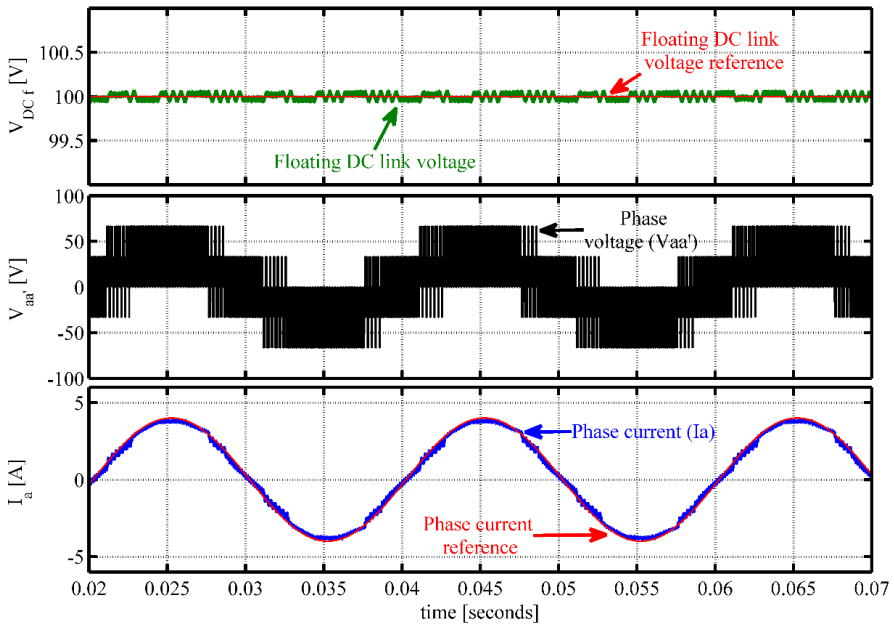


Figure 6.14 Floating DC link voltage, phase voltage and current for R-L load when the reference was set to 4 Amps (capacitor control in cost function).

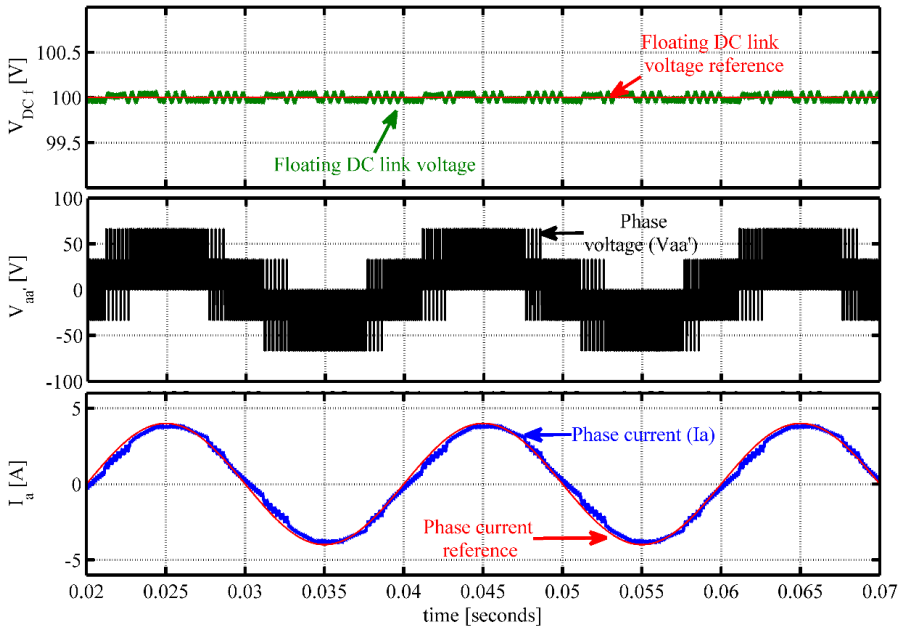


Figure 6.15 Floating DC link voltage, phase voltage and current for R-L load when the reference was set to 4 Amps (capacitor control in modulation).

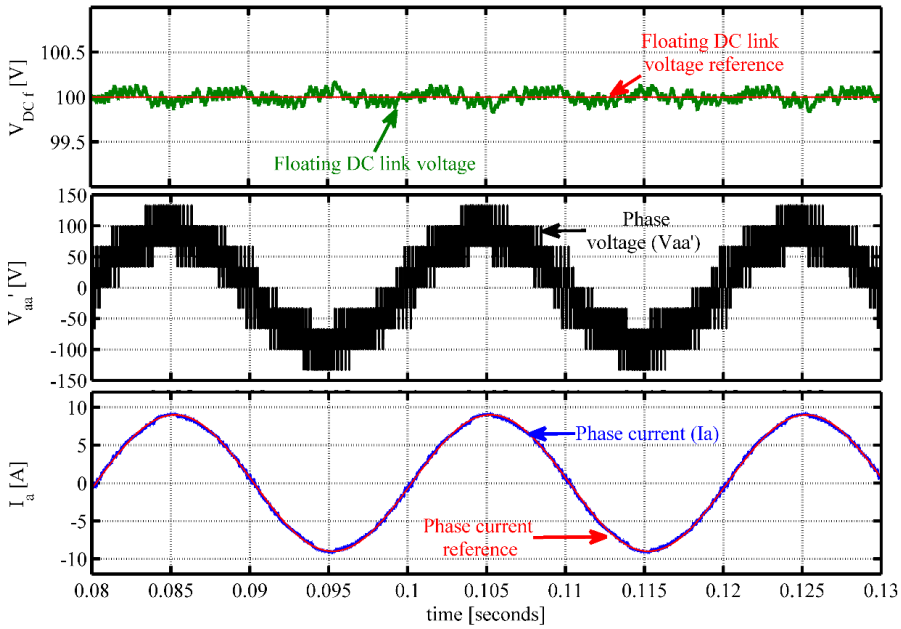


Figure 6.16 Floating DC link voltage, phase voltage and current for R-L load when the reference was set to 9 Amps (capacitor control in cost function).

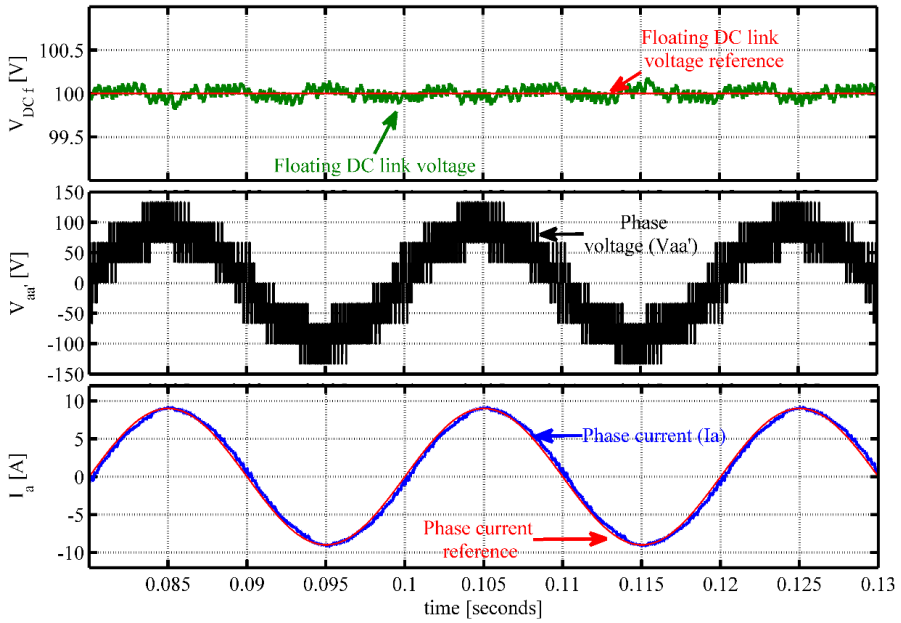


Figure 6.17 Floating DC link voltage, phase voltage and current for R-L load when the reference was set to 9 Amps (capacitor control in modulation).

To show the operation of the converter in three-level mode a 9Amps reference current was set. The results are shown in Figures 6.16 and 6.17. The average floating capacitor voltage is close to the reference voltage and the current waveforms are tracking their references. A step change in the reference current amplitude was then applied to the controller, results are shown in Figures 6.18 and 6.19. It can be seen

that the currents are changing quickly to match the overall reference value. Capacitor voltage deviation increases after the high current was demanded from the system. This is due to the operation of the converter closer to its modulation limit, where a limited number of charging sequences are available.

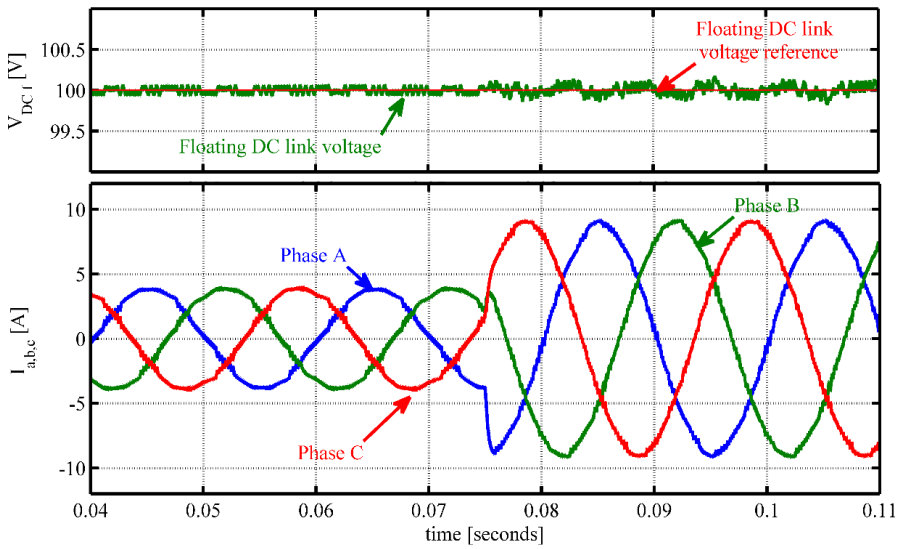


Figure 6.18 Step response of the controller (R-L load) from top to bottom: Floating DC link voltage, three phase currents (capacitor control in cost function).

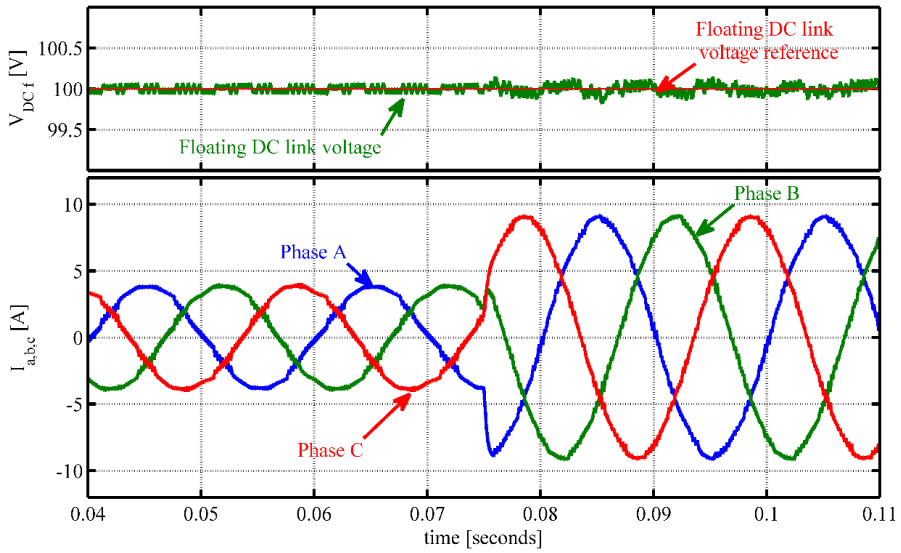


Figure 6.19 Step response of the controller (R-L load) from top to bottom: Floating DC link voltage, three phase currents (capacitor control in modulation).

A frequency spectrum of the load current for both the MMPC algorithms is shown in Figure 6.20 and in Figure 6.21 for the converter operation at multilevel mode. It can be seen that most of the current harmonics are clustering around the sampling

frequency and the harmonics distortions are much lower than the predictive control algorithm shown in Figure 6.5. The frequency spectrum and the control dynamics for both MMPC algorithms show the same results, which suggest that the capacitor control inside modulation scheme will provide the same results along will lower computational time for practical implementation.

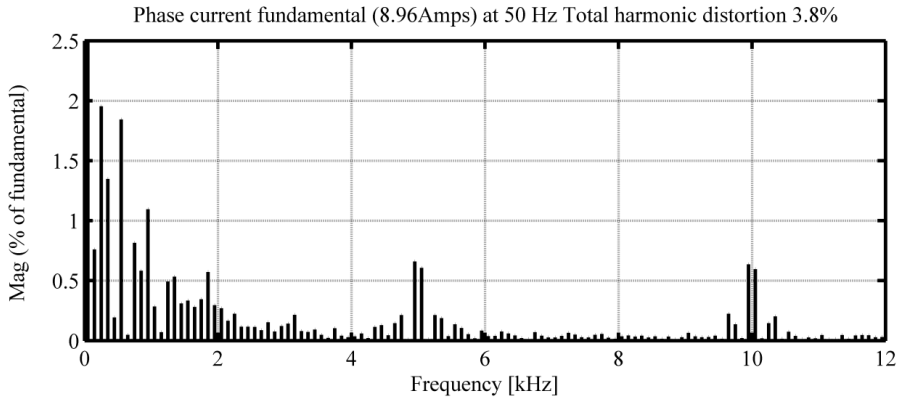


Figure 6.20 FFT of phase current when 9Amps current was demanded from the system (capacitor charging in cost function)

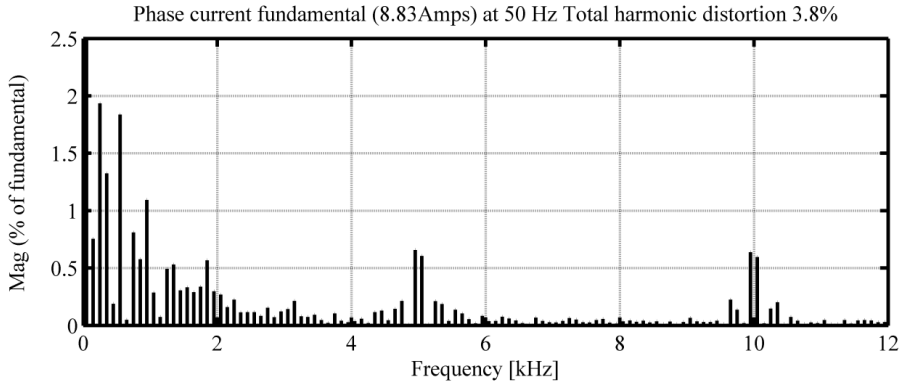


Figure 6.21 FFT of phase current when 9Amps current was demanded from the system (capacitor charging in modulation scheme).

An induction motor drive was simulated to obtain results for the MMPC algorithm for both cases. To achieve the results the main converter was supplied with a constant DC voltage source of 500Volts and the floating capacitor voltage reference was set to 250Volts. The floating capacitor was initially charged at 200Volts. After the capacitor was charged a 6Amps reference magnetising current was set. A reference floating capacitor voltage of 250Volts was set after the machine was magnetised. The effect of the charging transient from 200Volts to 250Volts is

shown in Figures 6.22 and 6.23.It can be seen from the Figures 6.22 and 6.23 that the capacitor charging transient is faster when the capacitor control was incorporated within the cost function minimization algorithm.

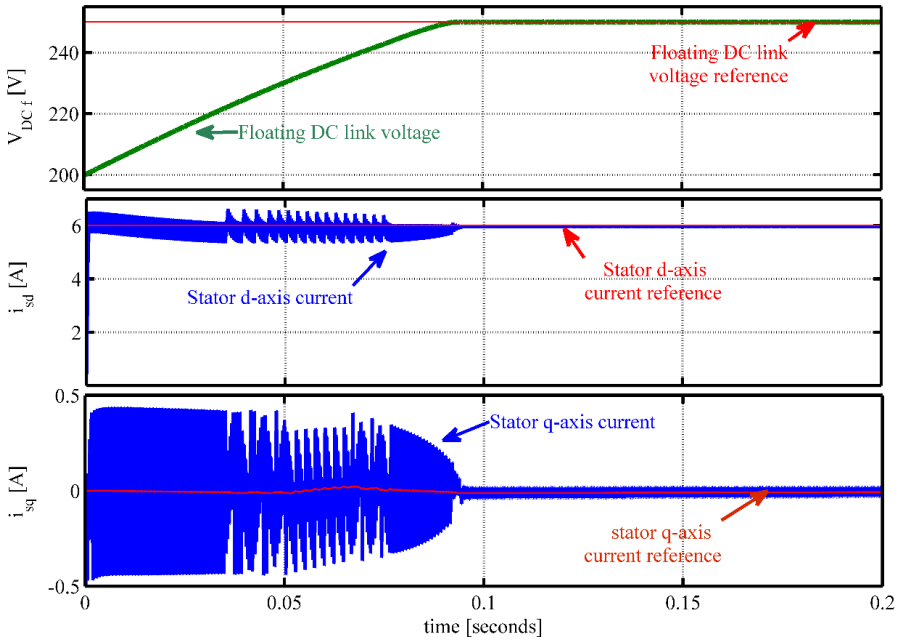


Figure 6.22 Initial charging of floating capacitor after machine was magnetised (capacitor control in cost-function).

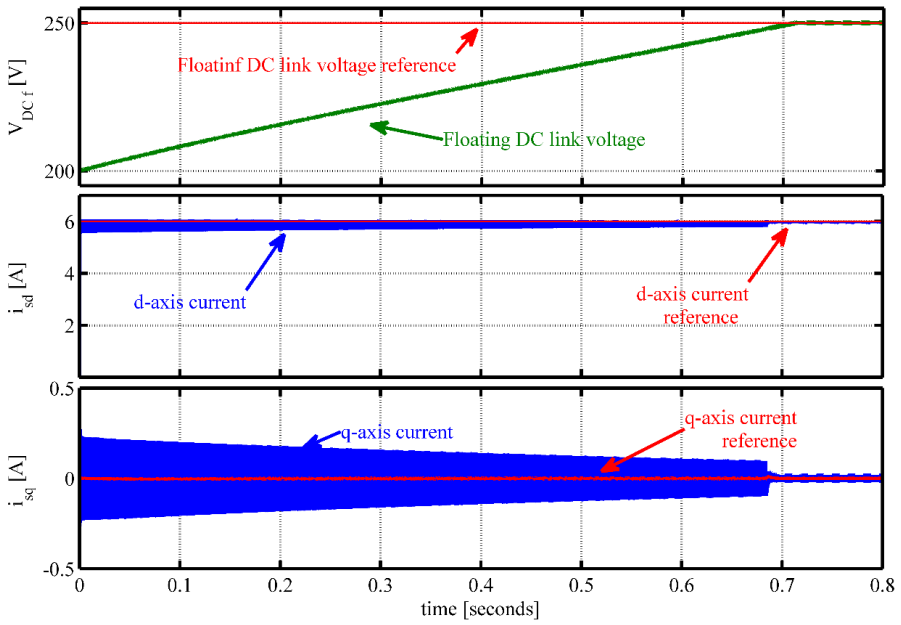


Figure 6.23 Initial charging of floating capacitor after machine was magnetised (capacitor control in modulation).

Similar to all other previously shown motor drive results, a speed demand of 700 rpm was set to the controller after the floating capacitor voltage reached steady-state. The results are shown in Figure 6.24 and in Figure 6.25 for the operation of both MMPC algorithms. The results are as expected, the torque producing current increases very quickly to provide maximum available torque to overcome the machine inertia.

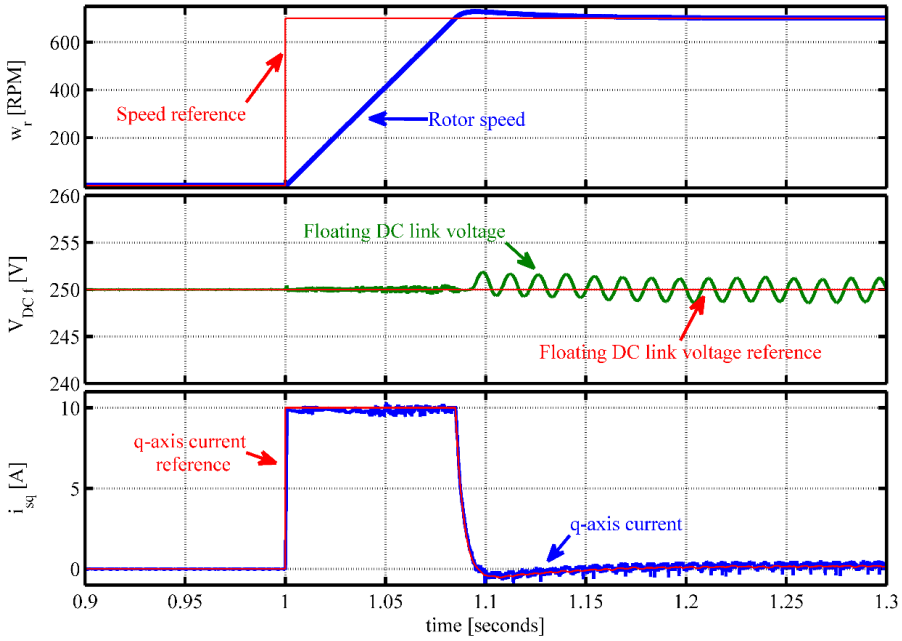


Figure 6.24 FOC response of no load speed to a step reference speed command (capacitor control in cost-function).

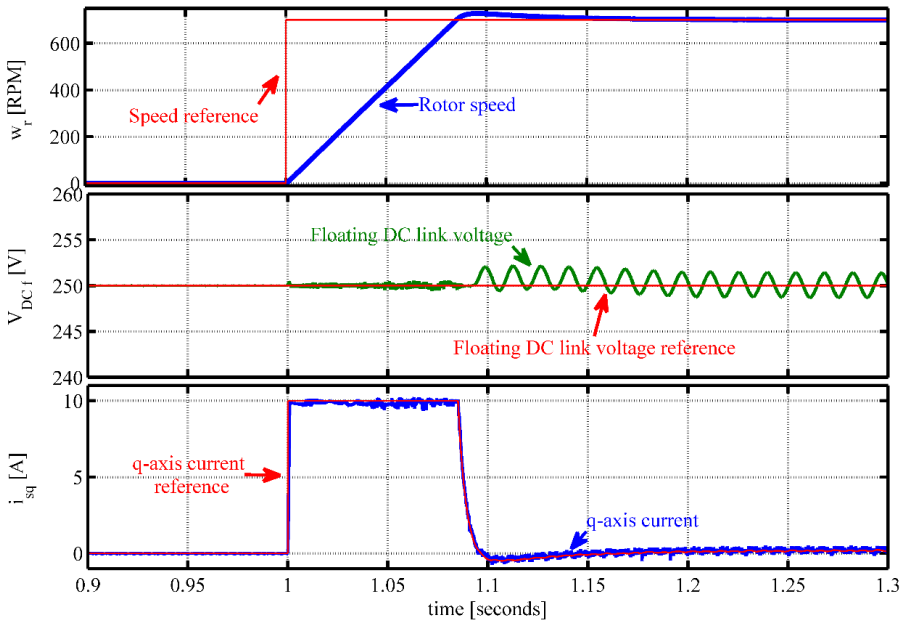


Figure 6.25 FOC response of no load speed to a step reference speed command (capacitor control in modulation).

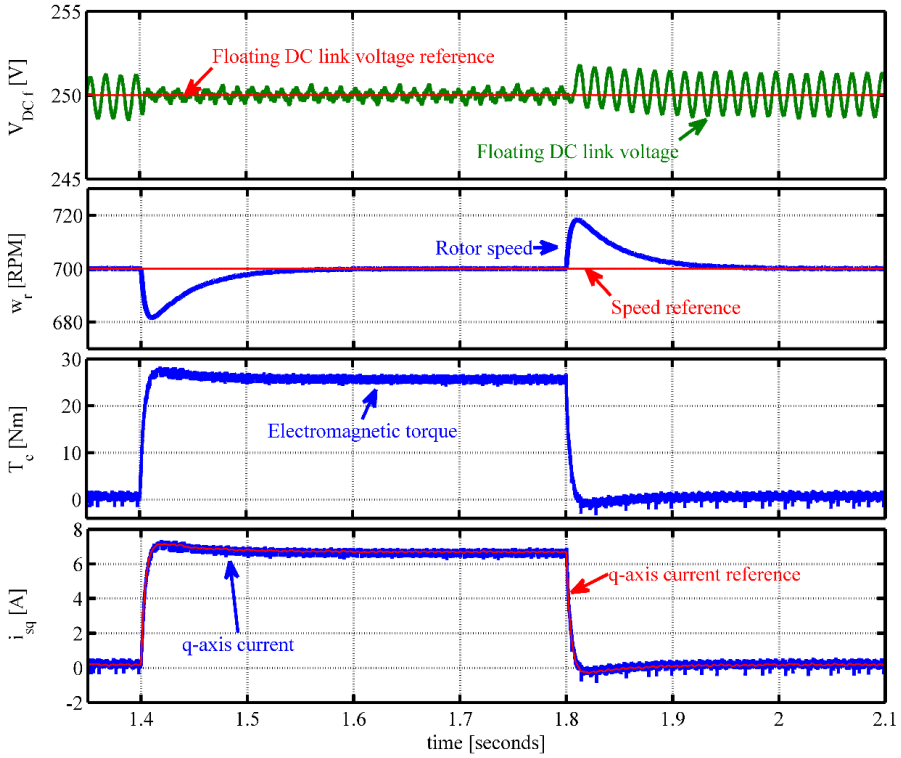


Figure 6.26 FOC response to a step load applied after the speed reaches steady-state (capacitor control in cost function).

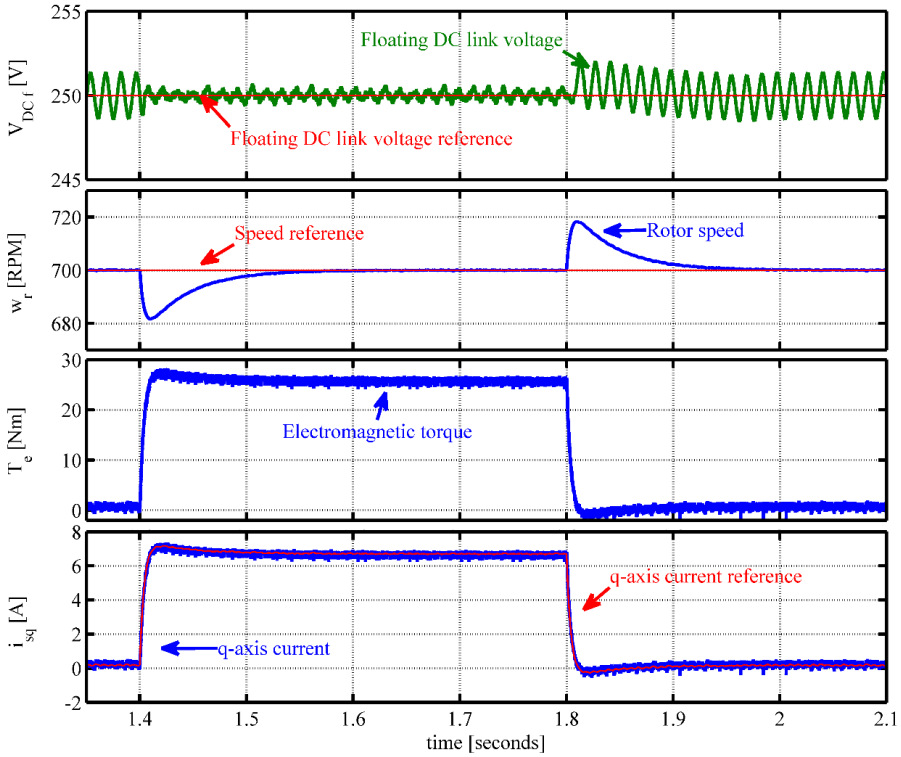


Figure 6.27FOC response to a step load applied after the speed reaches steady-state (capacitor control in modulation).

Finally, a reference load of 25Nm was set, it can be seen from Figures 6.26 and 6.27 that for both MMPC schemes the torque producing current increase quickly to counter the load torque. The capacitor voltage control shows better performance when the machine was loaded, this is due to the real power flow through the system.

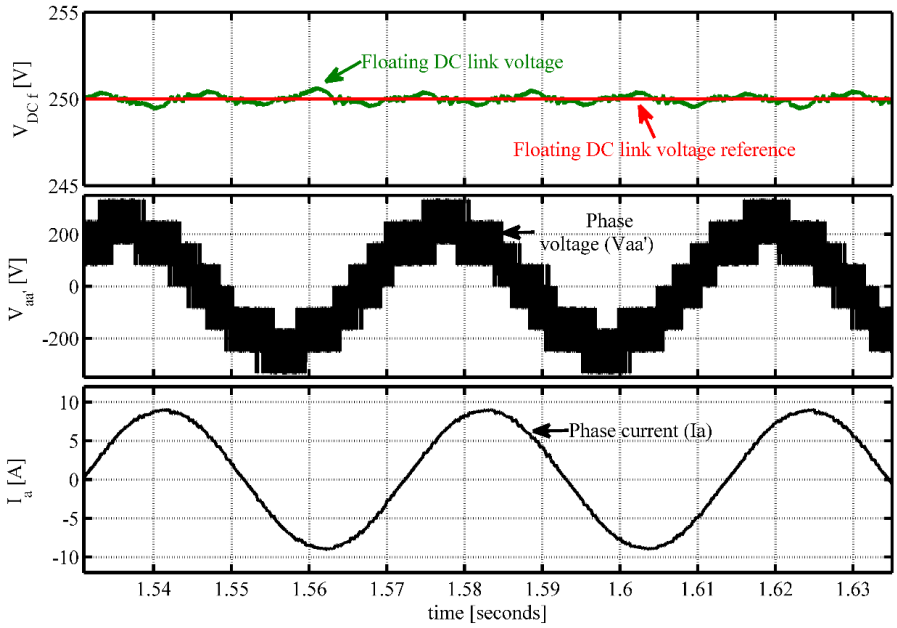


Figure 6.28 Floating DC link voltage, phase voltage and current when the machine was loaded (capacitor control in cost-function).

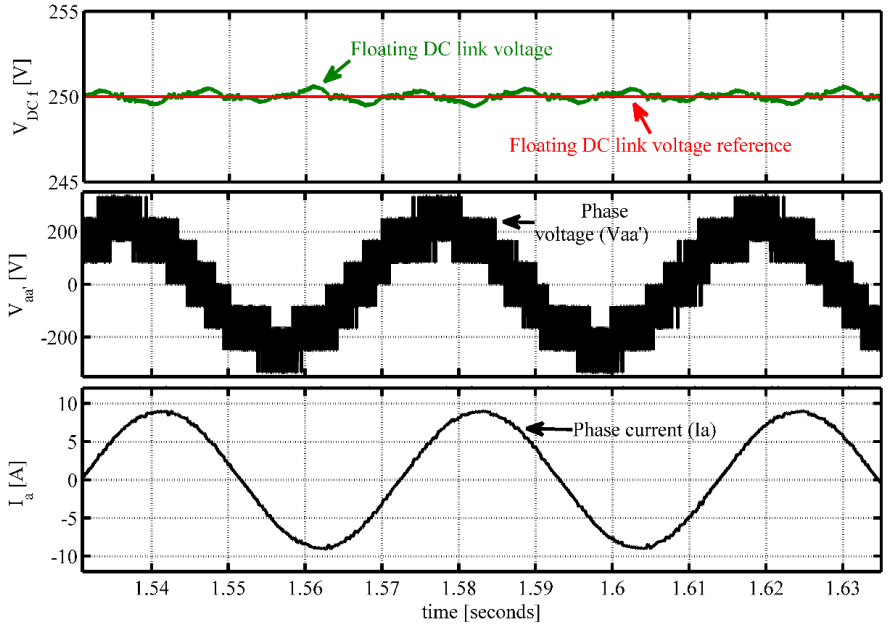


Figure 6.29 Floating DC link voltage, phase voltage and current when the machine was loaded (Capacitor control in modulation).

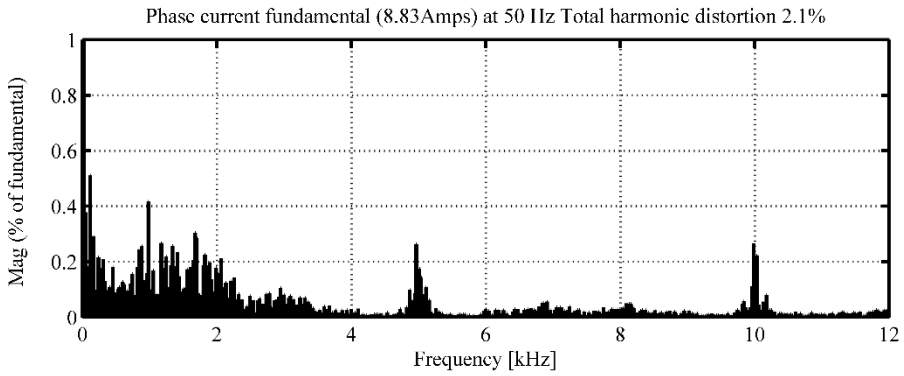


Figure 6.30 FFT of phase current when the machine was loaded (cap-charge in costfunction).

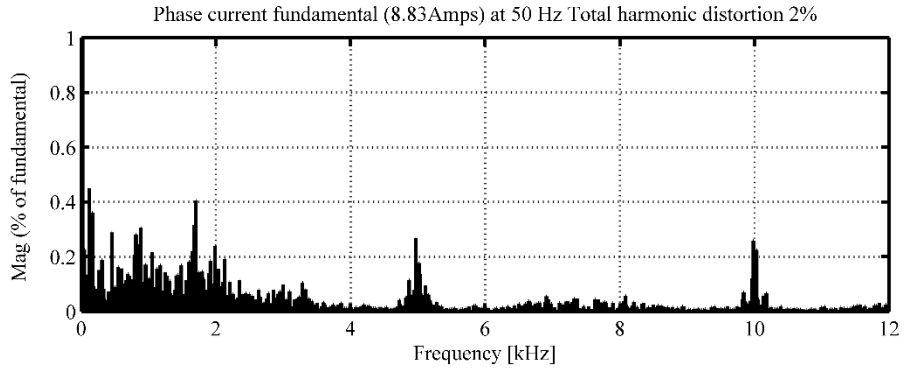


Figure 6.31 FFT of phase current when the machine was loaded (cap-charge in modulation).

The output voltage and current of the machine are shown in Figures 6.28 and 6.29 for the operation when the machine was loaded. In both cases, the average floating capacitor voltage is following the reference closely and the converter achieves nine distinct voltage levels across the load similar to a three-level converter.

A frequency spectrum of the load currents are shown in Figures 6.30 and 6.31, in both cases the THD remains the same. It is also evident from the frequency spectrum that the current THD is much better than for the conventional predictive control algorithm.

6.3 Comparison of control dynamics

A comparison of control systems dynamics and their effect on load current for all three controls strategies presented in this thesis is shown in this section. The comparisons are shown between the PI based controller, predictive control and modulated model predictive control algorithms. The values for the load current THD for all the controllers are shown in Tables 6.1 and 6.2. The predictive control algorithm has an average switching frequency of 3kHz for R-L load and 2.5kHz for

an IM with a sampling frequency of 12.5kHz, as shown in Tables 6.1 and 6.2. It can be seen from the tables that the predictive control algorithm has the highest load current harmonic distortion with more than twice the sampling frequency than modulated model predictive controller. The waveform quality was improved incorporating modulation scheme inside cost function minimization algorithm.

The results shown in Figure 6.32 verify the dynamic response of the controllers when a step change in reference current amplitude was applied from 9Amps to 4Amps with an R-L load. It can be seen that the MPC controller has the fastest dynamic response than the other three controllers. Dynamic responses of the OEW-IM drive are also shown. A response to the magnetising current i_{sd} is shown in Figure 6.33 for a step change in the reference current from 0Amps to 6Amps was applied. It can be seen that the PI based controller has a much slower dynamic response.

Table 6.1 THD comparison of different controllers for R-L load.

Modulation	Sampling frequency (kHz)	Load current THD (%)
PI	5	1.9
MPC	12.5	4.9
MMPC (Cap-charge in cost-function)	5	3.8
MMPC (Cap-charge in modulation)	5	3.8

Table 6.2 THD comparison of different controllers for IM drive.

Modulation	Sampling frequency (kHz)	Load current THD (%)
PI	5	1.6
MPC	12.5	4.3
MMPC (Cap-charge in cost-function)	5	2.1
MMPC (Cap-charge in modulation)	5	2

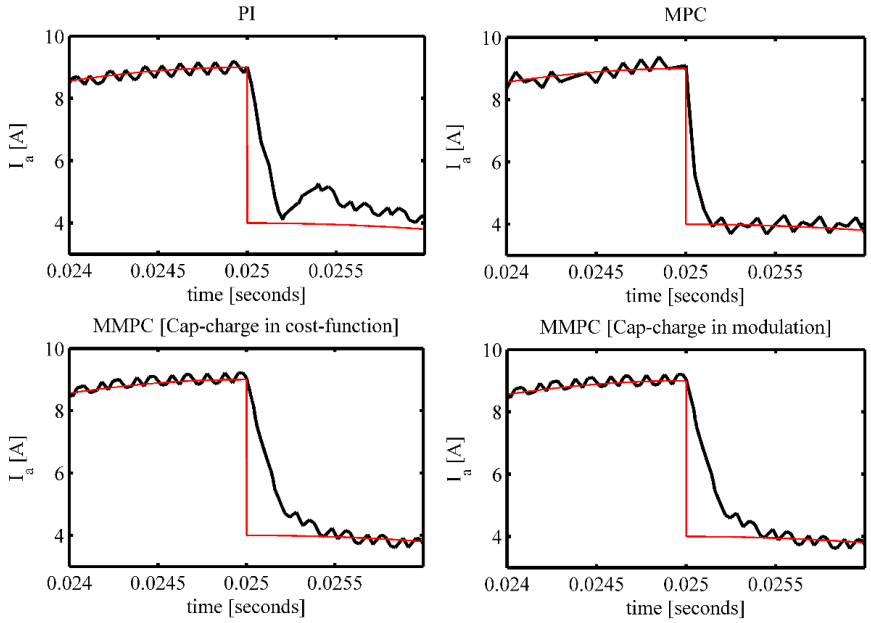


Figure 6.32 Response of control methods for a step change in the amplitude of the reference current for R-L load.

The MPC and MMPC have the fastest response but shows fluctuations in the steady-state region. The predictive control algorithm works like a hysteresis controller, the controller tries to minimise the error in each sample time thus the steady-state fluctuations can be seen. The band of the fluctuation can be decreased by increasing the sampling frequency or by increasing states of the converter.

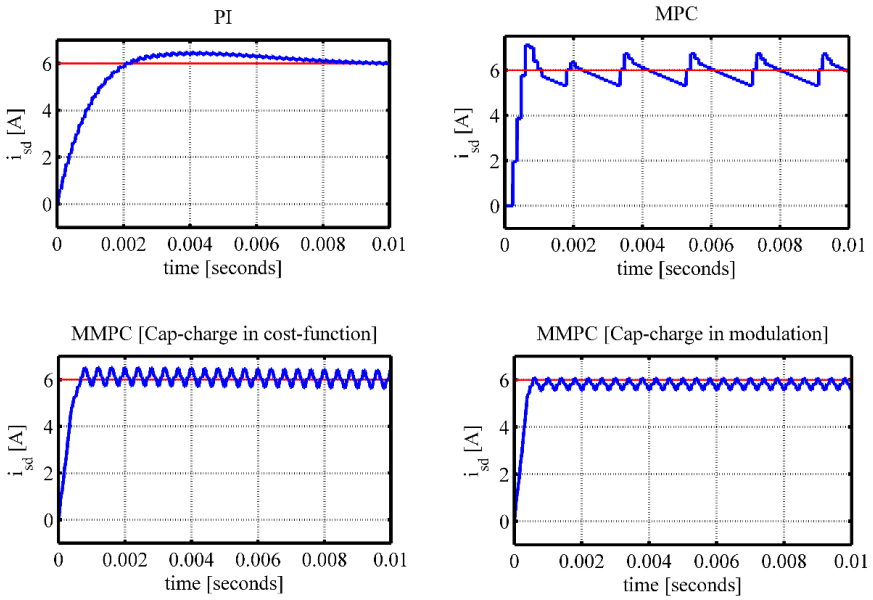


Figure 6.33 Response of control methods for a step change in the amplitude of the reference flux producing current i^*_{sd} for induction motor drive.

The step response of the control methods for a change in the capacitor voltage reference is shown in Figure 6.34 for the condition where the machine was fully magnetised and speed demand was set to zero. It is evident that if the capacitor control is incorporated into the modulation scheme then the transient of the capacitor voltage is slower.

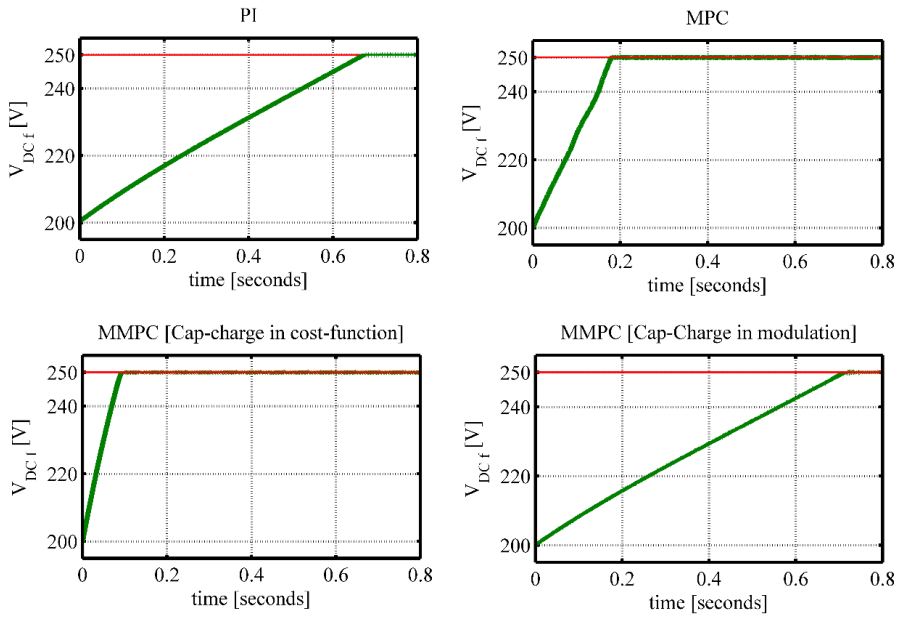


Figure 6.34 Response of control methods for a step change in the amplitude of the reference floating DC link voltage for induction motor drive.

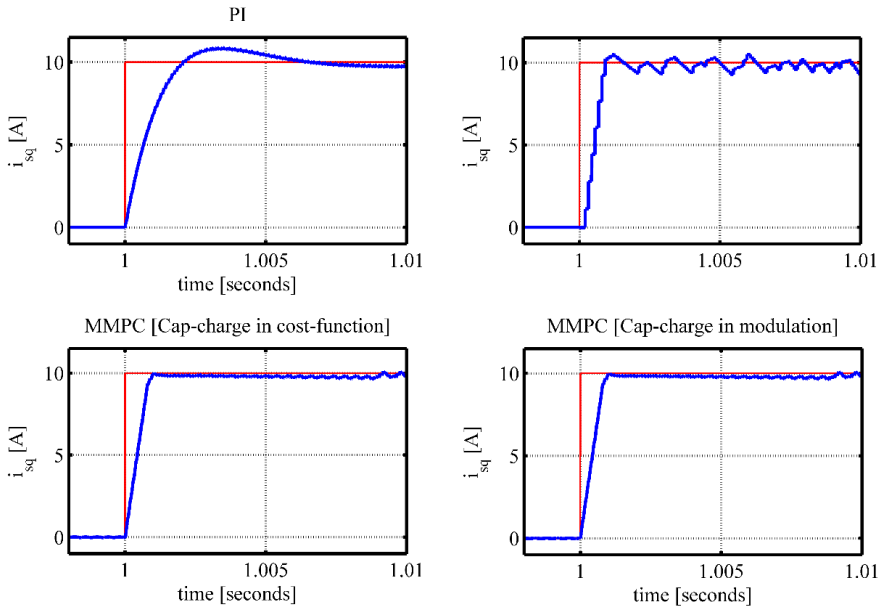


Figure 6.35 Response of control methods for a step change in the amplitude of the reference torque producing current i^*_{sq} for induction motor drive.

It is evident from the figures that the steady state operation of the capacitor voltage is the same for all control schemes, the capacitor charging is a slow system thus the faster predictive control and the control in modulation will not affect the capacitor voltage in steady state.

Finally, the response of the controllers for a step change in the reference torque is shown in Figure 6.35. The behaviour of the controller was as expected, the PI based controller has the slowest response of them all and also shows overshoot in the current waveform. It is evident from the comparison of the results that for this particular application the PI based controller has lower load current distortion than any other controllers and has an advantage in terms of losses. The predictive and modulated predictive control schemes have higher load current distortion but have a better dynamic response than the PI based controller. These controllers have advantages in fault tolerant applications where faster response time is crucial.

6.4 Conclusion

This chapter has presented a detailed analysis of predictive control algorithm for the proposed converter for a static R-L load and for IM drive application. The predictive control algorithm has variable switching frequency, thus the load current frequency spectrum is spread all over the frequency plane. To overcome this challenge a modulation scheme inside the predictive control algorithm was introduced and the calculation for a new cost function algorithm was also shown. The modulated model predictive control was then simulated and results were compared with PI based controller and conventional predictive control algorithm.

It has been shown that the PI based controller has lower load current harmonic distortion. The advantage of modulated model predictive control is its faster dynamic response. These characteristics are advantageous for some applications. It has also been shown that the incorporation of floating capacitor control either with modulation or with cost function minimization for modulated model predictive control algorithm does not affect the control dynamics thus any one of them can be used in simulation platform. The calculation time will be lower if the capacitor control is incorporated within the modulation scheme for the practical implementation.

Chapter 7

Experimental Setup and Results

This chapter presents the experimental results from a prototype of the dual inverter topology with one of the bridges is floating in order to validate the simulation results presented in Chapters 5 and 6. The converters used for the experimental setup were traditional two-level inverters. An outline of the circuit diagram of the system is shown in Figure 7.1. The main converter of the dual inverter system was supplied using a variac and a bridge rectifier. The variac was used to manually control the primary DC link voltage.

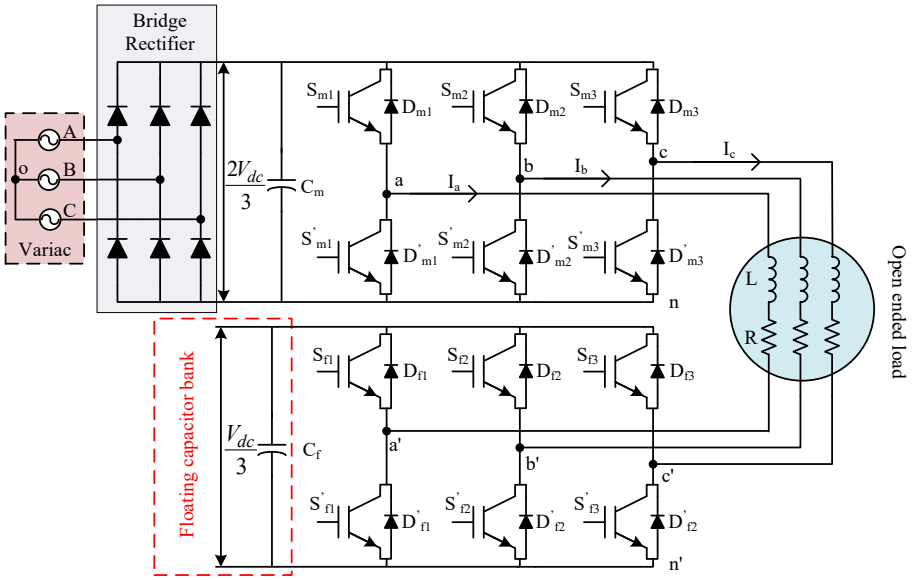


Figure 7.1 Experimental arrangements circuit diagram.

The floating inverter is connected to a capacitor bank which has a DC link controller to have a voltage of half the main inverter's DC link voltage. The load, as shown in Figure 7.1, represents either an R-L load or an induction motor as appropriate. This chapter presents the detailed specification of the experimental setup along with the experimental results to support the simulation and analysis presented in the previous chapters.

7.1 Experimental setup

The experimental system consists of power converters and their power supplies, control units, measurement circuits and the loads. The main converter was supplied from a variac and three-phase rectifier. The output DC link voltage of the rectifier was controlled manually using a variac to control the AC input voltage to the rectifier. The secondary converter was connected to a second capacitor bank. The two-level inverters used in this experimental setup were 'off the shelf converters'. The load used for these experiments was a three phase squirrel cage open stator phase induction motor and an open three phase R-L load.

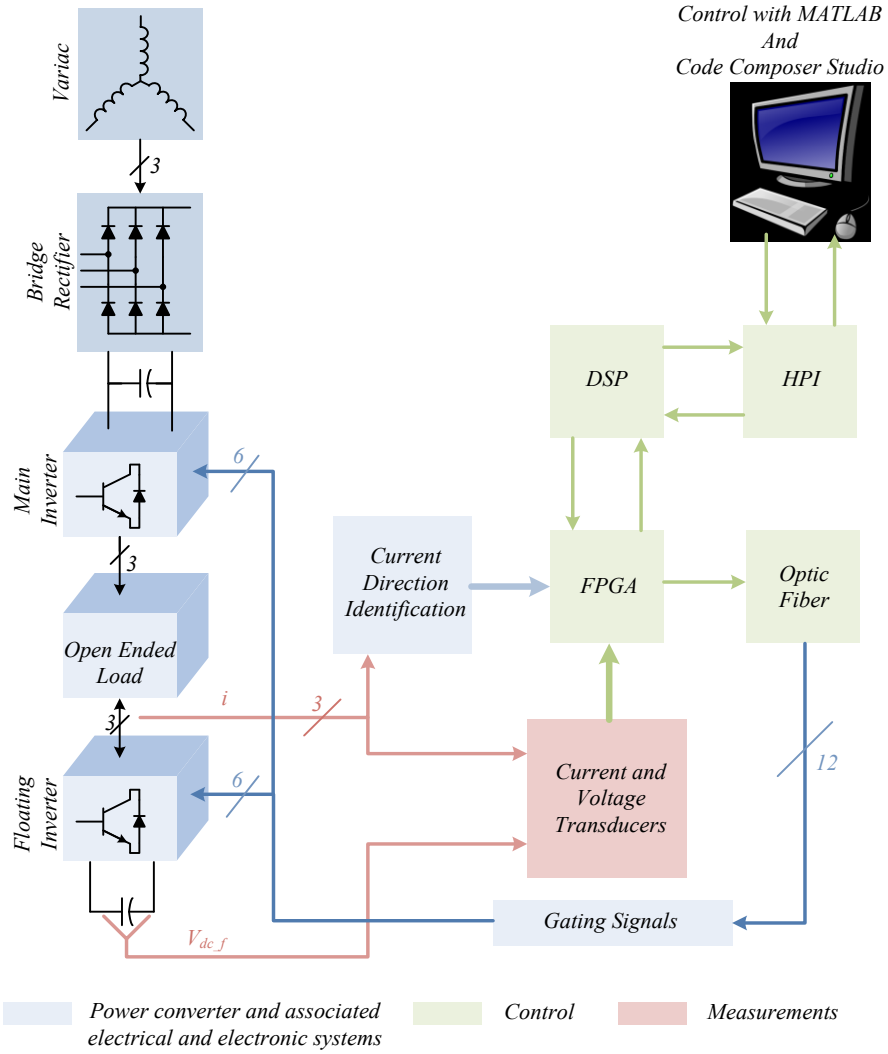


Figure 7.2 Block diagram of control implementation.

It was not difficult to find a motor which can be used as an open stator phase motor as many industrial motors are designed to have access to the both ends of the

windings so that the windings can be arranged as a star or delta. For the experimental results shown in this chapter, a 11kW Siemens motor (1LA7163-4AA60-Z-160M) was used[152], while the machine fed from both ends of the three phase windings. A block diagram of the system implementation is shown in Figure 7.2.

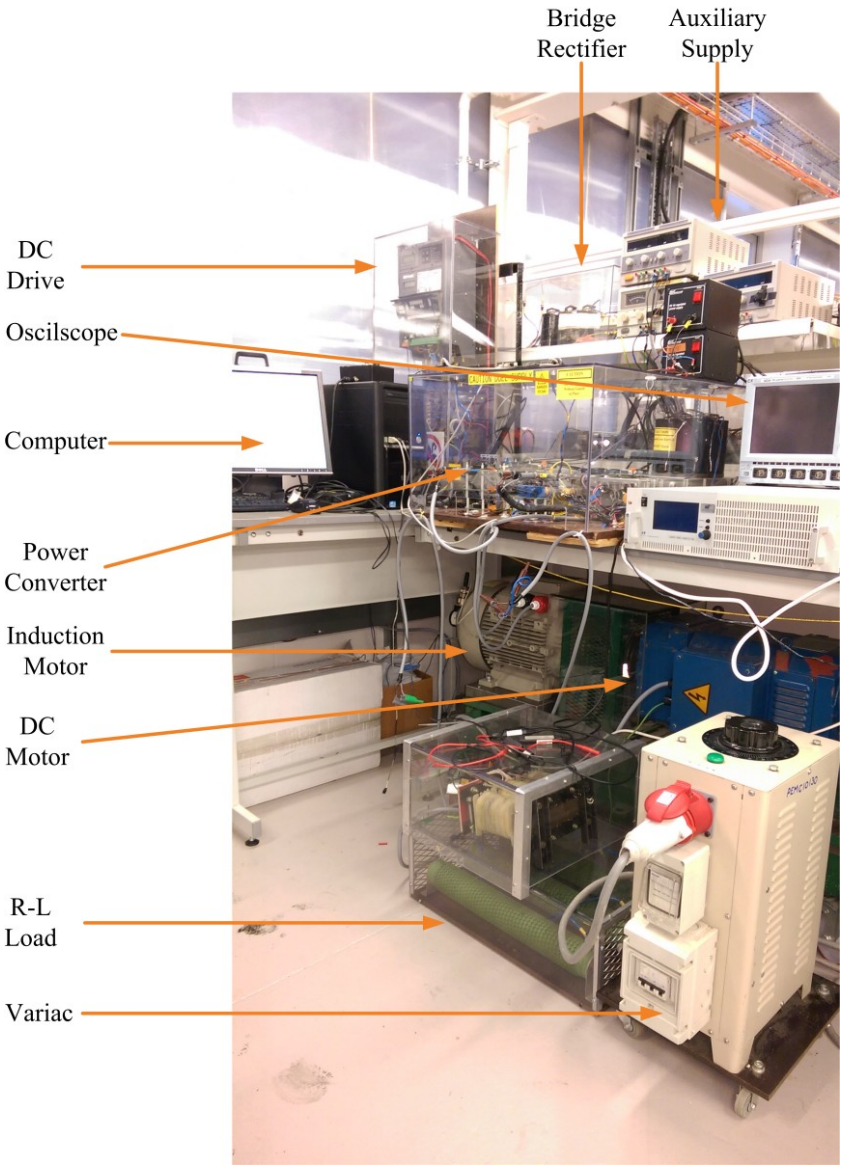


Figure 7.3 Experimental setup.

It can be seen from the Figure 7.2 that the converters are controlled using a DSP and FPGA platform. The actual voltage and currents are measured using transducers to enable the close loop control. A current direction detection circuit was also used to modify the gating pulses to avoid dead-time spikes which are inherent in the proposed topology. A picture of the experimental setup is shown in Figure 7.3.

7.1.1 Experimental converter

The converters used for this experimental setup were two 200kW two-level converters (SKAI 45 A2 GD12-W12DI) produced by SEMIKRON for automotive applications [153]. These converters have integrated gate drivers with on board dead-time, DC link capacitors, RC snubbers and input-output common mode chokes. A circuit diagram of the converter is shown in Figure 7.4. It can also be seen from the figure that the converter is integrated with Y-capacitors to suppress EMI and the mid-point of Y-capacitor has to be connected to earth.

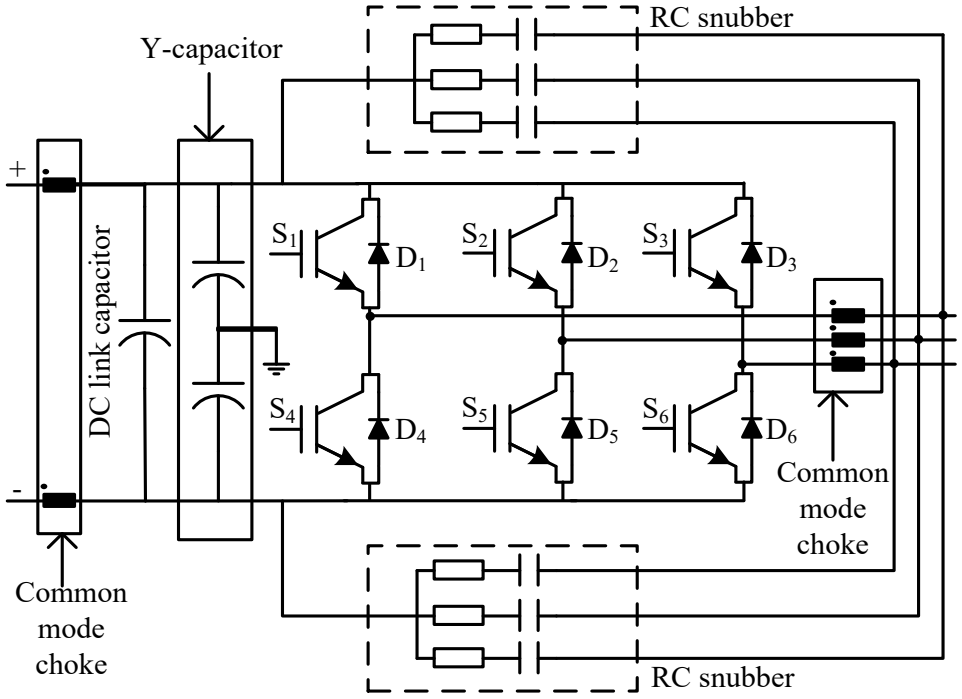


Figure 7.4 Experimental two-level converter configuration.

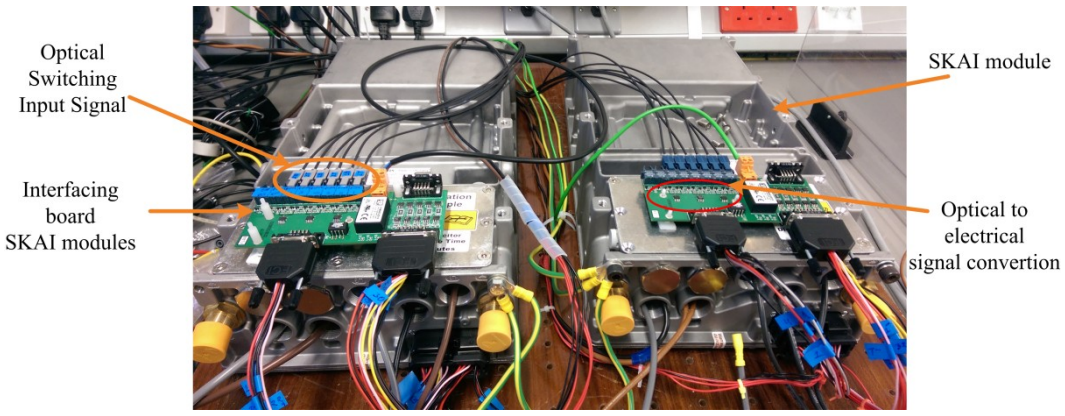


Figure 7.5 SKAI module and interfacing board.

The floating converter was not earthed as the earth will provide the path for common mode current flow in this topology. These industrial converters require 12Volt supply to operate gate drivers and other protection circuits integrated with this system. An interfacing board was also designed to convert optical signals from FPGA to the 12Volt electrical signals which are required by the converter system. A picture of the interfacing board and the converters is shown in Figure 7.5.

7.1.2 Voltage and current measurements

The current and voltage measurements are taken using transducers and used for the converter control. The voltage transducers are Hall-effect transducers which can measure up to 500Volts; the model of the transducer used for this work was the LEM LV25-P [154]. The load current measurements were also measured using Hall-effect current transducers, the LEM LA55-P, which can measure up to 50Amps with a bandwidth of 200kHz [155]. The output of both the current and voltage transducers are current values and scaling factors are provided in the datasheet. A burden resistor is used to convert the current signals into voltage signals for analogue to digital conversion, components which are integrated with Field Programmable Gate Array (FPGA) board.

7.1.3 Control boards

To implement the control of the proposed converter topology a Digital Signal Processor (DSP) and FPGA platform is used. The DSP board used for this converter is the Texas Instruments TMS3206713DSK. The signal processor has a clock of 225MHz and a 32 bit external memory interface [156]. An expansion board was also used to interface the DSP with a computer, the TMS3206713 DSK HPI DAUGHTERCARD [156]. An FPGA board was used to generate gating pulses for the power semiconductor switches. The FPGA board is an Actel ProASIC3 A3P400 and the board is integrated with ten analogue to digital channels [157]. The clock frequency of the FPGA board is 50MHz. The FPGA and DSP interface are controlled together, an interrupt is defined in DSP and FPGA at the same rate as the sampling frequency. At every interrupt the FPGA reads the data from the A-to-D channels and the DSP board reads the values and converts them to the exact values. These values are then used by the control algorithm.

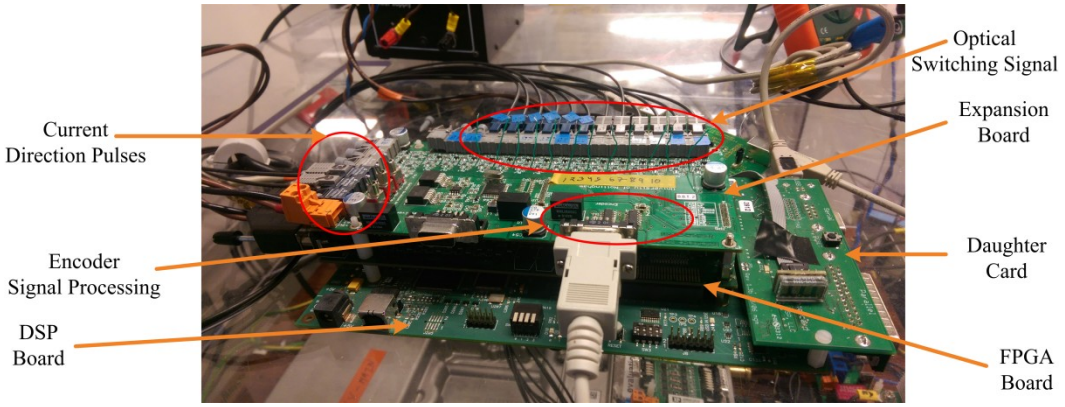


Figure 7.6 Control platforms.

A picture of the DSP and FPGA control platform is shown in Figure 7.6. An extension board was used to provide the twelve optical output signals for gate pulses, three optical inputs to have three phase current directions, as well as the isolation and signal processing for the encoder pulses, were integrated with the extension board.

7.1.4 Current direction identification

Identification of the direction of phase current was necessary for the proposed topology to eliminate phase voltage spike during the dead-time interval. In this thesis, the current direction was defined as positive when the current was flowing from the main converter to the floating converter. A circuit was designed with anti parallel schottky diodes, VS-30CTQ045PBF, in series with the converters phase connections. The schottky diodes are used due to their lower turn on voltage and fast recovery time due to the lower stored charge in the device.

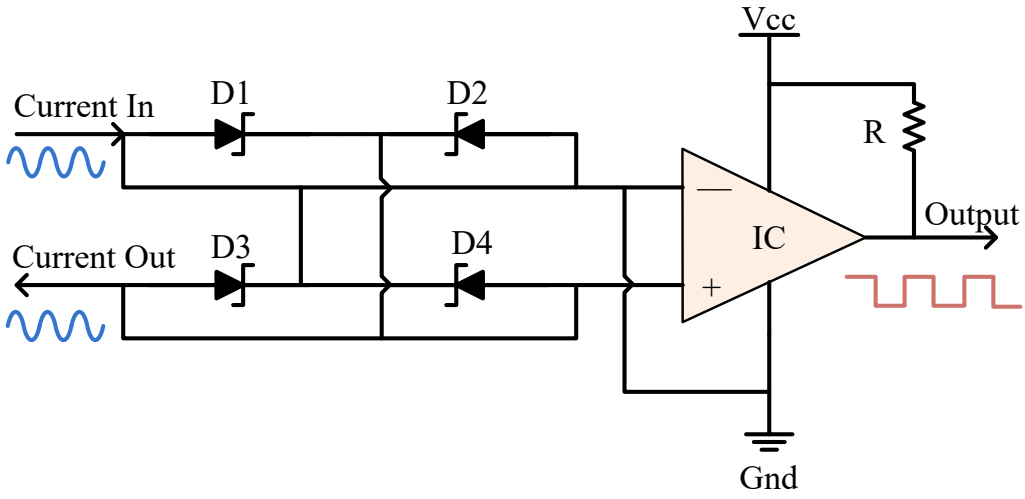


Figure 7.7 Circuit diagram of current direction identification circuit.

The circuit diagram for the current direction detection circuit is shown in Figure 7.7, the voltage drop across the schottky diodes are then compared with zero using an analogue comparator, an LM311DR. The output of the comparator is a digital signal which provides either 0 or 5Volts for negative and positive current direction respectively.

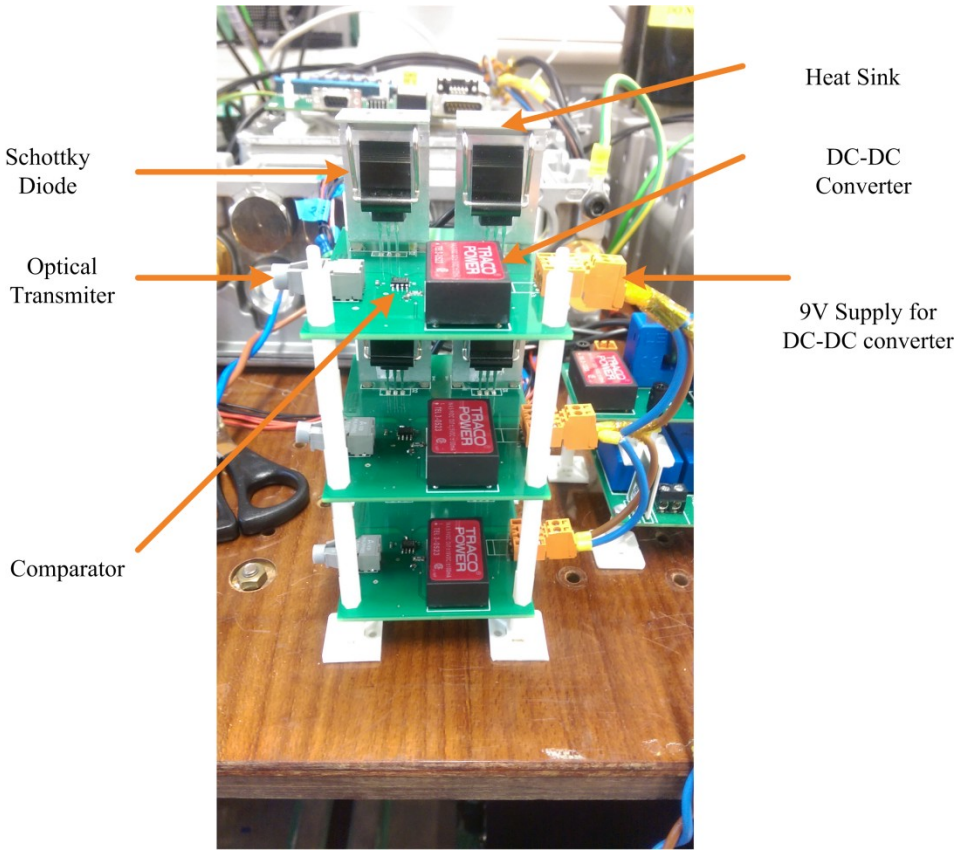


Figure 7.8 Current direction detection circuits.

A picture of the current direction detection circuit is shown in Figure 7.8. It can be seen that the output pulses are transmitted through optical transmitters and received by the FPGA board directly, where the gating pulses for the phase legs are altered depending on the direction of the currents as described in Chapter 5.

7.1.5 Rotor speed measurement

The measurement of the rotor speed was necessary to implement speed control in the induction motor drive. The rotor speed was measured using an encoder; the encoder was connected to the shaft of the motor and will rotate synchronously with

the rotor speed. The encoder used in this work is manufactured by British Encoders, a 725 flange mount series [158]. The encoder outputs six pulses which are then read by the FPGA and decoded before being sent to the DSP at each interrupt.

7.1.6 Industrial DC drive

A DC motor was connected to the induction motor shaft to act as a load. The DC motor is operated in torque control mode using an industrial DC drive to control the DC motor, manufactured by Eurotherm Drives (590C/ 0350/6/4/0/1/0/00/000) [159].

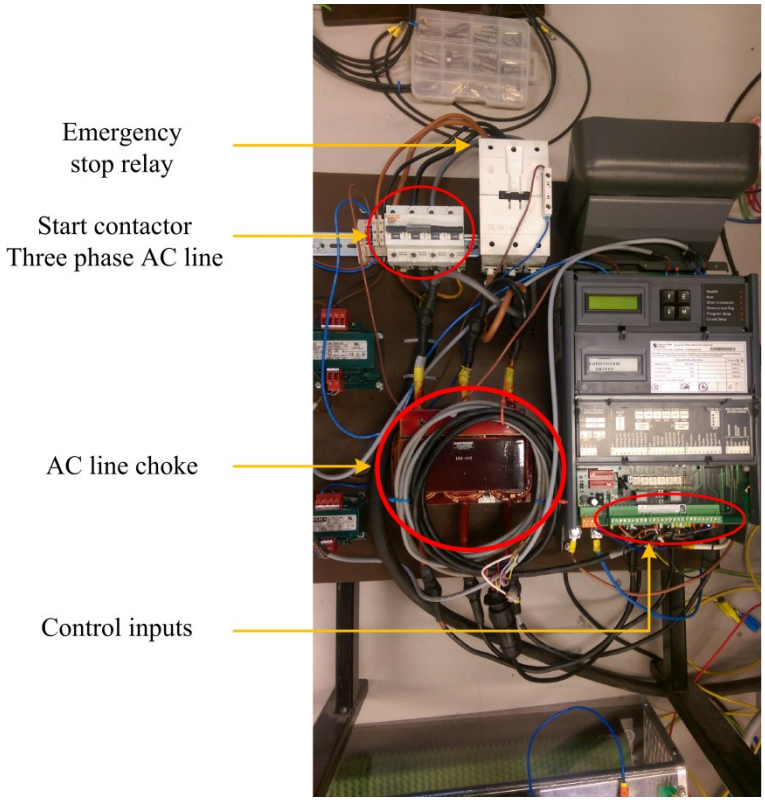


Figure 7.9 Industrial DC drive.

The drive was configured to achieve four quadrant control of the DC motor. A photo of the DC drive is shown in Figure 7.9.

7.2 Experimental results using a PI based controller

A PI based controller along with a Space Vector Modulation (SVM) scheme was used for the experimental results shown in this section. A capacitor was connected to the floating converter and the voltage of the capacitor was controlled using

redundant switching states, as described in Chapter 5. The floating capacitor voltage control was integrated with the SVM scheme as a bang-bang controller to avoid using an additional PI based controller. The converter and control scheme was first validated with a static R-L load and a 200Volts main DC link voltage. The floating capacitor voltage was initially charged to half of the main DC link voltage. The controller used for this experiment was the PI based load current controller to control the load currents.

The references were set in the *d-q* reference frame and the actual three phase load currents were transferred to rotational *d-q* coordinates using current vector angle. The sampling frequency was set to 5kHz and delay time to avoid dead-time spike was set to 4μs. Results are shown in Figure7.10 for a current reference of 4Amps to show the results for the two-level mode of operation of the proposed converter. It can be seen from the figure that load current is following the reference currents closely and the average floating capacitor voltage is controlled.

To demonstrate the multilevel operation of the converter a demand reference of 9Amps was set, the results are shown in Figure 7.11. It can be seen from the figure that the voltage across the load has nine distinct DC voltage levels (similar to a three-level converter) and the capacitor voltage is controlled at 100Volts. The ripple in the capacitor voltage is around 1Volts peak to peak.

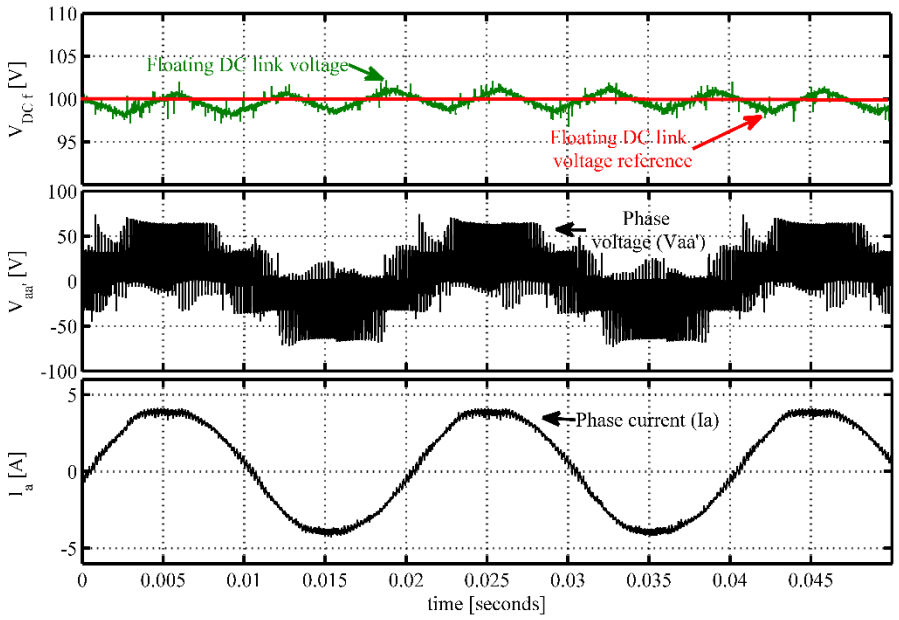


Figure 7.10 Response of the controller when 4Amps current was set to the controller, from top to bottom: Floating DC link voltage, phase voltage ($V_{aa'}$) and load current (I_a).

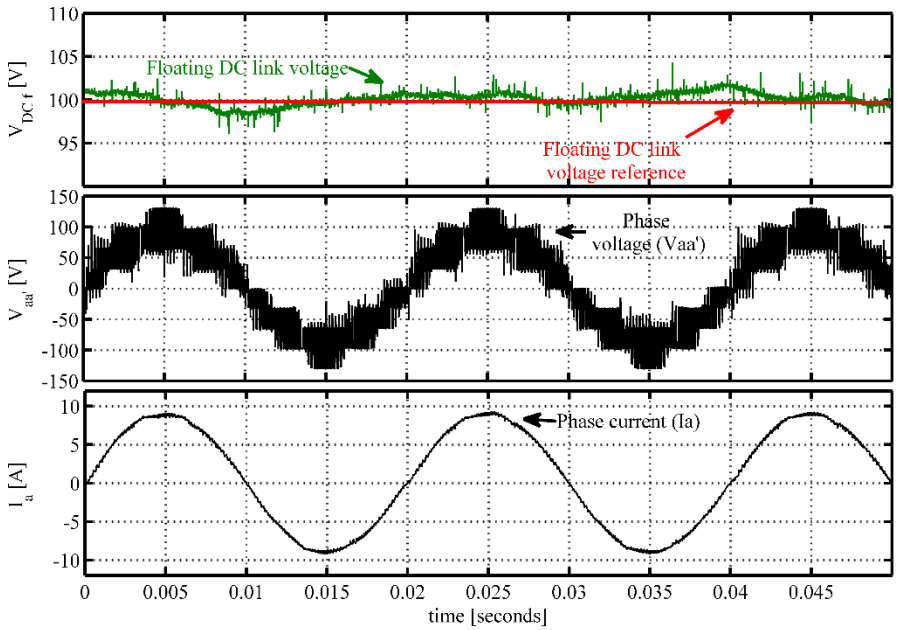


Figure 7.11 Response of the controller when 9Amps current was set from the system, from top to bottom: Floating DC link voltage, phase voltage ($V_{aa'}$) and load current (I_a).

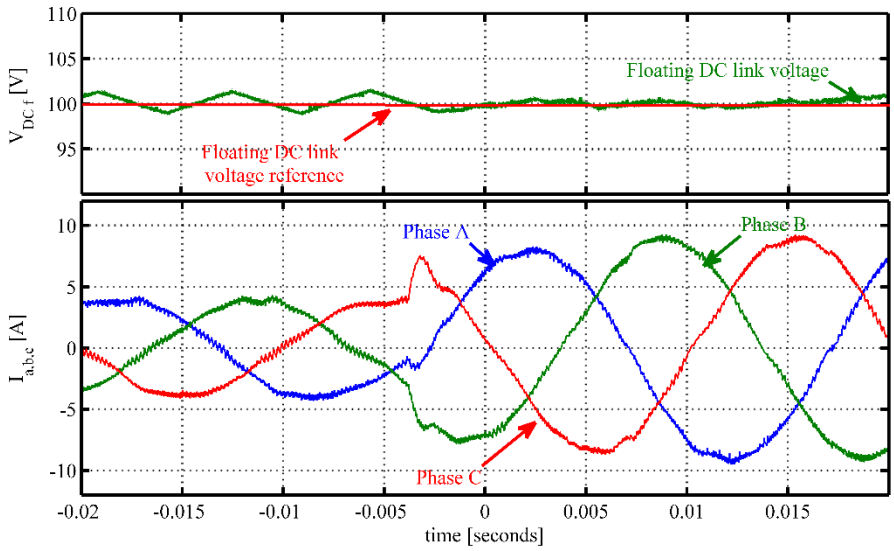


Figure 7.12 Response of the controller when a step change in the load current was set from 4Amps to 9Amps, from top to bottom: Floating DC link voltage and three phase currents.

To show the dynamic behaviour of the proposed converter a step change in the reference current was applied to the controller. The results are shown in Figure 7.12. It can be seen that the load currents change quickly to match the reference values and it has minimal effect on the floating capacitor voltage. The fluctuation of the DC link voltage is due to the switching sequence selection, as in two-level mode of operation the converter can only select the full charging sequences and can overcharge the

capacitor. In three-level mode of operation, the control can select between full and half charging sequences, shown in Chapter 5. The frequency spectrum of the phase current is shown in Figure 7.13. It can be seen that the harmonics are clustering around the sampling (switching) frequency as expected from space vector modulation scheme. The proposed system was operated with an Open End Winding Induction Motor (OEWIM) with an open loop *v/f* control algorithm.

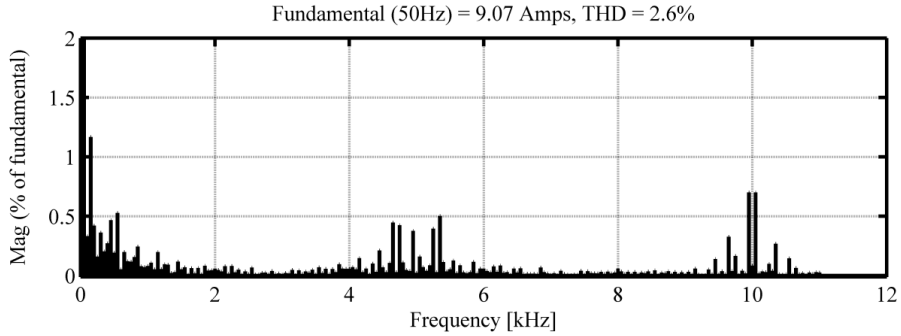


Figure 7.13 Frequency spectrum of phase current when the converter was operating at multilevel mode.

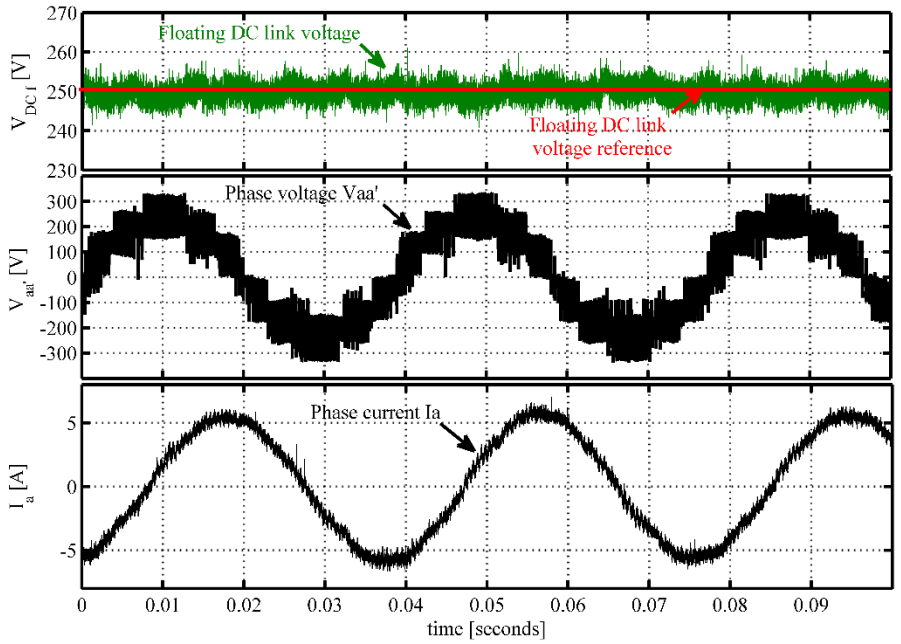


Figure 7.14 Steady-state response of the controller when frequency reference was set to 25Hz for v/f induction motor drive from top to bottom: floating DC link voltage, phase voltage ($V_{aa'}$) and load current (I_a).

To test the converter as an open loop *v/f* motor drive the main inverters DC voltage was set to 500Volts. The sampling frequency was set to 5kHz and the delay time was set to 4µs to avoid dead-time spikes. The floating converter reference voltage was set

to half of the main inverters DC link voltage. To demonstrate the steady state operation a demand reference frequency of 25Hz was set. The reason for choosing this frequency was to maintain the *v/f* ratio for the machine as the selected machine has rated voltage of 690Volts. The results from the open loop *v/f* controlled motor drive are shown in Figures 7.14 and 7.15. Figure 7.14 shows the no load voltage, current and floating DC link voltage. It can be seen that the drive charges the floating capacitor to required value and the converter achieves a multilevel output voltage waveform

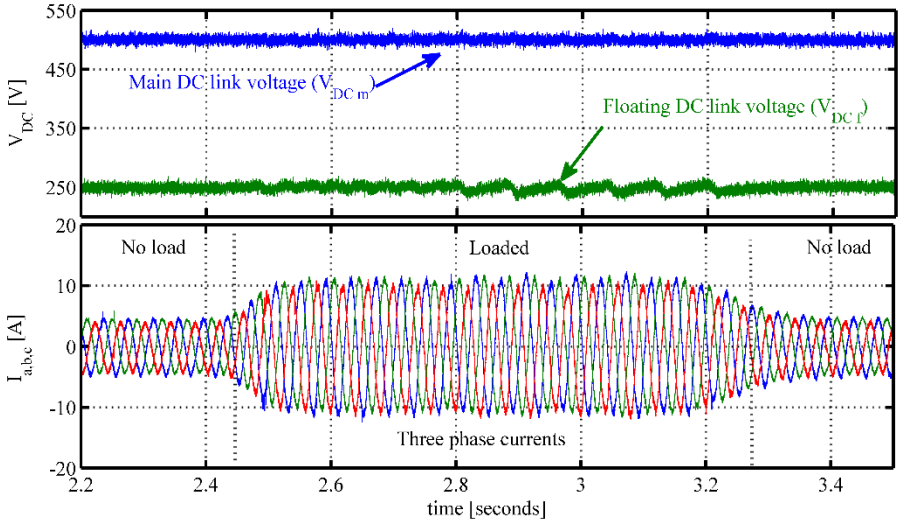


Figure 7.15 Response of the controller when a load was applied to the motor drive operating as open loop v/f drive: floating DC link voltage and three phase currents.

To validate the open-loop performance of an IM drive a step load was applied to the machine after speed reaches steady-state, as shown in Figure 7.15. It is evident from the figure that the capacitor voltage is controlled during a sudden change in load, the effect on the capacitor voltage is minimal.

The results shown in Figure 7.14 were achieved using the modified switching pulses to avoid unwanted voltage level during the dead-time interval. A magnification of the leg voltages and the phase voltage of the converters are shown in Figure 7.16 with no modification to the gating pulses. It can be seen that the phase voltage is clamped to an unwanted voltage state for the duration of the dead-time interval. The leg voltage and phase voltage are shown in Figure 7.17 after the introduction of the modified switching pulses, showing that the leg voltages are changing state at the same time and spike duration is short.

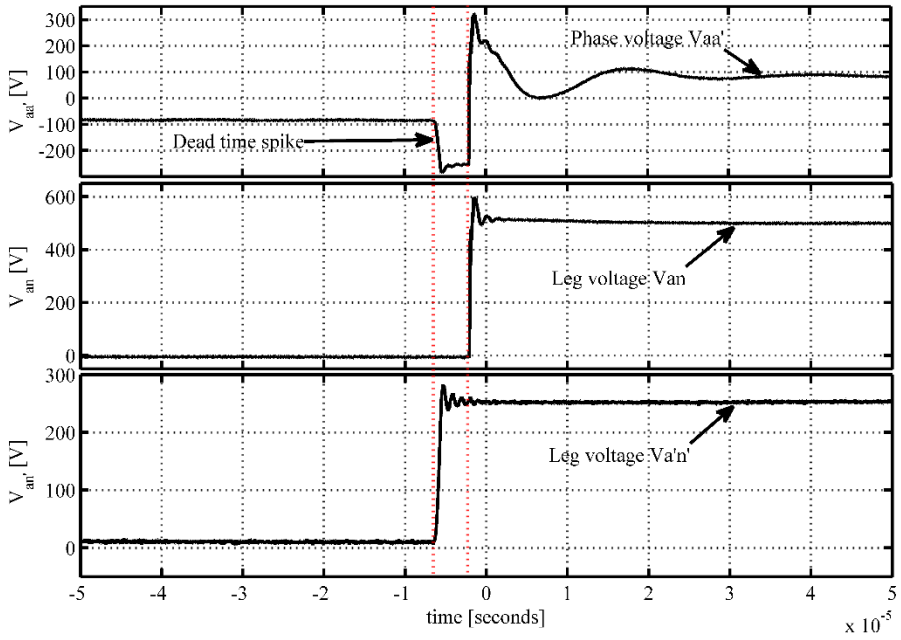


Figure 7.16 Dead-time effect on phase voltage waveform before the pulses were altered, from top to bottom: phase voltage ($V_{aa'}$), leg voltage of the main inverter (V_{an}) and leg voltage of the floating inverter ($V_{a'n'}$).

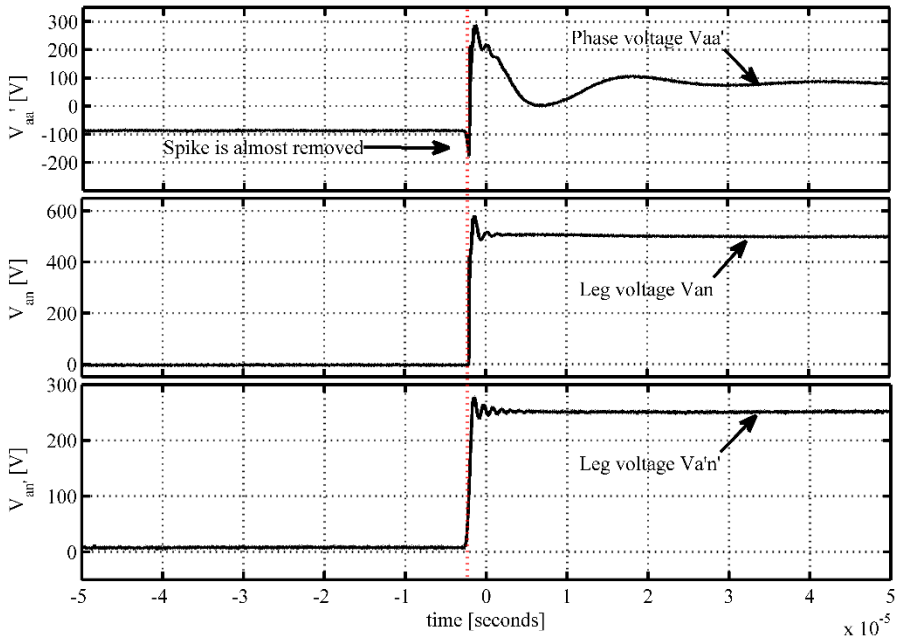


Figure 7.17 Dead-time effect on phase voltage waveform after the pulses were altered, from top to bottom: phase voltage ($V_{aa'}$), leg voltage of the main inverter (V_{an}) and leg voltage of the floating inverter ($V_{a'n'}$).

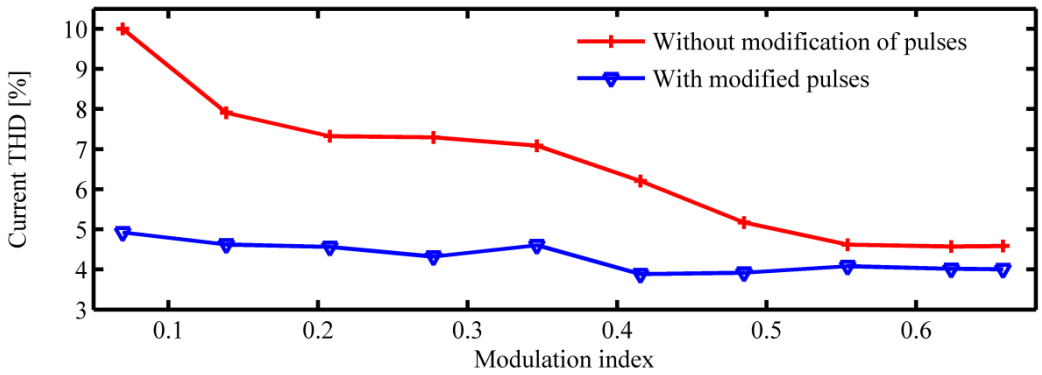


Figure 7.18 Harmonic distortion of load current when the IM was used as a load.

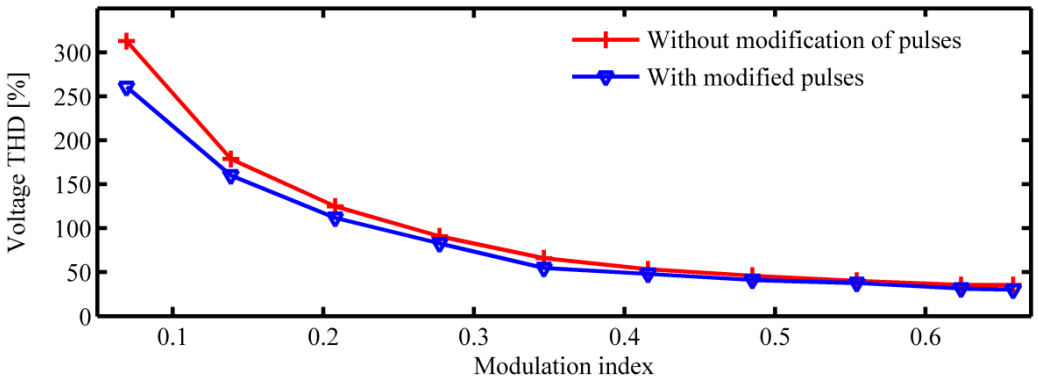


Figure 7.19 Harmonic distortion of phase voltage when the IM was used as a load.

To ensure that the modification of the pulses was necessary for this topology the THD of load current and voltage were analysed before and after the modified pulses were applied to the converters. The results are shown in Figures 7.18 and 7.19, the current and voltage THD reduced after the modified pulses were implemented. The difference between modified and non-modified THD curves decreases with the increase of modulation index.

It can be seen from Figures 7.16 and 7.17 that the phase voltages show oscillations after a change in voltage level and the frequency of the oscillation is near 35 kHz. This oscillation is due to the formation of LC resonant circuit in between the load inductance and the capacitance between the two converters, as shown in Figure 7.20. The parasitic capacitance shown in Figure 7.20 will provide a path for common mode current to flow thus a high frequency oscillation can be seen in the voltage waveform. To prove the described concept the capacitance value is calculated using the experimental waveform as shown in equation 7.1 and then a simulation model is created with a coupled capacitor in between the negatives of the DC rails.

$$f_r = \frac{1}{2\pi\sqrt{(L_{ls}/3)C}}\ [Hz]$$

$$35000 = \frac{1}{2\pi\sqrt{(0.0115/3)C}}\ [Hz] \tag{7.1}$$

$$C = 5.39e-9\ [F]$$

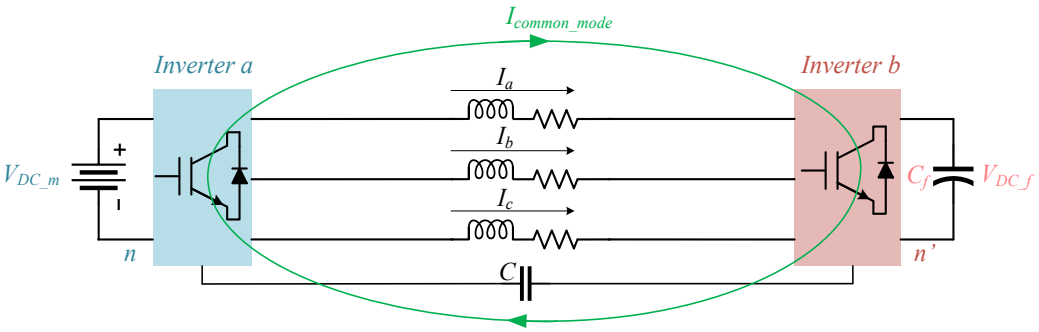


Figure 7.20 Common mode current flow of the converter system.

Using this capacitance value along with 500Ω damping resistor a simulation model is created and the results were acquired using the same parameters used to achieve experimental results. The simulation result can be seen in Figure 7.21. It can be seen from the figure that the phase voltage oscillated around 35kHz.

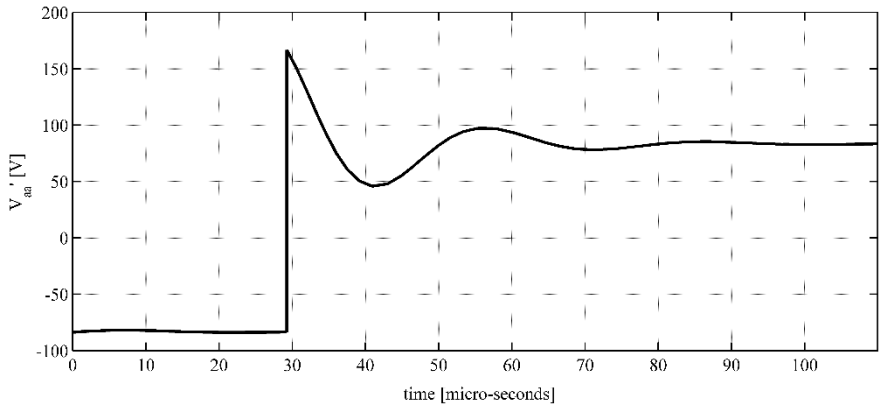


Figure 7.21 Phase voltage of IM drive using a parasitic capacitive coupling in between the negative rail of the DC bus.

To demonstrate the performance of the proposed converter with close loop control of IM drive, the main inverter was supplied with a 500Volt DC source. The aim of the floating capacitor voltage control was to charge the floating bridge capacitor to half of the main inverters DC link voltage. An indirect rotor flux orientation based control

was implemented to decouple the flux and torque producing current of the induction machine. A simplified block diagram of the field oriented control system is shown in Figure 7.22. The block 'condition' is a protection algorithm to monitor the floating capacitor voltage. The algorithm compares the reference and actual floating capacitor voltage at the period of initial charging transient. The controller will shut down the system if capacitor voltage is +/-15% of the reference voltage.

A flow chart for this algorithm is shown in Figure 7.23. Initial charging transient of the capacitor is shown in Figure 7.24. To charge the capacitor initially, the machine was first magnetised. The amplitude of the magnetising current reference i^*_{sd} was set to 6Amps. After the magnetisation process was completed, a step reference voltage was applied to show the charging dynamics of floating capacitor. It can be seen from Figure 7.24 that capacitor voltage tracks the reference value closely and reaches steady state within 1.5 seconds. The charging transient of the capacitor can be made faster with increased *d*-axis current. It can also be seen from the figure that the main DC link voltage fluctuates after the floating capacitor voltage reaches the steady state value, this was due to the charging and discharging of floating capacitor. In this period the rotor was at stand still and the machine was only drawing reactive power to maintain constant flux.

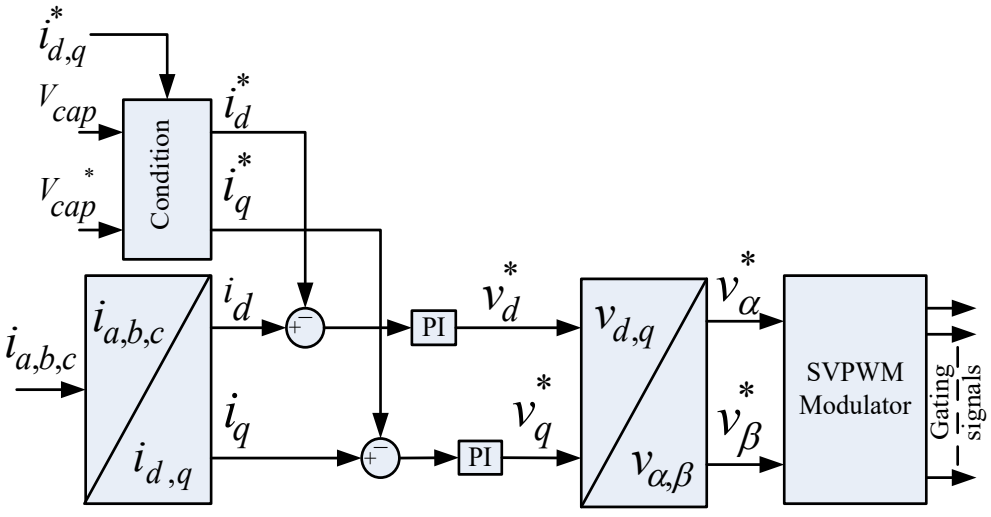


Figure 7.22 Simplified block diagram of IRFO based IM drive for practical implementation.

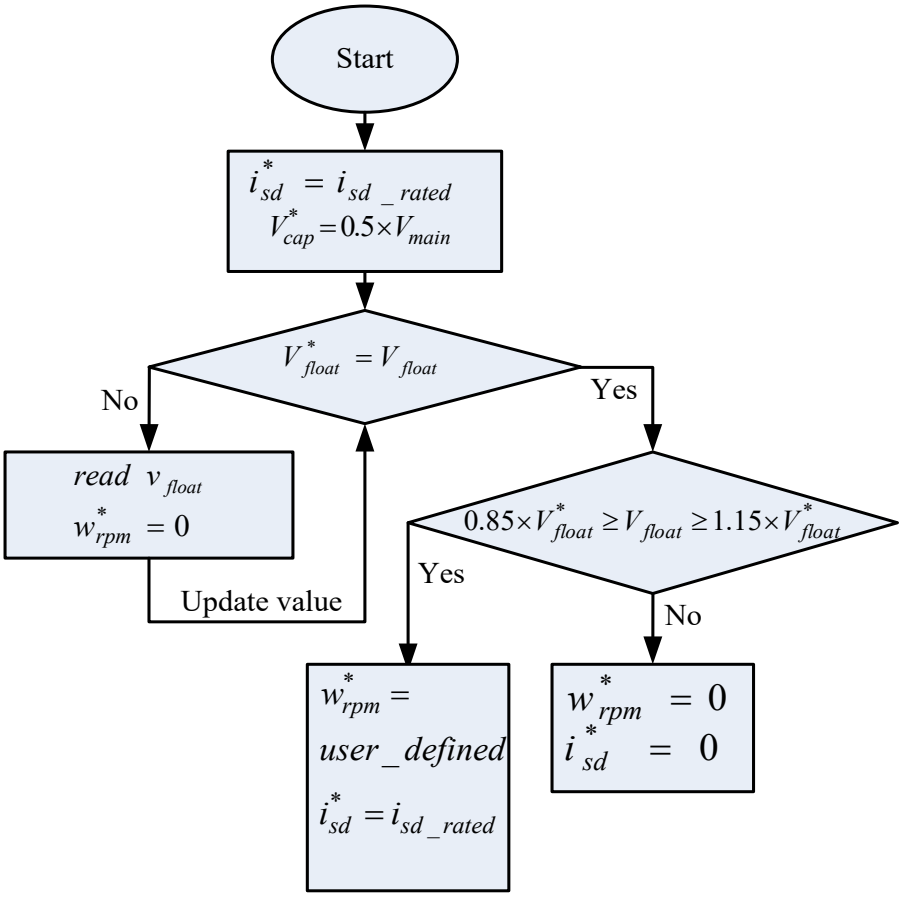


Figure 7.23 Floating capacitor charging and protection algorithm.

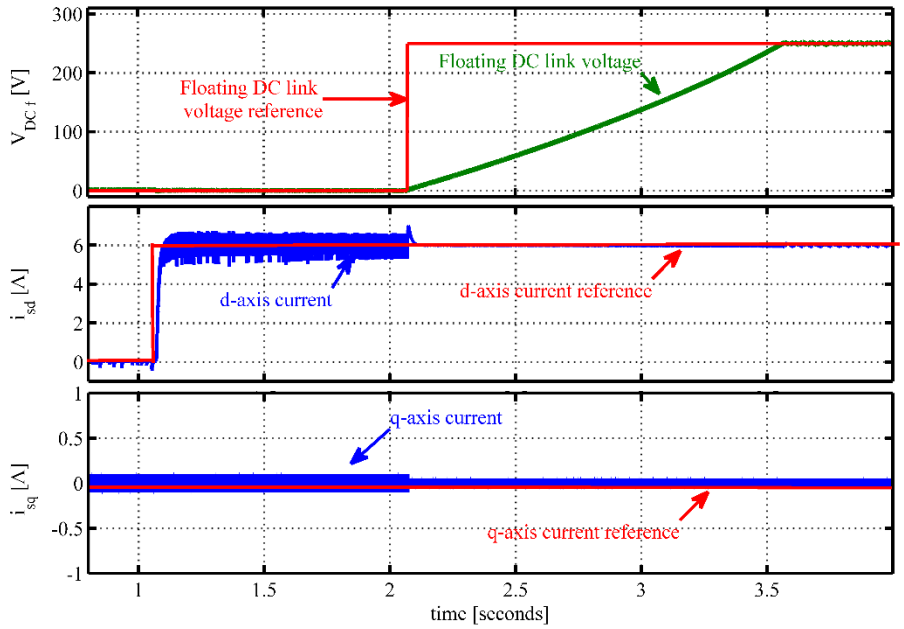


Figure 7.24 Charging transient of the floating capacitor voltage when the machine was magnetised and the rotor was at stand-still, from top to bottom: floating DC link voltage and reference, main inverters DC link voltage, stator d-axis current and stator d-axis current reference.

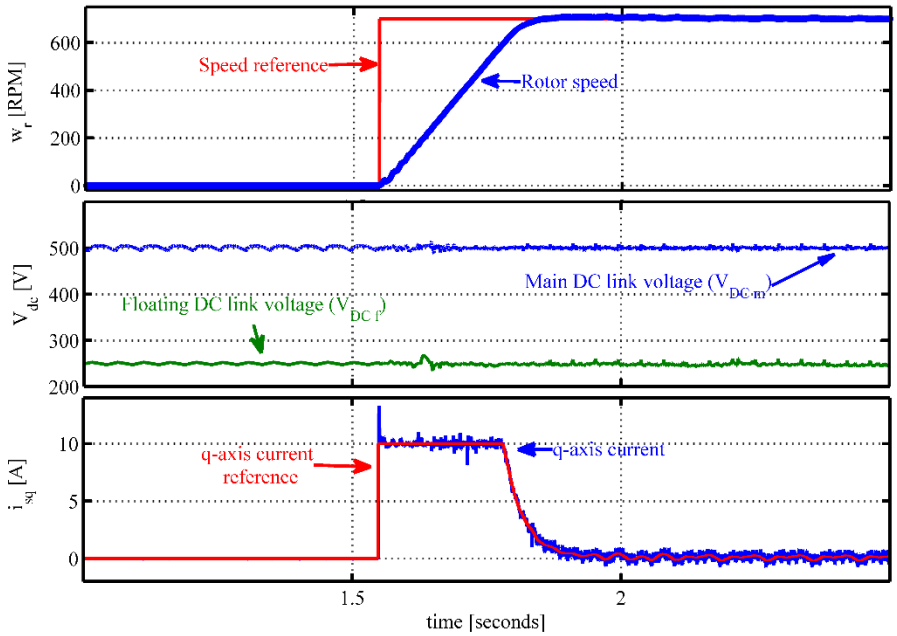


Figure 7.25 Response of the controller when a speed reference of 700rpm was set to the controller, from top to bottom: rotor speed and reference speed, main and floating inverters DC link voltage, stator q-axis current and stator q-axis current reference.

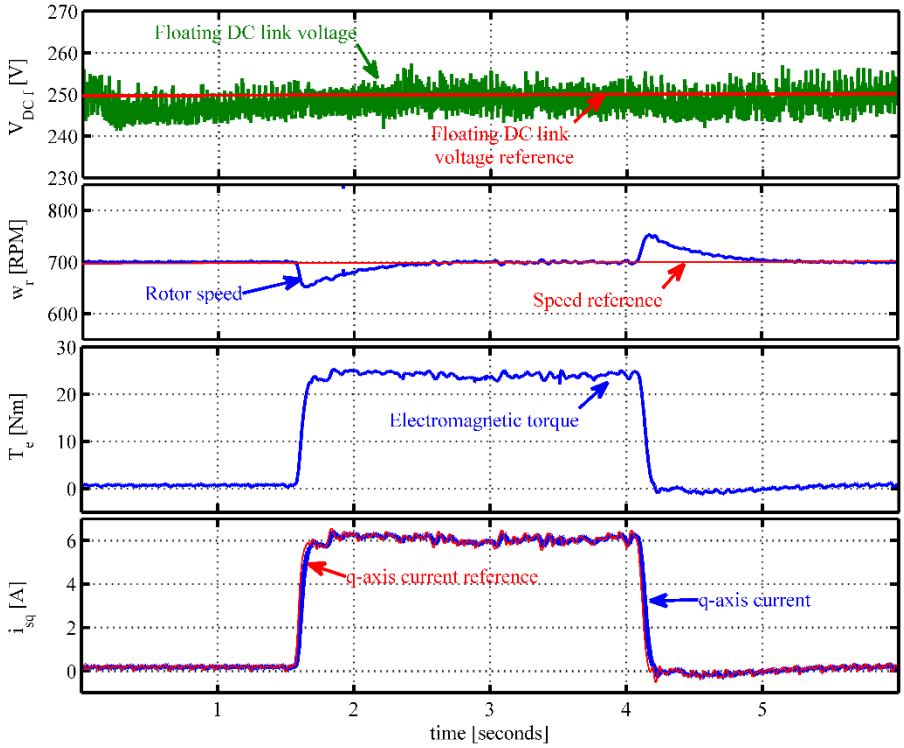


Figure 7.26 Response of the controller when a step load of 25Nm was demanded from the system after speed reaches steady-state, from top to bottom: floating inverters DC link voltage, rotor speed and reference speed, stator q-axis current and stator q-axis current reference.

A step speed reference of 700RPM was applied to the controller after the capacitor voltage reaches steady state. The response of the controller is shown in Figure 7.25. The q-axis current steps up immediately to provide maximum torque to overcome the inertia and holds its value until speed reaches steady state. A step demand reference load of 25Nm was applied to the controller after rotor speed reaches steady-state. The reference torque current i_{sq}^{*} which is generated from the speed loop steps up immediately to counter the load torque, as shown in Figure 7.26. It can be seen from Figures 7.15 and 7.26 that at no time does the capacitor voltage overcharge or collapse. The capacitor voltage ripple increases at no load as there was a small amount of real power flowing through the system, charging improves with loading.

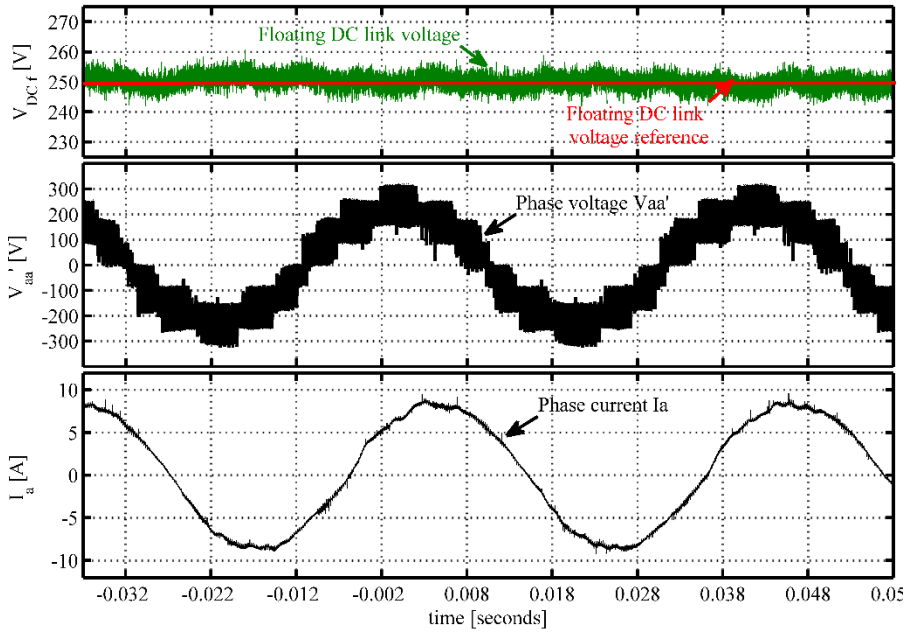


Figure 7.27 Floating DC link voltage, phase voltage ($V_{aa'}$) and phase current (I_a) when the machine was loaded.

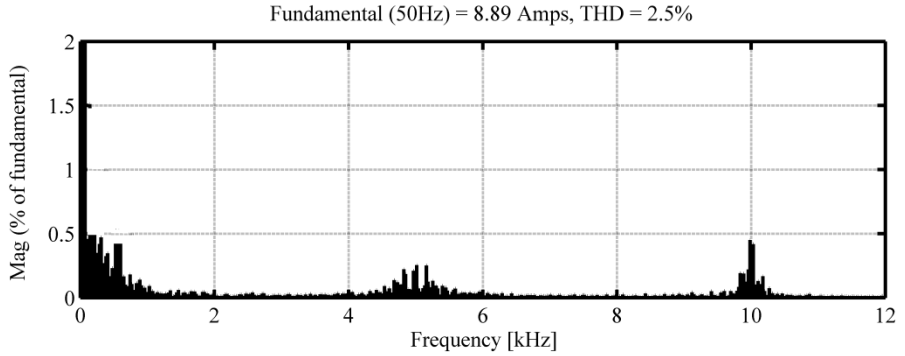


Figure 7.28 Frequency spectrum of the phase current when the machine was loaded.

Finally the phase voltage, current and floating dc link voltage are shown in Figure 7.27 for operation when the machine was loaded. It can be seen from that the phase voltage creates multilevel output waveforms. The phase current spectrum is shown in Figure 7.28 for the operation when the machine is loaded. It can be seen that the harmonics are clustering around the sampling frequency, which is expected from the SVM algorithm.

7.3 Experimental results using Predictive control

A model predictive control algorithm was used to validate the proposed converter topology. The predictive control algorithm was considered due to its fast dynamic response and its ability to control load currents and floating capacitor voltage in a single control loop. The results for this control are divided into two sets, one for a static R-L load and the other for an IM drive.

To obtain the results with R-L load the main DC link was set to 200Volts DC. The controller was designed to achieve control over load currents in the α-β reference frame. The reference α-β currents are generated using sine and cosine functions defined using the control platform. The reference floating DC link voltage was set using a constant value of 100Volts. The sampling frequency was set to 12.5kHz and delay time to avoid dead-time spike was set to 4µs. To show the performance of the proposed converter in the two-level mode of operation a 4Amps with 50Hz reference current was set and the results are shown in Figure 7.29.

A reference of 9Amps was set to observe the multilevel operation; the associated results are shown in Figure 7.30. The current follows the reference value closely and converter achieves nine distinct DC voltage levels across the load, similar to a three level converter. To show the dynamic performance of the controller a step change in the reference from 4Amps to 9Amps was applied, as shown in Figure7.31. It can be seen that the current changes quickly to match the reference and sudden change in demand current do not affect the control over floating capacitor voltage. The floating DC link voltage ripples increase when the control demanded 9Amps current. The reason for the increased oscillation is due to the operation of the converter at its highest modulation index. A frequency spectrum for the phase current is shown in Figure 7.32. It can be seen that the current has a wide range of harmonics, inherent with predictive control algorithms due to their variable switching nature [160].

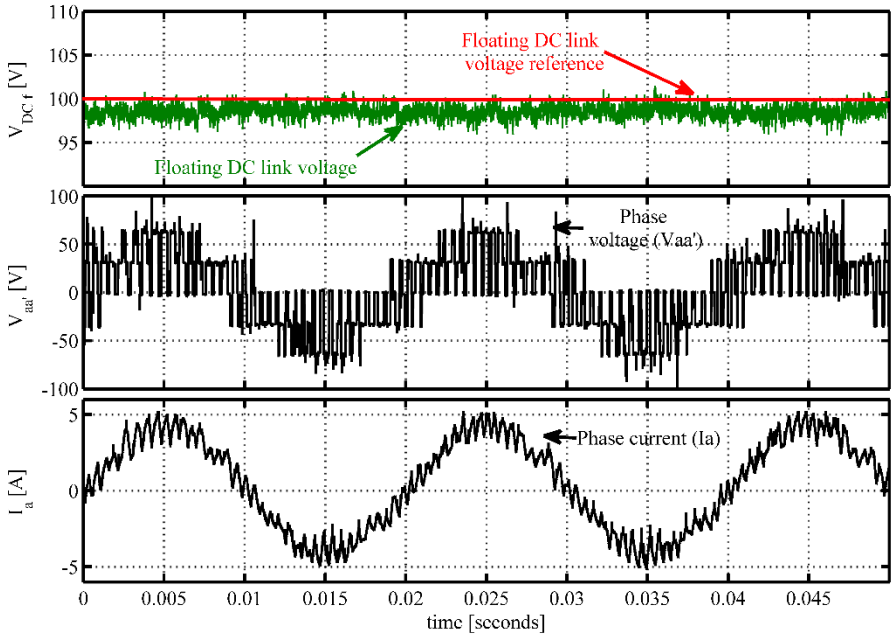


Figure 7.29 Response of predictive controller when 4Amps current was demanded from the system, from top to bottom: Floating DC link voltage, phase voltage ($V_{aa'}$) and load current (I_a).

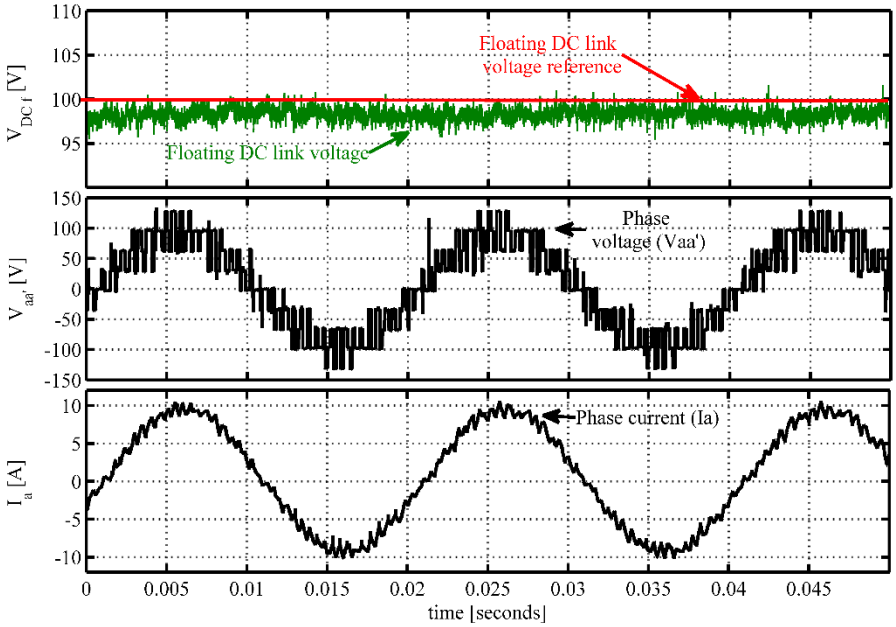


Figure 7.30 Response of predictive controller when 9Amps current was demanded from the system, from top to bottom: Floating DC link voltage, phase voltage ($V_{aa'}$) and load current (I_a).

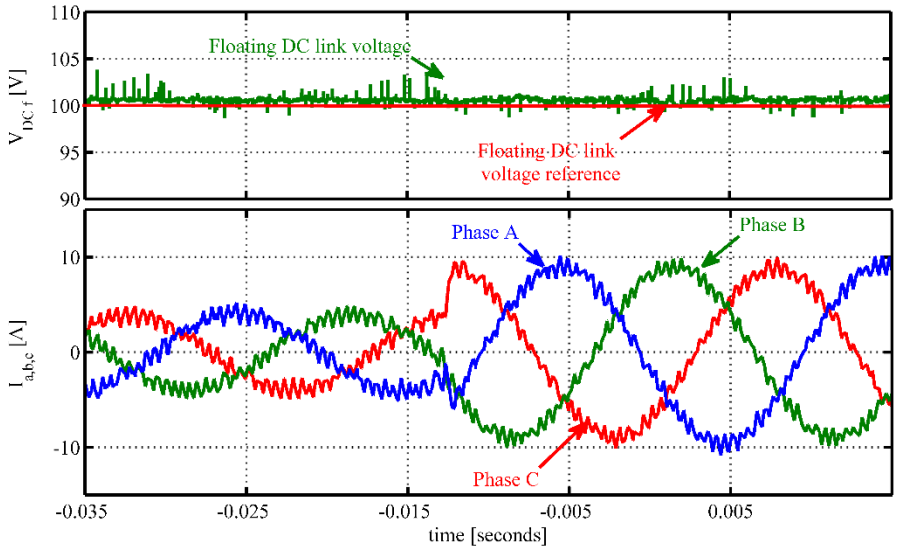


Figure 7.31 Response of predictive controller when step change in current was demanded from the system, from top to bottom: Floating DC link voltage and three phase currents.

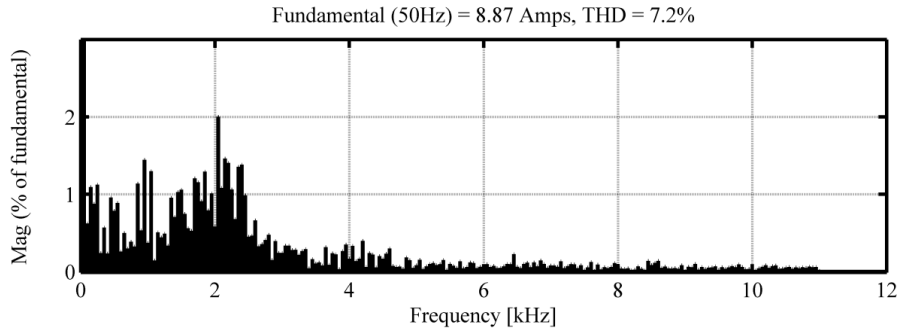


Figure 7.32 Frequency spectrum of the phase current for multilevel operation of the converter.

Finally, an induction motor was used to demonstrate the performance of the converter. The main inverter was supplied with a 500Volts DC link voltage. The floating converter voltage reference was kept constant at 250Volts. The controller used for this experiment was a hybrid controller, the PI and predictive control algorithm shown in chapter 6. To have control over the floating capacitor a reference magnetising current i^*_{sd} of 6Amps was set so that the controller can charge or discharge the capacitor by controlling the DC link current direction. After the machine was magnetised a step reference floating DC link voltage command from 0 to 250Volts was set. The results are shown in Figure 7.33. It can be seen that the capacitor charges quickly and can be controlled.

After the floating capacitor voltage reaches steady-state, a reference speed of 700rpm was set to the controller. The results are shown in Figure 7.34. It can be seen

from the figure that the torque producing current (i_{sq}) steps up immediately to overcome the machine inertia. The capacitor voltage fluctuation increase when the rotor speed reaches steady-state. This is because the machine was drawing reactive power and it was difficult to rapidly charge or discharge the capacitor.

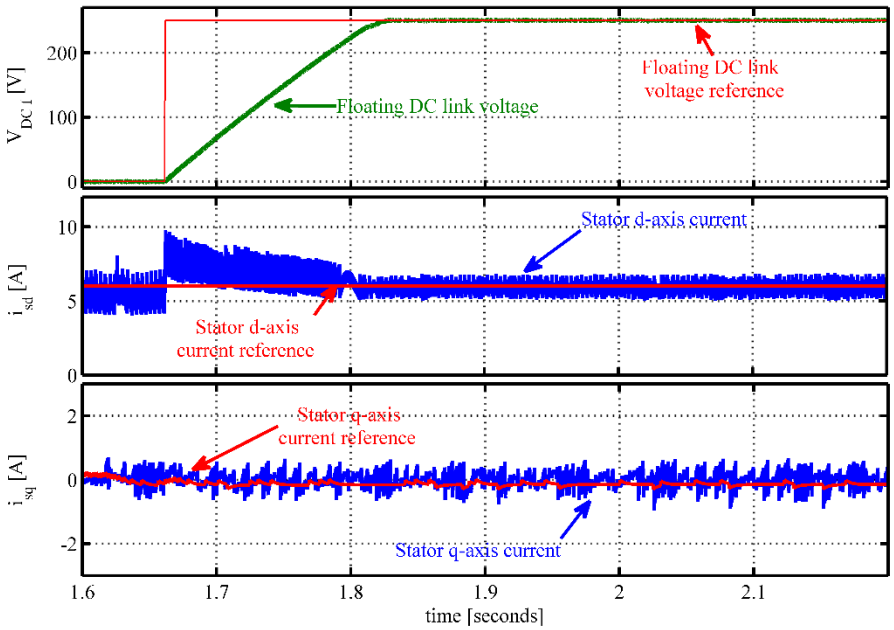


Figure 7.33 Charging transient of the floating capacitor voltage after the machine was magnetised, from top to bottom: floating DC link voltage and reference, stator d-axis current and reference *d*-axis current and stator q-axis current.

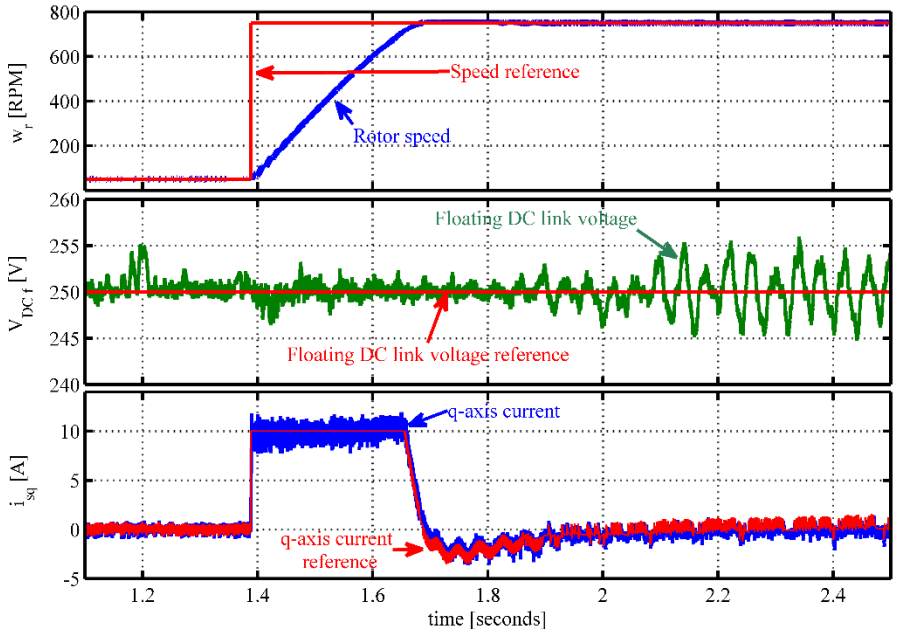


Figure 7.34 Response of the controller when a speed reference of 700rpm was set to the controller, from top to bottom: rotor speed, floating DC link voltage and stator q-axis current.

A reference torque was applied to the converter by running the DC machine in torque control mode (braking for IM) after the speed reaches steady-state, results are shown in Figure 7.35.

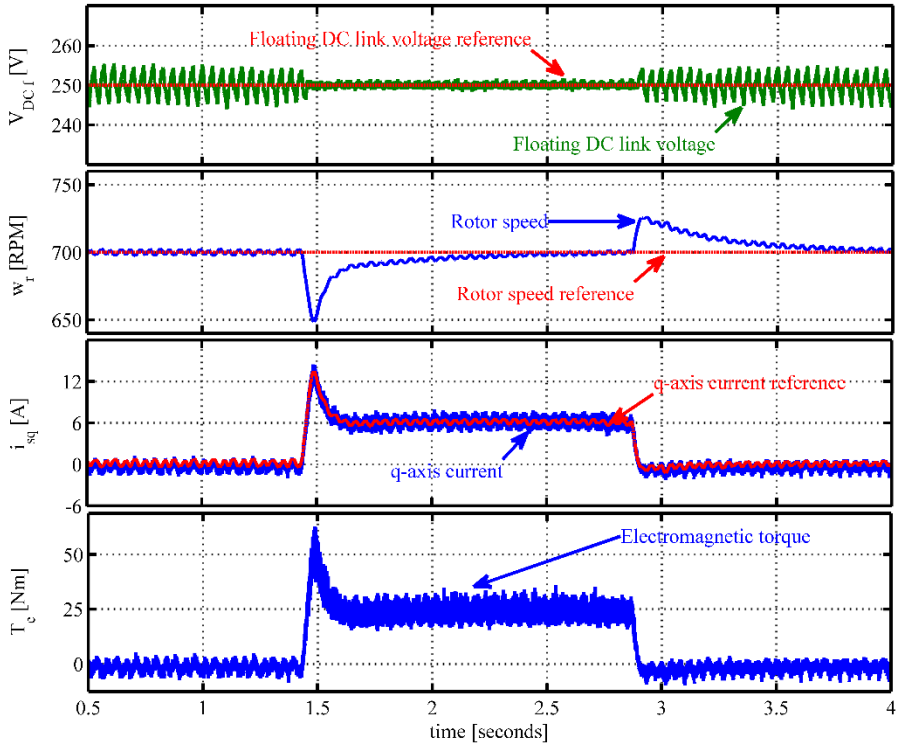


Figure 7.35 Response of the controller when a step load of 25Nm was set to the controller, from top to bottom: floating DC link voltage, rotor speed, stator q-axis current and electromagnetic torque.

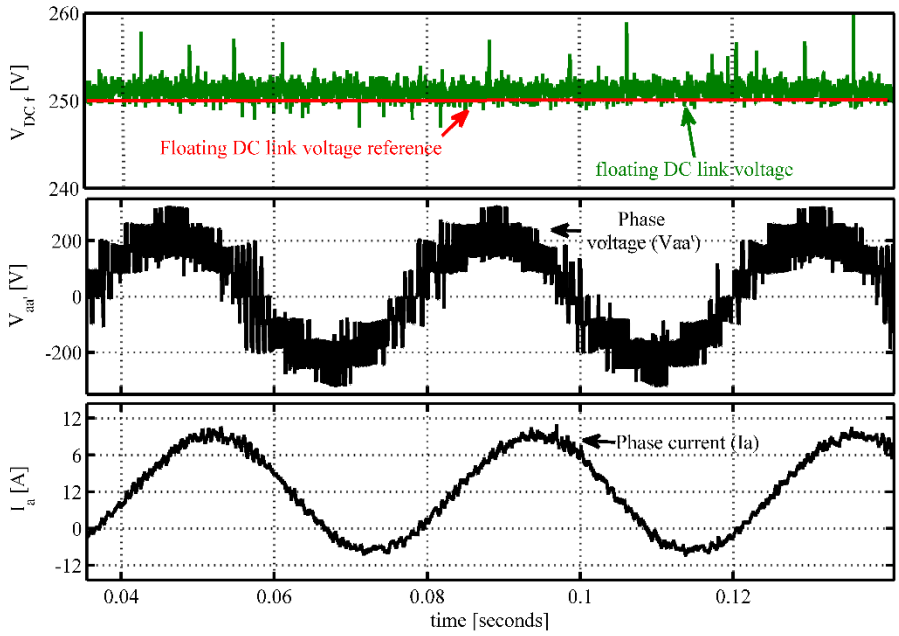


Figure 7.36 Floating DC link voltage, phase voltage and current when the machine was loaded.

It can be seen from the Figure 7.35 that the torque producing currents steps up immediately to counter the load torque. The speed decreased momentarily but recovers in 0.1seconds.

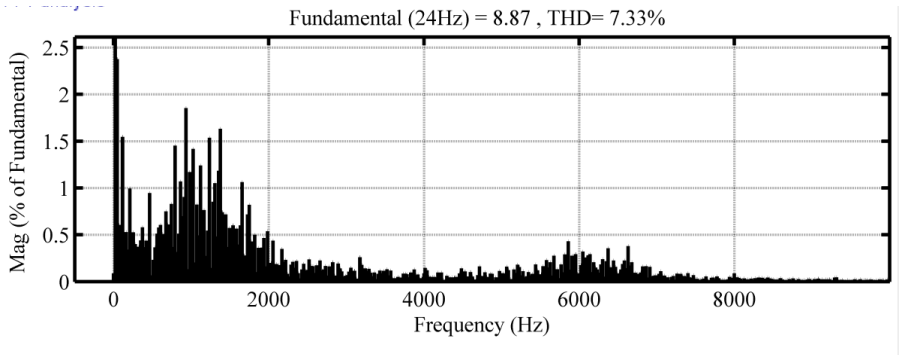


Figure 7.37 Frequency spectrum of load current when the machine was loaded.

It is evident from the results that the floating voltage control was better when the load was drawing real power. The fluctuations still remain in the floating DC link voltage, this is due to the operation of the proposed converter at its highest limit, as there is a minimum number of charging switching sequences. The fluctuation of the DC link voltage is acceptable up to 10% but in this case the fluctuation is below 3%. Figure 7.36 shows the converter's operation in the multilevel mode for the machine drive. It is evident from the figure that the converter can control the floating capacitor voltage and can create a multilevel output voltage. The frequency spectrum is shown in Figure 7.37 for when the machine was loaded.

7.4 Experimental results with modulated model predictive control

Results for the converter operating with modulated model predictive current control are shown in this section. The floating capacitor control was integrated into the modulation scheme, as described in Chapter 6. Including capacitor control inside modulation scheme will significantly improve the calculation time in the signal processor.

To obtain results with modulated model predictive control with a static R-L load the main converter was supplied with a voltage of 200Volts and the floating capacitor voltage reference was kept constant at 100Volts. The results for the two-level mode of operation of the proposed converter were obtained with a reference current of 4Amps. The results are shown in Figure 7.38. It can be seen from the

figure that the load current follows the reference closely and the average floating capacitor voltage value is equal to the reference value.

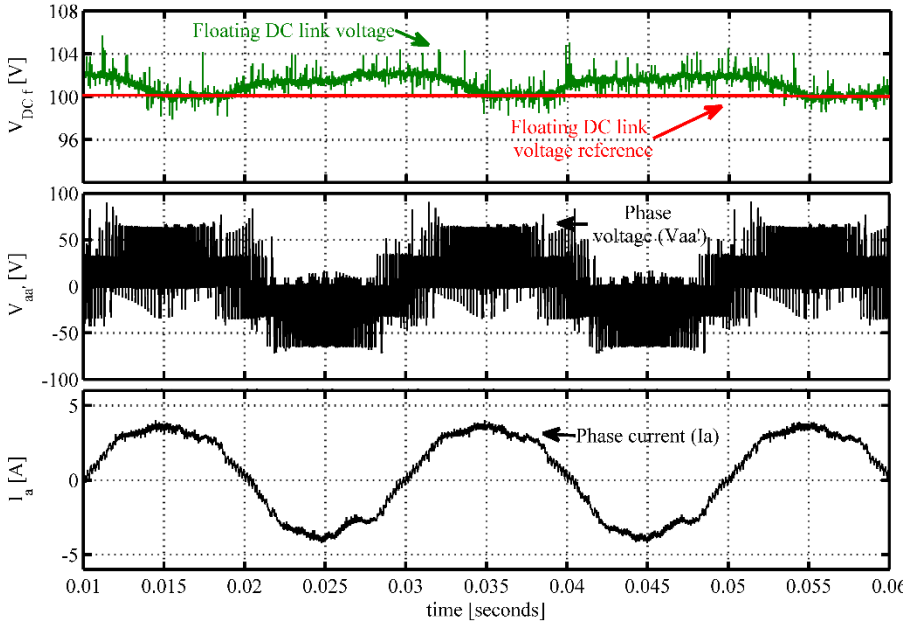


Figure 7.38 Response of the modulated predictive controller when 4Amps current was demanded from the system, from top to bottom: Floating DC link voltage, phase voltage ($V_{aa'}$) and load current (I_a).

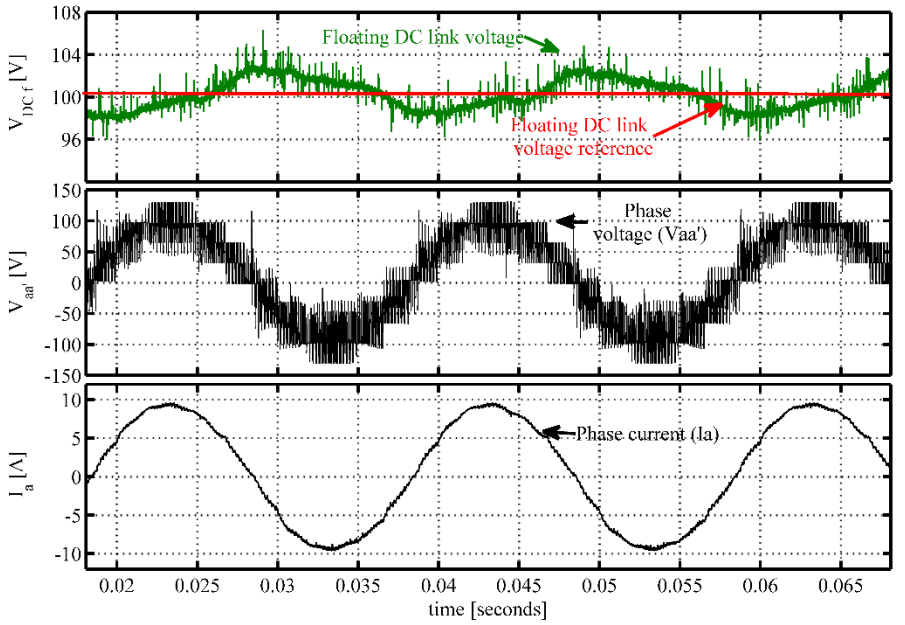


Figure 7.39 Response of the modulated predictive controller when 9Amps current was demanded from the system, from top to bottom: Floating DC link voltage, phase voltage ($V_{aa'}$) and load current (I_a).

To show the operation of the converter in multilevel mode, a reference current of 9Amps was set. The results are shown in the Figure 7.39.It can be seen that the voltage across the load has nine discrete voltage levels (similar to three-level converters) and the load current and floating DC link voltage is following the reference closely.

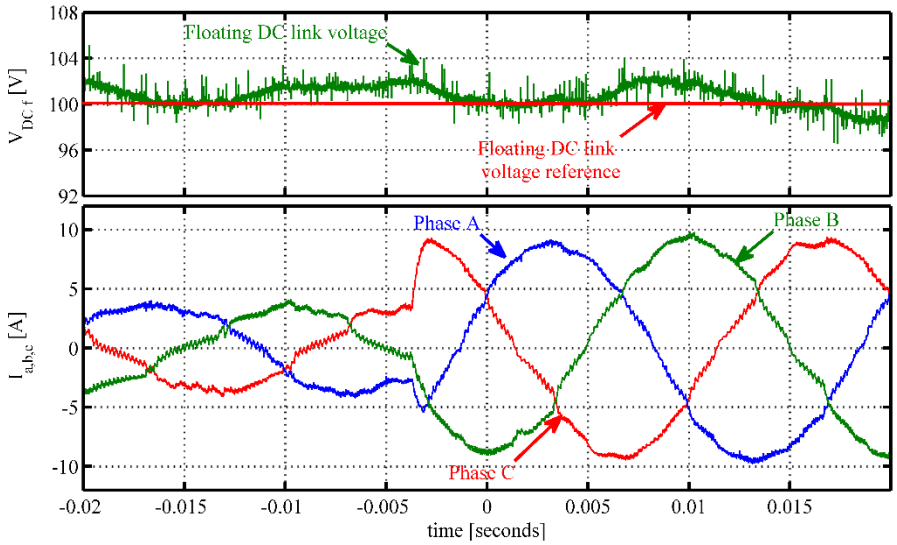


Figure 7.40 Response of the modulated predictive controller when a step change in current demanded from the system, from top to bottom: floating DC link voltage and phase currents.

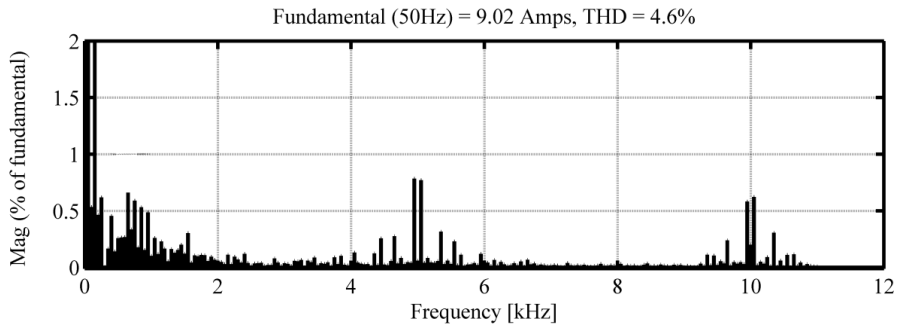


Figure 7.41 Frequency spectrum of load current when 9Amps current was demanded.

To show the dynamic response of the control a step change in reference current was applied to the controller. The current reference was changed from 4Amps to 9Amps and the results are shown in Figure 7.40. It can be seen from the figure that the load current changes quickly to match the reference values and has no impact on the floating capacitor controller.

A frequency spectrum of the load current is shown in Figure 7.41 for when the converter was operating at multilevel mode. It can be seen from the frequency

spectrum that most of the harmonics are clustering around the sampling frequency. The lower order harmonics can also be seen in the spectrum but it is unavoidable for the current controlled predictive control algorithm. The amplitude of the lower order harmonics can be reduced by increasing the sampling frequency. It is also evident from the frequency spectrum that the filter design will be much easier as the cut-off frequency can be set according to the sampling frequency.

7.5 Comparison of control dynamics

In this section, the control dynamics results are compared in terms of load current, control dynamics and the utilisation of the signal processor. All three control strategies PI, MPC and MMPC are compared for the operation with the open phase R-L load. Two control strategies PI and MPC are compared for IM drives as the MMPC for IM drive results were not taken. A comparison of load current and voltage harmonic distortion are shown in Tables 7.1 and 7.2. The SVM scheme has the lowest current harmonic distortion. The current THD for the MPC algorithm is higher than for the MMPC algorithm due to its variable switching frequency.

Table 7.1 THD comparison of different controllers for R-L load.

Modulation	Sampling frequency (kHz)	Load current THD (%)
PI	5	2.6
MPC	12.5	7.2
MMPC (Cap-charge in cost-function)	5	4.6
MMPC (Cap-charge in modulation)	5	4.6

Table 7.2 THD comparison of different controllers for IM drive.

Modulation	Sampling frequency (kHz)	Load current THD (%)
PI	5	2.5
MPC	12.5	7.3

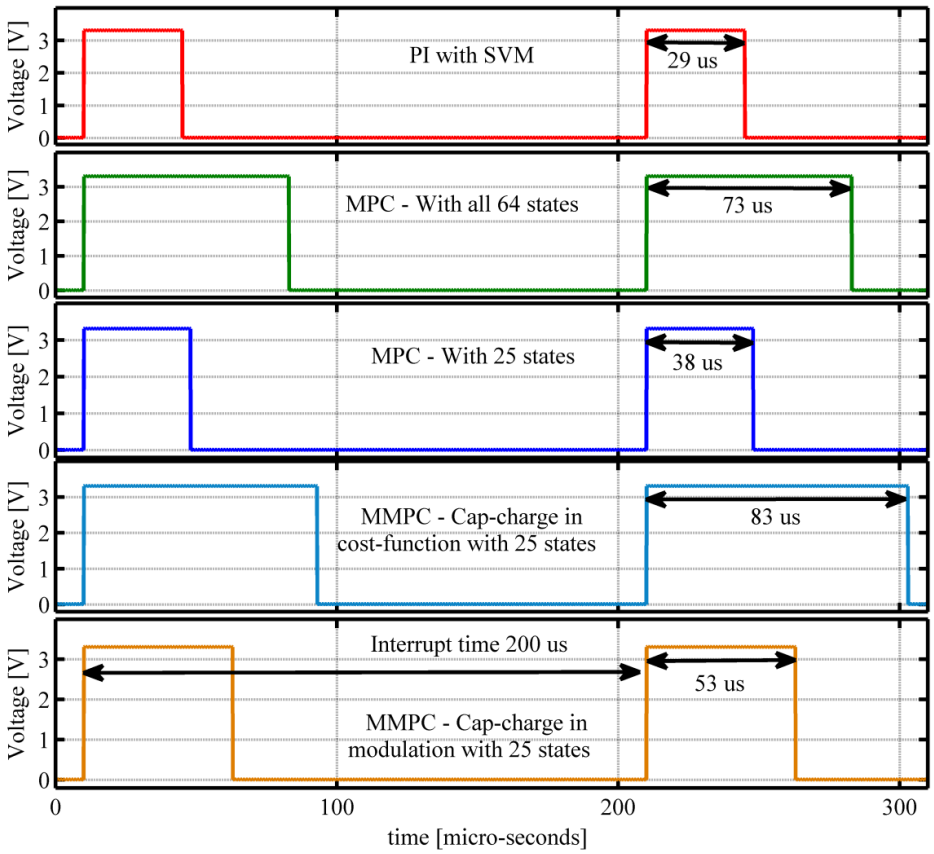


Figure 7.42 Computational time for the signal processor for different control algorithms.

It can be seen that the experimental THD values are much higher than the simulation results shown in Chapter 6. This is because the experimental converters experience additional distortion in current waveforms due to the parasitic coupling capacitance between two converters. Additionally, the dead time spikes are completely removed in simulation results, but due to diode reverse recovery along with the turn on and off delay of the power semiconductor devices it was difficult to completely remove the dead-time spike in the practical waveforms.

The calculation time of the digital signal processor for the different control algorithms are shown in Figure 7.42. It can be seen that the PI based controller along with the MPC controller utilising 25 states has the lowest computation time. The modulated model predictive control with the capacitor charging control in the cost-function algorithm has the highest calculation due to the design of that specific control scheme, but the calculation time is reduced by introducing the capacitor control inside modulation scheme. The reduction of calculation time is significant and is shown in Figure 7.42.

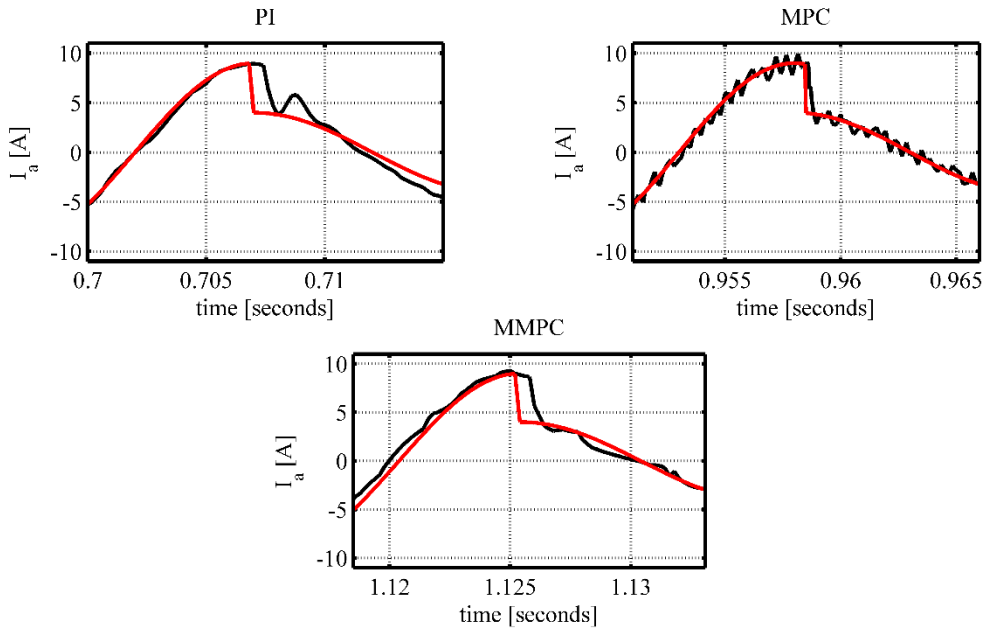


Figure 7.43 Response of control methods for a step change in the amplitude of the reference current for R-L load.

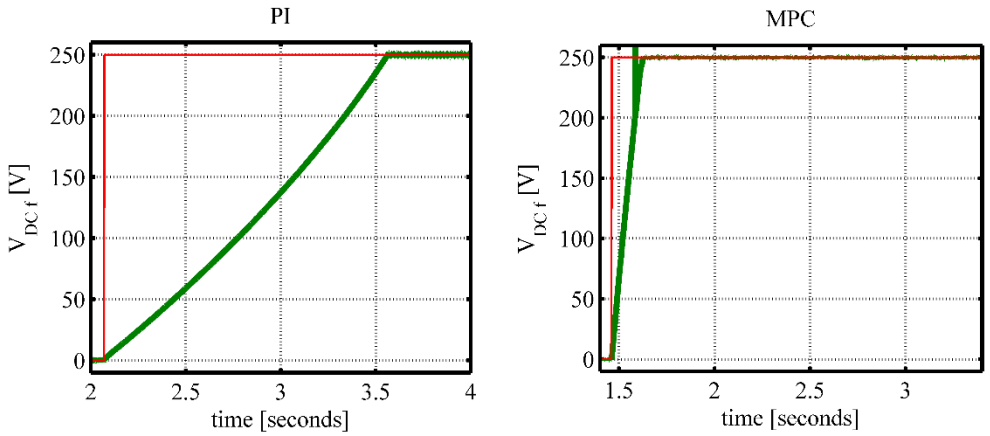


Figure 7.44 Response of control methods for a step change in the amplitude of the reference floating DC link voltage for induction motor drive.

The response of the controllers when a step change in reference current was set for R-L load operation is shown in Figure 7.43. It can be seen that the MPC algorithm has the faster dynamic response than the PI based and MMPC based control scheme. A floating capacitor charging transient is shown in Figure 7.44 for the IM drive. A step reference floating capacitor voltage from 0 to 250Volts was set to the controller after the machine was magnetised. The response of the PI based controller is much slower than the MPC based controller.

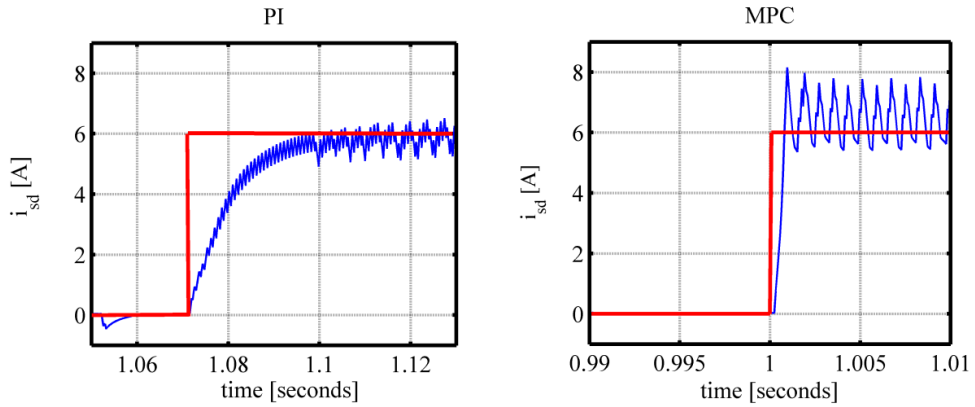


Figure 7.45 Response of control methods for a step change in the amplitude of the reference flux producing current (i^*_{sd}) for induction motor drive.

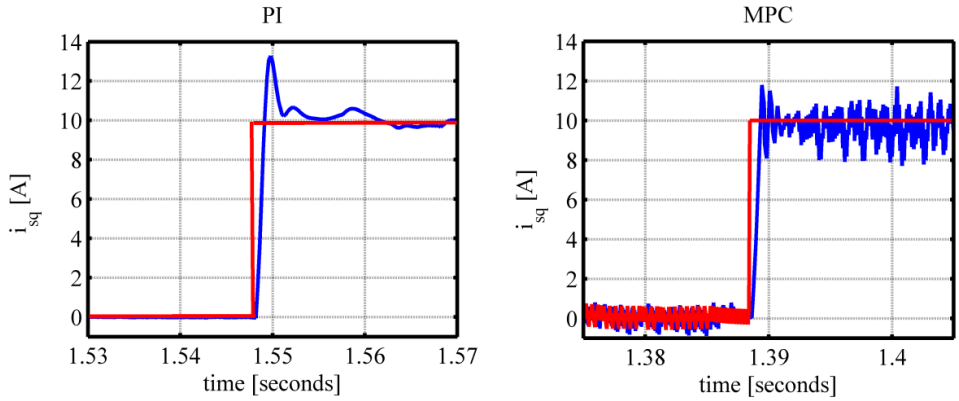


Figure 7.46 Response of control methods for a step change in the amplitude of the reference torque producing current (i^*_{sq})

The transients for the current controllers of IM drive are shown in Figure 7.45 and 7.46. It is evident from the figures that the PI based controllers have overshoot and undershoot, but with minimum steady-state fluctuations. The transient responses of the MPC algorithm are much faster and no significant overshoot can be seen. The average current for the MPC controller follows the reference closely but the fluctuation is higher than for the PI based controller due to the variable switching frequency of the MPC control algorithm.

7.6 Conclusion

This chapter has shown the practical results for the proposed converter along with three different control algorithms to support the simulation results and analysis presented in previous chapters. The results are shown for an open phase R-L load as well as with an IM drive. The experimental results are deviated slightly from the

simulation results due to considering ideal switches and not considering the parasitic of the practical converters. It can be concluded that the proposed converter can control the floating capacitor voltage and can also achieve multilevel output voltage waveforms.

Chapter 8

Conclusion and Future work

8.1 Summary

This thesis has presented a modified dual inverter topology in order to decrease system weight and volume as well as to increase system efficiency. The proposed converter system uses a floating capacitor bank in one of the two-level converters, thus avoids using a bulky isolation transformer. The floating capacitor is controlled using redundant states to achieve half of the main inverters DC link voltage. Using this particular voltage ratio (2:1) the load voltage of the converter experience a voltage spike during the dead-time interval. This voltage spike is mostly avoided by delaying the dead-time interval for each phase legs. Simulation results were presented and shown that the converter can control the floating capacitor voltage and can achieve multilevel load voltage waveform for both static R-L load and IM drive. A test rig has also been build and the performance of the converter was validated using high performance motor drive.

The dual-converter possess almost all the advantages of single sided multilevel converter topologies, however, due to the open phase connection of the load the common mode current can flow through the system. This phenomenon can be observed in the three phase H-bridge system and the challenge can be overcome by introducing isolated supplies. The Dual inverter system applies the same principle but requires only one isolated supply to reduce the path of common mode current flow. The supplies can be isolated using an isolation transformer thus increase losses, size and weight of the system, shown in Chapter 4. There has been previous research on operating dual inverter systems with a single source and every method introduced new challenges which either limit the modulation index, introduce extra circuitry or increase control complexity.

Taking the above challenges related to dual inverter topology into consideration, the research presented in this thesis uses a dual inverter where one of the bridge inverters was floating. The floating inverter's voltage can be controlled using the redundant switching combinations and a simple bang-bang control inside modulation scheme. A dual, two-level inverter was selected to evaluate the proposed modification of the traditional dual inverter system. The DC link voltage ratio of 2:1 was selected to achieve three-level output voltage waveform as well as to operate the converter at higher modulation index than dual inverter with equal voltage sources, as shown in Chapter 5. A space vector modulation technique was considered and the capacitor control was introduced inside modulation scheme using a bang-bang controller, thus the requirement of an additional PI controller was eliminated. It has also been shown in Chapter 5 that the dual inverter system with unequal voltage sources can introduce additional transient voltage spikes during the dead time interval. A method was proposed to avoid these unwanted spikes by delaying the dead time interval of each phase leg by the duration of the dead-time interval. Simulation results were also shown and the results suggest that the converter system can control floating inverters DC link voltage and was able to achieve multilevel output voltage waveform.

The results shown in Chapter 5 were acquired using PI based current controllers. The PI based control is slow and the system can experience damped, undamped or critically damped response depending on the controller design. To overcome these challenges an advanced control scheme was introduced in Chapter 6, predictive control. Predictive control was used to control the load currents and floating DC link voltage in a single control loop for the proposed converter topology and does not require an additional modulation scheme. The controller has a very fast dynamic response and was successfully implemented for the proposed system using a static R-L load and with an IM drive. Results from the predictive control suggest that the controller has an inherent variable switching frequency, thus the harmonic distortion was higher as shown in Chapter 6.

To overcome the challenge of variable switching frequency, a modified predictive control technique was introduced in Chapter 6. The modified predictive control integrates a modulation scheme into the traditional predictive control algorithm. A detailed description of the control algorithm with simulation results was presented in

Chapter 6. The control algorithm was successfully implemented for the proposed system and the results suggest that the variable switching nature of the traditional predictive control algorithm was eliminated and the harmonic distortion was much lower.

Finally, the simulation results presented in Chapter 5 and Chapter 6 were validated using experimental results. To conclude the isolation transformer from the traditional dual inverter topology was removed and the system was verified with three different control schemes. In all cases, the converter was able to control the floating capacitor voltage as well achieve multilevel output voltage waveforms.

8.2 Future work suggestions

The work presented in this thesis is focused on a dual inverter for open phase load used in conjunction with a predictive current control algorithm. The proposed system has been implemented employing standard two-level three phase inverters. The reason for using a two-level inverter was to prove the proposed topology using a much simpler system before progressing to a rather complex system. There are a few areas which can lead to further improvement of the proposed converter topology, a few such ideas are described in brief.

8.2.1 Increased modulation index

The floating bridge inverter proposed in this thesis has lower than ideal DC bus utilisation due to the limitation of redundant charging and discharging switching states. The converter system can control the floating DC link voltage if the reference voltage resides inside vector diagram produced by the main inverter, shown in Figure 5.2 and 5.3. Among the two converters, dual inverter with asymmetric voltage sources was selected for this thesis due to increased limit of modulation index. The way to further increase the modulation index for a floating bridge topology is to increase the ratio of two sources. The Dual two-level inverter with an asymmetric sources ratio of 3:1 has unevenly distributed voltage vectors thus it is difficult to modulate the system as a floating bridge topology. The dual inverter system can be used with a voltage ratio of 4:1 if the main inverter is replaced with a three-level converter, Shown in Figure 8.1. Using this ratio along with a three-level converter

the modulation index can be increased from 0.66 to 0.8 along with the increment of the load voltage levels from 9 (three-level) to 17 (five-level).

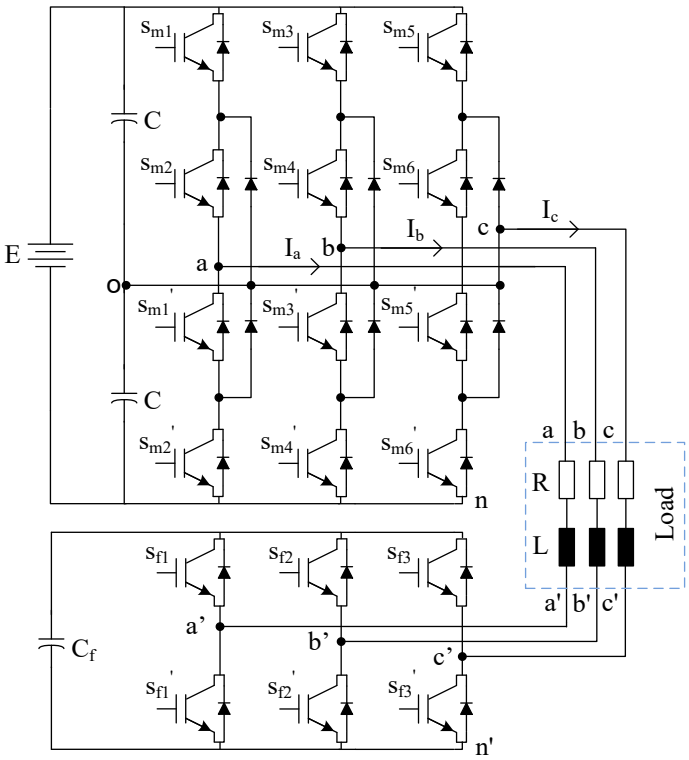


Figure 8.1 Dual floating bridge inverter with a three-level NPC converter as a main bridge.

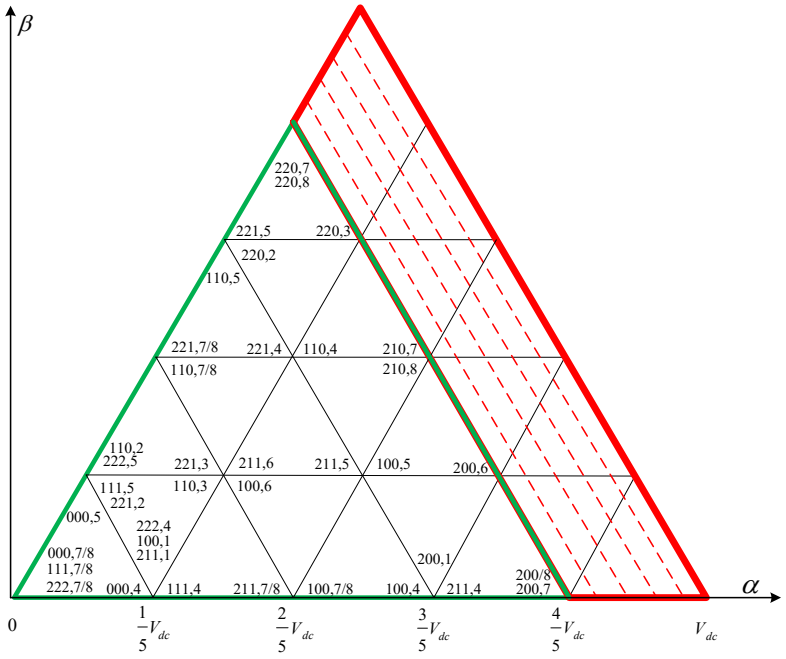


Figure 8.2 Space vector diagram of dual two-level inverter with three-level NPC as a main bridge with a DC link voltage ratio of 4:1.

8.2.2 Implement MMPC algorithm for IM drive

This thesis considered model predictive control algorithm for the proposed floating bridge topology. Predictive control is advantageous due to faster control dynamics and does not require tuning compared to PI based controllers. Additionally, the controller can independently select switching sequence thus eliminated the need for additional modulation schemes. The well-known challenge of the predictive control algorithm is variable switching and can introduce additional lower order harmonics. To overcome this problem a modified predictive control algorithm was introduced in Chapter 6 with a modulation scheme inside cost function algorithm. Simulation results were presented for simple R-L load and IM drive. Due to time limitations, the IM drive results were not experimentally validated. The experimental validation is necessary to validate the theory and simulation, this will be considered in the future.

Appendix A

Three Phase Isolation Transformer Design

A.1 Design of isolation transformer

A three phase isolation transformer is designed to eliminate the path of common mode current flow using the area product approach. In [139] a design procedure using core geometry approach is shown where the iron core is selected using according to the core geometry value. The similar approach is used to design the isolation transformer using area product. First, the design data are specified as shown in Table A.1 design data are specified according to the operation of the drive system, shown in Chapter 4.

Table A.1 Three phase isolation transformer design specification.

Primary line voltage	$V_{line(P)}$	230 V
Output voltage	V_o	135 V
Output current	I_o	190 A
Fundamental frequency	f	400 Hz
Efficiency	η	95 %
Regulation	α	5%
Flux density	B_{ac}	1.5 Tesla
Window utilisation factor	$Ku = K_{u(P)} + K_{u(S)}$	0.4
Diode voltage drop	V_d	1 V
Current density	J	350 A/cm^2
Rectifier	Full bridge	
Input/Output	Delta/Delta	
Magnetic material	Arnon 5	
Copper	100% IACS	

The full load power of the drive system is 50kW and the dual inverter with equal voltage sources will share the power between the converters. Thus the isolated side

of the converter will contribute 50% power to the load. The DC link voltage of the isolated converter is 135V and the DC link current of the isolated converter is close to 190A. The design specifications are shown in Table A.1.

To start with the design process, the apparent power P_t of the transformer is calculated. The apparent power of a transformer is the combined power of the primary and secondary side of the transformer. The apparent power can be defined as

$$P_t = P_{in} + P_o \tag{A.1}$$

$$\begin{aligned} P_t &= P_o(1+\frac{1}{\eta}) \\ P_o &= I_o(V_o + 2*V_d) = 26030\,W \\ P_t &= 53430\,W \end{aligned} \tag{A.2}$$

where P_o, Pin specifies output and input power of the transformer. The term η specifies the efficiency of the transformer which is specified by the designer. The next step is to calculate area product A_p which is the product of iron and window area as shown in equation for three phase system

$$A_p = 3\left[\frac{W_a}{2} A_c\right]\left[cm^4\right] \tag{A.3}$$

where W_a is the window area and A_c is the iron area for the transformer. The area product can also be calculated using the formula shown in the equation.

$$\begin{aligned} A_p &= \frac{P_t \times 10^4}{4.44 B_{ac} f K_u J}\left[cm^4\right] \\ A_p &= \frac{53430 \times 10^4}{4.44(1.5)(400)(0.4)(350)}\left[cm^4\right] \\ A_p &= 1433\left[cm^4\right] \end{aligned} \tag{A.4}$$

Where B_{ac} is the flux density of the magnetic material, f is the fundamental frequency, K_u is the window utilisation factor and j is the current density for the copper windings. According to the area product value, a three phase EI core is

selected. The core selection table can be found in [139]. The core specifications are shown in Table A.2 and the dimensions of the selected core are shown in figure A.1.

Table A.2 Core geometry of the isolation transformer.

Core number	1.800EI-3φ	
Selected iron material	ARON-5	
Selected copper material	100% IACS	
Mean length turn	MLT	26.3 cm
Iron area	A_c	19.858 cm^2
Window area	W_a	52.26 cm^2
Area product	Ap	1556.61 cm^4
Core geometry	Kg	470.453 cm^5
Surface area	At	1630 cm^2

Number of turns of the primary winding N_p is calculated [[139]]

$$N_p = \frac{V_{p(line)} \times 10^4}{4.44 B_{ac} A_c f}$$
$$N_p = \frac{230 \times 10^4}{4.44 \times 1.5 \times 19.858 \times 400} \cong 44 turns(primary) \quad \text{(A.5)}$$

The line and phase currents of the primary windings are calculated

$$I_{line(P)} = \frac{P_o}{3 V_{line(P)} \eta}$$
$$I_{line(P)} = \frac{26030}{3(230)0.95} = 39.71 A \quad \text{(A.6)}$$

$$I_{phase(P)} = \frac{39.31}{\sqrt{3}} = 22.93 A \quad \text{(A.7)}$$

Now the bare winding area of the primary windings copper wire can be calculated

$$A_{w(P)} = \frac{K_{u(P)} W_a}{4 N_P}$$
$$A_{w(P)} = \frac{0.2(52.26)}{4(44)} = 0.06 cm^2 \quad \text{(A.8)}$$

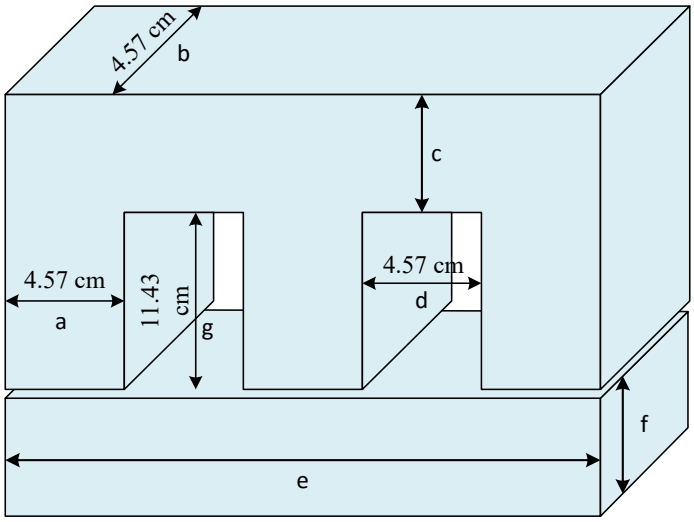


Figure A.1 Dimensions of the selected core.

Number of turns for the secondary winding is calculated using equation

$$N_{(S)} = \frac{N_{(P)}V_{(S)}}{V_{(P)}}\left(1+\frac{\alpha}{100}\right) \tag{A.9}$$

Where α is the voltage regulation for the transformer. Now the voltage of the secondary winding is calculated

$$\begin{aligned} V_{(S)} &= 0.740(V_o + 2V_d) \\ V_{(S)} &= 101.4V \end{aligned} \tag{A.10}$$

The number of turn for the secondary of the converter

$$N_{(S)} = \frac{44(101.4)}{230}\left(1+\frac{5}{100}\right) \cong 21\ turns(\text{sec}ondary) \tag{A.11}$$

The bare winding area of the secondary windings copper wire can be calculated

$$\begin{aligned} A_{w(P)} &= \frac{K_{u(S)}W_a}{4N_S} \\ A_{w(P)} &= \frac{0.2(52.26)}{4(21)} = 0.125cm^2 \end{aligned} \tag{A.12}$$

The line and phase currents of the primary windings are calculated using equations

$$I_{line(S)} = 0.471(I_o) = 89.49\ A \tag{A.13}$$

$$I_{phase(S)} = \frac{89.49}{\sqrt{3}} = 51.66\ A \tag{A.14}$$

Using these values a model of the isolation transformer is designed using MagNet simulation platform where the iron losses were calculated, the loss data is presented in Chapter 4.

A.2 Iron weight analysis

To design the isolation transformer the magnetic material is selected to achieve maximum flux density of 1.5Tesla. The name of the magnetic material is ARNON 5 SILICON STEEL, the datasheet can be found in [136]. According to the datasheet, the material mass density is 7650 kg/m^3, using these value the designed transformers iron weight is calculated. The iron volume is calculated using equation A.15 which is deduced using Figure A.1.

$$\begin{aligned}
&Iron\ area = 19.858[cm^2] \\
&Iron\ volume\ for\ E\ legs = a \times b \times g = 4.572 * 4.572 * 11.43 = 239[cm^3] \\
&Iron\ volume\ for\ I\ \text{section} = e \times f \times b = (5 \times a) \times 4.57 \times 4.57 = 477.22[cm^3] \\
&Total\ iron\ volume = (3 \times 239) + (2 \times 477.22) = 1673[cm^3] \\
&Mass\ density\ for\ selected\ material = 7650[kg/m^3] \\
&Total\ iron\ weight = 1.673 \times 10^{-3} \times 7650 = 12.8[kg]
\end{aligned} \tag{A.15}$$

A.3 Copper weight analysis

Annealed copper is selected for winding material named as Copper: 100% IACS. The mass density of the material is 8940 kg/m^3 and the electric resistivity of the material is 1.724e-8 Ohms.m. Using these values the volume of the bare copper and the weight and the resistance of the windings are calculated.

Primary winding copper volume

$$\begin{aligned} &Copper\ area\ for\ one\ slot = A_{w(p)} \times N_{s(p)} = 0.06 \times 44 = 2.64[cm^2] \\ &Copper\ volume\ for\ one\ winding = 2.64 * MLT = 2.64 * 26.3 = 69.43[cm^3] \end{aligned} \quad (A.16)$$

Secondary winding copper volume

$$\begin{aligned} &Copper\ area\ for\ one\ slot = A_{w(s)} \times N_{s(s)} = 0.125 \times 21 = 2.62[cm^2] \\ &Copper\ volume\ for\ one\ winding = 2.625 * MLT = 2.62 * 26.3 = 69.04[cm^3] \end{aligned} \quad (A.17)$$

Total copper volume

$$\begin{aligned} &Copper\ volume\ for\ six\ windings = (69.432 \times 3) + (69.04 \times 3) = 415.41[cm^3] \\ &Mass\ density\ for\ selected\ material = 8940[kg/m^3] \\ &Total\ copper\ weight = 4.154 \times 10^{-4} \times 8940 = 3.72[kg] \end{aligned} \quad (A.18)$$

$$Total\ weight\ of\ 3\phi\ transformer\ is = 12.8 + 3.72 = 16.52[kg] \quad (A.19)$$

A.4 Loss analysis of the transformer

Losses of single primary winding can be calculated as

$$Length\ of\ the\ winding, L_p = MLT \times N_{s(p)} = 26.3 \times 44 = 1157[cm] \quad (A.20)$$

$$Primary\ resistance, R_p = \rho \frac{L_p}{A_{wp}} = 1.724e^{-6} \frac{1157}{0.06} = 0.0332\,\Omega \quad (A.21)$$

$$Primary\ copper\ loss, P_{cu(p)} = I^2_{primary(p)} \times R_p = 22.93^2 \times 0.0332 = 17.5W \quad (A.22)$$

Losses of single secondary winding can be calculated as

$$Length\ of\ the\ winding, L_p = MLT \times N_{s(p)} = 26.3 \times 21 = 552.3[cm] \quad (A.23)$$

$$Primary\ resistance, R_p = \rho \frac{L_p}{A_{wp}} = 1.724e^{-6} \frac{552.3}{0.125} = 7.62e^{-3}\ \Omega \quad (A.24)$$

$$Primary\ copper\ loss, P_{cu(p)} = I^2_{primary(p)} \times R_p = 51.66^2 \times 7.62e^{-3} = 20.33W \quad (A.25)$$

Total copper loss of the isolation transformer

$$Copperloss, P_{cu} = (3 \times P_{cu(p)}) + (3 \times P_{cu(s)}) = 51.5 + 61 = 112.5W$$

Appendix B

Machine and Power Electronics Parameter for Loss Calculation

B.1 Machine parameter

Stator resistance	Rs	0.00206	Ohm
Stator leakage inductance	Lls	0.0207e-3	H
Rotor Resistance	Rr	0.00276	Ohm
Rotor leakage inductance	Llr	0.047e-3	H
Magnetising inductance	Lm	0.69e-3	H
Pole number	P	2	
Rated voltage	Vrat	150	Volts
Maximum stator current	Imax	400	Amps
Inertia	J	0.01	
Rated torque	T	55	N-m

B.2 Power electronics

Dc Link voltage	Vdc	270	Volts
Modulation index	m	0.83	
Blocking voltage (two-level)	V_dual	600	V
Current rating (for all)	I_rat	600	Amps
Dead time	Dt	1.7e-6	Sec

Appendix C

Coordinate Transformation

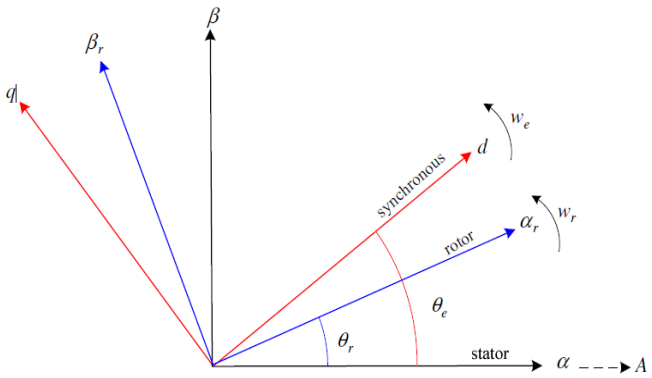


Figure C.1 Stator(rotor) synchronous reference frame

Figure C.1 shows the reference frame used to develop the vector control theory. Three phase stator is transformed to two phase system by the mean of Clarke's transformation[149]. Then α axis of the stator frame is aligned with the a-phase of the three phase system. Transformation matrix is shown in equation D.1

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{C.1}$$

Now, transformation from stationary to rotational reference frame can be done using Parks transformation as shown in equation C.1

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \begin{bmatrix} \cos(\lambda) & \sin(\lambda) \\ -\sin(\lambda) & \cos(\lambda) \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{C.2}$$

The inverse transformations from rotational to stationary reference frame can be done using following equations

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \begin{bmatrix} \cos(\lambda) & -\sin(\lambda) \\ \sin(\lambda) & \cos(\lambda) \end{bmatrix} \begin{bmatrix} f_d \\ f_q \end{bmatrix} \tag{C.3}$$

Finally, the fictitious two phase system can be transferred to the original two phase system using inverse Clarke's transformation, as shown in equation C.4.

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{C.4}$$

Where, f denotes either voltage or current as appropriate. The subscript α-β denotes the fictitious two phase system after Clarke's transformation is applied. The terms in subscript d-q represents the two phase system after rotational transformation is applied. All the control shown in this thesis were achieved using these transformation equations.

Appendix D

Indirect Rotor Flux Oriented Control of Induction Machine

The main purpose of field oriented vector control is to decouple flux and torque producing current so that AC induction machine can work as a dc machine. The basics of field oriented control involve the control of stator current of an induction machine in a way that one component of the current always aligned with the field and the second component is orthogonal. For a rotor flux oriented control the flux component of stator current is aligned with d-axis with synchronously rotating d-q frame so and thus it controls rotor flux. The orthogonal component aligned with the q axis and it controls the torque of the machine. Dynamic d-q equations of induction machine rotating at arbitrary speed can be written as

$$\begin{aligned} V_{ds} &= R_s i_{ds} + \frac{d\psi_{ds}}{dt} - \omega_e \psi_{qs} \\ V_{qs} &= R_s i_{qs} + \frac{d\psi_{qs}}{dt} + \omega_e \psi_{ds} \\ V_{0s} &= R_s i_{0s} + \frac{d\psi_{0s}}{dt} \end{aligned} \tag{D.1}$$

$$\begin{aligned} V_{dr} &= 0 = R_r i_{dr} + \frac{d\psi_{dr}}{dt} - (\omega_e - \omega_r)\psi_{qr} \\ V_{qr} &= 0 = R_r i_{qr} + \frac{d\psi_{qr}}{dt} + (\omega_e - \omega_r)\psi_{dr} \\ V_{0s} &= 0 = R_r i_{0r} + \frac{d\psi_{0r}}{dt} \end{aligned} \tag{D.2}$$

Where the flux of the machine are given by

$$\begin{aligned}\psi_{ds} &= L_s i_{ds} + L_m i_{dr} \\ \psi_{qs} &= L_s i_{qs} + L_m i_{qr} \\ \psi_{0s} &= L_s i_{0s}\end{aligned} \tag{D.3}$$

$$\begin{aligned}\psi_{dr} &= L_r i_{dr} + L_m i_{ds} \\ \psi_{qr} &= L_r i_{qr} + L_m i_{qs} \\ \psi_{0r} &= L_r i_{0r}\end{aligned} \tag{D.4}$$

The mechanical subsystem which outputs torque and rotor speed is designed using the equations provided below:

$$T_e = \frac{3}{2}\frac{p}{2}\frac{L_m}{L_r}\left(\psi_{dr} i_{qs} - \psi_{qr} i_{ds}\right) \tag{D.5}$$

$$\omega_e = \frac{p}{2j}\int (T_e - T_L)dt \tag{D.6}$$

And

$$\omega_m = \omega_e \frac{60}{(p/2)*2\pi} \tag{D.7}$$

Now for rotor flux oriented scheme, reference rotor flux vector is aligned with the d-axis of reference frame means reference rotor flux has no projection on q axis so

$$\psi_{qr} = 0 \tag{D.8}$$

$$T_e = \frac{3}{2}\frac{p}{2}\frac{L_m}{L_r}\left(\psi_{dr} i_{qs}\right) \tag{D.9}$$

Now from (D.4)

$$\begin{aligned} i_{dr} &= \frac{\psi_{dr} - L_m i_{ds}}{L_r} \\ i_{qr} &= -\frac{L_m i_{qs}}{L_r}\end{aligned} \tag{D.10}$$

Now, replacing i_{dr} & i_{qr} in stator flux equations in (D.3)

$$\begin{aligned}\psi_{ds} &= \sigma L_s i_{ds} + \frac{L_m}{L_r}\psi_{dr} \\ \psi_{qs} &= \sigma L_s i_{qs}\end{aligned} \tag{D.11}$$

Here

$$\sigma = 1 - \frac{L_m^2}{L_s L_r} \tag{D.12}$$

Replacing ψ_{ds} & ψ_{qs} in stator voltage equations in D.1

$$\begin{aligned}V_{ds} &= R_s i_{ds} + \sigma L_s \frac{d}{dt}(i_{ds}) + \frac{L_m}{L_r}\frac{d}{dt}(\psi_{dr}) - \left\{\omega_e \sigma L_s i_{qs}\right\} \\ V_{qs} &= R_s i_{qs} + \sigma L_s \frac{d}{dt}(i_{qs}) + \left\{\omega_e \sigma L_s i_{ds} + \omega_e \frac{L_m}{L_r}\psi_{dr}\right\}\end{aligned} \tag{D.13}$$

Equations shown in D.13 are used to develop the vector control scheme. Here the terms inside the second bracket are called compensation terms. Now the rotor equations in terms of i_s & ψ_r become

$$\begin{aligned}V_{dr} = 0 &= \frac{R_r}{L_r}\psi_{dr} - \frac{L_m}{L_r}R_r i_{ds} + \frac{d}{dt}\psi_{dr} - (\omega_e - \omega_r)\psi_{qr} \\ V_{qr} = 0 &= \frac{R_r}{L_r}\psi_{qr} - \frac{L_m}{L_r}R_r i_{qs} + \frac{d}{dt}\psi_{qr} + (\omega_e - \omega_r)\psi_{dr}\end{aligned} \tag{D.14}$$

As $\psi_{qr} = 0$

$$\begin{aligned}V_{dr} = 0 &= \frac{R_r}{L_r}\psi_{dr} - \frac{L_m}{L_r}R_r i_{ds} + \frac{d}{dt}\psi_{dr} \\ V_{qr} = 0 &= -\frac{L_m}{L_r}R_r i_{qs} + (\omega_e - \omega_r)\psi_{dr}\end{aligned} \tag{D.15}$$

Now from equation D.15

$$\frac{L_r}{R_r}\frac{d}{dt}i_{mrd} + i_{mrd} = i_{sd} \tag{D.16}$$

$$\omega_e - \omega_r = \omega_{slip} = \frac{R_r L_m}{L_r \psi_{dr}} i_{qs} = \frac{R_r}{L_r}\frac{i_{qs}}{i_{mrd}} \tag{D.17}$$

Here, $\psi_{dr} = L_m i_{mrd}$ (D.18)

It can be seen from equation D.16 that torque can be controlled using q-axis stator current and from equation D.17, the flux can be controlled using d-axis stator current. It is clear that the derived equations totally decouple the torque and flux producing current.

Appendix E

PI Controller Design

E.1 Speed control loop

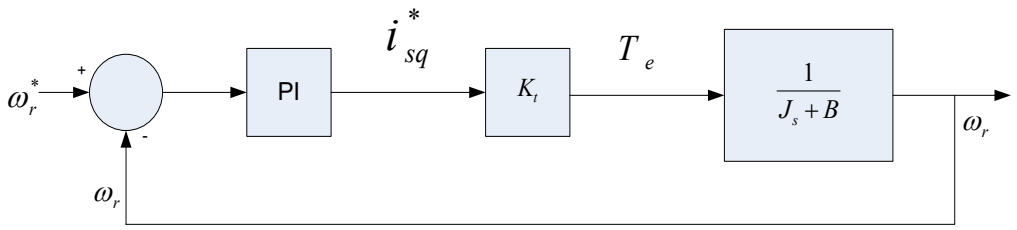


Figure E.1 Structure of speed control loop

The structure of the speed control loop is shown in FigureE.1. The s-domain transfer function for the PI controller is

$$PI(s) = \frac{k_c(s + a_c)}{s} \tag{E.1}$$

Characteristics equation for the above speed control loop is solved for *1+G(s)H(s)=0*. This is where *J=0.043* $B_m = 0.014$ and pole pair, P=2.

$$K_t = \frac{3}{2} P \frac{L_m^2}{L_r} i_{sd}^* = 4.56$$

$$0 = s^2 + \left(\frac{B + k_c k_t}{J} \right) s + \frac{k_c k_t a_c}{J} \tag{E.2}$$

$$0 = s^2 + \left(\frac{0.014 + k_c k_t}{0.043} \right) s + \frac{k_c k_t a_c}{0.043}$$

Now the coefficients of above equations are equated with equation E.3 which defines the desired close loop dynamics.

$$0 = s^2 + 2\xi\omega_n s + \omega_n^2$$

Where $\xi = 0.707$, $\omega_n = 10$ (E.3)

Now solving for k_c & a_c

$$k_c = 0.1268$$
$$\mathrm{a_c} = 7.22 \quad \text{(E.4)}$$

The PI transfer function for the speed loop can be written as

$$PI(s) = \frac{0.126(s + 7.22)}{s} \quad \text{(E.5)}$$

E.2 Current control loop

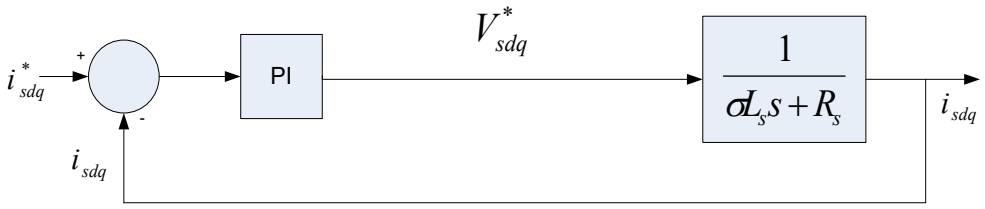


Figure E.2 Current control loop structure.

A reduced structure of current control loop is depicted in FigureB.2. The s-domain transfer function of PI controller can be written as

$$PI(s) = \frac{k_c(s + a_c)}{s} \quad \text{(E.6)}$$

The characteristics equation for current control loop is solved for *1+G(s)H(s)=0* .

$$0 = s^2 + \left(\frac{R_s + k_c}{\sigma L_s} \right) s + \frac{k_c a_c}{\sigma L_s}$$
$$where, \quad \sigma = 1 - \frac{L_m^2}{L_s L_r} = 0.0859 \tag{E.7}$$

Now replacing all the constant in equation E.7 and compared it with equation E.8

$$0 = s^2 + 2\xi\omega_n s + \omega_n^2 \tag{E.8}$$

Where $\xi = 0.707$
$\omega_n = 100$

Now solving for $k_c \,\&\, a_c$

$$k_c = 16.7$$
$$\mathrm{a_c} = 481.54 \tag{E.9}$$

The PI transfer function for the current loop can be written as

$$PI(s) = \frac{16.7(s + 481.54)}{s} \tag{E.10}$$

E.3 Field control loop

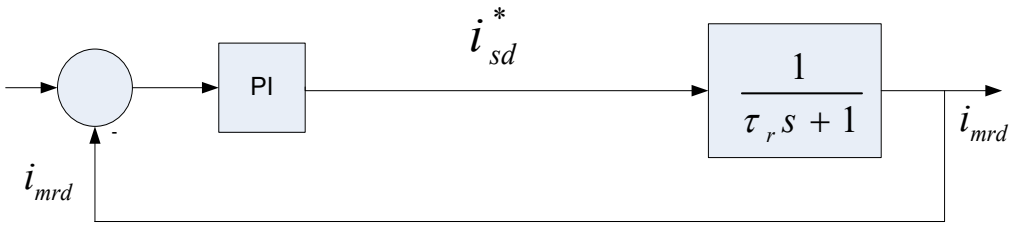


Figure E.3 Field control loop structure.

The reduced structure of field control loop is shown in Figure E.3. The s-domain transfer function for PI controller is

$$PI(s) = \frac{k_c(s + a_c)}{s} \tag{E.11}$$

The characteristics equation for field control loop is solved for *1+G(s)H(s)=0* .

$$0 = s^2 + \left(\frac{1 + k_c}{\tau_r}\right)s + \frac{k_c a_c}{\tau_r} \tag{E.12}$$

Where, $\tau_r = \frac{L_r}{r_r}$

Coefficients of the above equation is equated with the following equation

$$0 = s^2 + 2\xi\omega_n s + \omega_n^2 \tag{E.13}$$

Where $\xi = 0.707$
$\omega_n = 20$

Solving this two equation together

$$\begin{aligned} k_c &= 39.94 \\ \mathrm{a_c} &= 91.09 \end{aligned} \tag{E.14}$$

The PI transfer function for the field loop can be written as

$$PI(s) = \frac{16.7(s + 481.54)}{s} \tag{E.15}$$

Appendix F

Machine and Power electronics Parameter for Simulation and Experimental Validation

F.1 Machine parameter – star connected

Stator resistance	R_s	1.4	Ohm
Stator leakage inductance	L_{ls}	0.0115	H
Rotor Resistance	R_r	1.02	Ohm
Rotor leakage inductance	L_{lr}	0.00926	H
Magnetising inductance	L_m	0.2258	H
Pole number	P	4	
Rated voltage	V	690	Volts
Full load current	I_{rated}	12.4	Amps
Inertia	J	0.043	kgm^2
Rated torque	T	72	Nm
Frictional coefficient	B	0.014	kgm^2/second
Magnetising current	i_{sd}	7	Amps
Torque producing current	i_{sq}	16	Amps

F.2 Power electronics – for machine as a load

Main DC link voltage	V_{dc_m}	500	Volts
Floating DC link voltage	V_{dc_f}	250	Volts
Dead time	Dt	4.1e-6	Seconds
Main DC link capacitance		1250	µF
Floating DC link capacitance		3250	µF

F.2 R-L load

Resistance	R	10.6	Ohm
Inductance	L	3.8	mH
Main DC link voltage	V_{dc_m}	200	Volts
Floating DC link voltage	V_{dc_f}	100	Volts
Dead time	Dt	4.1e-6	Seconds
Main DC link capacitance		1250	µF
Floating DC link capacitance		3250	µF

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