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System-Layout-Dependent Thermally Induced Solder Stress & Reliability Implications

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System-Layout-Dependent Thermally Induced Solder Stress & Reliability Implications

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Bachelor of Science in Mechanical Engineering

By

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Abstract

Electronic flip chip assemblies consist of dissimilar component materials, which exhibit different CTE. Under thermal cyclic operating conditions, this CTE mismatch produces interfacial and interconnect stresses, which are highly dependent on system layout. In this paper, sensitivity analyses are performed using ANSYS FEA to establish how the proximity and arrangement of neighboring devices affect interconnect stress. Flip chip alignment modes ranging from edge-to-edge to corner-to-corner are studied. Results of these FEA studies, demonstrated that closely packing devices together has the effect of making them act as one. This results in a significant increase in the thermomechanical stresses induced on peripheral solder joints, heightening reliability risk. The sensitivity subsides gradually as device spacing increases, and eventually stops being a factor. 6mm is the threshold separation at which this occurs, in both edge-edge and corner-corner placement, for the system under analysis in this paper. Understanding the effect of system layout is instrumental for optimizing system design and improving reliability of power modules to meet the increasing power density needs.

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Introduction

1.1. Background of Flip Chip Technology

The ongoing trend of miniaturization and increased power density in power electronics has driven the growth of flip chip technology. Flip chip, also known as Controlled Collapsible Chip Connection (C4), describes a method of electrically and mechanically connecting the semiconductor die to the package substrate. Solder bumps are deposited on the die and the die is flipped over to align the solder with contact pads on the substrate. The bonding is then completed by reflowing the solder joints in a thermal oven [1-2]. Figure 1 below is an illustration of a simple flip chip package.

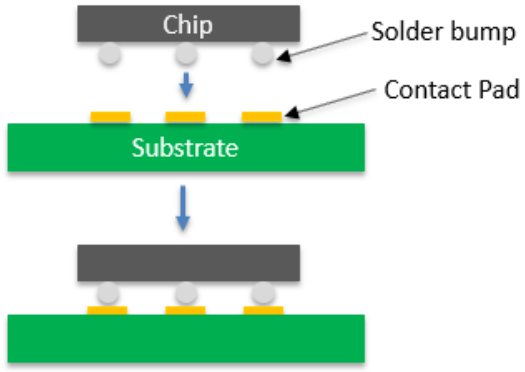


Figure 1. *Front view of a flip chip attachment*

Flip chip technology provides several advantages. Flip chip packages do not have the periphery limitations associated with wire bonding. The entire area under the chip can be utilized for input/output (I/O) connections, and devices can be moved closer together resulting in higher packaging density. The signal path between the die and the package is also minimized enabling better electrical performance [3].

Another major advantage of flip chip technology is 3D architecture. It provides the ability to stack chips or even heat removal devices, where wire bonds are limiting. However, these advantages add complexity to understanding and predicting the reliability of the packaging.

1.2. Flip Chip Reliability

Flip chip technology has enabled the development of power modules with increasing power capability, high current and high voltage resulting in significant power dissipations. This self-heating coupled with environmental conditions give rise to wide operating temperatures for flip chip packaging modules. In electric vehicle applications, for example, power modules are subjected to operating temperatures that can exceed 150^{o}C when the car is running, or fall below 0^{o}C when the car is stationary in cold weather conditions [4 - 5].

These thermal fluctuations represent a significant reliability risk for flip chip devices. Flip chip assemblies consist of dissimilar materials that have Coefficient of Thermal Expansion (CTE) mismatch. The organic substrates, on which flip chips are mounted to capitalize on their lower processing cost and lower dielectric constant, have much higher CTE (CTE $\geq$ 40 ppm/^{0}C) compared to that of the die (CTE $\approx$ 3ppm/^{0}C). Because of the CTE mismatch, layers of the flip chip expand and contract at different rates when temperature changes. This causes warpage and induces stress on interconnects and interfaces within the flip chip package [6].

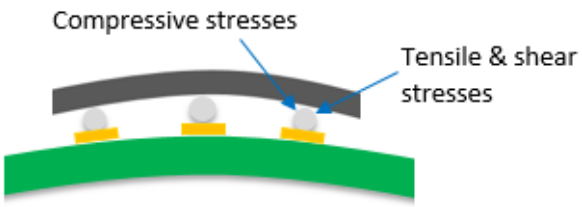


Figure 2. *CTE Mismatch stress induced by expansion in thermal conditions*

Previous studies have shown that solder interconnects represent significant reliability risk from the induced stress because of thermomechanical fatigue. With continued thermal cycling, inelastic strains and cumulative fatigue damage develop in the solder joints, leading to crack formation, propagation and, ultimately, causing device failure. The failure of solder interconnects in electronic modules under conditions of thermomechanical fatigue is well-documented [10-15]. In order to mitigate solder fatigue and improve package reliability, it is essential to understand how variables such as flip chip device geometry, material composition, and layout of neighboring devices affect thermomechanical stresses on the interconnects. Several works have looked at the impact of device geometry as well as material [16, 17], but there is still a lack of understanding on the impact of system layout. The focus of this research is to study the influence of proximity and arrangement of adjacent flip chip devices on solder stress in order to optimize system layout for reliability.

Approach

The objective of this approach is to investigate the impact of flip chip device layout on thermomechanical stresses that drive reliability failures in solder joints. Finite Element Analyses (FEA) using ANSYS® 17.1 is conducted to determine solder interconnect stress as a function of proximity for various placement modes of neighboring devices.

In this effort, the analyses are evaluated at a steady-state temperature profile, and the entire module is assumed to be isothermal. Concurrent FEM studies, conducted by Arie Smith, on the fatigue mechanisms of solder interconnects have shown that worst-case cold side exposure (-55 ^{o}C) drives the highest stress and reliability risk in solder interconnects (Appendix C, figure 15). Therefore, the layout studies were carried out at -55^{o}C, where the effects of system layout are accentuated, because of the high stresses. The stress-free reference temperature in the analysis is defined as the reflow (or melting) temperature of the solder, for which the value is 188^{o}C for 60/40 SnPb.

For the propose of the FEA simulations, a simplified flip chip device is used, taking advantage of symmetry to reduce computational time. The single device consists of a Silicon Carbide (SiC) die, 60/40 Tin-Lead (SnPb) solder, and FR-4 30% Glass filled Epoxy substrate. The dimensions of the full-sized device as well as an image of a quarter-symmetric model of the device are shown below:

- SiC chip: 10 x 10mm, thickness - 0.235mm
- 60/40 SnPb Solder bumps: 0.23mm diameter, (10 x 10)
- FR-4 Substrate: 30 x 30mm, thickness – 0.635mm

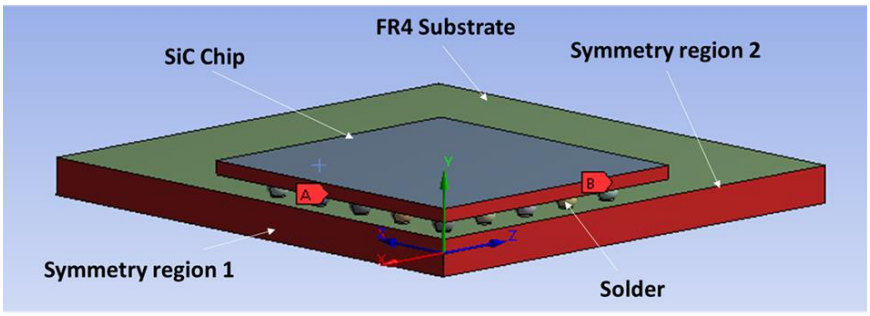


Figure 3*. Quarter-symmetric Flip chip model*

The layout sensitivity analyses are performed for three different device placement modes, the first one being at zero-degree parallel placement (edge-edge), and the second one at 45-degree rotated alignment (corner-corner). The final placement mode combined the previous two for an edge-corner layout. Figure 4 below provides an illustration of these placement modes. For edge-edge and corner-corner arrangement, the flip chip devices were mirrored through the use of planes. This then enabled the variation of device separation by changing the distance from the chip to the mirror plane. Proximity was varied from 0.1mm to the full length of the die at 10mm.

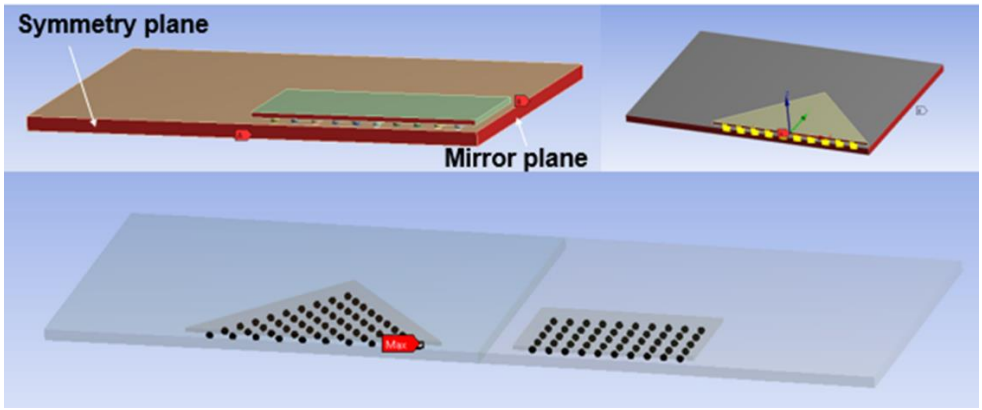


Figure 4*. From top left, edge-edge model, corner-corner model, and corner-edge model*

The thermal structural analyses in ANSYS Mechanical require that properties be defined for each material within the flip chip Assembly. The thermal aspect of the analysis requires, at minimum, that the Thermal Coefficient of expansion (CTE) of each material be defined. The structural analysis, on the other hand, requires a young's modulus as well as Poisson's ratio. The materials of the simple flip chip used in our modeling fall into two categories: isotropic and orthotropic. The latter refers to materials whose properties vary in magnitude depending on the direction of measurement, whereas the former refers to materials with uniform properties in all directions. The SiC die and 60/40 SnPb solder fall into the isotropic category whereas FR-4 belongs to the orthotropic class. The nature of FR-4 as a composite material composed of woven fiberglass and epoxy resin gives rise to this variation in properties in different directions. A compilation of the material properties at -55^{o}C is provided in table 1.

Table 1. *Material Properties at -55 ^{o}C [18]*

Material	CTE (C^{-1})	Young's Modulus, E (MPa)	Poisson's Ratio
SiC	4.00E-06	113500	0.14
60/40 SnPb	2.50E-05	34470	0.316
FR-4	X 1.30E-05	X 22604	XY 0.02
	Y 1.30E-05	Y 22604	YZ 0.143
	Z 7.00E-05	Z 6458	XZ 0.143

Other key elements that had to be incorporated in our models were displacement constraints. These were applied to get a statically determinate half-symmetry model, that is, there are no more constraints than would be required to prevent rigid-body motion (than would be required to keep the stiffness matrix non-singular).

2.1 Modelling Solder Joints

2.1.1 Singularities

In modelling solder interconnects, two major challenges were encountered, the first being singularities. A singularity prevents convergence of stress results as mesh size is refined for accuracy. The stress keeps increasing to infinity, because it is acting in a region with zero-surface area. With regard to the solder bump, the singularity occurs at the infinitely sharp re-entrant edge shown below.

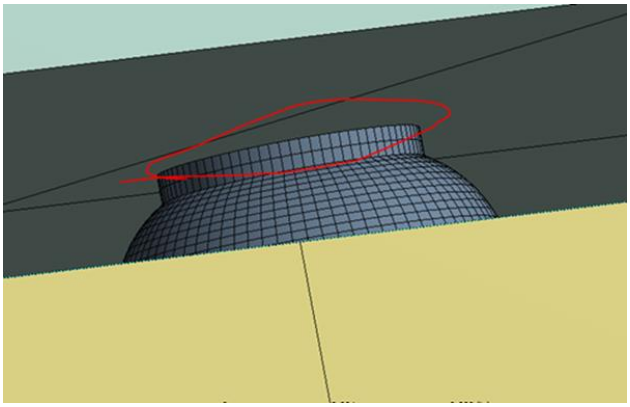


***Figure 5**. Singularity*

There are several plasticity models that can be used to account for singularities. When an external load is applied to a part in FEA, the internal strain is the dependent variable. Displacement is the primary variable that ANSYS solves for, and the strain is the first spatial derivative of that. Without plasticity models, the stress is linearly proportional to the strain resulting in the boundless increase observed at a singularity. If, instead of a linear constitutive law, an actual stress-strain curve (from a tensile test, for example) is defined, an upper limit can be placed on the stress response at a singularity. In principle, a singularity still exists, but the stress reaction increases far more slowly with mesh refinement. So slowly, in fact, that the stress values converge. A 1%

convergence may not be achieved, but 4% is feasible. In ANSYS, the stress-strain curve is defined for the solder bump using plasticity models, for which several are available to choose from.

The stress converges, but not the strain. This is acceptable as long as the strain remains under the ultimate strain limit. Furthermore, the strain response can be prevented from increasing without bound by turning on 'Large Deflection' effects in ANSYS under analysis settings (Figure 11 in Appendix A). This allows the highly stressed region to relieve itself by updating the deformed geometry. This practice is common in the electronics packaging industry.

2.1.2 Creep Behavior

The stress-strain behavior of solder is very complex. It is both temperature dependent and rate dependent. This time-dependent inelastic deformation is known as visco-plasticity or creep. Solder material typically have low melting temperatures, and as result operate at high homologous temperatures. Homologous temperature being the ratio of the operating temperature to the melting temperature of the solder in absolute degrees ($T_H = T_o/T_m$). Assuming a range of -55°C to 150°C for operating conditions, 60/40 SnPb solder, which melts at 188°C, would have T_H between 0.47 and 0.92. Metallic materials generally experience creep as the dominant form of deformation at $T_H > 0.4$ [7]. That means that even at the worst-case cold side temperature (-55°C), 60/40 SnPb solder would still exhibit considerable creep. Therefore, it is imperative to model solder as a rate and temperature-dependent visco-plastic material.

2.2 Anand's Viscoplasticity Model

Anand's Model [19] is an example of a visco-plasticity model that accounts for singularities as well as creep deformation of solder interconnects. As mentioned above, solder material exhibit two types of inelastic deformation: time-independent or plastic, and time-dependent or creep. Anand differentiates between elastic and inelastic strain, but unifies the two forms of inelastic behavior into a single inelastic term. The term is expressed in terms of internal state variables [8]. Anand's model relies on two equations; a flow equation and an evolution equation, to model this deformation behavior of solder [8].

Flow Equation

$$\dot{\varepsilon}_{in} = Ae^{\frac{-Q}{RT}}\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \qquad (1)$$

Evolution Equation

$$\dot{s} = \left\{h_o(|B|)^a \frac{B}{|B|}\right\}\dot{\varepsilon}_{in} \qquad (2)$$

Where

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_{in}}{A}e^{\frac{Q}{RT}}\right]^n$$

And

$$B = 1 - \frac{s}{s^*}$$

The $\dot{\varepsilon}_{in}$ is the inelastic strain rate and is the sum of time-dependent plastic strain rates and creep. The first part of the flow equation is an Arrhenius' Law-type term, which accounts for the dependence of the creep process on temperature. The hyperbolic sine term in the second part of the equation describes the stress dependence of the inelastic strain rate; the state variable is

included in this term. When it comes to solder behavior, the evolution equation mainly looks at the strain hardening effect through the hardening coefficient h_o[9].

Using the Anand model in ANSYS requires that all nine constants of the flow and evolution equations be inputted for the solder material. The constants are determined experimentally through creep testing. For 60/40 Sn-Pb, the material constants have been measured experimentally and documented in previous papers [18]. The table below contains the definitions of the constants as well as their corresponding values for 60/40 Sn-Pb.

***Table 2**. Anand's model constants for the solder material*

Parameter	Description	Units	60/40 SnPb
So	Initial value of deformation resistance	Stress (Pa, psi)	56.33
Q/R	Activation energy divided by universal gas constant	energy/volume (kJ/mole)	10830
A	Pre-exponential factor	1/time (1/S)	1.49E+07
ξ	Multiplier of stress	dimensionless	11
m	Strain rate sensitivity of stress	dimensionless	0.303
ho	Hardening/softening constant	Stress (Pa, psi)	2640.8
$\hat{s}$	Coefficient for saturation value of deformation resistance	Stress (Pa, psi)	80.42
n	Strain rate sensitivity of saturation value (deformation resistance)	dimensionless	0.0231
a	Strain rate sensitivity of hardening or softening	dimensionless a>1	1.34

*The procedure used to run the ANSYS analyses is outlined in Appendix A.

Results

The impact of neighboring devices on solder interconnect stress for edge-edge placement at 1mm spacing is demonstrated in Figure 6. The stress profile is for peripheral solder joints along half the device for 1 mm edge-edge separation. The solder bumps lining the mirrored edge and free edge are ordered in the direction of the arrows shown in figure 6a.

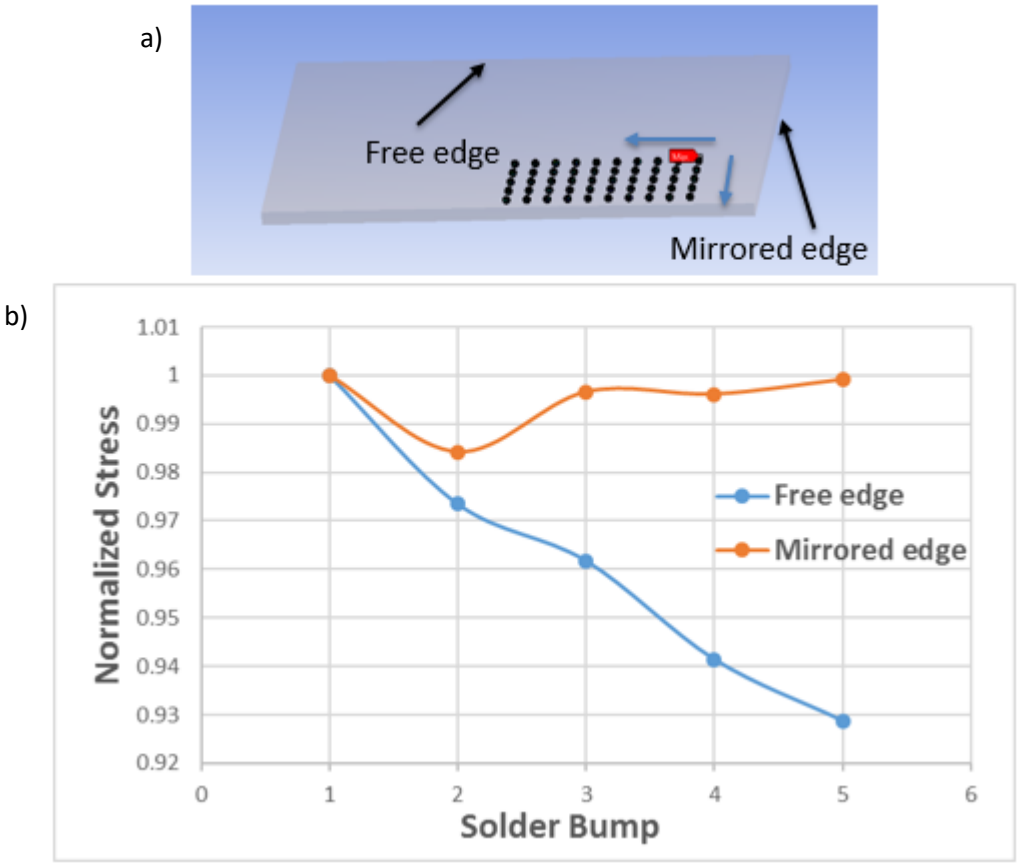


Figure 6. *(a) Edge-edge model (b) Peripheral Solder Stress profile for 1 mm separation*

Figures 7 illustrates results for peripheral solders in corner-corner placement at the same separation distance of 1mm.

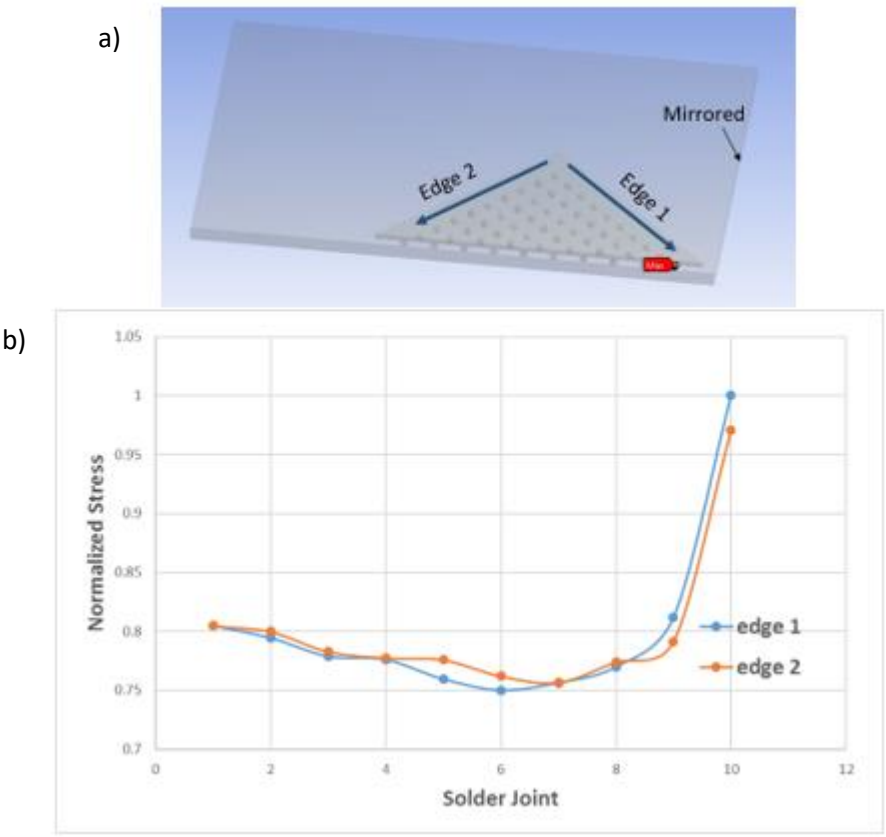
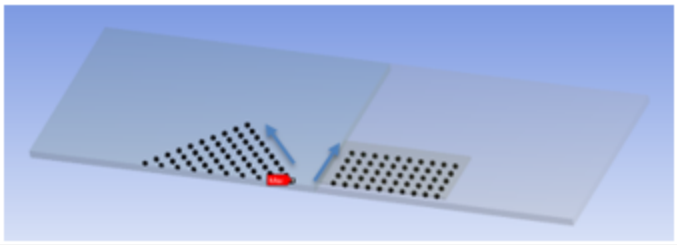


Figure 7. *(a) Corner-corner model (b) Peripheral Solder Stress profile for 1 mm separation*

Results in figures 6 and 7 show that thermomechanical stresses on solder interconnects are sensitive to neighboring devices. Both charts indicate that solder interconnects lining the mirrored edge experience higher stress than those lining the free edge. In particular, the corner solder joints, which are highlighted in figure 6a and 7a, experience the highest stress and, as a consequence, represent the highest reliability risk.

Figure 8 illustrates peripheral solder stress profile for edge-corner placement at 1mm spacing.

a)



b)

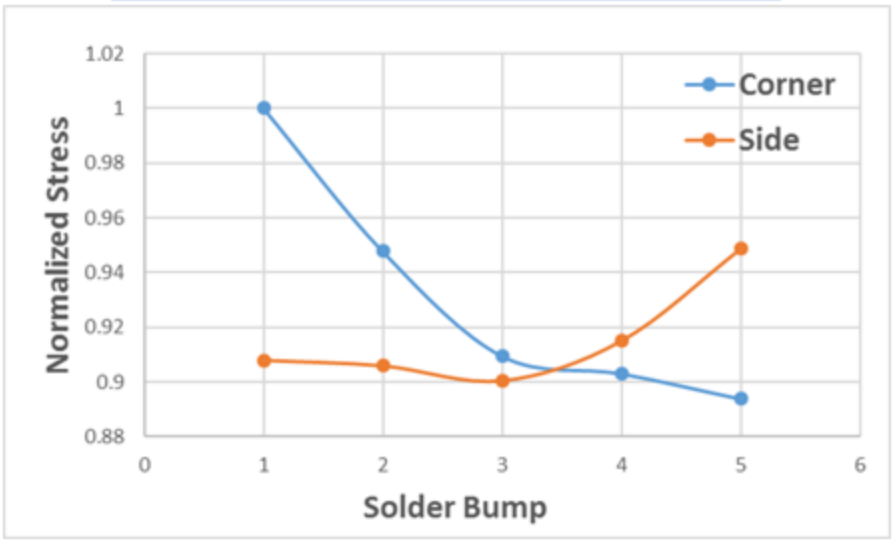


Figure 8*. (a) Edge-corner model (b) Peripheral solder stress for edge-corner at 1mm spacing*

From figure 8, it can be observed that corner alignment sees the most stress, particularly the corner solder joint (highlighted in red in figure 8a), furthest from the center of the package. However, for corner alignment, the stress decreases considerably as you move further away from the corner in the direction of the arrow in figure 8a. As for edge alignment, stress behavior is consistent with the trend observed in figure 6; peak stress occurs on solder joint furthest from the center of the package.

Figure 9 is a plot of peak solder stress as a function of proximity for corner-corner and edge-edge placement.

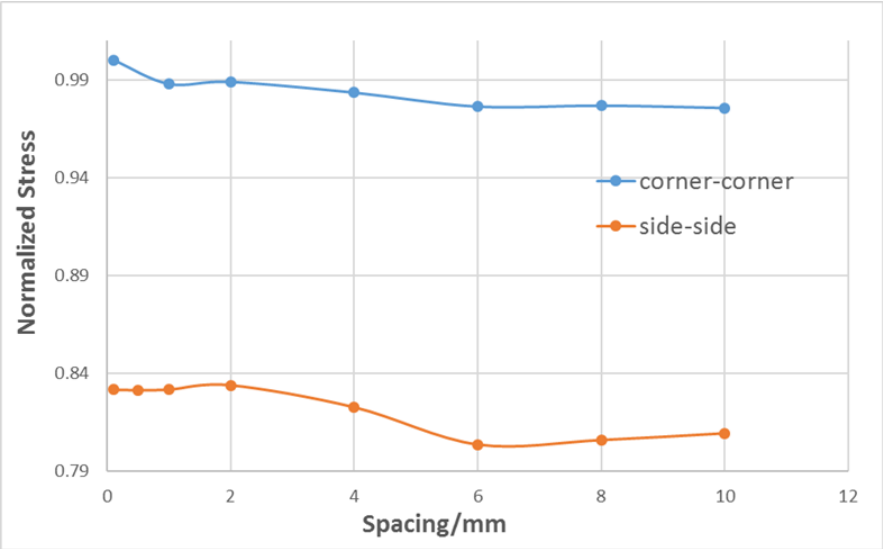


***Figure 9**. Max solder stress vs. spacing for edge-edge and corner-corner placement*

Results in figure 9 demonstrate that corner-corner placement drives the highest stress and reliability risk. Furthermore, both curves in figure 9 have an asymptote indicating that mechanical stress sensitivity between solder joints of neighboring devices stops being a factor at roughly 6mm spacing.

The fluctuations in the results are a result of convergence issues. Convergence was around 5-10%, which is not adequate for the stress analyses in this experiment. A lower allowable change was not possible because of limited computing power at the time of running the simulations. However, collected data still show useful trends that can inform system layout for reliability. Additional placement modes will need to be studied to fully understand and optimize for layout sensitivity. Parallel alignment from 0-45 degree location and rotated alignment from 0-45 degree location are examples of other possible placement modes. The effects of the substrates' stiffness

(that is thickness and young's modulus) should also be investigated, since the stresses are transferred through the substrate. Additionally, understanding behavior under transient temperature conditions will also be an area of interest.

Conclusions

Arrangement combined with proximity of neighboring devices result in variations of interconnect stress as well as the risk to failure, particularly on the peripheral solder joints lining adjacent edges of neighboring devices. Closely packing devices together has the effect of making the devices act as one. This has a considerable upward effect on the thermomechanical stresses induced on peripheral solder joints, heightening reliability risk. The sensitivity subsides gradually with increasing device spacing, and eventually stops being a factor. For the system under analysis in this paper, 6 mm is the minimum separation at which this occurs in both edge-edge and corner-corner placement. Results showed that the corner solder joint, furthest from the center of the package, in 45-degree rotated alignment (corner) experiences the highest stress and reliability risk.

This work is part of a project whose goal is to enable the prediction of reliability using FEA based on operating temperatures, material, and device/system layout in order to co-optimize power electronic system design for reliability and power density. In this effort, the FEA stress data will be correlated to experimental stress testing on test coupons and prototype modules. These experimental tests will provide empirical stress-based failure rates, which combined with the FEA stress states for different system designs, will provide a stress-based model for predicting reliability of power modules.

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Appendix A
Simulation Procedure

The analyses were performed using ANSYS 17.1 Mechanical. The simulation procedure was as follows:

1. Launch ANSYS Workbench
2. In the toolbox, locate and double click on Static Structural to insert a new analysis
3. In the new Static Structural Analysis, right click on the geometry cell and import geometry. SolidWorks model can be imported if saved as a STEP file
4. Double click on the Engineering data cell to input material properties from table 1
    a. Select Anand from the list of plasticity models
    b. Enter the Anand constants illustrated in table 2
5. Return to project homepage, and click on the model cell to open the Mechanical editor
6. In Mechanical editor, assign materials to each part and specify a stress-free reference temperature for each body. This corresponds to the melting temperature of the solder material (188^{o}C for 60/40 SnPb)
7. If taking advantage of symmetry, right-click the geometry branch to add symmetry regions
8. On the mesh feature, ensure that mechanical mesh is selected
9. Right click the static structural branch to add:
    a. Temperature load (-55^{o}C) and specify time steps
    b. Add displacement constraints. The model should be constrained from rotating
10. Right click the solution branch to insert result objects such as Max von Mises Stress, Strain energy and deformation

11. Right-click on a result object to inset a convergence criteria
    a. In the convergence detail, enter an allowable change depending on the level of accuracy required
12. Select the solution branch and increase the number of allowable refinement loops form default value, which is set at one. This enables adaptive meshing iterations
13. Click on Analysis settings branch
    a. Activate large deflection to prevent boundless increase of strain on the solder joints (figure 11)
    b. Change solver type to Iterative to speed up the solution as refinement loops increase mesh size
14. Solve the model

*To vary distance to the mirror plane, the parts were modified in design modeler with the help of the extrude feature

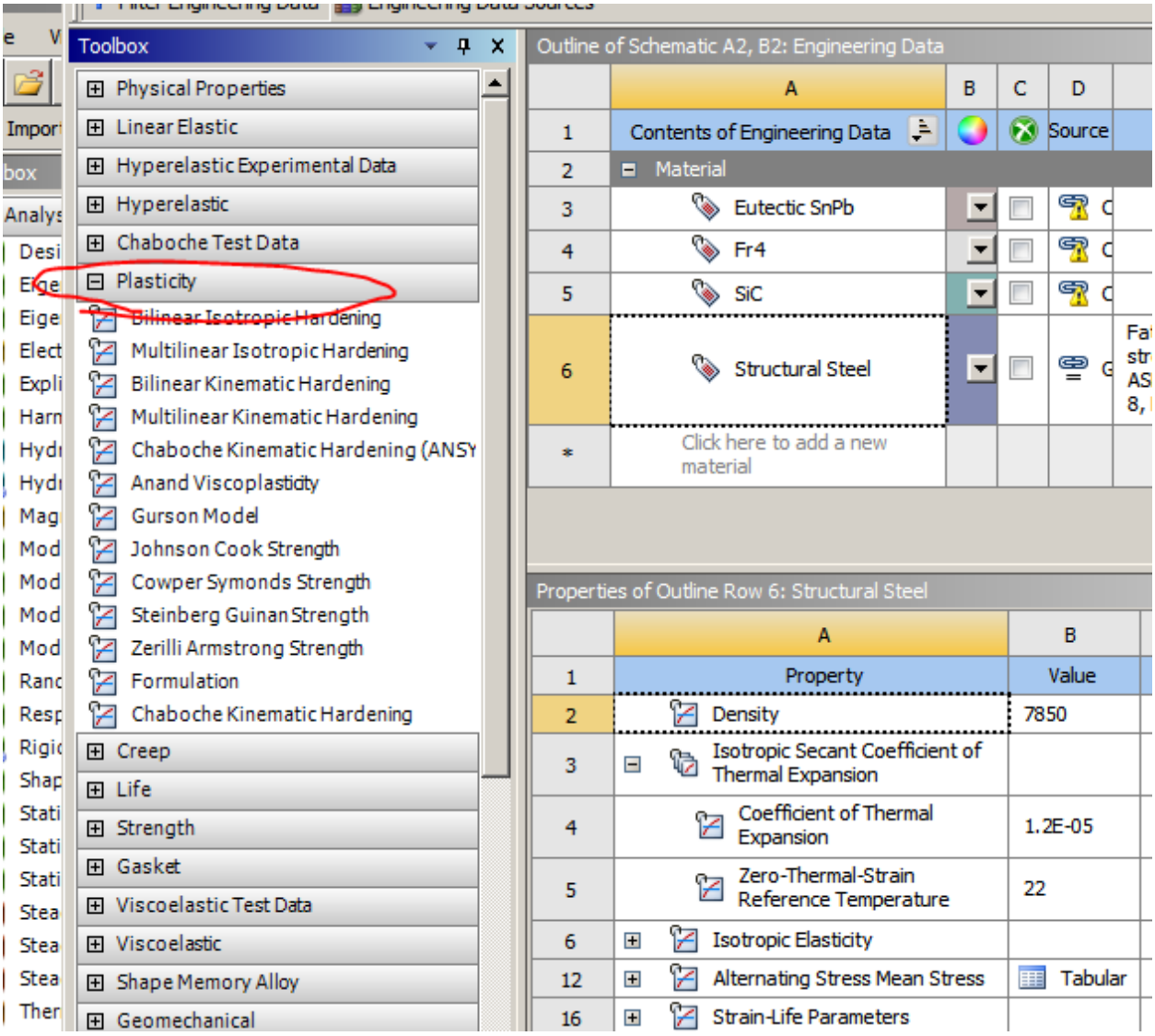

Figure 10. *ANSYS Plasticity models*

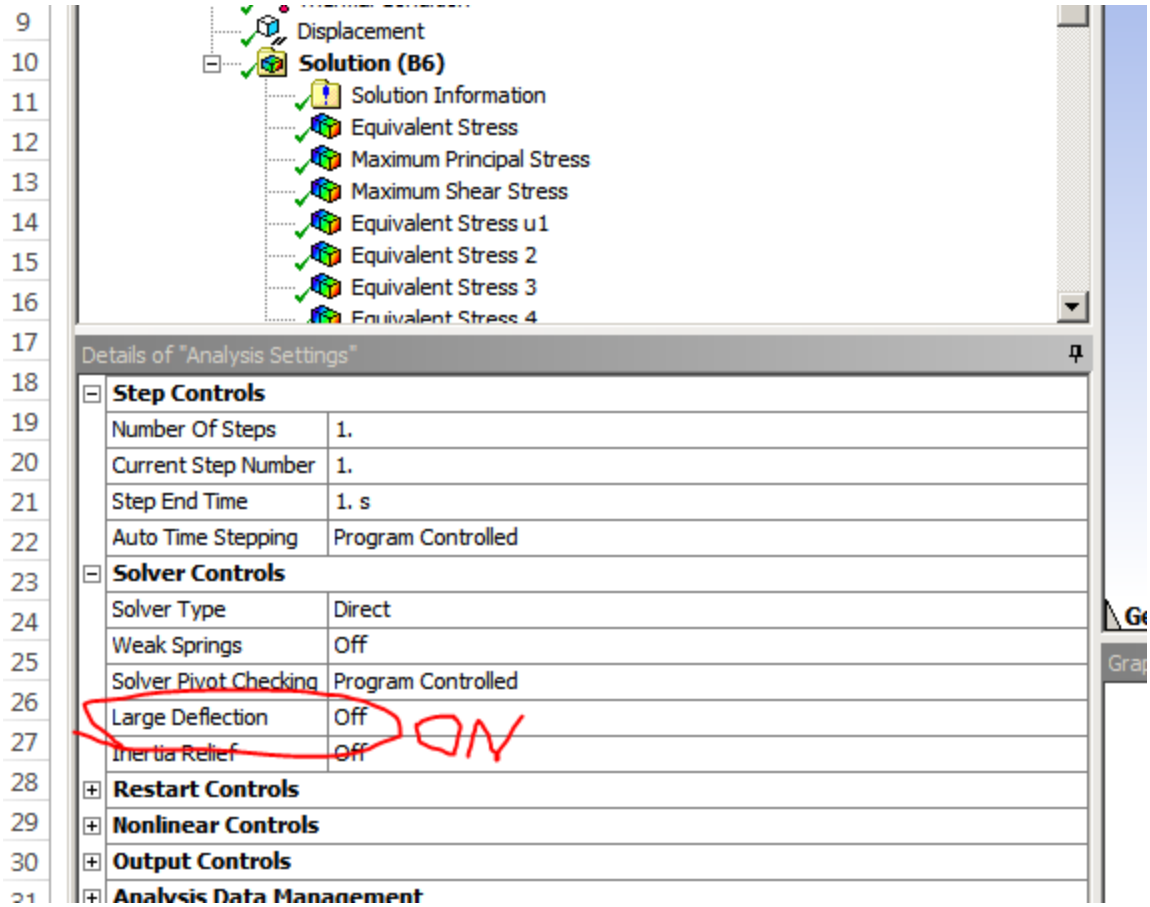

Figure 11. *ANSYS Large Deflection feature*

Appendix B

Raw data

Table 3. *Corner-corner data*

# 04/04/2017 23:38:07						
# The parameters defined in the project are:						
#	P1 - Extru	P2 - Equiv	P3 - Equiv	P4 - Strain	P5 - Equiv	P6 - Equivalent Stress 4 Maximum [MPa]
#						
# The following header line defines the name of the columns by reference to the parameters.						
Name	P1	P2	P3	P4	P5	P6
DP 0	0.05	128.5776	94.12112	6.28E-05	94.12112	90.42891
DP 1	0.5	129.3392	92.97201	6.16E-05	92.97201	90.24223
DP 2	1	130.4823	93.06643	6.17E-05	93.06643	89.92102
DP 3	2	129.854	92.55281	6.14E-05	92.55281	90.01887
DP 4	3	129.3624	91.88613	6.22E-05	91.88613	90.0917
DP 5	4	129.4803	91.93232	6.29E-05	91.93232	90.06051
DP 6	5	130.5494	91.81896	6.28E-05	91.81896	89.56138
DP 7	6	130.0764	91.85539	6.13E-05	91.85539	90.30582

Table 4*. Edge – edge data*

# 04/05/2017 01:04:01						
# The parameters defined in the project are:						
#	P10 - Extru	P5 - Equiv	P6 - Equiv	P7 - Equiv	P8 - Equiv	P9 - Strain Energy Maximum Maximum Value Over Time [mJ]
#						
# The following header line defines the name of the columns by reference to the parameters.						
Name	P10	P5	P6	P7	P8	P9
DP 0	0.05	78.51965	119.8865	78.27162	77.10787	8.01E-05
DP 1	0.25	78.58443	120.3474	78.25181	77.34028	8.00E-05
DP 2	0.5	78.43825	120.2726	78.27879	77.24013	8.04E-05
DP 3	1	79.00829	120.1728	78.48701	77.5388	8.11E-05
DP 4	2	77.42922	117.6689	77.42922	76.43641	8.01E-05
DP 5	3	75.62765	115.0934	75.62765	74.00674	7.32E-05
DP 6	4	75.84599	115.201	75.84599	74.00357	7.37E-05
DP 7	5	76.17182	115.5902	76.17182	74.03174	7.56E-05
DP 8	6	78.13243	119.0887	78.13243	77.21689	7.91E-05

Table 5. *Corner-edge data*

# 04/05/2017 10:34:21								
# The parameters defined in the project are:								
#	P1 - Equival	P2 - Equivale	P3 - Equivale	P4 - Equivale	P5 - Strain En	P6 - Equivalen	P7 - Equivalen	P8 - Equivalent Stress 7 Maximum [MPa]
#								
# The following header line defines the name of the columns by reference to the parameters.								
Name	P1	P2	P3	P4	P5	P6	P7	P8
0.1	113.638191	82.1375969	82.1375969	72.4696044	7.00E-05	76.54036856	75.79756506	73.06696135
0.25	113.933433	80.8044845	80.8044845	72.3484609	7.05E-05	76.89330326	76.09039533	73.09153712
0.5	116.442393	81.9945571	81.9945571	74.7977321	8.33E-05	78.75962352	77.58223439	74.39563393
1	113.394729	82.4530973	82.4530973	74.7746132	8.43973E-05	79.20769203	78.06529531	75.50410845
2	116.263113	82.310607	82.310607	74.64185	8.28E-05	79.63228591	77.36293634	74.77407171
3	114.216866	82.7722279	82.7722279	74.8440083	8.0148E-05	79.37304265	78.11215011	75.234786
4	112.093046	82.0848787	82.0166001	71.714662	7.93E-05	79.01857496	77.39982463	75.03843332
5	110.348586	82.9217534	82.9217534	72.7029149	8.18197E-05	79.56998248	77.83729388	75.58626381

Appendix C

Peak stress on Solder

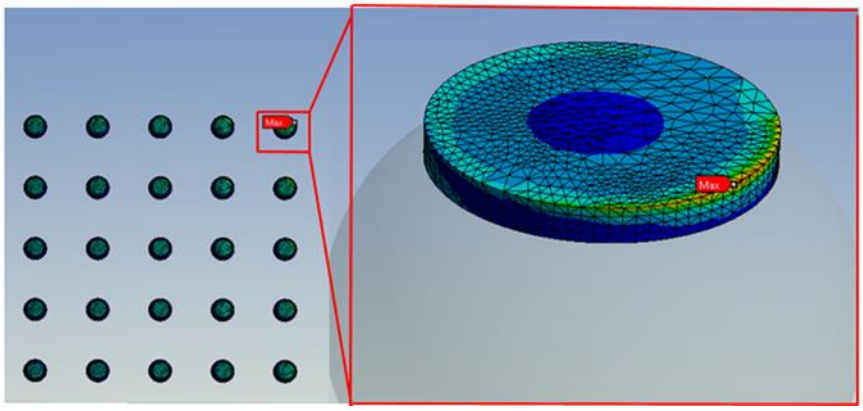

Figure 12. *Peak stress location (By Arie Smith)*

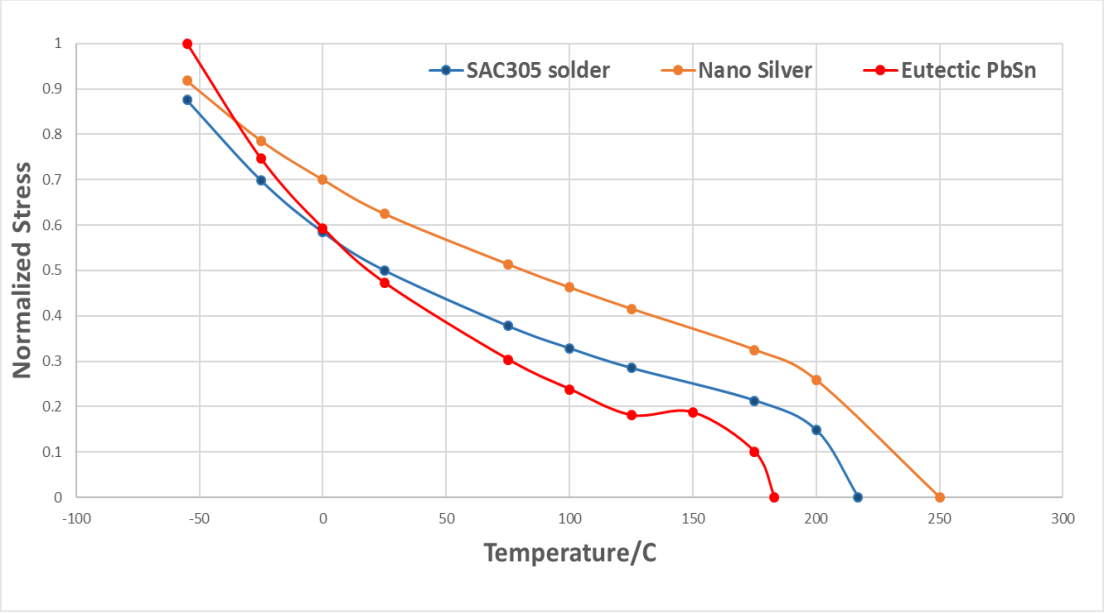

Figure 13. *Normalized stress vs Temp for different Solder Material (By Arie Smith)*

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