University of Arkansas, Fayetteville
ScholarWorks@UARK

Theses and Dissertations

8-2016

Compact Modeling of SiC Insulated Gate Bipolar Transistors

Sonia Perez
University of Arkansas, Fayetteville

Follow this and additional works at: http://scholarworks.uark.edu/etd

 Part of the Electronic Devices and Semiconductor Manufacturing Commons, and the VLSI and Circuits, Embedded and Hardware Systems Commons

Recommended Citation
Perez, Sonia, "Compact Modeling of SiC Insulated Gate Bipolar Transistors" (2016). *Theses and Dissertations*. 1708.
http://scholarworks.uark.edu/etd/1708

This Thesis is brought to you for free and open access by ScholarWorks@UARK. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of ScholarWorks@UARK. For more information, please contact scholar@uark.edu, ccmiddle@uark.edu.

Compact Modeling of SiC Insulated Gate Bipolar Transistors

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Microelectronics-Photonics

by

Sonia Perez
Henderson State University
Bachelor of Science in Physics, 2008

August 2016
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

Dr. H. Alan Mantooth
Thesis Director

Adjunct Professor Tom Vrotsos
Committee Member

Dr. Anthony Matt Francis
Committee Member

Dr. Greg Salamo
Committee Member

Dr. Rick Wise
Ex-Officio Member

The following signatories attest that all software used in this thesis was legally licensed for use by Sonia Perez for research purposes and publication.

_____	_____
Ms. Sonia Perez, Student	Dr. H. Alan Mantooth, Thesis Director

This thesis was submitted to http://www.turnitin.com for plagiarism review by the TurnItIn company's software. The signatories have examined the report on this thesis that was returned by TurnItIn and attest that, in their opinion, the items highlighted by the software are incidental to common usage and are not plagiarized material.

_____	_____
Dr. Rick Wise, Program Director	Dr. H. Alan Mantooth, Thesis Director

Abstract

This thesis presents a unified (n-channel and p-channel) silicon/silicon carbide Insulated Gate Bipolar Transistor (IGBT) compact model in both MAST and Verilog-A formats. Initially, the existing MAST model mobility equations were updated using recently referenced silicon carbide (SiC) data. The updated MAST model was then verified for each device tested. Specifically, the updated MAST model was verified for the following IGBT devices and operation temperatures: n-channel silicon at 25 ˚C and at 125 ˚C; n-channel SiC at 25 ˚C and at 175 ˚C; and p-channel SiC at 150 ˚C and at 250 ˚C. Verification was performed through capacitance, DC output characteristics, and turn-off transient simulations. The validated MAST model was then translated into the Verilog-A language, and the Verilog-A model results were validated against the updated MAST model.

Acknowledgements

I would like to thank Dr. Matt Francis, Tom Vrotsos, Ramchandra Kotecha, Staci Brooks, Dr. Rick Wise, and Dr. Alan Mantooth for their time, patience, and knowledge throughout my education. I would not have gained this incredible amount of knowledge, perspective, and confidence without you all. I would also like to thank my family for supporting me throughout the extended time it took me to complete this work. I would also like to acknowledge Dr. Seuss' inspirational quotes from the beloved book "O the Places You'll Go."

This program is financially supported by the National Science Foundation under Grant No. DUE-0728636. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author and do not necessarily reflect the views of the National Science Foundation.

Dedication

This thesis is dedicated to Kathy Kirk, Dr. Pam Mathews, Gordon Pearson, Tom Vrotsos, and my parents for their continued support throughout my journey to complete this degree.

Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

The focus of this thesis is on maturing and verifying a compact semiconductor device model to be utilized within circuit designs. The device discussed is a 4H silicon carbide (SiC) Insulated Gate Bipolar Transistor (IGBT). Therefore, when SiC is mentioned within this thesis it is referring to the 4H-SiC polytype. Initially, an overview of why SiC IGBTs are of interest, what a compact model is, and what other IGBT models exist in the field is discussed. Once these topics have been introduced to the reader, a detailed description of the following will be presented: the operation of an IGBT, the Unified IGBT model, the core changes to produce the current model, the results from the current model, and the possible future work to further update this silicon/SiC IGBT model.

1.1 SiC IGBT Impact on the Power Electronic Industry

Silicon (Si) based electronics have propelled technology to the mobile and high power world we live in today. Insulated Gate Bipolar Transistors (IGBTs) are well utilized within power electronics applications due to their ability to provide high blocking voltage capability, with the advantage of a voltage-controlled gate. The highest known Si IGBT breakdown voltage is 6.5 kV and only operates up to 200 ˚C [1]. Although well above the average requirements for most printed circuit board applications, this device is not capable of withstanding extreme environment conditions of aeronautical and automotive applications that frequently exceed 200 ˚C. With the addition of SiC IGBTs underway, the next generation technology of high power and thermally efficient applications are being developed.

Intrinsic carrier concentration, thermal conductivity, and critical electric field are all material properties of SiC that provide spatial and performance improvements over Si

semiconductor devices. The lower intrinsic carrier concentration of SiC gives these devices the ability to operate in higher ambient temperatures than Si devices. The higher thermal conductivity of SiC, compared to Si, allows devices to operate during rapid temperature changes. Both thermal conductivity and intrinsic carrier concentration reduce the reliance on cooling systems to remove excess heat from the device to avoid destructive temperature effects. Without cooling systems, solely in place for continuous operation in Si devices, the size of these completed SiC devices is significantly reduced. The critical electric field of SiC is larger than that of Si. This material property allows vertical devices to be produced with thinner widths (or thinner base regions in terms of IGBTs) for the same blocking voltage capabilities [2]. Generally, a device designed with a thinner base region allows for more cells to be produced in the same x-y dimensions, resulting in a smaller device. These material advantages give SiC devices the ability to impact the power electronics industry through the miniaturization of electronics.

SiC devices possess the ability to switch at higher frequencies than their silicon counterpart. A device designed to switch at higher frequencies requires physically smaller passive components in the surrounding circuitry. Therefore, the footprint of the switching circuit will be reduced with a SiC device. Also, a device switching at higher frequencies requires passive components to be coupled closer to the device, further miniaturizing the switching circuit. As passive component values and interconnect path lengths are reduced, the closer the passive components are to semiconductor device; therefore, the passive components are now exposed to the same temperatures as the switching device. This presents an issue as there is a limited selection of passive components that are reliable over a wide range of temperatures [2]. In addition to the limited amount of passive components available, the size of these high temperature passives are undesirable as they combat the miniaturization effects of SiC devices.

However, SiC devices allow circuits to be designed and fabricated smaller than their silicon counterparts.

1.2 SiC Material Properties

An overview of how SiC impacts the performance of IGBTs and other similar semiconductor devices will be briefly reviewed. Table 1.1 shows a few of the superior material properties that SiC has compared to Si for developing high temperature devices [3]. The rest of this section will discuss how the intrinsic carrier concentration, band gap, and the thermal conductivity affect the higher thermal operation limit of SiC.

Table 1.1 Material Properties Affecting High Temperature Performance of SiC Devices

Properties	**Si**	**SiC**
Intrinsic carrier concentration 300 K (cm^{-3})	1.4 X 10^10	6.7 X 10^-11
Band gap (eV)	1.11	3.26
Thermal conductivity (W/m·K)	1.5	3.7

A low intrinsic carrier concentration, n_i, at room temperature allows SiC devices to operate at higher temperatures. (Within the Si/SiC IGBT model, the intrinsic carrier concentration is a model value and denoted as ni; therefore, from this point on the intrinsic carrier concentration will be referred to as ni.) The concentration of intrinsic carriers in a semiconductor material is directly proportional to the temperature; therefore, with an increase in temperature, ni increases. Figure 1.1 depicts a cross section of a silicon n-channel IGBT. For current to flow in this IGBT, the N+ source region requires a "connection" to the N- base region. Therefore, at room temperature, with no stimulus applied to the IGBT, current will not flow. However, as the temperature rises, electron-hole pairs are created within the semiconductor material, which increases the free electron concentration in the material. This decreases the

difference in the doping concentrations between the N+ source region and the P+ body region. This will eventually create a short, or "connection," between the N+ source region and the N- base region, with no external stimuli applied to the IGBT. Now, with any voltage applied to the collector, current will begin to flow through the device with little effort, regardless of the voltage applied at the gate. The lack of control at the gate renders this IGBT useless in any situation. This is a limit Si device designers must account for by adding large heat sinks and other cooling measures to keep the device under its theoretical temperature limit.

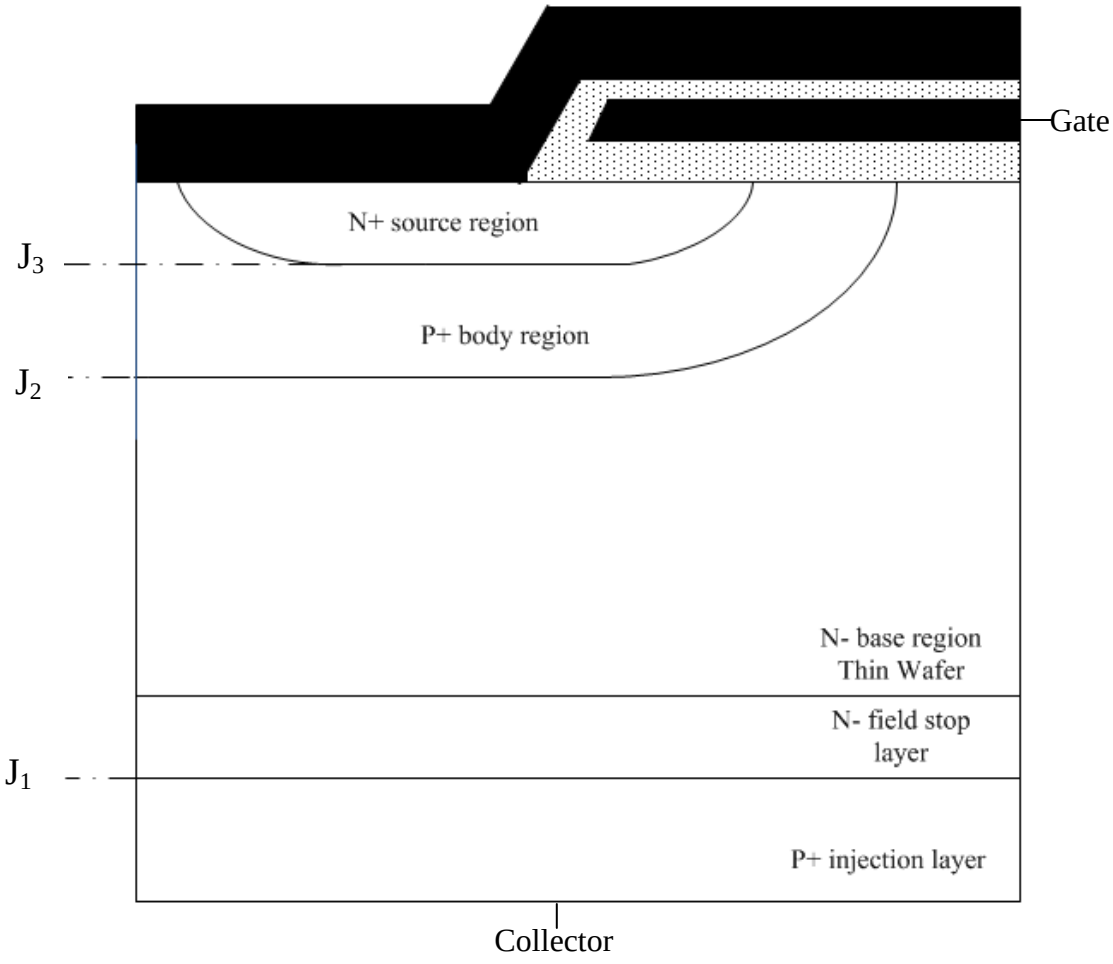


Figure 1.1 Cross section of an n-channel IGBT.

The upper temperature limit of most silicon semiconductor devices commercially available is 150 ˚C. Since the intrinsic carrier concentration in SiC starts at 20 orders of magnitude less than the intrinsic carrier concentration of Si at room temperature, this degenerative effect takes place at a much higher temperature in SiC devices. It has been shown, with the appropriate electronic packaging, SiC devices can operate higher than 400 ˚C [4]–[6].

Band gaps of semiconductor materials also affect the thermal operation limit in codependence with intrinsic carrier concentration, as the intrinsic carrier concentration of a material is proportional to its band gap. The larger the band gap, the more thermal energy is required for carriers to become thermally excited. Therefore, less intrinsic carriers are generated as the temperature rises. In other words, the large band gap correlates to the production of less intrinsic carriers at a given temperature, hence the co-dependence. As previously explained, with less intrinsic carriers, the device is able to operate at higher temperatures.

Thermal conductivity also relates to the operating temperatures of a semiconductor device. This property dictates how fast a material can dissipate heat. The lower the thermal conductivity, the longer it takes for heat to evenly distribute throughout the material. That is, it takes a silicon device longer to dissipate heat than its silicon carbide counterpart. Since SiC can dissipate heat at a faster rate, less bulky and inefficient hardware (i.e., heatsinks, fans, water-cooled systems, etc.) is required to cool the device. This allows devices to operate during rapid temperature changes without the hardware normally required, thereby increasing the reliability while simultaneously reducing the size and cost of SiC components needed for extreme environment conditions.

Not only does the high thermal conductivity of SiC benefit normal operation at high temperatures, this material property also enhances the ability of the device to operate under

continuous high current and high voltage conditions. All devices experience self-heating to some degree at extreme operation limits. Devices created with SiC can release the heat generated through self-heating faster than Si. This reduces the deleterious effect of self-heating which would be seen in the same Si device under the same conditions.

With the higher thermal conductivity of SiC, devices created from this material are able to operate under high temperature conditions without the dependency of cooling systems. The intrinsic carrier concentration, band gap, and thermal conductivity are all superior properties silicon carbide boasts over silicon. Devices created with SiC are able to withstand higher temperatures, endure rapid temperature changes, and require less cooling systems.

1.3 SiC IGBT State of the Art

IGBTs have been in production since the early 80s. Since their arrival in the industry they have added a great option for the medium frequency (5 -50 kHz) and for high voltage applications (.2 – 2 kV), opening up applications in industrial motor drives [7]. Now with the arrival of SiC Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) on the market, SiC IGBTs are the next most powerful SiC device to be developed. In the mean time, experimental devices are being developed and their impressive achievements are published in peer-reviewed conferences such as The International Symposium on Power Semiconductor Devices and ICs (ISPSD). In 2012, the results of both SiC n-channel and p-channel IGBTs were published. The p-channel SiC IGBT supported a 15 kV blocking voltage. The n-channel SiC IGBT supported a 12 kV blocking voltage [5]. Results of an n-channel IGBT were also published during 2013 and boasted an improved 20 kV blocking voltage [10]. Within the same year, the static and dynamic characterization of a 15 kV n-channel IGBT was reported. This characterization, at the time of publication, was the highest voltage switching characterization

performed on a single power semiconductor device at 11 kV [11]. The following year the results of a 22 kV n-channel device were published, proving to be the highest rated MOS-controlled device to that time [9]. In 2014, another p-channel IGBT was realized with a blocking voltage of 13 kV and showed static and dynamic results at 250 ˚C [12].

1.4 Compact Device Modeling

A compact model describes the electrical behavior of a circuit component under certain conditions, and is then utilized within a circuit simulator [13]. A finite element device model is one that is based upon semiconductor device physics. Designing a device model as a compact model has a number of benefits over finite element models. Finite element models contain equations to solve in two or three dimensions and are designed to compute every physical effect carriers encounter. Although extremely accurate, finite element models do not offer circuit designers the short simulation time to simulate numerous transistors in one circuit.

Compact models are focused on the terminal behavior of the device, rather than how a single electron traverses through the material. With this focus, compact models are only concerned with 1-D device simulation, drastically reducing the computation power required to simulate a device under specific conditions. This is ideal for circuit designers, since they are only concerned with the electrical behavior at each terminal. A compact model with a 1-D device simulation focus can rely on empirical equations. This allows flexibility within the compact model, adding accuracy without computationally expensive and time-consuming features. Also, compact models should employ easily extractable parameters. Easily extractable parameters allow the user to provide a device model to a circuit designer in less time.

The purpose of creating such device models is to provide a reliable prediction of how a specific device will behave under specific conditions, defined by circuit designers who utilize the

compact model in a simulator. Using a model to optimize the design of the physical circuit, engineers use this method to reduce the time to create a finished product. The most common simulators used by designers are SPICE based. However, SPICE based simulators, such as HSPICE and Spectre, accept specific languages, a point explained further in the following section and in Chapter 5. Providing a circuit designer with a compact device model first entails selecting the compact model to send. There are three options for selecting a compact device model: select an existing model, edit and update an existing model, or create a new model. Once a compact model is chosen, the following steps provide the remaining process to deliver a model that simulates the physical device characteristics of the transistor chosen:

1) measure a specific device requested in a circuit design project under various conditions (device characterization);
2) simulate the model under the same conditions (simulation);
3) overlay the measured data with the simulated data (fitting);
4) adjust the model parameters to produce a simulation that matches the measured device (model parameter extraction); and
5) provide the model and parameter set to circuit designers.

1.5 Published IGBT Models

Models were created and published shortly after the invention of IGBTs in the early 1980s. A list and review of all models prior to 1998 can be found in [14], and a summary of IGBT modeling challenges can be reviewed in [15]. The foundation of this model is based upon [16], therefore a description of the models following this author's career is presented.

Dr. Hefner has published a variety of models following advancements in the structural development of the IGBT. In 1994, he published his first Si IGBT model [16]. In 1995, a buffer

layer model was published, adding effects of a highly-doped buffer layer to the IGBT model [17]. Recently, a SiC Field Stop IGBT (FS IGBT) has been published. This model added SiC material properties as well as the slight variation in physics that the FS layer adds to the IGBT in comparison with the buffer layer model [18]. Although parameter extraction software for each of these models has been created [19], all of these models implement only n-channel IGBT physics.

Although n-channel IGBT devices and models are actively researched, there is a lack of interest in p-channel IGBT models. p-channel IGBTs pose an extremely positive impact in the power electronics field through the application of complementary circuits. A complementary circuit, for example, can be implemented within an inverter. The traditional inverter topology includes an n-channel IGBT referenced to the collector of another n-channel IGBT. The reference point in this topology is floating, as the collector of the second n-channel IGBT is not constant. The floating reference causes significant problems with gate control. This creates a complication while designing a gate controller for each IGBT included in the inverter topology. However, if the referenced IGBT was a p-channel IGBT, the reference point of the p-channel IGBT is the constant positive power supply. Creating a constant reference point greatly reduces the complexity of the gate driver circuit, and therefore the entire inverter topology. Including p-channel IGBT in designs that benefit from complementary circuitry can reduce the complexity of the design as well as reduce the overall components required.

Another problem with all of the aforementioned models is that they are implemented within the MAST language and the Saber Simulator®. While this simulator has been used for some time in the power electronics industry and for power device modeling, MAST based models are not the most commonly used among circuit designers, many of whom depend on more traditional SPICE-based simulators. Verilog-A, an analog description language based on

the digital Verilog standard, has become a *de facto* standard through the efforts of industry such as the Compact Model Council [13], and many SPICE simulators accept Verilog-A models as an input format. Any disconnect between device modelers and the circuit designers hinders the advancement of technology. Therefore, there is a need for compact device models that are in languages beneficial to the broadest base of circuit designers.

Other IGBT models have been developed that are not MAST based. In 2003, a FS IGBT model and parameter extraction were developed [11], [20]. However, only turn-off time was modeled within this paper, and does not include any static characteristics. A SPICE based IGBT model was developed in 2004 accounting for IGBT latch-up and temperature effects [21]. In 2009, a physics based SPICE compact model was created with some ability to customize the device since this model can be used to characterize IGBTs with or without a FS layer [22]. The HiSIM IGBT model was published in 2011 for Si buffer layer IGBTs [23]. Although only measured against 2D device simulation data, this model showed promising predictions focusing on the turn-off behavior. In 2013, a SiC version of the same HiSIM model was published with similar results [24]. A high voltage SiC IGBT model was implemented in MATLAB and published in 2015 [25]. Again, this model will not benefit most circuit designers due to the fact that it is incompatible with any SPICE like simulator.

Although SiC n-channel IGBTs models have been researched and made available, the lack of p-channel IGBT models within the field inhibits the potential progress of power electronics. With the possibilities of complementary circuits, p-channel IGBT models are required to catapult this field into the next generation of high power and high density technology.

1.6 The Unified IGBT model

The Unified IGBT model is a physics based compact MAST model of an n-channel MOSFET driving a PNP Bipolar Junction Transistor (BJT) [26]. It has been previously proven to simulate the performance of SiC n- and p-channel devices [27], and it contains the ability to simulate Si n- and p-channel device configurations as well. The foundation of the model is based upon a widely used Si IGBT model [16]. However, the Unified IGBT model reduces the amount of variables within the code to improve performance without sacrificing noticeable accuracy. This model will be fully explained in detail within Chapter 4.

1.7 Maturing the Unified Model

The goal of this thesis is to update and mature the Unified IGBT model mentioned above. The maturation is accomplished by updating SiC mobility equations, creating a parameter extraction sequence, and creating a Verilog-A version of the model. The current model is in the process of being published as the first SiC p-channel IGBT model. It is also the first IGBT model to combine both Si and SiC material types with n- and p-channel device configurations.

Chapter 2 IGBT Operation

2.1 Operation States of the IGBT

An IGBT can be thought of as a voltage-controlled bipolar junction transistor (BJT) with some inherent MOSFET characteristics, or as commonly referred, a MOSFET driving a BJT. It is a normally off device due to the fact that when the gate voltage applied is less than the threshold voltage of the device, the IGBT is off - the same concept as in the MOSFET. The explanation of how an IGBT works can be divided into three operating conditions: the blocking state, the on-state, and when the device is being switched. The blocking state refers to when the device's purpose is to prevent current from flowing through its collector-emitter nodes. This is the equivalent of a switch in the off position. The on-state refers to when current is flowing between the collector-emitter nodes, and the switching condition is when the device is being turned on and off.

The operation of the IGBT will be explained in reference to a non-punch-through (NPT) n-channel IGBT, which is equivalent to a n-channel MOSFET driving a PNP BJT (PNP refers to the doping types of the two PN junctions associated with the BJT). A NPT IGBT is one of three common structure types of this device, and is constructed with the following layers:

- P+ injection layer – also called the P- emitter,
- N- base region – also called the drain of the MOSFET and base of the BJT,
- P+ body region – also called the collector of the PNP BJT, and the
- N+ source region – which is the source of electrons for the MOSFET current.

These layers and their functions will be explained in more detail in the following section. The other two common structures, PT IGBT and a FS IGBT, will be described in section 2.2. Not

shown in all the following figures, but is inferred, is the metal connection beneath the P+ injection layer, completing the collector terminal of the IGBT.

2.1.1 Blocking State

During the blocking state, the IGBT is off and a large amount of voltage can be applied to the collector-emitter terminals without allowing any current to flow through the device (besides a negligible amount of leakage current). For this condition to be met, the gate voltage applied to the device is less than the threshold voltage of the IGBT, so that the inversion layer beneath the gate does not form. However, every semiconductor device has an upper limit on the voltage it can support - referred to as the breakdown voltage - which can occur in two conditions.

The first condition is referred to as the reach-through condition. When a positive voltage is applied to the collector and a voltage less than the threshold voltage is applied to the gate, the junction labeled J2 in Figure 2.1 becomes forward biased. Junction J2 supports the forward blocking voltage until the depletion layer width, also depicted in Figure 2.1, reaches the P+ injection layer. When the depletion width reaches the P+ injection layer, or J1, the reach-through condition has been met. At this point, holes will be injected into the P+ body region, and a substantial amount of current will begin to flow through the IGBT. The voltage required to achieve the reach-through condition is one upper limit, or breakdown voltage ($BV_{reach-through}$), of a device and is represented by Equation 2.1 [3].

$$BV_{reach-through} = \frac{q \cdot nb}{2 \cdot \varepsilon_s} \cdot wb^2 \qquad 2.1$$

Where q is the electrical charge, nb is the N- base region doping concentration, wb is the width of the N- base region, and ε_s is the relative permittivity of silicon. Although this condition is not modeled in this work, it is an important consideration when designing a high voltage IGBT.

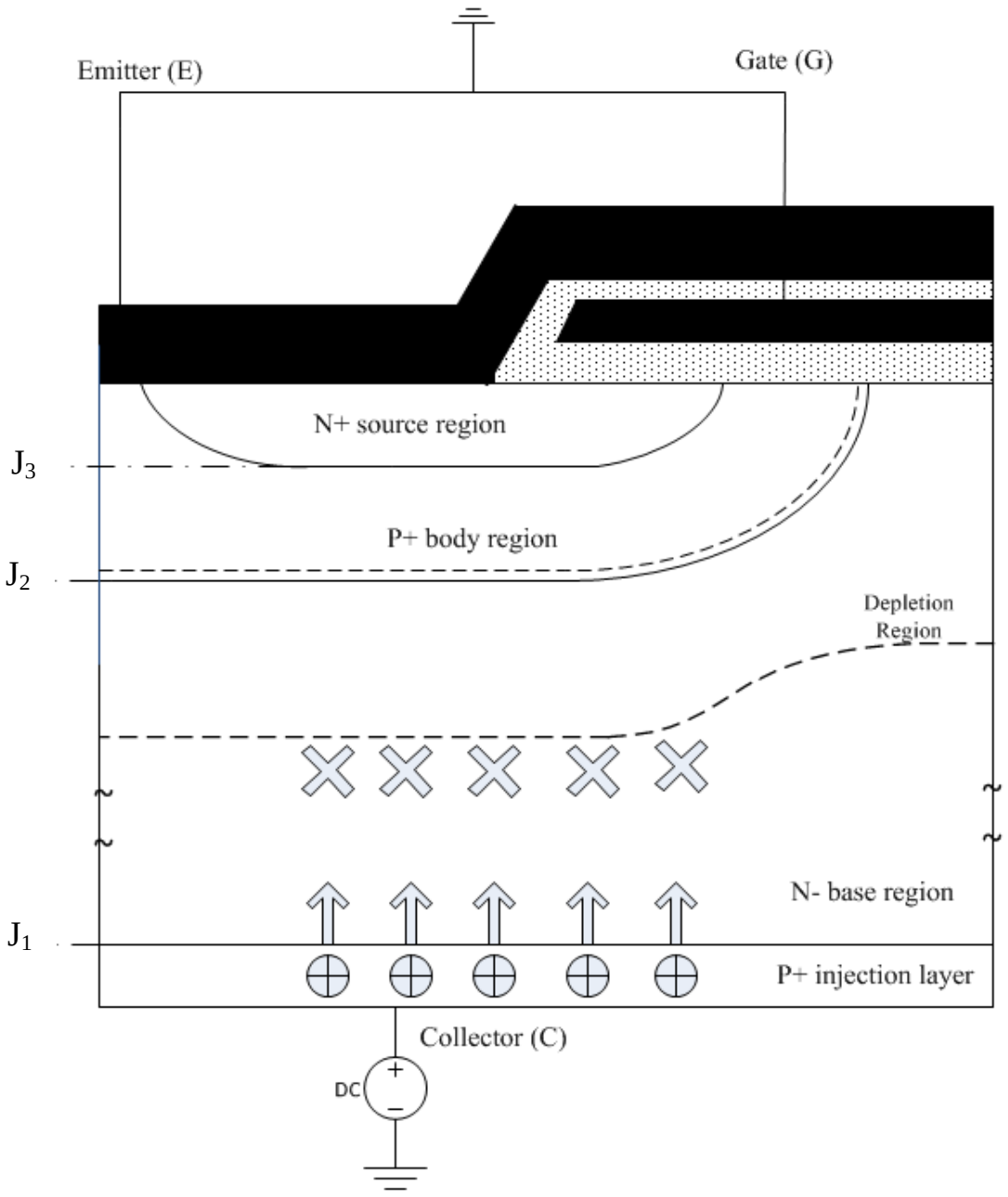


Figure 2.1 NPT n-channel IGBT cross section with a representation of the device in a forward blocking condition. The dashed lines are referring to the depletion regions, the "X's" represent that the depletion layer "stops" the hole current.

The second condition is determined by the process of avalanche breakdown, which is the condition modeled in the IGBT model and explained in Chapter 3. The same positive voltage is applied to the collector in this condition, and can take place regardless of the gate voltage of the

device. Avalanche breakdown takes place when the maximum electric field present within the depletion region (of the N- base region) equals the critical electric field of the semiconductor material. This condition is represented by Equation 2.2 [3].

$$BV_{AB} = 5.34 \times 10^{13} \cdot nb^{-0.75} \quad 2.2$$

A NPT IGBT has reverse blocking capabilities that are not present in the PT IGBT. Just as J2 (in Figure 2.1) is defined as the junction that supports the forward blocking voltage, J1 is similarly defined as the junction that supports the reverse blocking voltage capabilities. Since J1, like J2, is also a N-P+ junction, it has the equivalent blocking capability as J2. This is why the NPT IGBT is also referred to as the symmetric IGBT.

2.1.2 On-state

During the on-state, the voltage applied to the gate will be equal to or greater than the threshold voltage of the device. This allows an inversion layer to form beneath the gate, connecting the N+ source region to the N- base region. This connection allows current to flow into the N- base region, and is the MOSFET part of the IGBT, as it performs similarly. This flow of electrons serves as the driving force, or base current, of the PNP BJT. The flow of electrons into the N- base region creates a substantial amount of holes injected from the P+ injection layer into the N- base region. The injected holes travel towards the P+ body region by both drift and diffusion mechanisms [28]. As soon as the holes reach the P+ body region they are attracted by the electrons from the source metallization that contacts the N+ source region. The holes are then quickly recombined. This junction, J2, is “collecting” the diffusing holes, and thus functions as the collector of the PNP BJT. Since the internal BJT is in a PNP configuration, the BJT collector is the negative terminal, and the emitter is the positive terminal. Thus, the emitter of the PNP

BJT is the collector of the IGBT. Through the arrows and dotted lines, the flow of carriers during the on-state in represented within Figure 2.2.

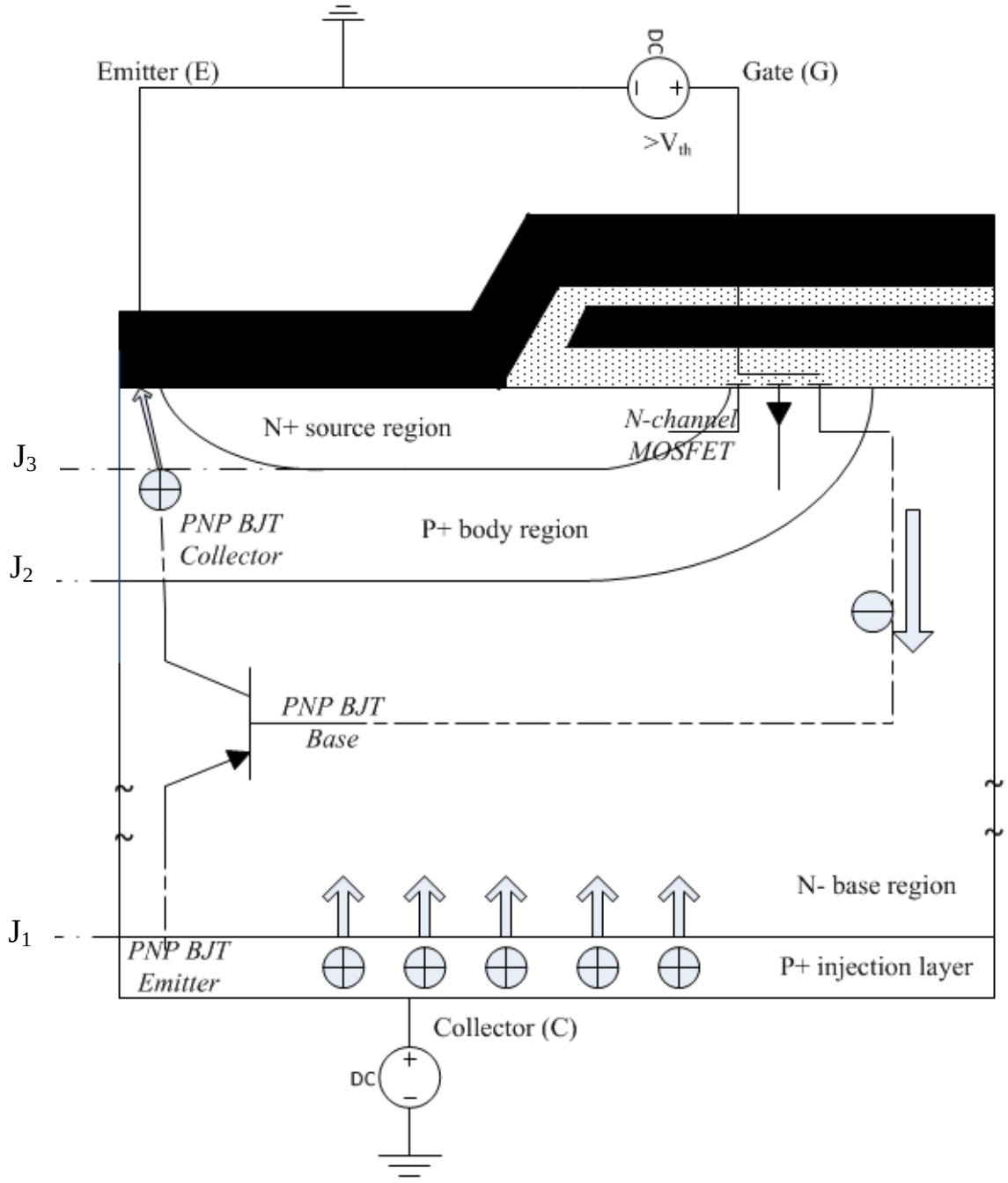


Figure 2.2 NPT n-channel IGBT cross section with an overlay representing the flow of carriers during the on-state.

2.1.3 Switching

The last operation condition to be discussed is when the IGBT is switched on and off. The transient data used to verify the Si-SiC IGBT model are inductive load turn-off responses; therefore, this specific condition will be described. This response is controlled by switching the gate from a value above the threshold voltage to a value below the threshold voltage. In a clamped inductive load testbench, as shown in Figure 6.11, the IGBT will not begin to decrease in current until the full load voltage of the circuit has been reached. The initial decrease in the IGBT's collector current is represented by *t1* in Figure 2.3.

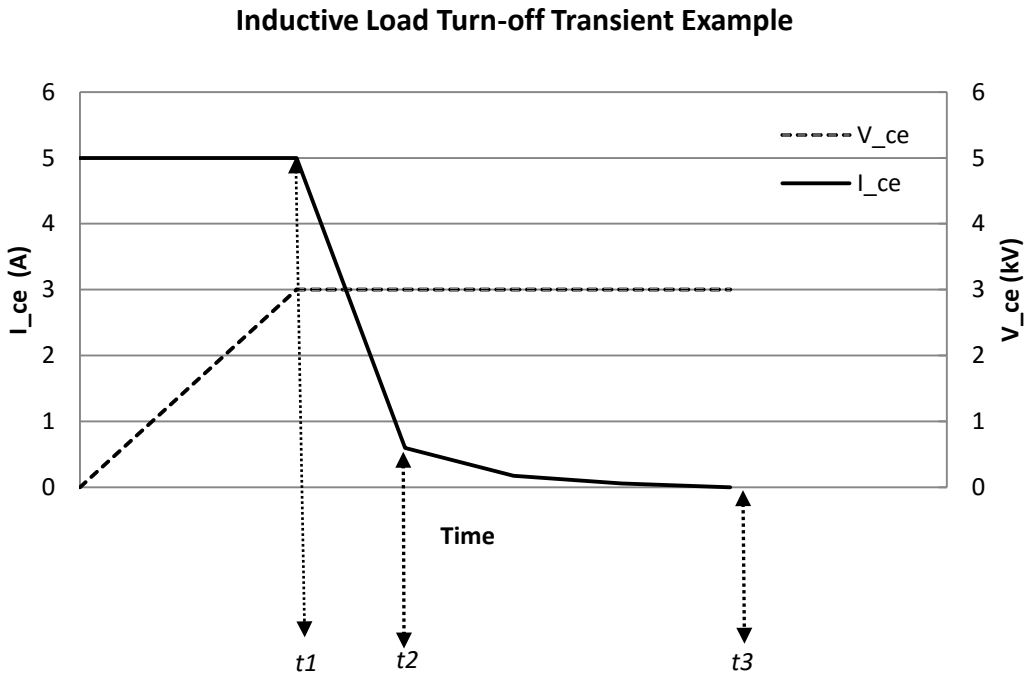


Figure 2.3 Example of an inductive load turn-off response.

After the initial decrease in collector current, the turn-off response is highly dependent on the excess carrier lifetime within the base. When the gate voltage is switched to a value below the threshold voltage, the inversion layer underneath the gate is cut off, and the flow of electrons

from the N+ source region to the N- base region ceases. The reduction in flow of electrons causes a dramatic decrease in the IGBT's collector current and is correlated to the MOSFET current ceasing, represented by *t2* in Figure 2.3. The excess flow of electrons in turn stops the injection of holes from the P+ collector into the N- base region. However, excess electrons from the MOSFET current and excess holes from the P+ injection layer are left in the N- base region. The tail current is an electrical representation of the physical recombination of electrons and holes within the N- base region. The excess carrier lifetime determines the time it takes for the recombination to take place. Once this happens, the device is fully off, and the process will repeat when the appropriate voltages are applied. The end of the tail current is represented by *t3* in Figure 2.3.

When designing an IGBT, a tradeoff must not only be made between the on-state losses and the breakdown voltage, a tradeoff between the on-state losses and a faster turn-off time must also be made. The NPT IGBT concentration of hole injection can be controlled by the doping profile of the moderately doped P+ injection layer [11]. This allows the amount of excess carriers within the N- base region to be reasonably low, reducing the losses during turn-off, while still having enough holes injected into the N- base region to cause conductivity modulation in the base. Conductivity modulation needs to occur in the base to decrease the amount of on-state resistance within the IGBT. Hence, a tradeoff between on-state losses and turn-off time is required.

2.2 Variations in Structures of IGBTs

There are two other variations to the IGBT structure that are presented here: PT IGBT, or buffer layer IGBT, and field-stop IGBT. As the benefits and structural properties of the NPT IGBT have been discussed in section 2.1, the PT and FS IGBT structures will be discussed here

in a similar manner. Not discussed in this chapter are the varieties of gate structures commonly used, such as the trench gate structure. These gate structures are similar to those utilized in MOSFET designs and have comparable benefits.

The PT-IGBT is created using a P+ substrate as the IGBT's collector terminal with a lightly doped N- base region, and a highly doped, N+, buffer layer, shown in Figure 2.4. As explained in the Blocking Region section of 2.1.1, the depletion region of J2 must be prevented from reaching through to the P+ injection layer. The N+ buffer layer does this by drastically reducing the electric field of the N- base region as it approaches the N+ buffer layer, giving the IGBT the more desirable trapezoidal electric field distribution. The trapezoidal electric field distribution of the IGBT allows the N- base region to be significantly shorter than that of a NPT IGBT at the same forward blocking voltage, decreasing the on-state losses [11]. The on-state characteristics are also improved by a large hole injection due to the high doping concentration in the P+ injection layer. However, the high amount of hole injection increases the required amount of excess carriers that must be removed during turn-off, increasing the tail current of the IGBT.

To combat this loss, the excess carrier lifetime must be controlled by designing the device with a lifetime reduction process. However, this process increases the on-state losses, as it reduces carriers within the entire N- base region, not just around the P+ substrate where the excess holes are being injected [11]. This is why a lower lifetime in the base region correlates to low conductivity in the base, which increases the on-state resistance of the device. Therefore, a tradeoff between turn-off times and on-state losses must be made when designing a PT IGBT, just as in the NPT IGBT.

As briefly described earlier, the addition of a buffer layer takes away the ability for the PT IGBT to have any practical reverse blocking capability. With a highly doped buffer layer, J1 is now bounded by two highly doped regions, reducing this junction's breakdown voltage to a few tens of volts [28]. The addition of the buffer layer also causes the structure to become asymmetrical, the origin of the asymmetrical IGBT namesake.

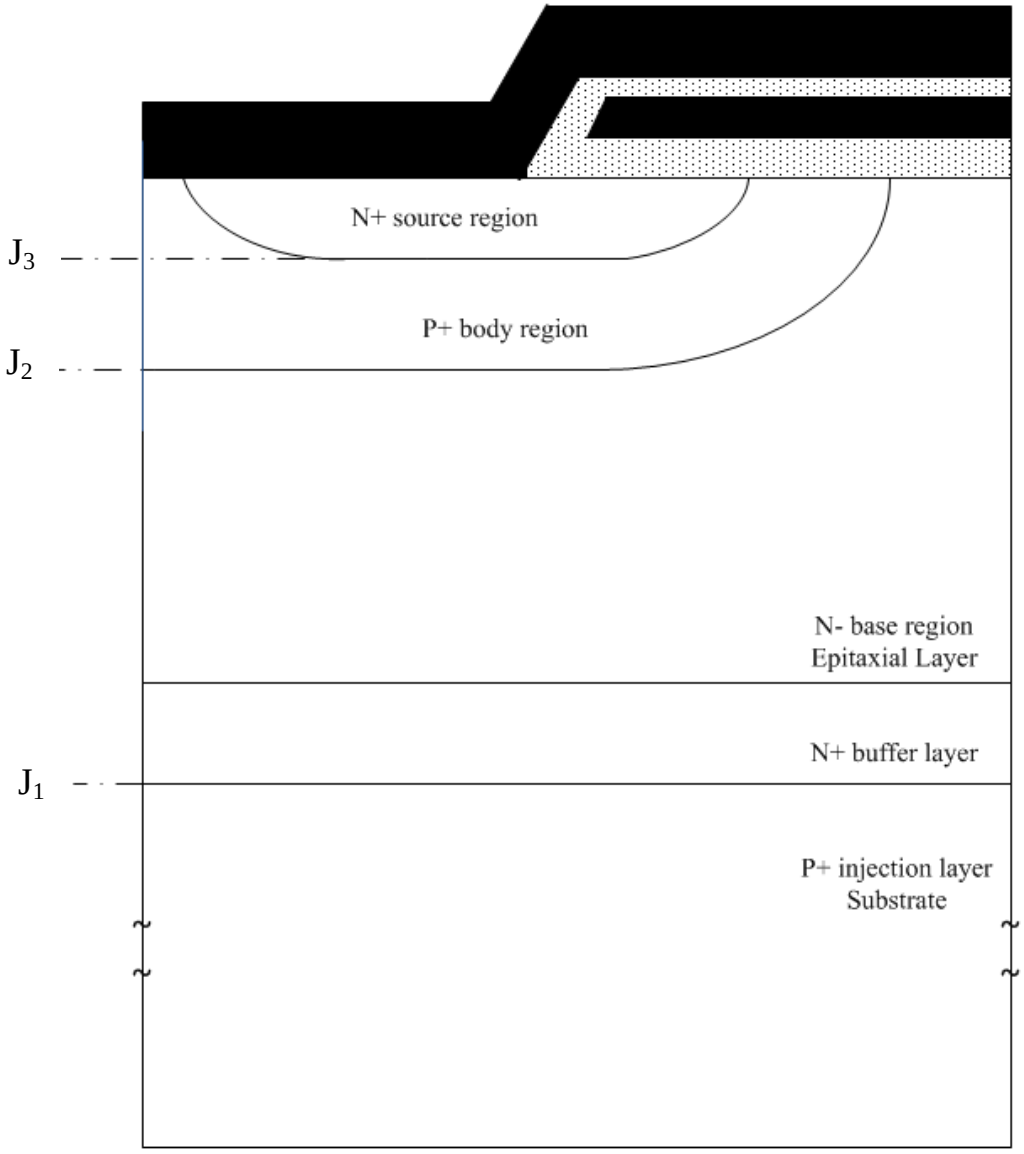


Figure 2.4 N-channel PT IGBT cross section.

The field-stop layer IGBT, shown in Figure 2.5, combines the thin moderately doped P- emitter of the NPT IGBT and the moderately doped N+ buffer layer of the PT IGBT creating a superior IGBT structure utilizing both enhancements of NPT and PT structures. This results in: (1) a thin N- base region, lowering the on-state conduction losses without reducing the breakdown voltage; and (2) a low hole injection from the P- emitter, lowering the amount of stored charges in the base [11]. With fewer charges to recombine within the base, the tail current of the field-stop IGBT is shorter than a PT IGBT. The tail current can now be modified without reducing the conductivity in the base.

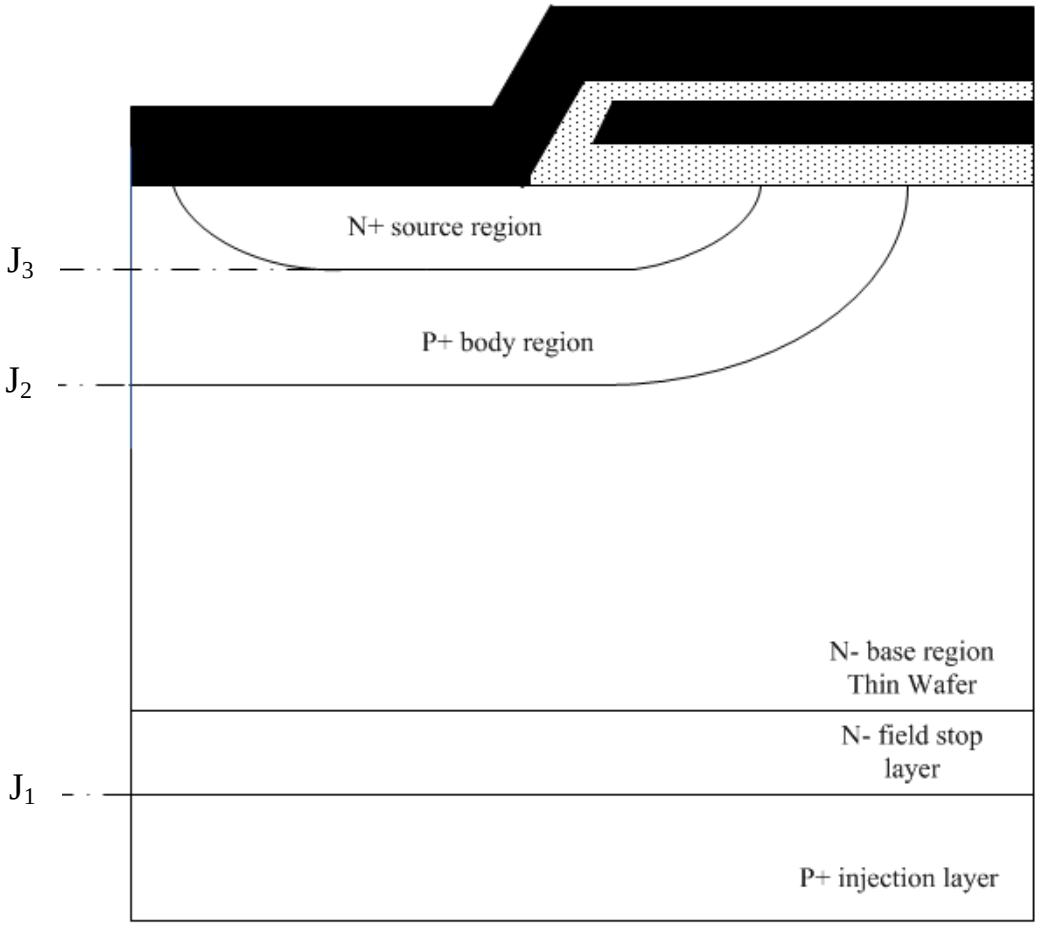


Figure 2.5 N-channel FS IGBT cross section.

Generally, a perfectly designed IGBT only exists for one specific application. Due to all the tradeoffs discussed throughout this chapter, an IGBT's turn-off time, blocking voltage, and on-state resistance cannot be optimized for all types of circuits. Following is a description of the tradeoffs that are made within each major layer of the IGBT, as well as a summary of all the tradeoffs that have been mentioned in this chapter. As mentioned previously, the gate structures share the same tradeoffs with MOSFETs, so the tradeoffs for different gate structures will not be discussed here.

Figure 2.6 shows a visual representation of the tradeoffs required in each section of an IGBT. Within the N- base region, two properties, lifetime and width, must be compromised with the following:

- a smaller width leads to lower on-state resistance;
- a larger width leads to higher blocking voltage ratings;
- a shorter lifetime correlates with a smaller tail current; and,
- a longer lifetime sustains a high conductivity modulated base, which reduces the on-state resistance.

The field-stop layer needs to provide the IGBT with a reduction in hole injection from the P+ injection layer, compared to a NPT IGBT. However, the field-stop layer still has to provide enough hole injection to produce conductivity modulation in the base. Similar to the field-stop layer, the P+ injection layer must be doped highly enough to produce conductivity modulation in the base, and still not flood the N- base region with excess charges, inhibiting the tail current of the device.

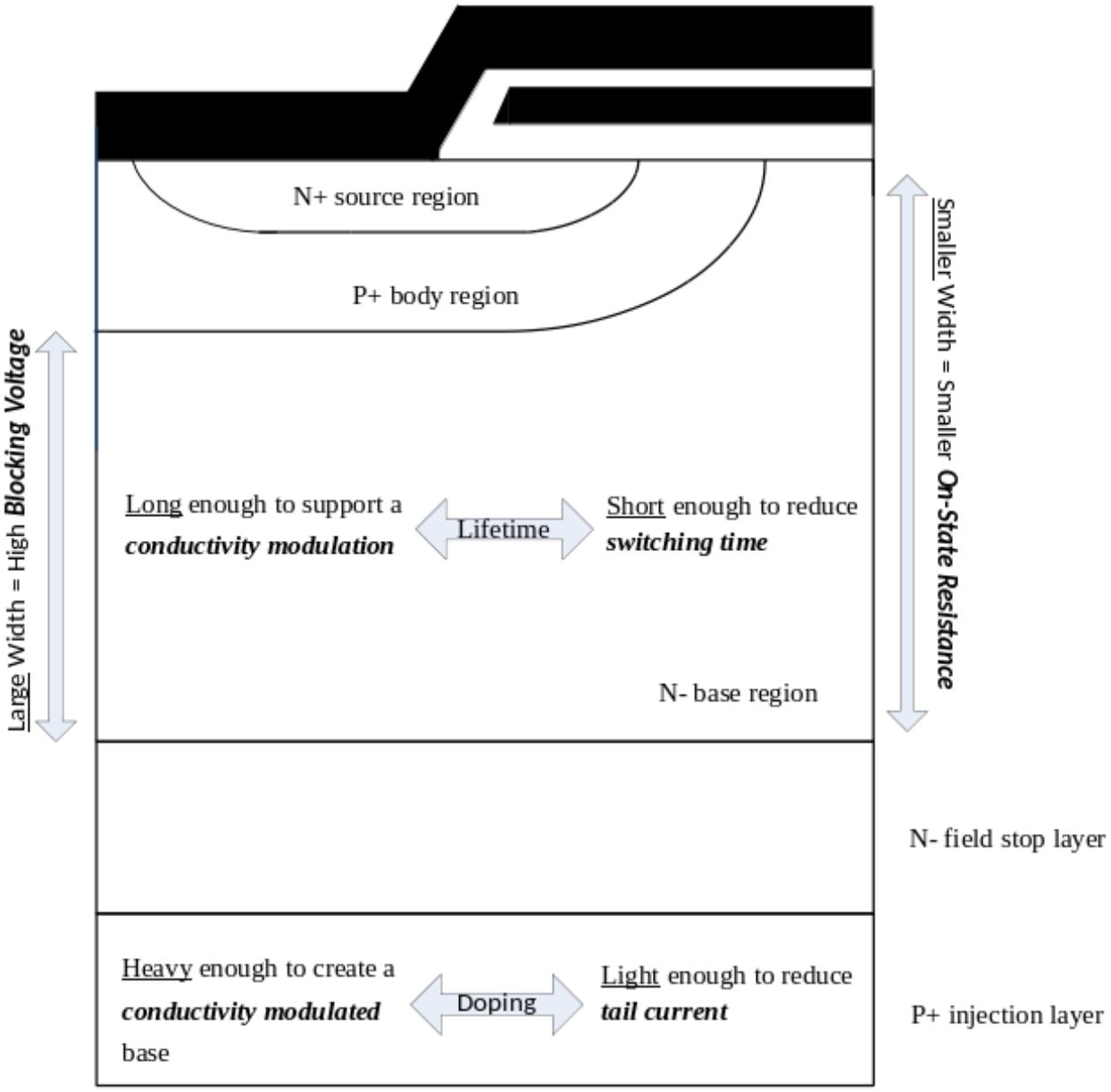


Figure 2.6 Trade-offs of designing an IGBT by layer.

Chapter 3 The 2012 Unified IGBT Model

3.1 Introduction

The Unified IGBT model is a physics based compact model that predicts the performance of Si, SiC, n-channel, and p-channel devices. The foundation of the model is based upon a Si IGBT model [16], and is modified to incorporate SiC and p-channel physics. The latest SiC mobility equations and material properties are used, as described in detail in Chapter 4. The physics to describe the IGBT's performance is designed for a non-punch through device; however, this model is proven to predict the performance of Field-stop Layer IGBTs. As a physics based compact model, it not only accurately predicts the performance of these IGBTs, but allows circuit designers to use the model without the extended simulation time of finite element based physical models. Empirical temperature scaling equations are implemented, allowing the user to fully utilize the model in any circuit design from 25 to 500 ˚C [26]. Discussed further is a description of how physical effects in IGBTs are accounted for, and how the model is formulated in the MAST language. A description of parameters for this model is given in Appendices A.1 and A.2.

Approximations to the foundation model have been made to improve simulation speed, with the slightest reduction in accuracy. This is discussed in Section 3.4.1, as the approximations are implemented within the BJT portion of the model. The value $m\_channel$, present in the MOSFET current equations, effects the polarity of the device and is explained in detail in section 3.5.

3.2 Structure

A common n-channel NPT IGBT structure is shown in Figure 3.1, overlaid with a detailed circuit representation of the model [16]. The device has three terminals, the gate (G), the collector (C), and the emitter (E). The MOSFET and BJT symbols within the circuit show how the MOSFET drain provides base current to the BJT portion of the device. The internal drain (d) and source (s) nodes, as well as the gate terminal (G) are associated with the MOSFET portion of the IGBT. The internal collector (c), emitter (e), and base (b) nodes are associated with the PNP BJT portion of the device. In the formulation of the model, nodes, d and e are named internal nodes, as they both connect to the internal BJT and the MOSFET of the IGBT. Nodes b and d, shown in Figure 3.1, combine to form node d when the model is implemented. Likewise, nodes c and s combine and are implemented as the Emitter terminal (E).

3.3 MOSFET Portion

This portion of the model consists of the MOSFET current (I_{mos}) - which supplies current to the base of the BJT - and three capacitances: the drain-source junction (C_{dsj}), C_{gs}, and the gate-drain (C_{gd}). I_{mos} is defined by the piecewise behavior around the device drain voltage given in Equations 3.1 and 3.2 I_{mos} utilizes the common transconductance parameters, K_{Plin} and K_{Psat}, differently to produce kf and kp [17] , shown in Equations 3.3 and 3.4. The model parameter $theta$, shown as θ in Equation 3.5, accounts for channel mobility reduction due to the high transverse electric field. The entire reduction factor is introduced as $mufact$, and is shown in Equation 3.5.

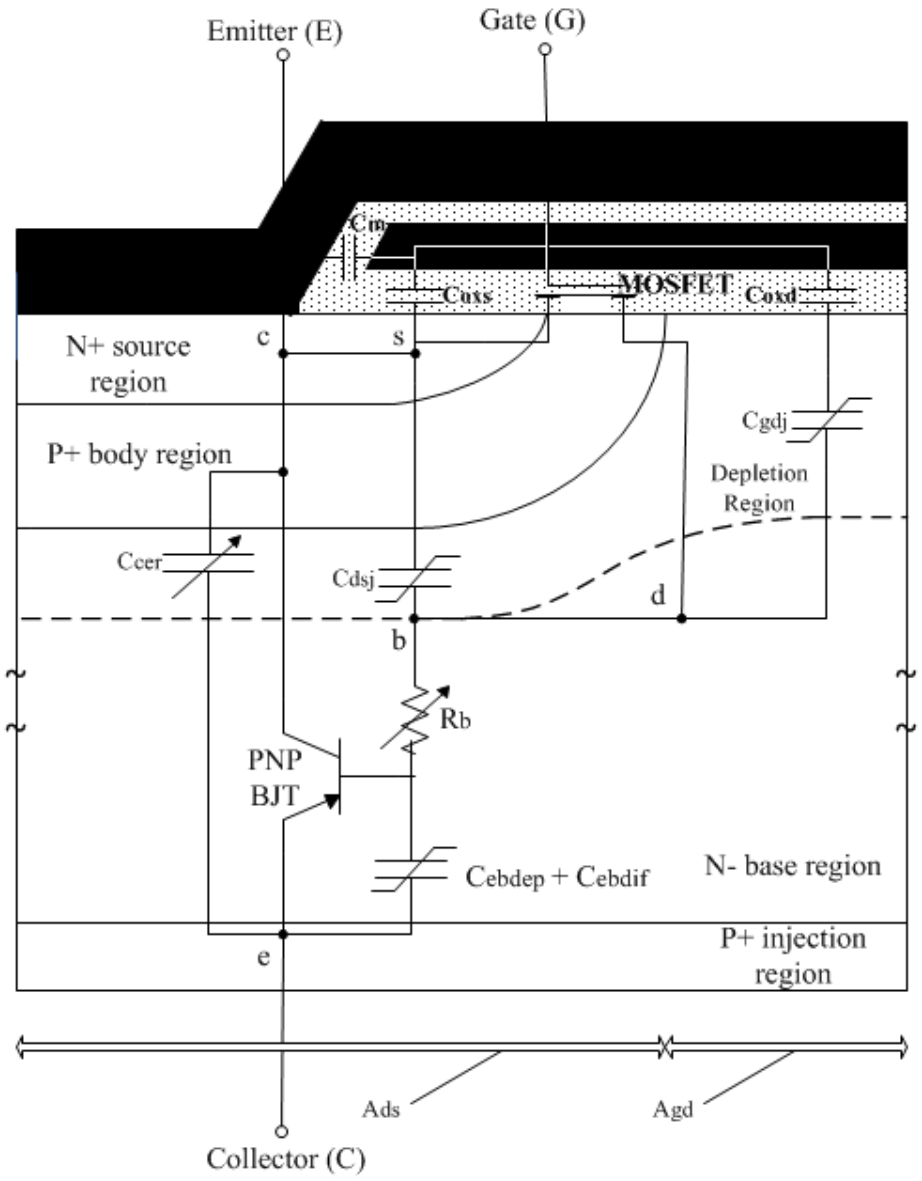


Figure 3.1 Cross-section of a NPT IGBT overlaid with an equivalent circuit of the IGBT model [16].

$$I_{mos_{V_{ds}\geq 0}} = \begin{cases} 0 & ,V_{gs} < vt \\ \dfrac{kp \cdot kf \cdot \left(V_{gs} - vt - kf \cdot \dfrac{V_{ds}}{2}\right) \cdot V_{ds}}{mufact} & ,V_{ds} \leq (V_{gs} - vt)/kf \\ \dfrac{0.5 \cdot kp \cdot (V_{gs} - vt)^2}{mufact} & ,V_{ds} \geq (V_{gs} - vt)/kf \end{cases} \quad 3.1$$

$I_{mos_{V_{ds}<0}}$

$$= \begin{cases} 0 & , \quad m_{channel} \cdot (V_{gs} - V_{ds}) < vt \\ \dfrac{kp \cdot kf \cdot \left[m_{channel} \cdot (V_{gs} - vt) - kf \cdot \dfrac{V_{ds}}{2}\right] \cdot V_{ds}}{mufact}, & -V_{ds} \leq m_{channel} \cdot \dfrac{\left[(V_{gs} - V_{ds}) - vt\right]}{kf} \\ \dfrac{-0.5 \cdot kp \cdot \left[m_{channel} \cdot (V_{gs} - V_{ds}) - vt\right]^2}{mufact} & , V_{ds} \geq \dfrac{V_{gs} - vt}{kf} \end{cases} \quad 3.2$$

$$K_{plin} = \frac{kf}{kp} \quad 3.3$$

$$K_{psat} = kp \quad 3.4$$

$$mufact = 1 + \theta(V_{gs} - vt) \quad 3.5$$

Capacitances related to the MOSFET portion of the device involve the gate terminal and the drain and source nodes, which can be seen in Figure 3.1. The gate-source capacitance (C_{gs}) is the source metallization capacitance (C_m) summed with the portion of the gate oxide capacitance which overlaps the source (C_{oxs}), as shown in Figure 3.1. C_{gdj} and C_{oxd} combine to form the gate-drain capacitance, (C_{gd}). The gate-drain capacitance is implemented as a piece-wise equation, shown in Equation 3.6, due to the fact that when $V_{ds} > (V_{gs} - V_{td})$, the area beneath the gate-drain overlap region becomes depleted, reducing the capacitance. The drain-source junction capacitance (C_{dsj}), shown in Equation 3.8, is a depletion capacitance over the drain-body junction, where cjo is the zero bias junction capacitance and mj is the gradient coefficient. A_{gd} is the gate-drain overlap area and A_{ds} is the body region area, where the sum of these areas is equal to the active area of the device, a [16]. This relationship is represented in Figure 3.1.

$$C_{gd} = \begin{cases} coxd & , V_{dg} \leq -V_{td} \\ coxd \Big/ \left[1 + \left(coxd \cdot W_{gdj} \Big/ A_{gd} \cdot \varepsilon\right)\right] & , V_{dg} > -V_{td} \end{cases} \quad 3.6$$

$$C_{bcj} = \begin{cases} \dfrac{a \cdot cjo}{\left(1 + \dfrac{V_{ds}}{pb}\right)^{mj}} \ , V_{ds} \geq (-fc \cdot pb) \\ \dfrac{a \cdot cjo \cdot \left[1 - (1 + mj) \cdot fc - mj \cdot \dfrac{V_{ds}}{pb}\right]}{(1 - fc)^{mj+1}} \ , V_{ds} < (-fc \cdot pb) \end{cases} \quad 3.7$$

$$C_{dsj} = C_{bcj} \cdot \frac{A_{ds}}{a} \quad 3.8$$

Due to the fact that V_{ds} and V_{bc}, are equivalent, the depletion capacitance C_{bcj} is used to calculate C_{dsj}, which is shown Equation 3.8. C_{bcj} is also used to calculate the capacitance between the emitter and the collector (C_{cer}). This capacitance is part of the BJT component and will be described in the following section.

To compute the current contributions of C_{gs}, C_{gd} and C_{dsj}, two different methods are employed. The currents generated from C_{gs} and C_{dsj} are computed by defining the charge and then taking the time derivative as explained later. These charge calculations are shown in Equations 3.9 and 3.10. The capacitance calculated in Equation 3.8 is utilized for capacitance verification. The current contribution from C_{gd} is calculated by multiplying the capacitance by the time derivative of its voltage. This is shown and explained in the MAST Formulation section.

$$qcgs = C_{gs} \cdot V_{gs} \quad 3.9$$

$$qcdsj = A_{ds} \cdot \sqrt{2 \cdot \varepsilon_s \cdot (V_{ds} + pb) \cdot q \cdot nb} \quad 3.10$$

3.4 BJT Portion

There are three current contributions related specifically to the BJT: the base current (ibp), the total emitter current (irb), and the collector current (icp), shown in Equations 3.11 through 3.14.

$$ibp = qceb \Big/ \left(tauhl + \left[\frac{qceb^2 \cdot nb^2 \cdot isne}{qb^2 \cdot ni^2} \right] \right) \quad 3.11$$

$$rb = \begin{cases} \dfrac{w}{mun \cdot a \cdot q \cdot nb} + rs \quad , & qceb \leq 0 \\ \dfrac{w}{mueff \cdot a \cdot q \cdot neff} + rs \, , & qceb > 0 \end{cases} \tag{3.12}$$

$$irb = \begin{cases} V_{ae}/rb \quad , & qceb \leq 0 \\ V_{ae}/rb \quad , & qceb > 0 \end{cases} \tag{3.13}$$

$$icp = \frac{irb}{(1+b)} + \frac{b}{(1+b)} \cdot \left(\frac{4 \cdot dp \cdot qceb}{w^2}\right) \tag{3.14}$$

As given, $qceb$ is the emitter to base charge, qb is the background base charge, w is the quasi-neutral base width, mun is the electron mobility, rs is the series resistance implemented as a model parameter, $mueff$ is the effective mobility, and $neff$ is the effective base doping concentration. b is the ambipolar mobility ratio, and dp is the hole diffusivity.

3.4.1 Approximations

Two approximations have been made within this model: the carrier-carrier scattering effect, which reduces the carrier mobility, as well as the second order component of the space charge concentration, N_{sat}, are both negligible, and thus can be eliminated. Both of these approximations are used within the BJT portion of the model. These two approximations reduce the number of simultaneous equations, and thus improve the speed of this compact model.

The carrier-carrier scattering effect approximation is taken into account within the total emitter current through the base resistance, rb, shown in Equation 3.12. In Equation 3.12, mun, the electron mobility, is used solely in the calculation of rb instead of accounting for the additional reduction in mobility, μ_c, due to carrier-carrier scattering. With this second order effect, μ_c, taken out of the equation, the base resistance becomes slightly smaller than what it would have been if the carrier-carrier scattering effect was taken into account. Although this approximation may reduce the total accuracy of the model by a minute amount, the difference

can be accounted for empirically through the parameter rs, the series resistance, which is added to the calculated value of rb shown in Equation 3.12. Adding an empirical amount of series resistance to rb increases the total base resistance; this accounts for the mobility reduction effect. However, the series resistance is a linear approximation of the mobility reduction instead of a dynamic mobility reduction dependent on the excess carriers within the base region, $qceb$. Since μ_c has been replaced by rs, as $qceb$ decreases, rb is not decreasing. Although this effect is no longer dependent on $qceb$, reducing the total number of simultaneous equations and adding the effect through a parameter reduces simulation time, and allows an approximate value of base resistance to be modeled.

In addition to reducing the overall simulation time, adding an empirical model parameter to model the carrier-carrier scattering effect adds another level of flexibility to the model, making it easier to verify. Without the series resistance included in Equation 3.12, no model parameter can directly control the total base resistance in a similar manner. Adjusting model parameters to indirectly affect the total base resistance of the IGBT increases the time it takes to characterize and fit the model. Therefore, with a direct correlation between rs and rb, the parameter extraction process is simplified.

Since μ_c has been ignored, the value of $mueff$ has also been approximated to the value shown in 3.15. The approximation from the original $mueff$ equation is explained in [26].

$$mueff = mun + mup \cdot \frac{p0}{nb} \Big/ \left(\left[\frac{p0}{nb} + 1 \right] \right) \tag{3.15}$$

The second-order effect on the space charge concentration, N_{sat}, approximation is taken into account when calculating the total charge concentration. The total space charge concentration within the base-collector region is equal to only the base doping concentration, nb, because the additional space charge N_{sat} is negligible. Also, because N_{sat} has been ignored, the

value of qb is approximated and is shown Equation 3.16. Likewise, all equations involving nb have been approximated this way.

$$qb = a \cdot q \cdot w \cdot nb \tag{3.16}$$

3.4.2 Base Charge

To define the emitter to base charge of the IGBT, $qceb$ is solved such that the emitter-base junction voltage, V_{ebj}, and the sum of $voff$ and the emitter-base terminal voltage (V_{eb}) are equal. This "solve such that" (or implicit constraint equation) definition of $qceb$ is identified via a colon in the MAST language, and is shown in Equation 3.17. Although this equation contains only voltage and parameter values, Equation 3.17 is a simultaneous equation and therefore must be implemented via the equation section of the MAST model. An explanation of the formulation of the MAST model is described in Section 3.5. Equation 3.17 is also implemented differently within the Verilog-A model, as explained in Chapter 5.

$$qceb: V_{ebj} = V_{eb} + voff \tag{3.17}$$

The emitter base junction voltage is calculated during three operation points:

- reverse conduction,
- forward conduction when $qceb$ is less than the zero bias base charge, $qceb0$, and
- forward conduction when $qceb$ is greater than $qceb0$.

V_{ebj} is shown in Equation 3.18, and $qceb0$ is shown in Equation 3.19.

$$V_{ebj} = \begin{cases} V_{ebdep}, & qceb \leq 0 \\ \dfrac{qceb \cdot V_{ebdif}}{qceb0}, & 0 < qceb < qceb0 \\ V_{ebdif}, & qceb \geq qceb0 \end{cases} \tag{3.18}$$

$$qceb0 = a * \sqrt{2 * \varepsilon * q * nb * pb} \tag{3.19}$$

V_{ebdep}, the emitter-base depletion voltage, and V_{ebdif}, the emitter-base diffusion voltage, are shown in Equations 3.20 and 3.21, respectively. $p0$, a factor used to simplify the equation, is shown in Equation 3.22.

$$V_{ebdep} = pb - \left(0.5 \cdot (qceb - qceb0)^2 \Big/ q \cdot nb \cdot a^2 \cdot \varepsilon \right) \quad 3.20$$

$$V_{ebdif} = V_{th} \cdot \ln\left[\left(\frac{p0}{nb} + 1\right) \cdot \left(\frac{p0 \cdot nb}{ni^2} + 1\right)\right] - \frac{2 \cdot mun \cdot mup \cdot {V_{th}}^2}{2 \cdot V_{th} \cdot (mup + mun) \cdot mun} \cdot \ln\left[\frac{p0}{nb} + 1\right] \quad 3.21$$

$$p0 = qceb \Big/ q \cdot a \cdot l \cdot \tanh\left(\frac{w}{2 \cdot l}\right) \quad 3.22$$

V_{ebdep} and V_{ebdif} represents the voltage across the capacitors C_{ebdep} and C_{ebdif}, respectively, as shown in Figure 3.1. These capacitances, in part, determine the emitter-base voltage, shown through the relation of V_{ebj} in Equation 3.18.

3.4.3 Collector to Emitter Capacitance

The collector to emitter capacitance (C_{cer}) is a function of the internal BJT's base charge [16]. It is defined in Equation 3.23:

$$C_{cer} = qceb \cdot C_{bcj}/(3 \cdot qb) \quad 3.23$$

where C_{bcj} is defined in Section 3.3.

3.4.4 Breakdown Voltage and Multiplication Factor

Although not specifically confined to the BJT portion of the device, the breakdown voltage and avalanche multiplication current will be explained here. The collector-base breakdown voltage, BV_{cbo}, is approximated using Equation 3.24 [16]. Throughout the remainder of this thesis, the collector-base breakdown voltage will be denoted as $bvcbo$, as it is denoted in the model. The parameter bvf is added to the approximation described in Equation 2.2 to

account for the shorter N-base regions that can support a higher blocking voltage with the same doping concentration due to the overall device structure, as described in Chapter 2.

$$bvcbo = \frac{bvf \cdot 5.34e13}{nb^{0.75}} \tag{3.24}$$

In the model, if V_{ds} is greater than the collector-base breakdown voltage multiplied by the breakdown uniformity factor – i.e. if V_{ds} reaches the breakdown voltage defined, then the avalanche multiplication factor, m, will equal such a value that causes the IGBT current to increase accordingly. Due to its size, this equation can be found in Appendix A.1. However, when the breakdown voltage is not reached, m still affects the total current of the IGBT, albeit in a small manner. The value of the avalanche multiplication factor when the breakdown voltage has not been reached is given as Equation 3.25. m is then used to determine the multiplication current, $imult$, which also contains the amount of current generated thermally, $igen$. Equations 3.26 and 3.27 describe $igen$ and $imult$, respectively.

$$m = \begin{cases} 1, & V_{ds} \leq 0 \\ \dfrac{1}{\left(1 - \left(\dfrac{V_{ds}}{bvcbo}\right)\right)^{bvn}}, & V_{ds} < fc\_bvbco \cdot bvcbo \end{cases} \tag{3.25}$$

$$igen = \frac{q \cdot ni \cdot a \cdot \sqrt{2 \cdot \varepsilon \cdot \left|\frac{V_{ds}}{q \cdot nb}\right|}}{tauhl} \tag{3.26}$$

$$imult = (m-1) \cdot \left|imos + icp + \left(C_{cer} \cdot \dot{V_{ds}}\right)\right| + (igen \cdot m) \tag{3.27}$$

3.5 MAST Formulation

Before the formulation of the model can be described, a brief overview of how MAST models are constructed is given. MAST models are separated into multiple sections with specific functions: structure, parameters, values, and the equation section. While there are other sections

that can be implemented in MAST models (namely in support of mixed-signal constructs) they are not required for a model of this type and the discussion will be limited to sections relevant to compact device models.

The structure section is used to denote the model interface. Here the outline of the model and the user parameters are defined. The outline of the model includes items such as terminals, options (parameters) the user will be able to select, and a list that includes all numbers, values, and variables – i.e. every item that is used throughout the model. Within the MAST model, a variable is defined by a simultaneous equation, and a value is an item that is dependent on one or more variables or values. The parameters section contains the number definitions. A number is any item defined as a numerical value – e.g. the zero bias base charge ($qceb0$), defined by Equation 3.19. Within Equation 3.19, all components are constant numerical values. More definitively, a number cannot contain an item that is dependent on a value or a variable. Therefore, only user parameters defined in the structure section and numbers can be listed in the parameter section. The values section contains the definition of all items that are dependent on variables. For example, voltages are defined here, and hence all items dependent on voltages. The equations section is where the current contributions are defined. This is also where the simultaneous equations are coded, dictating how to solve the variables. The equations section is shown in Figure 3.2.

The Unified IGBT model has the option to simulate both n-channel and p-channel IGBTs. In the interface of the model, the user selects the option for an n- or p-channel device configuration. This selection determines the sign of $m\_channel$ - a value that affects areas of the model involved with determining the polarity of the device. As an example, if the user selects the model to be a p-channel device, then $m\_channel$ will equal negative one. The voltage

definitions, one area affected by the polarity of the device, are calculated to be opposite to that of the n-channel model. *m_channel* also effects the MOSFET current, and was discussed in Section 3.3. Also, as seen in Figure 3.2, when the p-channel model is selected, the currents are listed in the same order as presented in the circuit diagram; however, they are written with negative values. This also accounts for the reverse in the polarity of the p-channel device.

```
equations {
        if(channel==p_channel) {
                i(g->k) +=          -d_by_dt(qcgs)
        i(d->g) += -icdg
        if(model->bvf == inf) {
            i(d->k)     += -imos - d_by_dt(qcdsj)
            }
        else {
            i(d->k)     += -imos - imult - vds/rds - d_by_dt(qcdsj)
            }
        i(e->k)         += -icc
        i(e->d)         += -ibp                          - d_by_dt(qceb)
        i(a->e)         += -irb

        #...Lagging filter
        vdgx:   d_by_dt(vdgx_w) = dvdgdt
        vdsx:   d_by_dt(vdsx_w) = dvbcdt

        qceb:   vebj = veb-model->voff
        }

        else {

                i(g->k) +=          d_by_dt(qcgs)
        i(d->g) += icdg
        if(model->bvf == inf) {
            i(d->k)     += imos + d_by_dt(qcdsj)
            }
        else {
            i(d->k)     += imos + imult + vds/rds + d_by_dt(qcdsj)
            }
        i(e->k)         += icc
        i(e->d)         += ibp                  + d_by_dt(qceb)
        i(a->e)         += irb

        #...Lagging filter
        vdgx:   d_by_dt(vdgx_w) = dvdgdt
        vdsx:   d_by_dt(vdsx_w) = dvbcdt

        qceb:   vebj = veb+model->voff
```

Figure 3.2 Capture of the equations section within the MAST IGBT model. It is separated between n and p-channel operations, with currents defined accordingly between each node listed.

The current contributions from each capacitor within the model are calculated using two methods. The time derivative of the three charges used to compute the current contribution are

$qcgs$, $qcdsj$, and $qceb$. Two other current contributions from the capacitances, $C_{gd}$and C_{ccer}, are calculated following Equations 3.28 and 3.29. As stated in Section 3.3, $qcdsj$ is only calculated for the current contributions and Equation 3.8 is used for the purpose of verifying the capacitances during the parameter extraction process, explained in Section 4.2.1. The current generated from C_{cer} is computed within the total collector current (icc) which is the sum of icp and $iccer$.

$$icgd = C_{gd} \cdot {}^{dV_{gd}}/_{dt} \tag{3.28}$$

$$iccer = C_{cer} \cdot {}^{dV_{ds}}/_{dt} \tag{3.29}$$

3.6 Temperature Scaling

The model contains temperature scaling capabilities via eight parameters: $tauhltexp$, $kptexp$, $kftexp$, $bvntexp$, $bvftexp$, $vtdtco$, $vttco$, and $isnetexp$. The first step in the temperature scaling process is to adjust model parameters so that the simulated data overlays the measured data at room temperature and set all temperature scaling parameters to zero. After room temperature validation has been completed, only the parameters with temperature scaling parameters can be changed: $tauhl$, kp, kf, bvn, bvf, vtd, vt, $isne$. The following equations are then used to extract the temperature scaling parameters externally after the parameter extraction sequences have been performed. This technique involves both nonlinear and linear scaling. The nonlinear temperature scaling equations are represented by Equations 3.30 through 3.35. The linear temperature scaling equations are designed for vt and vtd, and are represented by Equations 3.36 and 3.37 [26].

$$tauhlt = tauhl_{300} \cdot \left[\frac{templim}{tnom}\right]^{tauhltexp} \tag{3.30}$$

$$kpt = kp_{300} \cdot \left[\frac{tnom}{templim}\right]^{kptexp} \quad 3.31$$

$$kft = kf_{300} \cdot \left[\frac{tnom}{templim}\right]^{kftexp} \quad 3.32$$

$$isnet = isne_{300} \cdot \left[\frac{templim}{tnom}\right]^{isnetexp} \cdot e^{1.4\cdot\left(\frac{1}{tnom}-\frac{1}{templim}\right)} \quad 3.33$$

$$bvnt = bvn_{300} \cdot \left[\frac{templim}{tnom}\right]^{bvntexp} \quad 3.34$$

$$bvft = bvf_{300} \cdot \left[\frac{templim}{tnom}\right]^{bvftexp} \quad 3.35$$

$$vtt = vt_{300} \cdot vttco(templim - tnom) \quad 3.36$$

$$vtdt = vtd_{300} \cdot vtdtco(templim - tnom) \quad 3.37$$

Chapter 4 Updating the Unified IGBT Model

To update the Unified IGBT model, SiC mobility equations were researched and a parameter extraction sequence was created.

4.1 Equations and Temperature Dependence

4.1.1 Mobility Model

To estimate the carrier mobility within the IGBT, the bulk mobility within the drift region is modeled and, thus, is dependent on the drift region doping concentration and the temperature of the device. The mobility model is implemented via four main mobility equations: Si electron, Si hole, SiC electron, and SiC hole. The electron mobility is expressed as mun, or $mun0$; where $mun0$ represents the mobility before temperature scaling has been applied, and mun represents the electron mobility after temperature scaling effects have been applied. mup and $mup0$ represent the hole mobility in the same way. If n-channel is selected as an option by the user, $mun0$ will be equal to its calculated mobility equation, and $mup0$ will be equal to its minority carrier mobility constant value. If p-channel is selected, $mun0$ will be equal to the minority carrier constant, and $mup0$ will be equal to it calculated mobility equation, as shown in Equations 4.1 through 4.4 within Tables 4.1 and 4.2

The Si mobility equations and their estimated constants are taken from [3], as the mobility of Si has been studied extensively. The equations associated with the Si mobility model are shown below. The implementation of the temperature dependence of these mobility equations will be described in section 4.1.3.

Table 4.1 Si n-channel Initial Mobility Equations

Si n-channel	
$mun0 = \frac{5.1E18 + 92 \cdot nb^{0.91}}{3.75E15 + nb^{0.91}}$ (4.1)	$mup0 = 495$ (4.2)

Table 4.2 Si p-channel Initial Mobility Equations

Si p-channel	
$mun0 = 1360$ (4.3)	$mup0 = \frac{2.9E15 + 47.7 \cdot nb^{0.76}}{5.86E12 + nb^{0.76}}$ (4.4)

4.1.2 Updated SiC Equations

The basic form of the SiC mobility equations is shown in Equation 4.5. Using the fitting parameters presented in [29] and [30] the SiC n- and p-channel mobility models are implemented, respectively. Table 4.3 organizes the SiC fitting parameters from each of the mobility models. The electron constant is taken from [3], and the hole constant is taken from [31]. The rest of the fitting parameters are cited from their respective mobility equation references. Equations 4.6 through 4.9 reveal the SiC n- and p-channel mobility equations with fitting parameters included.

$$mobility = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{nb}{N_{ref}}\right)^{\alpha}} \quad 4.5$$

Table 4.3 SiC Mobility Model Parameters

	μ_{min}	μ_{max}	N_{ref}	α	Constant
SiC n [29]	0	977	1.17E17	0.49	1140
SiC p [30]	0	113.5	2.4E18	0.69	175

Table 4.4 SiC n-channel Initial Mobility Equations

SiC n-channel			
$mun0 = \frac{977}{1+\left(\frac{nb}{1.17E17}\right)^{0.49}}$	(4.6)	$mup0 = 175$	(4.7)

Table 4.5 SiC p-channel Initial Mobility Equations

SiC p-channel			
$mun0 = 1140$	(4.8)	$mup0 = \frac{113.5}{1+\left(\frac{nb}{2.4E18}\right)^{0.69}}$	(4.9)

In addition to the SiC mobility equations, the intrinsic carrier concentration of SiC was researched and updated, and is shown in Equation 4.10 [3].

$$ni_{SiC} = 1.7E16 \cdot \left({templim^{1.5}}/{e^{(20800/templim)}} \right) \quad 4.10$$

4.1.3 Temperature dependence of mobility

Temperature dependence was added to the mobility equations using the ratio shown in Equation 4.11, and implemented in Equations 4.12 through 4.21. The temperature exponent is based on [3] for the silicon electron and hole, as well as the SiC electron models. The exponent for the silicon carbide electron mobility is dependent on the doping concentration of the drift region, and is implemented through the value $beta$, shown in Equation 4.14 [29]. Since the SiC p-channel mobility equation includes temperature dependencies for every fitting parameter, the entire hole mobility is calculated in three steps shown through Equations 4.18 through 4.21 [30].

$$trat = \frac{t_{nom}}{templim} \quad 4.11$$

Table 4.6 Silicon n- and p-channel Mobility Temperature Dependence

Electron Mobility	Hole mobility
$mun = mun0 \cdot (trat)^{2.42}$ (4.12)	$mup = mup0 \cdot (trat)^{2.2}$ (4.13)

Table 4.7 Silicon Carbide Mobility Temperature Dependence

	Electron Mobility	Hole Mobility
n-channel	$mun = mun0 \cdot (trat)^{beta}$ (4.14)	$mup = mup0 \cdot (trat)^{2.5}$ (4.15)
p-channel	$mun = mun0 \cdot (trat)^{2.7}$ (4.16)	$mup = \frac{mup1}{1 + \left(\frac{nb}{mup2}\right)^{mup3}}$ (4.17)

$$beta = 1.54 + \frac{1.08}{\left(1.0 + \left(\frac{nb}{1.14E17}\right)^{1.35}\right)} \quad 4.18$$

$$mup1 = 113.5 \cdot (trat)^{2.6} \quad 4.19$$

$$mup2 = 2.4E18 \cdot \left(\frac{1}{trat}\right)^{2.9} \quad 4.20$$

$$mup3 = 0.69 \cdot (trat)^{0.2} \quad 4.21$$

4.2 Simulation Analysis

4.2.1 Parameter Extraction

The parameter extraction sequence's purpose is to provide an efficient, practical way to fit the model to a specific set of data. The extraction sequences created in this work were designed based upon the data set provided for each case. Therefore, there is still room to expand and improve each extraction sequence by gathering more data. Parameters not used in each

extraction sequence are considered minor effects and will not be discussed, as their values when changed, provided negligible effects.

Silicon

This sequence was designed based on the data set from the IXYS IXBK55N300 IGBT datasheet, and the extraction sequence from [19], [20], [32]–[35]. The measurement column in Table 4.8 describes a specific data set to fit. The model value describes the value to plot when overlaying the measured data. The parameter symbol is the parameter to adjust when fitting the simulated value to the measured data. The fitting target is a description of the measured data used when adjusting the simulated value to the measured data. A detailed explanation of each step presented within this parameter extraction sequence is listed below.

Table 4.8 Si IGBT Parameter Extraction Sequence

Step	Measurement	Model value	Parameter symbol	Fitting target
1	Turn off temp scaling	--	Ending in exp or co	Set equal to 0.0
2	Breakdown Voltage	$bvcbo$	bvf	Set equal to breakdown voltage
3	Cres	C_{gd}	$coxd$	Low V_{ce}
			V_{td}	Vce where Capacitance decreases
			nb	High V_{ce}
			A_{gd}	High V_{ce}
4	Coss	$C_{dsj} + C_{gd}$	a (if not known)	Entire Coss graph
			pb	Low V_{ce}
			nb	High V_{ce}
5	Cres	C_{gd}	A_{gd}	High V_{ce}
6	Ciss	$C_{gd} + C_{gs}$	C_{gs}	Entire Ciss graph
7	Ice vs V_{ge}	i(c)	vt	Turn on voltage
			kp	Saturation region
8	Gate charge	G	wb	Miller cap.
9	V_{ce} vs V_{ge}	V_{ce}	$tauhl$	V_{ce} parallel to y-axis
			$voff$	V_{ce} parallel to x-axis
10	Ice vs V_{ce}	i(c)	rs	Linear region
			kf	Linear region
			$voff$ (if needed)	Offset voltage

Table 4.8 Si IGBT Parameter Extraction Sequence (Cont.)

Step	Measurement	Model Value	Model Parameter	Fitting Target
			kp (if needed)	Saturation region
11	V_{ce} vs V_{ge}	V_{ce}	$tauhl$ (if needed)	Vge intercept
12	Ice vs V_{ge}	i(c)	$theta$	Saturation region
13	Ice vs V_{ce}	i(c)	kf (if needed)	Linear region

1) The first step in a room temperature parameter extraction sequence is to turn off all the temperature scaling dependencies in the model. This is done by setting all temperature scaling parameters to zero.
2) Step two consists of estimating the parameter bvf using the reported breakdown voltage of the IGBT. Set $bvcbo$ to the breakdown voltage of the device and solve for bvf using Equation 3.24.
3) Measurement Cres: In step three, $coxd$ is determined by the maximum value of the Cres curve from the datasheet [20]. Next, vtd is determined by adjusting the simulation to the point at which C_{gd} becomes depleted. The parameter nb is used to match the capacitance at high V_{ce}. The typical maximum doping concentration of the epitaxial base region is 2.0e14 cm^{-3}, therefore when verifying the model to a Si IGBT, nb should not surpass this value [3]. If nb reaches 2.0e14 cm^{-3}, then A_{gd} can be increased until the simulation overlays the targeted measured data.
4) Measurement Coss: The goal of step four is to overlay the measured and simulated output capacitance. First, use a to adjust the entire shape of the Coss graph. As pb approaches infinity, C_{dsj} becomes flat. As pb approaches zero, C_{dsj}, at 0 V_{ce}, becomes large. Adjust pb to match the low V_{ce} section of the Coss measured data. Next nb is altered to adjust the output capacitance at high V_{ce} values until the simulation overlays the measured data.

5) Measurement Cres: Step five only needs to be done if nb is changed in the process of simulating Coss. Adjust A_{gd} to match the simulated C_{gd} plot to the measured Cres curve.
6) Measurement Ciss: Since Ciss is the sum of C_{gd} and C_{gs}, C_{gs} can be altered to optimize the input capacitance. Adjust C_{gs} to match the simulated plot to the measured Ciss curve.
7) Measurement Ice vs V_{ce}: vt is found by locating the intercept of the tangent to the Ice vs V_{ge} graph, while V_{ce} is held at a constant value. Next, kp is optimized until the simulated value of Ice is parallel to the measured data.
8) Measurement Gate Charge: During this parameter extraction process with the measured data available, the gate current was assumed to be constant. Therefore, for non-constant gate current measurements, this step will need to be revised. Use wb to alter the simulated gate voltage so that the end of the simulated miller capacitance, or where the voltage begins to increase again, overlays the measured data.
9) Measurement V_{ce} vs V_{ge}: This step can be broken into two stages. Adjust $tauhl$ so the portion of V_{ce} that is parallel to the y-axis overlays the measured V_{ce} vs V_{ge} data. Secondly, adjust $voff$ so the portion of V_{ce} that is parallel to the x-axis conforms to the measured data.
10) Measurement Ice vs V_{ce}: First adjust rs so that the simulated Ice plot is parallel to the highest measured gate voltage curve. Adjust kf so that the simulated lower gate voltage curves match the measured data. $voff$ and kp can be adjusted in this step if the turn on voltage or saturation current simulation overlay to the measured data is not acceptable, respectively. The parameter vt can be verified via the lowest gate voltage curve. Also, Ice vs V_{ge} curve should be verified if vt, $voff$, or kp is changed.

11) Measurement V_{ce} vs V_{ge}: If $voff$ was adjusted in step ten, $tauhl$ must be optimized following the same procedure in step nine.
12) Measurement Ice vs V_{ge}: Adjust $theta$ so that the simulated saturation current is most like the measured data. If any adjustments are made, it should be kept slight, since kp and $tauhl$ both affect the same area of the V_{ce} vs V_{ge} plot.
13) Measurement Ice vs V_{ce}: This step allows for the final adjustments to be made. Since $tauhl$ has been changed in step eleven , kf might need to be adjusted to accompany the changes within the output characteristics.

Silicon Carbide

Since the SiC data available was not as thorough as the available Si data, a trimmed version of the parameter extraction process was developed. This trimmed parameter extraction consists of a list of model parameters to adjust to overlay the simulated data to the measured data. This organization of parameters is separated into three steps and also details certain parameters that effect specific areas of data plots. Table 4.9 shows the trimmed parameter extraction sequence to verify the IGBT model to SiC data, for both n- and p-channel configurations.

For any DC measurements, the parameter relations and processes to verify the model are the same as in the silicon parameter extraction sequence. A general list of what parameters to adjust while simulating DC data is provided in step 1. The turn-off transient under an inductive load test circuit was readily available in SiC IGBT journal and conference papers [8], [12], therefore it was the method to verify the dynamic characteristics of the devices. Steps 2 and 3 provide the parameters to adjust while simulating the two segments of the turn-off transient. The first time segment, T1, describes how to simulate the turn-off transient immediately before the

tail current. The second time segment, T2, describes how to adjust the tail current of the IGBT turn-off transient.

Table 4.9 SiC IGBT Parameter Extraction Sequence

Step	Measurement	Parameter Symbol	Fitting Target
1	DC	$tauhl$	Shape of graph
		kp	Saturation region
		kf	Linear region
		nb	Entire graph
		$voff$	Offset voltage
		vt	Lowest V_{ge} simulation.
		rs	Linear region
		a	Entire graph
		agd	Entire graph
		$theta$	Saturation region
2	Turnoff T1	All capacitances	Initial decrease in Ice
		vtd	Initial decrease in Ice
		a	Shape of turn off current
		agd	Shape of turn off current
		$tauhl$	Entire graph
3	Turn off T2	$tauhl$	Size of tail
		nb	Shape of tail
		wb	Shape of tail
		agd	Shape of tail
		a	Shape of tail
		bvn	Shape of tail

4.2.2 Implementing Debugging Parameters and Tools

If a model does not converge during a simulation, a process called “debugging” is required. As the name suggests, this is a process to determine where a problem lies within the model. User parameters, or debugging parameters, are tools that the modeler can implement to effectively turn off parts of the model. Typically, the first part of the model to turn off is any section that requires a calculation of a derivative, leaving what is called the DC part of the model. The lack of derivatives dramatically reduces the complexity of the simulation, and can single out which portion of the model is causing the convergence issues. Other types of

debugging parameters can be implemented; however, they are generally used to turn off or on certain sections of the model, reducing the complexity of the simulation.

Another debugging tool commonly used is a voltage probe. Voltage probes are implemented at a specific node to view the calculated voltage at each iteration. These probes are particularly beneficial since they do not add any complexity to the simulation. To insert a voltage probe, a branch is placed around the inquired node, and the current of that branch is set to zero. The simulator stores the voltage value at every iteration, enabling the user to then print these values during the simulation. If a specific voltage is approaching infinity, has large gaps, or is cyclic, the user may note the problem and investigate further.

Message statements are basic tools that make the debugging process more efficient. If a certain condition is met, and it is also a condition of interest when determining convergence issues, a message can be printed during the simulation alerting the user. Message statements can also employ the option to stop the simulation, saving time and allowing the modeler to view what state the model was in at the time the simulation failed. In Verilog-A, the message statement can be formatted following Equation 4.22, where the output would read "The value of parameter x is #." The number sign in the output statement represents the current value of x.

$$\$strobe("The\ value\ of\ parameter\ x\ is\ \%f"\ , x) \tag{4.22}$$

This output statement is designed to print real numbers, and is classified as such by the letter after the percent sign. Verilog-A has other definitions for different types of numbers, but they will not be described here, as real numbers were the only values of interest in this work.

Modifying the simulation conditions can also help simplify the debugging process. Simulating with all terminals grounded is the first simulation that should be computed. This ensures that any existing issue is within the model, not a complication of the test conditions.

Next, DC simulations can be computed. Capacitance computations should not be simulated before the DC simulation has completed. This is due to the fact that charges are required to compute capacitances, and therefore time derivatives of node voltages are required to be computed. As stated previously, this dramatically increases the computation time required.

Chapter 5 Creating a Verilog-A Compact model through Paragon 2.0

5.1 Necessity of a Verilog-A Compact models

A compact model simulates the electrical behavior of a component, and is then utilized within a circuit simulator [13]. As such, these models are the backbones of circuit designs created by both students and professional engineers. Also, the circuit simulation can only be as accurate as the backbones supporting it. Therefore, for the best outcome within a design project, accurate compact models are required.

Verilog-A is a hardware description language, or HDL, and has been updated to specifically benefit compact modeling. Before HDLs dominated the realm of compact modeling, component models written for circuit simulators were commonly written in C. This required hand coding derivatives as well as handling the simulator interface, which included tasks such as: reading model parameters, initializing values, loading the Jacobian matrix, and others. These error prone and extensive tasks are now obsolete to the modeler's conscience, as Verilog-A compilers, and the construct of the language, easily completes these tasks. For this reason, Verilog-A compact models are portable between simulators, a feature unimaginable with models written in C. Although C component models are fast, commercially available simulator compilers have improved to provide a Verilog-A model that is only 5 – 20% slower than C models. This margin will only decrease as compilers continue to improve [13].

Verilog-A is also a widely used scripting language among circuit designers, therefore a large percentage of designers are in need of Verilog-A compact model. If the model is needed in another language, or for another simulator, e.g. Spectre or HSpice, Paragon 2.0 is the program ready for students to easily convert their model to fit the designers' needs.

5.2 Utilizing Paragon 2.0

Paragon 2.0 is an educational tool that allows a user to create a model by drawing an equivalent circuit and correlating the appropriate equations to the branches within the circuit. This allows the user to visualize the model in a more tangible way, opening circuit and device modeling to many users from multiple backgrounds. In addition to the visualization benefit, this tool takes the burden of most syntax issues away from the user, allowing the focus to be on the physics of the circuit or device rather than on the computer engineering skills [36], [37].

To draw the equivalent circuit, Paragon 2.0 provides branches as the building blocks. A single branch is shown in Figure 5.1. It has two nodes on either side, one which is the positive node, and the other is negative. This visual tool also provides an ability to comment, reminding the modeler of the purpose of the branch. The arrow in the Figure 5.1 represents what direction current is flowing. There is also the option to select symbols to show inside the box, further indicating what purpose the branch is to serve. For example, a resistor pattern can be chosen to be viewed inside the box to show that the branch symbolizes a resistive current.

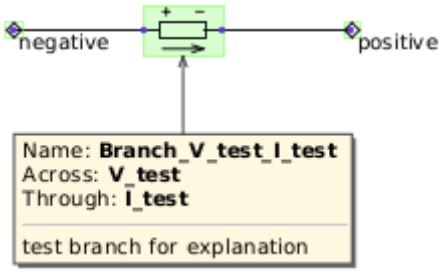


Figure 5.1 A branch with both positive and negative nodes labeled as “test” and with a comment of “test branch for explanation.”

The Verilog-A version of this IGBT model was created by taking the MAST code and creating an equivalent circuit to match the formulation of the model within Paragon 2.0. As stated in Chapter 4, the equation section within the MAST code describes how current flows

through each node, detailing an equivalent circuit. Once this basic frame of the model is visualized, Paragon 2.0 allows the user to create separate logical sections including: Parameter and Object Declarations, Analysis Initialization, Model Sequential Code, Branch Equations, and System Equations. There are other options within the Paragon 2.0 program, but only the ones used within this work will be discussed. This breaks the code into logical pieces, easier for future students to see and develop better coding techniques, or easily expand a section of the behavioral model, progressing the model's accuracy.

Within Paragon 2.0 there are multiple ways to declare a certain value, or piece of the model. With the IGBT model, Parameter and Object Declarations are the only declarations used within Paragon 2.0. A Parameter Declaration is an option the end user can set and change within the interface of the device model. As an explanation, cgs is declared a Parameter. An Object Declaration is a value that can be made a function of other values. For example, the breakdown voltage is a function of Parameters and constants. So the breakdown voltage is declared as an Object. Objects can also be a function of currents and voltages calculated within the model. As an example, vgs is declared as an Object, as it is a function of the voltage at the Gate terminal and the voltage at the Emitter terminal.

The Analysis Initialization section reduces the amount of equations calculated at every instance of the simulation. Objects that are only dependent on constants and model parameters are inserted in this section. This entire portion is only calculated once at the beginning of the simulation. This is the equivalent of the parameter section in MAST code. This reduces the complexity of the model by reducing the number of times certain equations are solved. Within the Analysis Initialization section, any Object can be defined as long as it does not depend on

variables. A variable in this definition would be any voltage or current flowing through any of the branches.

The Branch Equation segments are in place to assign which current is flowing through that specific branch. In Paragon 2.0 there is always the same number of Branch equation segments as there are branches within the topology, or circuit. However, a defined current is not required. Left undefined, the model assumes the current is zero through that branch. This is a handy tool when debugging the model, as it allows the user to view the value of the voltage through that specific branch. A branch is named following Equation 5.1, where $name$ is the word used to describe the branch. When calling the value of the voltage of a branch within an equation, Equation 5.2 will be use. These segments are the equivalent to the equations section in the MAST code.

$$Branch\_V\_name\_I\_name \tag{5.1}$$

$$V\_name \tag{5.2}$$

Model Sequential Code segments are where the equations that depend on variables are defined and solved. As the name suggests, they must be coded in a sequential order. However, the user can create as many segments as needed. This is to aid in the organization of the model, and allows the user to visualize what is being calculated when. These segments are the equivalent to the values section in MAST models.

The last segment used within this work is the System Equation segment. This component of the model defines all variables. Earlier, variables were defined as voltages and currents for understanding the difference in the equations that can be defined in the Analysis Initialization versus the Model Sequential Code segments. The true definition of variable, in terms of modeling, is a value that is defined by a simultaneous equation. For every variable within a

model, a simultaneous equation that contains this variable is required. The only variable, in this true definition, within the IGBT model is $qceb$, or V_qceb in terms of the topology and Paragon 2.0 format. The arrangement of V_qceb will be discussed in the following section.

5.3 The Verilog-A IGBT Model through Paragon 2.0 tool views

Figure 5.2 shows the topology of the model, as viewed in Paragon 2.0. To aid in the simplicity of the model, additional branches were created, traveling the opposite direction, for the p-channel model. These p-channel Branches are represented by the purple fill color within Figure 5.2. When the p-channel model is selected, the n-channel Branches become inactive, and the p-channel branches become non-zero. This reduces the amount of mistakes that are possible within the code without adding any complexity to the simulation.

The code is broken up into two Analysis Initialization segments, seven Mode Sequential Code segments, one System Equation segment, and 23 Branch Equations for both n-channel and p-channel options. The Analysis Initialization segments are separated by dependence on parameters. The first segment defines values that only depend on real numbers, such as key constants that are used throughout the model. The second segment utilizes Parameters and includes the mobility model for each material and channel. The Model Sequential Code segments are labeled: voltages, widths and charges, mufact, imos, rb, currents, and avalanche multiplication factor. These code segments are labeled in the manner that explains their purpose and what is calculated within each. When the code is exported to a Verilog-A format, the names of the segments are implemented as comments.

To define the one variable within the IGBT model, $qceb$, the System Equation section is added to solve the simultaneous equation set, shown in Equation 3.17. Simultaneous equations can be implemented numerous ways, depending on what is to be achieved. Within Paragon 2.0, a

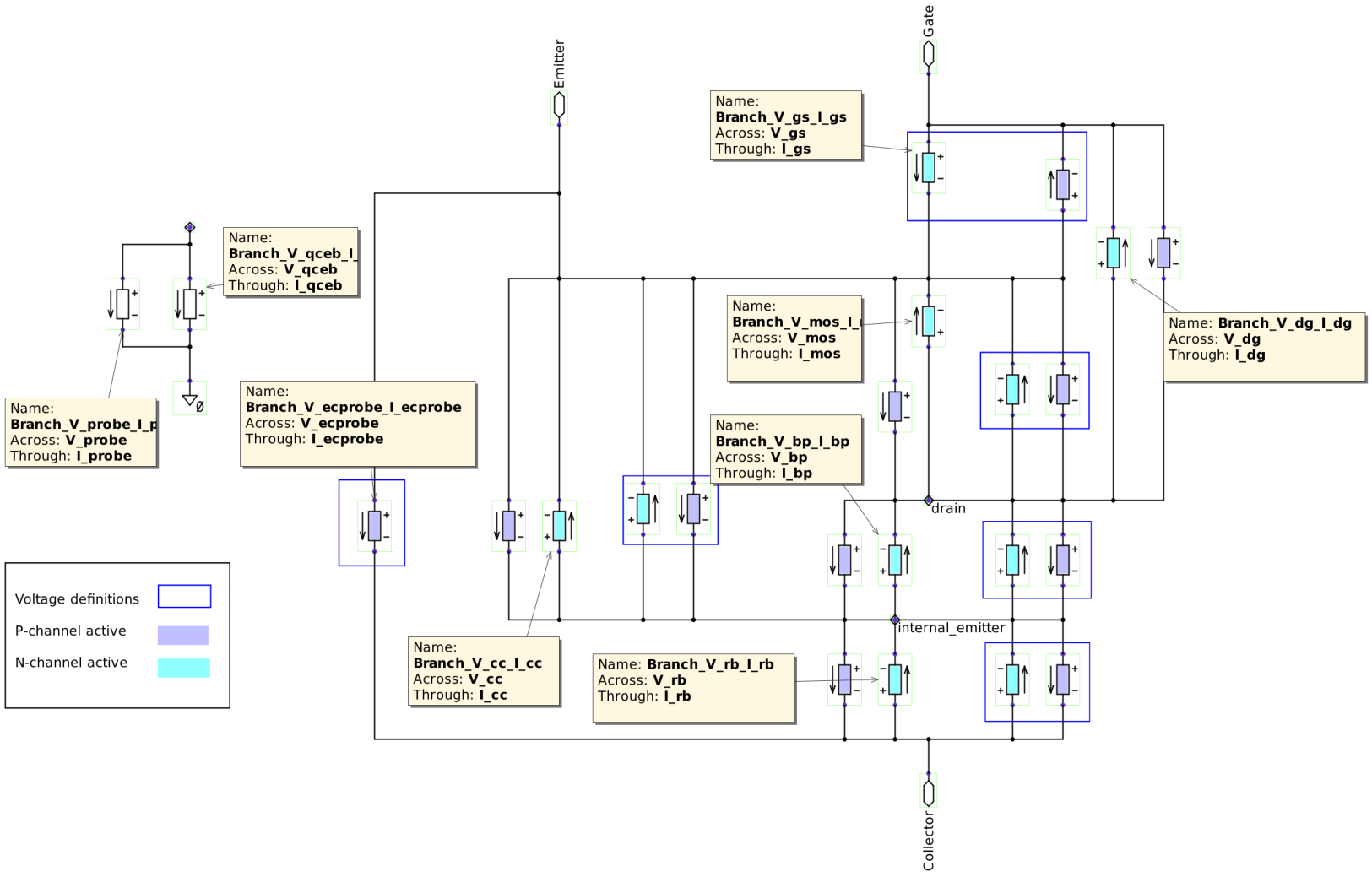


Figure 5.2 Topology of IGBT model within Paragon 2.0, with terminals Gate, Emitter, and Collector

branch is used to define the voltage V_qceb, which represents $qceb$. With the variable now identified, the branch and simultaneous equation can be defined. To solve for V_qceb, a floating branch is inserted into the topology and connected to ground, where current is flowing from the floating node to ground. (A floating node is a node that is not connected.) The current for this floating branch is set to zero, i.e. I_qceb is set to zero. With I_qceb set to zero, Equation 3.17 can be rewritten, as shown in Equation 5.3. Now, Equation 5.3 can be set to I_qceb, which creates Equation 5.4.Equation 5.4 is then implemented within the Systems Equation segment as the simultaneous equation defining V_qceb. (This is the same voltage probe technique as explained in Section 4.2.2.)

$$0 = veb + voff - vebj \tag{5.3}$$

$$I\_qceb = veb + voff - vebj \tag{5.4}$$

This equation is valid and solvable because veb is the known node voltage within the model, $voff$ is a parameter, and as stated above, I_qceb is zero. This only leaves one variable to solve for in the equation: $vebj$. As shown in Equations 3.18 through 3.22, solving for $vebj$ also defines V_qceb. This correlates with the description of the MAST simultaneous equation of solve $qceb$ such that $vebj$ equals veb plus or minus $voff$. Following the MAST equations section, V_qceb is taken into account within the I_bp Branch.

Chapter 6 Results

The SiC IGBT model was verified with a Si IGBT, a SiC n-channel IGBT, and a SiC p-channel IGBT including temperature effects. The Si IGBT used to verify the model was an IXYS IXBK55N300 device, and was chosen due to its availability and average ratings. Due to the snapback phenomenon present within the device used for testing, the data used for verification was digitized from the IXYS IXBK55N300 datasheet. Both SiC devices were the most recently published at the time of this work, the SiC n-channel IGBT [8] and SiC p-channel IGBT [12] were chosen due to this reason. SiC n-channel and p-channel device data were digitized from [8] and [12], respectively, due to the lack of commercially available SiC IGBTs.

6.1 Si IGBT Results

The results from the parameter extraction, discussed in Chapter 4, are described here. The presentation of results will be in groups dependent on the testbenches.

The testbench used to simulate the output and input characteristics for both 25 and 125 ˚C is shown in Figure 6.1. To simulate the output characteristics, the Collector-Emitter voltage, Vce, was swept from 0 to 10 volts, and the Gate-Emitter voltage, Vge, is simulated at 5, 10, 15, and 25 volts. To simulate the input characteristics, the Collector-Emitter voltage was held at a constant value of 6 volts, and the Gate-Emitter voltage was swept from 0 to 10 volts.

Figure 6.2 shows the simulation results versus the measured results of the room temperature (RT) Si output characteristics. This result shows an acceptable match between measured and simulated data.

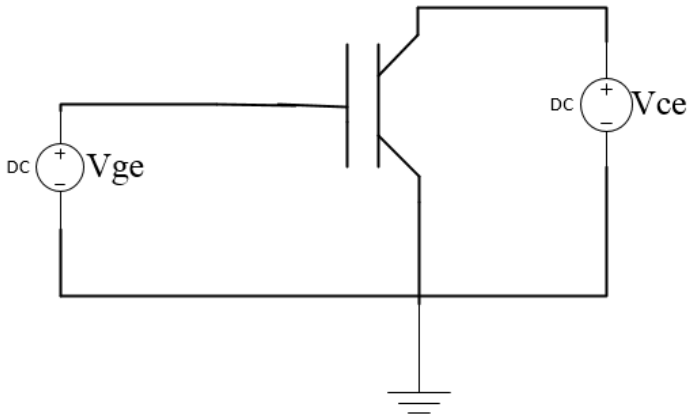


Figure 6.1 DC Testbench. Vce is swept and Vge is stepped at voltages described in text.

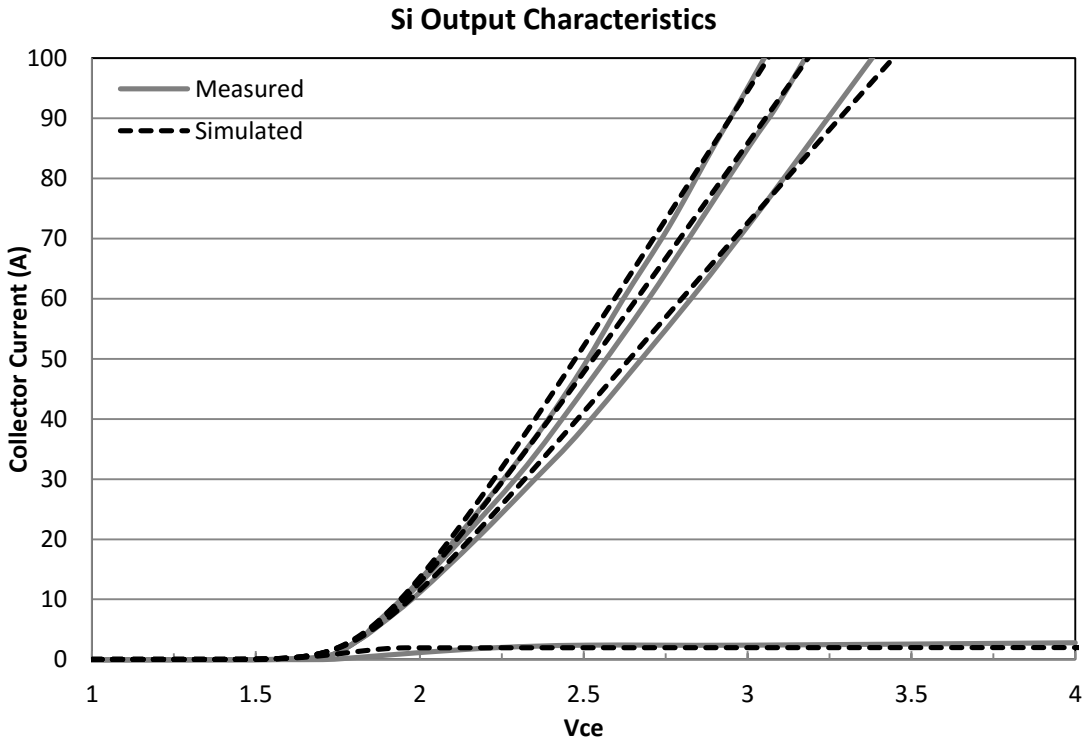


Figure 6.2 Si IGBT Output Characteristics at 25 ˚C.

Figure 6.3 shows the simulation results of the RT Si input characteristics. This measurement was used to extract the threshold voltage of the device. Since the gate voltage was swept, the approximate value of the threshold voltage is at the Vge intercept of the tangent to the measured collector current. Therefore, within this data set, the most important area for the simulation to match the measured data is between 4.5 and 5.5 volts. This area of simulation data is an agreeable match to the measured data. However, the slight separation between the measured and simulated Collector Current between 6 and 8 volts correlates to the tradeoff made between the output and input characteristics. The MOSFET transconductance parameter, kp, and the offset voltage, $voff$, were optimized between the two simulations.

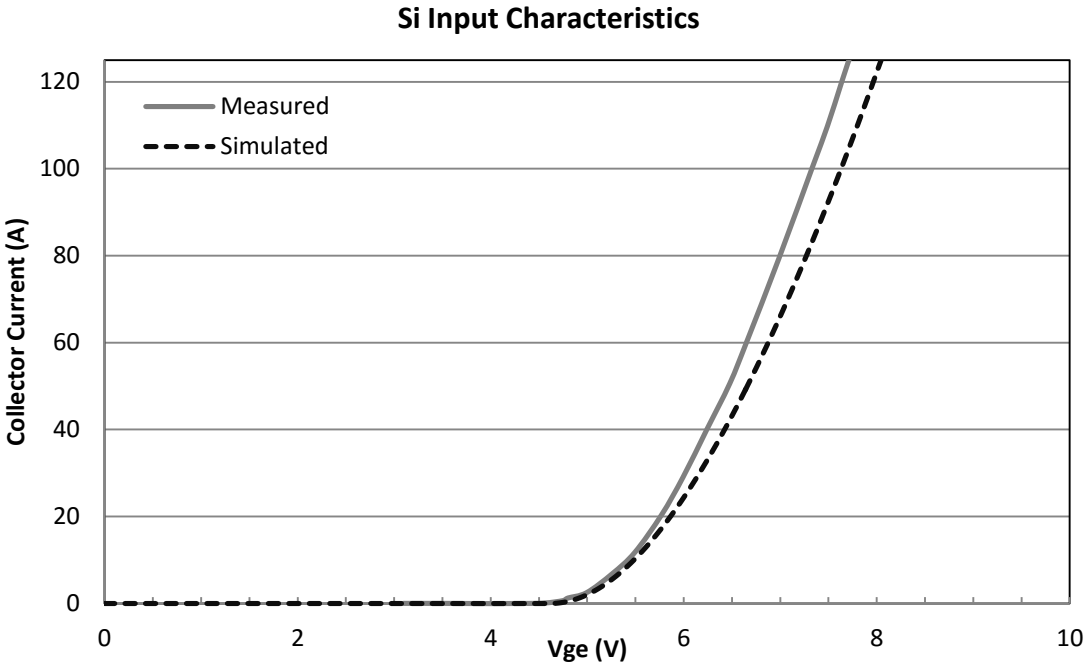


Figure 6.3 Si IGBT Input Characteristics at 25 ˚C.

Figure 6.4 displays the capacitance results of the Si IGBT model. To simulate the capacitances, the testbench utilized was similar to that of Figure 6.1. However, the Gate and the Emitter of the IGBT were shorted together and Vce was swept from 0 to 40 volts. C_{ies} is the sum

of C_{gs} and C_{gd}, and does not decrease with increasing Vce, in comparison to C_{oes} and C_{res}. This is due to the fact that the Gate-Emitter depletion region does not depend on Vce. Therefore, with increasing Vce, the depletion region across the Gate and Emitter does not increase. An increasing depletion region correlates to a reduction in capacitance, therefore, C_{ies} does not decrease [38]. This fact is modeled correctly in this work, as C_{gs} is implemented as a model parameter. C_{res} and C_{oes} decrease with the increase in Vce because the depletion region of the N- base is increasing with Vce. This can also be seen through Equation 3.6, as an increase in Vce leads to an increase in the depletion width, W_{gdj}.

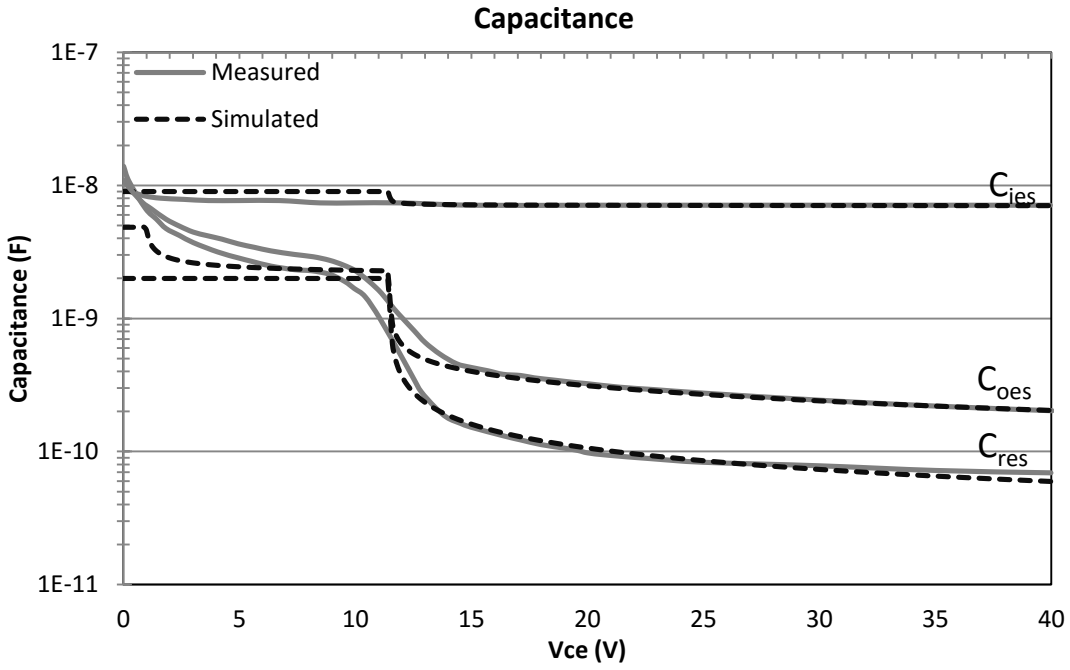


Figure 6.4 Si IGBT capacitance characteristics.

The second decrease in capacitance seen in Figure 6.4, at 10 volts, correlates with the expansion of the depletion region into the entire N- base region from the Gate-Emitter region of the IGBT. This transition takes place at Vce equals V_{td}, as explained in Chapter Four. When Vce is larger than V_{td}, the capacitance is accurately modeled. However, at Vce less than V_{td}, C_{ies} and

C_{oes} are decreasing, and an average capacitance is simulated. In this work, the value of C_{gd} is held at a constant until V_{dg} is larger than $-V_{td}$, as shown in Equation 3.6. For this reason, an average capacitance was simulated between 0 and 10 volts.

Figure 6.5 shows the on-state voltage, or Vce, versus the gate voltage, or Vge. To produce this simulated data the collector current was set to 55 A, the gate voltage swept from 0 to 15 volts, and the values of Vce were plotted. This graph shows an acceptable match between simulated and measured data. The slight disagreement with this plot is accounted for in the tradeoff between $voff$ and $tauhl$.

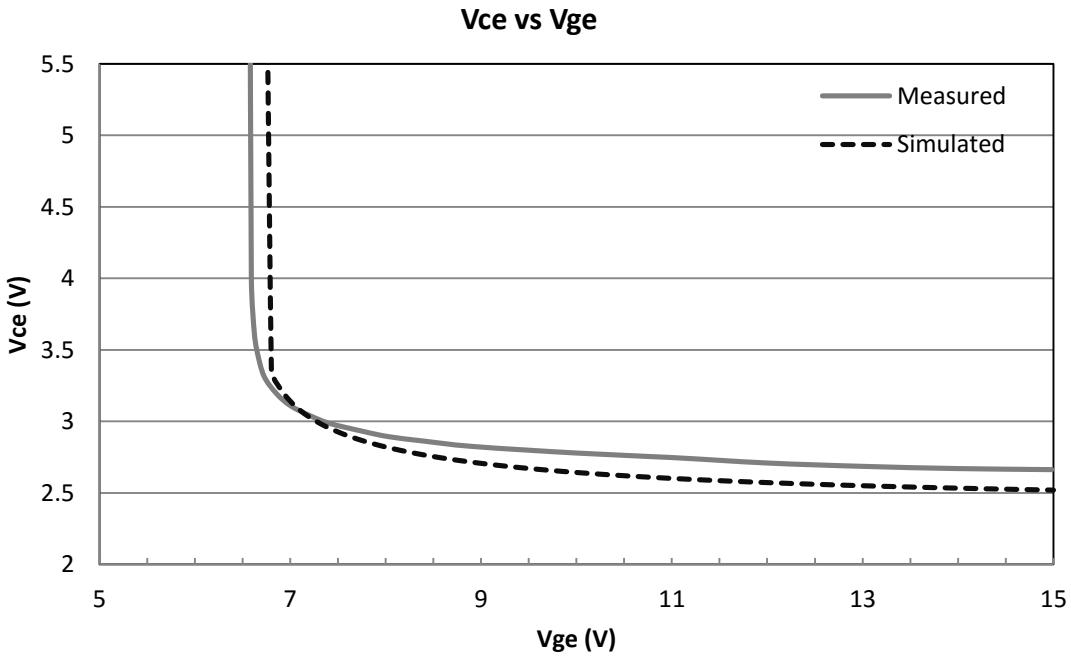


Figure 6.5 Si IGBT on-state voltage versus the gate voltage.

Figure 6.6 and Figure 6.7 depict the simulated gate charge measurement and result. This simulation was created via a resistive load testbench shown in Figure 6.6. The gate current was held constant, therefore, the value of time in this simulation is the equivalent of charge. Previous to the Miller plateau of the gate charge plot, both C_{gd} and C_{gs} terminal capacitors are being

charged; however C_{gs} is much larger than C_{gd} at this point [39]. Therefore, the approximation of C_{gs} used in Figure 6.7 affects this portion of the gate charge plot and is a tradeoff between the two characteristics. The Miller capacitance of the IGBT model, depicted in Figure 6.8, was accurately modeled; however, the second increase in gate charge was simulated at a lower slope than that of the measured gate charge. At this point, C_{gd} is dependent on V_{dg} as shown by Equation 3.6 through the value of W_{gdj}. This can be seen through the decreasing rate of gate charge produced in this simulation. This simulation was produced as a tradeoff between the capacitance and gate charge characteristics.

Figures 6.8 and 6.9 reveal the DC characteristics of the Si IGBT model at 125 ˚C. The same conditions and testbench was used to simulate these characteristics as Figure 6.1.

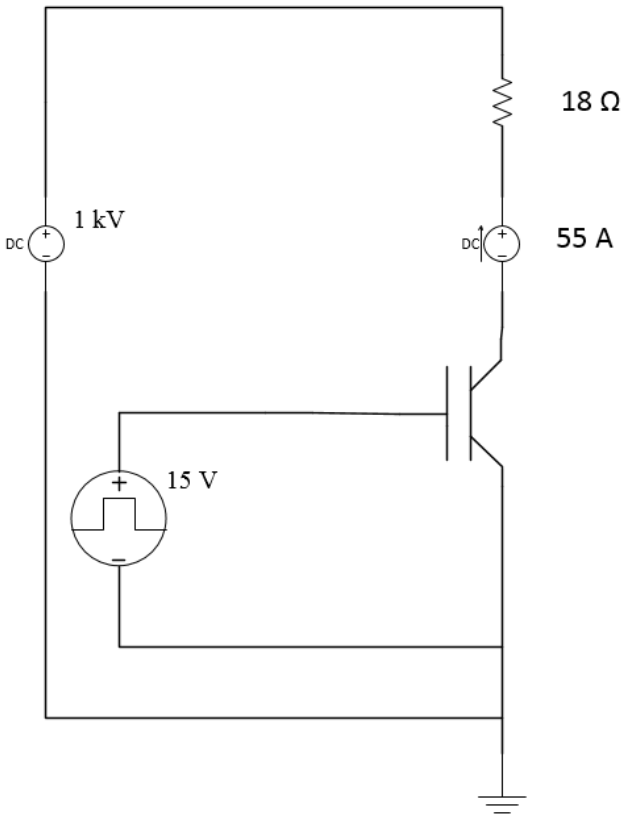


Figure 6.6 Resistive load testbench to simulate the Si gate charge plot.

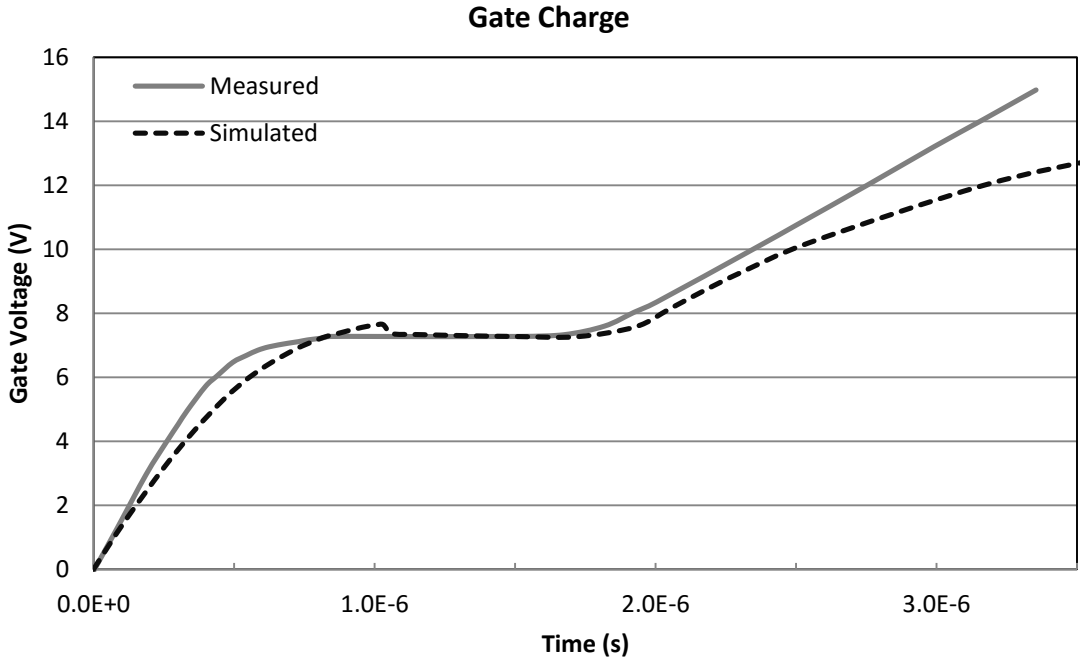


Figure 6.7 Si IGBT gate charge.

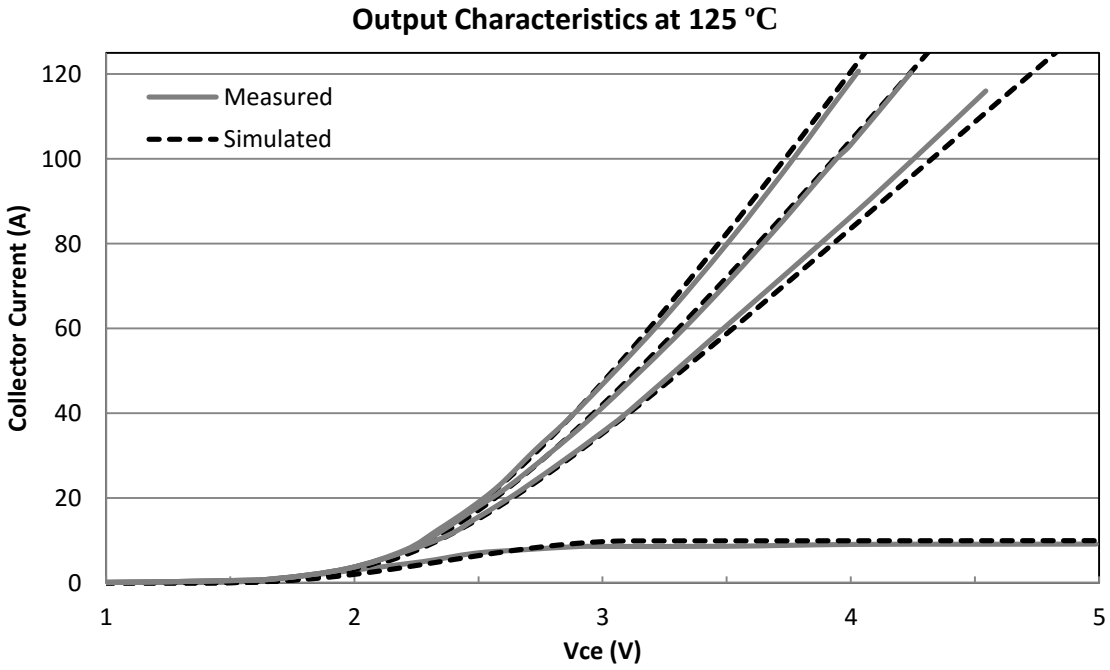


Figure 6.8 Si IGBT output characteristics at 125 ˚C.

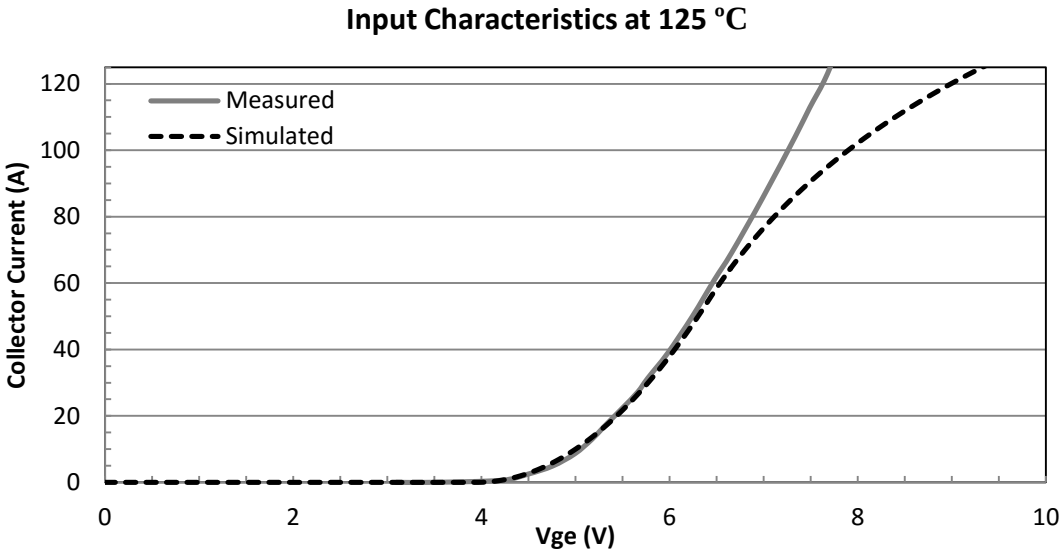


Figure 6.9 Si IGBT input characteristics at 125 ˚C.

6.2 SiC n-channel IGBT Results

Figure 6.10 displays the simulated result of the 12 kV SiC n-channel IGBT at room temperature [8]. The testbench to produce the output characteristic simulation is identical to Figure 6.1, however, the Gate-Emitter voltage was stepped at 10, 15, and 20 volts.

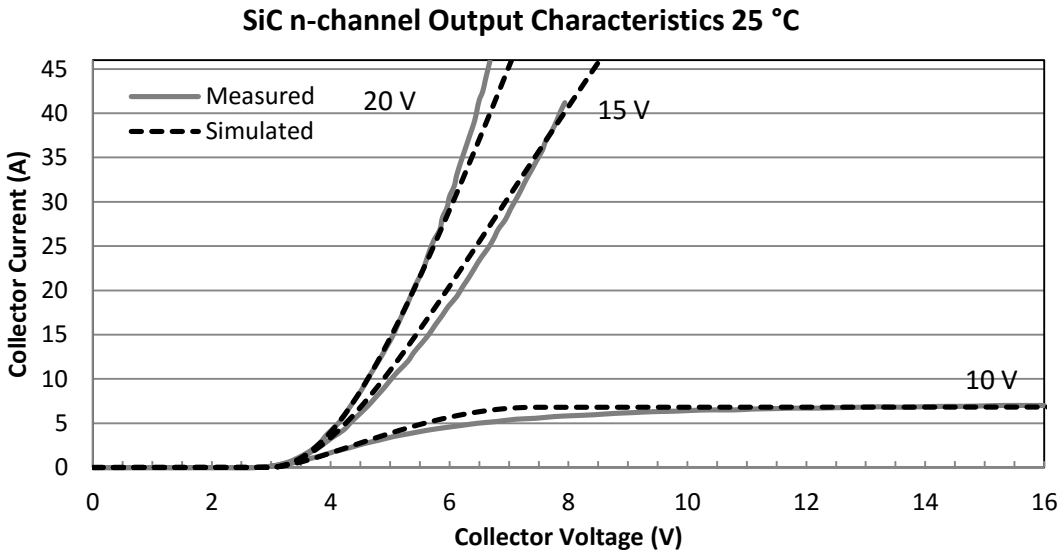


Figure 6.10 SiC n-channel IGBT output characteristics at room temperature.

The available transient data presented in reference 8 was turn-off voltage and current waveforms at room temperature and 125 ˚C. To produce these waveforms, the testbench shown in Figure 6.11 was used. Figures 6.12 through 6.15 present the simulation results for the turn-off voltage and current waveforms at RT and 125 ˚C, respectively. The SiC n-channel IGBT produced by reference 8 was a Field Stop IGBT, described in Chapter 2, and possesses a two stage voltage rise transient behavior. The initial rise in voltage, or “bump”, in Vce represents the removal of holes within N- base depletion region. The second rise in voltage occurs when the depletion region breaches the FS layer, i.e. the rise the voltage correlates with the reach-through condition. Once the depletion region surpasses the FS layer, the electric field becomes trapezoidal, and the voltage increases rapidly. The initial decrease in collector current corresponds to the removal of holes in the N- base region. The tail current represents the recombination of charges within the FS layer [31]. Due to the fact that this work does not possess equations to model the additional effects the FS layer produces, an average fit was produced. However, the tail current of this SiC n-channel IGBT was accurately modeled.

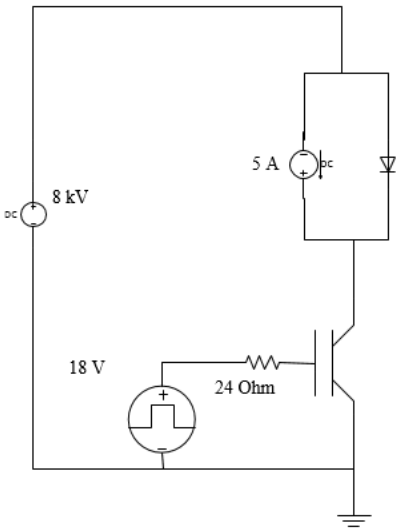


Figure 6.11 SiC n-channel IGBT clamped-inductive load testbench.

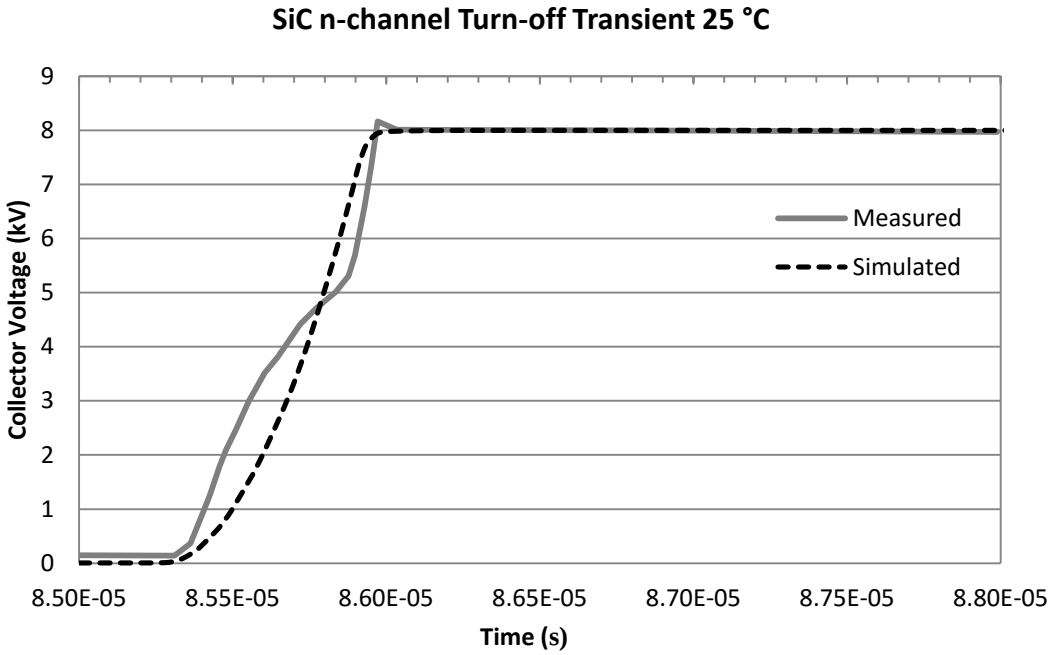


Figure 6.12 SiC n-channel turn-off voltage characteristics at 25 ˚C.

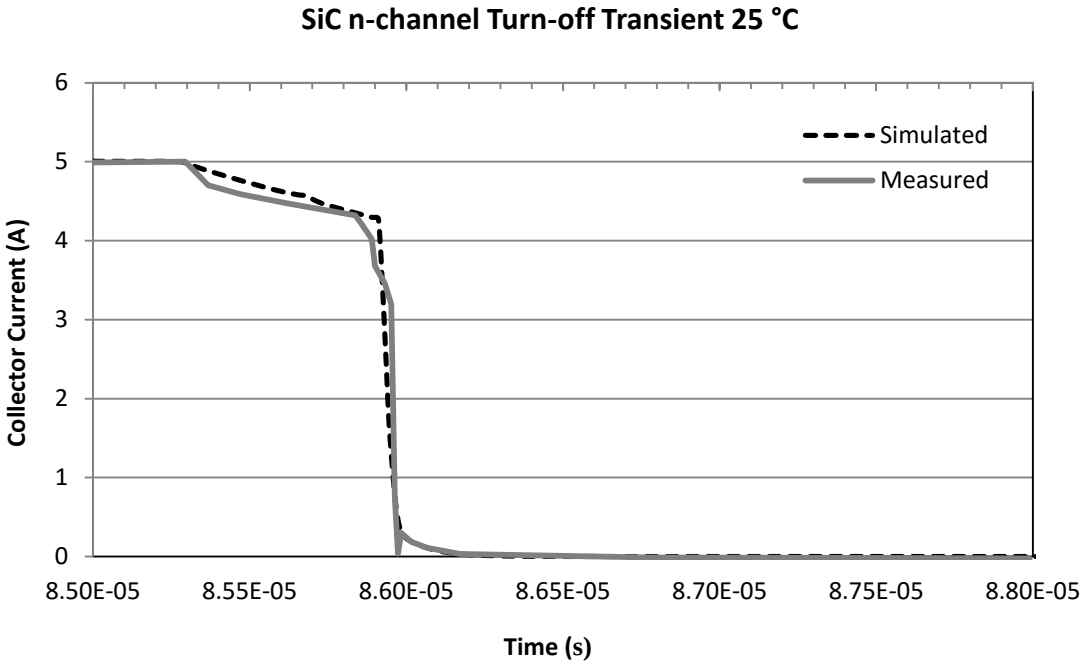


Figure 6.13 SiC n-channel turn-off current characteristics at 25 ˚C.

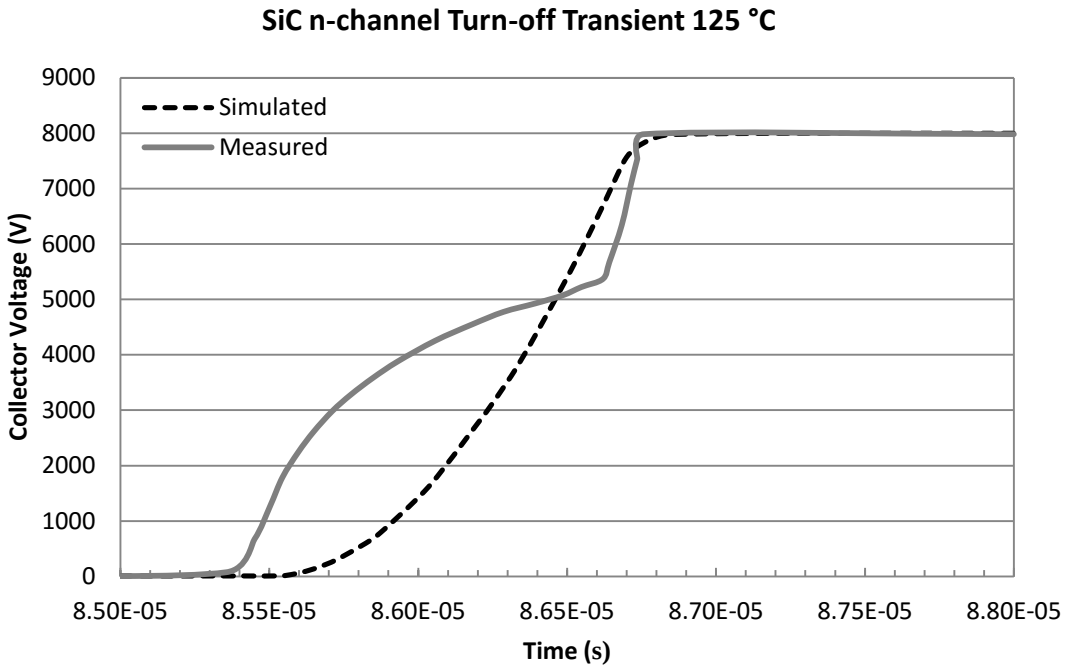


Figure 6.14 SiC n-channel turn-off voltage characteristics at 125 ˚C.

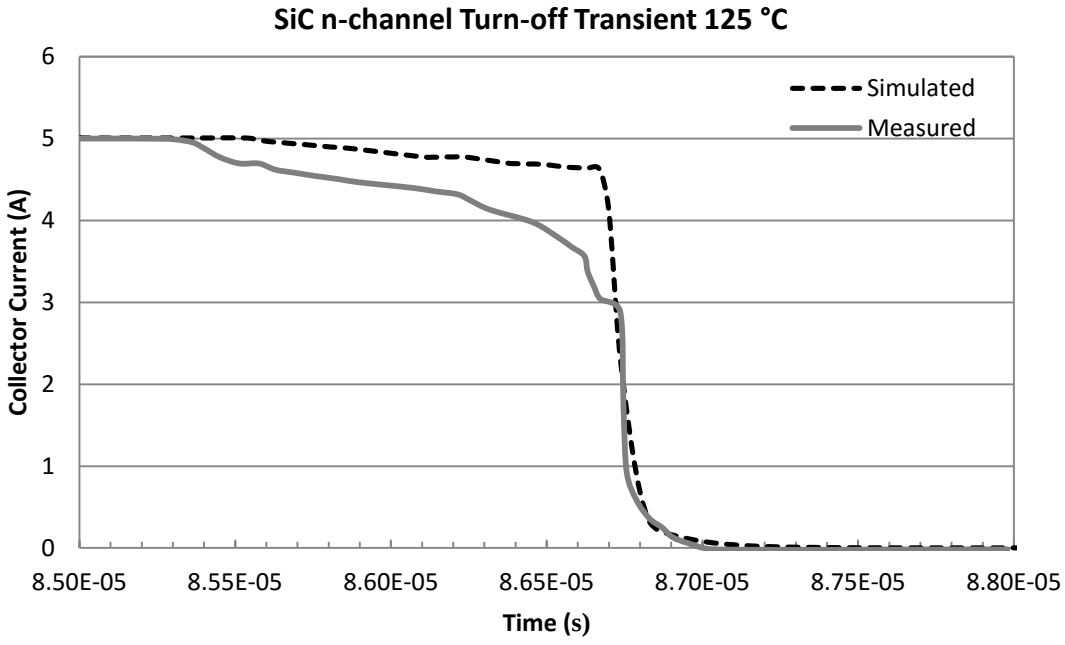


Figure 6.15 SiC n-channel turn-off current characteristics at 125 ˚C.

6.3 SiC p-channel IGBT Results

Figure 6.16 displays the simulated result of the 13 kV SiC p-channel IGBT at 250 ˚C [12]. The publication providing these results did not allow for an accurate digitization of the room temperature output characteristics. However, the previous results prove that this model is capable of producing accurate room temperature output characteristics. This data set provided gate voltage plots of 10, 15, and 20 volts, and Figure 6.1 is used to produce these results.

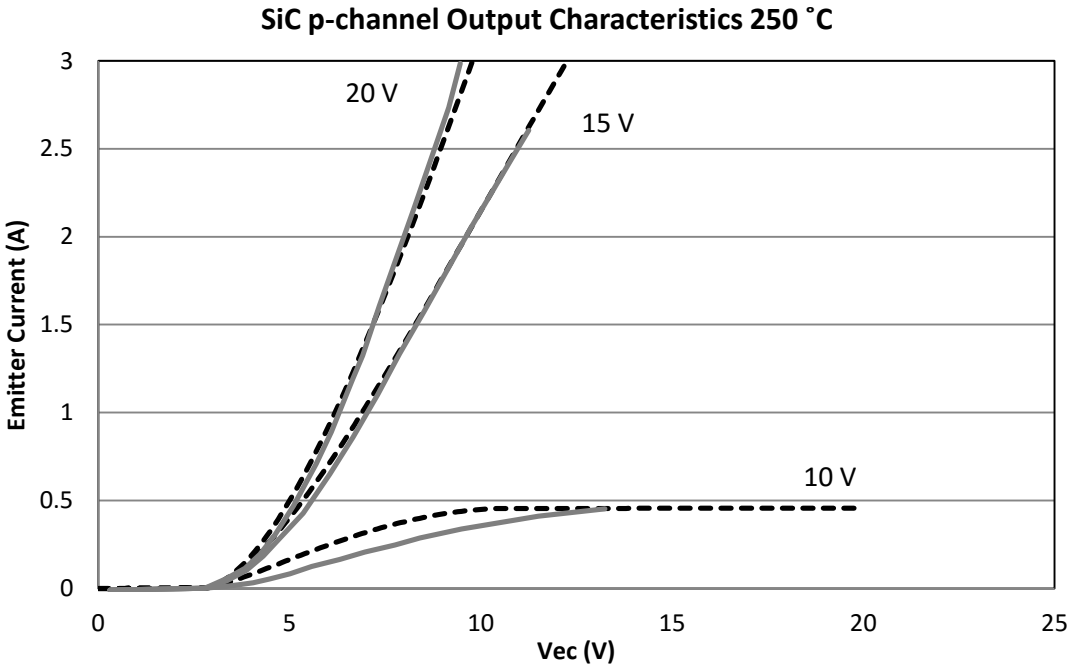


Figure 6.16 SiC p-channel output characteristics at 250 ˚C.

This publication also provided turn-off transient current and voltage waveforms at high temperatures. To further prove the temperature scaling capabilities of this model, the 250 ˚C and 150 ˚C data sets were used. However, since the output characteristics at 150 ˚C were not provided, the simulation result of the 150 ˚C turn-off transient was not fully optimized. This can be seen in the turn-off transient simulation of 150 ˚C in Figure 6.19. To produce the turn-off transient simulation, Figure 6.17 was utilized.

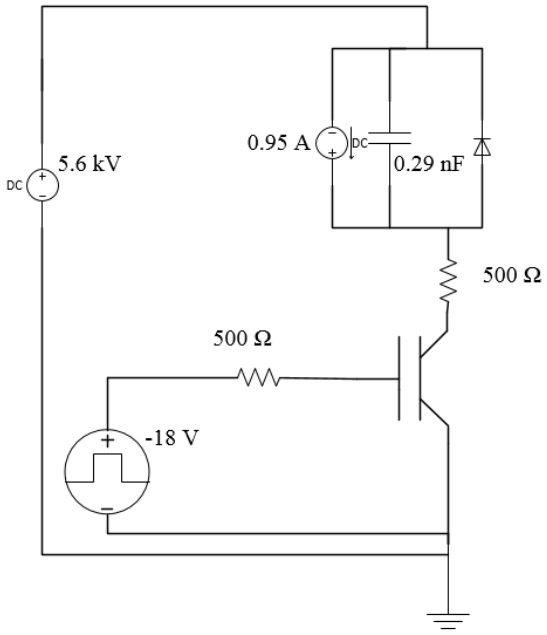


Figure 6.17 SiC p-channel clamped-inductive load testbench.

Figures 6.18 though 6.21 reveal the simulated versus measured results of the SiC p-channel IGBT. The SiC p-channel IGBT transient data provided was unique in the dramatic initial decrease in collector current. Also, unlike the SiC n-channel IGBT, the voltage rise of this device did not produce a "bump" in collector voltage. Vce does not produce a slow voltage rise transient since the load voltage applied to the IGBT was at 5 kV, much lower than the reported punch-through voltage of 11 kV [12]. (The punch-through voltage describes the voltage that is required to produce a depletion region that extends into the buffer layer.) Although the collector voltage is explained, it is thought that the large decrease in collector current is due to parasitics within the physical testbench [12]. To model non-ideal effects into an inherently ideal testbench, a capacitor with a value of 0.27 nF was placed in parallel with the load. This specific value of capacitance was added to the simulated testbench to achieve the initial decrease in collector current seen in Figure 6.20. (Again, the 250 ˚C simulation was matched to the data first.) While

simulating the turn-off response at 150 ˚C, the value of the parasitic capacitance was not altered, so this simulation has not been modified and, hence, the initial decrease in the simulated collector current does not match the data provided.

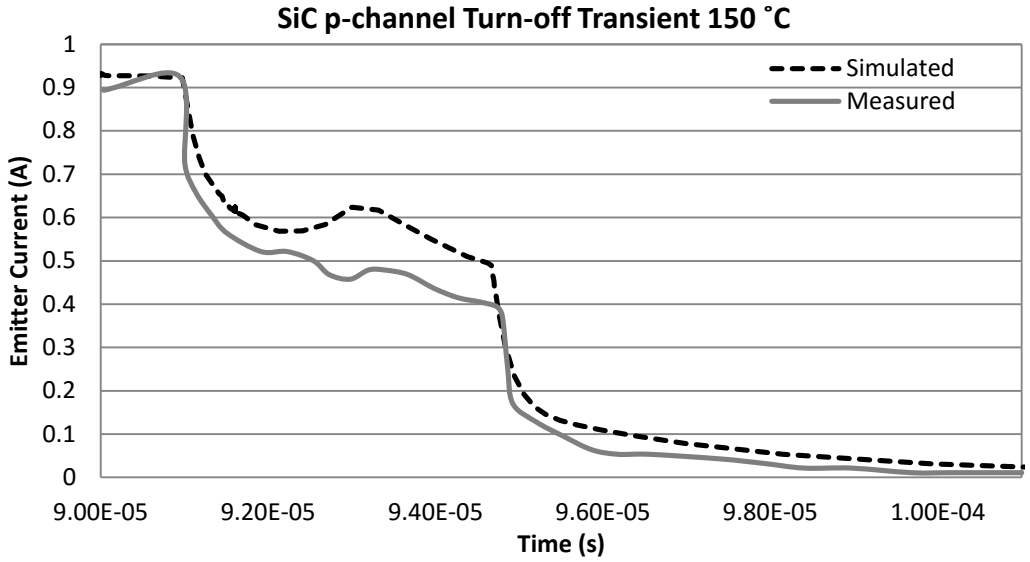


Figure 6.18 SiC p-channel turn-off current characteristics at 150 ˚C.

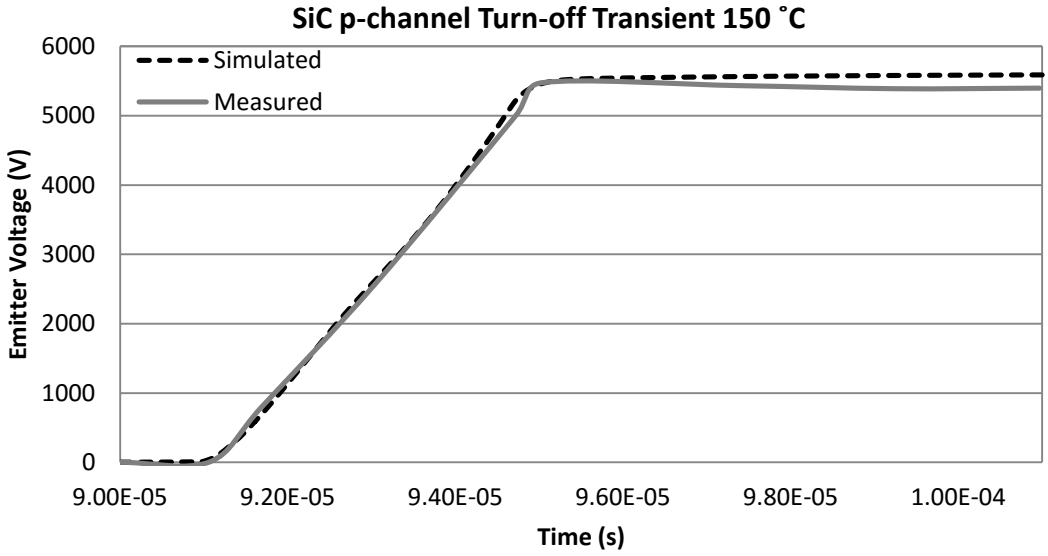


Figure 6.19 SiC p-channel turn-off voltage characteristics at 150 ˚C.

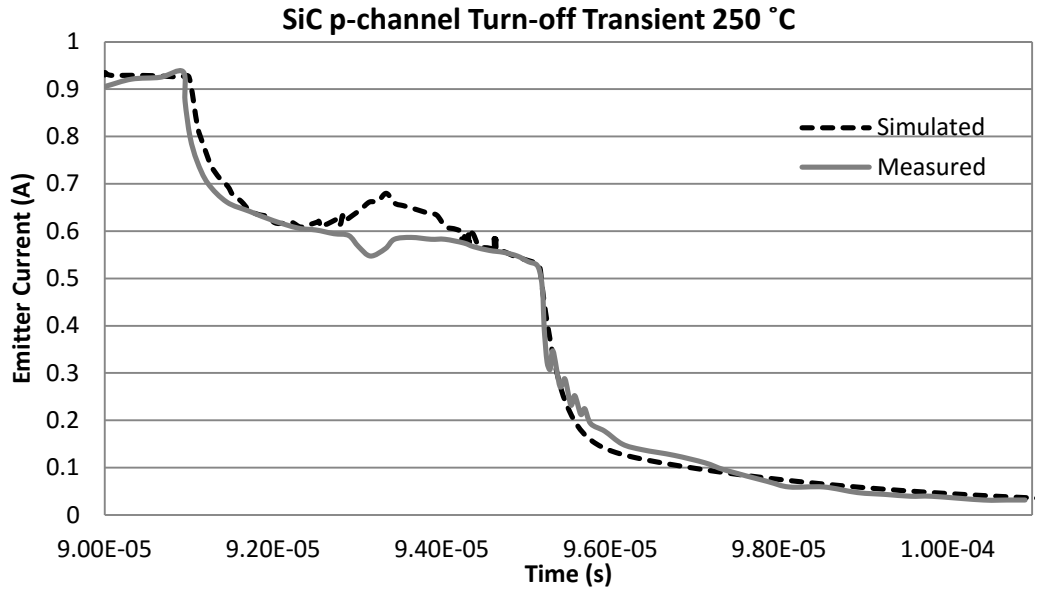


Figure 6.20 SiC p-channel turn-off current characteristics at 250 ˚C.

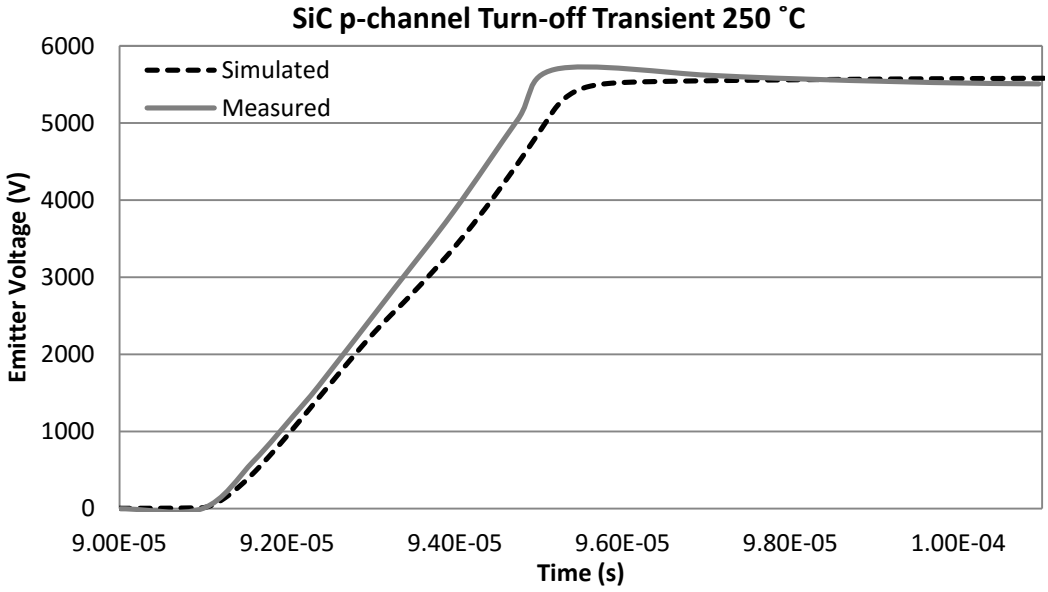


Figure 6.21 SiC p-channel turn-off voltage characteristics at 250 ˚C.

Table 6.1 contains the parameters required to produce the simulation results presented within this chapter.

Table 6.1 Model Parameters for Each Device

Parameter	Si n	SiC n	SiC p	Parameter	Si n	SiC n	SiC p
tauhl	3.9e-6	0.09e-6	9.06255e-6	***cgs***	7.0e-9	16.0e-9	1.5e-9
tauhlexp	6.0183	1.563753	0.156693	***coxd***	2.0e-9	1.5e-9	2.0e-9
wb	11.2e-3	0.016	0.0153	***vtd***	-10.5	0.0	0.0
nb	2.0e14	2.0e+14	5.2e+14	***vtdco***	0.0	0.0	0.0
a	0.3	0.71	0.022	***bvf***	1.0	26.0	36.3
agd	0.08	0.4	0.02	***bvftexp***	0.0	0.0	0.0
isne	1.0e-14	1.0e-60	1.0e-60	***bvn***	2.5	4.0	4.0
isnetexp	0.0	0.0	0.0	***bvntexp***	0.0	0.0	0.0
vt	4.6	8.4	7.6	***tnom***	27	27	27
vttco	6.6225e-3	-0.04898	0.0	***gmin***	1.0e-12	1.0e-12	1.0e-12
rs	0.009	0.01	0.0001	***fc***	0.5	0.5	0.5
theta	0.01	0.01	0.02	***mj***	0.5	0.5	0.5
thetatexp	8.135	0.0	0.0	***fc_bvcbo***	0.99	0.99	0.99
kf	1.8	0.47	0.45	***fc_neff***	0.999	0.999	0.999
kftexp	-1.4325	0.0	0.0	***voff***	-0.98	-0.15	0.3
kp	8.65	4.15	0.0165	***pb***	0.1	3.0	3.1
kptexp	0.7842	0.0	0.0				

6.4 Verilog-A Si/SiC IGBT Model Validation

Validation is required to prove the Verilog-A model produces approximately the same simulation as the MAST Si/SiC IGBT model under identical conditions and model parameters. To validate the Verilog-A version of the Si/SiC IGBT model, a range of simulations were compared to imitate data found on common datasheets. Figures 6.22 through 6.24 present the simulation comparison of the two models. The Si capacitance, Si output, and the SiC p-channel turn-off transient characteristics were compared between the two models, respectively. The MAST model produced a constant Coss plot between zero and one V_{ce}. This was not present in the Verilog-A model, as Coss simulated properly, and is also more accurate to the datasheet value of Coss. This validation falls within reasonable limits of simulator distinction, proving the validity of the Verilog-A model.

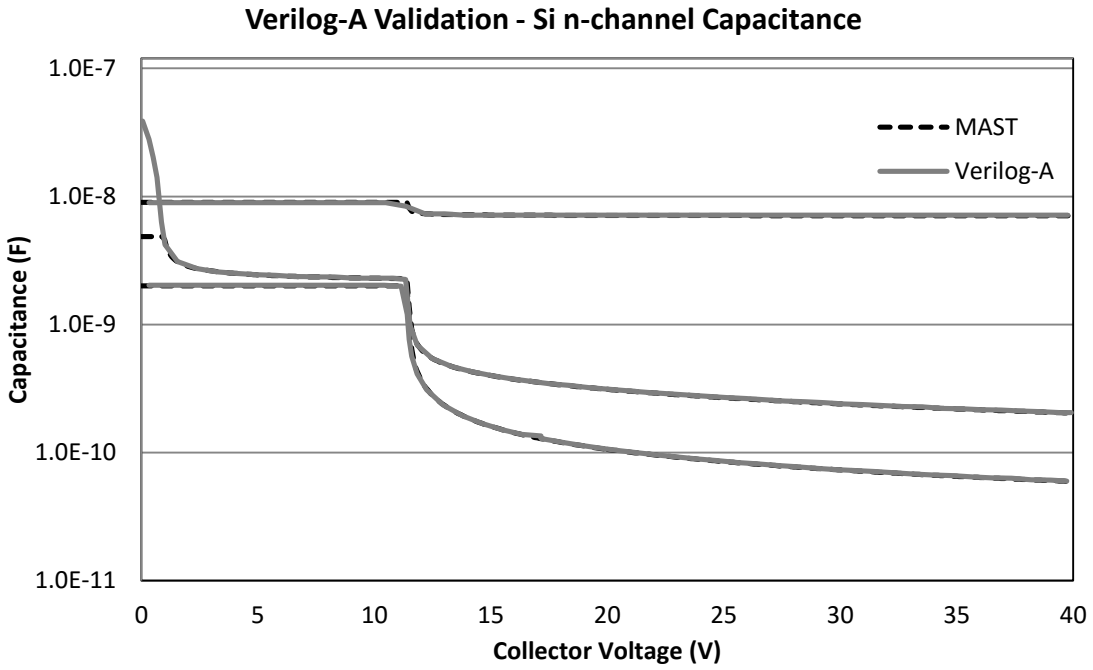


Figure 6.22 Si capacitance Verilog-A validation.

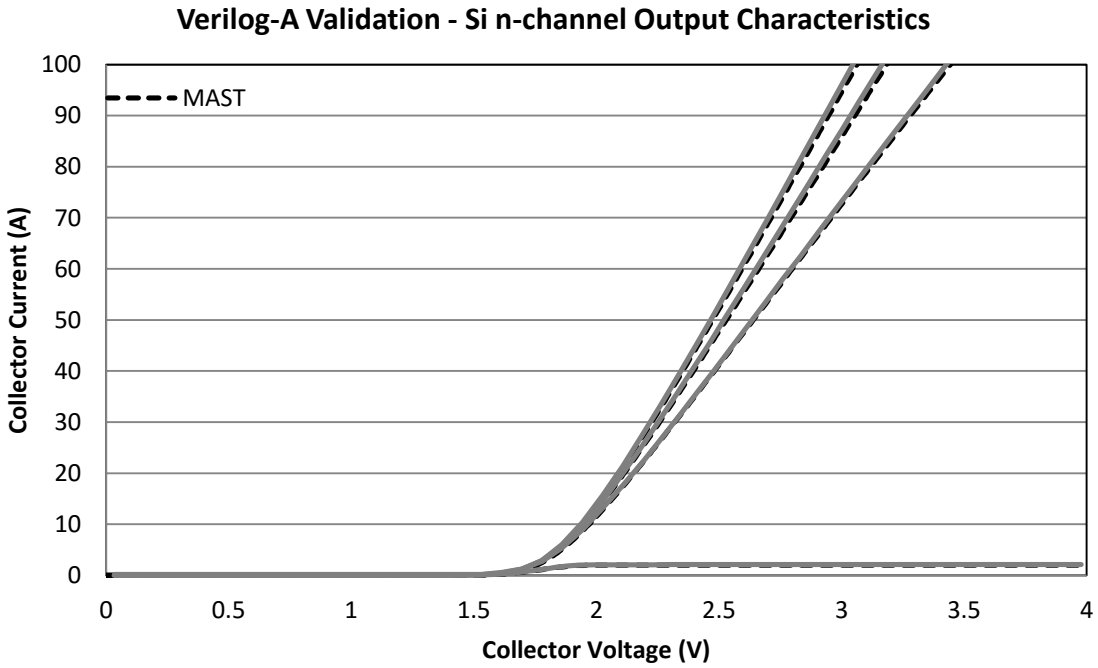


Figure 6.23 Si output characteristics Verilog-A validation.

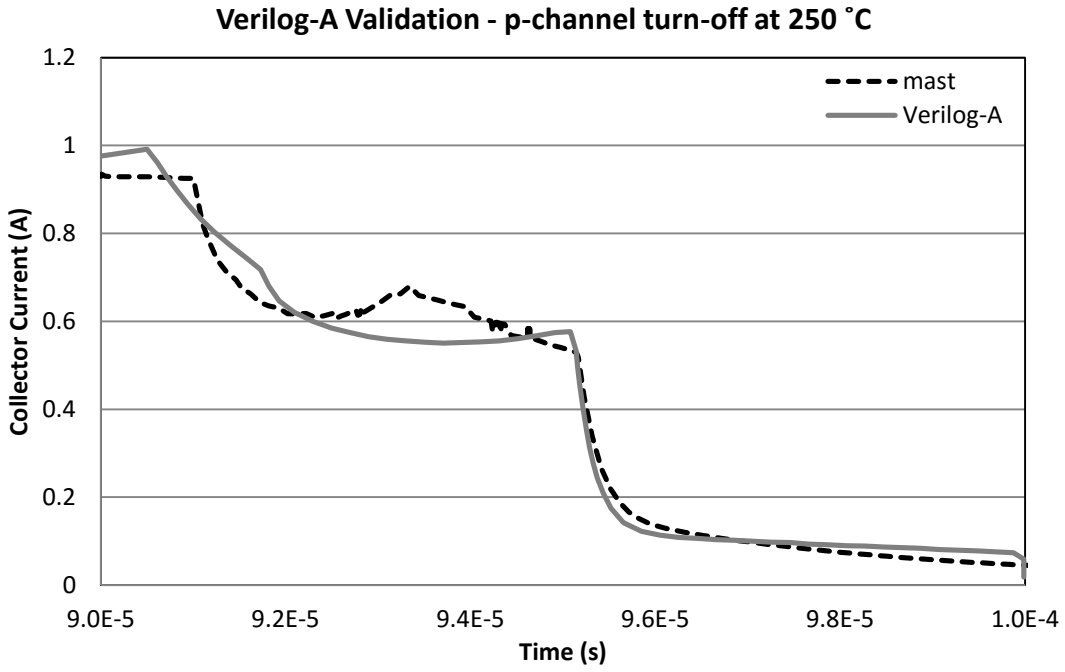


Figure 6.24 SiC p-channel turn-off current characteristics at 250 ˚C Verilog-A validation.

Chapter 7 Conclusion

SiC IGBTs will dramatically impact the power electronics industry with their high voltage and high temperature capabilities. A change of material from Si to SiC improves the operation of IGBTs by allowing for higher operation temperatures, larger temperature fluctuations, higher power densities, and higher operation frequencies. These material advantages lead to products that require less cooling system hardware, smaller base regions, and smaller valued passives, ultimately resulting in miniaturized products.

Although SiC n-channel IGBTs have been well researched, and p-channel IGBTs are becoming more popular, models of p-channel SiC IGBTs are not overly common. Due to the advantages of complementary circuits, a model that provides all possible combinations of Si, SiC, n-, and p-channel configurations is needed for the convenience of device modelers and circuit designers alike. Thus, a Si/SiC IGBT model that supports both n- and p-channel configurations in two languages has been presented. SiC mobility models were researched and implemented, and a preliminary parameter extraction method was developed. The model was verified with recently fabricated (2012 and 2014) SiC IGBTs under DC and transient conditions. In addition to the MAST model, a Verilog-A version of the Si/SiC IGBT model was created and successfully validated.

Although functional, verified, and validated, improvements can still be made on the Si/SiC IGBT model. It is advised that a smoothing function be added between the definitions of w and $wmin$ — model values discussed in Chapter 3. Another recommendation is to implement an automatic regression test suite for reliable model convergence. Further suggestions are to configure the breakdown voltage equation for a simple assignment, and to investigate FS IGBT

physics — as all SiC IGBTs reported include a buffer layer, as mentioned in Chapter 2. Lastly, the parameter extraction sequence presented in this thesis could be expounded upon utilizing direct device measurements.

A smoothing function is recommended due to a slight discontinuity throughout the calculation of the base width. When simulating turn-off characteristics, a discontinuity was discovered in the model as the base width approached $wmin$. Because there is a discontinuity in w, every aspect of the model that contains w also contains a discontinuity, including the tail current. To correct this discontinuity, a resistor at an arbitrary value was placed in the testbench, as seen in Figure 6.17. This resistor reduces the rate at which Vds increases, causing w to approach $wmin$ at a reduced rate. This removes the sudden change in the base width, thus smoothing the discontinuity. Although this testbench solution removed the discontinuity in the model, a permanent smoothing function should be implemented. The smoothing function should be based on the tanh function, and implemented when w equals 1.05 times $wmin$ and when w equals 0.95 times wb. Implementing a smoothing function would ensure that as w approaches $wmin$, a discontinuity is not produced.

An automated suite of testbenches available to the end user for proper function of all model aspects is also suggested. This suite of testbenches would allow the user to verify that the model is simulating appropriately, and would ensure convergence issues do not appear unexpectedly. The order of the tests should be as follows:

- all nodes grounded,
- output characteristics,
- input characteristics,
- capacitance,

- transient response, and
- complex circuit.

Currently, defining the breakdown voltage within the model is a multi-step process. The model parameter bvf has to be solved to define the breakdown voltage of the device, as explained in Chapter 4. It is advised that this process be simplified by implementing an equation that will allow bvf to be solved by inputting the actual breakdown voltage of the device. Defining the breakdown voltage in one step creates less confusion and reduces possible errors.

In addition to the aforementioned suggestions, it is recommended that the device physics of FS IGBTs is investigated and implemented. The FS IGBT provides many advantages over other structural designs of IGBTs, as explained in Chapter 2. Future devices will most likely be based on the FS design and will contain a buffer layer. Although the presented model simulated the SiC IGBT device characteristics adequately, a model that accurately simulates the transient voltage characteristics of SiC devices is recommended. Therefore, buffer layer physics must be implemented within a future model.

The parameter extraction method presented in this thesis serves as a preliminary method, as it relied upon the measurements available in the data sets mentioned in Chapter 6. To improve the extraction sequence, direct measurements of parameters from device characteristics are necessary. Instead of adjusting model parameters during a simulation to match a physical device measurement, a more robust method would include defining a parameter directly from the device measurement. For example, the collector current is measured at a specific collector and gate voltage, and a parameter is defined via an equation using the gathered information.

Since its invention in 1980, the Si IGBT continues to affect many aspects of our daily lives. With applications in inverter and motor drive circuits, the IGBT has modernized numerous

inventions from the combustion engine to the air conditioner through electronic components such as the electronic ignition system and variable speed motor drives, respectively. Through material properties of intrinsic carrier concentration, thermal conductivity, and critical electric field, SiC will continue to extend the circuit applications of the IGBT in high temperature, power density, and frequency applications.

With blocking voltages of SiC IGBTs reported in experimental fabrication reaching 22 kV, the SiC IGBT will be an excellent candidate for grid-connected applications [9]. For solar panels to provide energy to a house or to the grid, a solar inverter is necessary. A single power device with a 22 kV rating dramatically reduces the cost of these high power inverters, one hurdle manufacturers must overcome for alternative energy to become standard. Thus, SiC IGBTs will transform the power electronics industry in a similar manner to the way Si IGBTs transformed the internal combustion engine and air conditioners. Consequently, the groundwork for the next generation of high power, high temperature electronics is laid with SiC IGBTs.

References

[1] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[2] H. A. Mantooth, M. D. Glover, and P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 3, pp. 374–385, Sep. 2014.

[3] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY: Springer Science, 2008.

[4] R. R. Lamichhane, N. Ericsson, S. Frank, C. Britton, L. Marlino, A. Mantooth, M. Francis, P. Shepherd, M. Glover, S. Perez, T. McNutt, B. Whitaker, and Z. Cole, "A wide bandgap silicon carbide (SiC) gate driver for high-temperature and high-voltage applications," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, 2014, pp. 414–417.

[5] A. Rahman, P. D. Shepherd, S. A. Bhuyan, S. Ahmed, S. K. Akula, L. Caley, H. A. Mantooth, J. Di, A. M. Francis, and J. A. Holmes, "A family of CMOS analog and mixed signal circuits in SiC for high temperature electronics," in *2015 IEEE Aerospace Conference*, 2015, pp. 1–10.

[6] T. Funaki, J. C. Balda, J. Junghans, A. S. Kashyap, H. A. Mantooth, F. Barlow, T. Kimoto, and T. Hikihara, "Power Conversion With SiC Devices at Extremely High Ambient Temperatures," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1321–1329, Jul. 2007.

[7] On Semiconductor, "Appl. Note AND9070/D." .

[8] S.-H. Ryu, C. Capell, C. Jonas, L. Cheng, M. O'Loughlin, A. Burk, A. Agarwal, J. Palmour, and A. Hefner, "Ultra high voltage (>12 kV), high performance 4H-SiC IGBTs," in *2012 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2012, pp. 257–260.

[9] E. V. Brunt, L. Cheng, M. O'Loughlin, C. Capell, C. Jonas, K. Lam, J. Richmond, V. Pala, S. Ryu, S. T. Allen, and others, "22 kV, 1 cm 2, 4H-SiC n-IGBTs with improved conductivity modulation," in *Power Semiconductor Devices & IC's (ISPSD), 2014 IEEE 26th International Symposium on*, 2014, pp. 358–361.

[10] S. Ryu, C. Capell, C. Jonas, Y. Lemma, M. O'Loughlin, J. Clayton, E. Van Brunt, K. Lam, J. Richmond, A. Burk, D. Grider, S. Allen, J. Palmour, A. Agarwal, A. Kadavelugu, and S. Bhattacharya, "Ultra high voltage IGBTs in 4H-SiC," in *2013 IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2013, pp. 36–39.

[11]X. Kang, A. Caiafa, E. Santi, J. L. Hudgins, and P. R. Palmer, "Characterization and modeling of high-voltage field-stop IGBTs," *IEEE Trans. Ind. Appl.*, vol. 39, no. 4, pp. 922–928, Jul. 2003.

[12]T. Deguchi, T. Mizushima, H. Fujisawa, K. Takenaka, Y. Yonezawa, K. Fukuda, H. Okumura, M. Arai, A. Tanaka, S. Ogata, T. Hayashi, K. Nakayama, K. Asano, S.-I. Matsunaga, N. Kumagai, and M. Takei, "Static and dynamic performance evaluation of #x003E; 13 kV SiC p-channel IGBTs at high temperatures," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, 2014, pp. 261–264.

[13]C. C. McAndrew, G. J. Coram, K. K. Gullapalli, J. R. Jones, L. W. Nagel, A. S. Roy, J. Roychowdhury, A. J. Scholten, G. D. J. Smit, X. Wang, and S. Yoshitomi, "Best Practices for Compact Modeling in Verilog-A," *Electron Devices Soc. IEEE J. Of*, vol. 3, no. 5, pp. 383–396, Sep. 2015.

[14]K. Sheng, B. W. Williams, and S. J. Finney, "A review of IGBT models," *Power Electron. IEEE Trans. On*, vol. 15, no. 6, pp. 1250–1266, 2000.

[15]B. J. Baliga, "Analytical Modeling of IGBTs: Challenges and Solutions," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 535–543, Feb. 2013.

[16]A. R. Hefner and D. M. Diebolt, "An experimentally verified IGBT model implemented in the Saber circuit simulator," *Power Electron. IEEE Trans. On*, vol. 9, no. 5, pp. 532–542, 1994.

[17]A. R. Hefner, "Modeling buffer layer IGBTs for circuit simulation," *Power Electron. IEEE Trans. On*, vol. 10, no. 2, pp. 111–123, 1995.

[18]T. H. Duong, A. R. Hefner, J. M. Ortiz-Rodriguez, S.-H. Ryu, E. Van Brunt, L. Cheng, S. Allen, and J. W. Palmour, "Physics-based electro-thermal Saber model and parameter extraction for high-voltage SiC buffer-layer IGBTs," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 460–467.

[19]A. Hefner Jr and S. Bouche, "Automated parameter extraction software for advanced IGBT modeling," in *Computers in Power Electronics, 2000. COMPEL 2000. The 7th Workshop on*, 2000, pp. 10–18.

[20]X. Kang, E. Santi, J. L. Hudgins, P. R. Palmer, and J. F. Donlon, "Parameter extraction for a physics-based circuit simulator IGBT model," in *Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE*, 2003, vol. 2, pp. 946–952.

[21]R. Azar, F. Udrea, M. De Silva, G. Amaratunga, J. C. W. Ng, F. Dawson, W. Findlay, and P. Waind, "Advanced SPICE modeling of large power IGBT modules," *IEEE Trans. Ind. Appl.*, vol. 40, no. 3, pp. 710–716, May 2004.

[22]M. Cotorogea, “Physics-Based SPICE-Model for IGBTs With Transparent Emitter,” *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2821–2832, Dec. 2009.

[23]M. Miyake, D. Navarro, U. Feldmann, H. J. Mattausch, T. Kojima, T. Ogawa, and T. Ueta, “HiSIM-IGBT: A Compact Si-IGBT Model for Power Electronic Circuit Design,” *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 571–579, Feb. 2013.

[24]M. Miyake, M. Ueno, U. Feldmann, and H. J. Mattausch, “Modeling of SiC IGBT Turn-Off Behavior Valid for Over 5-kV Circuit Simulation,” *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 622–629, Feb. 2013.

[25]Meng-Chia Lee, Gangyao Wang, and Alex Huang, “4H-SiC 15 kV n-IGBT physics-based sub-circuit model implemented in Simulink-MATLAB,” *APEC*, 2015.

[26]M. Saddeh, “Modeling of SiC P-channel insulated gate bipolar transistors (IGBTS).” University of Arkansas, Dec-2011.

[27]M. Saadeh, H. A. Mantooth, J. C. Balda, E. Santi, J. L. Hudgins, S.-H. Ryu, and A. Agarwal, “A unified silicon/silicon carbide IGBT model,” in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 1728–1733.

[28]Mohan, Ned, Robbins, William P., and Undeland, Tore M., *Power Electronics Converters, Applications and Design*, 3rd ed. John Wiley & Sons Inc., 2002.

[29]S. Kagamihara, H. Matsuura, T. Hatakeyama, T. Watanabe, M. Kushibe, T. Shinohe, and K. Arai, “Parameters required to simulate electric characteristics of SiC devices for n-type 4H–SiC,” *J. Appl. Phys.*, vol. 96, no. 10, p. 5601, 2004.

[30]T. Hatakeyama, K. Fukuda, and H. Okumura, “Physical Models for SiC and Their Application to Device Simulations of SiC Insulated-Gate Bipolar Transistors,” *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 613–621, Feb. 2013.

[31]B. J. Baliga, *Advanced High Voltage Power Device Concepts*. New York, NY: Springer Science, 2011.

[32]R. Withanage, N. Shammas, S. Tennakoorr, C. Oates, and W. Crookes, “Igbt Parameter Extraction for the Hefner IGBT Model,” in *Universities Power Engineering Conference, 2006. UPEC ’06. Proceedings of the 41st International*, 2006, vol. 2, pp. 613–617.

[33]D. Navarro, T. Sano, and Y. Furui, “A Sequential Model Parameter Extraction Technique for Physics-Based IGBT Compact Models,” *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 580–586, Feb. 2013.

[34]A. Claudio, M. Cotorogea, and M. A. Rodriguez, “Parameter extraction for physics-based IGBT models by electrical measurements,” in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, 2002, vol. 3, pp. 1295–1300.

[35]T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and S.-H. Ryu, “Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence,” *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 353–363, Mar. 2007.

[36]V. Chaudhary, M. Francis, W. Zheng, A. Mantooth, and L. Lemaitre, “Automatic generation of compact semiconductor device models using Paragon and ADMS,” in *Behavioral Modeling and Simulation Conference, 2004. BMAS 2004. Proceedings of the 2004 IEEE International*, 2004, pp. 107–112.

[37]P. Mallick, M. Francis, V. Chandrasekhar, A. Austin, and H. A. Mantooth, “Achieving language independence with Paragon,” in *Proceedings of the 2003 International Workshop on Behavioral Modeling and Simulation, 2003. BMAS 2003*, 2003, pp. 149–153.

[38]T. Funaki, N. Phankong, T. Kimoto, and T. Hikihara, “Measuring Terminal Capacitance and Its Voltage Dependency for High-Voltage Power Devices,” *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1486–1493, Jun. 2009.

[39]Advanced Power Technology, “Appl. Note APT0103.” 2001.

Appendix A Si/SiC IGBT Model Equations and Parameters

A.1 Si/SiC IGBT multiplication factor equation

Multiplication factor when $V_{ds} \geq fc\_bvcbo \cdot bvcbo$.

$$m = \left(\frac{1}{(1 - fc\_bvcbo^{bvn\_t})}\right)^2 \cdot \left[\left(\frac{bvn\_t}{bvcbo\_t}\right) \cdot fc\_bvcbo^{(bvn\_t - 1)} \cdot V_{ds} + 1 - (fc\_bvcbo\_t \cdot bvn\_t) \cdot (bvn_t + 1)\right]$$

A.2 Model Parameters applicable to both MAST and Verilog-A

Parameter	Description	Units	Default value
a	Device active area	cm^2	0.5
agd	Gate-drain overlap active area	cm^2	0.2
bvf	Avalanche uniformity factor	-	15.0
$bvfexp$	Temperature exponent for bvf	-	0
bvn	Avalanche multiplication exponent	-	4.0
$bvntexp$	Temperature exponent for bvn	-	0
cgs	Gate-Source capacitance	F	1.0e-9
$coxd$	Gate-Drain oxide capacitance	F	1.0e-9
fc	Forward-bias non-ideal junction capacitance coefficient	-	0.9
fc_bvcbo	Breakdown voltage coefficient	-	0.999
fc_neff	Concentration ratio coefficient	-	0.99
$gmin$	Minimum slope for MOSFET current	-	1.0e-12
$isne$[1]	Emitter electron saturation current	A	1.0e-15[1]
$isnetexp$	Temperature coefficient for $isne$	-	0
kf	Ratio of kf in linear region to that in the saturation region	-	0.5
$kfexp$	Temperature exponent for kf	-	0
kp	MOSFET channel transconductance in saturation region	A/V^2	4
$kpexp$	Temperature exponent for kp	-	0
mj	Junction grading coefficient	-	0.5
nb	Epitaxial layer doping concentration	cm^{-3}	2.0e14
pb	Built in potential of the drain-source junction	-	0.6
rs	Intrinsic anode series resistance	Ω	0
$tauhl$	High level injection excess carrier lifetime	s	8e-6
$tauhlexp$	Temperature exponent for tauhl		0
temp	Simulator temperature	˚C	27
temprise	Rise in temperature in IGBT above simulation temperature	˚C	0
$theta$	Transconductance reduction factor	V^{-1}	0
$thetaexp$	Temperature exponent for $theta$	-	0
tnom	Temperature at which temperature exponents are based on.	˚C	27
$voff$	Offset voltage	V	-0.5
vt	MOSFET channel threshold voltage	V	5
$vttco$	Temperature coefficient for vt	V/K	0
vtd	Gate-Drain overlay depletion threshold voltage	V	0
$vtdco$	Temperature coefficient for vtd	V/K	0
wb	Metallurgical base width	cm	2.0e14

A.3 Model Parameters Applicable to MAST model only

Parameters	Description	Default Value
Channel	Chooses n- or p-type configuration	n_channel
Type	Chooses Si or SiC material	Si

A.4 Model Parameters Applicable to Verilog-A model only

Parameter	Description	Default Value
Channel[2]	Chooses n- or p- type configuration	1[2]
Material[3]	Chooses Si or SiC material	1[3]

A.5 Model Parameter Notes

1) If SiC model is selected, $isne$ is required to be larger than or equal to 1.0e-60.

2) For the Verilog-A model, 1 represents the n-channel model, and 2 represents the p-channel model. No other numbers are valid.

3) For the Verilog-A model, 1 represents a Si type device, and 2 represents a SiC device.

Appendix B Description of Research for Popular Publication

An IGBT, or insulated gate bipolar transistor, is a power switch that controls the flow of current in electronic circuits, and has had a large impact in almost every aspect of our daily lives since its invention in 1980. Utilized in inverter and motor drive circuits, IGBTs impact our lives from reducing the cooking time of our modern microwaves by 30%, to allowing our light bulbs to last eight times longer and reduce power consumption by 75% (when comparing compact fluorescent lamps to the incandescent light bulb). This single semiconductor device has affected the transportation, consumer appliance, industrial equipment, lighting, and renewable energy source industries, generating energy, cost, and space savings in every application [1].

Within the transportation industry, the IGBT is the single device that realized the replacement of automotive distributors with the electronic ignition system in the early 1990s. IGBTs are also instrumental in the advancement of low cost, high mileage electric vehicles through their use within electric motor drives, regenerative breaking systems, and battery charger technologies. Modern electric aircraft also owe a debt to the IGBT, as this device allows the replacement of all hydraulic equipment with a more reliable electronic system, resulting in less maintenance and real time monitoring of all systems [1].

IGBTs are the high power transistors chosen for these applications due to their abilities to provide high blocking voltage, operate at high frequencies, and contain an easy drive circuit. Specifically in the example of the compact fluorescent lamp (CFL), the IGBT provided the electronic ballast to be fabricated at a size which could fit into the existing base of incandescent bulbs. For CFLs to become successful, the infrastructure to use these bulbs had to be identical to the existing the hardware used to attach incandescent bulbs, i.e. light sockets. Without the same size light socket, the cost to integrate CFLs would not outweigh the savings generated by their

70% efficiency. IGBTs, at the time, were 60% smaller than BJTs, 70% smaller than MOSFET, and had the advantage of being a voltage controlled device. (A voltage controlled device requires less components in the final circuit design.) In the end, the IGBT allowed the ballast design to be reduced by 50% when compared with a design which utilized either MOSFETs or BJTs [1].

Just as silicon IGBTs transformed the transportation industry, silicon carbide IGBTs are the next installment in high power small package electronics. Due to material properties, silicon carbide devices possess the ability to operate at high temperatures, to endure faster temperature swings, and to produce smaller electronics. These advantages give silicon carbide devices the ability to launch the next generation of high power, reliability, and density products. With high power, reliability, and density device benefits, the realization of cheaper, miniaturized products are born.

Before a device is fabricated, a computer model of the circuit is compiled. The circuit is comprised of individual components – such as resistors, diodes, and IGBTs, for example – joined via electrical connections. Therefore, to create an entire computer model of the device, individual computer models of each circuit component are connected via simulated electrical connections – the same as those planned to be used in the physical circuit when fabricated.

The modeling process reduces the number of fabrication runs needed to produce a working device. Modeling the circuit before the fabrication is approved allows for unseen errors and effects (caused by electrical and magnetic interactions between components and connections) to be remedied efficiently, the device design to be optimized, and the reduction of the time to market and market cost. This is the reason semiconductor device models are required; they support the advancement of technology through the engineering efforts of circuit designers.

Therefore, to create the next generation of high power high temperature circuits, a model that can describe the electrical behavior of silicon carbide IGBTs is needed.

Presently, there are only a few IGBT models circuit designers have to choose from, and out of these models many are not supported by the most commonly used simulators. This work aims to provide the need of an IGBT model that can be utilized by a variety of circuit designers in a wide selection of designs. Designers also need different electrical configurations of IGBT models: n-channel and p-channel. These different configurations provide circuit designers the ability to create complimentary circuit designs, reducing the components needed within the entire circuit. Provided is an IGBT model that supports silicon, silicon carbide, n-, and p-channel configurations in both the Verilog-A and MAST formats.

[1] B. Jayant Baliga, *IGBT Device : Physics, Design and Applications of the Insulated Gate Bipolar Transistor*. Binghamton, NY, USA: Elsevier Science, 2015.

Appendix C Executive Summary of Newly Created Intellectual Property

Intellectual property was not created in this thesis, nor are any items patentable items.

Appendix D Potential Patent and Commercialization Aspects of listed Intellectual Property Items

There were no potential patents created during this thesis.

Appendix E Broader Impact of Research

E.1 Applicability of Research Methods to Other Problems

The research method employed for this thesis involved the following: choosing an existing model, reviewing the approximations made within the model, updating constants and equations, creating a parameter extraction sequence, and rewriting the model in another language. To model silicon carbide IGBTs, an existing compact model was selected to be the foundation of the new SiC model. Generally accepted existing IGBT models were considered, and the Unified IGBT model –unified for Si, SiC, n-, and p-channel IGBT configurations– was chosen. All approximations made within the existing Unified IGBT model were reviewed. For example, the mobility and base doping concentration effects were removed from the original model (as discussed in Chapter 3), and this simplification of the model was confirmed. Silicon carbide material constants and equations were researched and the latest data collected. For example, as discussed in Chapter 4, a constant within the intrinsic carrier concentration equation was adjusted. Updating the constant resulted in a decreased rate at which the intrinsic carrier concentration increased with temperature, and ultimately resulted in a more accurate model. A parameter extraction sequence was created, including the order of measurements as well as the order individual parameters within the measurements Lastly, the Unified IGBT model was written in the MAST language, limiting the usability in simulators. Thus, after updating the MAST model it was written in a more popular modeling language – Verilog-A.

While this research method is specific to the SiC IGBT model presented in this thesis, the general approach to modeling presented is applicable to all semiconductor device models. Specifically, the methods of selecting a model, reviewing approximations, and updating constants and equations are all methods that any device modeler should employ.

E.2 Impact of Research Results on U.S. and Global Society

To produce the next generation of high power circuits, circuit designers create models consisting all of the physical components in the circuit. Each individual component requires a device model, which is then integrated into the broader circuit model. Thus, compact device models that simulate the unique characteristics of chosen devices are required.

To provide a device model, physical measurements of the device are executed and the data collected, i.e. the device is characterized. From this data, an existing compact device model may be adjusted until the simulation data resembles the physical device data. Once a device model accurately simulates the electrical behavior of a physical component, it can be integrated into the circuit model and used to optimize the design. Optimization before the first fabrication run is extremely beneficial, as it reduces the time to market, losses in labor and energy, as well as wasted material.

The device model presented in this thesis contains updated SiC equations, as well as the option of both n- and p-channel configurations. This unification allows circuit designers the ability to create complimentary circuits utilizing the same base model with only different model parameters. Complimentary circuits require fewer components to create due to a reduction in design complexity. Again, reducing the number of components in a large circuit reduces the cost as well as the time to create a market ready product.

In addition to the unification feature, the model presented within this thesis was produced in two languages: MAST and Verilog-A. Currently, IGBT models do not exist in Verilog-A. As also explained in Chapter 5, Verilog-A is accepted by the most common simulators circuit designers utilize. Therefore, there is a need for a Verilog-A IGBT model.

In addition to having a direct societal effect by allowing for more efficiently designed and produced circuits, the Si/SiC IGBT model could realize many other indirect societal effects through Si and SiC IGBTs applications. After their invention in 1980, the Si IGBT allowed for the replacement of the automotive distributor with the electronic ignition system, the fulfillment of adjustable speed motor drives, and the realization of the electronic ballast for the compact fluorescent lamp (CFL). These three applications dramatically influenced both the U.S. and world economies.

The replacement of the automotive distributor with the electronic ignition system reduced fuel consumption of vehicles by at least 10%. This correlated to an estimated 326 billion gallons of gasoline saved from 1990 to 2010 in the United States [1].

Adjustable speed motor drives are utilized in many consumer and industrial applications, e.g. air conditioners, refrigerators, and in water pumps. It has been calculated that two thirds of the electricity in the US is utilized to power motors in consumer and industrial applications. Before the invention of the IGBT, dampers were used to control induction motors resulting in poor efficiency. Adjustable speed motor drives utilize IGBT based inverters, improving efficiency by at least 40%. This increase of efficiency correlated to cost savings of 2 trillion dollars from 1990 to 2010 in the United States alone [1].

The IGBT realized an electric ballast that fit within the existing infrastructure (i.e. light sockets). Without fitting the existing infrastructure, the CFL would not have been cost efficient enough to replace the 4% efficient incandescent light bulb. The CFL has 10 times the lifespan of an incandescent bulb and operates with 75% less power to produce the same amount of light. Using CFLs, the US has saved 48 billion dollars in energy cost for lighting alone. Worldwide,

CFL use is widespread, and the cost savings from 1990 to 2010 total up to 1.8 trillion dollars due to efficient light bulbs alone [1].

Although SiC IGBTs are still in the research and development stages of production, the SiC IGBT outperforms the silicon IGBT in breakdown voltage, max temperature rating, and on-state resistance. These improvements are due to the material properties of SiC alone. Just as the Si IGBT improved transportation, lighting, and motor drive applications, and saved the world an estimated 15.8 trillion dollars, the SiC IGBT will realize further savings for these same applications [1].

Many applications worldwide have already realized efficiency improvements with the introduction of the Si IGBT, however, these three IGBT applications have perhaps been the most influential on society: the electronic ignition system, adjustable speed motor drives, and compact fluorescent lamps. The Si/SiC IGBT model presented within this thesis provides the ability for circuit designers to create the next generation technology and improve upon the Si IGBTs already utilized in electronic applications. This model is needed as it allows for simulation of Si, SiC, n-, and p-channel IGBTs in MAST as well as Verilog-A – a language that is accepted by the most commonly used simulators. With this model as an open source document, engineers around the world have the ability to design circuits that further allow for cost and time savings both nationally and globally.

E.3 Impact of Research Results on the Environment

Appendix E.3 explains how each IGBT application discussed in Appendix E.2— the electronic ignition system, the adjustable motor drive, and the CFL — has affected the environment through carbon dioxide emissions. All reduction of carbon dioxide emissions are an estimation through the period of 1990 to 2010 [1].

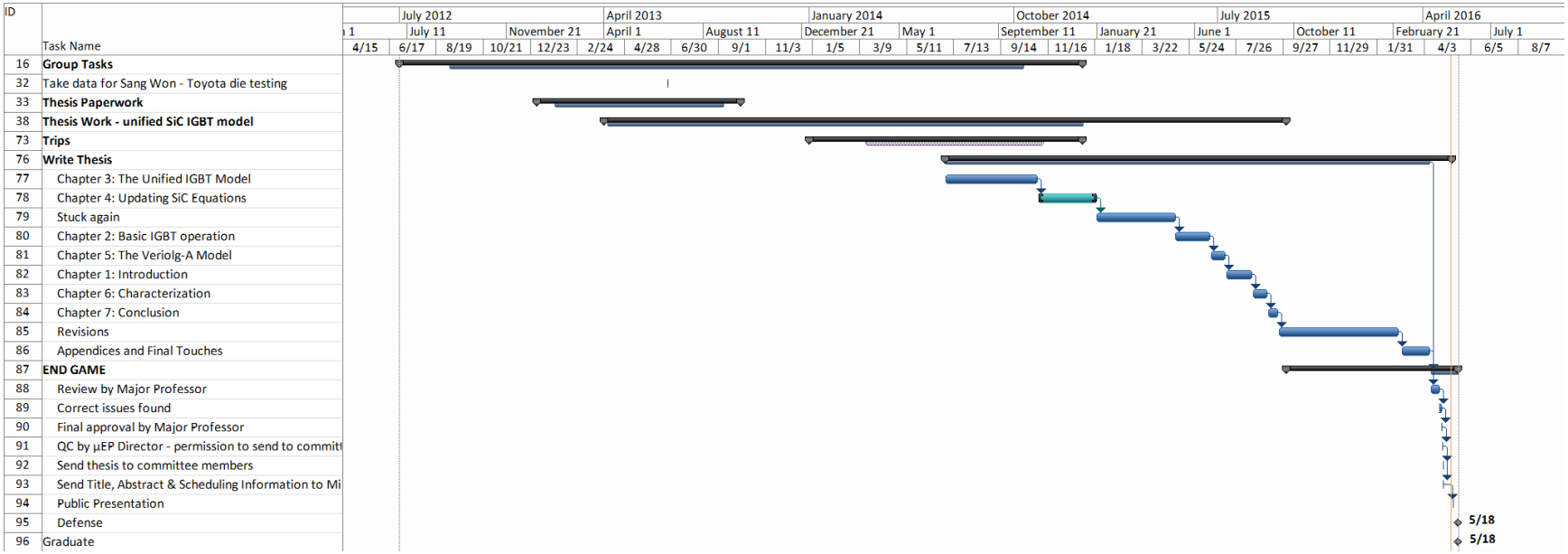
The introduction of the electronic ignition system in gasoline powered engines resulted in a reduction of 6.3 trillion pounds of carbon dioxide (CO_2) emissions by the United States alone. Worldwide, the reduction of CO_2 emissions is estimated at 22.2 trillion pounds, simply by reducing the fuel consumption of gasoline-powered vehicles by 10% [1].

With an increase in efficiency of at least 40%, utilizing adjustable speed motor drives reduced the amount of CO_2 emitted by the US by 27.9 trillion pounds. Globally, CO_2 emissions were reduced by 46 trillion pounds [1].

Although the use of CFLs has decreased due to the advent of affordable LED light bulbs, the CO_2 emitted from the United States was reduced by 659 billion pounds through a 20 year period as a result of replacing incandescent light bulbs. Universally, the use of CFLs are more common and the reduction during this period has totaled to 10 trillion pounds of CO_2 [1].

[1] B. Jayant Baliga, *IGBT Device : Physics, Design and Applications of the Insulated Gate Bipolar Transistor*. Binghamton, NY, USA: Elsevier Science, 2015.

Appendix F Microsoft Project for MS MicroEP Degree



ID	Task Name
16	**Group Tasks**
32	Take data for Sang Won - Toyota die testing
33	**Thesis Paperwork**
38	**Thesis Work - unified SiC IGBT model**
73	**Trips**
76	**Write Thesis**
77	Chapter 3: The Unified IGBT Model
78	Chapter 4: Updating SiC Equations
79	Stuck again
80	Chapter 2: Basic IGBT operation
81	Chapter 5: The Veriolg-A Model
82	Chapter 1: Introduction
83	Chapter 6: Characterization
84	Chapter 7: Conclusion
85	Revisions
86	Appendices and Final Touches
87	**END GAME**
88	Review by Major Professor
89	Correct issues found
90	Final approval by Major Professor
91	QC by µEP Director - permission to send to committ
92	Send thesis to committee members
93	Send Title, Abstract & Scheduling Information to Mi
94	Public Presentation
95	Defense
96	Graduate

Appendix G Identification of All Software Used in Research and Thesis Generation

Computer #1:

Location: CSRC

Owner: UA Electrical Engineering Dept.

Software #1:

Name: Microsoft Office 2010

Purchased by: UA Electrical Engineering Dept.

Software #2:

Name: Saber 2013

Purchased by: UA Electrical Engineering Dept.

Software #3:

Name: Microsoft Visio 2010

Purchased by: University of Arkansas Site License

Software #4:

Name: Eclipse

Purchased by: UA Electrical Engineering Dept.

Software #5:

Name: Paragon 2.0

Owned by: UA Electrical Engineering Dept.

Appendix H All Publications Published, Submitted and Planned

A. Rashid, S. Perez, R. Kotecha, S. Ahmed, T. Vrotsos, M. Francis A. H. Mantooth, "A Unified Silicon/Silicon Carbide Compact IGBT Model for N- and P-Channel Devices." Planned for submission to Transactions on Power Electronics, 2016.

R. R. Lamichhane, N. Ericsson, S. Frank, C. Britton, L. Marlino, A. Mantooth, M. Francis, P. Shepherd, M. Glover, S. Perez, T. McNutt, B. Whitaker, and Z. Cole, "A wide bandgap silicon carbide (SiC) gate driver for high-temperature and high-voltage applications," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, 2014, pp. 414–417.