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Epitaxial Growth of Silicon on Poly-Crystalline Si Seed layer at Low Temperature by Using Hot Wire Chemical Vapor Deposition

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by

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Abstract

There has been a growing interest in using low cost material as a substrate for the large grained polycrystalline silicon photovoltaic devices. The main property of those devices is the potential of obtaining high efficiency similar to crystalline Si devices efficiency yet at much lower cost because of the thin film techniques. Epitaxial growth of Si at low temperatures on low cost large grained seed layers, prepared by aluminum induced crystallization method (AIC), using hot wire chemical vapor deposition (HWCVD) system is investigated in this thesis. In this work, different parameters have been studied in order to optimize the growth to reach the goal of epitaxial growth. The growth of epitaxial silicon using HWCVD system is controlled by four parameters: flow rate of gases, pressure, substrate temperature and filament temperature. As a result, in this work, those four factors were varied to optimize the growth process.

Crystallinity quality is a significant factor toward confirming the epitaxial layer. Raman scattering, X-Ray Diffraction (XRD), Scanning Electron Microscope (SEM), and Transmission Electron Microscope (TEM) were used to determine the crystallinity. Epitaxial growth of Si at 500 °C was obtained even with a low vacuum of 1×10^{-3} torr.

Furthermore, heavily doped large grained polycrystalline silicon seed layers were formed at first using AIC on Indium Tin Oxide (ITO) coated glass substrates to be ready for the following step which was epitaxial growth of Si. The grains were continues in the center of the film which was a single crystal that no one has reported it before. Epitaxial growth of Si was successfully achieved as the SEM results showed similar grain sizes before the epitaxial growth and after the epitaxial growth. The TEM results confirmed the epitaxial growth but stacking faults were observed. Also, different orientations were present as Moiré Fringes was seen in the TEM images.

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Dedication

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Chapter 1: Introduction and Motivation

1.1 Introduction

Interest in sustainable energy has increased worldwide due to the environmental consequences of using fossil fuels such as carbon emission and acid rain. Fossil fuels such as oil and gas are limited natural resources. Once consumed, they need millions of years to form again. The problem is that if the growth rate of human population remains the same, in 50 years the number of people on earth will be doubled. Consequently, the need for energy will increase, which will increase energy prices as well.

Natural resources are materials that occur in nature and can be consumed for economic gain. The most common types are water, fertile lands, forests, and minerals. Throughout history, natural resources have been increasingly exploited in the development of civilizations. From cooking on wood fires to propelling airplanes using enormous fuel engines across oceans, natural energy resources are essential for any society to progress.

At the current rate of consumption, natural energy resources will be depleted in the future, since these resources are finite. Over-use of these natural resources can also have negative impacts on the environment, such as global warming due to greenhouse gas emission. As a result, the push toward renewable energy use as a solution for many global issues has resulted in increased funding for promising alternative energy research. Such research holds the potential to impact multiple facets of global human interest from poverty to pollution.

Sun radiation could be the solution that covers this growing demand for energy by way of the photoelectric effect. When light hits solar cells, electrons get excited so that electricity is generated. Solar cells work as a p-n junction, which consists of two kind of materials: p-type and

n-type semiconductor materials. A better understanding about silicon (Si) is needed in order to further explain p-n junctions.

Silicon is a chemical element that has an atomic number of 14 and has four electrons in its outermost shell. These four electrons are shared with adjacent silicon atoms to form an orbital of eight atoms. Silicon is not only a poor electrical conductor but also a poor insulator, therefore it is called a semiconductor. It is also an indirect band gap material.

The band gap in the solid state represents the energy difference between the top of the valance band and the bottom of the conduction band. There are some materials that are direct band gap such as GaAs and others are indirect band gap such as Si. In direct band gap materials, the top of the valance band is aligned with the bottom of the conduction band because they have the same momentum value, which results in light emission when electrons excite these materials. However, indirect band materials have their top of valance band and bottom of conduction band at different values of momentum.

Thermal energy can break the Si-Si bonds and create a free electron. When an electron gets excited to a higher energy level it leaves behind a hole that has a positive charge. In pure semiconductors, the number of electrons and the number of holes are equal and they are termed the intrinsic carrier concentration (n_i). At room temperature, 300 K, the intrinsic carrier concentration (n_i) in silicon is about 1.4×10^{10} cm^{-3}[1].

Silicon is a great choice for photovoltaic devices since it is abundant and non-toxic. In addition, the electrical conductivity of Si can be improved and controlled when adding some other materials such as group three (III) or group five (V) elements of the periodic table that are called impurities.

Column IV of the periodic table has the semiconductor elements such as silicon and germanium, all of which form the same bonding where all four electrons in the outermost shell are bound to its four neighboring atoms resulting in a stable arrangement. Their conductivity depends on temperature change, optical excitation, and doping content. This electrical property that provides control of the required conductivity makes semiconductor materials significant for electronic devices. Figure 1 shows a p-n junction solar panel.

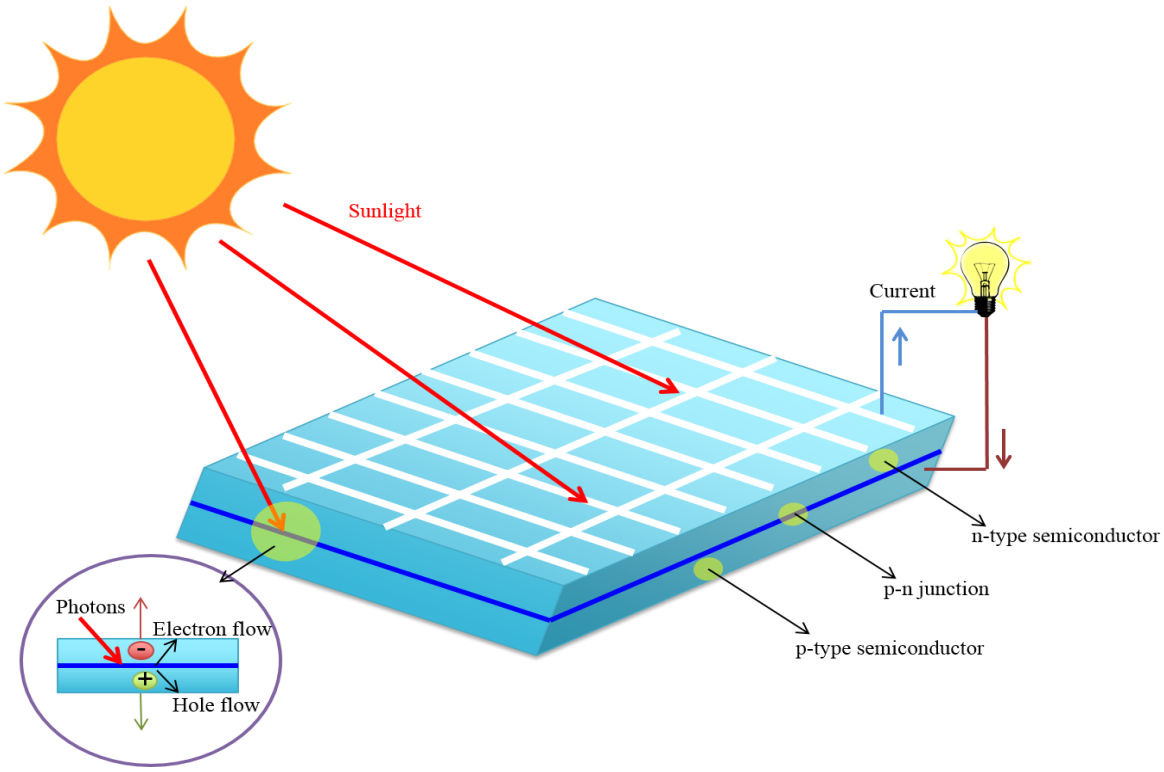

Figure 1. A schematic diagram of solar panel

In order to form a p-n junction, elements from group three or five of the periodic table are bound to silicon. Column III elements such as boron have three electrons in their outermost shell so they create a p-type semiconductor when added to column IV elements. These three electrons bind with three Si electrons which leave one hole so the number of holes is larger than number of electrons (p-type material). On the other hand, column V has elements that have five electrons in their outermost shell, such as phosphorus, so they form n-type semiconductors when added to

column IV elements. Introducing those elements of group three and five of the periodic table to group four, semiconductor elements, is what is termed doping. Doping in semiconductors can be performed using diffusion or ion implantation [2].

There are two different kinds of solar cells: crystalline Si (c-Si) based solar cells and thin film Si based solar cells. Currently, the most common solar cell products are based on c-Si, which is expensive in terms of initial costs but generates high efficiency. Crystalline silicon solar cells were the first generation of photovoltaic devices and are still the most common because of their high efficiency. The thickness of the silicon wafer that is used in c-Si solar cells is between 200 and 500 μm[3].

The solar cell industry depends on either increasing the solar cells efficiency or decreasing the cost of manufacturing, without sacrificing the device efficiency. The cost of solar cells depends greatly on the c-Si substrates. In the last six years, a worldwide demand for photovoltaic devices has increased by over 30% per year[4]. In 2011, the solar cell industry produced about $125 million in revenue. The growth rate of the revenue from 2010 to 2011 was 81.4%[5].

Thin film silicon solar cells have many advantages over c-Si solar cells. One such advantage is that they have a lower cost due to the fact that thin film technology is using less active materials. A thin-film photovoltaic cell (TFPV) is a solar cell that is fabricated by depositing one thin layer, or several thin layers of photovoltaic material on an inexpensive substrate. The thickness varies from a few nanometers to tens of micrometers. Thus, the active materials included in the thin film solar cells such as silicon are less compared to normal solar cells. “Conventional solar cells use silicon wafers that are over 100 micrometers thick, while thin-film devices have thicknesses of a few micrometers”[6].

Thin film technology has the ability of separating the active materials from the mechanical support material. This can be done by depositing a thin layer of active materials on a low cost substrate such as glass. As a result, the cost of these solar cells compared to the c-Si solar cells is lower due to using less Si in the thin film technology.

However, the problem associated with thin film solar cells is that their relatively low efficiency compared to the efficiency of c-Si solar cells puts thin film solar cells at a disadvantage despite their lower production cost. Therefore, increasing the quality of thin film solar cells toward having a higher efficiency is a topic of great interest which has been researched for decades.

There are different types of thin film solar cells, such as amorphous Si based thin film solar cells (a-Si) and CdTe based thin film solar cells. Large grained polycrystalline silicon solar cells are another type that have many advantages over their other thin film solar cell counterparts. Due to the health risks of using cadmium in the fabrication of solar cell, new regulations in the European Union was implemented to ban using CdTe solar cells[7]. According to United Solar LLC, currently their commercial a-Si solar cells have low efficiency of about 9.5%[4].

This type of solar cells could have the potential to have efficiency of about 15% like crystalline Si solar cells but at lower costs[4]. Therefore, epitaxial growth on large grained polycrystalline silicon seed layers is just one significant improvement of thin film technology in the solar cell industry and is the focus of investigation which is detailed in this thesis.

1.2 Motivation for Epitaxial Growth

The increasing cost that is anticipated in the future of solar cells is the leading motivation for using less active photovoltaic materials, which would decrease the price of c-Si solar cells even more. Decreasing the amount of active materials in photovoltaic devices is one of the main targets

for the leading companies in the solar cell industry. Thus, thin film technology is a solution that would lead to a competitive advantage for these companies.

Epitaxial growth is a technique that has drastically improved thin film technology due to the high quality deposition that is produced. The quality of a solar cell is extremely important and needs to be taken into consideration because of the way it impacts the device efficiency. The silicon wafer manufacturing process has been improved significantly, but defects on the surface remain which are produced during crystal growth. Any type of defect, such as interstitials or vacancies, can damage device performance. Due to the thickness of the epitaxially grown layer, a mechanical support is needed. Thus, an inexpensive substrate such as glass was used and prepared by aluminum induced crystallization (AIC) to be seed layers for the epitaxial thickening.

Using AIC method on glass provides large grains compared to directly depositing Si on glass which results in small grains. The grain boundaries are recombination sites for the charge carriers that result in a drastic reduction of their lifetime. This affects the efficiency of the device which means that the grains must be larger than the thickness of the solar cells.

This work demonstrates epitaxial growth on large grained poly-crystalline Si seed layer by means of AIC with the goal of reducing the high cost of crystalline silicon (c-Si) substrates and providing high quality thin layers.

1.3 Organization of Thesis

This thesis begins with a brief introduction about the driving force for thin film photovoltaic devices in general and, more specifically, for epitaxial growth of Si. Chapter two introduces a theoretical background about different techniques of thin film deposition and ends with aluminum induced crystallization. Literature reviews on epitaxial growth of Si on c-Si substrates and seed layer substrates are then discussed in chapter three. Chapter four presents the

experimental methodology and the equipment that was used to make this work possible. Chapter five contains a description of the results and discussion. The final conclusion is presented in chapter six with suggested future work.

Chapter 2: Theoretical Background

2.1 Epitaxial Growth

One of the major methods of crystal growth is that of thin film on a matched substrate. This is called an epitaxial growth[8]. The term “Epitaxy” has Greek roots that are “epi” and “taxis”. The first syllable “Epi” means above and “taxis” means “an ordered manner” [9]. Therefore, epitaxial growth generally means growth of a single crystal that is in an ordered manner on top of a crystalline substrate.

Using thin film manufacturing procedures plays a major role in cost reduction efforts. Therefore, epitaxial growth on large grained seed layer is an efficient approach for the future of renewable energy. The devices that are produced by this approach and followed by HWCVD at low temperatures to deposit epitaxial Si on top of the substrate could be the next generation of photovoltaic devices[10].

There are two types of epitaxial growth: homo-epitaxy and hetero-epitaxy. Homo-epitaxy is an epitaxial layer of a material that is the same as the substrate. An example of this kind is the epitaxial growth of Si on crystalline Si substrate[11]. This kind can be used to grow a film that is more pure than the original substrate. Also, it can be used to form layers that are different in doping levels. It is usually easier to grow an epitaxial layer on top of the same material, due to lattice matching.

Hetero-epitaxy is epitaxial growth of a material that is different from the substrate. An example of this is the epitaxial growth of Si on glass or seed layers [11]. Hetero-epitaxy can be used to fabricate combined crystalline layers from various materials. As aforementioned, hetero-epitaxy is more difficult to achieve but possible under suitable conditions.

B. Lattice matching

Lattice matching is an important factor to obtain epitaxial growth. In homo-epitaxial junctions, it is easier to get a high quality single crystal because of the structure matching. However, Si epitaxial growth on top of a different material than the substrate, such as hetero-epitaxial junctions is possible.

It is important that the lattice structure of the substrate matches the lattice structure of the epitaxial layer. For example: GaAs has the same zinc blende structure as AlAs does. The lattice constant for this structure is about 5.65A. As a result, the epitaxial growth of AlGaAs is possible on a GaAs substrate [8].

Figure 2 shows three different cases of lattice structure matching. In general, matched lattice structure enables the epitaxial growth easier than the other types. In matched lattice structures, the quality of the film is higher than the other matching conditions and there are fewer defects. Also, here the mobility of electrons is highest.

Strained lattice happens when there is a mismatch in the lattice structures, so the film may strain to adapt to that difference. However, if the accommodation to the strain is difficult, defects and dislocation may occur. In this case the change is called relaxed matching [12]. When less than ~9% lattice mismatch is present, the first layers of film will grow "pseudomorphically"[10].

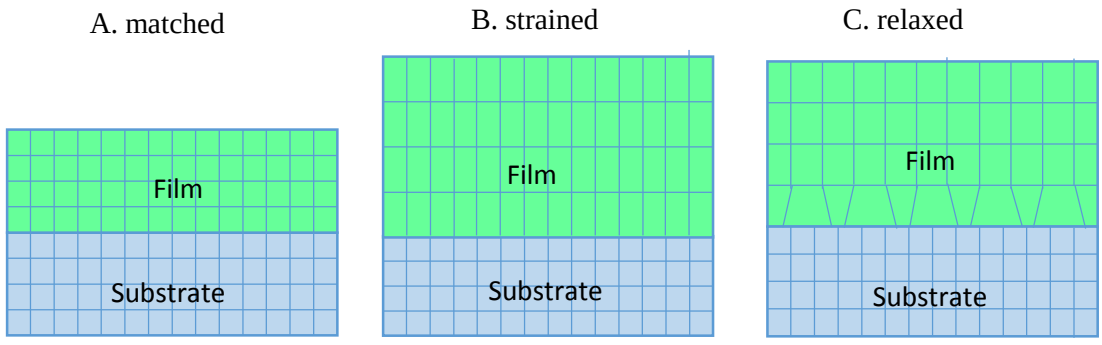

Figure 2. A Schematic diagram of lattice strains: A. matched lattice structure, B. strained lattice structure, and C. Relaxed lattice structure.

C. Methods of epitaxial growth

There are many techniques to obtain thin film deposition. The two main categories are: chemical vapor deposition (CVD) and physical vapor deposition (PVD). Plasma enhanced chemical vapor deposition (PECVD) and hot wire chemical vapor deposition (HWCVD) are two significant types of CVD methods. However, the focus of this thesis is solely on HWCVD.

D. The substrate orientation

The orientation of the c-Si substrate is significant in epitaxial growth due to some orientation plane properties which exhibit preference to grow epitaxially than other types. In this work (100) c-Si was chosen to grow the epitaxial layer of Si on top of it. Many studies suggested that (100) c-Si planes have an advantage over (111) c-Si planes because of the fact that each Si atom has two bonds that can be incorporated in a lattice location. On the other hand, the Si atoms in the planes of (111) have only one bond which might not be enough to grow an epitaxial layer[13].

2.1.1 Chemical Vapor Deposition (CVD)

2.1.1.1 Plasma Enhanced Chemical Vapor Deposition (PECVD)

A thin film of various materials can be deposited using plasma enhanced chemical vapor deposition (PECVD) technique. A thermal source is incorporated in the chamber of PECVD in order to initiate the chemical reactions. Adding the plasma source in this method allows the deposition to occur at lower temperatures than those methods that have only a thermal source. A typical PECVD chamber has parallel electrodes where one electrode is grounded while the other one is RF-energized[14]. The lower temperatures that are required for the deposition make the PECVD advantageous over the CVD method. High quality SiO_2 films can be obtained in the

PECVD system at 300˚ to 350 °C, whereas the CVD system requires higher temperatures that range from 650 to 850 °C.

Plasma in the PECVD technique is used to decompose the introduced gases in the chamber to ions, atoms, molecules, reactive radicals, and other species. These species will interact at the substrate surface[15]. Some of the applications of PECVD are: “the deposition of dielectric films and passivation films like silicon oxide or nitride or ONO layers at low temperature”[16].

One of the disadvantages of the PECVD system is the accelerated ions that are produced in the chamber and go directly toward the surface of the substrate. This could be harmful to the deposited film and can damage the quality of the film substantially. The high cost of the PECVD equipment is another disadvantage factor[17][4].

2.1.1.2 Hot Wire Chemical Vapor Deposition (HWCVD)

Hot wire chemical vapor deposition or catalytic chemical vapor deposition are methods that use a hot filament to break the chemical bonds in SiH_4, H_2 or other gases. Hot wire chemical vapor deposition is of great importance in the thin film industry. Not only because of the cost reduction, but also because it causes less ion damage in comparison with other methods such as PECVD.

In the HWCVD technique, a heated filament decomposes a gas mixture that is introduced in the chamber into radicals. Then, the product of the decomposed gas mixture is deposited on the surface of the substrate. “The chemical composition of the layers can be adjusted very well by way of the selection and the mixing ratio of the types of gas that are employed.” [18]

The precursors in the HWCVD after thermal decomposition have an energy of about 0.2 eV which is less energetic than the accelerated ions in PECVD. The growth rate is also a factor due to the low growth rate which can create defects and increase the cost of capital. HWCVD system "offers a high deposition rate of up to 5 nms^{-1}" [4] . By using HWCVD, the uniformity of the film can be increased when using more than one filament. The disorder decreases when depositing Si by HWCVD more than it does with PECVD [19]. The filament can play a great role in the passivation of the bulk and the film [4][20]. There are four critical factors that control growth in the hot wire chemical vapor deposition method: flow rate of gases, pressure, substrate temperature and filament temperature[21].

Using a hot filament at temperatures ranging from 1200-2000 ˚C can fully break SiH_4 and H_2. The products are then deposited on top of a substrate, which is heated by either an external source or by the hot filament at temperatures ranging from 200 to 800 °C. This method is much cheaper than PECVD or MBE. The filament material choice is important because it has a great effect on the epitaxial growth process.

The materials that have been used by different research groups are: tungsten (W), tantalum (Ta), and graphite (C) filaments. Tungsten at a temperature of about 1500 °C has a very high cracking factor for silane. This is very important for gas consumption. Tantalum is more expensive than tungsten, but it produces a larger thickness film than tungsten in the same circumstances. Graphite is quite new in reference to hot wire chemical vapor deposition. It does not contaminate the film with carbon any more than tungsten would, as was previously thought.

If there is any contamination, it is not as damaging as the other filament materials such as tungsten and tantalum. The filament temperature also affects the cracking process and the

contamination level of the film. The species coming off of the filament are created based on the filament temperature [22].

In general, any temperature above 1500 °C will provide a dominant silicon in the outcomes species in the case of tungsten filament (W). As a result, the experiments in this work were performed at 1900 °C and above to guarantee the species that will result are predominantly silicon. At lower temperatures, some species such as SiH_2, SiH_3 could be present because SiH_4 will not be fully decomposed. At high temperatures, some residue products form gases which can be found in the film. Because W has a successful history, it will be used as the filament material.

There are four main sources to produce silicon for commercial epitaxial growth. They are: silicon tetrachloride ($SiCl_4$); trichlorosilane ($SiHCl_3$); dichlorosilane (SiH_2Cl_2); and silane (SiH_4) [23]. In this research, SiH_4 will be discussed as the source of silicon. Growth of Si from a gas source reduces the cost of solar cell materials. Moreover, Si can be reused due to this thin film technology which increases the utilization of materials and cuts the industrial cost [22].

Silane gas can be used pure or mixed with other gases like atomic hydrogen or argon (Ar). The results from the diluted mixture of hydrogen and Si were a combination of amorphous and crystalline Si as the pure SiH_4 results. However, the crystalline fraction X_c increased when using diluted SiH_4 in atomic hydrogen. There is no evidence or clear understanding of the behavior of the deposition when adding hydrogen, except that atomic hydrogen helps the epitaxial growth by lowering the deposition rate to increase the crystallinity[24].

The overall chemical reaction of the epitaxial silicon growth using SiH_4 is not fully known, but can be written as: $SiH_4 \Rightarrow Si + 2H_2$ [23]. The structure of the resulted thin films of Si in this work differ from one set of conditions to another.

2.1.2 Physical Vapor Deposition (PVD)

Using physical processes to deposit a film instead of chemical reactions as in CVD system is another avenue of thin film deposition. This physical process is called physical vapor deposition (PVD). In PVD systems almost any kind of material can be deposited, which make them more flexible than CVD systems. The two types of PVD methods are evaporation and sputtering. They have been utilized for over one hundred years for thin film metal coating. The most common method today is sputtering, but evaporation is still utilized for some applications[1].

2.1.2.1 Evaporation

In evaporation systems, the chamber is pumped down to less than 10^{-5} torr to obtain a high vacuum. Then a source is heated so the atoms of the source evaporate and condense on the surface of the samples. The probability of the atoms to be scattered is low due to the atoms traveling in a high vacuum, unlike CVD systems [1].

2.1.2.2 Sputter Deposition

Sputtering is a process where a substrate is placed in a high vacuum chamber to be coated. This chamber contains a target source of the material that will be deposited on the substrate surface. A negative charge is applied to the target source so that a plasma will glow. Electrons are emitted from the target source and flow colliding with Ar atoms. Therefore, the negatively charged Ar atoms will be positively charged ions that will be “attracted to the negatively charged target material at a very high velocity that ‘sputters off’ atomic size particles from the target source”[25].

Sputter deposition has some advantages over evaporation thus it is used in many technologies. It does not require high vacuum, so a vacuum ranging from 1 to 100 mTorr is

enough. On the other hand, evaporation requires less than 10^{-5} torr. Even though sputtering is favored over evaporation, the high pressure in sputtering can cause contamination. As a result, evaporation is thought more desirable for special applications and technologies[1].

2.2 Aluminum Induced Crystallization

Aluminum-induced crystallization (AIC) for seed layer preparation:

The most common approach to prepare seed layers on glass for solar cell fabrication is aluminum-induced crystallization which is also identified as aluminum-induced layer exchange (ALILE) [26]. A continuous large grained poly-silicon seed layer can be obtained by AIC. The resulting seed layers will be a heavily doped p-type due to the fact that aluminum functions as an acceptor in silicon [4].

For the AIC process, a layer of oxide on top of aluminum before an a-Si deposition is obtained by exposing the sample to ambient air. This oxide layer separates the a-Si layer and the aluminum layer during the process. It acts as a permeable membrane and controls the diffusion of the a-Si and aluminum [20]. In general, transformation from amorphous phase to crystalline phase can be achieved when some metals are in contact with a-Si. Some examples of metals that can be used to crystallize a-Si are: Al, Ag, Au, Sb, Cu, and Ni.

The significance of metal and a-Si structure comes from the fact that a-Si interacts with metals and transforms from amorphous phase to crystalline phase at lower temperatures than the eutectic temperature of the Si-Al contact (577 ºC)[27]. Otherwise, a-Si requires temperatures above the eutectic temperature of the Si-Al contact.

The conversion temperatures must be below the eutectic temperatures of the metal and a-Si system. Below is a table of the metals and their eutectic temperatures (T_{eu}) when they are in contact with amorphous silicon. Table 1 below shows the eutectic temperatures for some metals when they interact with a-Si

Table 1. The eutectic temperatures for some metals when they interact with a-Si [50].

Metal	T_{eu} (°C)
Al	577
Ag	830
Au	360
Sb	630
Cu	802
Ni	964

The interaction between the metal and a-Si is defined by the difference in their chemical potential, called free energy. The free energy of the a-Si is higher compared to metals which initiate the chemical reactions to reduce it.

Another contribution to the chemical reactions is the large amount of stress in a-Si. Dries Van Gestel et al [28] pointed out a basic model to understand the interaction in which the metal (Al in this case) induces decomposition of Si atoms at the interface between aluminum and a-Si.

Annealing enhances the diffusion of the Si atoms through the aluminum oxide to the Al layer. At this point, nucleation has happened and the driving force is the difference in Gibbs free energy. This causes a silicon concentration in aluminum which is above the critical concentration of silicon nucleation. Then, silicon grains will start to grow in all directions until they reach the substrate which limits the grains to lateral growth. Aluminum diffuses during the Si grain growth into the top layer to decompose Si atoms. A secondary AIC will occur on the top layer when Al atoms interact with the remaining a-Si [28].

The driving force toward choosing Al over the other metals is because when Al is incorporated in the poly-Si atoms as an impurity, new energy levels will be present. There are two kinds of new energy levels: shallow energy levels that are close to the valance or conduction bands and deep energy levels that are close to the middle of the band gap.

Aluminum introduces an energy level that is close to the valance band, which is an advantage of Al over the other metals. The reason for this is the reduction in recombination that is caused by Al due to the energy level near the valance band. There are only two cases that can happen to the carriers: re-excitation or recombination. What happens here is re-excitation which reduces the harmful consequences caused by the other metals[27]. There are two configurations of AIC growth: aluminum induced crystallization (AIC) or seeding structure and top-down aluminum induced crystallization (TAIC) also known as capping structure[29].

2.2.1 Aluminum Induced Crystallization (AIC)

The structure of this type begins with an Al layer on a glass substrate and then an a-Si:H layer will be deposited on top of it so the configuration of this type is (glass/Al/a-Si:H). After annealing, the resulting order will be (glass/poly-Si/Al). In this case, Si islands will be present on the surface as a secondary crystallization as mentioned previously. This work includes more results of the configuration of AIC than TAIC[29]. A schematic diagram of a fabrication process of AIC is shown in Figure 3.

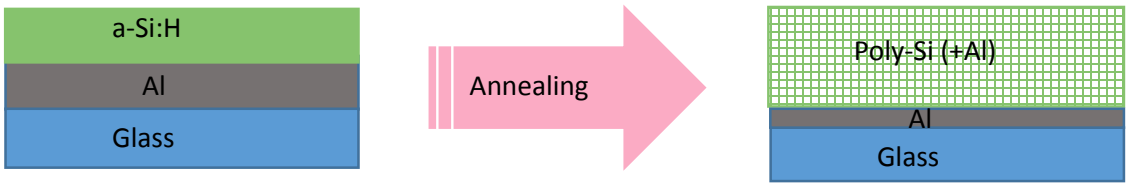

Figure 3. A schematic diagram of AIC fabrication process.

2.2.2 Top-Down Aluminum Induced Crystallization (TAIC)

The reverse aluminum-induced crystallization (R-AIC) or top-down aluminum-induced crystallization (TAIC) has an opposite configuration than the normal aluminum-induced crystallization (AIC). It starts with a glass substrate and then a-Si:H is deposited on it and lastly is an Al layer. The configuration can be written as (glass/a-Si/Al). The resulting structure will be (glass/Al/poly-Si) as shown in Figure 4.

The smooth surface of seed layers that have been prepared using TAIC is a definite advantage. Silicon islands that are present in AIC, on the top layer in this case, are underneath the poly-silicon layer, which means no further removal process is required. In addition, another advantage of TAIC is the very conductive layer that is formed on glass and can be utilized as a back contact in the solar cell. This highly conducting layer reduces resistance, which results in higher efficiency of the solar cell[26] .

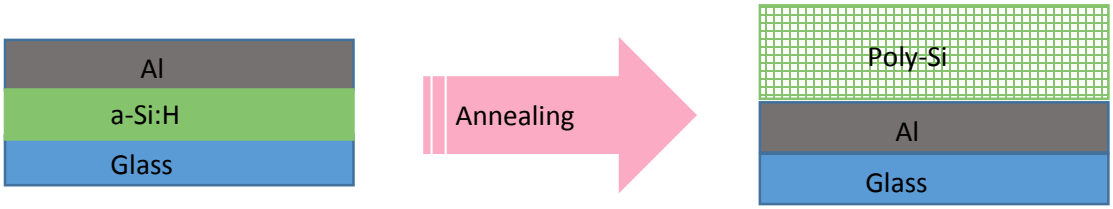

Figure 4. A schematic diagram of TAIC fabrication process.

Chapter 3: Literature Reviews

3.1 Epitaxial Growth of Si on c-Si

In 1999, Thiesen et al. [21] successfully performed epitaxial growth at temperatures ranging from 195˚ to 325 ˚C. They used c-Si as a substrate that was cleaned using the RCA cleaning procedure. The cleaned substrate was loaded in a chamber which was then evacuated to $3x10^{-7}$ torr.

When the filament reached a temperature between 1800˚ and 2200 ˚C, SiH_4 gas was introduced to the chamber with a flow rate of 5-40 sccm and pressure of 5 and 40 mtorr with different growth times. They reported an epitaxial layer up to 4500 Å thick and stacking faults were observed in the film. The experiment was done using only pure SiH_4 without any additional H_2[21].

In 2000, Seitz and Schroder[30] studied the effect of filament temperatures on the dissociation of SiH_4 and the radicals that were formed, and how it affected the deposition rate. They found that deposition rate, substrate temperature, and gas pressure determine the formation of c-Si, a-Si, or mixed phase.

They observed the formation of a mixed phase of amorphous silicon and crystalline silicon at a deposition rate of 2 Å sec^{-1}. Also, there was a linear decrease in the crystalline volume fraction during the deposition. Furthermore, the epitaxial growth had been achieved as the deposition rate went down to 1Å sec^{-1} at a substrate temperature of 300˚C without having surface roughening and stacking faults. They also noticed that the epitaxial films had a low density of defects near the c-Si and epitaxial film interface[30].

In 2003, Mason et al. [31] achieved the epitaxial growth of thin Si film by HWCVD on Si substrate at low temperatures (300 ˚C). They deposited a 300 nm thick Si film on silicon

substrate and SiO_2 substrates using 20 sccm of H_2 at a pressure of 70 mtorr and SiH_4 diluted in hydrogen with flow rate and pressure of 20 sccm and 100 mtorr, respectively. The filament in this experiment was at a distance of 5 cm from the substrate and heated to 1850 ˚C.

The results of the work of Mason et al. confirmed the existence of epitaxial growth using TEM cross section. However, the film-substrate interface was rough, which was expected due to the effect of the surface etching process by atomic hydrogen during the growth. After the epitaxy continued growing to a thickness of 240 nm, the film's structure changed to highly twinned[31].

In 2005, Richardson et al.[32] used a high hydrogen partial pressure dilution ratio of 50:1 in order to promote crystalline growth. They used tungsten wire of 0.5 mm diameter placed at a distance of 2.5 cm from the substrate.

The wire temperature was 1800 ˚C with a growth rate of 1Å sec^{-1}, while the substrate temperatures were set from 300˚ to 475 ˚C. They observed four phases of growth with this dilution ratio and temperatures. They derived a phase diagram which is a plot of the substrate temperatures against the thickness from their results that showed the four phases. At 300 ˚C, epitaxial phase and twinned phase were the most dominant phases with polycrystalline growth occurring at 1 and 2 micron thickness.

The epitaxial and twinned phases no longer existed as the temperature was increased, while the polycrystalline Si growth occurred at smaller film thickness. They believed that this was due to contamination in the chamber[32].

3.2 Epitaxial Growth on Seed Layers

In 2005, Stradal et al.[33] used the University of New South Wales's (UNSW) system to produce large-grained polycrystalline seed layers on borofloat glass substrate using the

aluminum induced crystallization method at temperatures below 500˚C with a deposition rate of 10 Å sec^{-1}.

The seed layer had a thickness of 150-300 nm. The resulted grains have three major orientations, which were (100), (220), and (311). The (220) and (311) orientations are not as easy as (100) grains to grow epitaxial layer.

For the epitaxial growth, they cleaned the seed layers with piranha etch followed with HF dip to enable achieving a thick epitaxial layer. The epitaxial growth was done using HWCVD in PASTA, multi-chamber Ultra–high vacuum system. They achieved epitaxial growth at a temperature of 370˚C with a deposition rate of 1Å sec^{-1}.[33].

In 2007 another group Lee et al. [22] fabricated the epitaxy layer on polycrystalline layer using two steps for the preparation. First, they prepared the seed layer on oxidized Si wafers using vapor induced crystallization (VIC) method. In the VIC method, two heating zones were used for heating and annealing. The source consist of $AlCl_3/NiCl_2$ (10:1). The temperatures that were used for evaporation and annealing during the crystallization of a-Si were 200 ˚C and 480-500˚C for 60 min. The second step was the growth of 40 nm of epitaxial Si in the HWCVD at a filament temperature of 1900 ˚C. During this step, 20% silane diluted with Ar gave a deposition rate of 2.6 Å/s at 450 ˚C of substrate temperature.

The vacuum pressure and chamber pressure are $5x10^{-7}$ torr and 100 mtorr. The XRD showed strong diffraction peaks of Si <111>, <220>, and <311>. From planar and cross-sectional TEM analyses, epitaxial Si by HWCVD at 450°C was successfully grown on the poly-Si seed film. They also found that the two steps helped in reducing the concentration of Ni and Al at the surface of the poly-Si[22].

In 2011, Young et al.[24] used two types of surfaces, n^+ Si:P wafers and LT c-Si films oxide-bonded Corning glass (SiOG) to investigate the influence of the different seed layer types in obtaining low-defect density epitaxial films. Then, they explored the effect of material quality and device characterization on these two substrates. They used hot wire CVD for epitaxial growth on the LT seed layer at temperature ranges from 650– 830˚C. They used a heterojunction structure and hydrogenated amorphous silicon to form the emitter of the solar cell device.

Also, they used In_2O_3: Sn film as a transparent conducting contacting layer and an antireflective coating. For the solar cell device that was formed on n^+ Si:P wafers, the contact was made directly with the highly conducting wafer with no need for the n^+ layer. The result of the solar cell device on LT c-Si films oxide-bonded Corning glass (SiOG) was an open-circuit with voltages (V_{oc}) above 560 mV.

The reason behind the high voltage is the low-defect epitaxial Si (epi-Si) growth and effective hydrogen passivation of defects. The open circuit voltage of solar cell devices that was formed on n^+ Si:P wafers was around 630 mV with efficiency of 8% with no dependence on light trapping features[24].

The National Renewable Energy Laboratory (NREL) has conducted much research on HWCVD epitaxial growth on AIC seed layers. In 2007, NREL worked with Hahn-Meitner-Institute in Berlin, Germany on epitaxial growth of Si on poly-crystalline Si seed layers on glass[34].

The seed layers that were produced using the AIC method were large grained poly-Si thin layer that had grain size of about 10 μm. They first deposited a 300 nm thick Al layer on borosilicate glass and then a-Si layer that had thickness of 375 nm. After annealing and layer

exchange during this annealing, a poly-crystalline Si layer was achieved. Chemical mechanical polishing was done to remove the top Al(+Si)layer.

Then, NREL cleaned the seed layers before the epitaxial growth in an organic solvent, with the oxide on the surface being removed by HF dip for 30 seconds. In the HWCVD chamber, the base pressure reached down to 10^{-6} torr. The W filament was heated to 2100 ˚C and the flow rate of SiH_4 was 20 sccm with no additional hydrogen being introduced in the chamber. Also, they added an additional filament of Ta to heat the substrate. At a chamber pressure of 10 mtorr and 5 min. deposition time, they reported an epitaxial growth of 0.5 μm at 670 ˚C.

They confirmed their results using SEM images for the seed layer before and after epitaxial growth. The grain boundaries were visible and both results have similar grain size, which confirmed the epitaxial growth. Their TEM results gave interesting observations at the interface. The propagation of the film was not normal and was attributed to the difference in the growth rate for each orientation.

They suggested that this growth rate difference could be helpful to grow larger grains since the faster growing grains could surpass slower growing grains. Additionally, they noted some defects and nucleation at the epitaxy/seed interface. There was not a breakdown into a-Si or poly-Si phase in the only first 600 nm of deposition which requires further optimization in order to use them in solar cells[34].

In 2010, NREL[35] fabricated an epitaxial layer on display glass using HWCVD for solar cell applications. Their results indicated that decreasing the substrate temperature leads to an increase in the defect density. However, they achieved an epitaxial layer of approximately 2 μm at low dislocation densities of 6×10^{-4} cm^{-2} using HWCVD at substrate temperature of 760 ˚C.

They reduced the dislocation densities using hydrogenation treatment to passivate the surface prior to epitaxial growth. As a result, the efficiency of solar cell had been improved due to decreasing defects and contamination on the surface[36].

The cooperation between NREL and Corning Incorporated resulted in an epitaxial Si solar cell that has open-circuit voltage (V_{oc}) > 560 mV. They accomplished this high voltage because of the high quality epitaxial layer with low defects as a result of the hydrogenation treatment. Since the temperature of the Corning glass that they used as a substrate cannot tolerate the high temperature of hydrogen annealing, they examined two ways to smooth the surface. The first approach was a chemical mechanical polishing, being careful not to remove the 600 nm thick film.

Using this technique, grooves were present in the surface, which are not desired. Thus, the other approach was explored, which was annealing the seed layer at 800 ˚C in hydrogen for 30 min. However, this method did not provide sufficient results of decreasing the roughness of the film. Their previous research showed oxide on the surface prior to the deposition in the HWCVD chamber, which creates dislocations in the grown epitaxial layer. Thus, HWCVD was used to deposit epitaxial layer of Si, using oxygen-filtered SiH_4 in response to their previous findings [24].

Wu et al in 2012 [37] accomplished grain size of 700 nm using the AIC method. At room temperature Al was deposited on Corning glass substrate at a thickness of 500 nm using an E-Beam evaporator. Then, buffer oxide etching diluted in deionized water for 30 seconds was performed to remove Al-oxide. After that, the sample was exposed to ambient air for 24 hours to form Al-oxide.

The process of removing Al-oxide before the exposure to ambient air ensured the same oxide thickness in all the samples. After that, HWCVD was utilized to deposit an a-Si layer 300 nm thick. Raman results demonstrated that increasing annealing temperature and duration could help to obtain higher crystallinity[37].

In 2013, Gestel et al.[38] reported that seed layers with large grains up to 100 μm had been achieved. They used AIC in order to crystallize a-Si on flowable oxide that was coated with alumina or SiO_2 using an E-beam evaporator.

They deposited Al first with 250 nm thickness which was then exposed to ambient air to form Al-oxide. After that, a-Si with 270 nm thickness was deposited on the Al-oxide. Annealing was performed to obtain large grained poly-crystalline Si seed layer at 500 ˚C for four hours.

Then, wet chemical etching was used to remove the Al layer that was on top of the seed layer. For the epitaxial growth, they used high temperature atmospheric pressure chemical vapor deposition (APCVD) at 1130 ˚C. Passivation was done using hydrogen to enhance the performance of the solar cell and plasma texturization to trap the light[38].

The Silicon Materials and Devices Group and NREL [39] achieved epitaxial growth of Si on seed layer on display glass, dead wafers and oxide coated metal foil substrates at 620 ˚C to 800 ˚C. They accomplished epitaxial growth at a thickness of 2.5 μm on dead Si substrate. Although the substrate was not hydrogenated and did not have any light trapping textured, open circuit voltage in 2 μm solar cell was 0.57 V.

The dislocation densities was lowered to 6×10^{-4} cm^{-2} by reducing the surface impurities at the initial stage of growth. The seed layers were obtained using AIC that was prepared by the Hahn-Meitner Berlin group, and the grain size was above 10 μm. Then, HWCVD was used to grow an epitaxial layer of Si at 670 ˚C.

The epitaxial layer was attained without significant breakdown in the grown layer. From their results, they developed a model that describes their epitaxial growth. This model suggested that even at higher deposition rate, epitaxial growth can be achieved. Also, they believed that with few modifications this model could be applied to any material[40].

Epitaxial growth on poly-crystalline seed layers has a great potential to compete with other photovoltaic technologies that dominate the market right now. Further investigation is significant in order to optimize this technology. The goal of this research was to fabricate larger grained heavily doped p-type poly-crystalline Si seed layer on inexpensive substrate. Then, the subsequent step was the growth of epitaxial layer of Si on this seed layer at low temperature. Achieving these objectives could have a great impact on the photovoltaic industry and could replace the dominant technologies such as c-Si solar cells.

Chapter 4: Experimental Methodology and Equipment

4.1 Growth and Processing Approach

This chapter presents the methods and parameters that were used in order to deposit Si on c-Si substrates, glass, and ITO coated glass substrates. Figure 5 is a flow chart that shows the steps of c-Si deposition used to achieve the epitaxial growth on large grained polycrystalline seed layers. The ITO glass was used in this order to get a back contact for the fabrication of solar cells in future work.

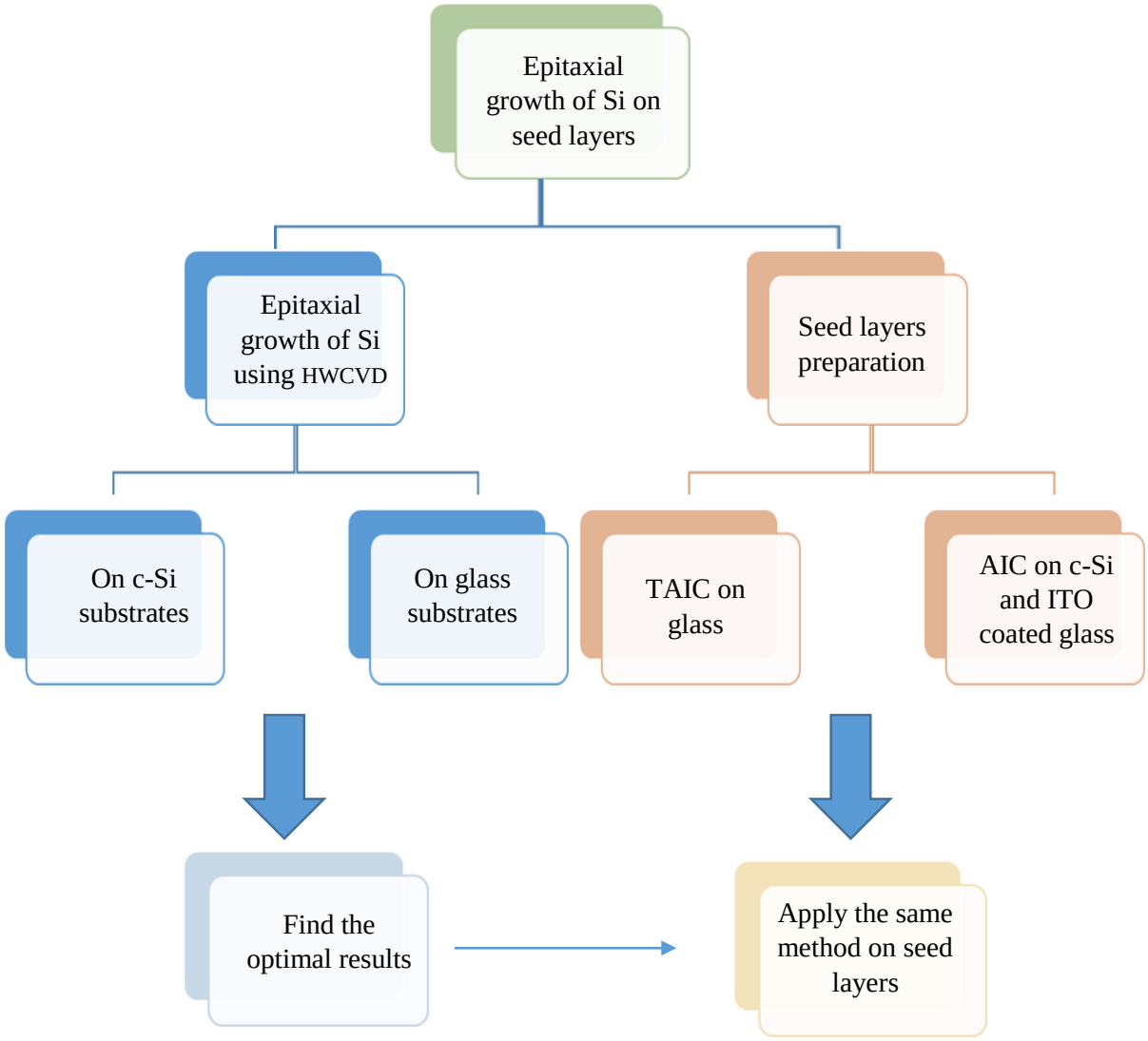

Figure 5. A schematic diagram of the methodology that had been performed in order to obtain the objective of this work.

Figure 6 shows a schematic diagram of the experimental procedure that was followed in this work from seed layer preparation to epitaxial growth. Step one was to understand epitaxial growth of Si at low temperatures using the HWCVD technique on c-Si substrate. Step two was epitaxial growth on AIC large grained seed layers on glass.

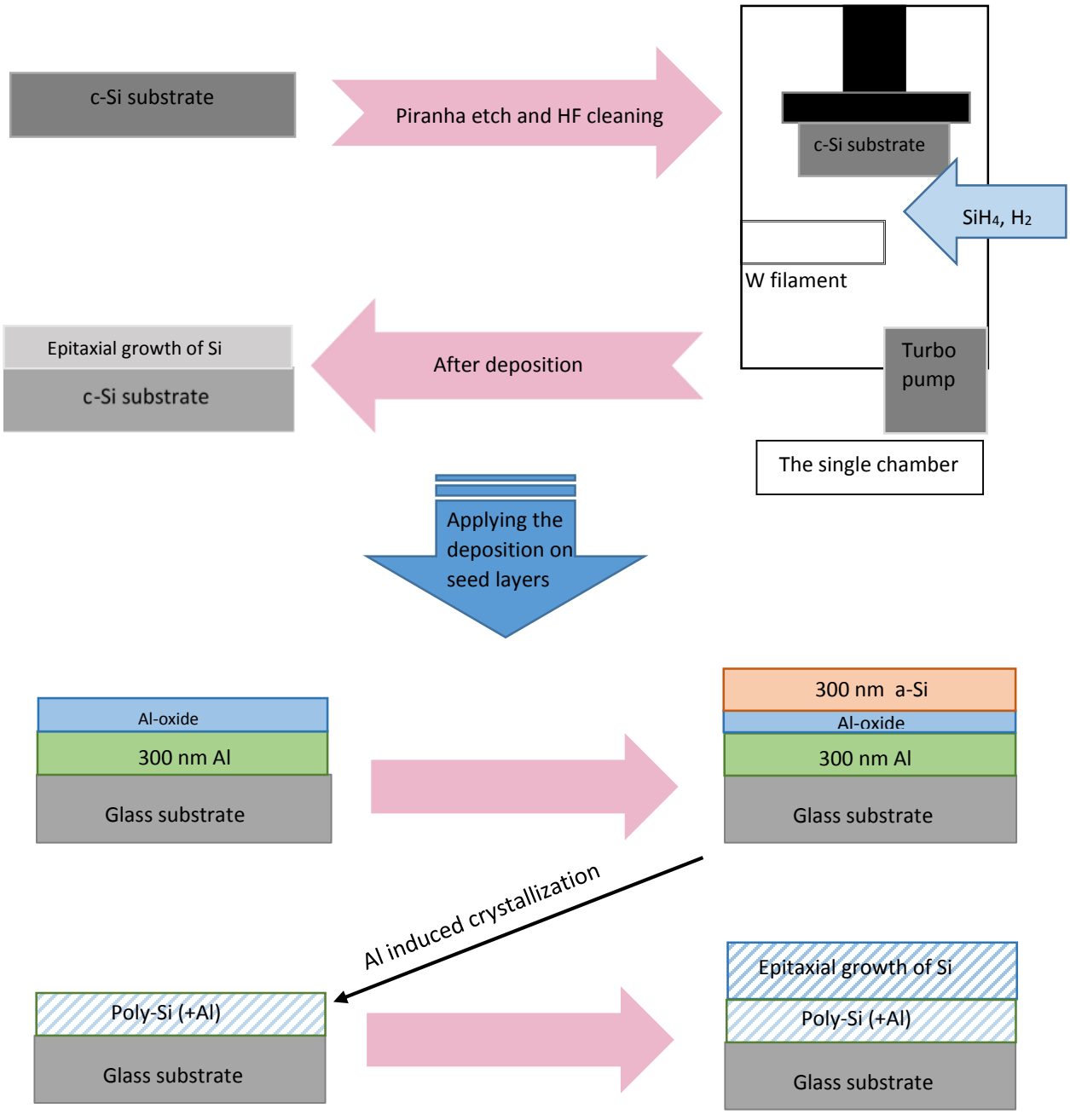

Figure 6. A schematic diagram of the experimental process.

4.2 Detailed Growth Steps

4.2.1 Epitaxial Growth of Si on c-Si and Glass

Before the deposition process, the substrates must be cleaned, due to the very sensitive nature of the growth to any organic contamination or oxidation and water vapor on the surface. Contamination on the surface can prevent epitaxial growth.

4.2.1.1 Substrate Cleaning

There are different methods of cleaning samples depending on whether they are glass or c-Si substrates, and also geared toward specific types of contamination (silicon dioxide, organic contamination such as fingerprint, or water vapor).

4.2.1.1.1 Crystalline Si Substrate Cleaning

Before loading the silicon samples into the chamber, they were cleaned in a two-step process. The first step was Piranha etch which is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in a 50:50 ratio. Piranha etch was used to clean the Si surface from any organic contamination such as fingerprints. Then, the second step was using hydrofluoric acid (HF) with deionized (DI) water in a 1:10 ratio to clean the surface of the Si from silicon dioxide (SiO2).

4.2.1.1.2 Borosilicate Glass (Corning 1737) Cleaning

Ultrasonic bath was used to clean borosilicate glass (Corning 1737) substrates to remove organic contamination. “Sonication is a process in which sound waves are used to agitate particles in solution. Such disruptions can be used to mix solutions, speed the dissolution of a solid into a liquid (like sugar into water), and remove dissolved gas from liquids”[41].

Ultrasound waves with frequencies above 20 kHz are typically used in sonication baths. Glass samples were immersed in heated acetone at 40 °C for 10 min. then dried using a nitrogen

gun. The samples were immersed for 10 min. a second time but in heated methanol at 40 °C, and a steady stream of nitrogen was used as the final step to dry the samples.

4.2.1.2 Epitaxial growth of Si on c-Si and glass substrates

As mentioned in chapter one, the goal of this work was to achieve epitaxial growth on large grained polycrystalline silicon seed layers. To accomplish this goal, there were different growth processes to fully understood how to get the epitaxial layer on the ideal substrate and to accomplish the optimal results.

At first, the HWCVD technique was utilized to deposit Si on p-type c-Si substrates with an orientation of (100). Parameters were varied to optimize the results, such as substrate temperatures and dilution ratio (by either changing the SiH_4 flow rate or the H_2 flow rate). Tables 2,3,4,5, and 6 show the conditions that were used during the growth.

Table 2. Parameters used during epitaxial growth using HWCVD system by varying the dilution ratio.

Sample code	SiH_4 flow rate (sccm)	H_2 flow rate (sccm)	Time (min)	Substrate temperature (˚C)	Filament temperature (˚C)	Chamber pressure (torr)
HW1	5	0	30	400	1900	0.1
HW2	5	5	30	400	1900	0.1
HW4	5	10	30	400	1900	0.1
HW5	5	30	30	400	1900	0.1

Table 3. Parameters used during epitaxial growth using HWCVD system by varying the substrate temperature.

Sample code	SiH_4 flow rate (sccm)	H_2 flow rate (sccm)	Time (min)	Substrate temperature (˚C)	Filament temperature (˚C)	Chamber pressure (torr)
HW3	5	10	30	400	1900	0.1
HW4	5	10	30	600	1900	0.1
HW5	5	10	30	500	1900	0.1
HW6	5	10	30	700	1900	0.1
HW7	5	10	30	750	1900	0.1

Table 4. Parameters used during epitaxial growth using HWCVD system by increasing the dilution ratio.

Sample code	SiH_4 flow rate (sccm)	H_2 flow rate (sccm)	Time (min)	Substrate temperature (˚C)	Filament temperature (˚C)	Chamber pressure (torr)
HW8	1	200	30	600	2200	0.4
HW9	2	200	30	600	2200	0.4
HW10	4	200	30	600	2200	0.4
HW11	6	200	30	600	2200	0.4

Table 5. Parameters used during epitaxial growth using HWCVD system by varying the growth temperature at fixed SiH_4 flow rate of 1 sccm.

Sample code	SiH_4 flow rate (sccm)	H_2 flow rate (sccm)	Time (min)	Substrate temperature (˚C)	Filament temperature (˚C)	Chamber pressure (torr)
HW12	1	200	30	550	2200	0.4
HW13	1	200	30	600	2200	0.4
HW14	1	200	30	650	2200	0.4
HW15	1	200	30	700	2200	0.4

Table 6. Parameters used during epitaxial growth using HWCVD system by varying the growth temperature at fixed SiH_4 flow rate of 2 sccm.

Sample code	SiH_4 flow rate (sccm)	H_2 flow rate (sccm)	Time (min)	Substrate temperature (˚C)	Filament temperature (˚C)	Chamber pressure (torr)
HW16	2	200	30	550	2200	0.4
HW17	2	200	30	600	2200	0.4
HW18	2	200	30	650	2200	0.4
HW19	2	200	30	700	2200	0.4

4.2.2 Epitaxial Growth of Si on Seed Layers

Seed Layer Preparation:

Crystalline Si substrates (100) and ITO coated glass substrates were prepared to serve as a seed layer for the following step. Then, the following step was an epitaxial growth on the seed

layers using HWCVD. Two methods of seed layer preparation were examined: aluminum induced crystallization (AIC) and top down aluminum induced crystallization (TAIC).

4.2.2.1 Top-down Aluminum Induced Crystallization (TAIC)

In this research, top-down aluminum induced crystallization (TAIC) seed layer was formed on glass samples (Corning 1737). Then, hot wire chemical vapor deposition technique was used to grow an epitaxial layer.

The TAIC method began with depositing a thin layer (300 nm) of a-Si:H on the oxide layer. Afterward, the sample was exposed to air for 10 minutes and then exposed to oxide plasma for one second.

A thin layer of aluminum (140 nm) was deposited on the previous layers using a thermal evaporator. After that, IR-belt furnace was used to anneal the sample at different zone temperatures as the belt was moving (Zone 1 = 200 °C, Zone 2 = 500 °C, Zone 3 = 500 °C) in order to initiate a layer exchange process. It is believed that the oxide layer serves as a substrate so that it can restrict silicon atoms from diffusing into the glass sample.

4.2.2.2 Aluminum Induced Crystallization (AIC)

An inverted configuration, called aluminum induced crystallization (AIC) was performed to get large grained polycrystalline silicon seed layers. In this method, the order of the deposited layers was glass/aluminum/Al-oxide/a-Si:H and the final structure after annealing was glass/polycrystalline Si/Al-oxide/ aluminum. Here is the detailed process of the AIC method for the seed layers in preparation for the subsequent step.

4.2.2.2.1 Al Deposition

A 300 nm thick layer of Al was deposited on c-Si substrates and ITO coated glass using an E-beam evaporator. The samples were then exposed to the ambient air for different periods of

time ranging from 1-10 days. Exposure time to the atmosphere was varied to study its effect on the crystallization process.

4.2.2.2.2 Amorphous Si Deposition

A 300 nm thick layer of a-Si:H (same thickness of aluminum layer) was applied on the Al-oxide layer. Plasma enhanced chemical vapor deposition (PECVD) was used to create the a-Si:H layer at a power of 4 Watt. The substrate temperature was 250 °C and at base pressure of 2.3×10^{-7} torr. The flow rate of SiH_4 was 20 sccm for 21 minutes deposition time.

4.2.2.2.3 Annealing System

Infrared belt furnace (IR-belt furnace) was utilized to anneal the samples in order to initiate the layer exchange. Further information is provided in the next section. The samples were exposed to three zones of temperatures in this furnace. The first zone was 350°C, the second zone was 500°C, and the third zone was 350°C. After about 8 hours of annealing, the Al segregated into the amorphous Si layer, which results in crystallization of the a-Si layer.

4.2.2.2.4 Al Etching

After a complete layer exchange had been done, the Al layer had to be removed. A wet chemical etching was performed using Al etchant type D. It is basically a composition of phosphoric acid, Sodium-M-Nitrobenzene Sulfonate, acetic acid, and water.

Optical microscope, and SEM images were taken before etching the Al layer. Then, the samples were immersed in the Al etchant type D at 50 ˚C for 40 seconds.

4.2.2.2.5 Seed layers Cleaning

Before the epitaxial growth, the samples had to be cleaned to remove the silicon dioxide layer. The c-Si substrates were dipped in HF for 30 seconds.

4.2.2.2.6 Epitaxial growth

When heavily p-type doped polycrystalline Si seed layers were complete, the samples were ready for epitaxial growth by using HWCVD. The optimal results from Si deposition on c-Si substrates were applied on the seed layers.

4.3 Deposition Equipment

4.3.1 Hot-Wire Chemical Vapor Deposition (HWCVD)

The hot –wire chemical vapor deposition process can be implemented using a single chamber system that is made up of a small stainless steel tee, which is the main vacuum. A capacitive coupled electrode was housed inside the stainless steel tee that is powered by an RF generator. A pancake heater was used to heat the substrates by placing the heater directly above the substrate inside the vacuum chamber. The rest of the vacuum parts were below the table that the tee is set on.

The gate valve separated the turbo pump from the main processing chamber. A mechanical rotary vane pump supported the turbo-molecular pump. The exhaust of the rotary vane pump was attached to the original plumbing of the building, which removed the exhaust of the rotary vane pump to the outside of the building.

A throttle valve controlled the pressure, which was manipulated via computer control. A roots blower pump directs the corrosive gas load then removed it from the chamber to the Edwards Inc. GRC gas abatement system. A manually controlled high vacuum valve was located behind the throttle valve to ensure complete separation from the roots blower pump and processing chamber. A control panel consisting of a computer and monitor, operated the throttle valve that was responsible for controlling pressure in the chamber. It also contained a switch

box, which controlled the pneumatically operating vacuum valves that were responsible for gas flow in the gas manifold.

Also, contained with the control panel were: the RF generator, SiH_4 mass flow controller, pressure measurement gauges and turbo power supplier. Mass flow controllers and manually operated valves were housed in the gas manifold. Figure 7 is a schematic diagram of the HWCVD system that was used in this work. Figure 8 is the HWCVD system that was used in this work.

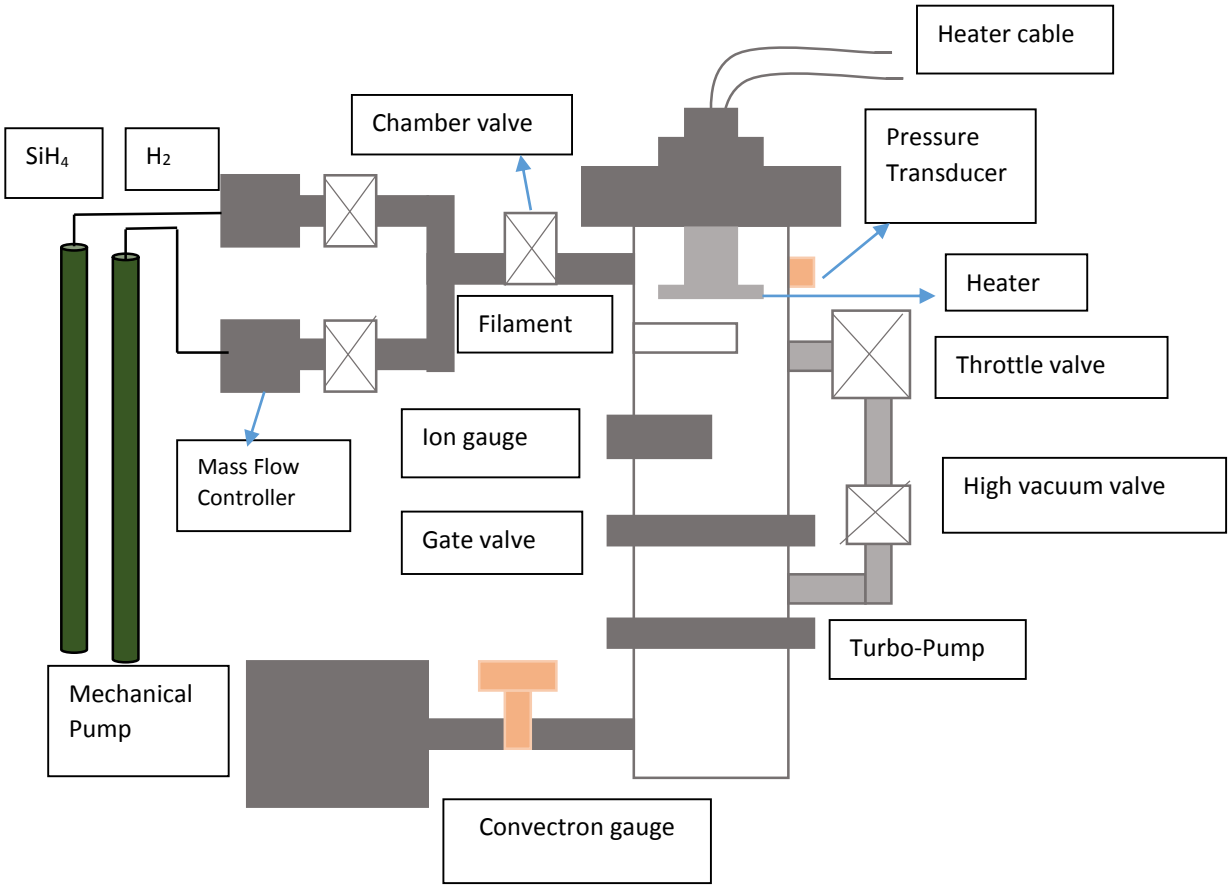

Figure 7. A schematic diagram of the single chamber that was used for HWCVD method.

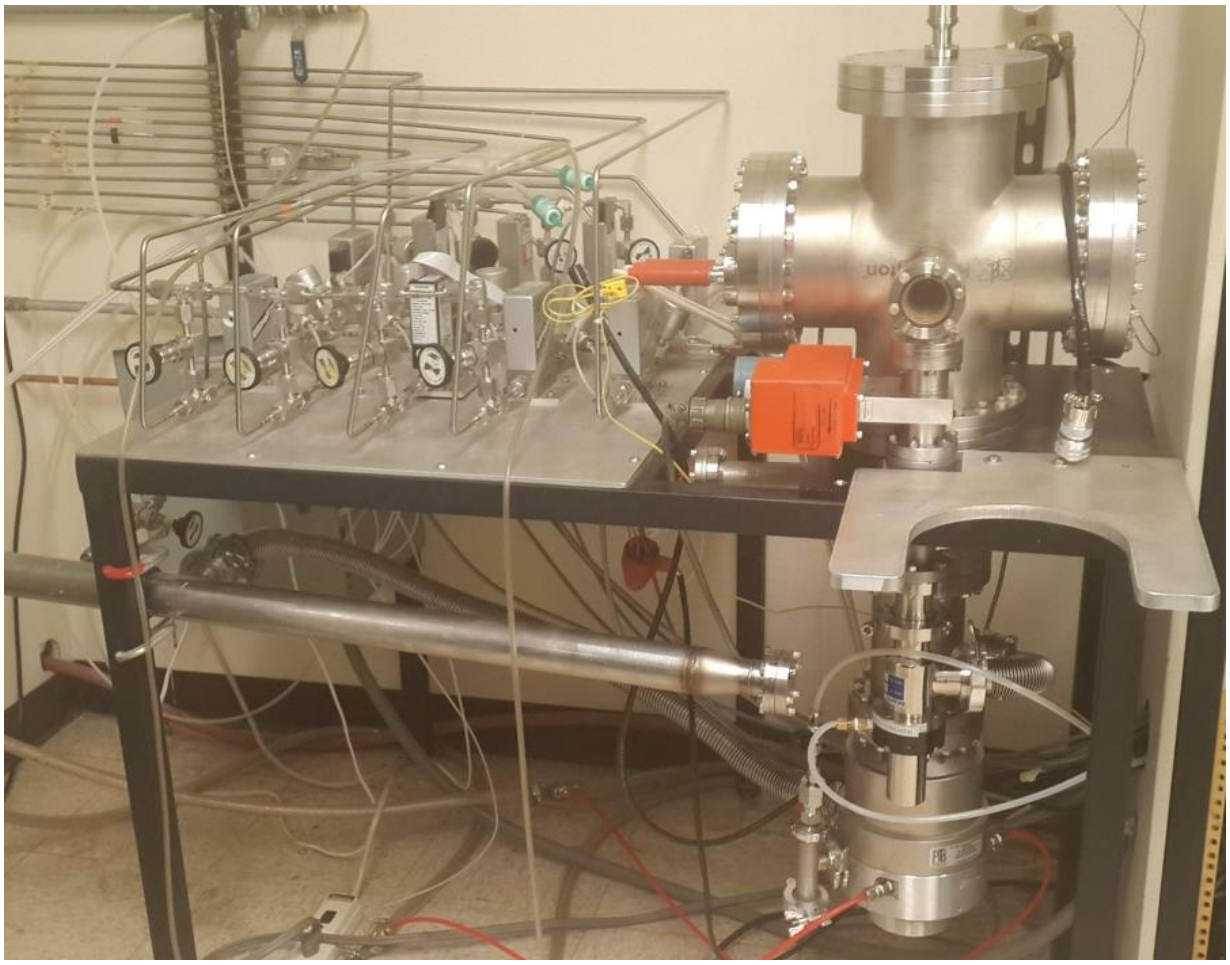

Figure 8. The single chamber that was utilized for HWCVD method in this research (picture taken by the author).

4.3.2 Multi-Vacuum System (MVS)

The system of MVS that was used in this research consists of seven stations. Each station had a different purpose than the others, as shown in Figure 9. Station seven, six and three were the stations that were used in this work. Station three and station two were used for the PECVD method. Station four and station five were used for sputtering processes, and station six was used for the E-beam evaporator.

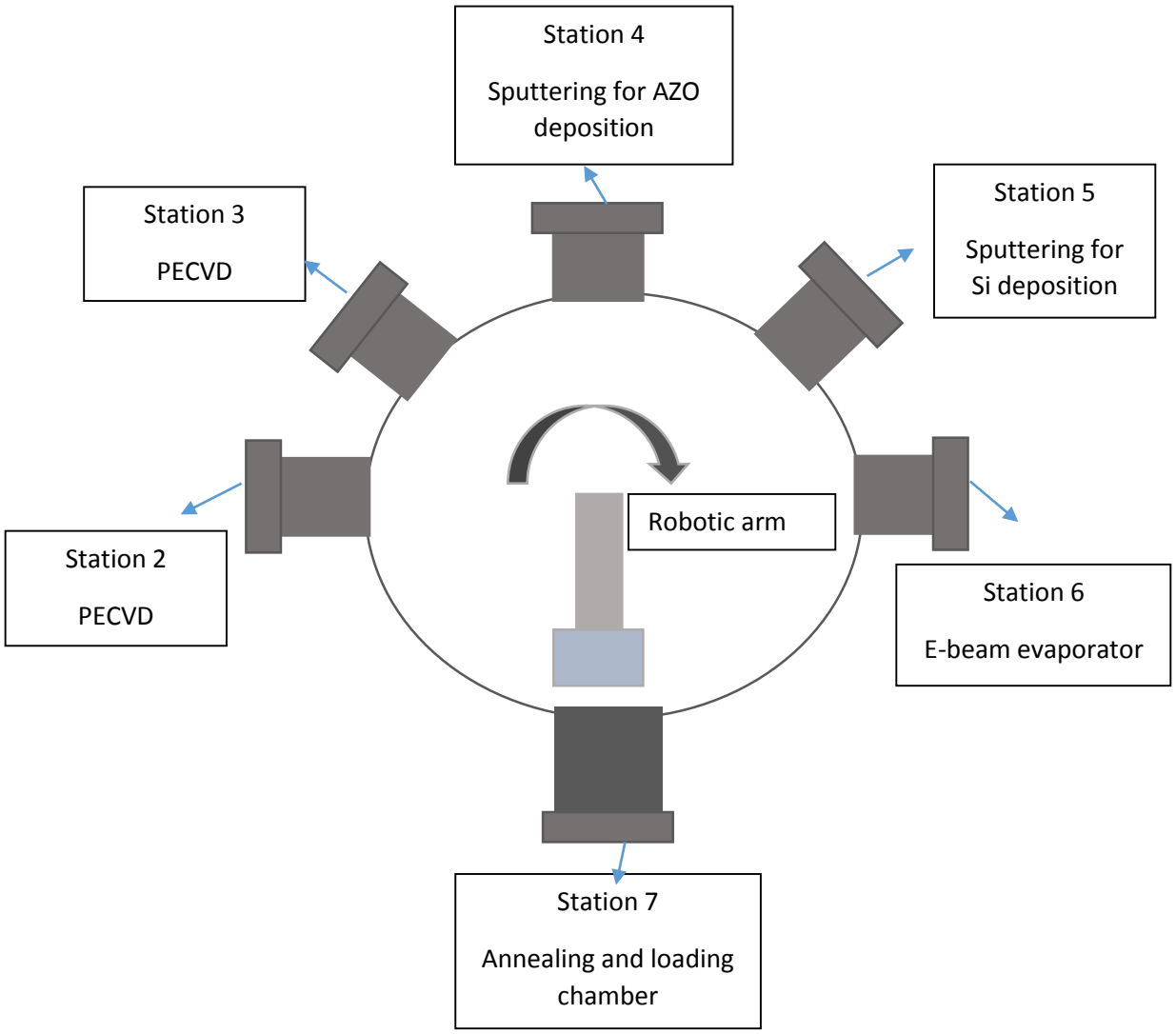

Figure 9. A diagram of the multi-chambers system that has PECVD chamber and E-beam evaporator chamber.

Station seven was where the sample was loaded and transferred to any station under vacuum. A robotic arm took the sample holder and placed it according to the command entered in the robotic arm controller. When the arm took the sample to the desired chamber, it would go back to station seven until the deposition was done. Figure 10 shows the multi chamber tool that was used in this work.

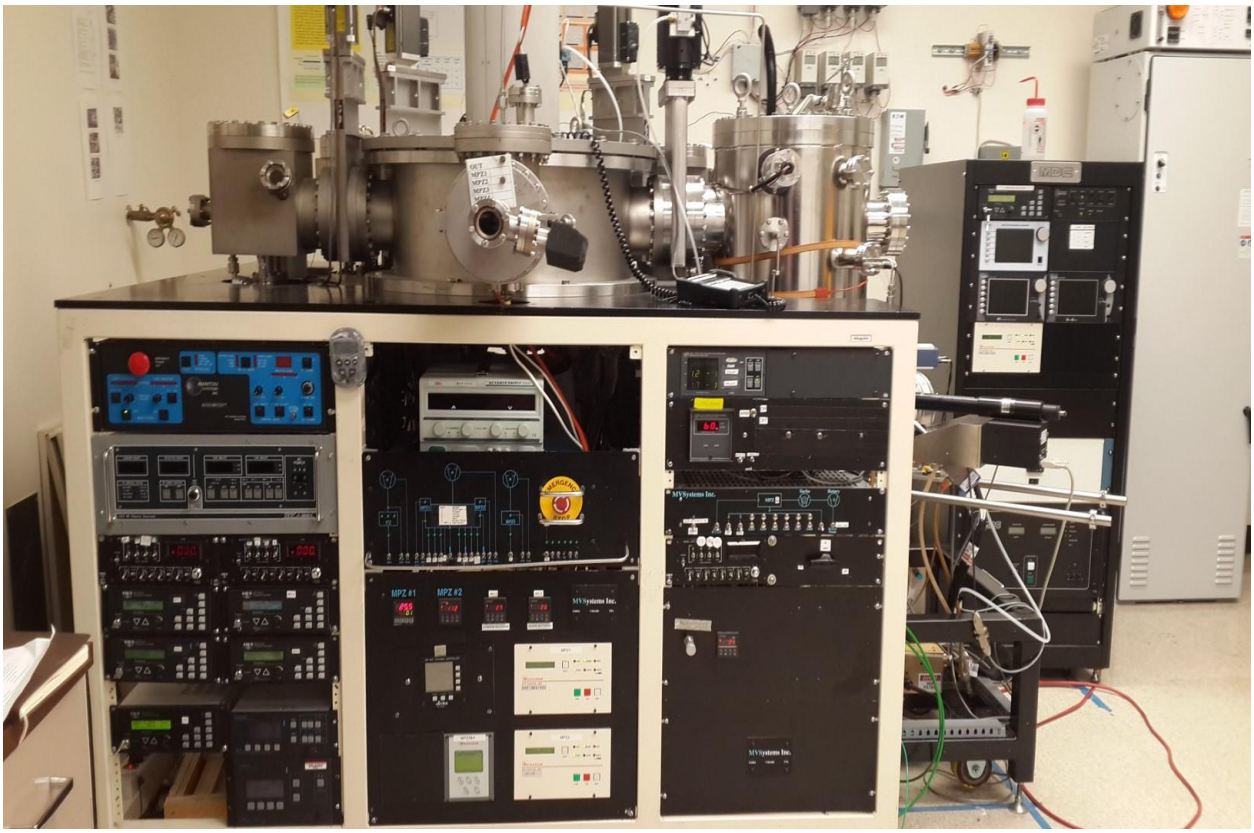

Figure 10. The multi-vacuum system that has PECVD chamber and E-beam evaporator chamber (picture taken by the author).

4.3.3 Infrared Belt Furnace (IR-Belt furnace)

The IR-Belt furnace is a long tunnel that has a moving belt which transfers the sample. There are three independent temperature zones. Control thermocouples above the moving belt that sense any change in the temperature are used to maintain the temperature in each zone. The control panel is on the front side of the furnace to power on the furnace and to set the temperatures and the speed of the belt. Figure 11 shows the IR belt furnace at High Density Electronics Center (HiDEC) that was used in this research.

Figure 11. The IR-Belt furnace at HiDEC (picture taken by the author).

4.4 Analytical Techniques

4.4.1 Raman Scattering

Raman spectroscopy is a common method utilized to characterize mixed phase Si layers. It does not require any type of sample preparation and is a non-destructive technique. Raman scattering is an inelastic scattered light when an incident photon interacts with lattice vibrations, called phonons, in the film. The interaction between the lattice vibrations and incident light results in scattering the incoming beam.

The scattered beam can have the same energy as the incident light, called Rayleigh scattering, or can be shifted and have the same energy as the photons, called Raman scattering. Figure 12 shows a schematic of Raman scattering when a light beam from a source interacts with lattice vibrations. The Raman scattering energy (V_{Raman}) is measured via a spectrometer and is subtracted from the incident beam energy (V_{Laser}) to find the lattice vibrations (Δv) according to Equation 4.1[42].

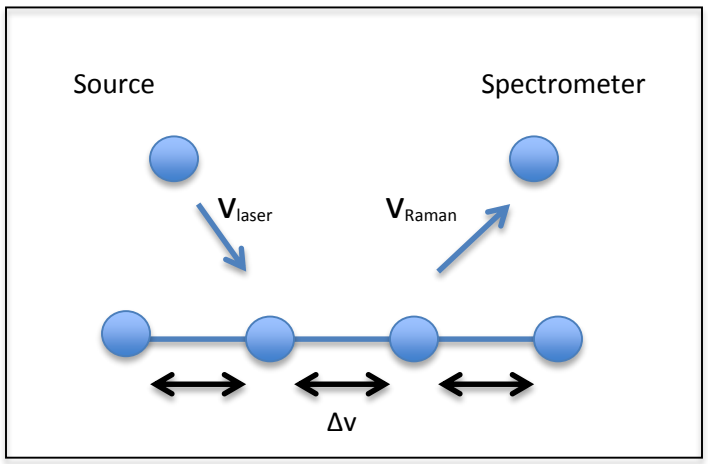

Figure 12. A schematic of Raman scattering that showed the interactions between the incident beam and lattice vibrations.

$$\Delta v\ (cm^{-1}) = V_{Laser} - V_{Raman} \qquad \text{(Equation 4.1)}$$

The crystalline quality of the Si samples in this research were characterized using Raman scattering spectroscopy with a 632 nm laser source. The uniform and symmetrical bonds of crystalline silicon generate a sharp strong peak at 520 cm^{-1}. However, amorphous silicon bonds are different with wide angles resulting in a broad peak at 480 cm^{-1}.

There are two types of scattering when light hits an atom: elastic scattering that is called Rayleigh scattering and inelastic scattering that is called Raman scattering. In Rayleigh scattering, the energy of the incident light is the same as the energy of the scattered photons. However, Raman scattering has two types based on their energy level: Stokes scattering and anti-Stokes scattering [43]. Figure 13 demonstrates Raman scattering and Rayleigh scattering. Figure 14 shows Raman setup that was utilized in this work.

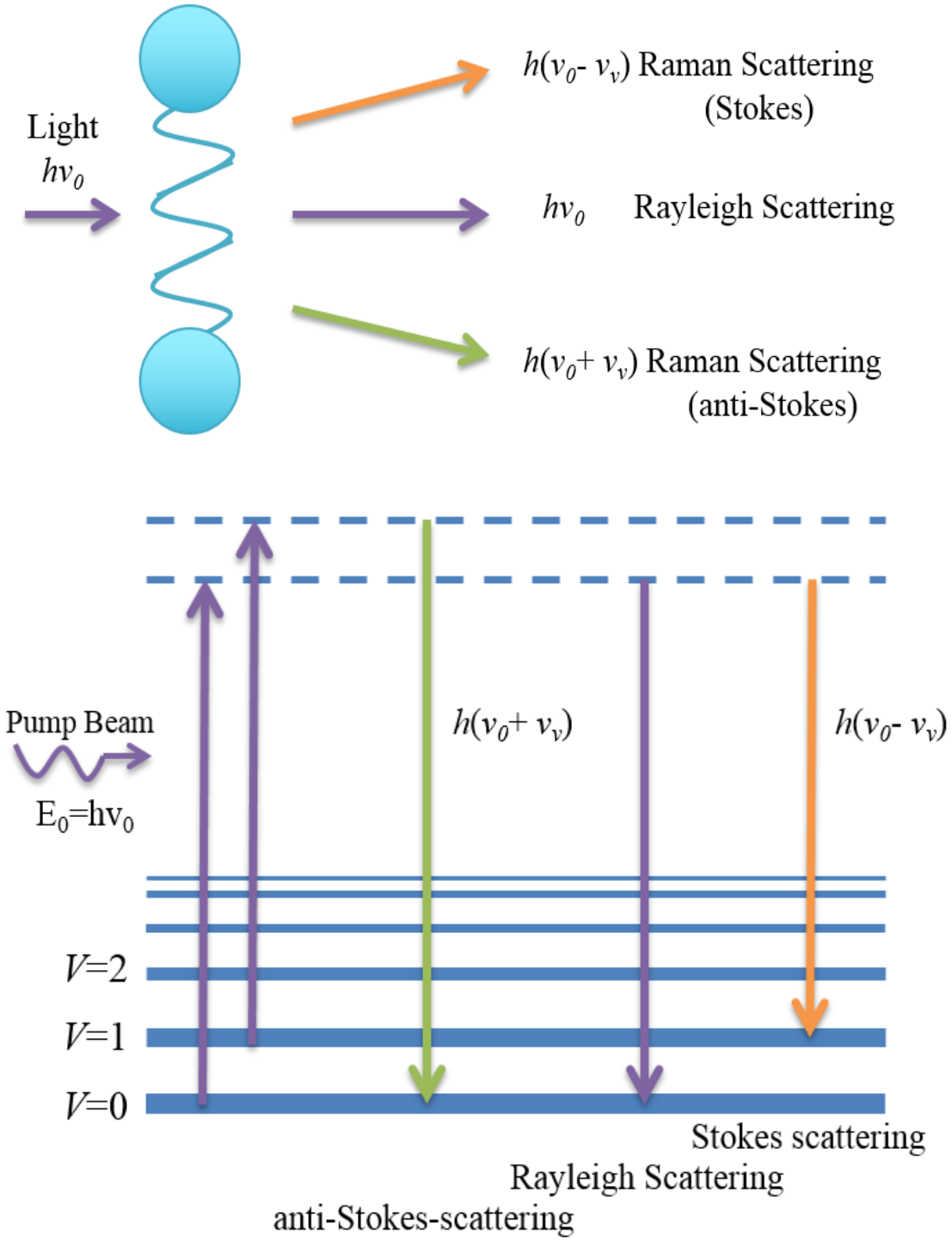

Figure 13. The interaction of the incident light and the vibration of the molecular.

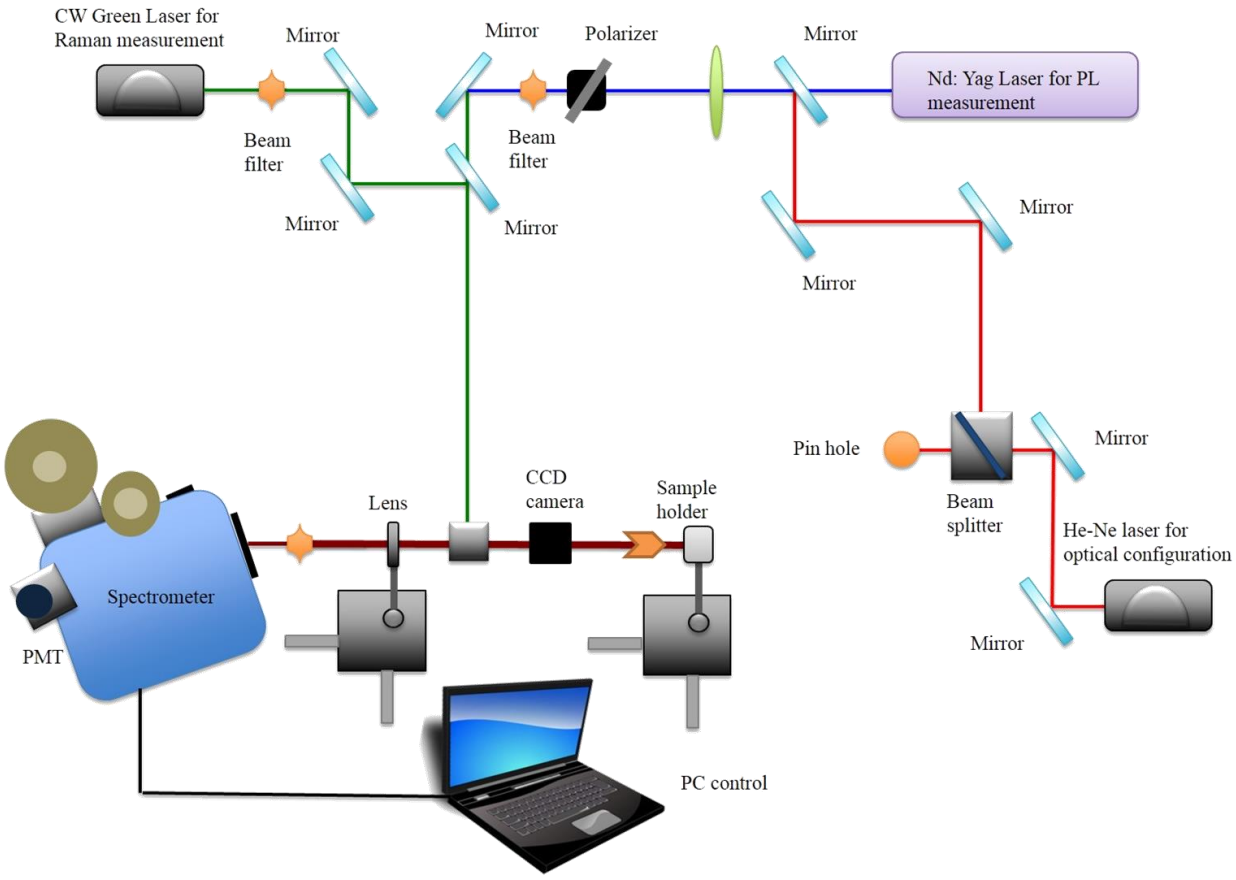

Figure 14. A schematic diagram of Raman setup that was used in this work

4.4.2 X-Ray Diffraction (XRD)

X-rays, discovered in 1895, enable the analysis of the structure of a crystal at the atomic level. X-ray is a type of electromagnetic radiation which has a wavelength similar to the height of an atom, which is about 1 Å (10^{-10} m).

X-ray diffraction was discovered in 1912. Analyzing the structure of a crystal and fingerprint characterization are two main things that have been performed using X-ray diffraction. Figure 15 shows the main parts that exist in any X-ray diffraction process which are: X-ray source, X-ray detector, and sample stage. When the X-ray hits the atoms, part of it scatters while the other part passes through to the next atomic level. Then, the X-ray in the next level

scatters partially and the other part passes through. A diffracted peak happens only when Bragg's law is satisfied [44].

$$n\lambda = 2d \sin\theta \qquad \text{(Equation 4.2)}$$

Where n is an integer number, λ is the wavelength, d is the distance between diffracted planes and θ is the angle of incidence of the X-ray. Figure 16 demonstrates the atomic levels and the X-ray interaction with the atoms.

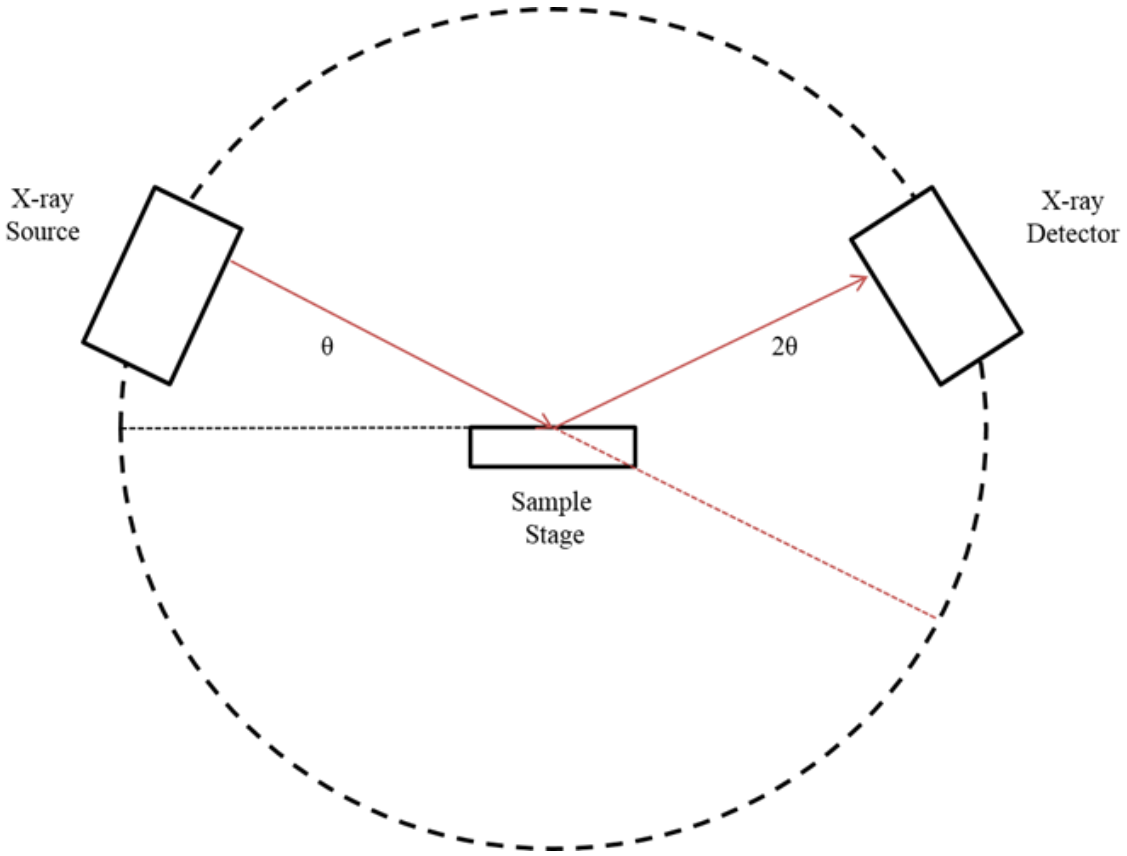

Figure 15. XRD diffraction process that consists of: X-ray source, X-ray detector, and sample stage.

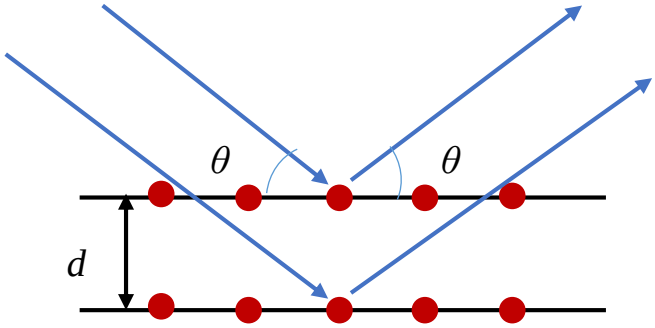

Figure 16. The atomic levels and the X-ray interaction with the atoms according to Bragg's law.

To calculate the angle the peaks of poly-crystalline Si occur, this relationship in Equation 4.3 between the spacing (d) between planes and the lattice structure (a) will be used.

$$\frac{1}{d^2} = \frac{h^2 + k^2 + l^2}{a^2} \qquad \text{(Equation 4.3)}$$

In this equation h, k, and l are the Miller indices. From Equation 4.2 and Equation 4.3 this relationship between theta and the Miller indices can be derived as follow.

$$\sin^2\theta = \frac{\lambda^2}{4a^2}(h^2 + k^2 + l^2) \qquad \text{(Equation 4.4)}$$

The sum of the Miller indices is always an integer number and the lattice constant (a) of Si is 5.42 Å. Using Equation 4.4, the orientations and their corresponding peaks angles can be calculated. Table 7 shows silicon XRD peaks and their corresponding orientations.

Table 7. Silicon XRD peaks and their corresponding orientations.

Peak	Angle (2Theta (Deg))
(111)	28.49
(220)	47.38
(311)	56.22
(400)	69.25

4.4.2.1 Grazing Incidence X-ray Diffraction

Using a small incident X-ray beam angle, the beam's penetration will be limited. Thus, grazing angle can be utilized to study the surface instead of having contribution from the substrate. In this case, the detector will be moving and measuring at different angles while the sample will be fixed as well as the incident beam. In this work, the incident X-ray beam was fixed at 3 degrees. Figure 17 shows a schematic diagram of grazing angle XRD analysis.

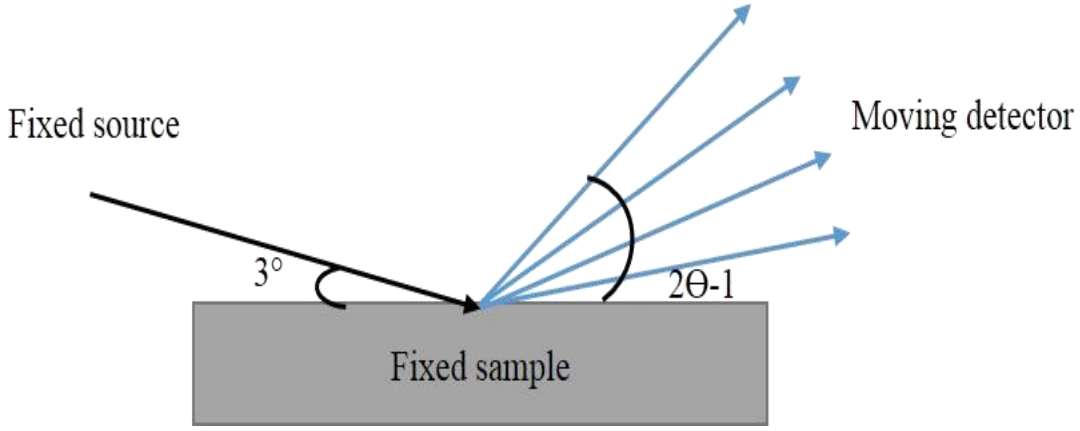

Figure 17. Schematic diagram of grazing incidence XRD.

4.4.3 Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy is a non-destructive technique that has been used to analyze a material's surface. Unlike a conventional optical microscope which forms the image using light when photons are reflected from the sample surface, SEM forms the image using electrons. The interactions between the electron beam and the atoms in the material's surface generate various signals.

These signals can be detected so that an image of the sample is formed. The SEM has a significant role in all fields which require solid material analysis. Some advantages of the SEM

over the optical microscope are the high resolution of the produced images. Based on the fact that each element emits a certain wavelength, energy dispersive X-ray spectroscopy (EDX) was utilized to analyze the sample and give a distribution curve of the materials.

Even though EDX was meant to be an examination for the materials on the surface, the produced X-ray does not come only from the surface. It penetrates deeper in the sample based on the atomic number Z of the element and the energy of the electron beam. When the atomic number is low, the penetration in the sample is deeper. However, when the energy of the electron beam is higher, the depth of the penetration increases. Figure 18 shows a standard components of SEM. Figure 19 shows SEM instrument that was used in this research.

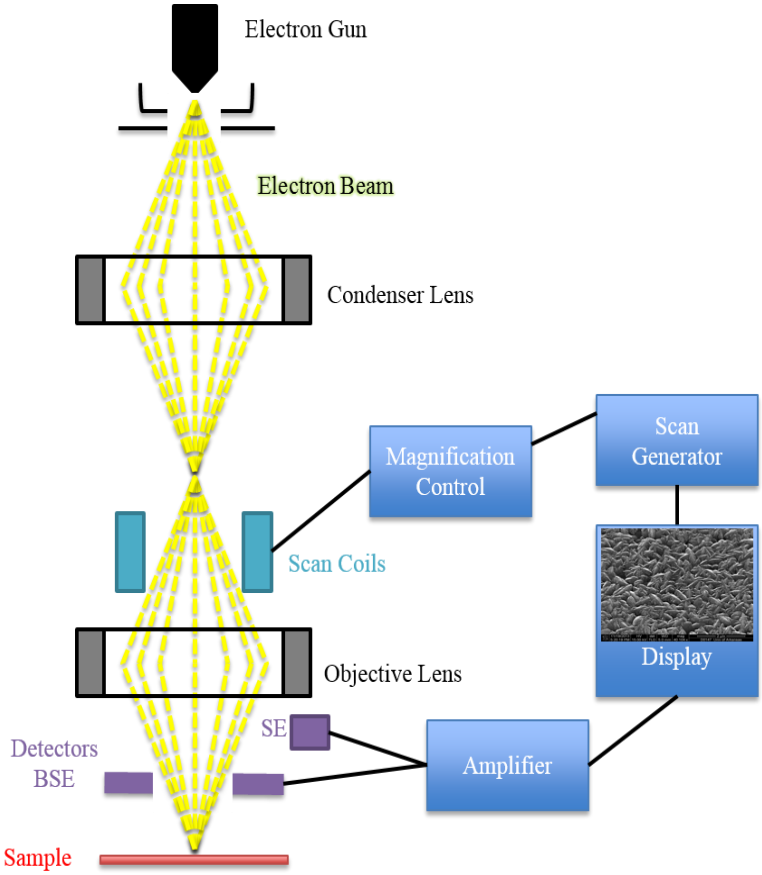

Figure 18. A schematic diagram of a standard SEM.

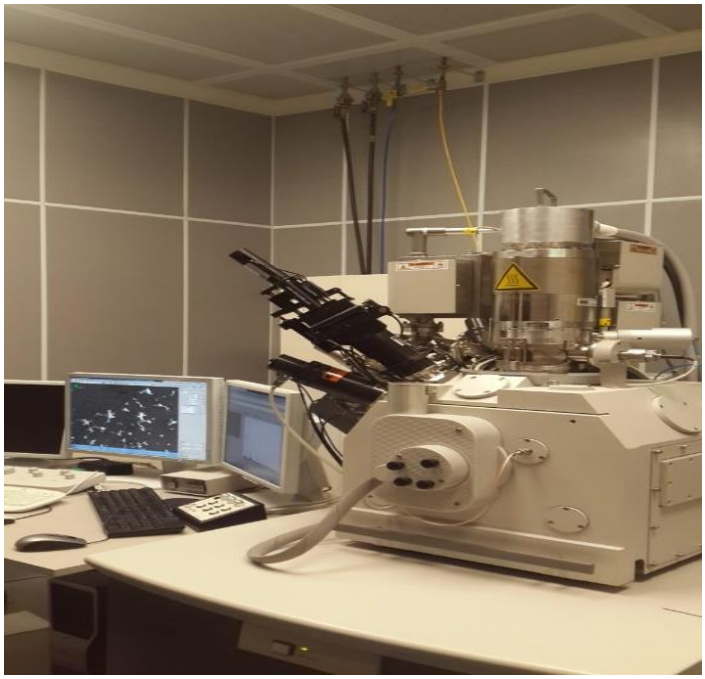

Figure 19. Scanning electron microscope (SEM) that was used in this research (picture taken by the author).

4.4.4 Transmission Electron Microscopy (TEM)

Transmission electron microscopy is similar to SEM in some aspects, such as the imagery being a result of electron interactions. However, TEM images are generated by the transmission of electrons through a sample, while SEM images are generated because of the electrons being reflected from the sample's surface. As a result, TEM samples require special treatment so that the thickness of the samples is less than 100 nm before it can be analyzed.

The sample's preparation involves cutting, gluing, polishing and thinning to acquire the cross sectional TEM image. A strip of the sample was cut to about 1mm in width and then cut in half length-wise. Then, these two pieces were glued together face-to-face using a special glue.

After that, the samples were polished mechanically using disk grinder with a SiC polishing pad and diamond polishing pad. Lubricant was used during polishing process in order to reduce the fraction and also to remove the particles after polishing away from the sample.

When the thickness of the sample reached about 1 µm, it was thinned by making a hole in the middle to less than 100 nm using ion-milling technique. Figure 20 demonstrates a schematic representation of a standard TEM. Figure 21 shows the FEI Titan HRTEM that was used in this research.

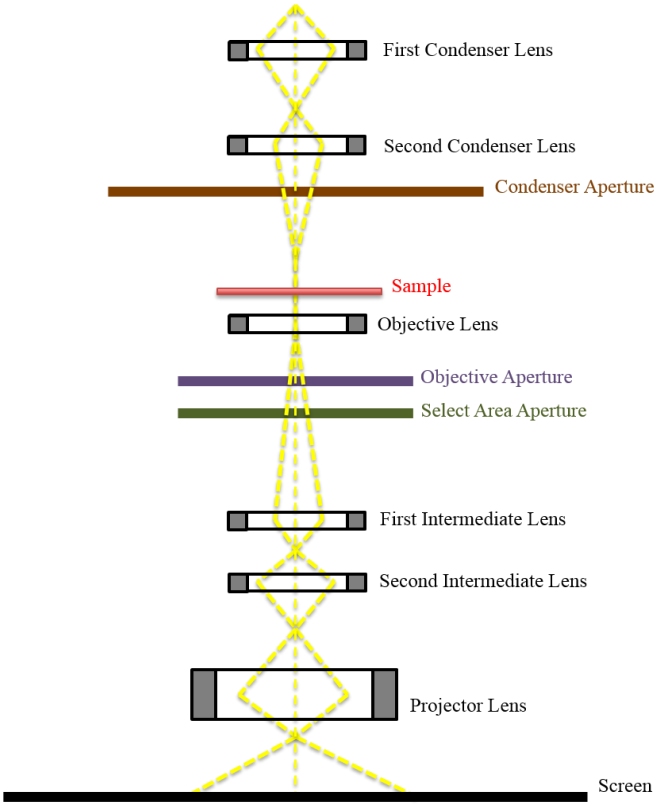

Figure 20. A schematic representation of a standard TEM.

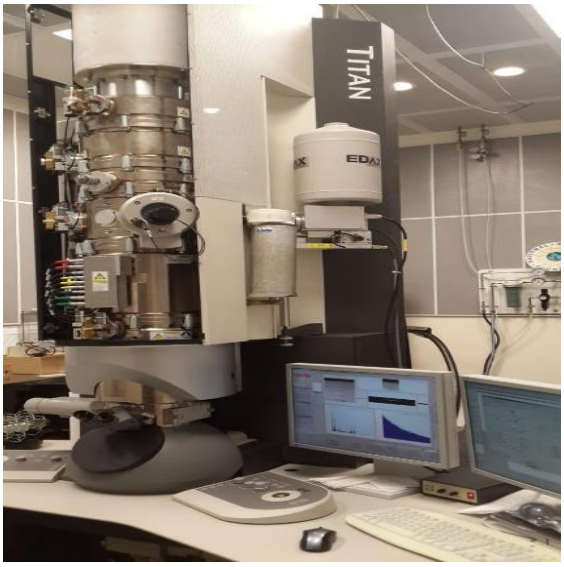

Figure 21. FEI Titan HRTEM that was used in this research (picture taken by the author).

4.4.5 Dektak Profilometer

The depth of the grown layer can be determined by a profilometer which has a needle that scans the surface in a contact mode measurement. The scan parameters can be chosen according to the sample properties. Then, the location of the samples will be shown on a video camera to place the sample properly. Next, the needle is lowered down to scan the surface. The scan results are shown on the screen and can be leveled as well in the software.

Also, the data can be printed with the height shown dependent upon on where you put the cursors in the software. The Dektak measurement error is +/- 500 angstrom (Å). In the case of having a thickness less than 1000 Å, AFM should be used instead of the Dektak. Figure 22 shows the Dektak at HiDEC that was used in this work.

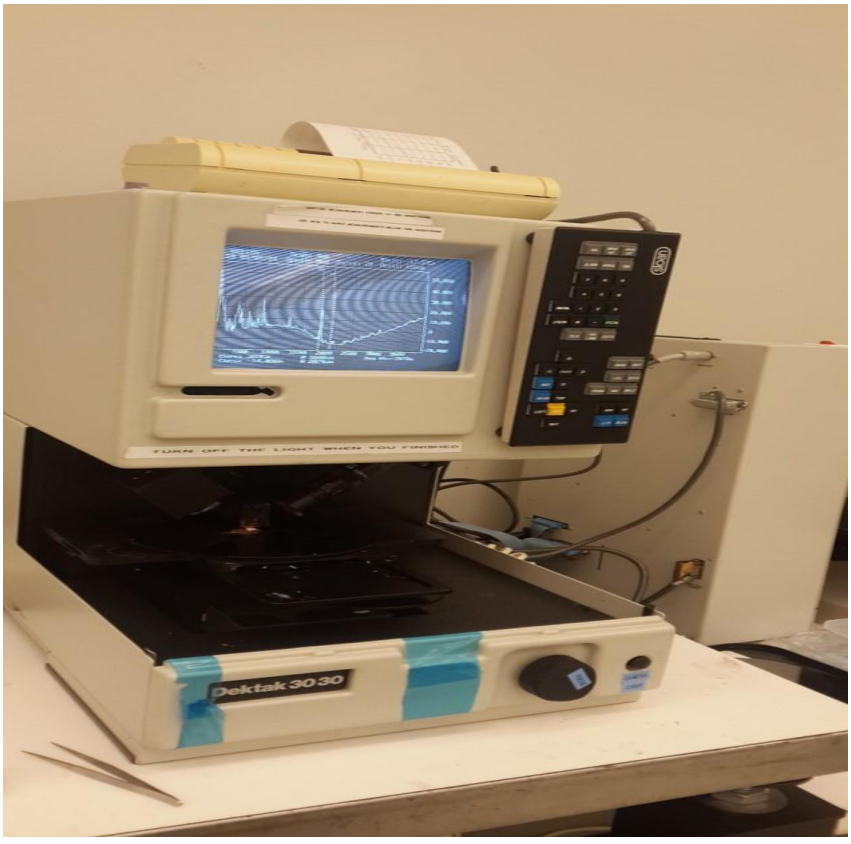

Figure 22. Dektak at HiDEC that was used in this work (picture taken by the author).

Chapter 5: Results and Discussions

This chapter presents the results, analysis and discussion of the experiments conducted during the period of this thesis work. As indicated in Chapter Four, a set of experiments were performed to obtain epitaxial growth of Si on c-Si substrates. Other sets of experiments were performed on glass substrates to achieve epitaxial growth of Si on low cost materials. Additionally, seed layers were prepared by means of AIC on ITO coated glass substrates. The images and plots from these experiments are presented in this chapter. Characterization tools such as SEM, XRD, Raman scattering and TEM were utilized to analyze the samples.

5.1 Epitaxial Growth of Si on c-Si Substrate and Glass

Hot-wire CVD (HWCVD) technique was used to deposit Si on c-Si substrates and on Corning glass substrates. As indicated in Chapter Two, the growth of epitaxial silicon using HWCVD is controlled by four parameters: flow rate of gases, pressure, substrate temperature and filament temperature. As a result, in this work those four factors were varied to determine the optimal growth process.

For most of the samples at the same conditions, the results on both c-Si and Corning glass substrates were similar when comparing their Raman shift and the corresponding FWHM. The experiments were implemented under two distinct conditions. The first one was when the single chamber was utilized at low vacuum (10^{-3} torr) which was a limitation of the machine. Next, a turbo pump was added to help the vacuum to achieve a pressure of 10^{-5} to 10^{-6} torr.

Raman scattering spectroscopy showed that all the samples at low vacuum (10^{-3} torr) were not fully crystalline even at high diluted SiH_4. Those samples had some crystalline phase peaks at 520 cm^{-1} with amorphous peaks at 480 cm^{-1} but with different crystalline quality. At high vacuum (10^{-5} to 10^{-6} torr) there were similarities to the low vacuum results in the crystalline

quality in terms of Raman shift and FWHM at low dilution ratio. Nevertheless, there was a significant change in the crystallinity of the film when the dilution ratio of the introduced gases was very high (up to 200 sccm of H_2 flow rate to 1-6 sccm of SiH_4).

5.1.1 Characterization of Epitaxial Growth of Si on c-Si

5.1.1.1 The Effect of Atomic Hydrogen on Epitaxial Growth

Starting the first set of experiments without the use of the high vacuum chamber affected the results substantially. The Si film deposited on c-Si substrate with pure SiH_4 at low vacuum displayed a broad peak at about 480 cm^{-1}, which is a typical Raman value for the amorphous Si phase. Broader peaks in Raman scattering usually are present when there is inhomogeneous bonding among the atoms.

This implies that the atoms are not in an ordered arrangement. The flow rate of SiH_4 was 5 sccm, the substrate temperature was 400 °C, and the growth time was 30 min. However, at the same conditions adding 5 sccm of H_2 showed a shoulder towards lower wavelength numbers at 480 cm^{-1} with a sharp peak at about 519 cm^{-1}, which is very close to the typical Raman peak of crystalline Si at 520 cm^{-1}. This suggests that the grown film was improved in terms of crystalline quality and was not fully crystallized but contained an amorphous phase. Figure 23 demonstrates Raman intensity against Raman shift.

The FWHM was compared with regard to the FWHM of the c-Si substrate, which was about 10-11 cm^{-1}. The pure SiH_4 sample was found to have a very broad peak so the FWHM was 84 cm^{-1} whereas the diluted SiH_4 sample exhibited a sharper peak that had FWHM of about 11 cm^{-1}. Hydrogen atoms play a major role during the growth as they clean the chamber from any contamination and passivate the surface. Hydrogen is known for its ability to induce desorption of oxygen from the surface and also to avoid water vapor and oxygen adsorption.

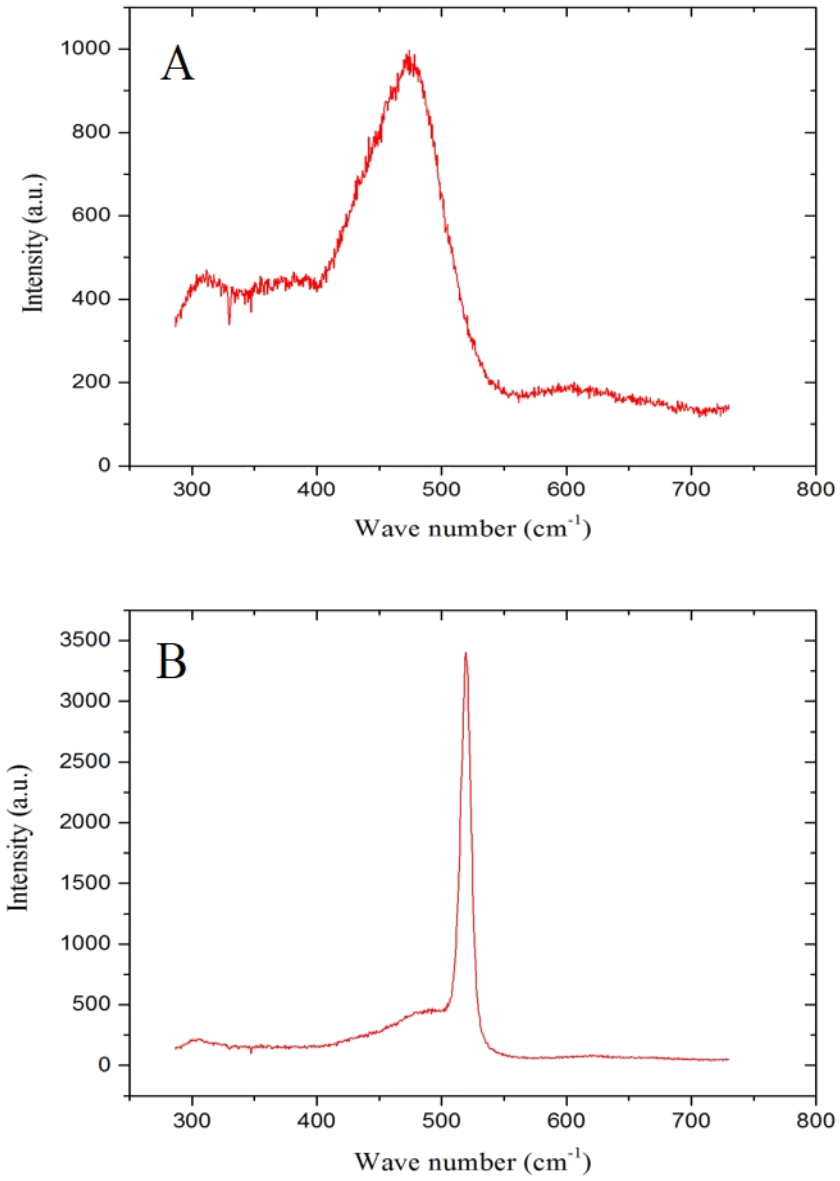

Figure 23. Raman scattering for two samples at the same condition but: A. with pure SiH_4, B. with diluted SiH_4 in H_2.

Furthermore, H_2 enhances crystallinity due to its ability to reduce the activation energy of nucleation, hence, the grain boundaries growth. To evaluate the crystalline volume fraction, Xc,

from Raman spectra, the integrated intensities of crystalline peaks (I_{520}), the defects peaks I_{515}, and the amorphous peaks I_{480} have been calculated as follows [45], [42]:

$$Xc = (I_{520}+I_{515})/(I_{520}+I_{515}+I_{480}) \times 100\% \qquad \text{(Equation 5.1)}$$

This method was developed by Seth Shumate from Silicon Solar Solutions (SSS) [45] and Figure 24 shows those peaks. The dotted peaks is the sum of the four peaks where it should be fitted with the results of this work to calculate the crystalline volume fraction.

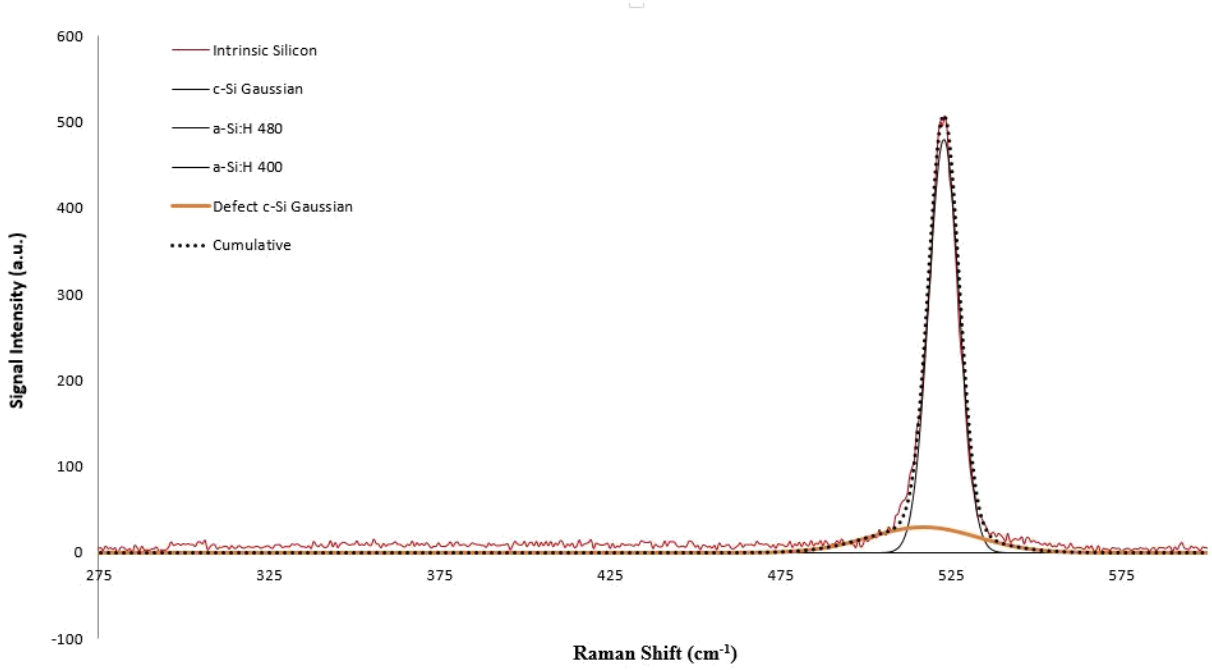

Figure 24. Crystalline fraction template peaks.

The calculated crystalline volume fraction, Xc, for the pure SiH_4 peak was about 1%, whereas diluted SiH_4 gave a crystalline fraction of 60%. Many studies have suggested that hydrogen is important but without fully understanding the reasons. However, it could be as a result of many factors such as passivation of the surface or pushing the Si atoms to find their lower energy state faster than defect growth.

It could also be because of the preferential etching of defects faster than crystalline growth. In general, atomic hydrogen has an undeniably significant role during the epitaxial growth when hydrogen reduces the defect density by reducing Si dangling bonds. This, increases the crystallinity of the film so the electrical properties will be improved.

5.1.1.2 The Effect of Substrate Temperature on Epitaxial Growth

Next, the substrate temperature was varied, but the dilution ratio remained fixed to study the effect of the substrate temperature. Increasing the substrate temperature had a major impact on the deposited film. As the substrate temperature was raised, the peak position of the Raman spectrum became increasingly closer to 520 cm^{-1}, and the intensity of the shoulder at 480 cm^{-1} became less. Figure 25 demonstrates Raman spectrum of several Si films that were deposited by using HWCVD method at temperatures: 300 °C, 400 °C, 500 °C, 600 °C, 700 °C and 750 °C. These experiments were performed at a fixed SiH_4 flow rate of 5 sccm, fixed H_2 flow rate of 10 sccm, a filament temperature of 1900 °C, and a 30 min. deposition time.

The crystalline volume fraction, Xc, increased as the substrate temperature was raised. It went from only about 1% crystalline fraction at 300 and 400 °C to about 85% crystalline fraction at 700 and 750 °C. At 500 °C, the crystalline fraction was almost fully crystallized and the Xc was about 100%. However, at 600 °C, there was unexpected results as Raman peak showed an amorphous phase at 480 cm^{-1} with the crystalline peak at about 520 cm^{-1}. In addition to that, the crystalline volume fraction dropped to only about 20%. This observation could be a result of the cleaning process not being enough to remove all the contamination or silicon dioxide from the surface. It also could be related to oxidation of the surface just before loading the substrate in the chamber.

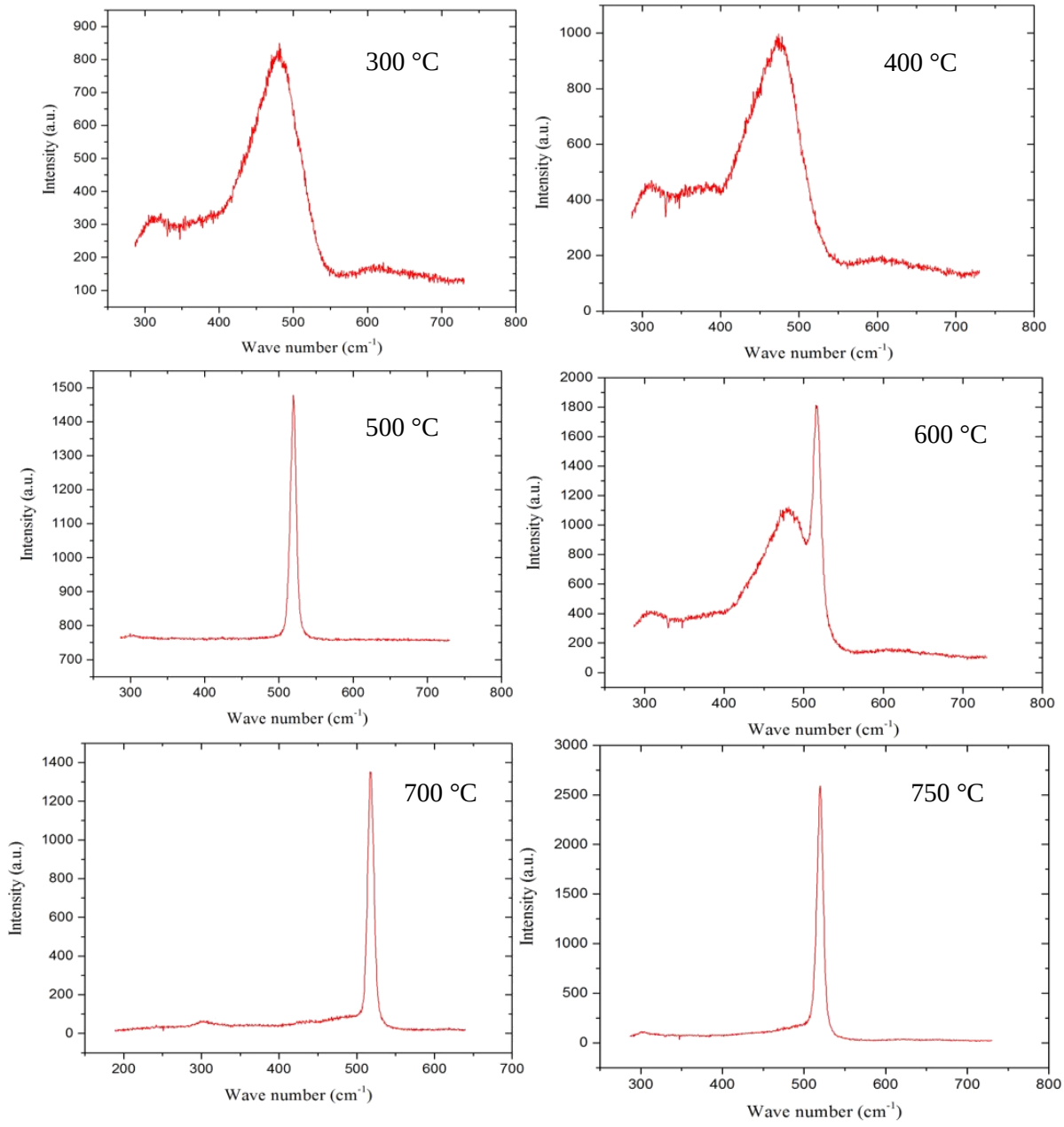

Figure 25. Raman scattering for samples at the same conditions but with different substrate temperatures.

There were encouraging results which suggested the need for further investigations to determine whether or not the film is epitaxially grown. At 500 °C, the Raman spectrum displayed a narrow peak at 519 cm^{-1} and the amorphous broad peak was hardly present.

However, Raman scattering gives only an indication whether or not the film is crystalline, but it cannot ensure whether the crystalline peak is coming from the film. It depends on the thickness of the film and the power of the laser. In this case, TEM was performed to evaluate the crystalline quality of the layer grown and confirm the epitaxial growth.

Figure 26 shows the images taken using TEM analysis. The thickness of the film was about 150 nm which was enough for the Raman beam to scatter from the film. The images show an epitaxial film considering it had the same orientation as the substrate orientation. Interestingly, it was observed that at the interface the atoms arranged themselves epitaxially for a few nanometers followed by kind of an amorphous layer. However, the interface was difficult to evaluate due to the Fresnel fringe effect.

When the electrons experience a difference in the scattering beam to the incident electron beam, fringes occur. The possibility of these fringes occurring increases when the two layers have different atomic numbers or different scattering powers more than if the two materials have less difference. "The visibility of the fringes increases with increasing defocus away from minimum contrast, while optimum resolution in bright-field imaging is obtained at the Scherzer defocus, which is about 100 nm from the minimum contrast for most high resolution microscopes. Fresnel fringes are thus present when imaging at optimum defocus."[46] Contamination on the surface, oxide, or defects could also contribute to this effect because of the use of a non-ultra-high vacuum chamber. Despite the random growth that occurred in the film, the atoms in some areas rearranged themselves similarly to the substrate atoms while some other areas took on another orientation. The amorphous layer was SiO_2 which had to be addressed to avoid the breakdown in the grown film to either poly-crystalline or amorphous phase.

The oxide seems like it was not continuous so the surface was partially oxidized. As a result, the grains that are attached to the surface atoms grew epitaxially while the other grains grew randomly but at some point the growth rate of the epitaxially grown grains was faster.

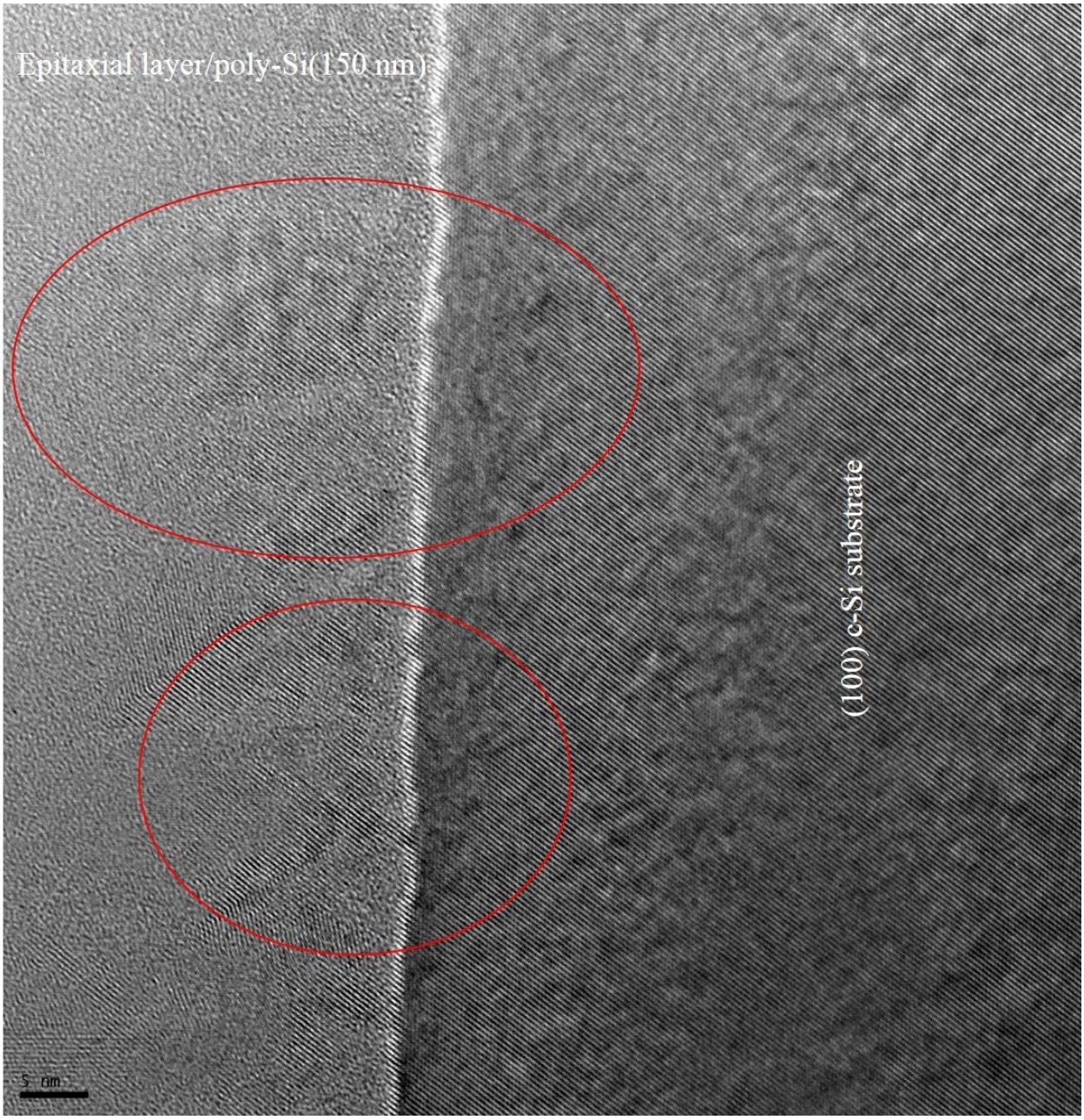

Figure 26. Cross-sectional TEM image of Si film grown on (100) c-Si substrate.

This difference in the growth rate seems to be helpful because the epitaxially grown grains expanded to join the grains that were next to them which created a larger epitaxial layer. Another possible explanation would be that the surface had a very thin layer of oxide so the atoms during the growth could still maintain the surface atoms orientation and get to the proper sites.

X-ray diffraction was also performed and the scan pattern θ-2θ shown in Figure 27 indicates that the film was epitaxially grown on the substrate, as only one peak at (400) was present. This peak corresponds to the orientation (100), and infers that the atoms aligned themselves on the surface of (100) c-Si substrate. The absence of the other poly-crystalline Si peaks in the XRD resulted pattern was evidence that the majority of the grains grew epitaxially.

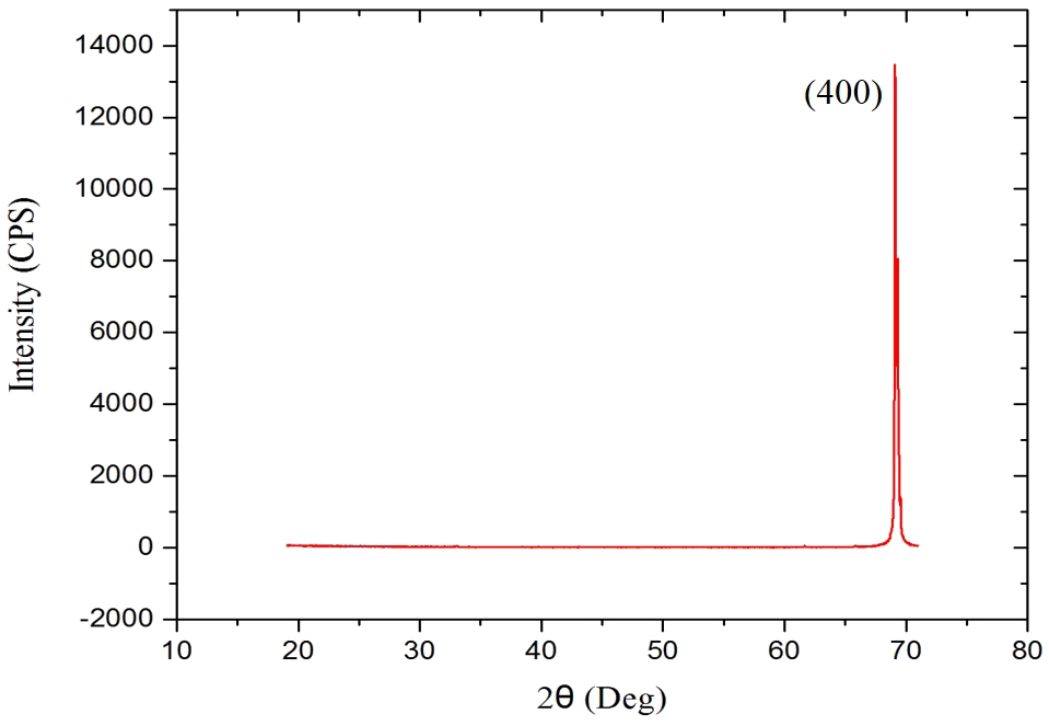

Figure 27. XRD pattern of θ-2θ scan that shows a sharp peak at (400) which corresponds to (100) orientation.

In summary, at low temperature (500 °C) and low vacuum (10^{-3} torr) it was possible to deposit this epitaxial layer. Nevertheless, there were still many issues that needed to be optimized in order to obtain the desired results.

One of the biggest concerns in the epitaxial growth process was contamination on the surface of the substrate. The interface contamination increases the dislocation density in the deposited film. Epitaxial growth is very sensitive so the substrate needs special preparation before the growth. The contamination can be native oxide, water vapor, or organic contamination such as fingerprints. The samples, therefore, were dipped in a sulfuric acid to remove any organic contamination and then immersed in hydrofluoric dip (HF) to remove SiO_2 from the surface. Transmission electron microscopy results in Figure 26 indicated that there was a layer of SiO_2, which was a barrier for the atoms to find their proper sites to match the atoms underneath which resulted in a breakdown into a polycrystalline film or amorphous film. Different orientations were present in the deposited layer, as highlighted in TEM images.

The reason is thought to be that despite the special cleaning process, the surface can still be oxidized in the low vacuum chamber. In order to solve this issue, hydrogenation was performed prior to the deposition process for 15 min. Hydrogen at 200 sccm was introduced in the chamber to clean the chamber and prevent oxidation during the deposition. Figure 28 shows four samples at the same condition before and after hydrogenation.

Unlike the results from un-hydrogenated deposition, H_2 atoms helped the Si atoms to grow with higher crystalline quality. The peaks for the samples that were not hydrogenated were broader so at 400 and 700 °C the FWHM was about 85 cm^{-1} and 21 cm^{-1} respectively. Then, the samples that were at the same condition but were hydrogenated displayed sharper peaks so the FWHM was 11 cm^{-1} at 400 °C and 10 cm^{-1} at 700 °C.

In addition, the amorphous content decreased after the hydrogenation process according to the crystalline volume fraction values. At 400 °C, the crystalline volume fraction went up from about 15% to 60% when the growth was hydrogenated first. On the other hand, even though at 700 °C, before applying hydrogenation process, the crystalline fraction increased to 60% due to the high temperature, the crystallinity increased even more up to 80% with use of a hydrogenation process prior to deposition.

The high substrate temperatures led to low defect density because of the high growth rate similar to the effect of atomic hydrogen at low temperature. At low substrate temperatures, the growth required assistance, in this case the atomic hydrogen, in order to passivate the dangling bonds and increase the deposition rate.

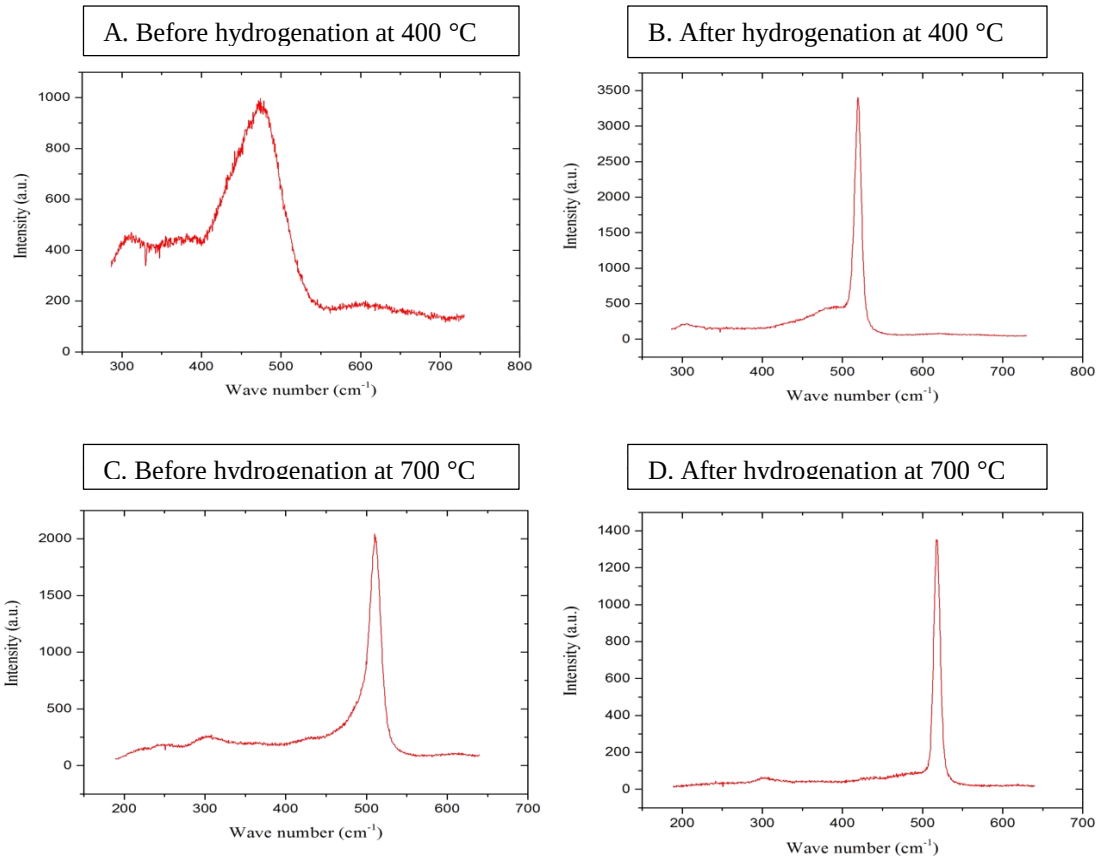

Figure 28. Raman scattering for samples at 400 and 700 °C in (A) and (C) before hydrogenation and in (B) and (D) after hydrogenation.

5.1.1.3 The Effect of Increasing the Dilution Ratio on Epitaxial Growth

Due to the encouraging results of both pre-deposition hydrogenation and dilution of SiH_4 in H_2, adding hydrogen was investigated in the next set of experiments. Additionally increasing the flow rate of H_2 (up to 200 sccm) over the flow rate of SiH_4 (which was only 1 to 6 sccm) resulted in a significant change in the crystalline quality at high vacuum (10^{-5} torr). Possibly it was the ability of hydrogen atoms to preferentially etch the defects and amorphous Si atoms faster than those Si atoms which are in epitaxial growth. In other words, hydrogen decomposes the weak Si-Si bonds and creates free sites for crystalline Si to form. Raman characterization was conducted to study the crystalline quality of the samples.

Raman scattering in Figure 29 confirmed the significance of hydrogen atoms prior to and during growth. The crystallinity had been improved up to about 90% but it was decreasing to about 60 to 70% as the flow rate of SiH_4 was increased. Figure 29 shows that using less SiH_4 (1 to 2 sccm) resulted in greater crystallinity compared to introducing 4 to 6 sccm of SiH_4. The FWHM and the corresponding Raman shift for them are demonstrated in Figure 30. Graph A demonstrates that as the dilution ratio increased the FWHM increased correspondingly which means the peak was not as sharp as a typical c-Si peak.

The relationship between Raman shift and the SiH_4 flow rate is plotted in graph B. of Figure 30. It was found that as the flow rate of SiH_4 was increased, the Raman shift decreased from a typical Raman shift of c-Si substrate which indicates that there is a possibility of stress in the grown film that could be either a tensile stress or compressive stress. In general, compressive stress results produce higher wave numbers of Raman shift, while a tensile stress results in lower wave numbers of Raman shift.

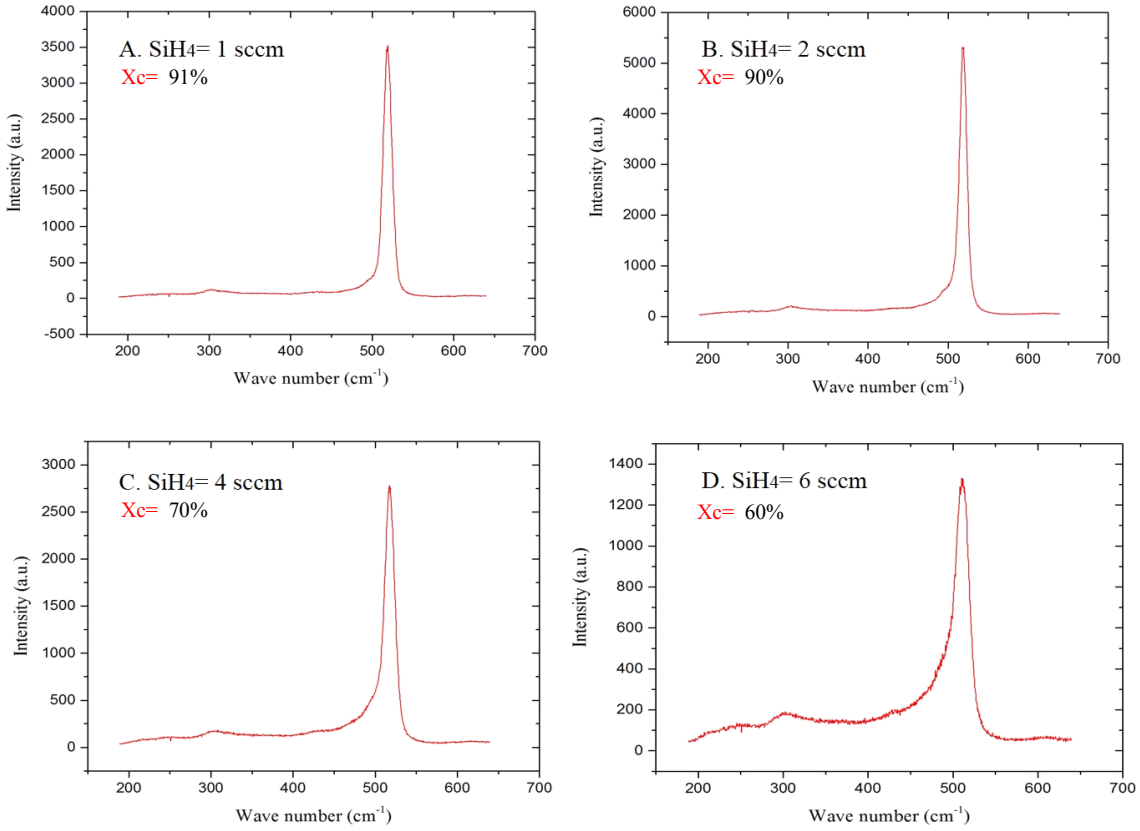

Figure 29. Raman scattering for samples at substrate temperature of 600 °C and H_2 flow rate of 200 sccm but with different SiH_4 flow rates: A. 1 sccm, B. 2 sccm, C. 4 sccm, and D. 6 sccm.

A possible explanation for the relationships in graph A and B is that when there were fewer Si atoms, in the case of high dilution ratio, the time was sufficient for them to arrange themselves in the proper sites. In this case, hydrogen atoms aided the Si atoms in ushering them to their proper sites.

The growth rate of Si atoms has to be slower so that the Si atoms can find their lowest energy states. On the other hand, at low dilution ratio the Si atoms oriented themselves more quickly to their sites which prevented them from arranging themselves properly.

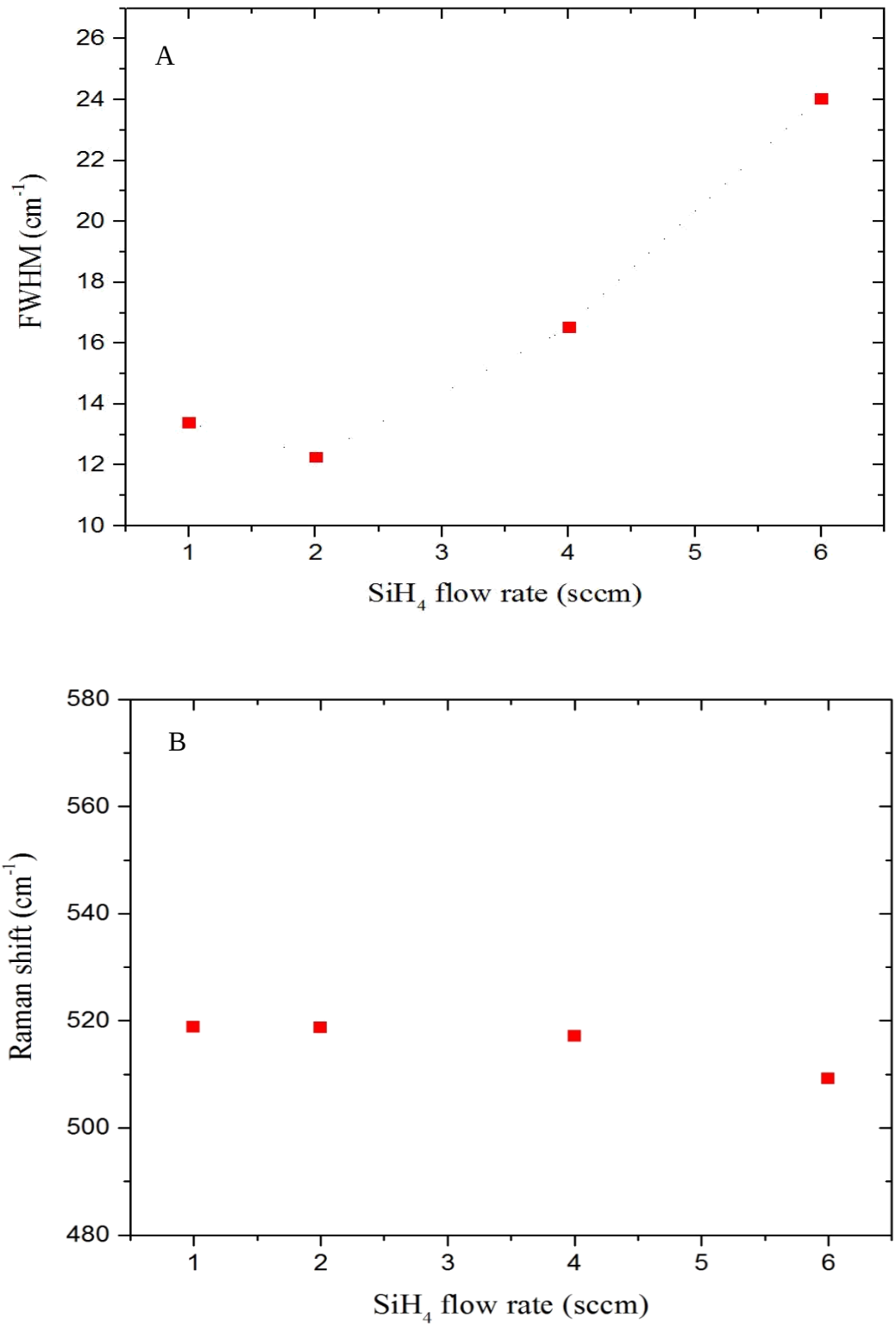

Figure 30. A. The relationship between SiH_4 flow rate and FWHM, and B. The relationship between SiH_4 flow rate and Raman shift.

X-ray diffraction (XRD) analyses are shown in Figure 31, Figure 32 and Figure 33. In XRD analysis, θ-2θ scan was done and a grazing around the orientation (004) at an incident angle of 3 degrees was performed. A typical 2θ value for (100) is 69.142° which corresponds to (004) reflection and this peak represents the c-Si substrate. The (111) orientation is located at 28.447° in the XRD pattern.

The X-ray diffraction pattern demonstrates several strong Si peaks that are typical results for a poly-crystalline thin layer as shown in Figure 31. The deposition of this sample was done at 600°C and a dilution ratio of 2:200 sccm. This result was a confirmation that the film is a poly-crystalline Si as different Si peaks were present in the XRD pattern.

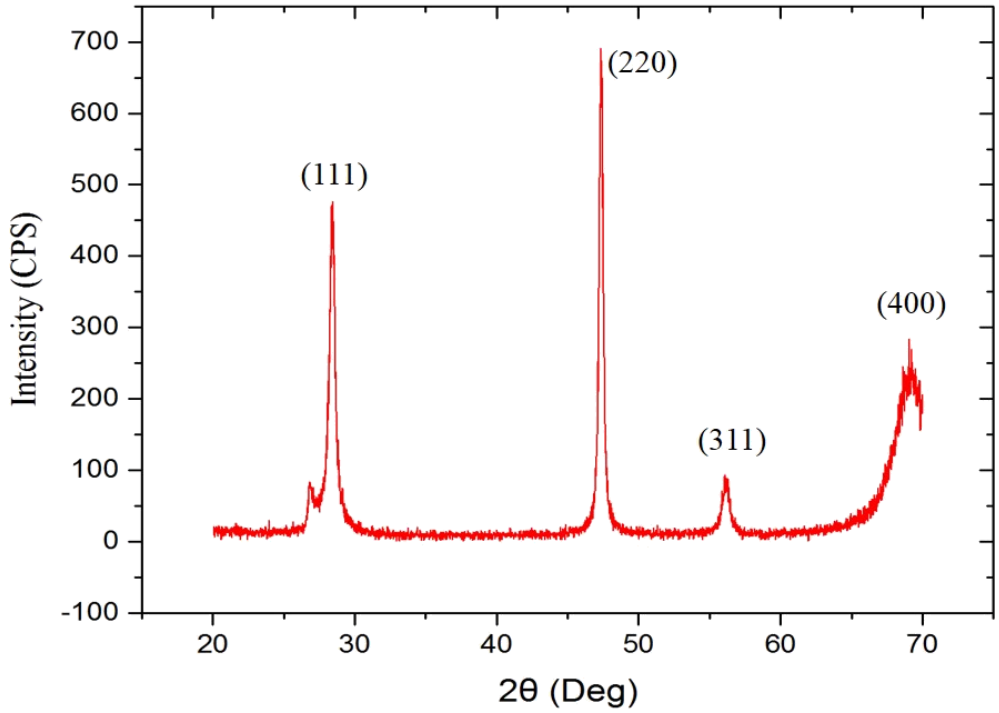

Figure31. X-ray diffraction of a poly-Si layer.

The standard X-ray diffraction powder patterns of poly-Si are shown in Table 8 below[47]. They show the percentage of each orientation in a relation to (111) orientation.

Table 8. The standard X-ray powder diffraction patterns of poly-Si [47].

No.	h k l	2 Theta (Deg)	I (%)
1	1 1 1	28.443	100
2	2 2 0	47.304	55
3	3 1 1	56.122	30
4	4 0 0	69.132	6

Getting the same percentages of peak intensities as this standard XRD pattern of poly-Si means that the grains in the grown film are randomly oriented. Thus, by comparing the Si peaks intensities with this standard pattern, the sample that is shown in Figure 33 shows that the crystalline grains distributed along a preferred orientation of (220).

The percentage of the intensity at 47. 325° to the intensity at 28.443° was 143.64% while 56.19° was 16.95%. Therefore, the orientation at 47.325° which is (220) was a preferred orientation.

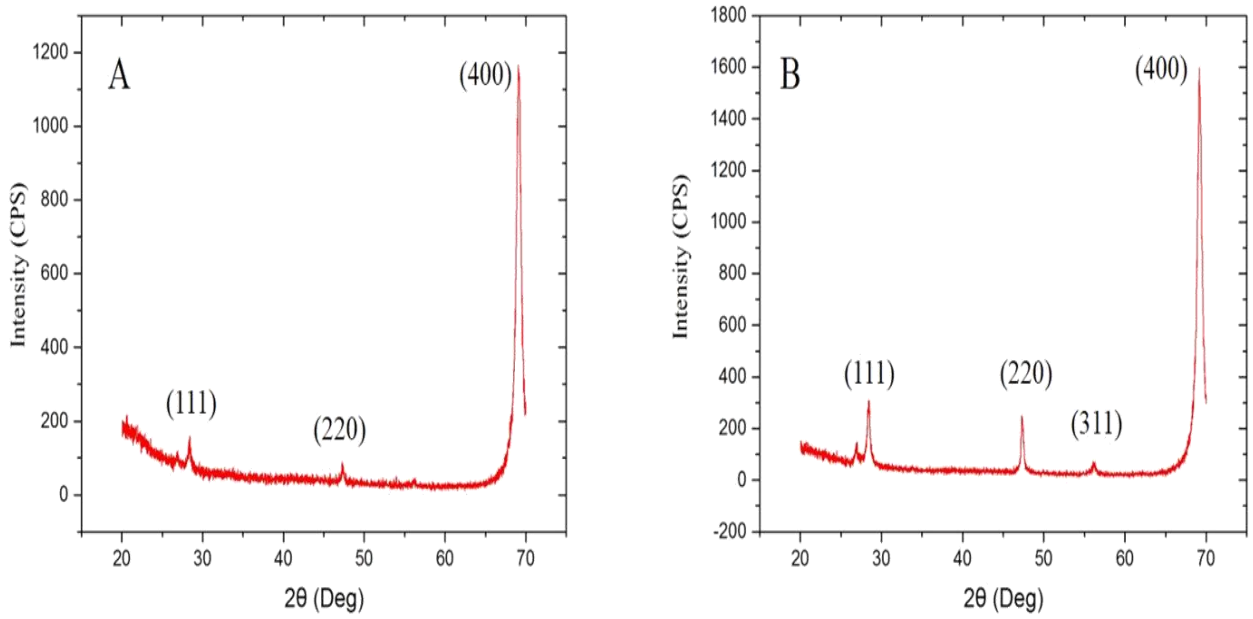

Figure 32. XRD pattern for two samples at the same growth conditions but with different SiH_4 flow rates: A. 1 sccm: 200 sccm, and B. 2 sccm: 200 sccm.

Even though the other samples showed a strong peak of (100) orientation and several weak peaks such as (111) orientation, this observation does not imply that the film had a preferred orientation around (100). Figure 32 shows the XRD pattern of poly-crystalline Si that was deposited at the same conditions but with different SiH_4 flow rates.

It must be said that these results are not enough to confirm that the film was epitaxially grown on the (100) orientation c-Si substrate. It could be a diffracted peak from the substrate itself. Therefore, further investigations were done using XRD measurement.

Grazing around (400) that corresponds to (100) orientation was performed for the same samples to prove whether the peak is coming from the film or not. Figure 33 demonstrates the grazing results around (400) and (111) at an incident angle of 3 degrees.

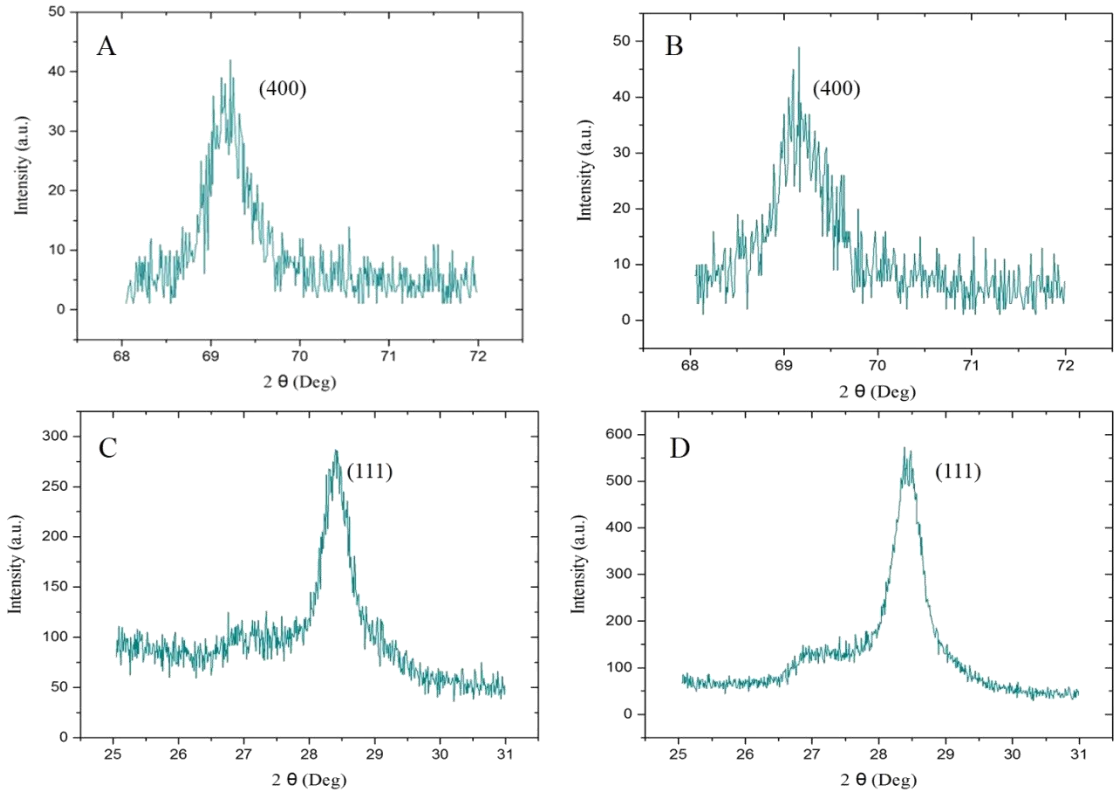

Figure 33. Grazing angle around (400) and (111) for: the sample in A and C was at 1 sccm SiH_4 flow rate and the sample in B and D was at 2 sccm SiH_4 flow rate.

When comparing the intensity of (111) in XRD grazing measurement for the two samples, it was found that there was a preferred direction for the deposited film along (111) in the samples compared to the other diffracted peaks intestines. However, the peak around (220) was a preferred direction over (111) orientation at 2 sccm of SiH_4 flow rate. At 1 sccm flow rate of SiH_4, it was a random oriented film.

Due to the absence of the sharp peak at 69.142°, it can be assumed that the film in both samples was not epitaxially grown. The reason for the unsuccessful epitaxial growth is not fully understood, but it is thought to be related to the pre deposition cleaning or the conditions during the process. It could also be related to the quality of the substrate before the growth. Growth rate, growth chemistry, high vacuum and deposition rate play a large role in the epitaxial growth process.

Unfortunately, the high vacuum that was used in this work might not be strong enough to provide a clean chamber during the deposition so oxidation could occur. The high growth rate of silicon could also be another factor that detrimentally affected the epitaxial growth.

Epitaxial growth requires a slow deposition rate to allow the atoms to align themselves on the substrate atoms. Otherwise, more Si atoms will accumulate on the surface while other atoms are not in their lowest energy state. This leads the atoms to grow randomly in different directions. In summary, a very low deposition rate could lead to higher costs, and a very high deposition rate could lead to breakdown of the crystalline phase into poly-Si or amorphous phase. Thus, the growth rate is very critical in the process of epitaxial growth of Si and must be taken into consideration. Also, prior to the deposition, even with the HF treatment, the c-Si substrate could develop oxide on the surface just before loading them in the chamber. All of

these difficulties that were encountered during epitaxial growth of Si at a low temperature affected the final results and led to a thin a-Si layer or a poly-Si thin layer.

5.1.2 Characterization of Si Growth on Glass

Similar results were achieved at the same growth conditions on c-Si and Corning glass substrates. This result was very important because the glass is amorphous material which is typically more difficult to grow a crystalline phase. However, as crystalline phase was accomplished on c-Si substrate, it was also reached on glass substrates. Figure 34 shows a comparison between the Raman peaks of the film grown on Corning glass and on c-Si substrates.

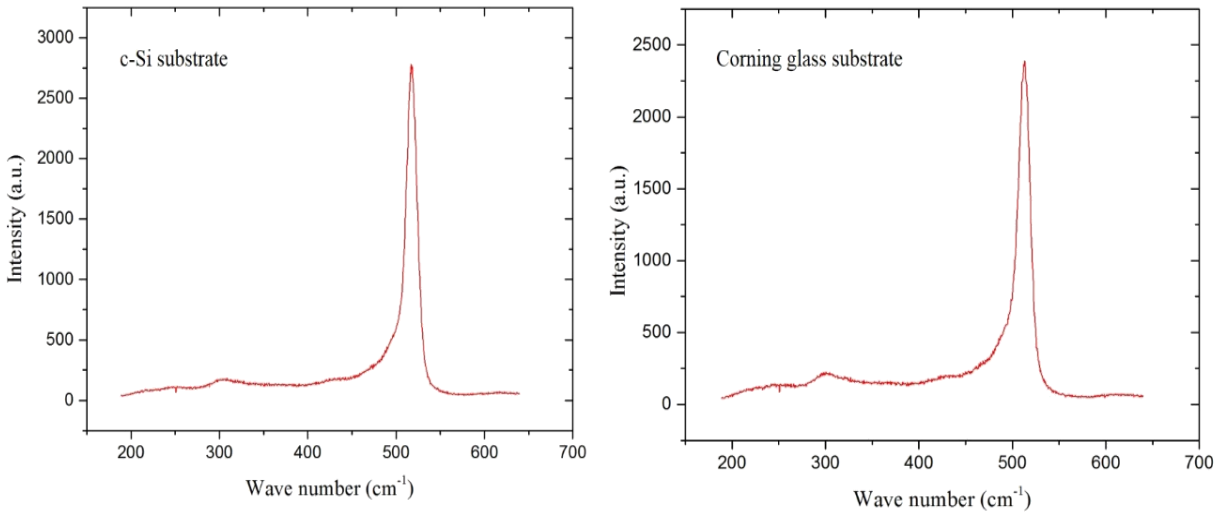

Figure34. Raman scattering for two samples at the same growth conditions.

At a substrate temperature of 600 °C, SiH_4 flow rate of 4 sccm, H_2 flow rate of 200 sccm, and filament temperature at 2200 °C, the FWHM for the film grown on c-Si substrate and on Corning glass was about 15 and 18 cm^{-1} respectively. Raman shift for both samples was 517 cm^{-1}. Even though the growth was at different epitaxial growth types which are homo-epitaxy (c-

Si substrates) and hetero-epitaxy (ITO coated glass substrates), the results for both cases were similar in terms of FWHM and Raman shift.

Crystallinity fraction Xc was about 60% in the glass sample and about 80% in the c-Si sample. This crystallinity fraction does not mean epitaxial growth. It could be poly crystalline with small grains. Figure 35 shows SEM results of the growth of epitaxial Si directly on c-Si substrate and on glass substrate.

The results of SEM shows that both samples had small grains and rough surface. This showed that directly depositing on glass and c-Si substrate resulted in small grains which require further surface treatments. Thus, aluminum induced crystallization method (AIC) was the next step used to get larger grains.

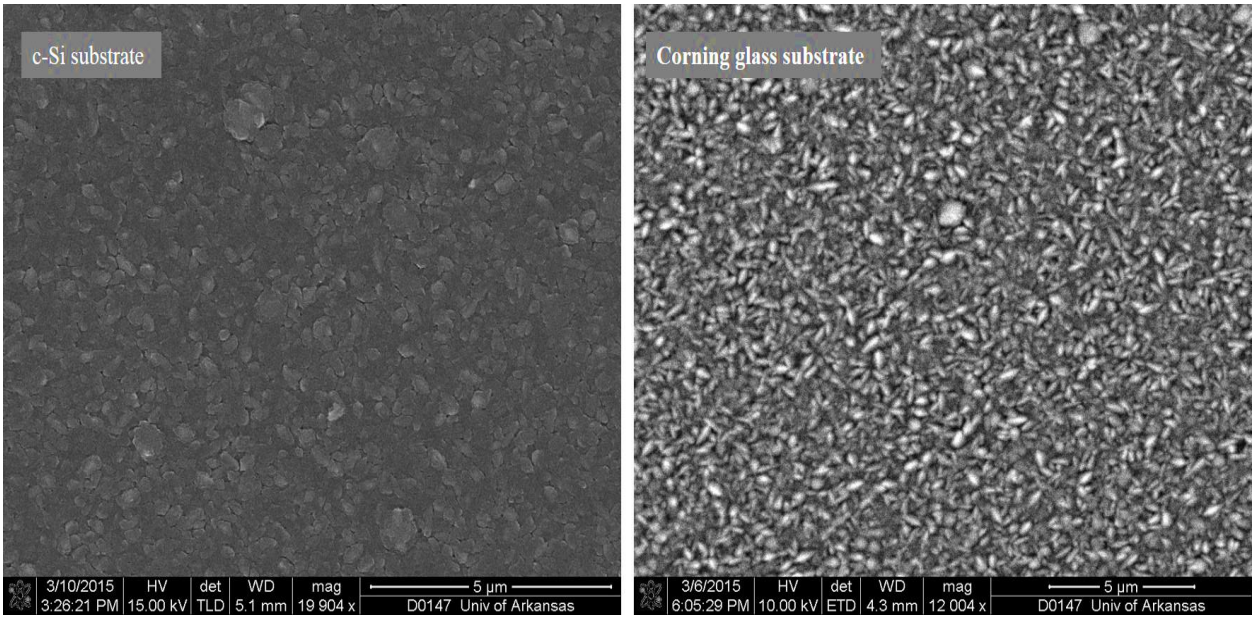

Figure 35. SEM images for two samples at the same growth conditions but on different substrates.

5.2 Epitaxial Growth of Si on Seed Layers

The main focus of this work was to achieve epitaxial growth on glass substrates, but this kind of substrate requires special treatment to make the epitaxial growth possible. Chapter Two reported that a continuous polycrystalline Si film at low temperatures could be achieved on inexpensive substrates, such as glass, when applying the AIC process. Thus, ITO coated glass was utilized to have the advantage of the high conductivity of the ITO film which could be a back contact in the fabrication of solar cell.

Many questions may be raised about this film, such as Al content, structure of the grain boundaries, and the electrical properties. This section includes a detailed characterization of the polycrystalline Si film to answer these questions. The Al content in the polycrystalline Si layer was examined after applying the AIC process. Scanning electron microscopy images were taken for this poly-silicon film before and after Al etching. Energy-dispersive X-ray spectroscopy (EDX), was used to quantify the content of the Al. To examine the structure of the film, TEM was used to study the samples after the epitaxial growth.

5.2.1 Preparation of Heavily Doped p-type Large Grained Poly-Si Seed Layers

The objective of the first experiments was to identify the optimal conditions that would allow a complete layer inversion to occur. The seed layer configuration was bare glass/a-Si:H/SiO_2/Al, which is called top-down aluminum induced crystallization (TAIC) as shown in Figure 36. Hydrogenated a-Si of 300 nm thick was grown by PECVD and then the samples were exposed to ambient air for 10 min. to develop native oxide. Plasma enhanced chemical vapor deposition was then used to deposit oxide for one second. Then, a thermal evaporator was utilized to grow an Al layer of 140 nm thickness.

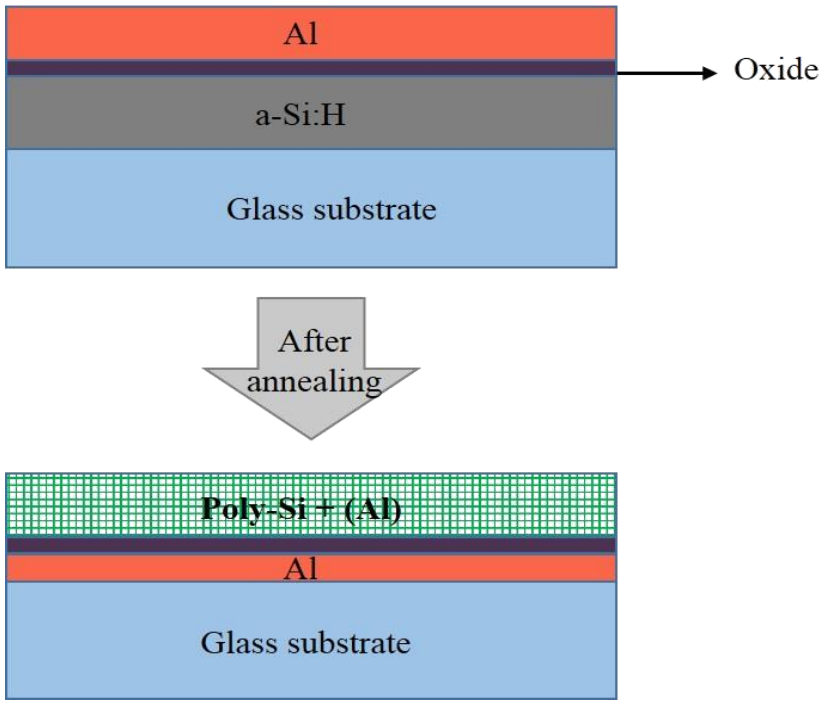

Figure 36. A schematic diagram for TAIC process before and after annealing.

The next step used the IR belt furnace with three temperature zones. The first zone was set to 200 °C, the second zone was set to 500 °C, and the third zone was set to 500 °C as well. The time of annealing was varied to examine the effect of annealing time on the layer exchange process. Then, Al was etched in Al etchant type D for 30 seconds. Figure 37 shows SEM images for three samples that had the same growth conditions but at different annealing times (10 min., 30 min., and 60 min.).

Even though the SEM images did not show significant change, the 60 min. time frame started to show larger grain boundaries. Unfortunately, these results were not desirable for epitaxial growth since the grains were not large enough and the poly-Si layer was not continuous. There were gaps in between the grain boundaries which implies that the crystallization process was not complete due to either the annealing time or the annealing temperature not being sufficient.

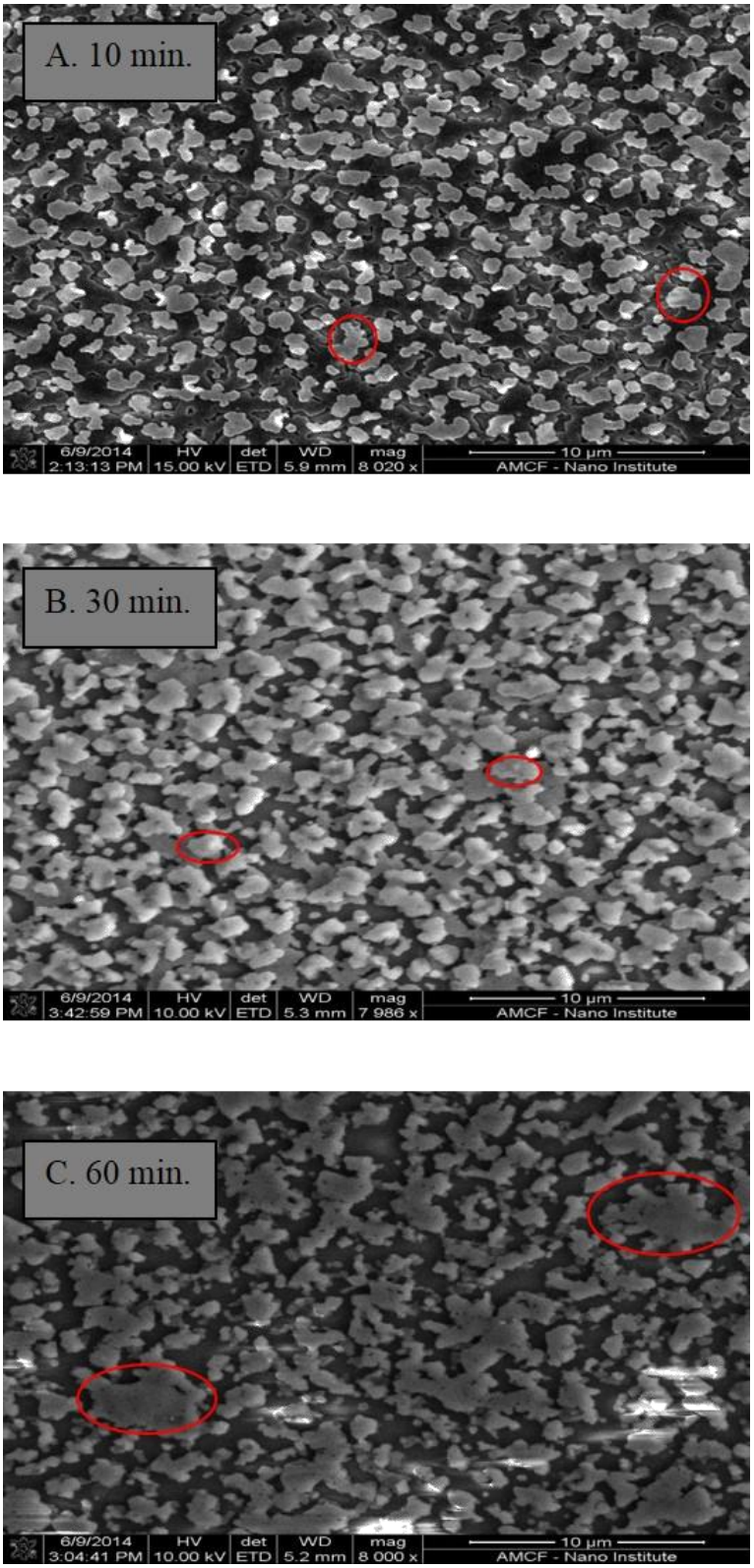

Figure 37. SEM images for three samples that had the same growth conditions but at different annealing time: a.10 min, b. 30min, c. 60 min.

The grain boundaries and defects negatively affect the electrical properties of the device and increase the electron-hole recombination. Additionally, the oxide thickness could have contributed to small grains and the discontinuous poly-Si layer. The EDX results in Figure 38 show that there was still Al content even though it was etched. The samples needed to have been immersed in the Al etchant type D longer.

The other materials that were present in the EDX mapping with Si and Al peaks were due to the ITO coated glass substrate. Although the EDX analysis is known for studying the materials on the surface, the electrons can penetrate deeper than the surface depending on the atomic number Z of the sample and on the energy of the incident electron beam as was explained in Chapter Four. As a result, the material from the substrates are shown in the EDX mapping due to the X-ray that emits from the substrate.

To optimize the results, the opposite configuration was applied as shown in Figure 39, ITO glass/Al/AlO_2/a-Si:H, and is called aluminum induced crystallization (AIC). Electron beam evaporator was used to deposit 300 nm thick layer of Al on (100) oriented c-Si substrate. Then, the samples were exposed for different periods of time to the ambient air to develop Al-oxide to study the effect of oxide thickness. Figure 40 shows optical images for the AIC seed layer on ITO coated glass substrates after Al etching that was exposed to ambient air for different periods of time.

The optical images show improvement in the crystallization growth after three days of exposure to ambient air. As the Al-oxide thickness increased, the grain growth increased as well and it became a more continuous layer of poly-crystalline Si.

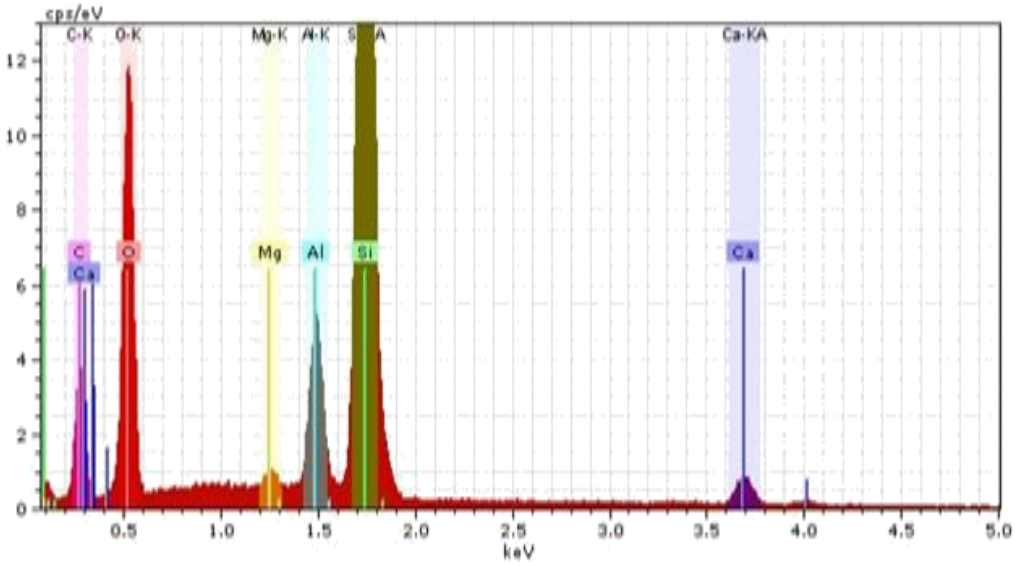

Figure 38. EDX mapping spectrum for a sample that was crystallized using AIC method at annealing time of 10 min.

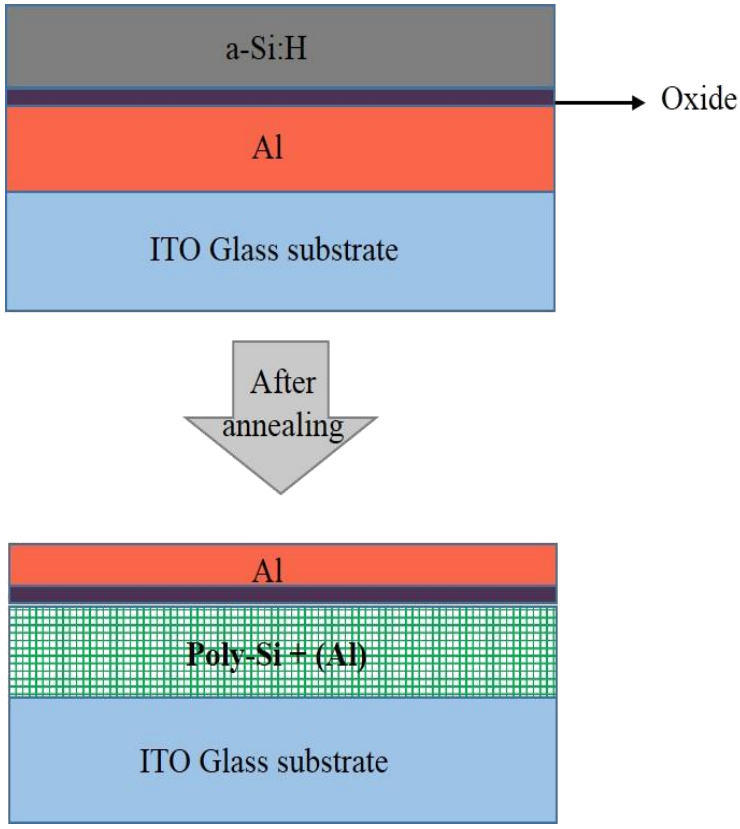

Figure 39. A schematic diagram for AIC process before and after annealing.

In Figure 40 and Figure 41, c-Si and ITO coated glass samples are shown after the AIC process and at different oxide thicknesses.

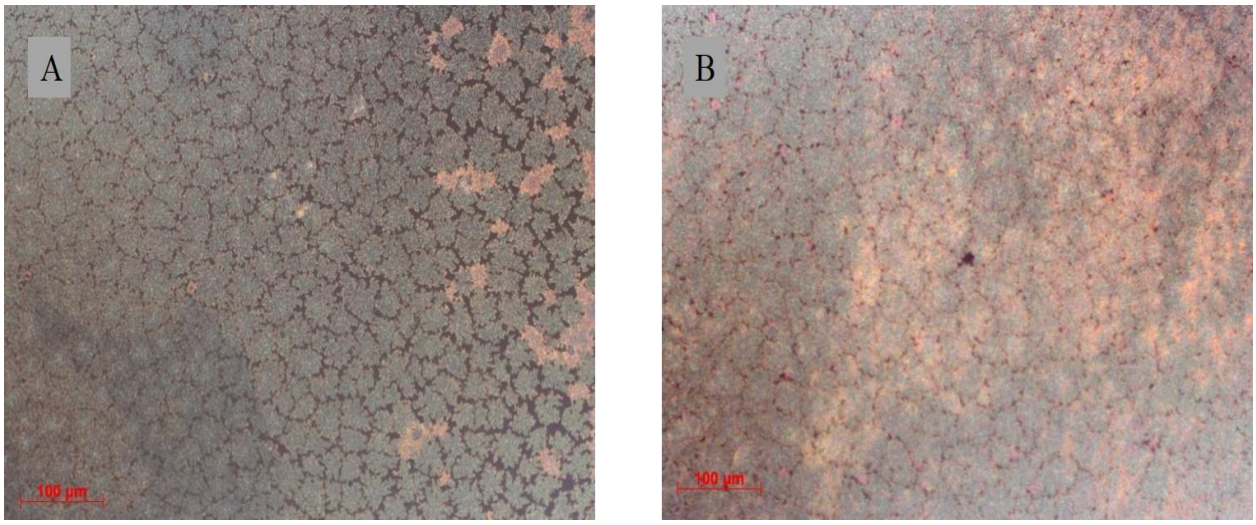

Figure 40. Optical micrographs for AIC seed layer on ITO coated glass samples that were exposed to ambient air for A. one day, and B. three days.

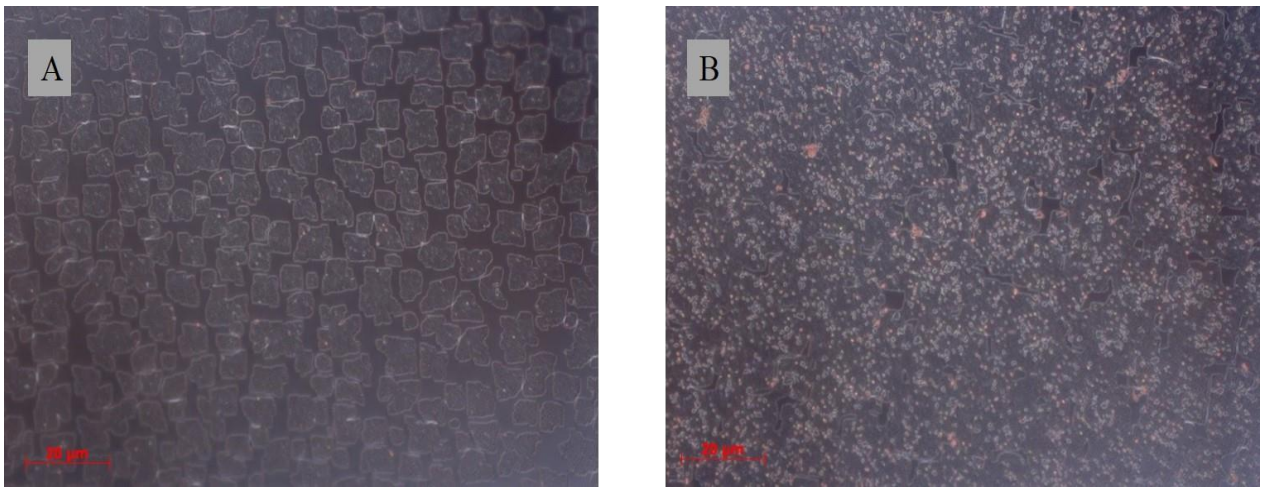

Figure 41. Optical micrographs for AIC seed layer on Si substrates after AIC that were exposed to ambient air for: A. one day, and B. three days.

Crystalline silicon substrates demonstrated similar results to the ITO glass samples. Three days of oxidation allowed the crystallization process to achieve a more continuous layer. Larger

grains were grown on the c-Si substrate compared to the grains at the one-day oxidation because the oxide layer acted as a membrane that controlled the diffusion of a-Si and Al atoms.

Scanning electron microscopy images were taken to study the grain boundaries in more detail. Figure 42 and Figure 43 show SEM characterization for AIC seed layer on ITO glass and c-Si substrates that were exposed to air for one and three days to develop Al-oxide before a-Si deposition. As the exposure time of the oxide increased, the grain sizes increased in both ITO and silicon substrates.

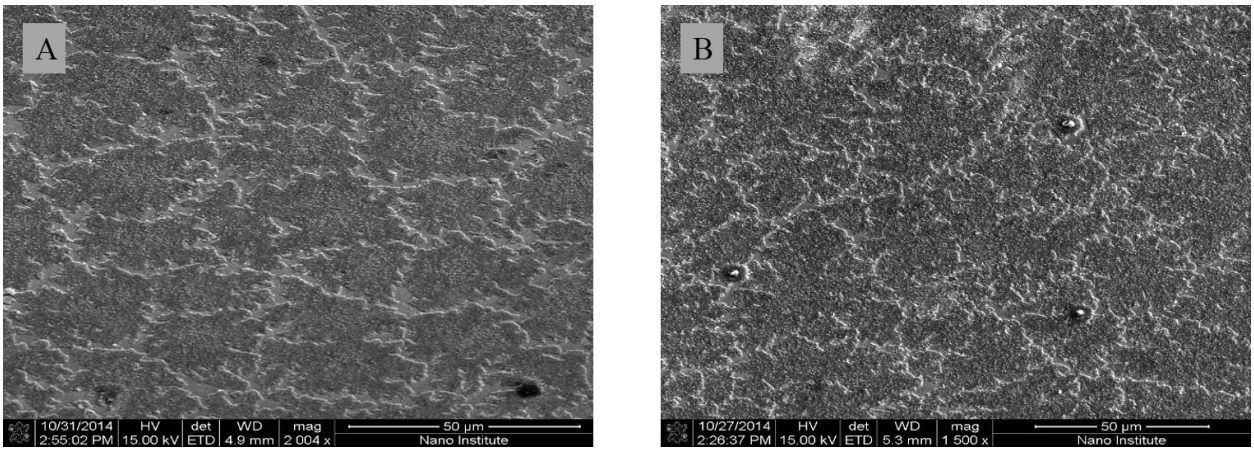

Figure 42. SEM images for glass samples after AIC at different oxide thickness: A. one day oxidation, and B. three days oxidation.

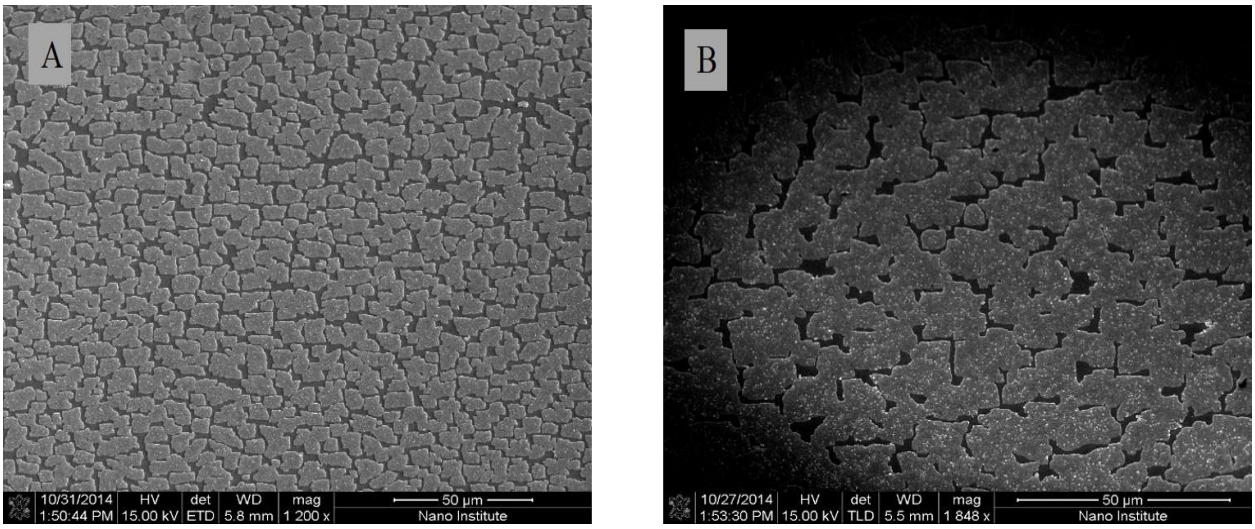

Figure 43. SEM images for c-Si samples after AIC process at different oxide thickness: A. one day oxidation, and B. three days oxidation.

From SEM images in Figure 44, it is observed that there are three regions or layers on top of each other. The substrate is the first region followed by the primary crystallized layer where the layer exchange happened. In this case, the defect energy was the driving force for the atoms to recrystallize.

The chemical potential of the a-Si phase and the defects is higher than the crystalline phase. This drives the atoms to lower their potential energy to be in their lowest state, which is the crystalline phase.

In general, atoms like to go into a more ordered arrangement to acquire a lower energy state. The three layers that appeared in SEM images can be explained as following: Al induced the dissociation of Si, Si diffused to the Al, and Al diffused to a-Si:H. Silicon atoms nucleated at the Al layer, and the Si grains started to grow which happens in any thin film deposition process.

Atoms nucleate first on the substrate, and then they start to grow and expand. Thus, at first a continuous crystallized layer grew in the primary crystallization phase. However, during the growth some of the primary crystallized grains had excess Al that initiated a secondary growth. Those Al atoms dissociated more Si atoms and induced the formation of Si islands on top of the primary grown layer grain. Consequently, the surface was rough due to many Si islands that formed on top of the crystallized layer.

It was observed that the grain boundaries were only at the edges of the samples while the center was almost continuous. There were some holes but the distance between two holes was about 100-150 μm as shown in Figure 45. This indicates that a single crystal was obtained in the center of the samples and TEM investigation confirmed that as shown later in Figure 51.

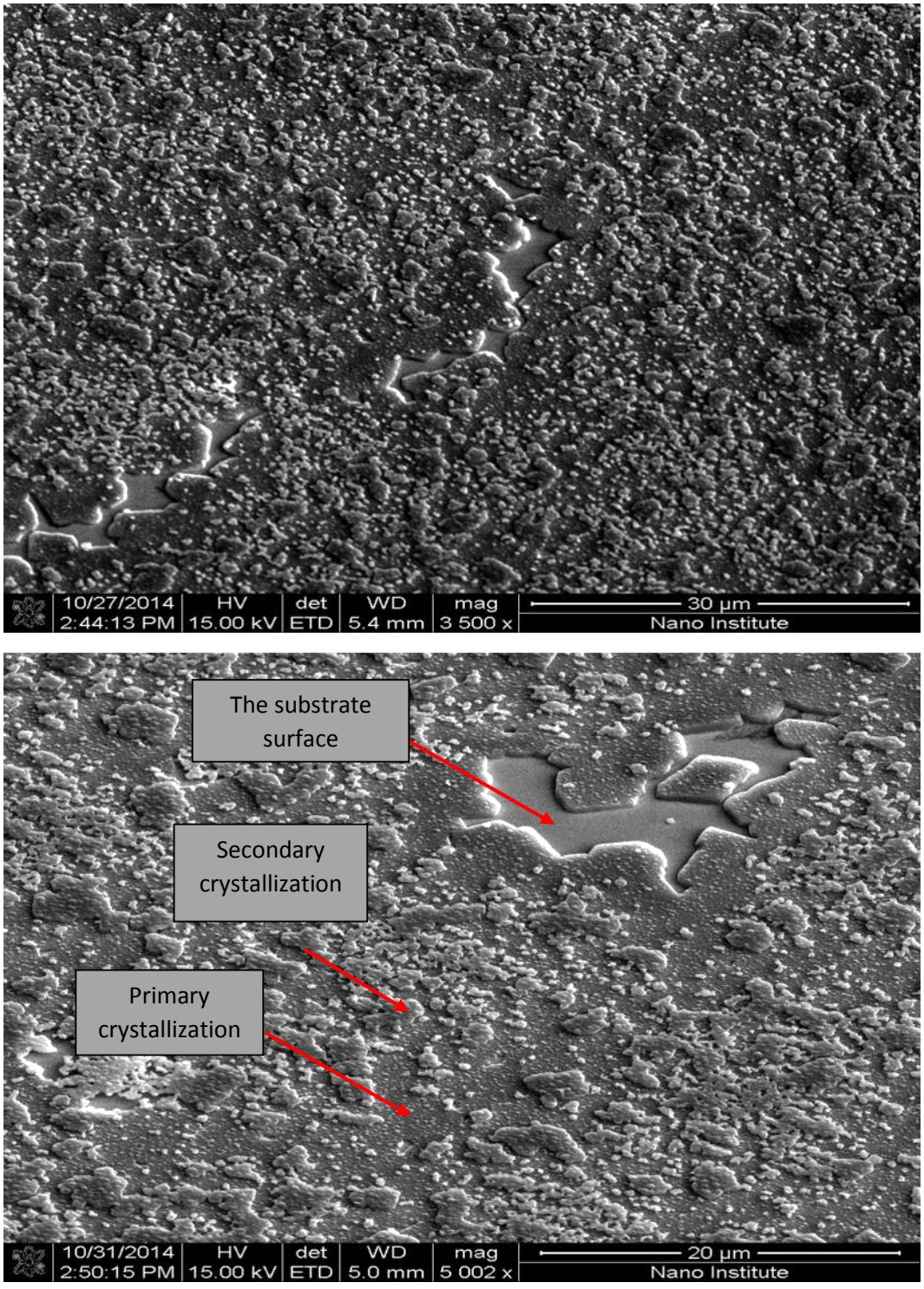

Figure 44. SEM images for a sample that were crystallized using AIC method at different magnifications.

The reason for the growth differences is related to the thickness of the a-Si that was deposited in PECVD. At the edges, the thickness of the a-Si was less than the thickness at the center of the sample. The size of the electrode and the frequency of the RF controlled the voltage distribution on the electrode. A non-uniform voltage distribution led to a non-uniform density of plasma and hence a non-uniform deposition.

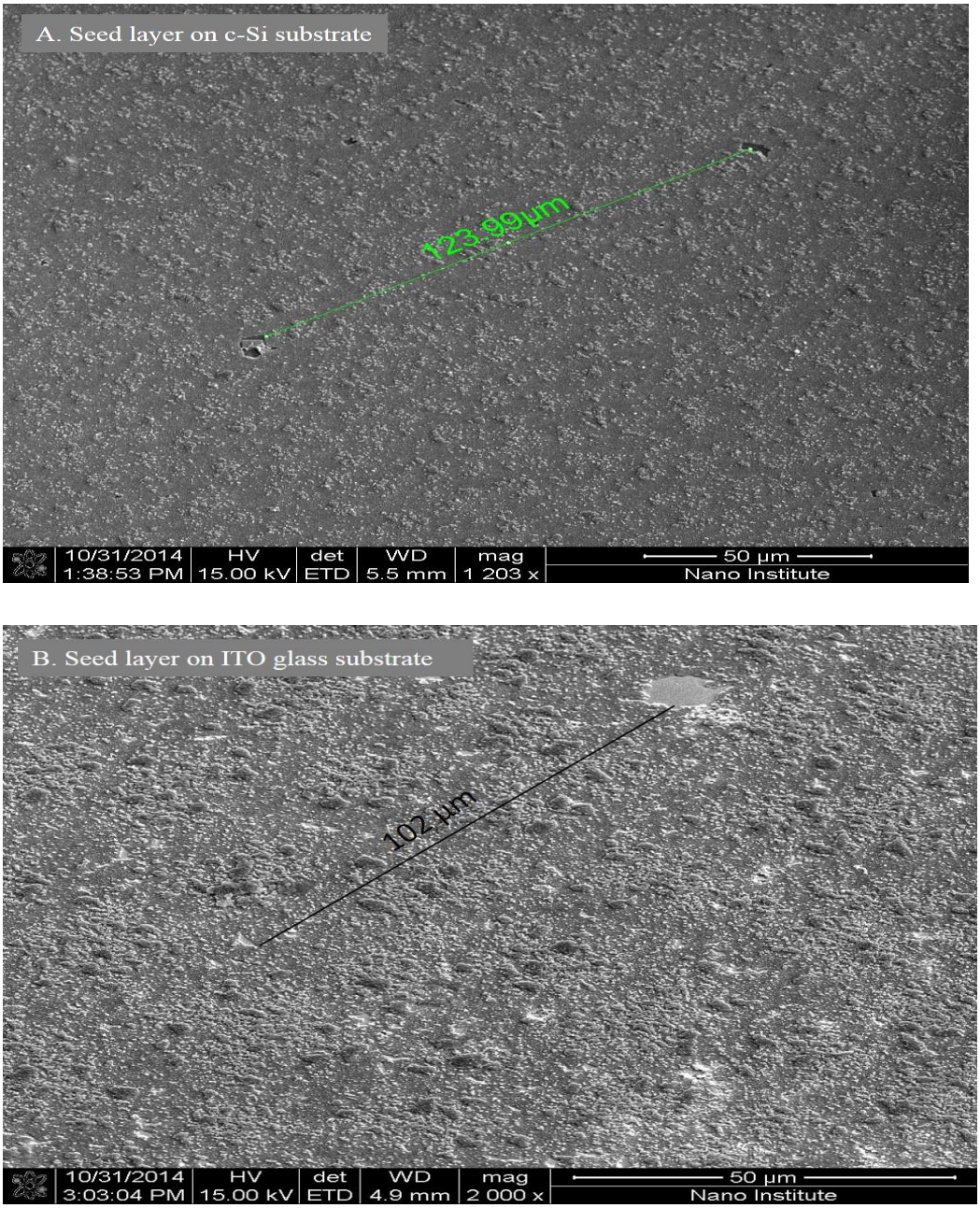

Figure 45. SEM images for: A. AIC seed layer on c-Si and B. AIC seed layer on ITO glass.

Raman scattering in Figure 46 shows that the samples were crystallized by AIC according to the sharp peak at 519 cm^{-1} on c-Si substrate and 515 cm^{-1} on ITO coated glass substrate, but this peak at 515 cm^{-1} is shifted toward lower wavelength numbers. Thus, the film had a strain thought to be tensile. The FWHM of the samples were about 12 cm^{-1} compared to 10-11 cm^{-1} a FWHM of c-Si value. The crystalline fraction was about 93% on c-Si substrate and about 91% on ITO glass.

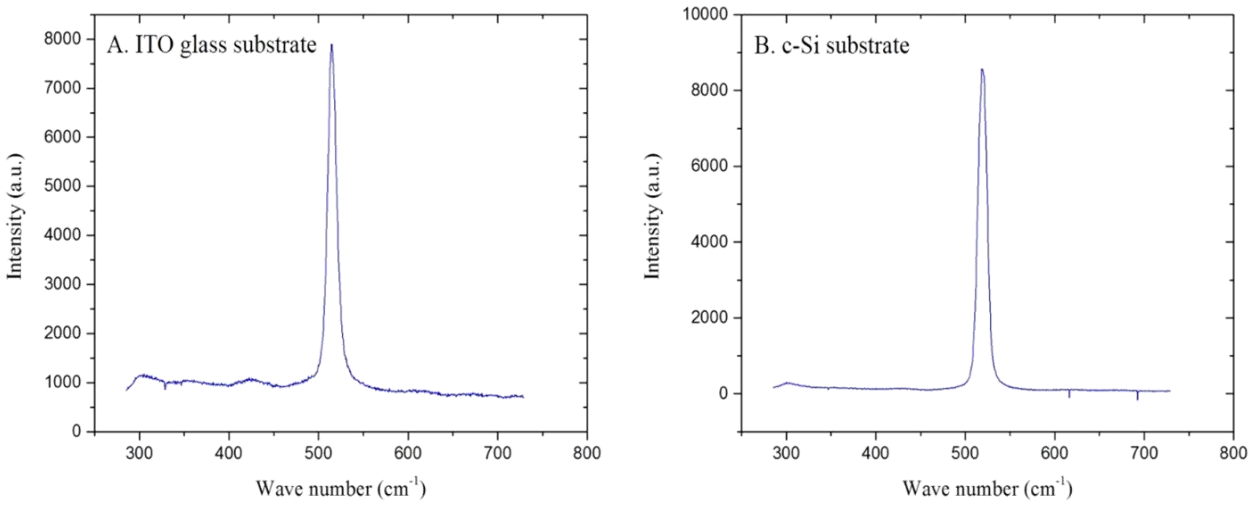

Figure 46. Raman scattering for samples after AIC process: A. ITO coated glass substrate, and B. c-Si substrate.

In X-ray diffraction pattern, different orientations were observed in both ITO glass samples and c-Si samples with a strong (111) peak. Also, other peaks of Si were present in the AIC seed layer on ITO glass substrate that were at (220) and (311) orientations.

The other peaks were coming from the ITO glass substrate. At 20° the orientation is (211), at 30° it is (222), at 35° it is (004), and at 50° it is (044). Figure 47 demonstrates the strong peaks around (111) and the other weak peaks that were present as well in both samples at different oxidation thicknesses.

The ITO coated glass seed layer XRD results at three days oxidation were similar to the results at one day oxidation. Figure 47 shows XRD pattern for ITO glass seed layer and c-Si seed layer that were exposed to ambient air for three days to develop native oxide on the Al layer before the deposition of a-Si:H.

On the other hand, c-Si substrate showed different XRD patterns at one day of Al oxidation and three days of Al oxidation in the ambient air. At one day oxidation, only one strong peak was present with noise that makes it difficult to evaluate the pattern. At three days oxidation there were multiple peaks of Si at (111), (220), and (311).

The noise that was present with (111) peak could be explained that the intensity of the other orientations was very weak due to small grain sizes and low density of crystals. Then, at three days of Al oxidation, the grains were larger and so more orientations were present in the XRD pattern as shown in Figure 48. This result agrees with many studies which suggested that the oxide thickness controls the grains sizes[48]. The grain size increases with increasing the oxide thickness.

Pole figure measurements were also done around (111) to examine the direction of the grown film. Figure 49 shows pole figure images for the samples that were exposed to ambient air to develop Al-oxide for one day and three days before a-Si deposition. It appears that the deposited film was grown in one direction (111) in the seed layer that was deposited on ITO glass substrate.

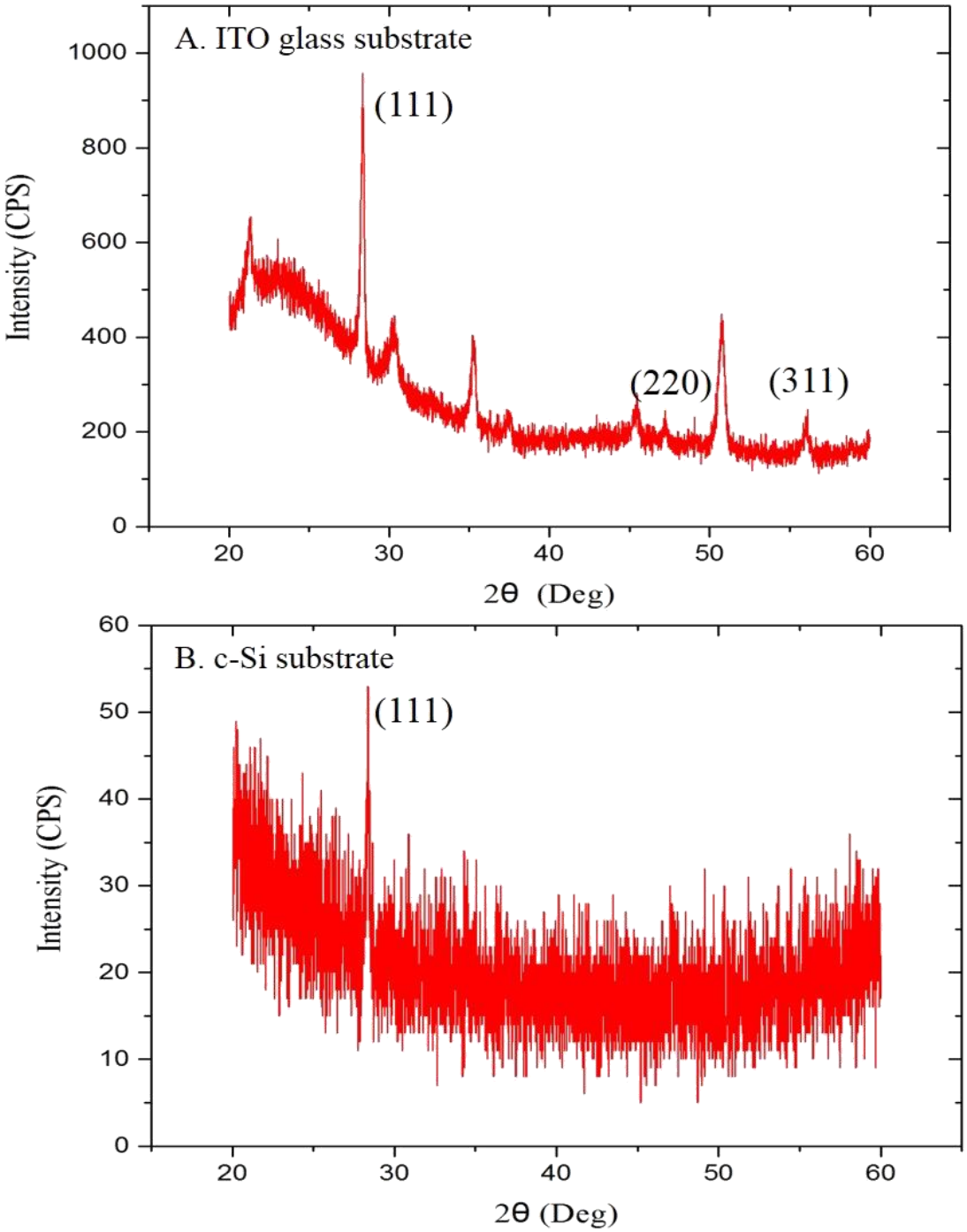

Figure 47. XRD results of θ-2θ scan for two samples that were fabricated using AIC method (one day oxidation): A. ITO glass and B. c-Si seed layer.

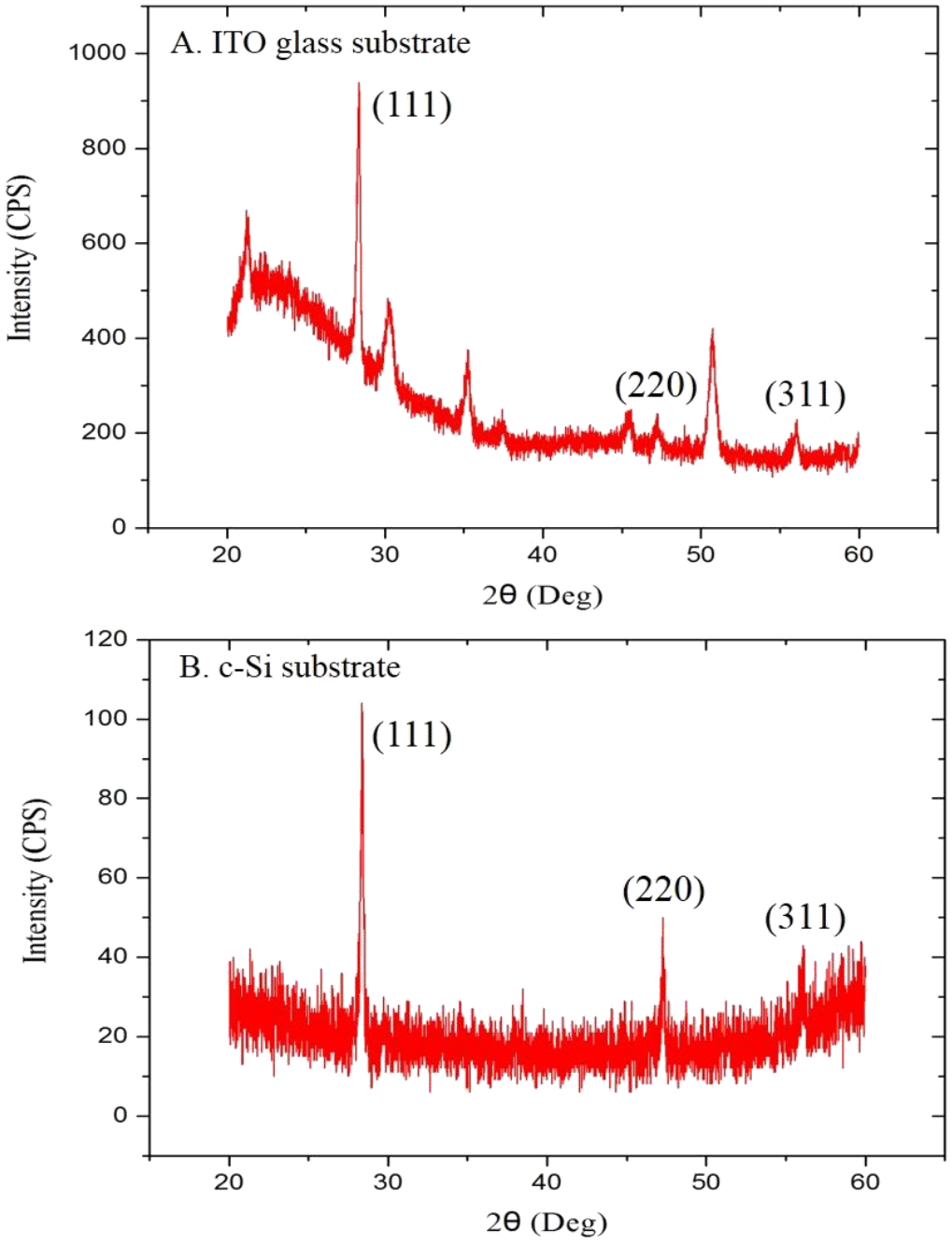

Figure 48. XRD results of θ-2θ scan for two samples that were fabricated using AIC method (three days oxidation): A. ITO glass and B. c-Si seed layer.

In the seed layer that was deposited on c-Si substrate there was a contribution coming from the substrate that led to the presence of the four strong peaks. It seems that the film was randomly oriented due to the same density that is distributed everywhere. However, there are also four other weak peaks in the center, which are coming from the film, and are going the same direction as the strong peaks.

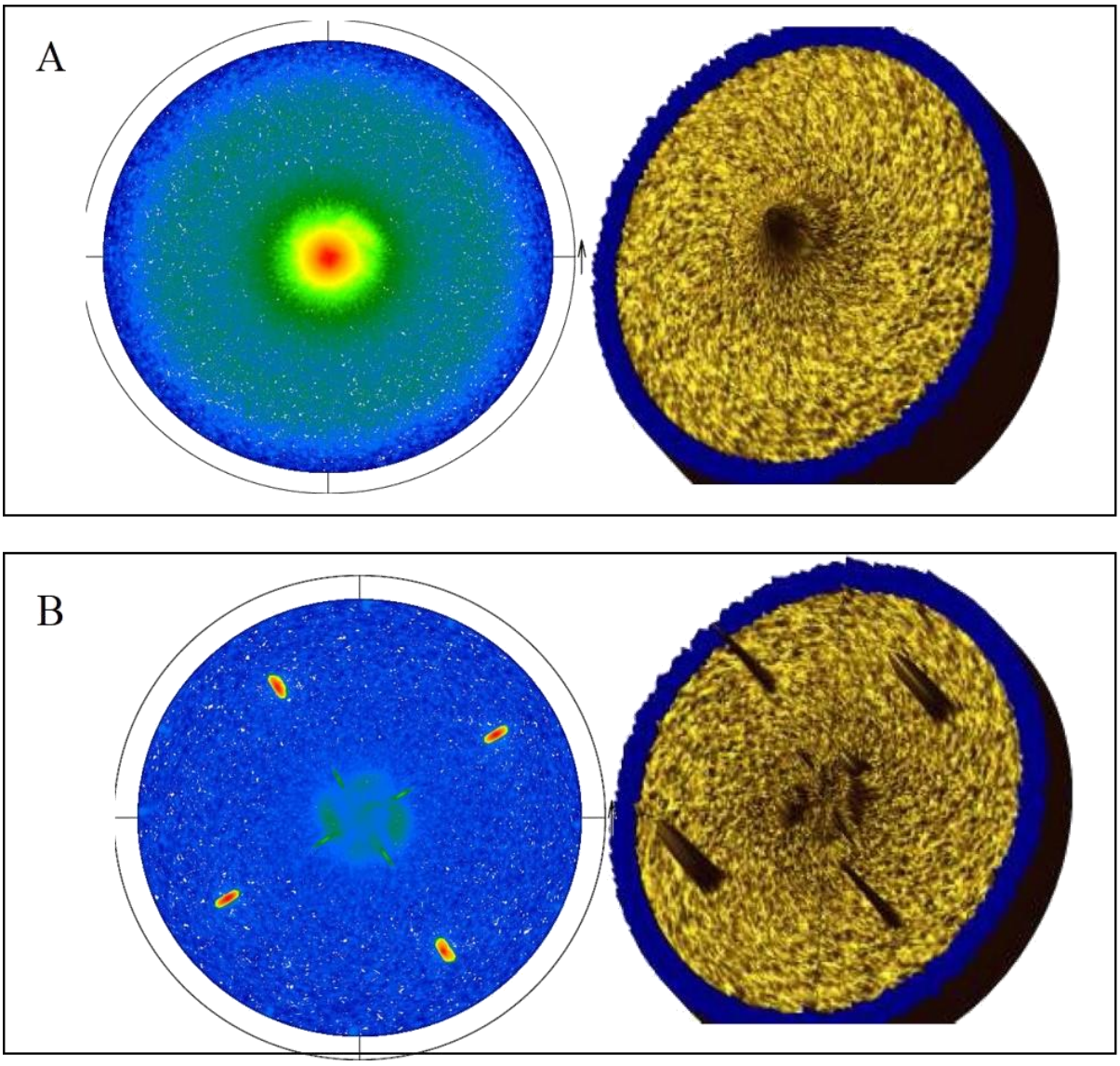

Figure 49. XRD pole figure results for the AIC seed layers that were exposed to ambient air for three days: A. ITO glass seed layer, and B. c-Si seed layer.

The weak intensity of these peaks differentiates them from the high intensity of the strong four peaks. The fact that both sets of peaks are going in the same direction means that some of the grains in the film grew epitaxially on the (100) c-Si substrate. The differing intensities of the peaks shows that the set with the stronger intensity came from the substrate, and the set with the weaker intensity came from the film.

Transmission electron microscopy images showed that the seed layer was a single crystal and it was difficult to find the grain boundaries. Although some stacking faults were present, the orientation was maintaining the crystalline Si substrate orientation. Figure 50 shows TEM image for the seed layer on c-Si substrate.

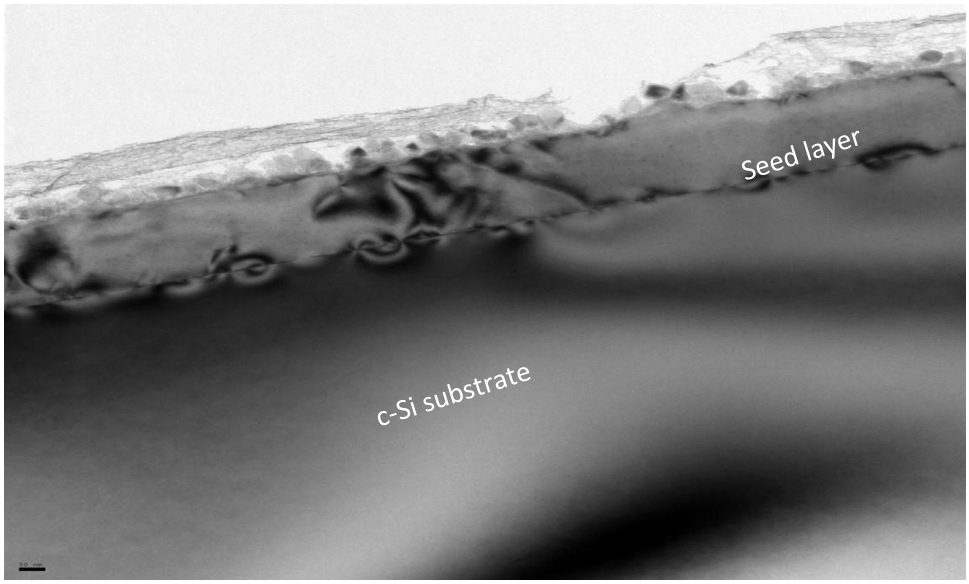

Figure 50. TEM cross sectional image that shows seed layer growth on c-Si substrate.

Figure 51 shows a cross sectional TEM image for the seed layer and c-Si substrate at higher magnification. The orientation of seed layer is the same as the c-Si substrate which was something that no one has reported before. The peaks in the XRD pattern can be explained that

they are coming from the small islands on the continuous seed layer. The interface according to EDX analysis is Al which was not completely removed by wet etching.

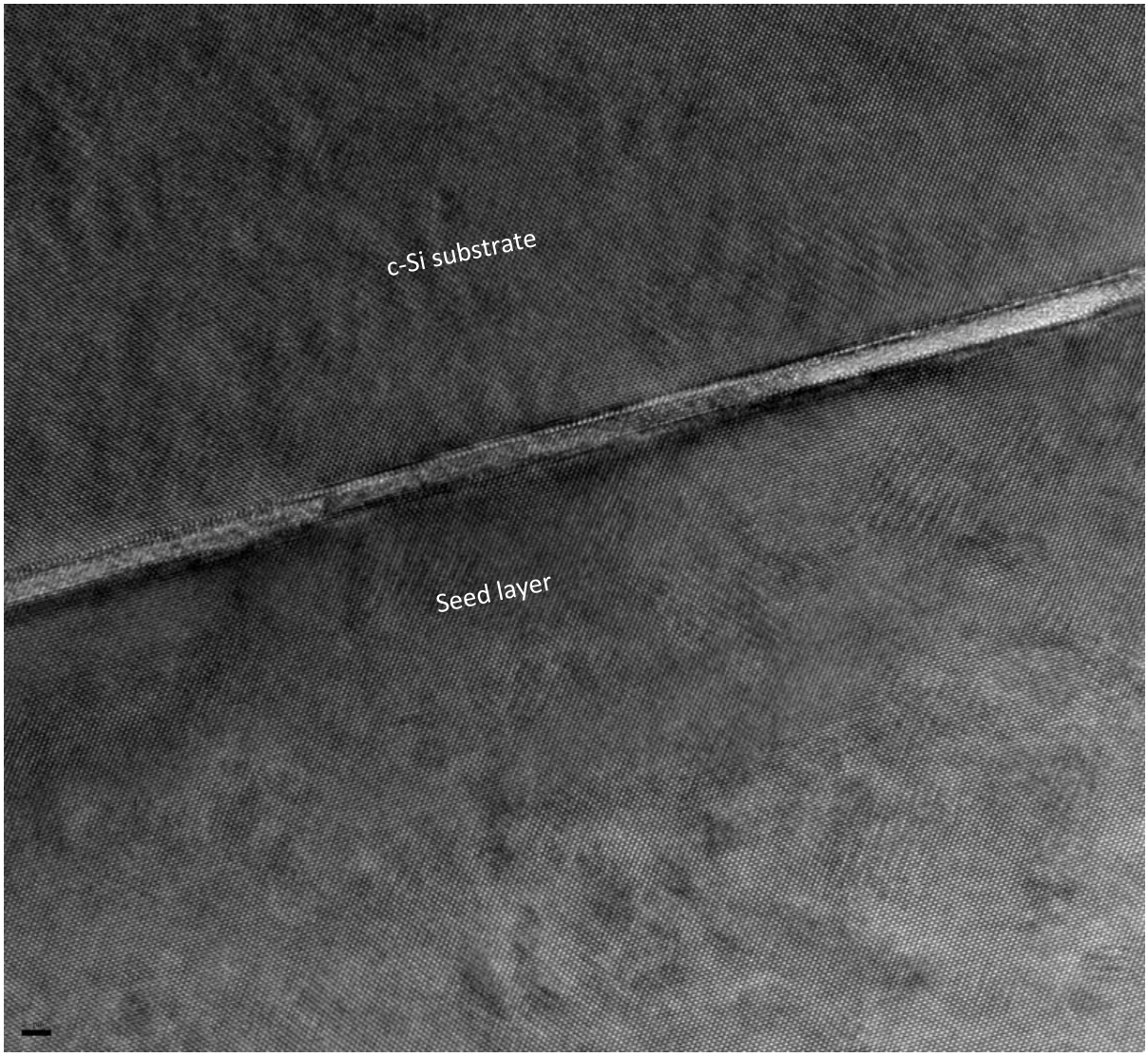

Figure 51. A cross-sectional TEM image that shows the single layer of Si that were growing using AIC.

5.2.1.1 Hall Effect measurement

Electrical properties of the seed layers were determined using Van der Pauw Hall Effect measurement.

Table 9. Electrical properties of poly-crystalline Si thin film seed layer on different substrates.

Samples	Resistivity (ρ)(Ω.cm)	Hall Coefficient (R_H)	Mobility(μ_m) ($cm^2/(V.s)$)	Carrier Concentration (cm^{-3})	Dopant type
Poly-Si/ glass substrate (TAIC)	1.78×10^{-1}	4.7	26.4	1.33×10^{18}	p-type
Poly-Si/ITO/glass Substrate (AIC)	5.88×10^{-4}	-1.99×10^{-2}	33.84	3.14×10^{20}	n-type
Poly-Si/c-Si Substrate (AIC)	5.47×10^{-3}	3.85	703.8	1.6×10^{18}	p-type

After the fabrication of the seed layers by means of AIC method, resistivity, mobility, carrier concentration and Hall coefficient were measured. Table 9 demonstrates the electrical properties of the large grained poly-crystalline Si thin film seed layer on bare glass, ITO glass and c-Si substrates. The negative hall coefficient indicates that the material is an n-type material while a positive hall coefficient indicates a p-type material. Although Hall coefficient shows that the large grained poly-crystalline Si is an n-type material, it is unexpected results as AIC method provides a heavily doped p-type seed layer. This is because Al has three atoms in outer most shell so it behaves as an acceptor in Si. Thus, it must be a result that came from using ITO coated glass substrate for the seed layer.

The ITO coated glass is a good contact and a heavily doped n-type material which can form a tunneling junction with the heavily doped p-type thin seed layer. When performing Hall measurement, the current goes through the poly-crystalline Si film to the ITO film because of the high conductivity compared to the poly-crystalline thin film. Additionally, the resistivity of the

ITO thin film is lower, which makes the current tunnels through the poly-crystalline layer to the ITO layer.

Similarly, the c-Si substrate is a p-type material, which means that the Hall coefficient is a result coming from the substrate. Only the bare glass result provides evidence that the poly-Si seed layer was a p-type material. In summary, the resulting large grained poly-crystalline Si was a p-type material despite the Hall effect measurements.

5.2.2 Epitaxial Growth on the Seed Layers

After preparing the heavily doped p-type poly-crystalline Si seed layers, the seed layers were dipped in HF acid for about 30 mins. It was difficult to clean silicon dioxide that developed on the surface of the seed layer on a glass substrates because the HF acid etches the glass. As a result, two approaches were performed on the seed layers that were on c-Si substrates before using the glass substrates. The first approach was etching the oxide using HF dip before loading them in the chamber for epitaxial growth. The other approach was using the seed layer on c-Si without etching the oxide.

Figure 52 shows SEM micrographs with HF etching and without HF etching after epitaxial growth. The deposition was done in HWCVD chamber at a base pressure about 10^{-5} torr and substrate temperature of 600 °C and diluted SiH_4 in H_2 1:200 sccm.

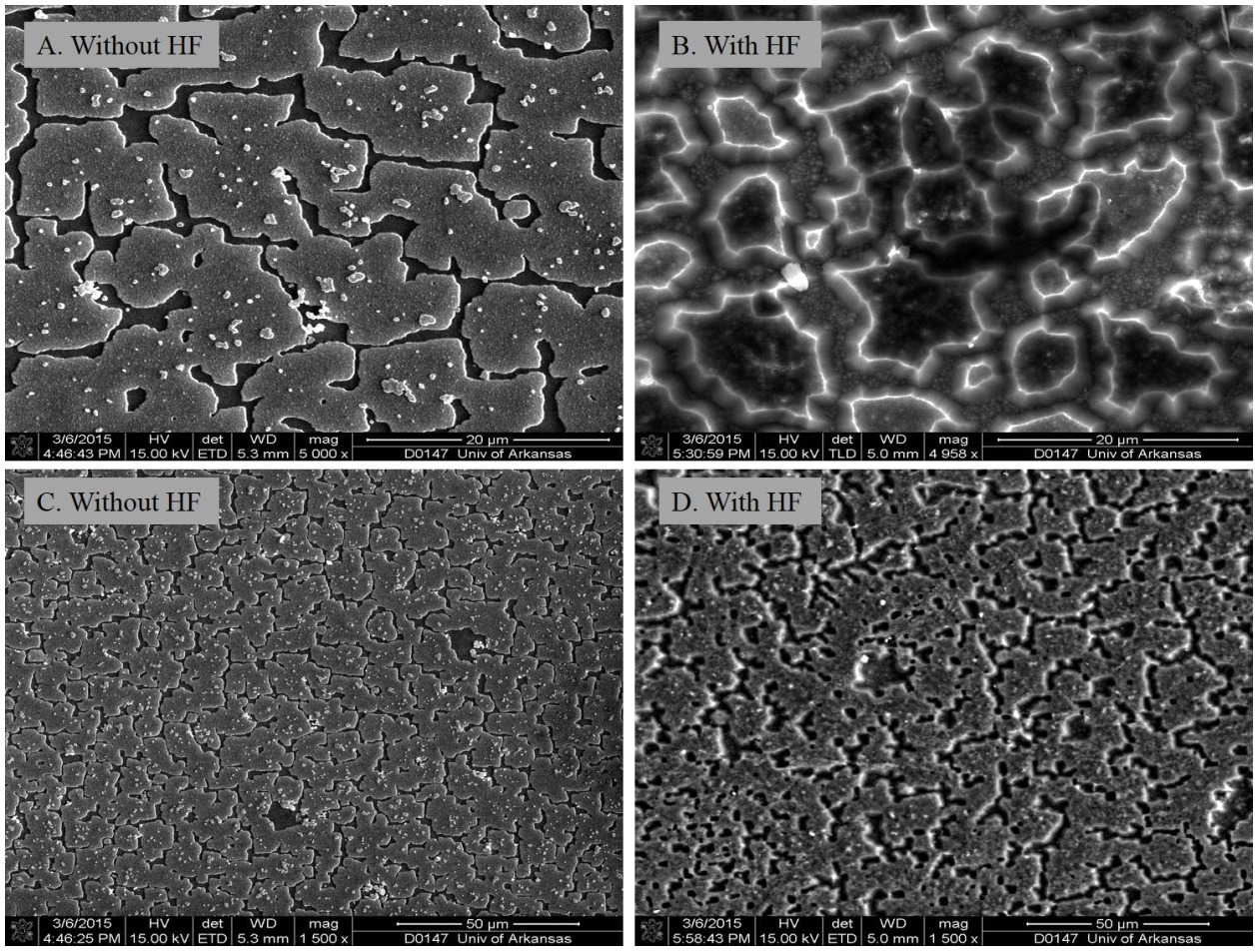

Figure 52. SEM micrographs with different magnifications for two samples: A and C were with HF treatment, B and C were without HF treatment.

The morphology of the surface appeared different in the SEM images. The grain boundaries were present in both samples but there was unexpected morphology on the seed layer that was cleaned with HF dip.

The grain boundaries looked like a 3D-like shaped structure. On the other hand, for the sample that was not cleaned with HF acid, the result was similar to the seed layer before epitaxial growth. Figure 53 shows SEM image for the seed layer on c-Si before and after epitaxial growth.

The similarity in the grain sizes suggested that the epitaxial growth of Si was successfully obtained on the majority of the grain orientations.

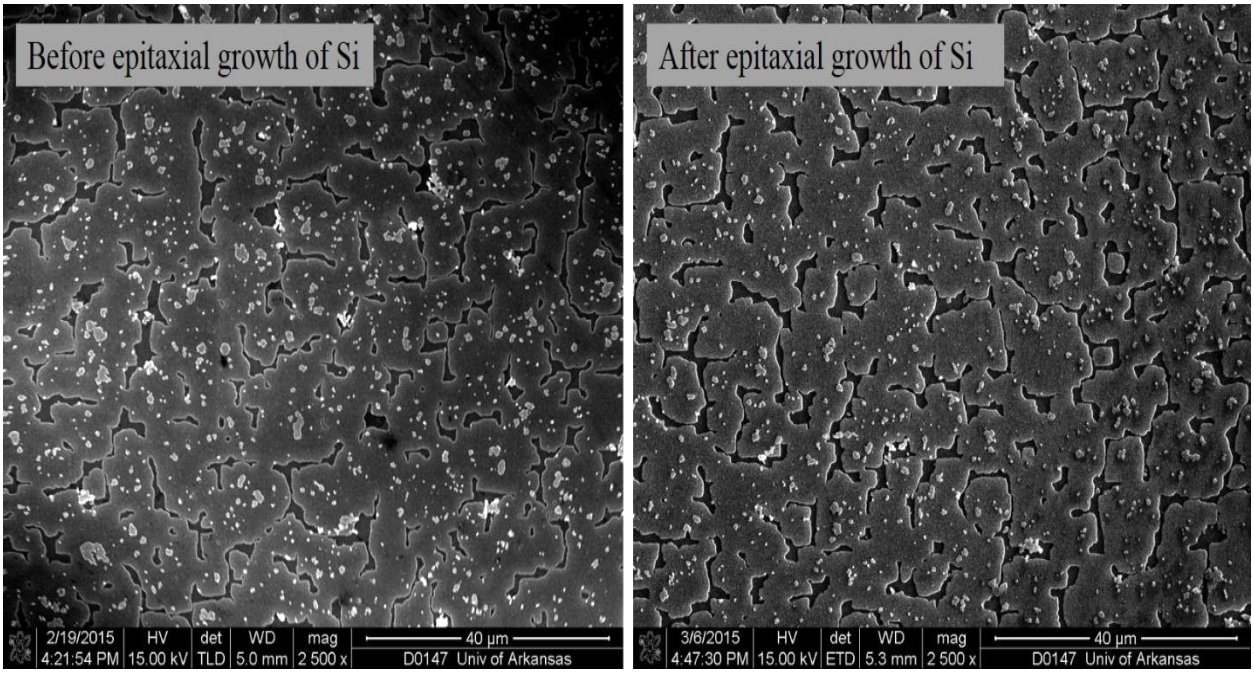

Figure 53. SEM micrographs of AIC seed layer on c-Si substrate before and after epitaxial growth.

The seed layers on ITO glass substrates were loaded in the chamber without HF cleaning. The results after the epitaxial growth were similar to those for in c-Si substrate as similar grain sizes before epitaxial growth and after the growth were obtained. Figure 54 demonstrates the morphology of the surface before epitaxial deposition and after epitaxial deposition on ITO glass substrates. It can be said that the epitaxial growth was successfully attained. Otherwise, smaller grain sizes would be present after the epitaxial growth.

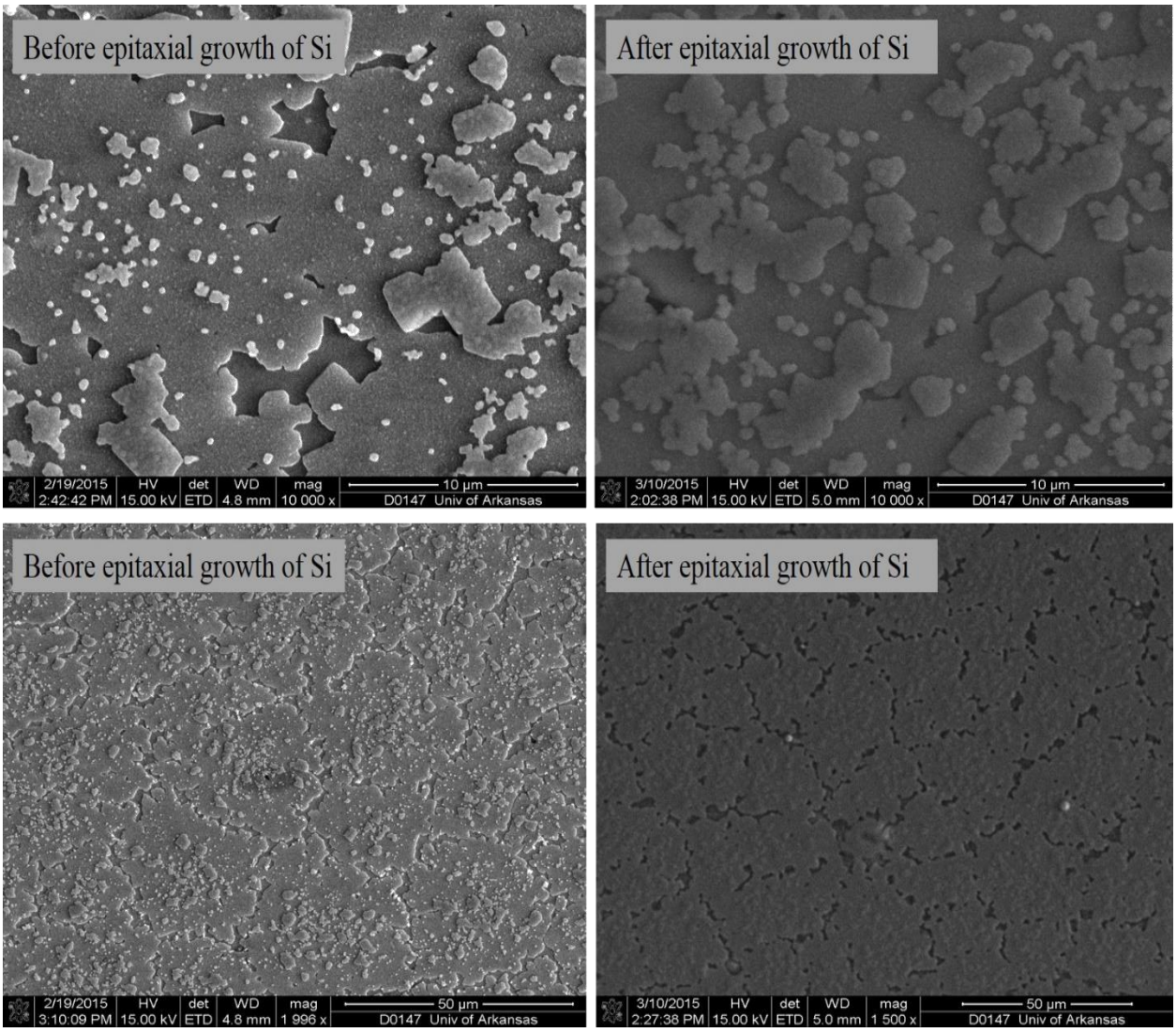

Figure 54. SEM images for seed layers on ITO glass before epitaxial growth and after epitaxial growth.

Raman characterization for both epitaxial growth of Si on c-Si and on ITO glass substrates are shown in Figure 55. A c-Si sharp peak at 519.8 cm^{-1} is present in the epitaxial growth of Si on the seed layer that was deposited on c-Si substrate and the corresponding FWHM is 11 cm^{-1}. On the other hand, the epitaxial growth of Si on the seed layer that was deposited on ITO glass substrates shows a sharp peak at 518.9 cm^{-1} and the FWHM was 13 cm^{-1}.

The crystalline volume fraction, Xc, calculated for both substrates was 93% on c-Si substrate but 90% on the ITO coated glass substrate. Therefore, the crystalline quality was high and may indicate that the film grew epitaxially on the substrate.

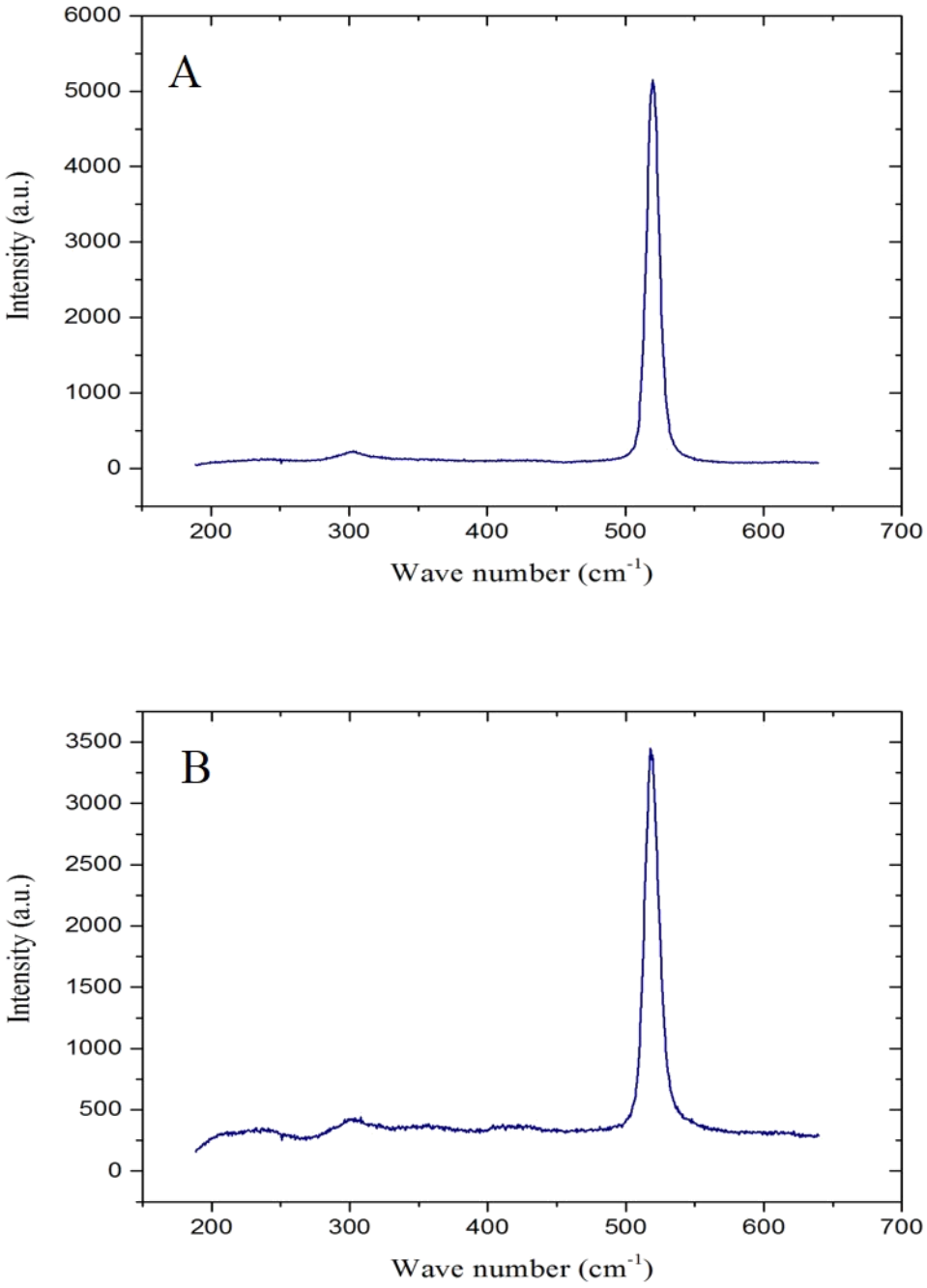

Figure 55. Raman scattering for epitaxial growth of Si on large grained poly Si on: A. c-Si substrate, and B. ITO coated glass substrate.

The XRD pattern results were investigated as shown in Figure 56. When removing the silicon dioxide on the seed layer prior to the epitaxial growth, the results showed a strong peak at (400) direction. Conversely, the seed layer that was not cleaned before the epitaxial growth, showed a peak at (400) but with other weak peaks at (111) and (220).

It could be explained that HF dip reduced the grain boundaries and defect density so that the grains epitaxially grown diffracted a peak at (400). Another possibility might be related to a thinner film that was left after the removal of the surface oxide. Thus, the diffracted peak could be coming out from the c-Si substrate. Further investigation is required in order to understand this result.

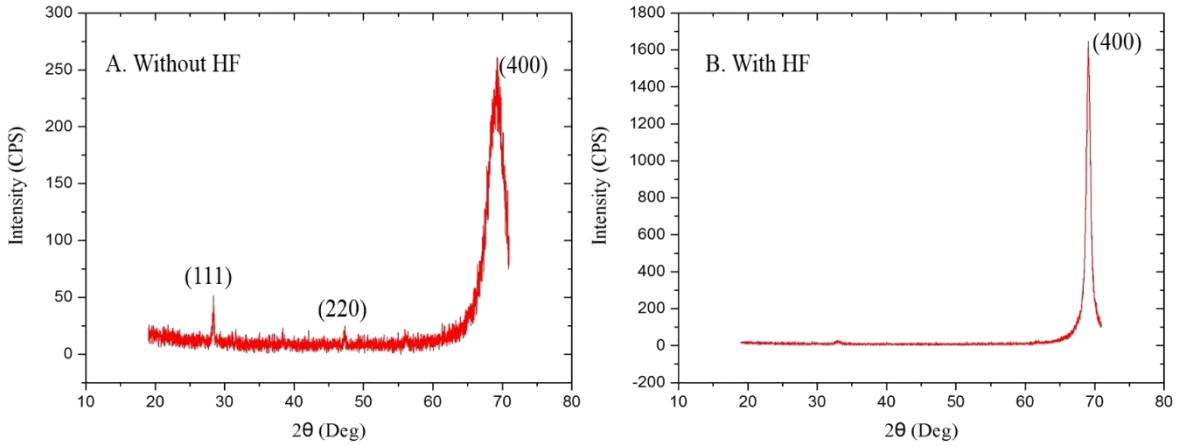

Figure 56. XRD pattern of: A. the poly-Si layer on c-Si without HF cleaning, and B. the poly-Si layer on c-Si with HF cleaning.

Figure 57 demonstrates XRD results of poly-crystalline Si layer on ITO coated glass substrate. Different peaks are present which are a strong sharp peak at (111), and weak peak at (220), (311) orientations and other weak peaks. The poly-crystalline thin layer on ITO glass substrate showed more random growth orientations compared to the c-Si substrate. It is an

expected result as the hetero-epitaxial growth is more difficult than homo-epitaxial growth as previously explained in Chapter Two.

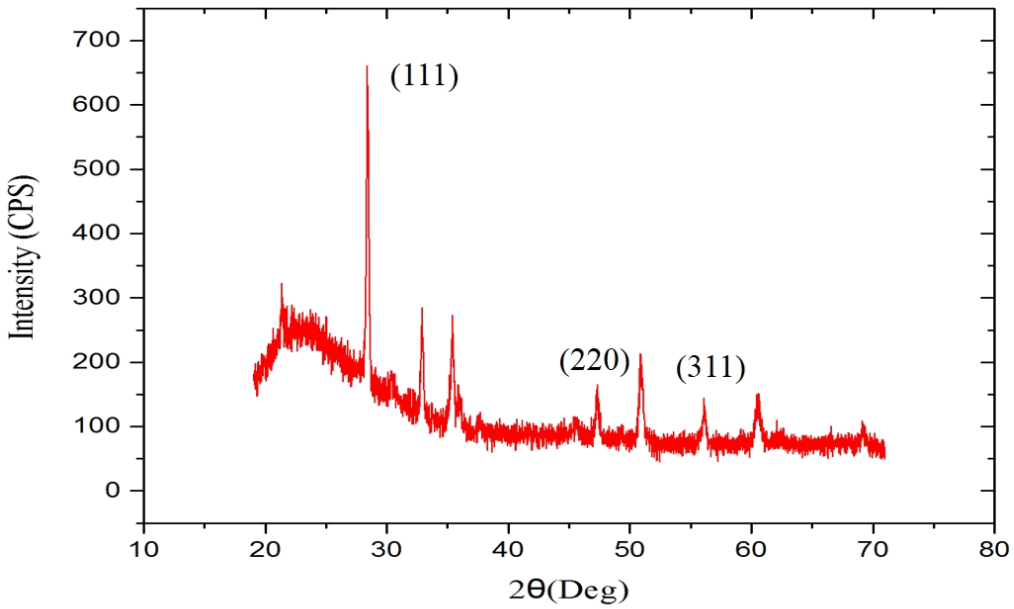

Figure 57. XRD pattern for poly-crystalline Si layer on ITO glass substrate.

The TEM cross sectional image in Figure 58 shows the structure c-Si substrate/AIC seed layer/ epitaxial growth of Si + poly Si. The TEM image suggests that the AIC seed layer had large grains that could be a very large single crystal but with stacking faults that were observed as well. It is an interesting result that even with the stacking faults, the orientation continued to be the same as the orientation before the stacking faults. The seed layer thickness was about 250 nm while the epitaxial thickening of Si was about 200 nm.

In Figure 59, the TEM image gives a closer look at the AIC seed layer/epitaxial growth of Si interface where different material was observed which could affect the epitaxial growth. This material is Al that was left after Al etching according to EDX results. It could be the reason for the Moiré fringes that appeared in the TEM image.

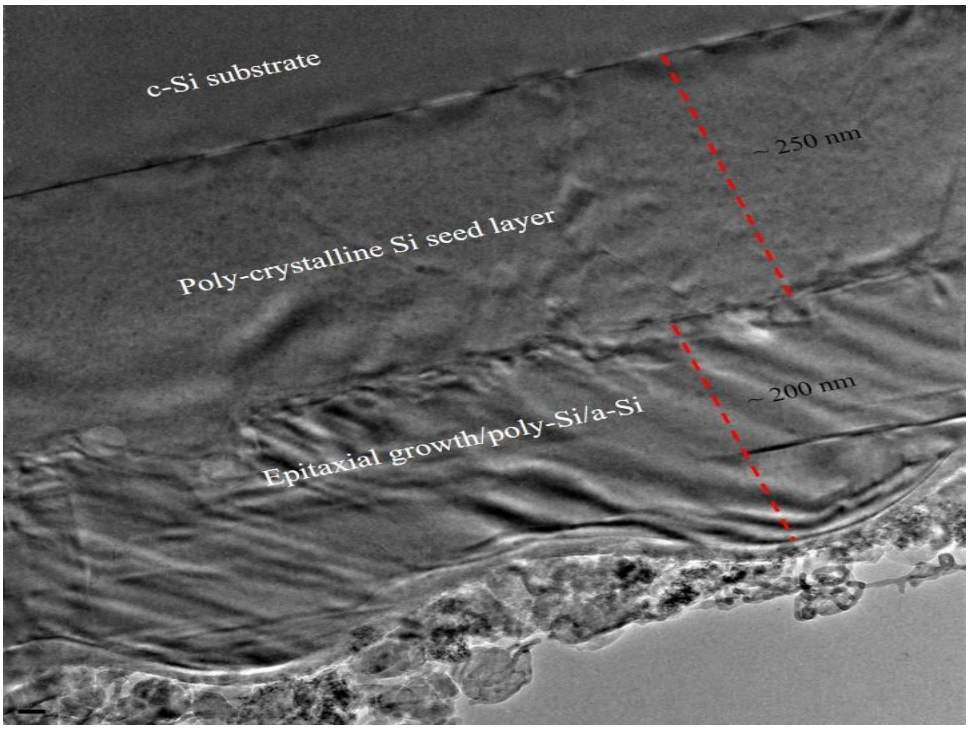

Figure 58. TEM cross-sectional image for epitaxial growth of Si on AIC seed layer.

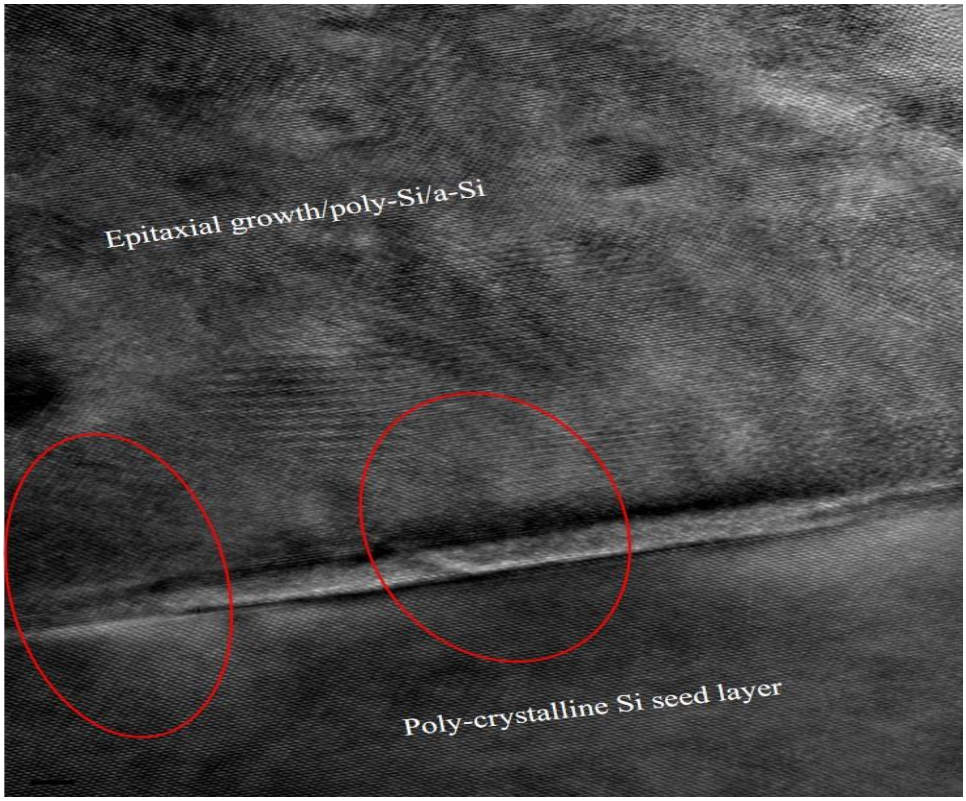

Figure 59. TEM image for epitaxial growth of Si on AIC seed layer.

Moiré fringes in TEM images means that there are different crystal orientations on top of each other. Moiré fringes are defined as “set of dark fringes produced when two ruled gratings or uniform patterns are superimposed”[49]. These fringes can be seen as parallel dark/light bands in the TEM images.

The growth rate of epitaxial Si layer was only about 7 nm /min which is a very low growth rate so defects could have occurred. This low growth rate was because the SiH_4 flow rate was only 1 sccm. In summary, the epitaxial growth was obtained at 600 °C with highly diluted SiH_4 in hydrogen (200:1 sccm) and further optimization is required. The factor that needs to be addressed by future work according to the TEM results is the poly-Si/epitaxial growth of Si interface.

Chapter 6: Conclusion and Future Work

Most of studies in the solar cells industry aim to either increase the efficiency of solar cells or reduce the cost of solar cells. This work focused on reducing the cost of solar cells. A drastic reduction in the cost might possibly attained when using glass as a substrate instead of using Si. Epitaxial growth was first done directly on c-Si and Corning glass substrates. The optimized results of this process were applied to the seed layers. Aluminum induced crystallization was utilized to crystallize a-Si:H at low temperatures to prepare the seed layers on glass substrates.

The effort of this project was aimed at preparing large grained poly-Si seed layers to be used for a subsequent step of epitaxial growth of Si. Therefore, heavily doped p-type poly-Si seed layers were grown successfully on ITO and c-Si substrates. Next, epitaxial growth of Si using HWCVD was performed on the seed layers on the various substrates: ITO coated glass and c-Si. Scanning electron microscopy confirmed that the epitaxial layer was successfully accomplished due to the similar grain sizes before the epitaxial growth and after the epitaxial growth. The TEM results showed very large grained AIC seed layer which was almost single crystal as well as epitaxial growth of Si with 200 nm thick.

Future work arising from this conclusion could be geared toward optimizing the process of fabricating a heavily doped p-type poly-Si seed layers for larger grains and a smoother surface followed by deposition of an epitaxial layer of Si for the absorber layer. Lastly, continuing the fabrication of this device to form a solar cell by depositing an n-type heavily doped Si layer and then adding Al contacts could also be investigated.

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Appendix A: Description of Research for Popular Publication

Better ways for cost-effective solar cells

By: Manal Aldawsari

A step toward a cost effective solar cell was taken at the University of Arkansas in Fayetteville in a project to obtain epitaxial growth on large grained poly-crystalline Si performed in Dr. Hameed Naseem's lab and led by Manal Aldawsari, a scientist and a graduate student in the Microelectronics-Photonics program.

Crystalline Si (c-Si) solar cells of approximately 200-500 μm thick dominate the solar cell market. Currently, the Si material accounts for about 50% of the cost of solar cells, because Si is the second most abundant element on earth's crust, thus, c-Si solar cells are reasonably affordable. Silicon can be found in clay, rocks, soils, and sand.

Despite its abundance, an increased demand for solar energy every year will inevitably cause the price of Si to be driven up within the next 50 years. Thus, making solar cells by directly depositing a high quality, thin c-Si layer of about 1 μm thick would not only ease the production of c-Si but also would provide more solar cells at the same price as producing only one conventionally manufactured c-Si solar cell. However, a thin layer of c-Si only 1 μm thick cannot be handled by itself, so, mechanical support is required. This gave rise to the idea of using an inexpensive substrate such as glass as a c-Si substrate replacement to decrease the cost of material and installation.

Glass is amorphous material, which means that the atoms are arranged in random order which makes depositing a layer of c-Si directly difficult. The question is: how can atoms arrange themselves in a crystal order while the underlying substrate is not? Fortunately, Dr. Hameed Naseem of the University of Arkansas has been successful in preparing inexpensive seed layers by using the aluminum induced crystallization (AIC) method. So what if these seed layers were

to be used as substrates for the epitaxial growth of silicon? The resulting solar cells would be more cost effective in response to the ever-increasing demand.

The most pressing issue has been the need for an ultra-high vacuum in order to enable the epitaxial growth. Any contamination on the surface would hinder the success in obtaining a high quality epitaxial growth without breakdown into poly-crystalline Si phase or amorphous-Si phase. Different approaches were taken in order to solve this dilemma such as hydrogenation prior the epitaxial growth in the chamber. Hydrogen atoms play an important role as they etch the defects and a-Si faster than the crystalline Si and passivate the surface.

Despite these challenges, Mrs. Manal Aldawsari managed to produce epitaxial growth on very large grained poly-crystalline Si seed layer at low temperature of 600 °C using hot wire chemical vapor deposition, as part of her graduate project for her master's degree from the University of Arkansas. Mrs. Manal Aldawsari says, "this will significantly improve the solar cell industry as it will make the production of solar cells faster, lower cost and with higher quality."

Appendix B: Executive Summary of Newly Created Intellectual Property

Growth of epitaxial layer of Si on heavily doped p-type low cost substrate at low temperature.

Appendix C: Potential Patent and Commercialization Aspects of Listed Intellectual Property Items

There are no potential patent and commercialization aspects of listed intellectual property items.

C.1 Patentability of Intellectual Property (Could Each Item be Patented)

There is no patentability of IP in this research.

C.2 Commercialization Prospects (Should Each Item Be Patented)

There is no commercialization prospects in this work.

C.3 Possible Prior Disclosure of IP

There is no possible prior disclosure of IP in this work.

Appendix D: Broader Impact of Research

D.1 Applicability of Research Methods to Other Problems

The process of epitaxial growth of Si on large grained poly-Si seed layers has potential for other technologies. Photovoltaic devices are one significant application to use this process in order to decrease the price of the solar panels. Epitaxial growth of Si could also be used in bipolar junction transistors (BJTs).

The heterojunction bipolar transistor (HBT) is an area of in the BJT technology which is usually created using epitaxial growth techniques. In general, silicon based manufacturing methods such as complementary metal–oxide–semiconductors (CMOS) can be developed using epitaxy.

D.2 Impact of Research Results on U.S. and Global Society

Thin film solar cells have been considered as cost-effective solar cells due to the drastic reduction of the active photovoltaic materials. The epitaxial growth technique can be used to produce thin film solar cells at low temperatures which are equivalent to c-Si solar cells.

In this way, the United States and the rest of the world could benefit not only economically but also environmentally. This would make it possible for the world to have a sustainable energy source at an affordable price which would help fulfil the growing demand for energy.

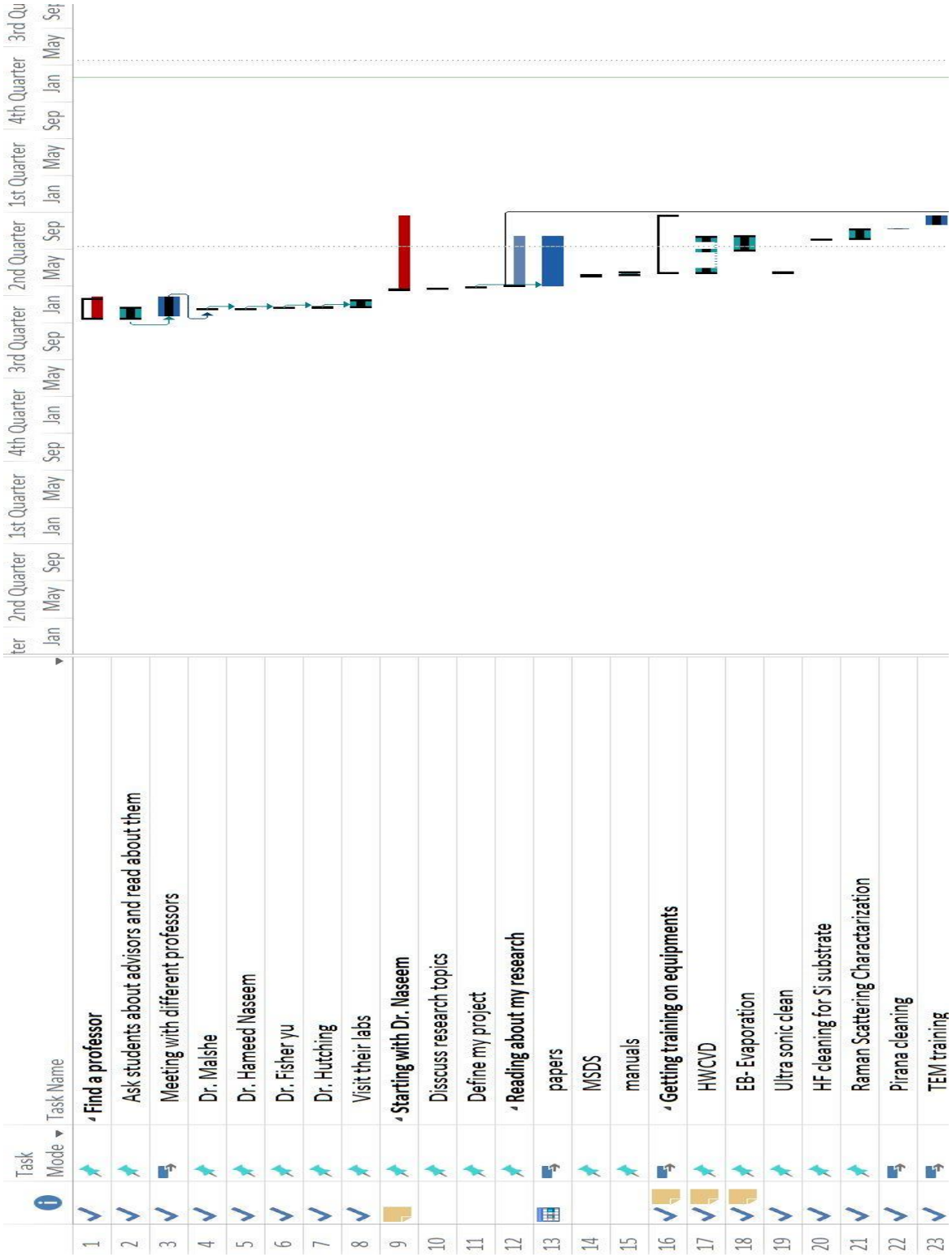
D.3 Impact of Research Results on the Environment

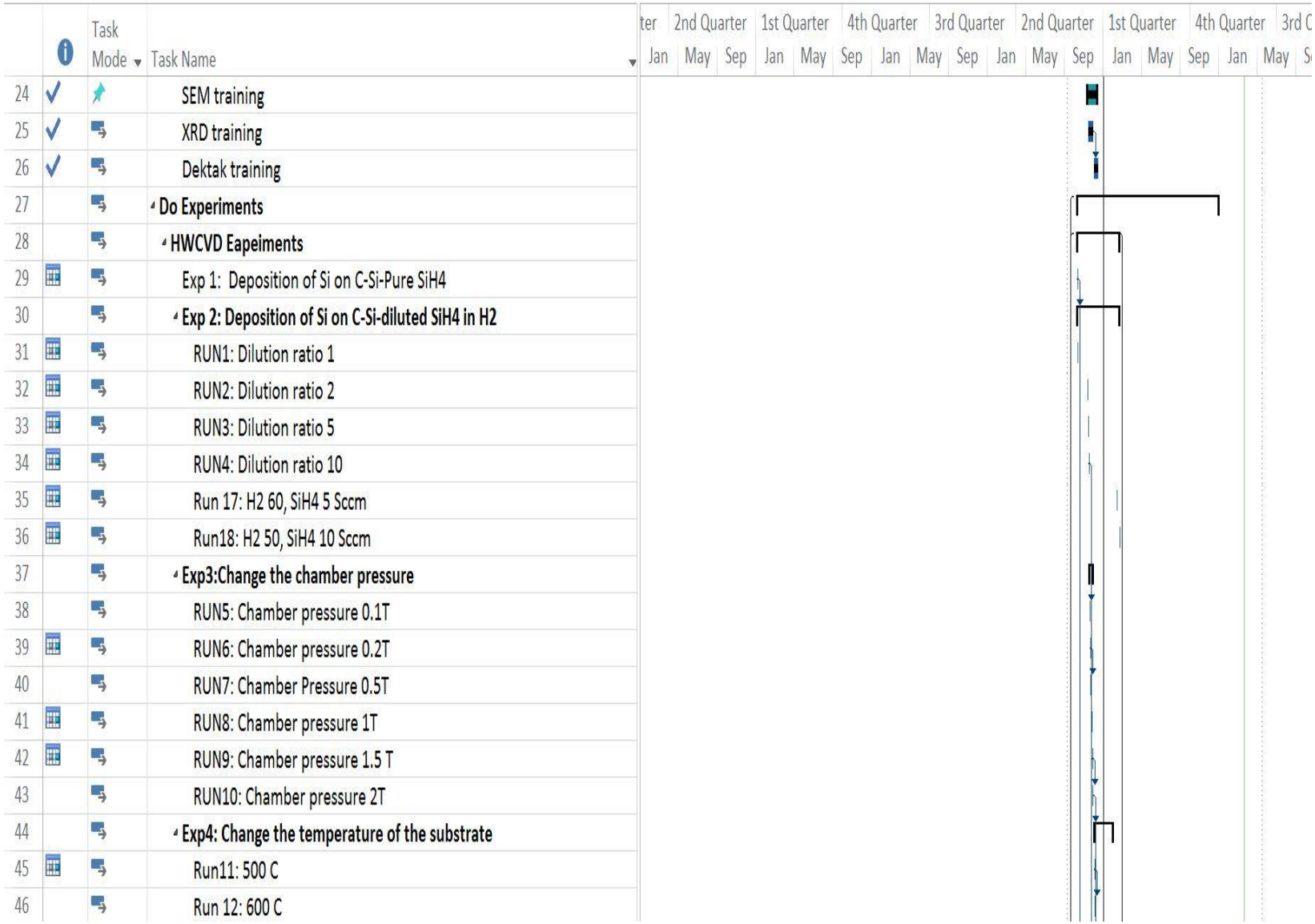
In this work, developing a technology that can be used for solar cells could improve the solar industry. One of the environmental effects of using solar energy is reducing the dependence on fossil fuels and hence the pollution will be reduced.

In addition, the epitaxially grown thin film does not have any harmful effects on the environment, but the processes to produce it gives way to some concerns if they are not handled properly. Using the HWCVD technique to produce epitaxial growth of Si requires the introduction of some gases in the chamber such as H_2 and SiH_4. However, those dangerous gases are well known and have been used in the solar cell industry for decades.

Thus, disposing this waste has been well understood and controlled in this project. Hydrofluoric acid was used as well to remove the native oxide from Si substrate and sulfuric acid for organic contamination removal. Nevertheless, all standard safety system guidelines were adhered to with all of the chemicals used in this research.

Appendix E: Microsoft Project for Ms MicroEP Degree Plan

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ter 2nd Quarter 1st Quarter 4th Quarter 3rd Quarter 2nd Quarter 1st Quarter 4th Quarter 3rd C
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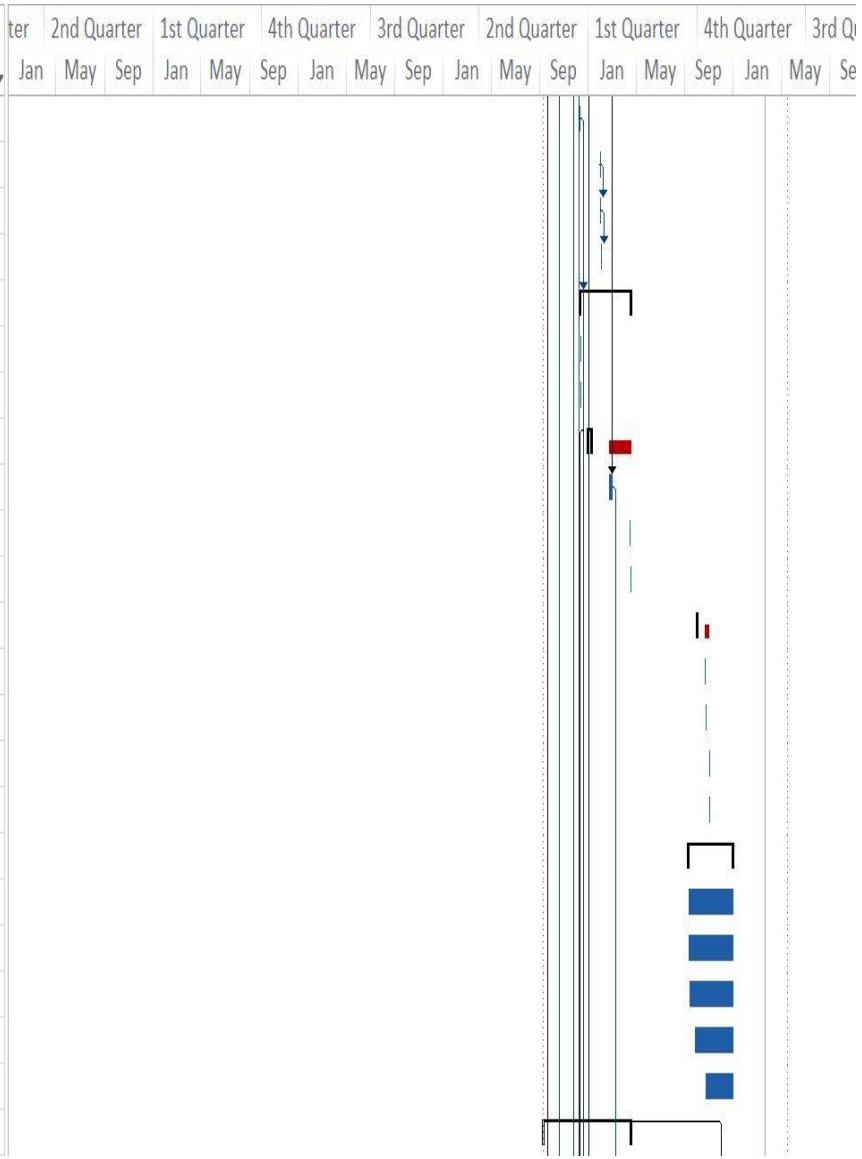
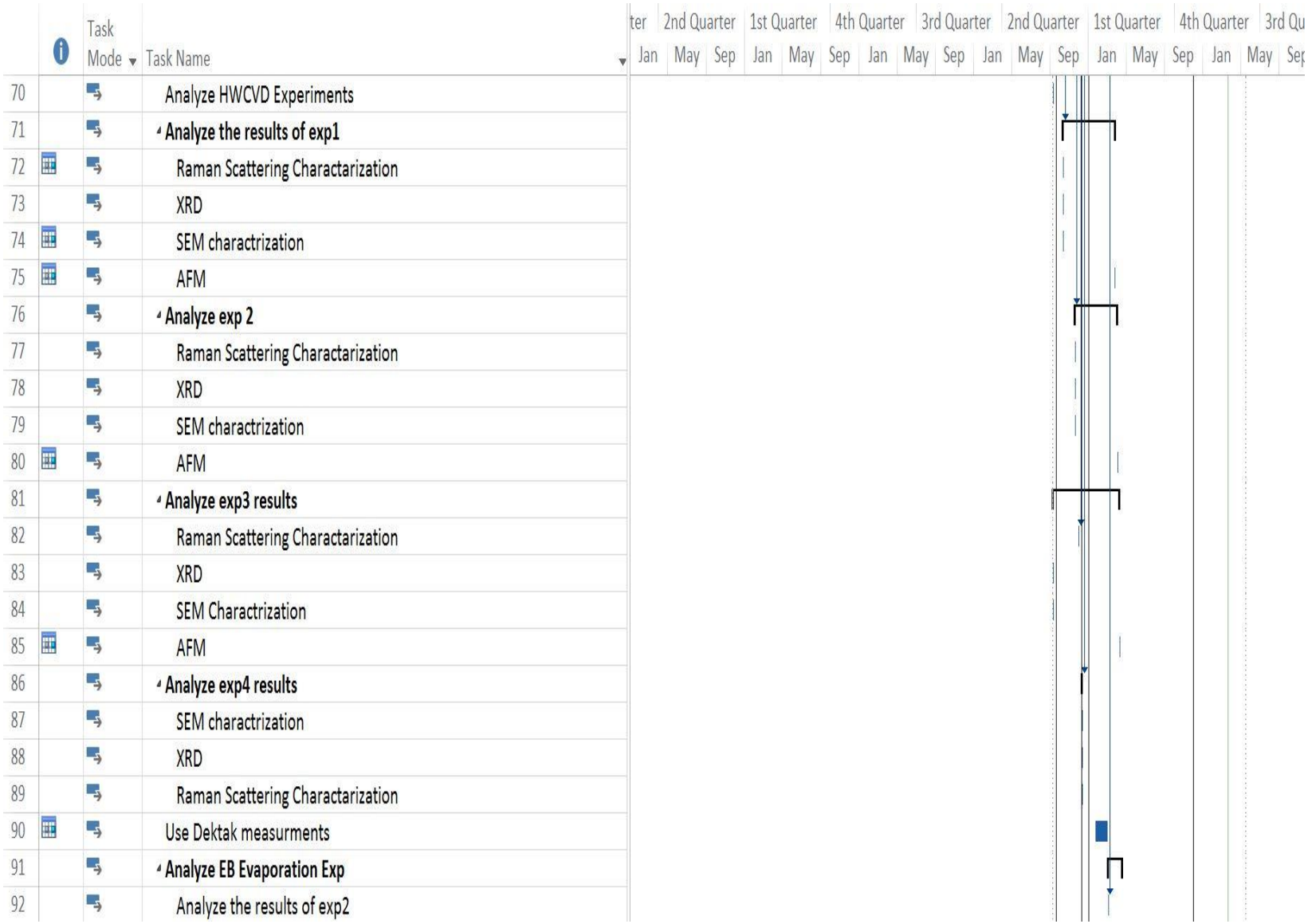
24 SEM training
25 XRD training
26 Dektak training
27 Do Experiments
28 HWCVD Eapeiments
29 Exp 1: Deposition of Si on C-Si-Pure SiH4
30 Exp 2: Deposition of Si on C-Si-diluted SiH4 in H2
31 RUN1: Dilution ratio 1
32 RUN2: Dilution ratio 2
33 RUN3: Dilution ratio 5
34 RUN4: Dilution ratio 10
35 Run 17: H2 60, SiH4 5 Sccm
36 Run18: H2 50, SiH4 10 Sccm
37 Exp3:Change the chamber pressure
38 RUN5: Chamber pressure 0.1T
39 RUN6: Chamber pressure 0.2T
40 RUN7: Chamber Pressure 0.5T
41 RUN8: Chamber pressure 1T
42 RUN9: Chamber pressure 1.5 T
43 RUN10: Chamber pressure 2T
44 Exp4: Change the temperature of the substrate
45 Run11: 500 C
46 Run 12: 600 C

	Task Mode	Task Name
47		Run13: 750 C
48		Run14: 200C
49		Run15: 250C
50		Run16:400 C
51		**Exp5: Deposition of Si on C-Si-Diluted SiH4 in Ar**
52		Exp6: Deposition of Si on glass
53		Exp7: increase the dilution ratio
54		**EB Evaporation Experiments**
55		Exp 1: Dep rate
56		change the substarte to glass
57		change the temperature of annealing
58		**preperation of seed layers**
59		using PECVD in Hidec to dep a-Si
60		using Thermal evaporater for Al dep
61		using IR built furnace
62		using HWCVD TO DEP Si
63		**Analyze the seed layers results**
64		Optical microscope to see the grains
65		Raman Scattering Charactarization
66		SEM
67		XRD
68		AFM
69		**Analyze the results**





	Task Mode	Task Name
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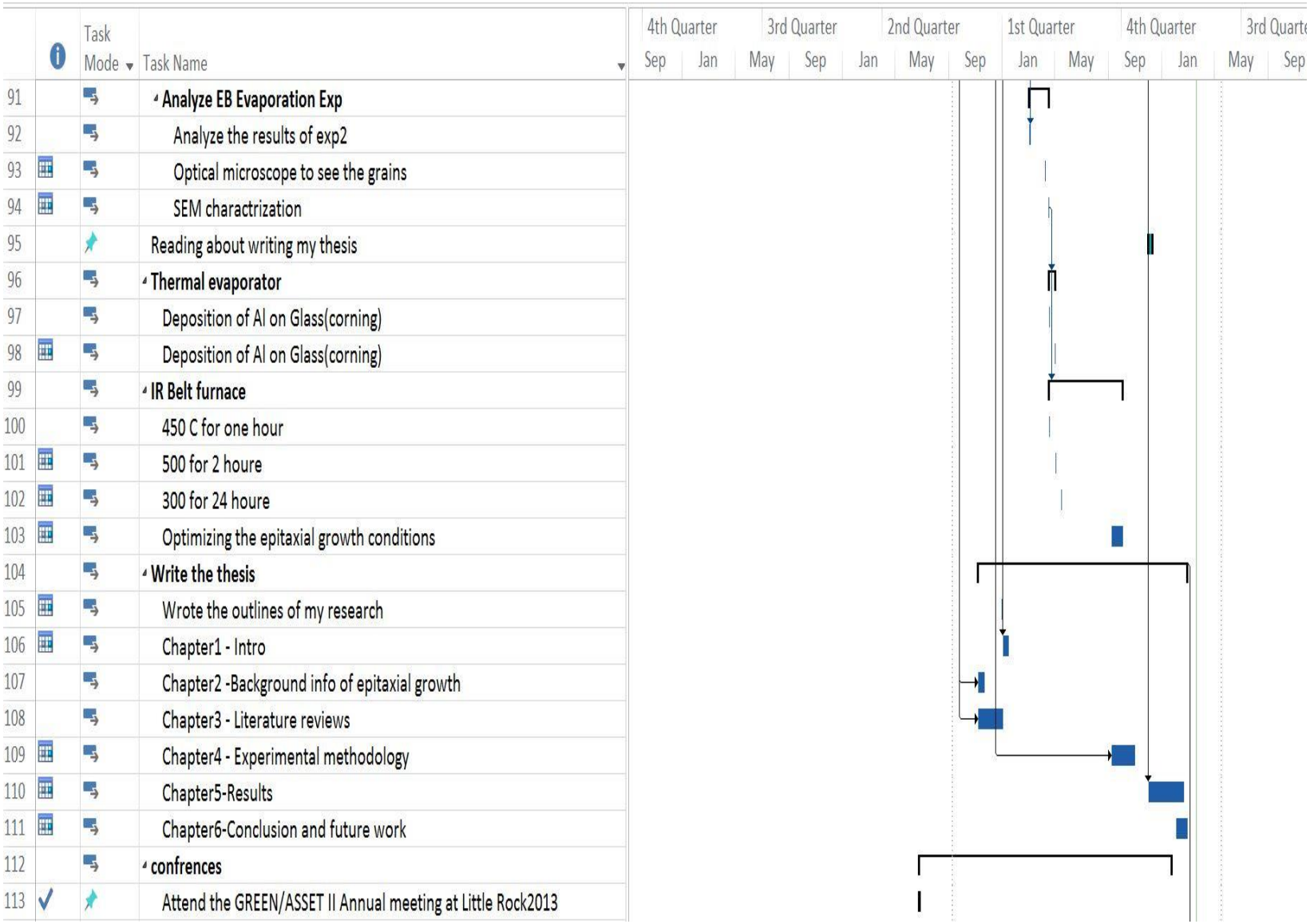
71		**Analyze the results of exp1**
72		Raman Scattering Charactarization
73		XRD
74		SEM charactrization
75		AFM
76		**Analyze exp 2**
77		Raman Scattering Charactarization
78		XRD
79		SEM charactrization
80		AFM
81		**Analyze exp3 results**
82		Raman Scattering Charactarization
83		XRD
84		SEM Charactrization
85		AFM
86		**Analyze exp4 results**
87		SEM charactrization
88		XRD
89		Raman Scattering Charactarization
90		Use Dektak measurments
91		**Analyze EB Evaporation Exp**
92		Analyze the results of exp2


Task Mode
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1st Quarter
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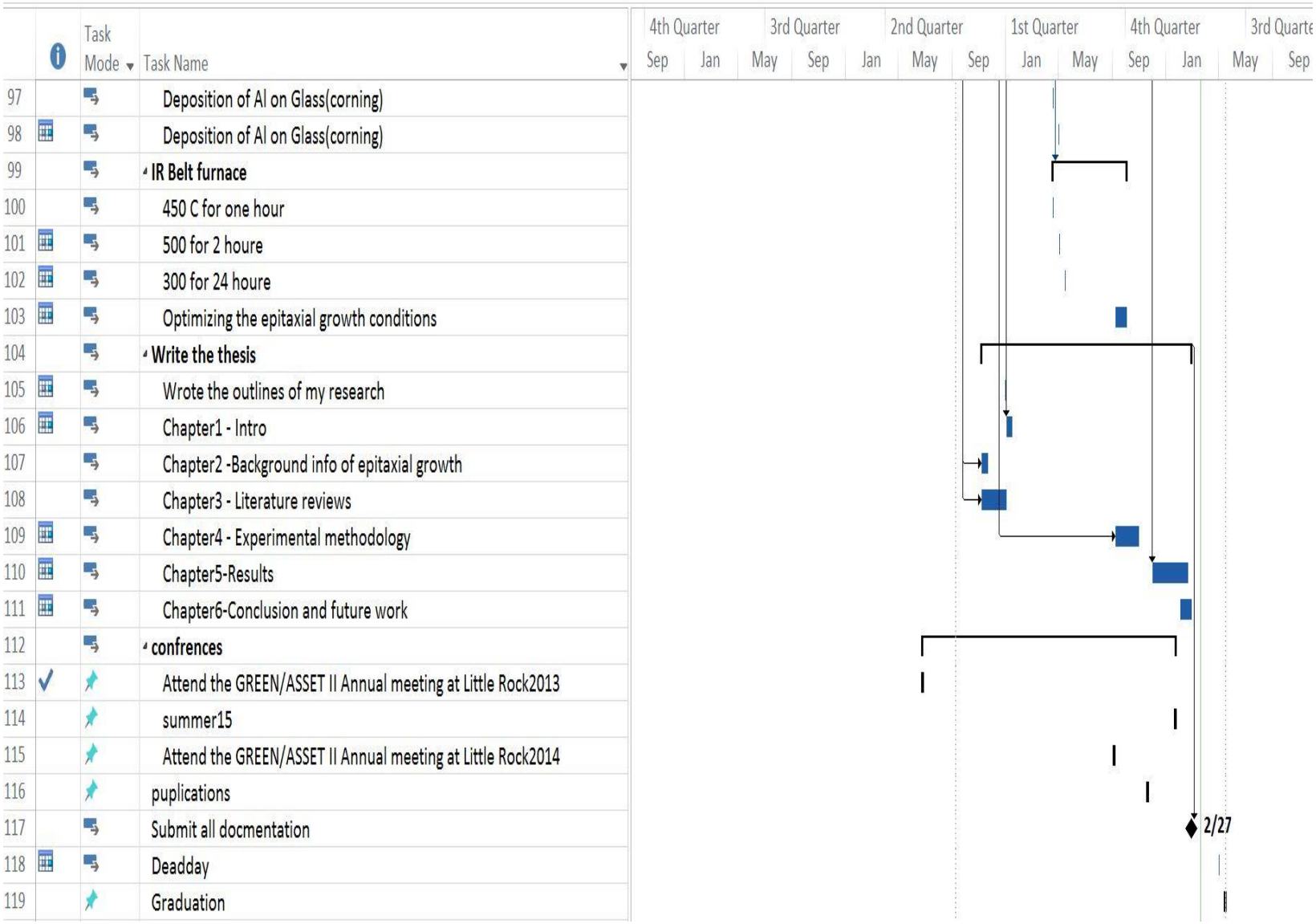
3rd Quarte
Sep Jan May Sep Jan May Sep Jan May Sep Jan May Sep
91 Analyze EB Evaporation Exp
92 Analyze the results of exp2
93 Optical microscope to see the grains
94 SEM charactrization
95 Reading about writing my thesis
96 Thermal evaporator
97 Deposition of Al on Glass(corning)
98 Deposition of Al on Glass(corning)
99 IR Belt furnace
100 450 C for one hour
101 500 for 2 houre
102 300 for 24 houre
103 Optimizing the epitaxial growth conditions
104 Write the thesis
105 Wrote the outlines of my research
106 Chapter1 - Intro
107 Chapter2 -Background info of epitaxial growth
108 Chapter3 - Literature reviews
109 Chapter4 - Experimental methodology
110 Chapter5-Results
111 Chapter6-Conclusion and future work
112 confrences
113 Attend the GREEN/ASSET II Annual meeting at Little Rock2013



		Task Mode	Task Name
97			Deposition of Al on Glass(corning)
98			Deposition of Al on Glass(corning)
99			**IR Belt furnace**
100			450 C for one hour
101			500 for 2 houre
102			300 for 24 houre
103			Optimizing the epitaxial growth conditions
104			**Write the thesis**
105			Wrote the outlines of my research
106			Chapter1 - Intro
107			Chapter2 -Background info of epitaxial growth
108			Chapter3 - Literature reviews
109			Chapter4 - Experimental methodology
110			Chapter5-Results
111			Chapter6-Conclusion and future work
112			**confrences**
113	✓		Attend the GREEN/ASSET II Annual meeting at Little Rock2013
114			summer15
115			Attend the GREEN/ASSET II Annual meeting at Little Rock2014
116			puplications
117			Submit all docmentation
118			Deadday
119			Graduation

Appendix F: Identification of All Software Used in Research and Thesis/Dissertation Generation

Computer #1:

Model Number: HP ENVY 14t-u000 Windows 8 Business Laptop PC

Serial Number: 5CD4386MS1

Location: 1764 North Leverett Ave. Fayetteville Arkansas 72703

Owner: Manal Aldawsari

Software #1:

Name: Microsoft Office 365-Student Version

Purchased by: Manal Aldawsari

Software #2:

Name: Origin Pro 2015 – Student Version

Purchased by: Manal Aldawsari

Computer #2:

Model Number: x86-64Full_14Sep2

Serial Number: Dell 1707FP

Location: ENRC

Owner: Department of Electrical Engineering

Software #3:

Name: Microsoft Office 2007

Purchased by: UA Department of Electrical Engineering

Appendix G: All Publications Published, Submitted and Planned

There are no publications published or submitted for this work.