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Experimental Verification and Integration of a Next Generation Smart Power Management System

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Experimental Verification and Integration of a Next Generation Smart Power Management System

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By

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ABSTRACT

With the increase in energy demand by the residential community in this country and the diminishing fossil fuel resources being used for electric energy production there is a need for a system to efficiently manage power within a residence. The Smart Green Power Node (SGPN) is a next generation energy management system that automates on-site energy production, storage, consumption, and grid usage to yield the most savings for both the utility and the consumer. Such a system automatically manages on-site distributed generation sources such as a PhotoVoltaic (PV) input and battery storage to curtail grid energy usage when the price is high. The SGPN high level control features an advanced modular algorithm that incorporates weather data for projected PV generation, battery health monitoring algorithms, user preferences for load prioritization within the home in case of an outage, Time of Use (ToU) grid power pricing, and status of on-site resources to intelligently schedule and manage power flow between the grid, loads, and the on-site resources.

The SGPN has a scalable, modular architecture such that it can be customized for user specific applications. This drove the topology for the SGPN which connects on-site resources at a low voltage DC microbus; a two stage bi-directional inverter/rectifier then couples the AC load and residential grid connect to on-site generation. The SGPN has been designed, built, and is undergoing testing. Hardware test results obtained are consistent with the design goals set and indicate that the SGPN is a viable system with recommended changes and future work.

ACKNOWLEDGMENTS

First and foremost special thanks are due to the academic advisor, Dr. Mantooth. He has been a constant guide and mentor schooling me to become a more technically sound engineer. His work ethic, vision, and constant leadership were an inspiration to accomplish my every goal. Without him, I could not have accomplished what I have. Thanks are also due to Dr. McCann and Dr. Balda for assistance and a source of technical expertise in various aspects of this project. The students, faculty, and staff at The University of South Carolina are owed a great debt of gratitude for their contributions to the other major half of this project. Special thanks are due to the project leader at USC, Dr. Roger Dougal. He has been a source of great organization and experience to rely on as us students pursued our education and developed this project.

I would like to specially thank my friend and colleague Brian Stalling for laying much of the research and design work before I became part of this project. No matter the issue or how big the problem he was always happy to assist and contribute. His help with fielding the late night "epiphanies" on how to make a breakthrough was instrumental in keeping motivation. I could not have done this without him. Finally, I would like to thank Chris Farnell, Yuzhi Zhang, Janviere Umuhoza, Fahad Hossain, and Haoyan Liu for their contributions to the SGPN V1 & V2, as well as the support with this project.

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CHAPTER 1

INTRODUCTION

1.1 Need for Residential Energy Management Systems

The steady increase in the price to produce electricity and efforts made to modernize the grid have led to an increasing focus on efficiency in power production and consumption. The primary fuel source in the United States for electricity generation is coal, making up 42%, followed by natural gas at 25% and nuclear at 19% [1]. According to American Electric Power (AEP), greenhouse gas legislation that is being introduced by the United States government will further restrict the amount of carbon emissions allowed which will affect energy prices due to increasing de-regulation of the electricity market [2]. This will ultimately add to an already capital intensive generation, transmission, and distribution process.

Renewable electricity sources such as Photovoltaic (PV) systems or wind generation offer attractive alternatives to using grid power. In addition to the "free cost" nature of these sources, they emit zero carbon emissions making them ideal for use at a residential setting.

Recently the "smart grid" initiative has established an interesting application for residential energy management systems and micro grids. With the increase in the price of electricity and the subjection of time-of-use pricing, a consumer should have the option to curtail usage of grid energy when the price is high. An intelligently automated energy management system would accomplish this goal with minimal to no user interaction. In addition, the development of "smart appliances" can be programmed to operate during low cost times and provide controllable loads in order to shift the load profile of the home to off peak times and even reduce energy consumption.

1.2 Current On-Site Electrical Generation Systems Available

Companies have started developing grid-connected systems that incorporate renewable sources and energy storage in anticipation of the "micro-grid" market. The focus on efficiency, decreasing cost of PE converters, and increasing capabilities in control and automation are driving the economic viability of smart energy management systems. This is applicable at not only the industrial level, but also commercial and residential. Solar inverters, energy storage, and grid-tied power electronics are becoming more prevalent given the decreasing cost. While typical energy management systems offered at the residential level do supplement grid power they do not offer much automation, customization, control, or "intelligent" operation.

Companies like Savant Systems [3] offer an energy monitoring system that allows the user to track energy usage and cost through their TrueControl^{TM} application via a mobile device or computer. Users can track individual loads through connections in the breaker panel, remotely dim lights, lower shades, and adjust the thermostat to conserve and control energy usage. The Savant Host Controller is the software package that "*control[s] all aspects of automation and control…* [4]" However, it mentions no explanation regarding what "automation" and "control" it is capable of performing. The SGPN was designed with the intention of a high level of automation performing various functions discussed in section 3.1.2.

In addition, the Savant system power supply requires a 100-200 V AC 50/60 Hz source [5]. Therefore if grid power is lost, the system will no longer be able to function. The SGPN was designed to operate on a 12 V DC voltage (a car battery) which is integral to the system. The system controller monitors the battery voltage to determine the level of discharge. If grid power is lost, the SGPN can still function in islanded operation. In fact, this is one of its features. It should be noted that there are cases where the battery storage will become severely discharged and the system must completely shut down (in the case of a cloudy day and an extended grid

outage for example). However, the architecture of the SGPN is such that the PV system can charge the batteries in islanded or grid-connected operation. Thus, there was some intentional redundancy designed into the hardware to reduce the exposure to unintentional shutdown.

Outback Power Systems have several complementary products that are geared for alternative energy production and consumption at the residential level. For example, Outback offers solar inverters, charge controllers, and integration platforms that allow for multiple products to be used in one application [6]. These products require frequent user interaction and do not address active control of home load profiles or on-site resources. The SGPN solution presents an integrated hardware/software package that can project load profiles, employs an artificial intelligence mechanism based on empirical load data to improve the predicted load profile (and therefore the battery use schedule), intelligently controls "smart" loads, and distributes on-site resources (battery and PV) in conjunction with the electric grid to yield energy savings for the consumer.

1.3 Benefits of Automated Energy Management

With the increased concern of C_O2 emissions causing an acceleration of negative climate change, there has been an increased focus on energy efficiency and particularly the generation profile of utilities. New EPA regulations have put strict requirements on all utilities to significantly reduce the amount of harmful emissions from existing and future fossil fuel source generation plants including reductions in arsenic, sulfur dioxide, NO_x, mercury, etc [7]. The 4 year timeline set forth by the EPA for hazardous pollutant reduction by coal and oil fired plants [7] is extremely ambitious. Coal fired plants generate the majority of "base-load" electricity in the United States. Often, the improvements that are required of legacy plants to comply with new regulations are more expensive than to build a new plant. Therefore utilities are forced to take action such as replacing coal plants with natural gas ones, which equate to about ½ the emissions

[8]. However, this pushes the generation profile more and more toward a “time of use” source. This move toward natural gas as the bulk electricity generation resource and the unstable nature (supply and price) of this fuel source puts the power reliability of the bulk electric system in jeopardy. In addition, the cost of the infrastructure required to build new power plants is generally passed on to consumers in the form of rate increases.

Renewable energy sources such as wind and solar, energy storage, and other forms of distributed generation allows the consumer to use a cheaper form or “no cost” form of energy generation. This can provide a way to help with grid stability, but the current paradigm of balancing generation with demand would need to be addressed. The issues associated with these types of local generation have an array of issues, but that analysis is beyond the scope of this thesis.

Automated energy management allows for user customization, cost/power resource optimization with pricing input from the utility provider, application specific preferences, and smart islanding techniques for independent operation. This yields cost savings for the consumer all with minimal human interaction. In addition the consumer would have the ability to monitor power consumption and remotely control loading throughout the home when away. In a wide-scale deployment this system can act as a peak shaving mechanism that could be beneficial for both the consumer and utility during peak demand times.

Having a smart device with communication capabilities could also allow the utility to obtain a very detailed – real-time status of the distribution system. Such a system could also provide active power factor control reducing losses on the system and improving power quality.

1.4 Thesis Organization

This thesis will be arranged as follows: Chapter 2 will present the relevant technical background required to understand the topics of control and hardware design for the integration

and testing of the SGPN. Chapter 3 will present the design and integration of the individual converters, control, as well as the full system operation. Chapter 4 will present the closed loop simulation results of the integrated hardware with the various operating modes of the SGPN. Chapter 5 will present closed loop individual converter and integrated hardware experimental results with discussion and analysis. Finally Chapter 6 will present the conclusions from the project and suggestions for improvements and future work.

CHAPTER 2

THEORETICAL BACKGROUND

This chapter presents the technical background necessary to understand the design and implementation of the work presented in this thesis. Given this was a continuation of a multi-year project, much of the background is referenced in the graduate theses of former students. The background for the system level controller developed by USC is detailed in [9] and [10]. Similarly, much of the control theory, switching converter theory, switching techniques, and device loss analysis are detailed in [11].

2.1 Electromagnetic Interference

ElectroMagnetic Interference (EMI) is a very broad and complex subject. A comprehensive discussion on the background is beyond the scope of this thesis. However, due to the effect on circuit performance seen through testing the prototype an overview of the causes and effects is presented here.

2.1.1 *EMI Overview*

DC-DC converters, especially boost converters have been known to generate a significant amount of EMI due to the pulsing nature of the input current [12]. EMI can either be radiated through some medium or conducted. Conducted EMI is dependent on the characteristics of the conductor it is propagating through. Similarly, the nature of radiated EMI depends on the medium in which it passes through.

There are many causes of EMI but the majority could be accounted for through parasitic inductance and capacitance, device switching, noise on power ground, PC board layout, and diode reverse recovery characteristics. Common mode EMI is caused by an electrical coupling (C dv/dt) from a parasitic capacitance to the ground reference. Differential mode EMI is an interaction through a magnetic coupling (L di/dt) from series parasitic inductors in board layouts,

inductive loops in device packages, etc [12]. Some of these can be compounded through interaction with each other such as parasitic inductance loops and noise on the power ground. Similarly many are related such as a poor PC board layout and the amount of parasitic elements in the circuit.

Parasitic inductance loops can be caused by a poor power board layout. For example, a thin, long current carrying trace will have a high parasitic inductance. Generally, it is a preferred practice to have short and planar traces to reduce this effect. Eq. $L_{trace} = 0.0002X\left[\ln\frac{2X}{(W+H)} + 0.2235\left(\frac{W+H}{X}\right) + 0.5\right]\mu H$ (2-1) shows the calculation of the inductance for a PC board trace where X is the length of the trace, W is the width of the trace, and H is the thickness of the conducting material [13]. A graphic illustrating the dimensions is shown below in Fig. 2.1.1.

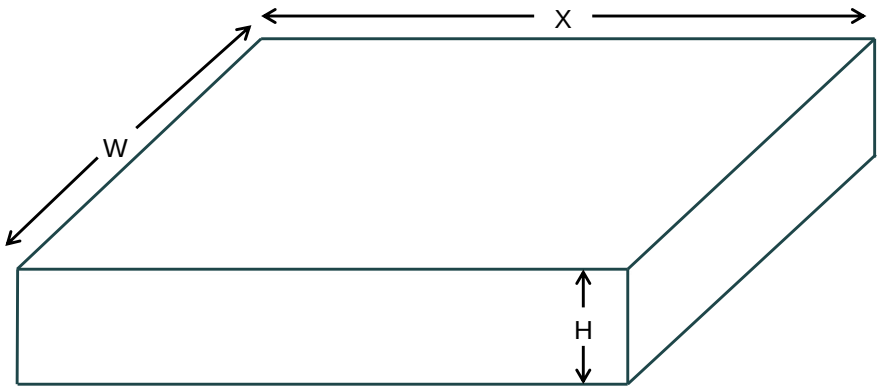

Fig. 2.1.1: 3D - PC Board Trace

$$L_{trace} = 0.0002X\left[\ln\frac{2X}{(W+H)} + 0.2235\left(\frac{W+H}{X}\right) + 0.5\right]\mu H \quad (2\text{-}1)$$

Even a small parasitic inductance can have a significant negative consequence on circuit performance especially in high frequency switching applications. Due to the "inductive kick" from interrupting current through an inductor, a voltage spike develops across any device at turn

off during hard switching. Given the governing equation of an inductor (Eq. $V_l = L_{par}\ \frac{d_i}{d_t}$ (2-2), it can be deduced that the higher the current the larger the voltage spike. Similarly, a faster switching frequency also increases the EMI conducted because it increases the $\frac{d_i}{d_t}$ seen by the device. By definition, the higher the interrupted current in the circuit, the higher the differential mode EMI. Therefore at high switching frequencies and high power levels, the susceptibility to EMI is much greater.

$$V_l = L_{par}\ \frac{d_i}{d_t} \tag{2-2}$$

$Cplate=0.0085\varepsilon RAd\ F$ (2-3) shows the equation for parasitic capacitance where εr is the dielectric constant of the insulating material in the PC board, A is the area of the plate, and d is the separation between the plates (which would be the thickness of the dielectric material) [13].

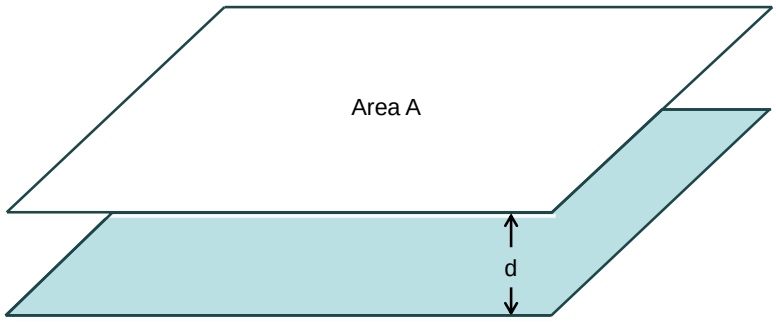

Fig. 2.1.2: Layer – Layer Coincident PC Board Traces

$$C_{plate} = 0.0085\varepsilon_R \left(\frac{A}{d}\right)\ F \tag{2-3}$$

Parasitic capacitance can develop between the "neutral" and the ground plane as well as inside the packaging of a device. Similarly, stray capacitance can be present on a current carrying trace to ground. A simple model with parasitic elements in a half bridge configuration is shown below in Fig. 2.1.3 for reference. Regarding PC boards, typically the capacitance developed with two traces crossing on adjacent planes is negligible. However, traces that run in

coincidence on different layers have non-negligible contributions to the parasitic capacitance of the board layout [13]. Parasitic capacitance can form between the ground plane and a trace because of this effect. This provides a path for high frequency noise to ground. Noise, meaning common mode currents flowing in the ground reference increases the EMI and degrades performance of the circuit.

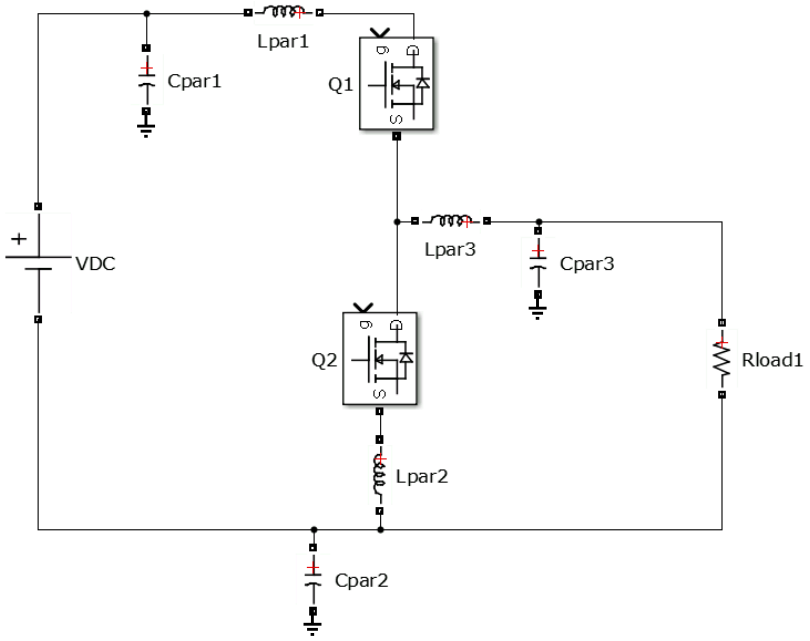

Fig. 2.1.3: Half Bridge Schematic Example with Parasitic Elements

The largest contributor to conducted EMI is the switching of a device. During device turn on, the slope of the current (I_{DS}) and voltage (V_{DS}) across the device is the rate of rise in current over time (di/dt) and rate of rise in voltage over time (dv/dt), respectively. This directly affects the amount of EMI conducted. Fig. 2.1.4 shows the graphical representation of a switch transition during hard switching.

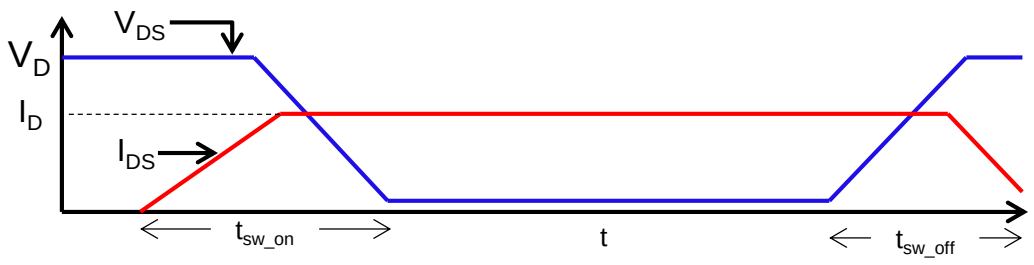

Fig. 2.1.4: Device Turn-on/off Voltage and Current Waveforms

There are methods that can reduce the circuit's susceptibility to EMI such as adding a gate resistance in series between the gate driver and the device. This slows the turn on and turn off time (the slope of current and voltage rise and fall), thus reducing the EMI. However, this increases the switching losses. An optimized board layout to minimize parasitic components is a way to avoid slowing device drive time and increasing losses through adding a gate resistor. Ultimately, a parasitic extraction must be done on board designs to be sure what mitigation techniques might be needed.

"Zero Voltage" or "Zero Current" switching are additional methods that use resonant tank circuits to force a switching transition to take place when there is no voltage across the device (ZVS) or no current running through the device (ZCS). This effectively reduces EMI since there is no dv/dt (V = 0 V) and no di/dt (I = 0 A) associated with the device. Ferrite cores can also be added to external cabling to reduce the effect of radiated EMI in sensitive circuits.

The slope of device voltage over time and slope of device current over time during switching transitions in a half bridge configuration are shown below in Eqs. $\left[\frac{dI_{DS}}{dt}\right]_{on} \approx g_m\left[\frac{V_{dd}-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}R_g}\right]$ (2-4), $\left[\frac{dI_{DS}}{dt}\right]_{off} \approx -g_m\left[\frac{V_{dd}-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}R_g}\right]$ (2-5), and $\left[\frac{dV_{DS}}{dt}\right] \approx \frac{i_g}{C_{rss}}$ (2-6), respectively [14]. These equations show the effect of a gate resistance, where it can be seen the larger this value the smaller the slope of current and voltage change.

$$\left[\frac{dI_{DS}}{dt}\right]_{on} \approx g_m\left[\frac{V_{dd}-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}R_g}\right] \tag{2-4}$$

$$\left[\frac{dI_{DS}}{dt}\right]_{off} \approx -g_m\left[\frac{V_{dd}-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}R_g}\right] \tag{2-5}$$

$$\left[\frac{dV_{DS}}{dt}\right] \approx \frac{i_g}{C_{rss}} \tag{2-6}$$

g_m is the transconductance of the device, V_{dd} is the gate voltage at turn off, V_{th} is the threshold voltage of the switching device, I_{DS} is the drain to source current, R_g is the gate resistance, and C_{iss} is the gate input capacitance for the above equations.

Switching transitions can also create ringing and oscillations within the circuit which is a source of conducted EMI. As an example, in a half bridge the energy stored in the parasitic capacitance and inductance of the circuit discharge during switching transitions. The resonance point created by the parasitic elements can cause an "LC" oscillation at extremely high frequencies (100 MHz – 200 MHz) [15]. The calculation of the resonance frequency is given by the simple equation of an LC filter, Eq. $f_{res} = \frac{1}{2\pi\sqrt{\sum L_{par}\sum C_{par}}}$ (2-7).

$$f_{res} = \frac{1}{2\pi\sqrt{\sum L_{par}\sum C_{par}}} \tag{2-7}$$

As mentioned above, an in depth discussion of all different causes, interactions, effects, and mitigation techniques of EMI is beyond the scope of this thesis. From this brief overview, it alludes to the extensive effect that interference can have in power electronic circuits. Given the potentially damaging effects, this is an important topic that should be considered when designing any switching power converter or power electronics system.

2.2 Radio Frequency Modulation/Demodulation

The background for RF modulation and demodulation is included because these principles are used in digital isolation. In general, modulation manipulates a signal with a carrier wave (usually at a much higher frequency) so that it may be "carried" across some medium such as a silicon isolation barrier, or even air. Demodulation is a method by which the information sent by the carrier wave is extracted once it reaches its destination.

With the advent of powerful digital processors modulation/demodulation can be accomplished through analog or digital means. Since the digital implementation tends to be more application specific, the background provided is the analog technique. The following sections will present the fundamentals between the different types of modulation and demodulation.

2.2.1 *Amplitude Modulation*

The fundamentals of amplitude modulation are relatively simple. The amplitude of a carrier wave is altered with respect to the message, or baseband signal. The carrier signal is usually chosen at a very high frequency because it is the most efficient means of transferring information long distances [16]. The waveforms associated with an amplitude modulated signal are shown below in Fig. 2.2.1. It can be seen the modulated signal has an "envelope" that appears similar in structure to the original message.

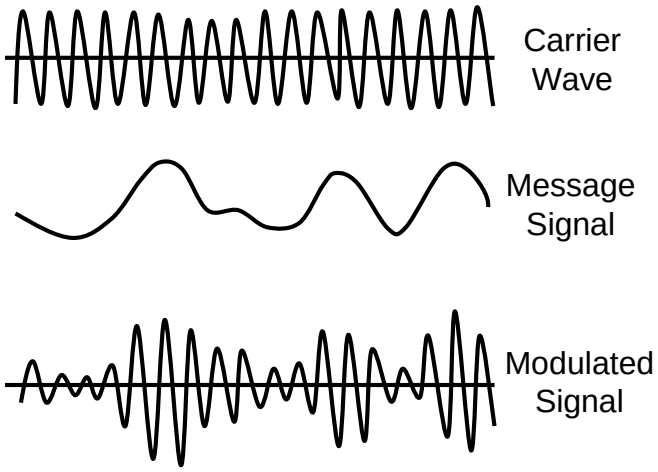

Fig. 2.2.1: AM Modulated Signals

Assuming a sinusoidal carrier wave, the signal can be described by eq. $c(t) = A_c sin(2\pi f_c t + \emptyset)$ (2-8) where A_c the amplitude of the carrier wave is, $\emptyset$ is a phase angle, and f_c is the carrier frequency:

$$c(t) = A_c sin(2\pi f_c t + \emptyset) \quad (2\text{-}8)$$

The amplitude is changed proportionally to the message the carrier wave is carrying. The message signal $m(t)$ is assumed as eq. $m(t) = M_b \cos(2\pi f_b t + \emptyset)$(2-9) where M_b is the amplitude of the baseband message and $f_b$is the baseband frequency [16].

$$m(t) = M_b \cos(2\pi f_b t + \emptyset) \quad (2\text{-}9)$$

To show the modulated signal, the carrier signal is summed with 1 and multiplied by the message signal (eq. $m_{bc}(t) = A_c\big(1 + m(t)\big)\cos(2\pi f_c t)$ (2-10)). From [16], the modulated signal $m_{bc}(t)$ can be represented as eq.$m_{bc}(t) = A_c \cos(2\pi f_c t) + \frac{M_b}{2}\cos(2\pi(f_c - f_b)t) + \frac{M_b}{2}\cos(2\pi(f_c + f_b)t)$ (2-11).

$$m_{bc}(t) = A_c\big(1 + m(t)\big)\cos(2\pi f_c t) \tag{2-10}$$

$$m_{bc}(t) = A_c\cos(2\pi f_c t) + \frac{M_b}{2}\cos(2\pi(f_c - f_b)t) + \frac{M_b}{2}\cos(2\pi(f_c + f_b)t) \tag{2-11}$$

2.2.2 *Frequency Modulation*

Frequency modulation transmits a baseband signal by changing the carrier wave frequency proportional to changes in the message. It is mostly used in television and radio broadcasts given the divisions of airwave frequencies [17]. The same message and carrier wave signals in section 2.2.1 are used here. The block diagram of the frequency modulation process is shown below in Fig. 2.2.2.

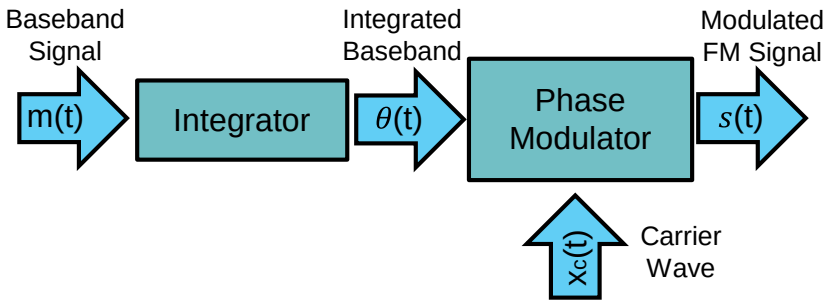

Fig. 2.2.2: FM Modulation Basic Block Diagram

In order to change the frequency of the carrier with respect to the changes in the message signal, the baseband must first be integrated with respect to time to get a function of phase that is proportional to the time varying message [17]. The second step is to superimpose the carrier wave on the phase representation of the original message. The output FM signal is then given by eq. $\theta(t) = 2\pi f_c t + 2\pi k_f \int_0^\tau m(\tau)d\tau$ (2-12) [17], where k_f is the frequency sensitivity.

$$\theta(t) = 2\pi f_c t + 2\pi k_f \int_0^\tau m(\tau)d\tau \tag{2-12}$$

The phase modulator block above consists of an "IQ" modulator, where "I" is the phase signal $\theta(t)$ and "Q" is the carrier wave. The modulator block itself consists of these two data fed into what is known as a mixer, where the "I" signal is compared with an oscillator. Similarly, the

"Q" signal is compared with an oscillator 90° out of phase. These two outputs are then summed together and amplified to yield the FM output signal [18]. The basic block diagram showing this operation is shown in Fig. 2.2.3.

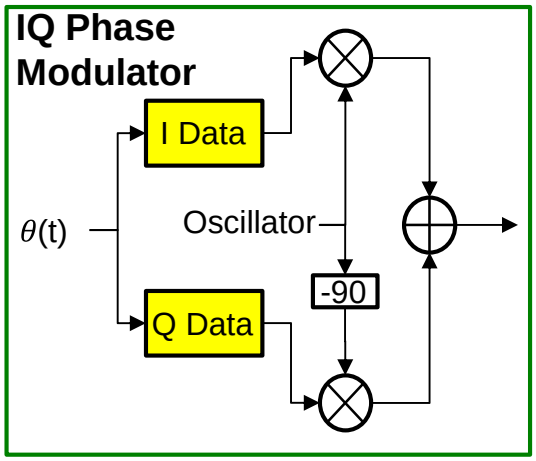

Fig. 2.2.3: IQ Phase Modulation Block Diagram

After this frequency modulator, the output FM signal is:

$$s(t) = Acos\left[2\pi f_c t + 2\pi k_f \int_0^\tau m(\tau)d\tau\right] = Acos\left[2\pi f_c t + 2\pi k_f \int_0^\tau Mcos(2\pi f_m \tau)d\tau\right] \quad (2\text{-}13)$$

The next step is to select the frequency modulation index. This is the ratio of the frequency variation from the carrier frequency over the carrier frequency. From [17], $\theta(t)$ can be simplified to eq. $\theta(t) = 2\pi f_c t + \frac{\Delta f}{f_m}\sin(2\pi f_m t) = 2\pi f_c t + \beta \sin(2\pi f_m t)$(2-14), where β is the modulation index.

$$\theta(t) = 2\pi f_c t + \frac{\Delta f}{f_m}\sin(2\pi f_m t) = 2\pi f_c t + \beta \sin(2\pi f_m t) \quad (2\text{-}14)$$

Finally, the final form of $s(t)$ can be obtained. Eq. $s(t) = Acos[2\pi f_c t + \beta\sin(2\pi f_m t)]$ (2-15) shows the final frequency modulated output equation.

$$s(t) = Acos[2\pi f_c t + \beta \sin(2\pi f_m t)] \quad (2\text{-}15)$$

2.2.3 *Amplitude Demodulation*

Demodulation is the technique of extracting the original message signal from a modulated one. There are 4 types of AM demodulation – envelope, coherent, square-law, and quadrature. Background on all techniques is beyond the scope of this thesis. Therefore only coherent AM demodulation is presented here.

The basic operation of coherent AM demodulation is to multiply the modulated signal by a local oscillator. The oscillator is generated by inputting the AM signal to a zero-crossing detector [19]. This allows for the carrier frequency to be accurately detected. A low pass filter is then used to filter out the high frequency carrier components leaving the original demodulated message. The block diagram illustrating AM demodulation is shown below in Fig. 2.2.4.

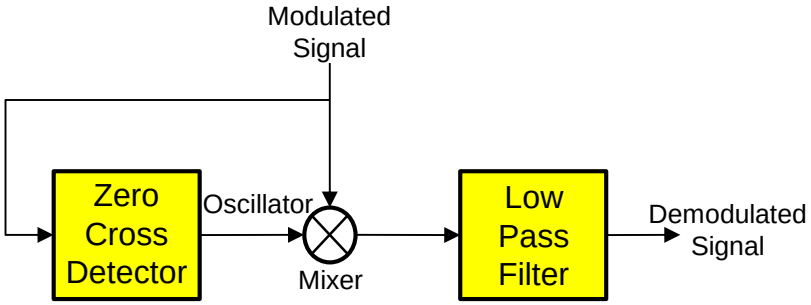

Fig. 2.2.4: Coherent AM Demodulation Block Diagram

Assuming a Dual Side Band (DSB) modulated signal, the output of the mixer after the local oscillator can be calculated. From [20], the output of the mixer is given by the following equation:

$$s(t) * x(t) = \frac{1}{2}m(t) + \frac{1}{2}A_c + \frac{1}{2}[m(t) + A_c]\cos(4\pi f_c t) \quad (2\text{-}16)$$

, where $s(t)$ is the modulated signal, $x(t)$ is the oscillator output, $m(t)$ is the original message, and f_c is the frequency of the carrier wave. $\frac{1}{2}A_c$ is the "DC" component of the signal,

while $\frac{1}{2}[m(t) + A_c]\cos(4\pi f_c t)$ is the high frequency component [20]. After passing through the low pass filter the HF component is eliminated leaving the demodulated signal, $\frac{1}{2}m(t)$. The demodulated output would then be scaled appropriately to give the original signal.

2.2.4 *Frequency Demodulation*

Frequency demodulation can be characterized by 3 main techniques – FM to AM conversion, zero-crossing, and quadrature demodulation. After a brief description of each, the zero-crossing technique is presented. FM to AM demodulation simply converts the FM signal to an AM signal then uses an AM demodulation technique to extract the message. Zero-crossing uses a detector to indicate a negative to positive zero-crossing and outputs a pulse train. This pulse train is dependent on the signal [20].

FM quadrature demodulation extracts the angle information from the modulated signal. The FM signal is passed through a mixer in which two oscillators (90° out of phase) at the carrier frequency are multiplied by the FM signal. The signals are then passed through separate low pass filters where the "Q" and "I" data are separated. After extracting the angle information from both data the demodulated signal is given by passing through a differentiator [20].

The basic block diagram of zero-crossing demodulation is shown below in Fig. 2.2.5.

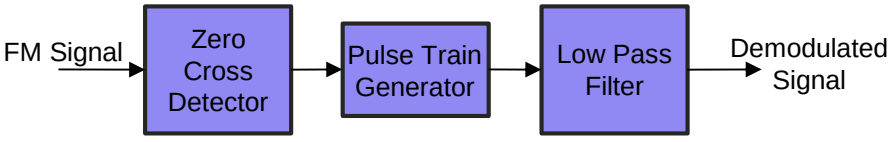

Fig. 2.2.5: Zero-Crossing FM Demodulation Block Diagram

After the zero crossing detection, the pulse generator converts that into a pulse train. Assume the instantaneous frequency of the FM signal is [20]:

$$f = f_c + \Delta f * m(t) \tag{2-17}$$

, where f_c is the carrier frequency and Δf is the maximum frequency deviation.

After passing through the low pass filter, the output is:

$$A * \frac{\tau}{T} = A\tau f_c + A\tau\Delta f * m(t) \tag{2-18}$$

, where A is the amplitude of the pulse train, τ is the width of the pulse train, and T is the inverse of the instantaneous frequency. The demodulated signal is then given by the equation below [20].

$$m(t) = A\tau\Delta f * m(t) \tag{2-19}$$

2.3 Object Oriented Programming Background

Object oriented programming is a hierarchical method of programming used to breakout complex programs into modules that are more intuitive to the programmer; This increases flexibility to suit the user's needs and is more efficient [21]. There are several ways to accomplish the same task through programming and there are philosophical discussions among programmers as to which are the best.

The background presented here is intended to give one methodology for developing a "clean" program and not to promote any particular programming style. OOP can be implemented in varying degrees of complexity and abstraction depending on the program purpose, size, intent, etc. The organization of this topic was taken from [21] which presents OOP as a design approach and a way to organize programs.

2.3.1 *Procedural Programming*

This paradigm is focused on processing; the programmer determines the process, and then finds the best algorithm to accomplish the task [21]. This method is focused primarily on types of arguments, passing arguments to functions, and using functions to manipulate data in an

efficient way [21]. Naturally, this involves creating pointer variables that reference the memory location of an object instead of a particular value. The memory location then holds the value.

Pointers can be beneficial when dealing with complex systems because they take up a smaller amount of "run-time" memory. For example, rather than directly manipulating a large data value (say a very large integer), the program can use a pointer to reference that variable holding the integer during operations and thus increase the efficiency and speed of the program. Pointers are very efficient at handling large amounts of data and dynamic memory location. In data structures such as linked lists, pointers can be used to add, delete, or insert data anywhere in the list [22]. However, with a static array for example, there would be no way to dynamically update the size of the array if the data ever grew beyond the original array size. It would have to be re-initialized each time the dataset grew beyond the allocated memory. This would be a very bad programming practice and not very practical.

2.3.2 *Modular Programming*

Modular programming builds on the concept of procedural programming by incorporating a set of related procedures and their data [21] into a single module. This technique can be used to take a low level function and use it in a hierarchical application. An example pseudo code is taken from [21] and used as an example below:

```
#include "Stack.h"
void main()
{
        Stack::push ('c');
        If(Stack:: pop () != 'c') error ("cannot perform operation")
}
```

In this implementation the definition of "Stack" is separately compiled and by using the "::" operation, the user main code is independent of the representation of "Stack". This file is simply "included" into the user's program. The operator functions "push" and "pop" are part of the definition of "Stack" and can be used to manipulate the stack for the purposes of the program. This is an example of how a module can be developed using the procedures of "push" or "pop".

2.3.3 *Data Abstraction*

Data abstraction takes another step up in the hierarchy for programs that are even more complex. It itself is an abstract concept in that a data type can be created from an existing module or by directly defining one (a user-defined type) [21]. For example, multiple stacks can be created from the module "Stack". There are many ways that a stack could be created, but it is not important how if the interface to the user is the same [21]. A simple example is adopted from [21] and shown below:

```
#include "Stack.h"
void main()
{
        Stack :: stack s1 = Stack :: create ();
        Stack :: stack s2 = Stack :: create ();

        Stack :: push (s1, 'c')
        Stack :: push (s2, 'k')
}
```

Here, the implementation of "stack" is a representation of the type "Stack". By using the "::" operation definition detail is hidden from the user, but now the variables "s1" and "s2" are separate stacks that can be manipulated within the main program.

There is much more detail regarding higher levels of hierarchy, implementation techniques, type definitions, issues with certain approaches, program structure, etc. that could be presented. However, as mentioned, this can easily develop into a philosophical discussion about best practices or preferred approaches which is not the purpose of this material. The above sections provided an overview on how to modularize a program so a programmer can easily make modifications or additions. This avoids confusion for future expansion without sacrificing the existing functionality and provides an efficient means for constructing a complex program.

2.4 Inrush Current From Bulk Capacitance in Circuit

The study of the sudden charging of bulk capacitance is of interest due to the potentially damaging inrush currents that can be experienced in switching DC-DC converters. At startup of the SGPN, the capacitive elements used for DC voltage stabilization may or may not have a pre-charge. The smaller the charge, the larger the dv/dt applied to them. Thus the worst inrush currents would be experienced from a completely discharged circuit.

The step response of a series RLC circuit exhibits this behavior of the inrush current. The schematic for this circuit is shown below in Fig. 2.4.1. The value R represents the combined ESR for the input inductor, capacitance, and the "ON" resistance of the power electronic devices. L is the value of the input inductance of the PV boost converter. Parasitic inductance is assumed to be 0 H since $\gg L_{parasitic}$. Finally, the value of C is the output capacitance of the PV boost converter and equivalent capacitance seen from the HV DC link at the LV DC link. It should be

noted that the current will decay exponentially at a rate equal to the RC resonance. However, the current spike experienced can damage or destroy switching devices.

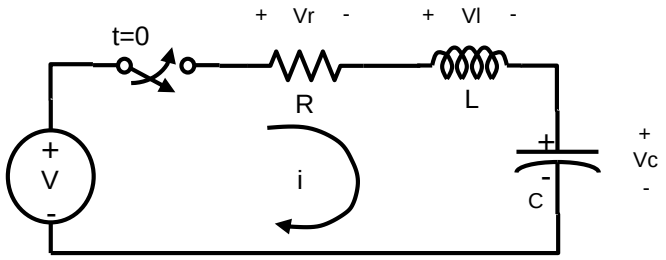

Fig. 2.4.1: Series RLC Circuit

At time t=0 s the switch to the circuit is closed. It is assumed that there is no energy in the circuit prior to this switching transition. Summing the voltages around the loop yields the following equation:

$$V = Ri + L\frac{di}{dt} + v_c \tag{2-20}$$

In order to get a convenient form of the equation, it is recognized that $i_c = C\frac{dv_c}{dt}$ and therefore $\frac{di}{dt} = C\frac{dv^2}{dt^2}$ [23]. After some algebraic manipulation the following equation is obtained for the circuit:

$$\frac{V}{LC} = \frac{v_c}{LC} + \frac{R}{L}\frac{dv_c}{dt} + \frac{d^2v_c}{dt^2} \tag{2-21}$$

$$\frac{V}{LC} = \frac{v_c}{LC} + \frac{R}{L}s + s^2 \tag{2-22}$$

The form of eq. $\frac{V}{LC} = \frac{v_c}{LC} + \frac{R}{L}\frac{dv_c}{dt} + \frac{d^2v_c}{dt^2}$ (2-21) is identical to the step response of a parallel RLC circuit in which the inductor current was solved [23]. From inspection, the current running through the inductor (at startup) is the same current flowing into the capacitor. This is shown in eq. $\frac{I}{LC} = \frac{i_l}{LC} + \frac{1}{RC}\frac{di_l}{dt} + \frac{d^2i_l}{dt^2} = \frac{i_l}{LC} + \frac{1}{RC}s + s^2$ (2-23) below.

$$\frac{I}{LC} = \frac{i_l}{LC} + \frac{1}{RC}\frac{di_l}{dt} + \frac{d^2 i_l}{dt^2} = \frac{i_l}{LC} + \frac{1}{RC}s + s^2 \quad (2\text{-}23)$$

Since both equations are of the same form, the analysis for finding the inrush current of a series RLC circuit is then similar in structure to the step response of a parallel RLC circuit [23]. As stated above $i_c = C\frac{dv_c}{dt}$ and then $v_c = \frac{1}{C}\int i_l d\tau$. By plugging these two equations into eq. $\frac{V}{LC} = \frac{v_c}{LC} + \frac{R}{L}\frac{dv_c}{dt} + \frac{d^2 v_c}{dt^2}$ (2-21), one gets:

$$V = Ri_l + L\frac{di_l}{dt} + \frac{1}{C}\int i_l d\tau \quad (2\text{-}24)$$

$il + Ldildt + 1Cild\tau$ (2-24) is differentiated with respect to i_l and rearranged to obtain the following equation:

$$0 = LC\frac{d^2 i_l}{dt^2} + RC\frac{di_l}{dt} + i_l \quad (2\text{-}25)$$

The response is assumed to be underdamped since the resistance of the circuit is very small. From [23], it is known the current response of an underdamped system is of the form eq. $i(t) = B_1 e^{-\alpha t}\cos\omega_o t + B_2 e^{-\alpha t}\sin\omega_o t$ (2-26) where α is the neper frequency and ω_o is the resonant frequency of the LC circuit. B_1 and B_2 are numerical values solved from initial conditions.

$$i(t) = B_1 e^{-\alpha t}\cos\omega_o t + B_2 e^{-\alpha t}\sin\omega_o t \quad (2\text{-}26)$$

The first step in solving for the inrush current is calculating the roots of the characteristic equation which are given in eq. $s_{1,2} = \frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} = -\alpha \pm \sqrt{\alpha^2 - {\omega_o}^2}$ (2-27).

$$s_{1,2} = \frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} = -\alpha \pm \sqrt{\alpha^2 - {\omega_o}^2} \quad (2\text{-}27)$$

Finally, given the circuit parameters and initial conditions, the full current response in terms of time will be had. Then, the current at t_0^+ can be calculated for the system.

2.5 Macromodeling

The concept of macromodeling is an adaption from integrated circuits in which complex systems are represented as a much simpler circuit that has similar behavior. The complexity of the model is dependent on the level of detail needed which gives the designer flexibility. The exact electrical description of the complex system is represented as an analog behavioral model [24]. The model can be adjusted to reflect the desired circuit behavior.

For example, the behavior of a transformer (as part of a much larger system) can be modeled as a constant gain block equal to the turns ratio if the voltage transformation in the circuit is of consequence but the detailed operation of the transformer is not. In this way, a 3rd order equivalent circuit that represents the magnetization parameters and leakage parameters is reduced to a "zero-th" order model.

In the context of a boost controller design, for the schematic shown in Fig. 2.5.1, the effective output capacitance seen by the boost converter includes its output capacitor and the capacitance at the output of the dual FB DC-DC converter. Obviously, the impedance of the second capacitor as seen from the primary side of the transformer is different than the secondary. The behavior of the overall circuit (the voltage transformation and reflected impedances) that affects the model needed for the boost controller is then accounted for. However, the full physical model that includes switching detail of the second stage and transformer dynamics is ignored. In this way, complex circuits can be reduced to reflect the circuit behavior. This approach of macromodeling has been proven to be robust and accurate while reducing complexity and saving time [24].

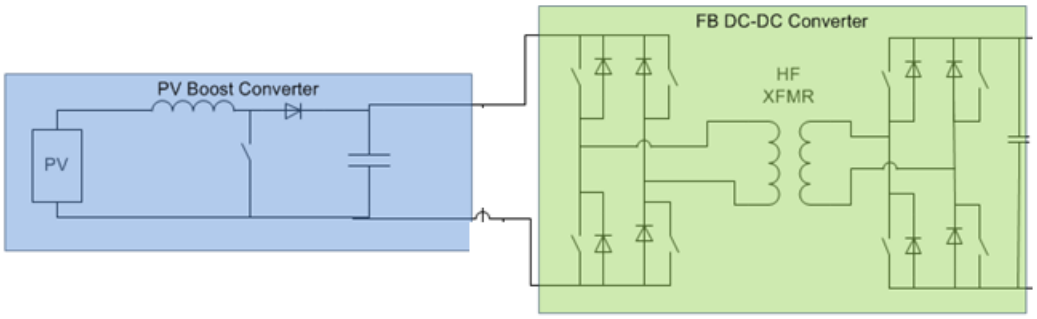

Fig. 2.5.1: PV Boost & Dual FB DC-DC Converter Schematic

Macromodeling in the context of integrated circuits generally involves some level of "equation – level" modeling depending on the circuit behavior desired [24]. This is analogous to the situation described above in that the boost converter is modeled by the state space averaged equations that represent the detailed operation of the circuit. The macromodel of the "load converter" and passive elements is then included to represent the behavior of the overall circuit.

As mentioned, the circuit behavior dictates the structure, detail, and content of the model. Therefore by nature, the models change. In system level power electronics design, a common need for modeling the full circuit is driven by the development of feedback control for a converter. The topology of the SGPN is configurable and therefore the operating mode being considered can affect the behavioral model associated with it. The background given here is an example of how to break down a complex circuit and retain the overall circuit behavior while maintaining the detail needed for an individual converter. The methodology applies to every circuit, but the details might change depending on the circuit configuration.

2.6 Transformer Background

Transformers are primarily used for an easy and robust way to either transform from a higher to a lower voltage (step down) or from a lower to a higher voltage (step up). Transformers also provide electrical isolation between the primary and secondary which can be beneficial for

safety reasons, but also for achieving performance objectives (e.g. “trapping” triplen harmonics in the delta winding). The fundamentals of ideal transformer theory are presented here to understand simple calculations needed to reflect impedances and voltages.

2.6.1 *Ideal Transformer Calculations*

The idealized schematic of a transformer is shown below in Fig. 2.6.1. The so-called “dot convention” indicates the current flows into and out of each respective winding. This also denotes the polarity of the transformer. Each transformer has conductive windings (usually copper) wrapped around a ferrite core on both the primary and secondary where the number of turns is designated by N_p and N_s, respectively [25].

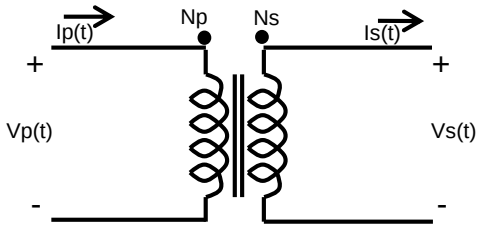

Fig. 2.6.1: Ideal Transformer Equivalent Circuit

The voltage relationship of the transformer is given as $\frac{V_p(t)}{V_s(t)} = \frac{N_p}{N_s} = N$, where N is the turns ratio of the transformer. For the purposes of calculating transformed voltages, currents, and impedances, the power losses inside the transformer can be assumed negligible. Obviously, in a real world application there would be some percentage loss to the windings, core, and magnetization currents. The power through the transformer is then, $N_p i_p(t) = N_s i_s(t)$. From this relationship the transformed currents can be calculated [25]. This is given in eq. $\frac{N_p}{N_s} = \frac{i_s(t)}{i_p(t)} = N$ (2-28) below:

$$\frac{N_p}{N_s} = \frac{i_s(t)}{i_p(t)} = N \tag{2-28}$$

Given the voltage properties of a transformer, the effective impedance value connected to a secondary will be different as seen from the primary. Given the equations above, the current or voltage can be calculated on either side of the transformer. Then from [25], the following expressions are given for impedance calculations where Z_L is the transformer load impedance and Z_L' is the reflected load impedance to the primary.

$$Z_L = \frac{V_s}{I_s} \tag{2-29}$$

$$Z_L' = \frac{\frac{N}{V_p}}{N * I_p} = \frac{V_p}{I_p} \tag{2-30}$$

$$Z_L' = \frac{V_p}{I_p} = \frac{NV_s}{\frac{I_s}{N}} = N^2 \frac{V_s}{I_s} = N^2 Z_L \tag{2-31}$$

The magnitude of this impedance changes based on the type of circuit element that is being considered. Therefore, all reactive elements should be treated as a reactance instead of a capacitance or inductance when doing impedance reflections. Reflecting a resistance is straightforward because it is not dependent on frequency, where capacitors and inductors do.

2.7 Low Frequency Ripple Induced on DC System from a Single-Phase Inverter

This section presents the background for the low frequency harmonics induced on the DC system due to the operation of the uni-polar SPWM H-bridge inverter. The overview of single phase inverters and uni-polar switching is detailed in [11]. The basic uni-polar switching operation is reviewed here in order to give a complete reference. Fig. 2.7.1 shows the schematic of an H-bridge inverter.

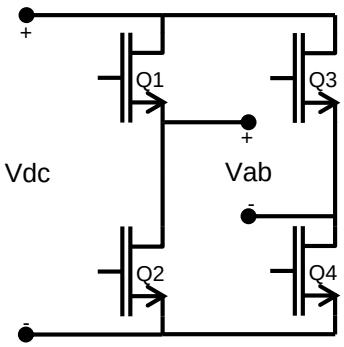

Fig. 2.7.1: H-bridge Configuration Schematic

Uni-polar switching uses two sinusoidal control waveforms that are 180° out of phase ($V_{control}$ and $-V_{control}$) with each other compared with a triangle carrier waveform (V_{tri}). The carrier waveforms are set to the period of the switching frequency, while the control waveforms are set to the desired output frequency [26]. The PWM generation waveform is shown below in Fig. 2.7.2.

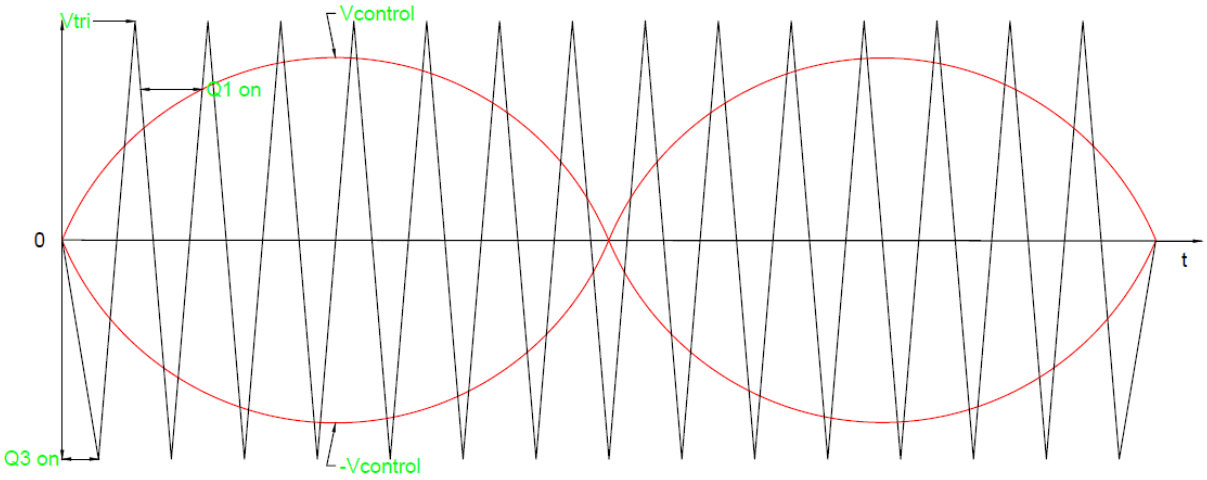

Fig. 2.7.2: Uni-polar SPWM Generation Waveform

The switching state is determined by whether the value of the control voltage is above the carrier waveform or below it. The devices are switched as diagonal pairs where Q1/Q4 is pair "A" and Q2/Q3 is pair "B". From [26], the summary of the switching table is given below in Table 2.7.1.

Table 2.7.1: Uni-polar SPWM Device Switching Table

Uni-Polar Switching Table		
Status	**Switch**	**Voltage (Va_)**
Vcontrol > Vtri	Q1	Vdc
Vcontrol < Vtri	Q2	0
-Vcontrol > Vtri	Q3	Vdc
-Vcontrol < Vtri	Q4	0

In order to simplify analysis of the 2nd harmonic induced on the DC side of the inverter, some assumptions are made. The switching frequency of the converter is assumed to be sufficiently high such that the high frequency switching ripple on the inverter output is negligible. This has a caveat that the AC filter elements then get smaller. Since the filter elements are considered very small, the energy stored in them is also very small [26]. Finally, the DC input is assumed to be ideal.

With these assumptions, the output AC waveform is an ideal sine wave, where v_{01} the fundamental is output voltage and ω_1 is the fundamental frequency:

$$v_{01} = v_0 = \sqrt{2}V_o \sin(\omega_1 t) \tag{2-32}$$

It follows that for a SPWM inverter, the output current would also be sinusoidal. This expression is given below in eq. $i_0 = \sqrt{2}I_o \sin(\omega_1 t - \emptyset)$ (2-33) where $\emptyset$ is the phase angle that the inverter current lags the voltage.

$$i_0 = \sqrt{2}I_o \sin(\omega_1 t - \emptyset) \tag{2-33}$$

All losses in filter elements and the inverter itself are considered to be zero for simplicity. Equating input and output power, eq. $V_d i_d^*(t) = v_o(t) i_o(t) = \sqrt{2}V_o \sin(\omega_1 t) * \sqrt{2}I_o \sin(\omega_1 t - \emptyset)$ (2-34) is obtained [26].

$$V_d i_d^*(t) = v_o(t) i_o(t) = \sqrt{2} V_o \sin(\omega_1 t) * \sqrt{2} I_o \sin(\omega_1 t - \emptyset) \quad (2\text{-}34)$$

The DC current $i_d^*(t)$ consists of a DC portion I_d and a low frequency component i_d^*. Solving for $i_d^*(t) = I_d + i_{d2}$, one obtains eq. $i_d^*(t) = I_d + i_{d2} = \frac{V_o I_o}{V_d} \cos(\emptyset) - \cos(2\omega_1 t - \emptyset) = I_d - \sqrt{2} I_{d2} \cos(2\omega_1 t - \emptyset)$ (2-35) [26]:

$$i_d^*(t) = I_d + i_{d2} = \frac{V_o I_o}{V_d} \cos(\emptyset) - \cos(2\omega_1 t - \emptyset) = I_d - \sqrt{2} I_{d2} \cos(2\omega_1 t - \emptyset) \quad (2\text{-}35)$$

,where V_d is the DC input voltage and I_{d2} is the magnitude of the 2nd harmonic current induced on the DC side. It follows then that [26],

$$I_d = \frac{V_o I_o}{V_d} \cos(\emptyset) \quad (2\text{-}36)$$

$$I_{d2} = \frac{1}{\sqrt{2}} \frac{V_o I_o}{V_d} \quad (2\text{-}37)$$

It can be seen the ripple portion of the DC side current is directly proportional to the output power served by the inverter. That is, the higher the power, the higher the ripple current. Without mitigation, this could cause mis-operation of the inverter. In practical situations, the DC voltage is not actually constant, so this ripple effect causes the same harmonic to be present on the voltage as well.

CHAPTER 3

HARDWARE AND CONVERTER CONTROL DESIGN

This chapter presents the design of the SGPN hardware and control at the system level, fully integrated level, sub-integrated level, and converter level. Most of the designs for the individual converters, individual converter controls, individual converter modeling, house power supply, sensing networks, and gate drive were detailed in [11]. These designs are integral to the continuation and success of the project, but are mostly beyond the scope of this thesis. It is recognized that there are many design fundamentals required, but some are referenced with the relevant topics explained and results stated. The designs presented are focused on the integration of tested hardware and the challenges encountered.

3.1 SGPN System Level Formulation

The SGPN system was originally proposed due to the interest and penetration of distributed generation systems, benefit(s) of active demand side management, and intelligent automation. This was brought about not only by the rising costs of electricity, but also the economic benefits of alternatives to grid energy. The SGPN is designed to incorporate 2- way communications with the utility, PV generation, energy storage, AC sources, demand side management, and intelligent automation in conjunction with the electric grid to power the home.

The SGPN system can be considered as two distinct layers with a software interface. “Layer 1” is the hardware operation and switching control. “Layer 2” is the high level system control algorithm which makes high level decisions based on available inputs, pricing structures, load profile, etc. The interface would be the data transmitted between layers 1 and 2 including system status (voltages and currents), load data, system level decisions on power flow/contribution, weather data, user preferences, etc. The following sections will present the topics related to the design and operation of the SGPN.

3.1.1 *SGPN Hardware and Hardware Control*

The basic SGPN hardware topology, control interface, and connection to loads within the home is shown below in Fig. 3.1.1.

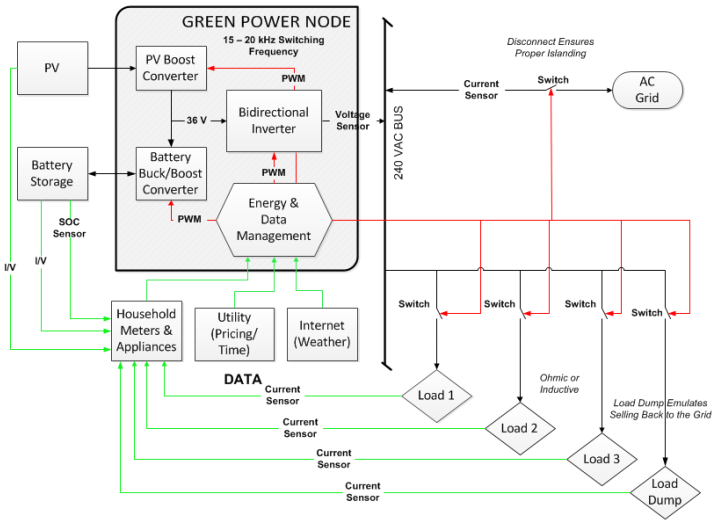

Fig. 3.1.1: SGPN Basic Functional Block Diagram

In order to be widely marketable the SGPN was designed to accommodate many user specific applications. It is realized that many residential users will have a variety of types, access, and investment in different on-site resources. In addition, there is a wide array of voltages that could be used as inputs based on the type and configuration of DC resources. Therefore, modular converters were designed to couple at a 36 V low voltage DC microbus that can accept input voltages from 12-36 V – thus a wide array of resources and resource configurations can be used. DC-DC converters are used to transform voltages to the appropriate level of the 36 V DC microbus and vice versa (for battery charging). For this prototype, a uni-directional PV boost converter and a bi-directional battery charge/discharge converter were designed. These topologies are universal and could be used with virtually any DC resource.

The central bi-directional inverter/rectifier is a two stage converter used to connect the low voltage DC microbus to the 240 V AC bus. The first stage is a “transformerized” dual full

bridge DC-DC converter which, in DC-AC power flow boosts the LV DC microbus to the HV DC bus, and in AC- DC power flow, the high voltage DC bus is “bucked” to lower voltages (used for battery charging from the grid). The second stage is an H-bridge inverter used to transform the HV DC link voltage to 240 V AC. Additionally, the SGPN is configurable through the system level and hardware controllers. Table 3.1.1 summarizes the different operating modes achievable with the SGPN topology illustrating its flexibility in operation.

Table 3.1.1: SGPN Operating Modes

SGPN Operating Mode Summary	
Islanded Operation	**Grid-Connected Operation**
PV only serving home load	PV and grid serving home load
Battery only serving home load	Battery and grid only serving home load
PV and battery serving home load	PV, battery, and grid all serving home load
	PV charging battery and grid serving home load
	PV/battery energy sold to grid

The hardware schematic of the SGPN is shown below in Fig. 3.1.2. It interfaces directly with the single phase, 3 wire AC bus in a typical US residence (neutral not shown). It features a disconnect switch such that in the case of a grid outage, it will detect the outage and safely island itself from the grid to prevent back-feeding of the residential feeder. Once the system is islanded, it performs load shedding and acts as an independent power supply to the home for as long as on-site resources allow. Additionally, through the AC bus, an AC generator could be connected. The topology of the SGPN is designed for this capability (again, for flexibility), but experimental

verification is beyond the scope of this prototype and this thesis. See CHAPTER 6 for further comments.

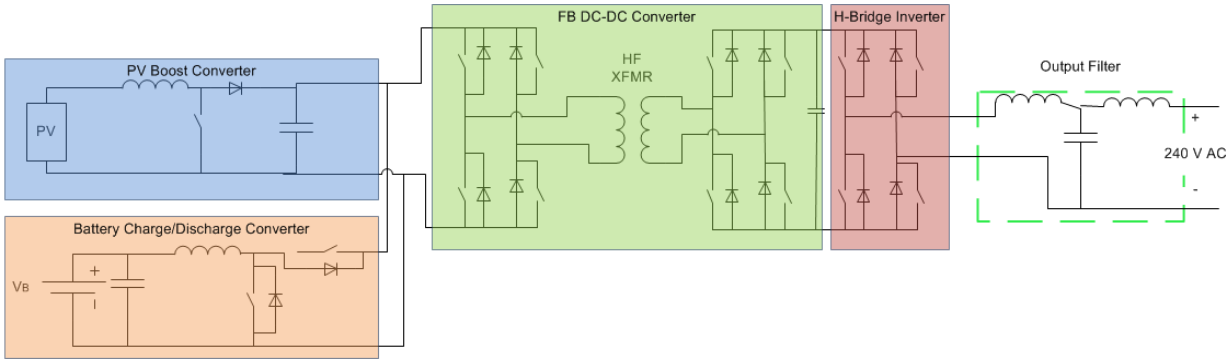

Fig. 3.1.2: SGPN Hardware Topology Schematic

The SGPN also features hardware control modules that produce PWM waveforms for individual switches to achieve voltage regulation and control power flow through the SGPN. Measured signals are communicated to the system level controller for hardware status information, real time power flow, and high level decision making. See [11] for details about the hardware control structure and design.

3.1.2 *System Level Control and Operation*

This section introduces the high level system controller operation and interface with the hardware and switching control layer. In order to facilitate this discussion, the detailed block diagram of the SGPN is shown in Fig. 3.1.3. A sophisticated system level control algorithm (developed by USC) processes and responds to multiple data inputs in order to dispatch the available resources to the home load in conjunction with the electric grid.

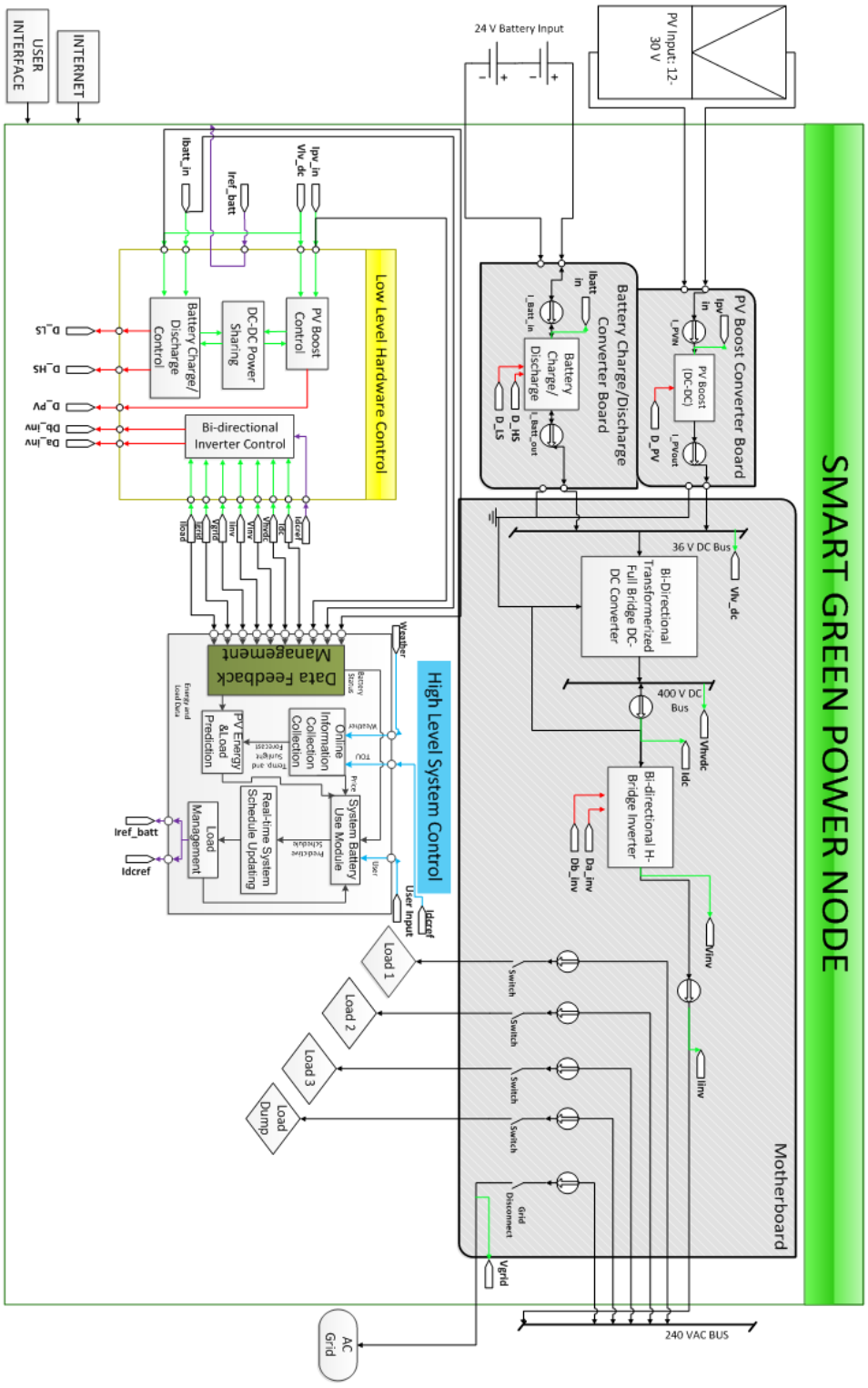

Fig. 3.1.3: SGPN Detailed Functional Block Diagram

Individual loads are monitored and managed automatically, but the home owner may prioritize loads based on importance and usage. Hardware status, energy usage, and on-site generation information is reported from layer 1 to layer 2 via the software interface. Weather data from an internet connection is used in order to project the power output from the PV panels. This information, in addition to the SOC/SOH of the battery, is used in order to calculate an optimized battery use schedule for a given 24 hour period. A particle swarm optimization algorithm is used to calculate the battery schedule producing a net cost savings [10] that is then easily calculated.

With the amount of data collected (as alluded to by user preference settings) a Human Machine Interface (HMI) showing efficiency, cost savings, grid energy price, home power demand, individual load power demand, and a settings page where the home owner can set/prioritize loads is incorporated. This would be useful to show the consumer real-time data that would otherwise be unavailable. This will be discussed in CHAPTER 6 .

Two-way communications between the utility and SGPN is a feature where a TOU rate structure can be sent to the home. Load information can be sent to the electricity provider thereby providing a real-time load profile of the distribution system in a wide scale deployment. This can be useful in not only localizing outages, but also diagnosing potential power quality issues.

The utility can request curtailment of grid energy during peak times through this communication platform. The SGPN uses on-site resources and load shedding techniques to comply with this request (if possible) in return for some type of rate incentive or other compensation. Additionally, the SGPN can be requested to push energy back on the grid during peak times receiving some similar type of monetary incentive. This automation of energy

management can optimize the load profile of the home to benefit both the home owner and utility economically, but also reduce the strain on the grid by acting as a peak shaving mechanism.

3.2 Phase Shifted PWM Generation Design

This section discusses the reason for a change in the switching scheme for the FB DC-DC converter. This was a necessary step in the continuation of the prototype testing as suggested in [11].

3.2.1 *Design Issue*

Originally a bipolar switching scheme was chosen for the full bridge DC-DC converter in which diagonal devices are paired and switched simultaneously (on the primary and secondary side of the transformer). Theoretically one could control the duty cycle to the respective high and low voltage H-bridge devices and therefore the output DC voltage. Fig. 3.2.1 shows the conventional PWM waveforms associated with the full bridge.

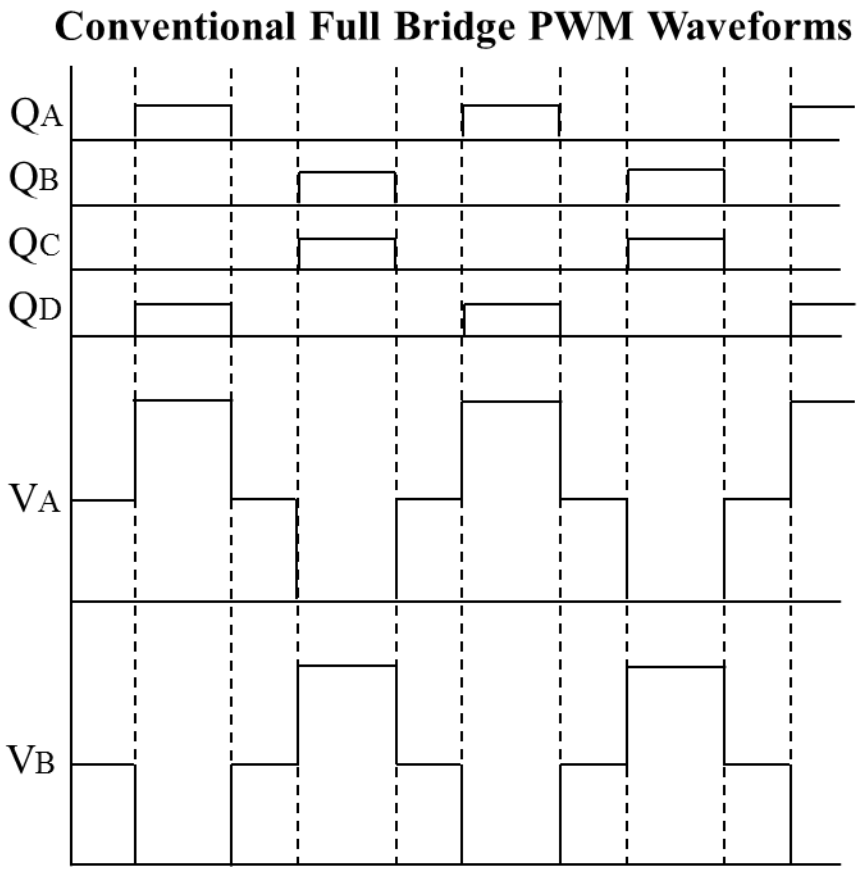

Fig. 3.2.1: Bi-polar FB DC-DC Converter Switching Waveforms

As discussed in [11], during the initial testing phases of the SGPN hardware, there was an issue discovered with the full-bridge DC-DC converter. For a very small load power, the duty cycle that was applied across the transformer did not "obey" the programmed value. This in turn affects the output DC voltage. An inability to control the DC input to the inverter could not only affect the AC output of the SGPN, but could also be destructive to the hardware itself.

With the original switching scheme, extending the dead time between switching legs had almost no effect on the duty cycle across the transformer. After extensive analysis it was determined that at low power the load cannot dissipate the current flowing through the transformer during the off time of Q_A/Q_D. The anti-parallel diodes continue to conduct this

current before the on time of Q_B/Q_C. Hence, there is still a voltage across the transformer. The result is an inability to control the duty cycle.

3.2.2 *Phase Shifted PWM Design*

As reported in [27] the absolute maximum rating of the high voltage devices is 500 V, but it is recommended to operate at no higher than 450 V. This allows for an overvoltage during switching transitions because of the loop inductance internal to the IGBT module. For safety and reliability of operation, an additional de-rating factor of at least 15 - 20% is needed. The schematic for the FB DC-DC converter is shown below in Fig. 3.2.2.

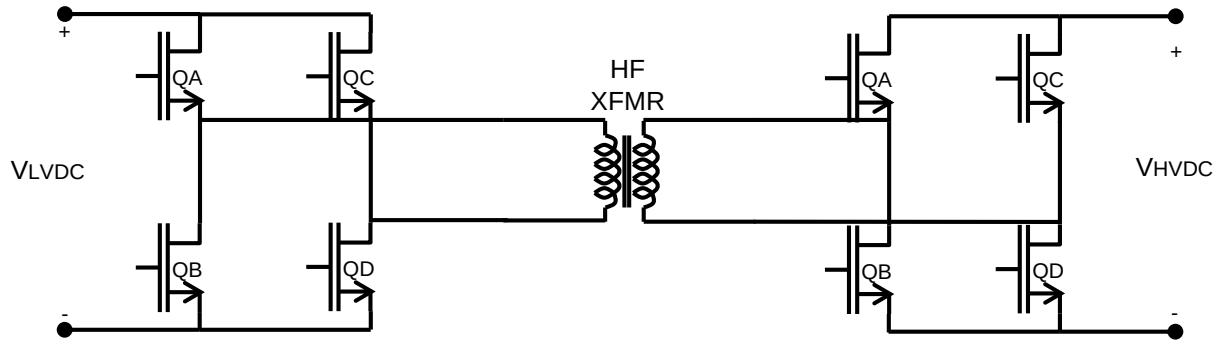

Fig. 3.2.2: Dual FB DC-DC Converter Schematic

The equation for the high voltage output of the full-bridge converter is given in $V_{HVDC} = 2\left(\frac{N_2}{N_1}\right) DV_{LVDC} = 2(13.7)(0.45)(36\,V) \approx 448\,V$ (3-1). The potentially damaging voltage level can be seen from this calculation.

$$V_{HVDC} = 2\left(\frac{N_2}{N_1}\right) DV_{LVDC} = 2(13.7)(0.45)(36\,V) \approx 448\,V \quad (3\text{-}1)$$

Given these problems, a phase shifted PWM switching scheme was implemented for the full bridge. This allows a direct control of the duty cycle applied across the transformer. The dead time is controlled by turning on either the two high side or two low side devices together. A TI application note [28] that shows the operation principles and design of a phase shifted control

was used as a guide to design the switching scheme for the full bridge. The switching waveforms are shown below in Fig. 3.2.3.

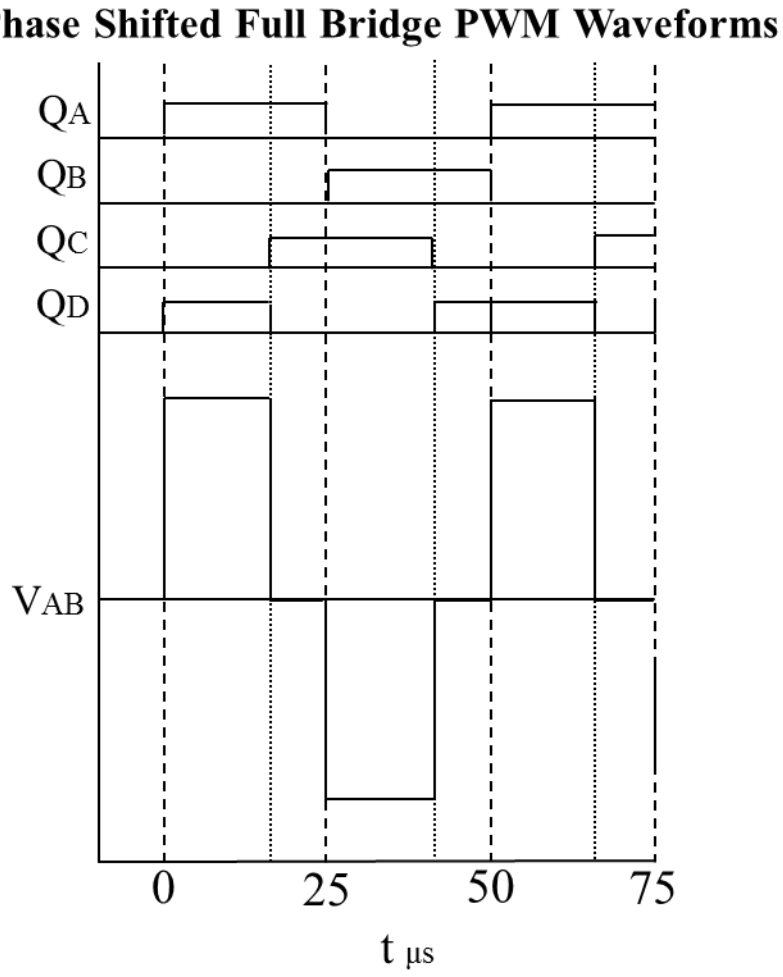

Fig. 3.2.3: Phase-shifted Dual FB DC-DC Converter Switching Waveforms

The behavior of the full bridge converter is identical between bi-polar switching and phase-shifted switching. D_{xfmr}, or the duty cycle that is applied to the transformer, is now determined by the phase shift between certain switches. Eq. $\phi_{sw,QC} = (D_{xfmr} * T_s) = (0.355 * 50\mu s) = 17.75\ \mu s$ (3-4) shows the relationship of the phase shift between switches, $D_{xfmr} * T_s$ is the phase shift term that implements the correct duty cycle, and from $V_{HVDC} =$

$2\left(\frac{N_2}{N_1}\right) D_{xfmr} V_{LVDC} = 2(13.7)(0.355)(36\,V) \approx 350\,V$ (3-6) the corrected minimum HV DC link voltage is calculated.

$$\phi_{sw,QA} = 0 \tag{3-2}$$

$$\phi_{sw,QB} = (0.5 * T_s) = (0.5 * 50\,\mu s) = 25\,\mu s \tag{3-3}$$

$$\phi_{sw,QC} = (D_{xfmr} * T_s) = (0.355 * 50\mu s) = 17.75\,\mu s \tag{3-4}$$

$$\phi_{sw,QD} = \left(D_{xfmr} * T_s\right) + (0.5 * T_s) = (0.355 * 50\,\mu s) + (0.5 * T_s) = 42.75\,\mu s \tag{3-5}$$

$$V_{HVDC} = 2\left(\frac{N_2}{N_1}\right) D_{xfmr} V_{LVDC} = 2(13.7)(0.355)(36\,V) \approx 350\,V \tag{3-6}$$

$\phi_{sw,Qx}$ (x = B, C, D) is the phase shift implemented from the reference switch Q_A, T_s is the switching period, V_{HVDC} is the high voltage DC output from the FB converter, V_{LVDC} is the low voltage DC input to the FB converter, and D_{xfmr} is the desired duty cycle across the transformer.

It can be seen that the corresponding conduction time between Q_A/Q_D and Q_B/Q_C is exactly equal to the phase shift implemented between the respective switches. The dead time is implemented by turning on Q_A and Q_C, shorting the terminals of the transformer after a $+V_{LVDC}$ has been applied. Similarly the dead time after $-V_{DC}$ has been applied to the transformer by turning on Q_B and Q_D. In this way the set duty cycle is forced across the transformer independent of the load. All switches have a conduction time of $\frac{T_s}{2}$ (minus dead time) while the appropriate phase shift is implemented by controlling the delay of Q_B, Q_C, and Q_D from the reference switch Q_A.

3.3 Internal Sine Wave Reference Voltage Generation

In order to control the frequency and amplitude of the output AC voltage from the SGPN, an internal reference voltage must be generated for use when the grid voltage is not present. In other words, this signal generation would only be needed in islanded operation.

The TI ControlSUITE™ signal generation library [29] provides a very convenient function for generating the reference signal needed. A "standard THD sin generator" , "Low THD sin generator, and a "High precision sin generator" are offered for differing applications. The high precision sine generator was chosen for this design which allows for precise control of frequency through linear interpolation between a 256 point look up table [29]. This allows for a 32 bit counter and data type yielding a higher fidelity signal.

Eq. $y = y_1 + \frac{y_2 - y_1}{x_2 - x_1} * (x - x_1)$ (3-7) shows the equation for linear interpolation in the sine signal generator which allows for finer frequency control as well as smooth sampled sine reference signal. It is recognized that a sine wave is a non-linear waveform and therefore a linear curve fit might not make sense without qualification. If the change in value is sufficiently small between table look up values, then the curve can be approximated as a line. This is the fundamental that is applied in order to implement the linear interpolation.

$$y = y_1 + \frac{y_2 - y_1}{x_2 - x_1} * (x - x_1) \tag{3-7}$$

y is the interpolated value, y_1 is the previous sine value, y_2 is the next sine reference value in the table, x is the interpolated time, x_1 is the previous time value, and x_2 is the next time value.

Eqs. $gain$=1 (3-8) through $freq = \left(\frac{Required_{freq}}{Max_{freq}}\right) 2^{31} = \left(\frac{60\ Hz}{60\ Hz}\right) 2^{31} = 2^{31}$ (3-10) show the calculations required to use the signal generation library correctly. The CPU clock frequency and switching frequency are required to calculate the correct frequency for the

reference sine wave, so this is observed in the calculations. The actual frequency is determined by the "StepMax" value which increments the “modulo” counter in the signal generation function. The gain term controls the amplitude of the signal. F_{60Hz} is the output frequency sine wave, F_{ISR} is the control loop sample time, and “freq” is the value the counter uses normalized by the maximum frequency needed [29]. In this case no frequency deviating from 60 Hz is desired.

$$gain = 1 \tag{3-8}$$

$$StepMax = \frac{F_{60Hz} * 2^{32}}{F_{ISR}} = \frac{60\ Hz * 2^{32}}{10\ kHz} = 257698903.78 \tag{3-9}$$

$$freq = \left(\frac{Required_{freq}}{Max_{freq}}\right) 2^{31} = \left(\frac{60\ Hz}{60\ Hz}\right) 2^{31} = 2^{31} \tag{3-10}$$

3.4 System Level Operation Control Design and Related Topics

The details regarding individual converter modeling, control design, and related topics as they apply are given in [11]. The models and controls were developed on an individual converter basis assuming a static loading proportional to the power ratings of different power stages. Integration of multiple power stages presents some challenges and changes the dynamics of the system. Through simulation and experimental analysis, design changes in software and hardware were implemented. This section will introduce the concept of system level modeling, hardware changes that were made from analysis of system level simulations (discussed in detail in CHAPTER 4), as well as the control modifications that were made.

3.4.1 *System Level Hardware Modeling*

There are several ways of modeling for control purposes. There is the individual converter modeling that is necessary to account for the switching level detail of converters and variable loading conditions. This generally assumes some type of simple load at the output, such

as a resistor or load current source. However, there are interactions with integrated topologies that affect these models.

When cascading multiple power stages one could consider them dynamically decoupled if separated with a shunt capacitor and as long as individual stages are stable [30]. For example, the FB DC-DC converter is separated from the battery and PV converter through the LV DC link capacitor. Likewise, the inverter is decoupled from the FB DC-DC converter through the HV DC link capacitor. However, at the system level, step loading affects every converter from output to input. Rather than the detailed modeling of every power stage, a macromodeling approach was adopted in which switching level detail of some converters is neglected and only circuit behaviors are considered. An overview of the modeling approaches considered is given below.

[31] discusses a problem of control network coupling from a multi-port paralleled DC-DC converter configuration in which the solution presents a decoupling network that ensures independent converter operation. This network calculates separate control objects for the respective converters with a requirement that the control loop bandwidth of different converters must be separated. This would be useful in ensuring independent control network operation; however, it does address physical hardware dynamics. Further, this approach only considers DC-DC conversion which does not address the full SGPN topology.

[32] suggests a modular approach to modeling converters based on the principle that any signal can be approximated by a subset of its Fourier series with an error inversely proportional to the order of the approximation. This method allows for individual converter models that are topologically and configuration independent. However, it drastically increases the complexity of each converter model which would make controller design complex. For example, a 1^{st} order Fourier approximation of a 2^{nd} order boost converter yields 6 state variables.

One method of modeling considers each converter topology as a separate LTI system. Then those models can be transformed into a series combination of multiple LTI systems. This provides an easy way to account for system dynamics in a single model. A simplified block diagram of this method is shown below in Fig. 3.4.1. However, again, this produces an extremely complex model which increases the control complexity. Additionally, as mentioned, this level of detailed modeling is simply not needed.

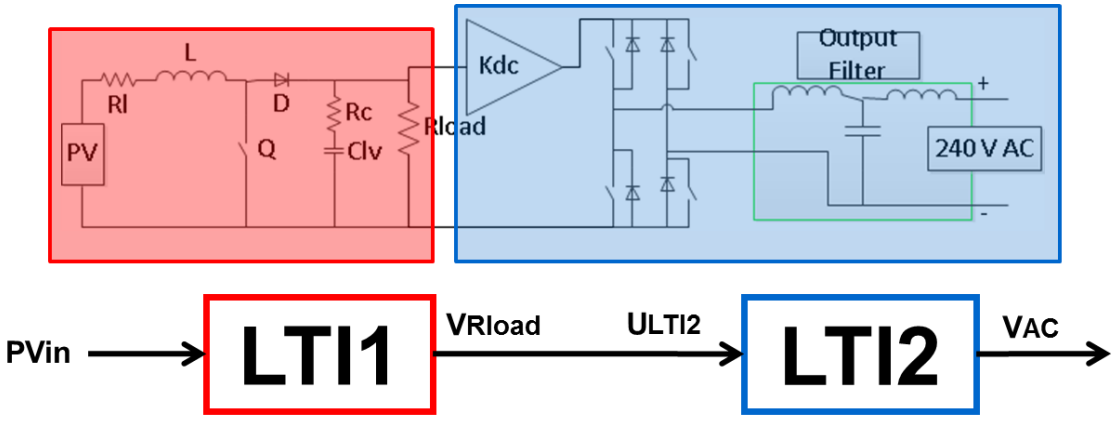

Fig. 3.4.1: Example SGPN Operating Mode - Series Combination of LTI Systems

The modeling solution preferred was a concept called macromodeling – adopted from integrated circuit design. This accomplished the goal of separating converter switching detail from system level behaviors. This allows for the original control targets to remain intact (the inductor current and capacitor voltage in the example of the boost converter) while maintaining the simple design techniques of linear control.

3.4.2 *PV Boost Converter Control Design*

From simulation and testing of the full system it was determined that a new control design was needed for the PV boost converter. Using the description of system level modeling in section 3.4.1 a detailed design analysis for the PV boost converter is presented. Before introducing the design, important factors affecting the model itself are presented.

3.4.2.1 Switching Dynamics

Switching of different converters can have unforeseen effects in a multi-stage system. For example, a uni-polar SPWM modulated single phase inverter induces a 120 Hz ripple on the DC system [26]. This non-ideality would propagate to the FB DC-DC converter, but also the PV boost and battery converter. The original control design assumed ideal inputs, but with the above real world effect, this assumption is no longer valid. Further, the system level circuit behavior was not considered initially.

Regardless of the individual switching frequencies, the high frequency switching effects of the FB DC-DC converter and H-Bridge inverter can be neglected if the Nyquist criteria are met. That is, as long as the cutoff frequency of the boost converter is at least ½ of the switching frequency [12]. By this justification the high frequency switching dynamics of the full-bridge converter and the H-bridge inverter are ignored and only the 120 Hz ripple is of concern.

3.4.2.2 Ripple Effect on Stability

The effect of inverter operation was mentioned above in section 3.4.2.1. A uni-polar modulated switching scheme was chosen for the inverter over bi-polar for its numerous benefits such as reduced harmonic distortion and reduced EMI [26].

Initially, linear control theory was used for PV boost converter. A stable controller can be designed using this technique assuming that the operation of the converter will not deviate significantly from its equilibrium point [33]. Conversely to high frequency switching ripple which is usually small, this low frequency ripple by the inverter can drastically affect the stability of the DC-DC converter.

One way to reduce the ripple is to increase the DC link capacitor. A large bulk capacitance has the consequence of slowing system response. However, as presented in section 3.4.3, the original design already had an undersized HV DC link capacitor. With the justified

need for increasing this value, and the benefit of stabilizing the system, this was the chosen solution.

Through calculations and experimental verification it was determined that under full load the ripple was reduced to a small enough percentage of the average value that the operation of the boost converter would not be significantly affected. Therefore simple linear control design techniques were retained.

3.4.2.3 Macromodel and MATLAB Control Design

Per sections 3.4.2.1 and 3.4.2.2 the model and design techniques in [11] are still valid. Therefore only relevant results and the new design are detailed here. The modeling of the system is quite simple once the desired circuit behavior is determined. It should be pointed out that since the SGPN topology is configurable, the circuit behavior desired can be different. This could potentially cause the model to change. Therefore a case by case analysis must be taken.

The two control targets of the boost converter are inductor current i_l and output capacitor voltage v_c. In full system operation, the effective output capacitance seen by the PV boost converter is much larger than what was considered in the original controller design. That is, the shunt capacitor on the low voltage DC bus C_{lv} and the reflected capacitance on the high voltage DC bus C_{hv} must both be considered.

Ignoring the switching dynamics of the FB converter, the HF transformer, and the inverter, the problem is reduced significantly. The transformer can then be modeled as a constant gain equal to the turns ratio $\frac{N_2}{N_1} = N = 13.667$. The full bridge converter can be modeled as a series resistance equal to the "on" resistance of its devices [34]. However, since the resistance of the MOSFET bridge device is very small (3.5 mΩ) [35] these values can be neglected.

Reflecting the HV capacitance across the transformer and adding the shunt capacitors in parallel, the equivalent output capacitance of the boost converter is shown in eq. $C_{eq} = C_{lv} + N^2 * C_{hv} = 2.7\,mF + 13.667^2 * 0.9\,mF = 170.8\,mF$ (3-11). It can be seen that there is capacitor value increase of over 63 x which could obviously cause instability in the original control design.

$$C_{eq} = C_{lv} + N^2 * C_{hv} = 2.7\,mF + 13.667^2 * 0.9\,mF = 170.8\,mF \tag{3-11}$$

From [11], the linearized state space model for the boost converter is shown in

$$\begin{bmatrix} \frac{x_{10}}{LR_L} - \frac{Rx_{10}+x_{20}}{C_{eq}(R+R_c)} + \frac{u_{10}}{L} \\ \frac{R_L x_{10}+x_{20}-u_{10}}{L} + \frac{x_{10}R_cR - x_{20}R_c}{L(R+R_c)} - \frac{x_{20}}{C_{eq}(R+R_c)} \end{bmatrix} \hat{d} + \begin{bmatrix} \frac{D}{L} \\ -\frac{D-1}{L} \end{bmatrix} \hat{u}_1 \tag{3-12}$$

where the output capacitance C is now the value of C_{eq}.

$$\begin{bmatrix} \hat{\dot{x}}_1 \\ \hat{\dot{x}}_2 \end{bmatrix} = \begin{bmatrix} -\frac{D}{LR_L} - \frac{R(D+1)}{C_{eq}(R+R_c)} & \frac{D-1}{C_{eq}(R+R_c)} \\ \frac{R_L(D-1)}{L} + \frac{R_cR(D-1)}{L(R+R_c)} & -\frac{R_c(D-1)}{L(R+R_c)} + \frac{D-1}{L} - \frac{D}{C_{eq}(R+R_c)} \end{bmatrix} \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \end{bmatrix} +$$

$$\begin{bmatrix} \frac{x_{10}}{LR_L} - \frac{Rx_{10}+x_{20}}{C_{eq}(R+R_c)} + \frac{u_{10}}{L} \\ \frac{R_L x_{10}+x_{20}-u_{10}}{L} + \frac{x_{10}R_cR - x_{20}R_c}{L(R+R_c)} - \frac{x_{20}}{C_{eq}(R+R_c)} \end{bmatrix} \hat{d} + \begin{bmatrix} \frac{D}{L} \\ -\frac{D-1}{L} \end{bmatrix} \hat{u}_1 \tag{3-12}$$

The control loop structure consists of an inner current loop and an outer voltage loop as before. The basic block diagram is shown below in Fig. 3.4.2. $C_2(s)$ is the voltage loop controller, $C_1(s)$ is the current loop controller, $G_{id}(s)$ is the input current to duty cycle transfer function, and $G_{vi}(s)$ is the output voltage to input current transfer function. The derivation of these transfer functions are detailed in [11]. V_o is measured and compared with a reference value V_{ref} equal to the desired low voltage DC bus. The voltage loop controller produces a current reference proportional to the load power demanded (at the output voltage level). The input

inductor current is measured and compared with the reference current from the voltage loop. The current loop controller then produces a duty cycle $0 \leq d < 1$ that is sent to the boost switch.

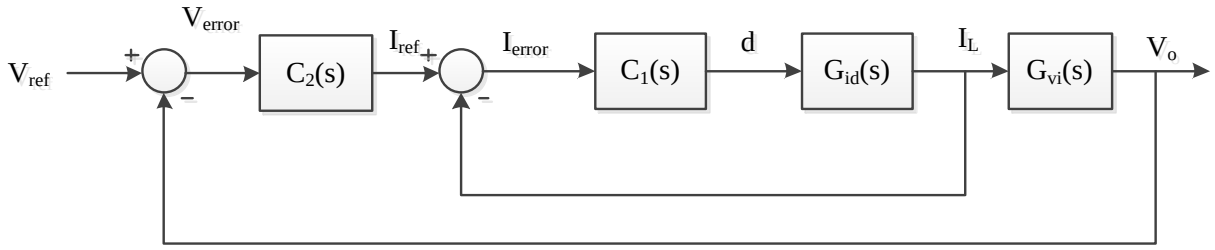

Fig. 3.4.2: PV Boost Converter Control Loop Structure - Courtesy of Brian P. Stalling [11]

The approach is to design the inner current loop first, and the outer voltage loop second since the closed loop transfer function of the inner current loop directly affects the voltage loop. The load resistance is set for the rating of the boost converter at $R = \frac{36\,V^2}{1000\,W} = 1.296\ \Omega$ and $C_{eq} = 170.8\,mF$ with all other parameters the same as in the original design.

The input current to duty cycle transfer function $G_{id}(s)$ is given by:

$$G_{id}(s) = \frac{2.12x10^8 s + 3.804x10^{12}}{s^2 + 1.871x10^6 s + 3.327x10^{10}} \tag{3-13}$$

The input voltage used to design the controller was 24 V (mid-point of the acceptable input voltage range) and the output voltage is specified at 36 V. The uncompensated open loop response G_{id} of the PV boost inner current loop is shown below in Fig. 3.4.3. It can be seen that the open loop response is closed loop stable, but has a crossover frequency of 33.7 kHz.

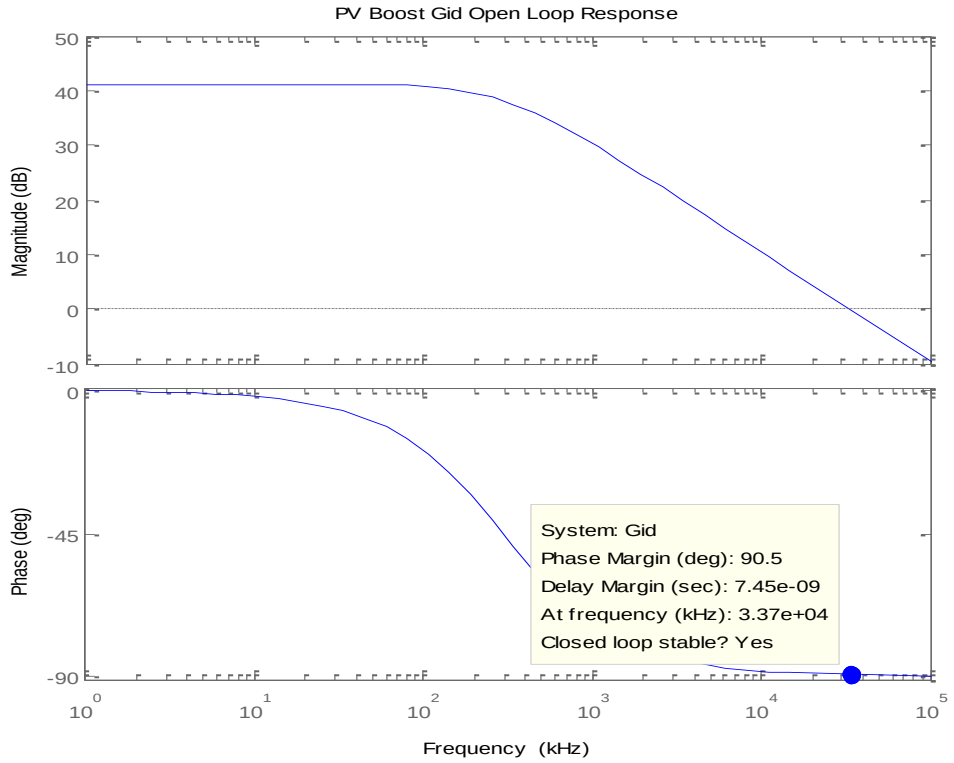

Fig. 3.4.3: PV Boost Converter - Gid(s) Open Loop Bode Plot

In order to satisfy Nyquist's theorem and achieve a damped system such that overshoot is minimized, the controller must reduce the crossover frequency <<f_s and achieve a large phase margin. Large positive phase margins ensure good stability, but can slow system response [33]. Since the increase in DC link capacitance slows the inherent response of the system, the current loop compensator was designed to keep the phase margin below 110°. A PI controller $C_1(s)$ was designed and given by the below transfer function.

$$C_1(s) = \frac{0.0028s+140}{s} \tag{3-14}$$

The compensated open loop response for the PV boost inner current loop G_i is shown below in Fig. 3.4.4. It is calculated in the frequency domain by $G_i = G_{id} * C_1$.

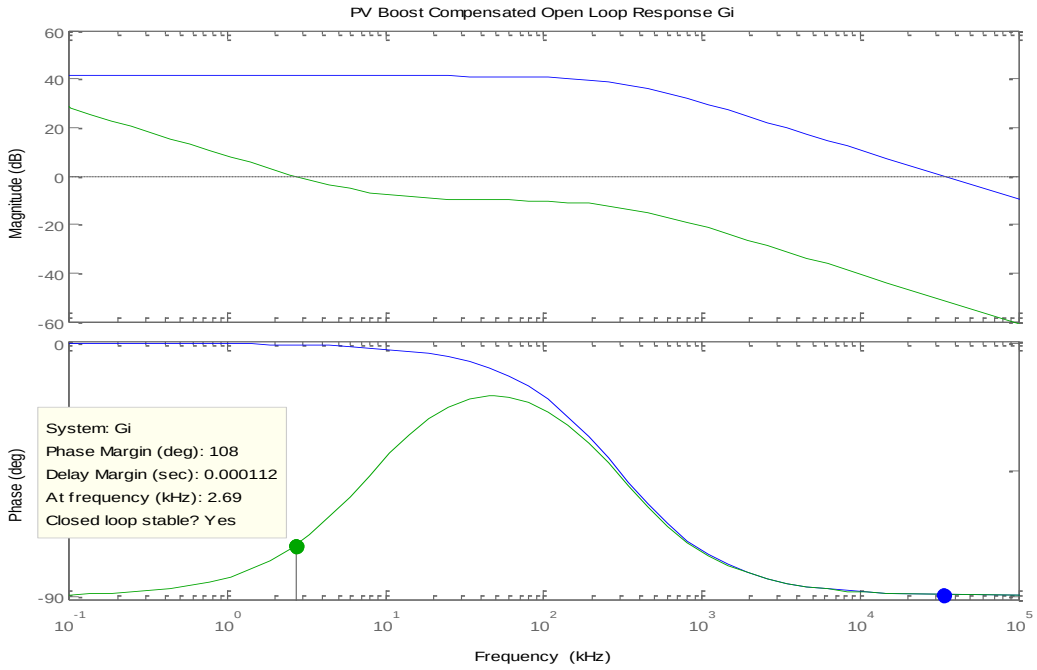

Fig. 3.4.4: PV Boost Converter - Gi Compensated Open Loop Response Bode Plot

It can be seen the designed controller reduces the crossover frequency to 2.69 kHz which is $< \frac{1}{6} f_s$ thus satisfying Nyquist requirements. Additionally the phase margin is within the design goal of 110° at 108°.

$G_i(s)$ is the closed loop transfer function with the current loop controller seen below in eq. $G_i(s) = \frac{5.9x10^5 s^2 + 4.0x10^{10} s + 5.3x10^{14}}{s^3 + 1.9x10^6 s^2 + 3.3x10^{10} s}$ (3-15). The closed loop step response of the inner current loop is shown below in Fig. 3.4.5. It can be seen that the system is critically damped such that there is no overshoot in the inner current loop. Even with a significant addition of bulk capacitance to the system, the redesigned controller achieves a reduction in settling time of >2.5x compared to the original design in [11].

$$G_i(s) = \frac{5.9x10^5s^2+4.0x10^{10}s+ 5.3x10^{14}}{s^3+1.9x10^6s^2+3.3x10^{10}s} \quad (3\text{-}15)$$

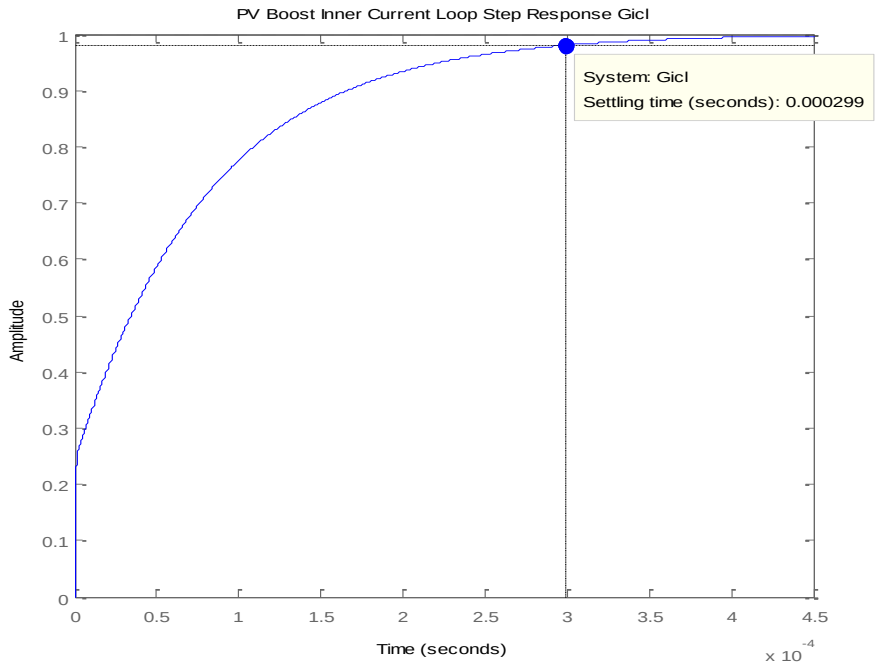

Fig. 3.4.5: PV Boost Converter - Inner Current Loop Closed Loop Step Response

The next step is to design the outer voltage loop compensator. First, the open loop output voltage to inductor current transfer function of the PV boost converter is given by:

$$G_{vi}(s) = \frac{G_{vd}(s)}{G_{id}(s)} * C_1 = \frac{\frac{V_c(s)}{D(s)}}{\frac{I_l(s)}{D(s)}} * C_1(s) =$$

$$\frac{1.8x10^{11}s^5+6.7x10^{17}s^4+6.4x10^{23}s^3+5.2x10^{28}s^2+1.2x10^{33}s+9.4x10^{36}}{2.1x10^8s^6+9.2x10^{14}s^5+1.0x10^{21}s^4+6.5x10^{25}s^3+1.6x10^{30}s^2+1.7x10^{34}s+6.7x10^{37}} \quad (3\text{-}16)$$

The open loop response of the voltage loop is shown below in Fig. 3.4.6. It can be seen that even at "0" frequency (DC), the system has a negative gain of -17.1 dB. A simple remedy is to design a controller with a sizable proportional gain. A large proportional gain can cause a large overshoot at startup since it depends solely on the amount of error between the reference

and measured signal [33]. For example, for an error of "10" at the output of the boost converter and a proportional gain K = 5, the proportional compensation would be 50. This has the benefit of increasing the response time of the system, but can cause oscillatory response if sized too large.

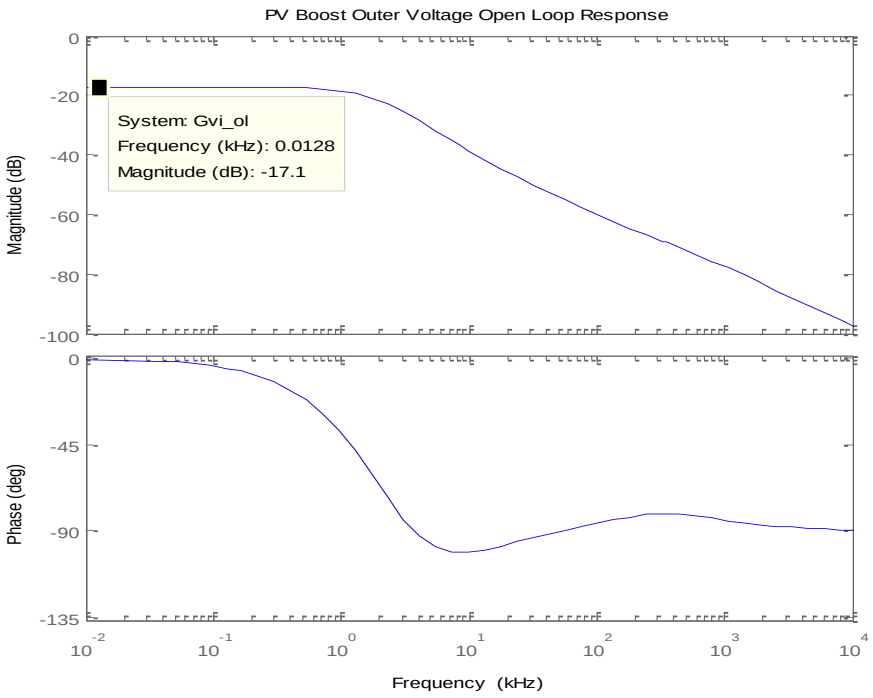

Fig. 3.4.6: PV Boost Converter - Outer Voltage Loop Open Loop Response Bode Plot

A PI controller was designed to give a good system response while minimizing overshoot. This was accomplished with a large proportional gain and a high phase margin. The controller C_2 is shown below in eq. $C_2 = \frac{10s+5000}{s}$ (3-17).

$$C_2 = \frac{10s+5000}{s} \tag{3-17}$$

The compensated voltage loop response is then given by:

$$G_v = G_{vi} * C_2 =$$

$$\frac{1.8x10^{12}s^6+6.7x10^{18}s^5+6.4x10^{24}s^4+5.2x10^{29}s^3+1.2x10^{34}s^2+1.0x10^{38}s+4.7x10^{40}}{2.1x10^{8}s^7+9.2x10^{14}s^6+1.0x10^{21}s^5+6.5x10^{25}s^4+1.6x10^{30}s^3+1.7x10^{34}s^2+6.7x10^{37}s} \quad (3\text{-}18)$$

The combined plot of the uncompensated (blue) and compensated (green) voltage loop response is shown below in Fig. 3.4.7. It can be seen that the controller achieves the desired large phase margin at 123° and a crossover frequency $\frac{1}{15}\ f_s$, while achieving the large gain boost needed.

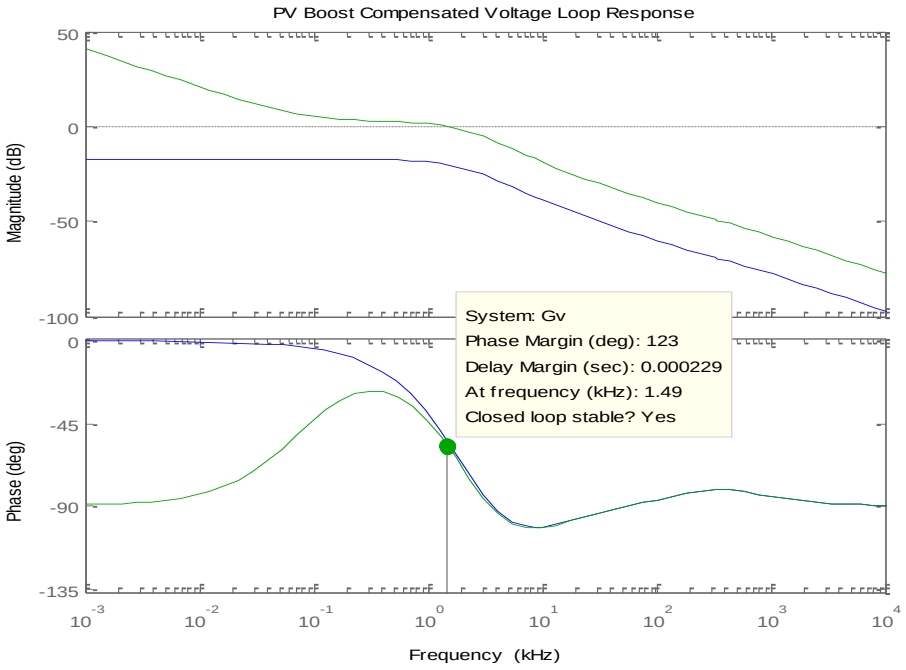

Fig. 3.4.7: PV Boost Converter - Compensated Open Loop Voltage Loop Response Bode Plot

The full closed loop step response for the PV boost converter with the new DC bulk capacitance is shown below in Fig. 3.4.8. Compared with the design in [11], the settling time of 10.3 ms is an increase by 25%. However given the significant increase in bulk capacitance to the system this is an acceptable performance while maintaining very simple design fundamentals. In the context of full system operation, 10.3 ms corresponds to ≈ 62% of a 60 Hz switching cycle meaning this design can recover from a step load condition in less than 1 output cycle.

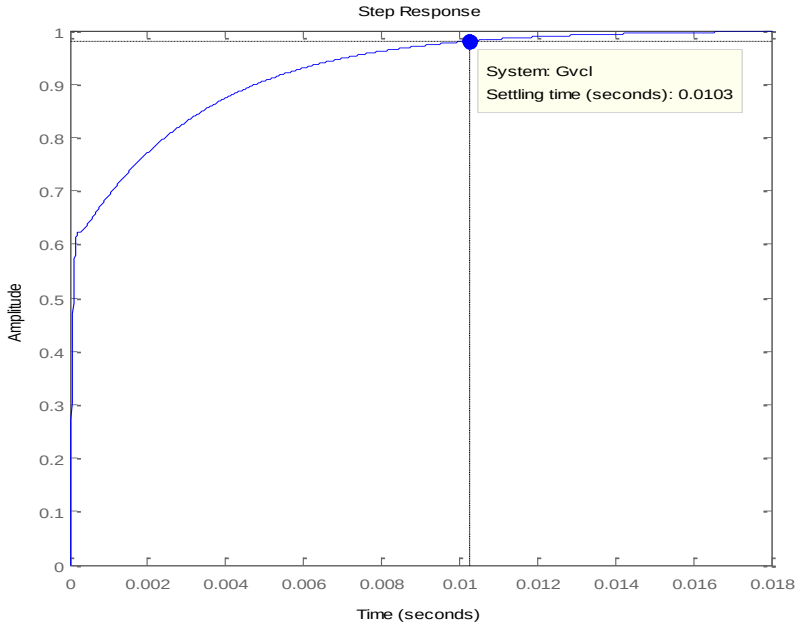

Fig. 3.4.8: PV Boost Converter - Closed Loop Step Response

3.4.3 *Hardware Changes*

This section shows the design of hardware changes that were needed after simulation and testing of the integrated system. As mentioned, uni-polar PWM single phase inverters produced a 2nd harmonic ripple on the DC link voltage (for 60 Hz output sine wave). It can be assumed that the switching frequency of the inverter is sufficiently high such that the high frequency ripple content is negligible. Therefore the DC side will only consist of a low frequency ripple and DC components [26].

In [11], it states that the 68 μF HV DC link capacitor was chosen based on a simulation that showed good ripple performance. This statement is applicable to the FB converter standalone design. However, through analysis of a comprehensive simulation study and experimental testing, it was determined that the originally designed capacitor was undersized to filter out the low frequency content induced by the inverter. Under rated power conditions this effect could cause mis-operation if the ripple on the DC voltage reaches a level below the

minimum peak AC sine voltage needed (≈340 V). For comparison, the ripple voltage calculations for the original design are given below based on [26]. Eq. $\widehat{v_{rip,original}} = \frac{P_{rated}}{2\omega V_{dc} C_{dc}} = \frac{2000\ W}{2(2\pi 60\ Hz)(350\ V)(68\mu F)} = 111.4\ V$ (3-20) is assuming that there is negligible energy stored in filter elements and a unity power factor. The following calculations are done for the worst case scenario, or minimum dc link voltage value.

$$C_{dc} = \frac{P_{rated}}{2\omega V_{dc} \widehat{v_{rip,original}}} \tag{3-19}$$

$$\widehat{v_{rip,original}} = \frac{P_{rated}}{2\omega V_{dc} C_{dc}} = \frac{2000\ W}{2(2\pi 60\ Hz)(350\ V)(68\mu F)} = 111.4\ V \tag{3-20}$$

$$\%v_{ripple,original} = \left(\frac{\widehat{v_{rip,original}}}{V_{dc}}\right) * 100\% = \left(\frac{111.4\ V}{350\ V}\right) * 100\% = 31.8\% \tag{3-21}$$

As can be seen, under full load the ripple voltage corresponds to 31.8 % which is an unacceptable performance, so the ripple voltage under full load was re-designed to be no more than 2.5%. Eq. $C_{dc,new} = \frac{P_{rated}}{2\omega V_{dc} \widehat{v_{rip,new}}} = \frac{2000\ W}{2(2\pi 60)(350\ V)(0.025*350\ V)} = 0.866\ mF \approx 0.9\ mF$

(3-22) shows the calculation for the improved capacitance value.

$$C_{dc,new} = \frac{P_{rated}}{2\omega V_{dc} \widehat{v_{rip,new}}} = \frac{2000\ W}{2(2\pi 60)(350\ V)(0.025*350\ V)} = 0.866\ mF \approx 0.9\ mF \tag{3-22}$$

$$\widehat{v_{rip,new}} = \frac{P_{rated}}{2\omega V_{dc} C_{dc}} = \frac{2000\ W}{2(2\pi 60\ Hz)(350\ V)(0.9\ mF)} = 8.42\ V \tag{3-23}$$

$$\%v_{ripple,new} = \left(\frac{8.42\ V}{350\ V}\right) * 100\% = 2.41\% \tag{3-24}$$

Based on the calculation above the new capacitance value was chosen to be 0.9 mF. This reduced the voltage ripple drastically making input to the inverter much more "stiff". The increased energy storage improves ride-through capability and ensures a more robust system operation.

It should be noted that this major increase in bulk capacitance to the system has certain consequences. It increases the size of the system, has a larger ESR, and increases losses. Also, given the governing equation of a capacitor, a large $\frac{dv}{dt}$ across the larger capacitance will draw a large inrush current from the input to the system. Thus there are design tradeoffs here between size, cost, protection, efficiency, and system reliability.

$$i_c = C\frac{dv}{dt} \tag{3-25}$$

For

3.4.4 ***Inverter Control: Island Model***

Based

3.4.4.1 Island Model Inverter Modeling

The

For a sinusoidal modulated system the equilibrium point is not constant, but periodic. However the state variable coefficients are constant; therefore the model for the converter is the same for every point [36]. The modeling of a single phase full bridge inverter is detailed in [36]. This same method is adopted and the state space inverter model in island mode is shown below $iL1vo = 0 - 1L11Cac - 1zacCaciL1vo + vdc0dab$ (3-26).

$$\begin{bmatrix} \dot{\imath_{L1}} \\ \dot{v_o} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_1} \\ \frac{1}{C_{ac}} & -\frac{1}{z_{ac}C_{ac}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_o \end{bmatrix} + \begin{bmatrix} v_{dc} \\ 0 \end{bmatrix} d_{ab} \tag{3-26}$$

After linearizing the state space model, the following final inverter model in islanded mode is obtained.

$$\begin{bmatrix} \hat{i}_{L1} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_1} \\ \frac{1}{C_{ac}} & -\frac{1}{Z_{ac}C_{ac}} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} V_{dc} \\ 0 \end{bmatrix} \hat{d}_{ab} \quad (3\text{-}27)$$

3.4.4.2 Island Model Inverter Control Design

The control system for the inverter is a double loop current mode control in which the plant function is split into an output voltage to inductor current(G_{vi}) and an inductor current to duty cycle (G_{id}) transfer function. The reference voltage sine wave is compared with the differential inverter output voltage across the filter capacitor producing an error that is the input to the voltage loop compensator. The outer voltage loop produces a reference current that is proportional to the power demanded at the load. The input to the current loop is the error between the voltage loop compensator output and the measured current across the first filter inductor. The duty cycle output from the current loop compensator is used for the drive signal to the inverter devices. For uni-polar switching a second duty cycle is created which is 180° out of phase with the current loop compensator. The structure of the control loop is shown below in Fig. 3.4.9.

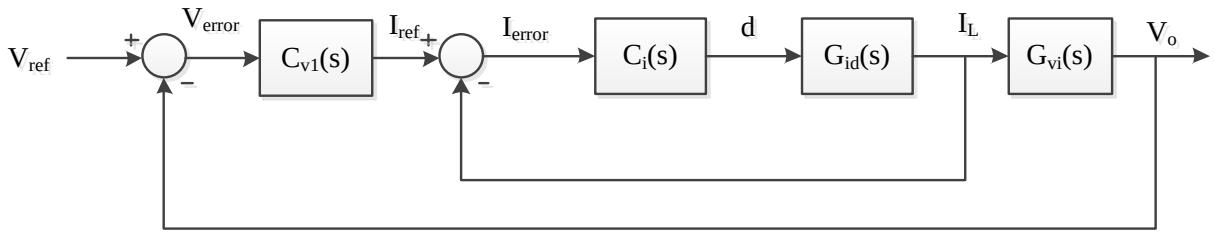

Fig. 3.4.9: H-bridge Inverter Control Loop Structure - Coutesy of Brian P. Stalling

The plant function derivations of the H-bridge inverter are detailed in [36]. These are shown below for reference.

$$G_{id}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}_{ab}(s)} = V_{dc}\frac{1}{L_1 s} \tag{3-28}$$

Recall that the minimum dc input to the inverter is 340 V. It should be noted that since the DC link voltage will vary with loading an operating input voltage is chosen as 385 V which can allow for flexibility in the DC link. The bode plot of the inner loop plant transfer function $G_{id}(s)$ is shown below in Fig. 3.4.10 with a crossover frequency of around 18 kHz.

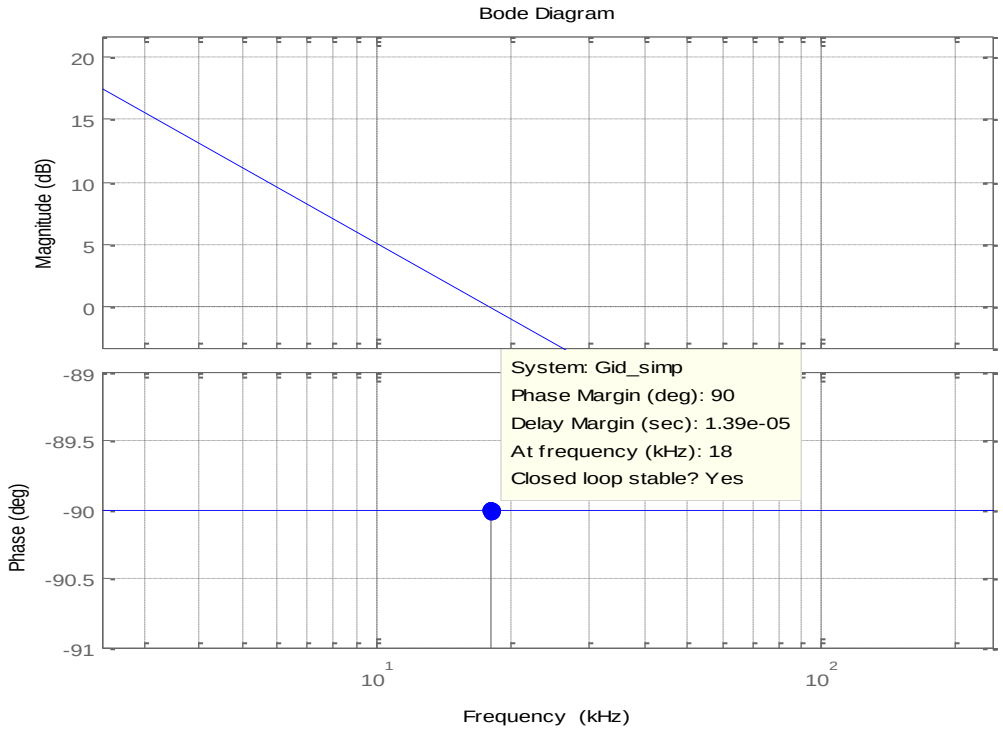

Fig. 3.4.10: H-bridge Inverter - Inner Current Loop Natural Circuit Response Bode Plot

A PI controller was designed to give a crossover frequency of around 3 kHz with a phase margin close to 90 degrees (eq. $C_i(s) = \frac{K_{pi}s+K_{ii}}{s} = \frac{0.18s+300}{s}$ (3-29)). This ensures that there will be good damping in the closed loop response and a good dynamic step response.

$$C_i(s) = \frac{K_{pi}s + K_{ii}}{s} = \frac{0.18s + 300}{s} \quad (3\text{-}29)$$

The open loop compensated transfer function is given by eq. $Gi = C_i G_{id}$ (3-30). The bode plot of the uncompensated (blue) and compensated (green) inner current loops are shown in below in Fig. 3.4.11.

$$G_i = C_i G_{id} \quad (3\text{-}30)$$

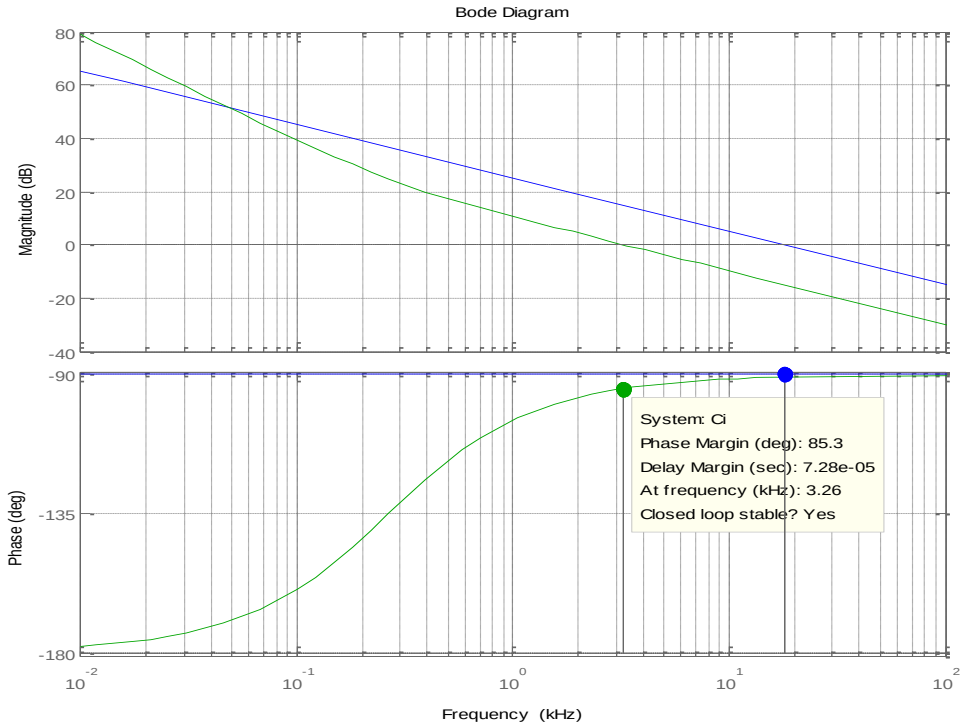

Fig. 3.4.11: H-bridge Inverter - Compensated Inner Current Loop Open Loop Response Bode Plot

Applying a unity feedback gain, the closed loop step response of the inner current loop is shown in Fig. 3.4.12.

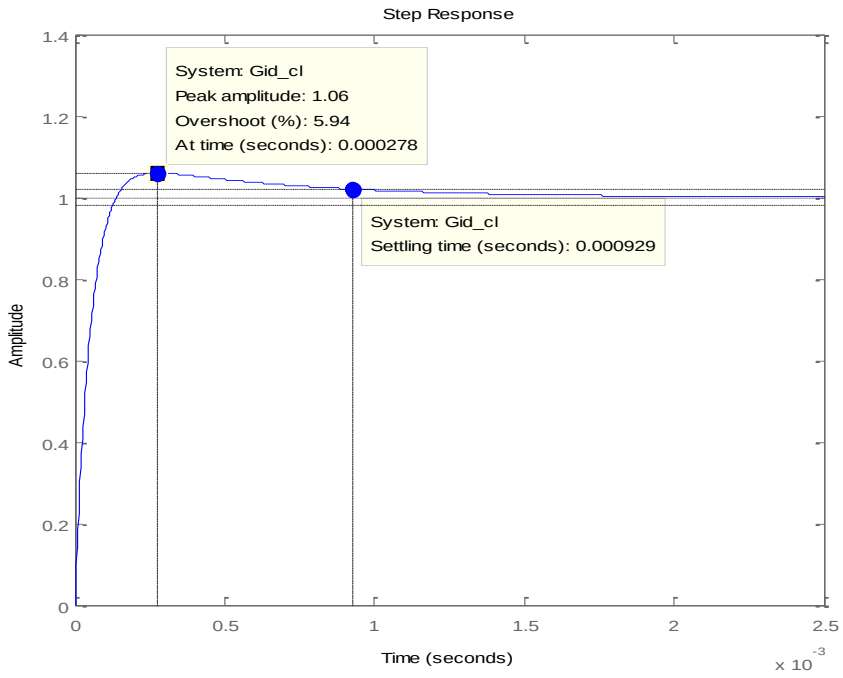

Fig. 3.4.12: H-bridge Inverter - Inner Current Loop Closed Loop Step Response

Compared to [11] the new controller has a reduction in overshoot by almost 3x while still achieving a fast settling time just over 5% of a 60 Hz period. This settling time is 2.5x the original design (2% of a 60 Hz period) but is still sufficient for a good dynamic performance.

The next step is to design the outer voltage loop controller for the voltage loop plant function which is realized by eq. $G_{vi}(s) = \frac{\hat{v}_o(s)}{\hat{\imath}_L(s)} = \frac{Z_{ac}}{1+Z_{ac}C_{ac}s}$ (3-31).

$$G_{vi}(s) = \frac{\hat{v}_o(s)}{\hat{\imath}_L(s)} = \frac{Z_{ac}}{1+Z_{ac}C_{ac}s} \quad (3\text{-}31)$$

Fig. 3.4.13 shows the uncompensated open loop gain of the outer voltage loop. It can be seen that both the inner and outer loop plant functions are inherently stable which makes designing a controller easier.

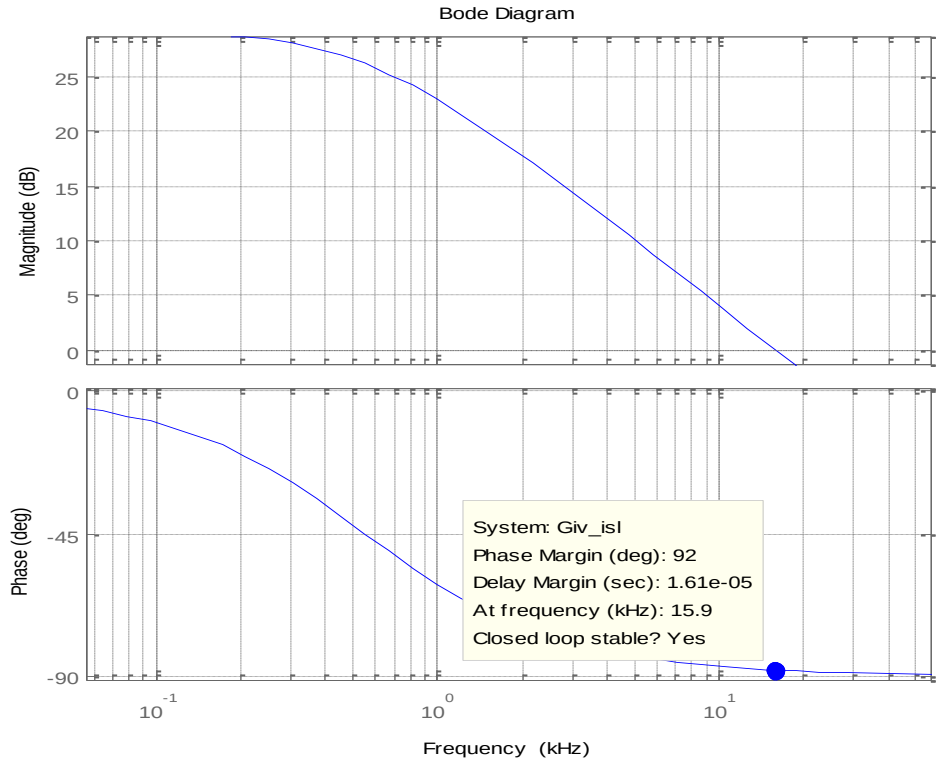

Fig. 3.4.13: H-bridge Inverter - Uncompensated Outer Voltage Loop Response Bode Plot

Similar to the inner current loop a PI controller given by eq. $C_v(s) = \frac{K_{pv}s+K_{iv}}{s} = \frac{0.105s+375}{s}$ (3-32) was tuned through testing and verified through design. The open loop gain of the outer voltage loop takes into account the closed loop gain of the inner current loop ($G_{i,CL}$) as well as the voltage plant function (G_{vi})and controller (C_v). This is shown below in eq. $G_v = G_{i,CL}G_{vi}C_v$ (3-33). This controller achieves a phase margin of around 62 degrees with a crossover frequency of 1.61 kHz. The bode plot showing the uncompensated and compensated open loop gain of the outer voltage loop is shown in Fig. 3.4.14.

$$C_v(s) = \frac{K_{pv}s + K_{iv}}{s} = \frac{0.105s + 375}{s} \tag{3-32}$$

$$G_v = G_{i,CL} G_{vi} C_v \tag{3-33}$$

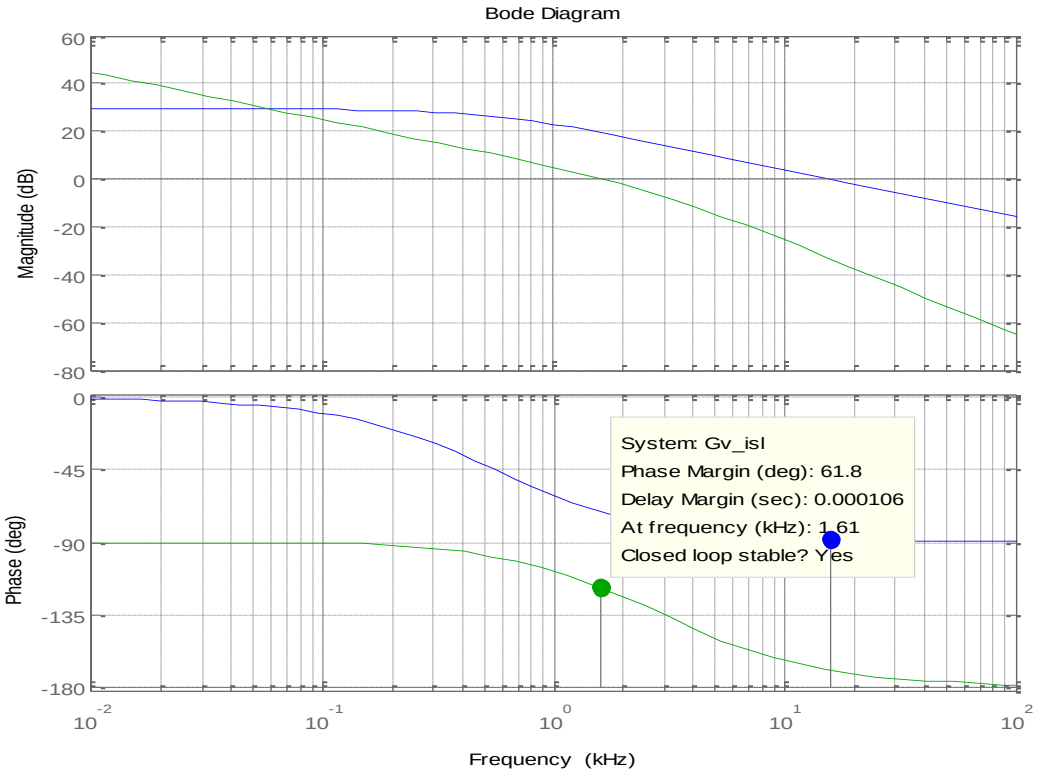

Fig. 3.4.14: H-bridge Inverter - Compensated Outer Voltage Loop Response Bode Plot

Finally, applying a unity feedback to the outer voltage loop the closed loop step response of the entire inverter is given in Fig. 3.4.15.

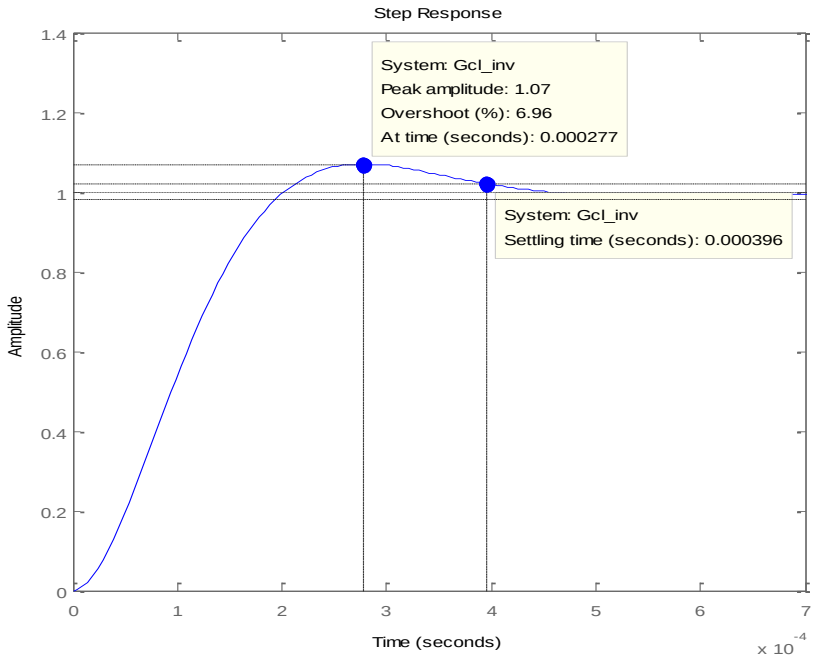

Fig. 3.4.15: H-bridge Inverter - Closed Loop Step Response

It can be seen that the controllers tuned to the actual hardware are stable with the model used proving that it is indeed fundamentally valid. Additionally, compared with the original control design the re-designed controls yielded a better performance. The closed loop step response of the outer loop with the re-designed controls showed a reduction in overshoot by almost 3x and a reduction in settling time of almost 4.5x. The summary of advantages and disadvantages of the inverter control re-design is summarized in Table 3.4.1.

Table 3.4.1: Comparison of Inverter Island Mode Control Design Performance Criteria

Comparison of inverter controls		
Metric	**Original Design**	**New Design**
Inner Loop		
Peak Response	X	✓
Settling Time	✓	X
Outer Loop		

Peak Response	X	✓
Settling Time	X	✓

3.4.5 *Control Isolation Design*

This section will cover the design of the SGPN isolation board used to isolate the control components from the power boards. The early version of USC's universal control platform that was used for the SGPN did not have any onboard isolation or protection. It was discovered through testing the full system that conducted EMI was causing failure of control board components as a result. Therefore, a separate digital isolation board was designed to protect the hardware.

3.4.5.1 Isolation Design

In order to have an isolated system, the reference ground for the control side and the power side must be electrically separate. This eliminates any noise generated by power switching devices from propagating to the control input. As long as the isolated side reference is electrically connected to the control board reference, and the power side reference is connected to the power board reference, signal integrity is maintained.

The first step to designing the isolation barrier is to ensure compatibility with the existing house power supply for the control board. The control platform has a DC regulator that is capable of supplying 1 A at 3.3 V. There are two chips that supply power to the board, one for digital circuits and another for the analog circuits. Given that the burden from the digital circuitry is very small, and the isolation chip used is digital, the digital regulator on the control board is used to power the control side of the isolation chip.

The power side of the isolation barrier requires an electrically separate power supply in order to maintain the isolation barrier. Therefore an isolated DC-DC regulator was chosen to

power the isolation chip from the power layout side of the barrier. The VBT1-S3.3-S3.3-SMT by CUI Inc. [37] takes a range of voltages from 3.0 – 3.63 V input and converts 1:1 to a 3.3 V output (nominal). This supply was chosen so the control side and power side of the isolation barrier have the same supply voltages. It requires an input capacitor of 4.7 μF and an output capacitor of 10 μF for voltage filtering. In addition it provides a minimum of 1 kV DC isolation [37].

The next step is to present the isolator for the SGPN. The Si8660BC-B-IS1 by Silicon Labs [38] is the low power digital isolator chosen. The Si8660x family features an isolation barrier up to 5 kV supporting data transmission rates of up to 150 Mbps, and signal propagation delay of only 10 ns (maximum) [38]. It uses a proprietary RF modulation/demodulation technique that is separated by a semi-conductor isolation barrier. The transmitter modulates the signal output from the control board which is then demodulated on the receiver/power board end [38]. The simplified functional diagram is shown below in Fig. 3.4.16.

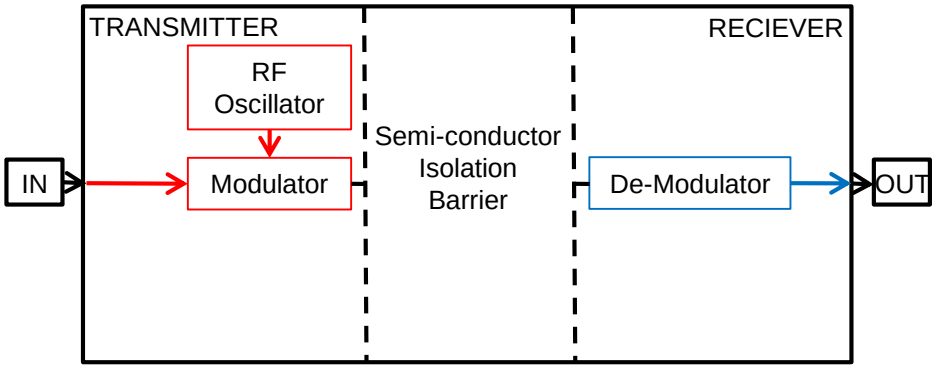

Fig. 3.4.16: Si8660 Digital Isolation Chip - Functional Block Diagram

This chip is designed to take a range of supply voltages from 2.5-5.5 V. It has an UVLO feature that will disable the chip if the supply voltage drops below 2.5 V [38]. This is a protection feature to avoid damaging the internal circuitry. Since the propagation of signals from power to control components needs to be avoided the chip selected is strictly a uni-directional

signal path- from the control side to the power side. As alluded to above, the isolation chip requires two electrically separated power supplies and references. The basic circuit configuration for the isolation chip is shown below in Fig. 3.4.17.

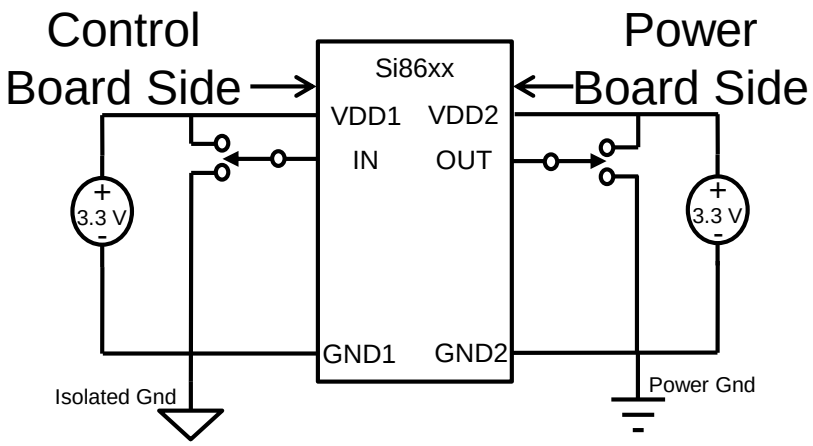

Fig. 3.4.17: Si8660 Digital Isolation Chip - Simplified Operational Schematic

3.4.5.2 Isolation Board Design

This section presents the SGPN isolation board layout design. A diagram of the board layout is shown below in Fig. 3.4.18. This board was designed in PCB Artist – a free layout software developed by Advanced Circuits for their customers. Since the isolation board is a relatively simple layout, only a two layer board was required.

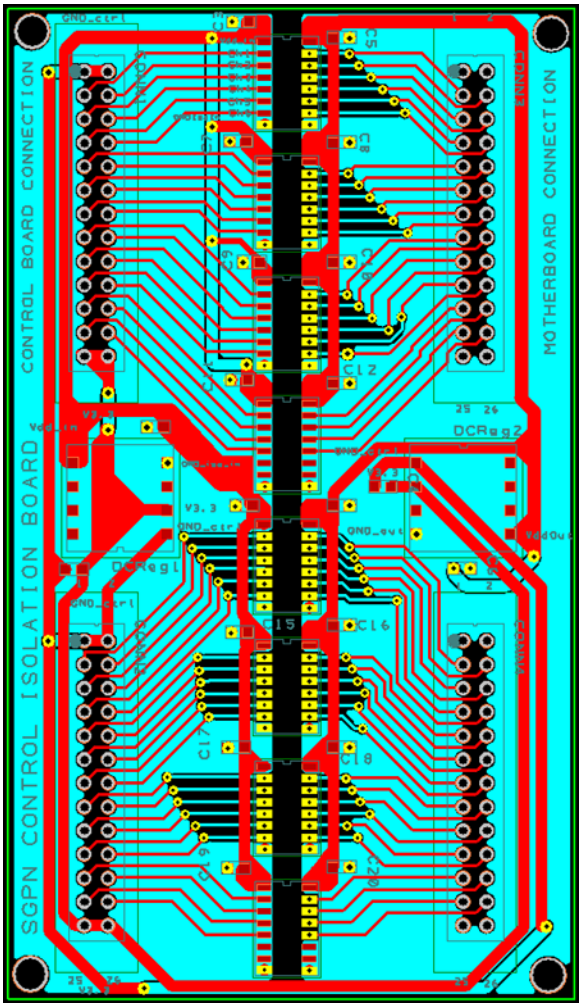

Fig. 3.4.18: Control Isolation Board Layout

The isolation chip lies directly in the middle between the control board side and the power board side. Signal routing was done such that a physical gap was left where no traces were run across the isolated area. This helps ensure that the isolation barrier remains intact. Given the large number of control signals required by the SGPN, a total of 8, 6 – channel isolation chips were used along with the respective connectors and power supply. The two distinctly separated light blue layers are the reference planes for the respective sides of the isolation barrier. The control board reference plane is connected to the control board ground and the power board

reference plane is connected to the power circuit ground. A picture of the finalized isolation board layout can be seen below in Fig. 3.4.19.

Fig. 3.4.19: Populated Control Isolation Board Picture

It should be noted that the overall prototype did incur a cost increase because of the new board and added more hardware. However, this was a necessary improvement to protect the system. Advanced Circuits fortunately has a program in which discount two layer boards are available to students. Otherwise the cost would likely be very high (for a single board order). The isolation chips are relatively inexpensive at $3.88/ea, the connectors are of negligible cost at $1.00/ea, and the isolated DC-DC regulators are around $3.70/ea (at the time of purchase). The total added cost to the prototype is summarized below in Table 3.4.2. It can be seen that the total

cost added is very small at $75.44, but this is not accounting for economies of scale and a multi-board order which would be a significant cost savings in a commercialized product.

Table 3.4.2: Isolation Board Cost Breakdown

Isolation Board Cost Analysis			
Item	**Cost each**	**Quantity**	**Cost**
Isolation Board	$33.00	1	$33.00
Isoaltion Chip	$3.88	8	$31.04
Isolated DC-DC Power Supply	$3.70	2	$7.40
Connectors	$1.00	4	$4.00
Total Isolation Cost			$75.44

CHAPTER 4

SIMULATION RESULTS

This chapter presents the closed loop simulation results of relevant individual converters, sub-integrated converters, fully integrated converters, and operating mode transitions. Simulation results including sensing circuitry, gate drivers, and many of the individual converters were detailed in [11]. Therefore this section is focused mainly on the integration of the closed loop hardware and only simulations of individual converters that were modified through experimental verification will be presented.

4.1 Closed Loop H-bridge Inverter

As mentioned, closed loop simulation of the H-bridge inverter was detailed in [11]. However the controls for the island mode operation were modified through testing to adjust for discrepancies between the simulation model and practical implementation. The design of this controller was detailed in 3.4.4. The grid connected inverter closed loop simulations were given in [11]. Since no change was made to the controls for grid-connected mode, the results are not restated here.

4.1.1 *Island Model*

Fig. 4.1.1 below shows the Simulink simulation model used to simulate the closed loop inverter. In order to simulate the worst case scenario for the inverter, an input of 350 V DC was used with the worst case calculated ripple voltage on the DC link of 8.75 V (section 3.4.3). To maintain linear modulation of the inverter, 340 V is the absolute minimum input voltage that can be supplied because the peak output of the AC sine waveform is 340 V. Any input voltage lower than this will cause the inverter to enter square wave operation. Therefore a minimum voltage of 350 V is maintained for a safety margin. The block labeled “Inverter Control” is the control structure depicted in 3.4.4.2 with the LCL filter designed in [11].

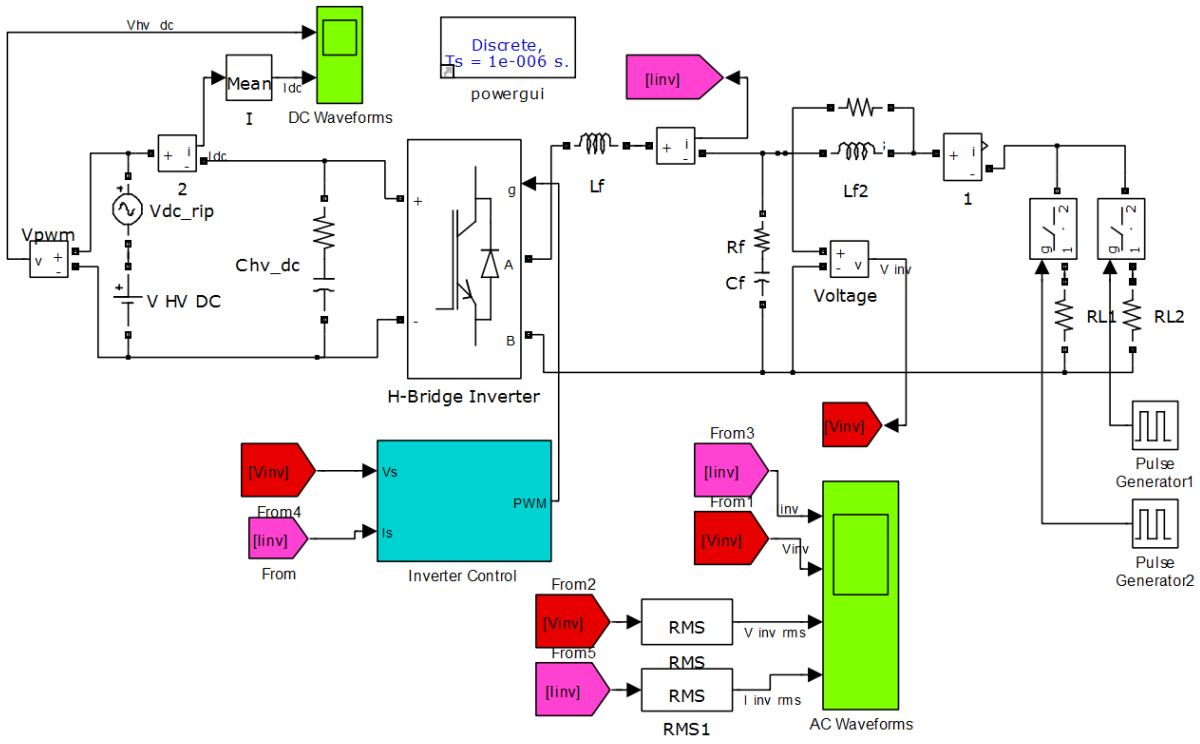

Fig. 4.1.1: H-bridge Inverter - Simulation Model

The control algorithm developed in section 3.4.4.2 was used for the simulation of the inverter. The inverter output voltage and current as well as its RMS values are shown below in Fig. 4.1.2. The simulation times are as follows:

$$\begin{bmatrix} 0 \leq t \leq 0.05\,s & \rightarrow NO\ LOAD \\ 0.05 \leq t \leq 0.1\,s & \rightarrow 2\,kW\ LOAD \\ 0.1 \leq t \leq 0.15\,s & \rightarrow NO\ LOAD \end{bmatrix}$$

It can be seen that the controller for the inverter maintains the output voltage very close to 240 V RMS, but with slight variations. The maximum deviated voltage from the reference of 240 V_{RMS} is 242.3 V which corresponds to an error of 0.958 %. This demonstrates the ability of inverter controls to maintain the specified residential voltage with an almost instantaneous response under a 100 % step loading condition.

There is very small inverter current which is mostly attributed to the reactive power being drawn by the LCL filter. Further discussion on this will be given in CHAPTER 6 . During load transition the inverter control shows stable operation with an extremely fast dynamic response for a 100% step load change.

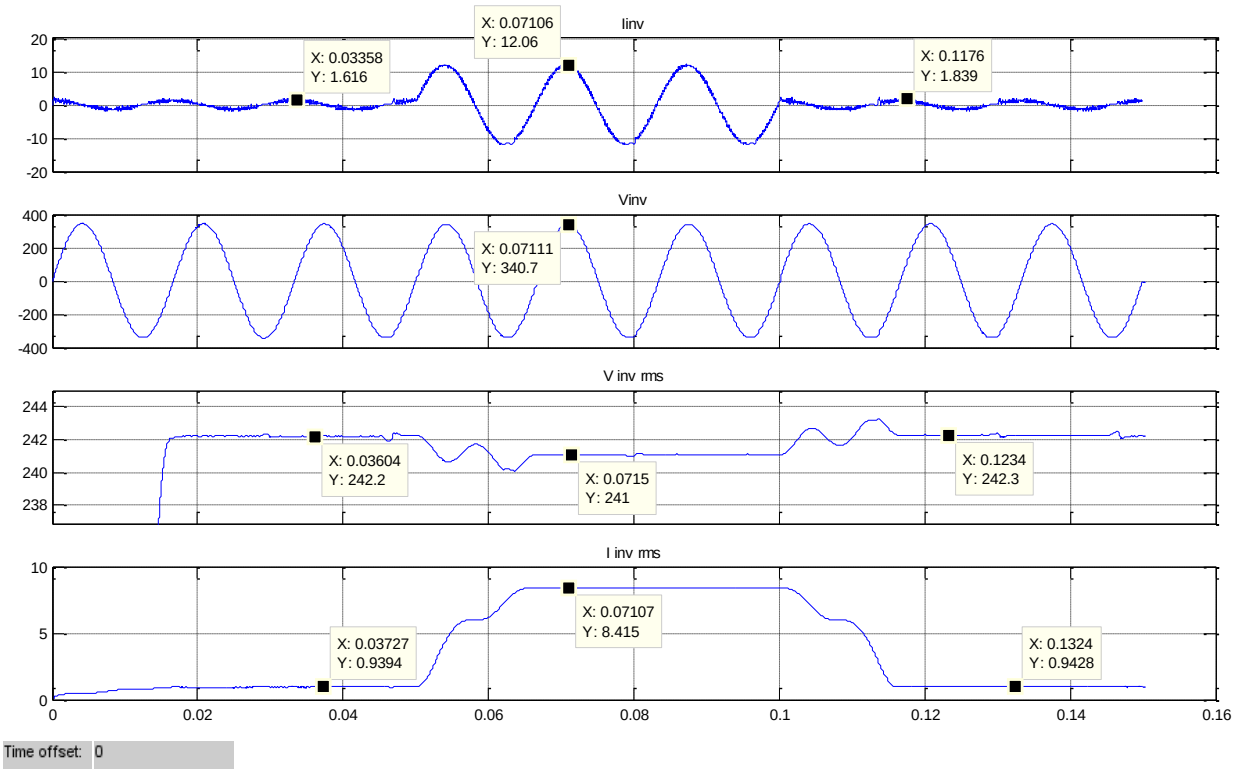

Fig. 4.1.2: Closed Loop H-bridge Inverter Simulation – Islanded - AC Waveforms

Fig. 4.1.3 shows the simulation results for the input and output power for the inverter. It can be seen that for the first simulation transition, there is a slight power draw from the DC side. This can be explained by the device losses and ESR of the HV DC capacitor, and AC filter elements. During full load the simulated efficiency of the inverter is approximately 98.4 % compared to the calculated efficiency of 96.85% presented in [11]. This yields an error of about 1.55 % between calculated and simulated efficiencies.

The part numbers for the inductors and bulk capacitors were used to find the true ESR values. The device losses for the IGBTs were estimated through the forward voltage of the IGBTs and the switching times quoted in the datasheet. The discrepancy between [11] and this simulation can be due to the two different simulators and slightly different simulation models. While an effort was made to build non-idealities into simulation, actual losses could be more due to the inaccuracy between simulations and the real world.

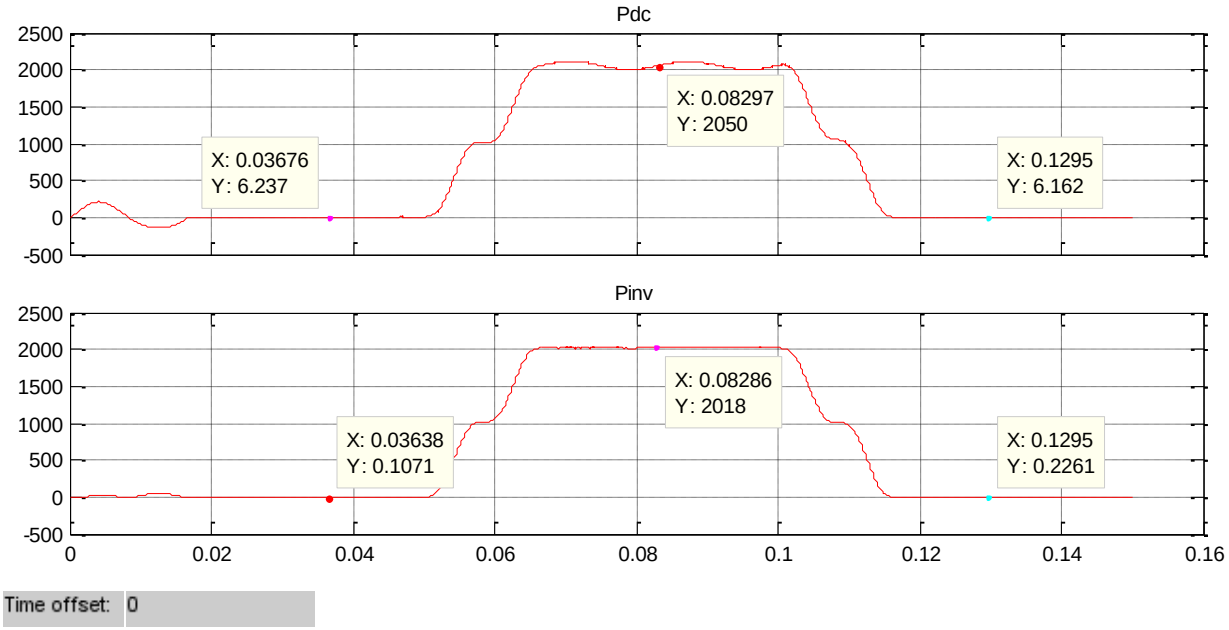

Fig. 4.1.3: Closed Loop H-bridge Inverter Simulation – Islanded - Power Waveforms

4.2 Full Inverter (FB DC-DC and H-Bridge Inverter)

Part of system integration involved a comprehensive closed loop full system simulation study after necessary modifications through experimental testing. One change demonstrated in 5.2 is the need for a phase shifted PWM scheme on the full bridge converter. While the grid connected simulations were not shown for the standalone inverter, they are included in the remaining simulations as they will be influenced by the new FB switching scheme.

The inverter simulation results were for full load under rated voltage conditions in order to demonstrate its intended operation. However, given the topology this cannot be accomplished without the full bridge DC-DC converter stage which is needed to boost the DC voltage to an appropriate level for AC inversion. The explanation of this topology requirement was given in 3.4.1. This section presents the simulation of the full inverter with the full bridge DC-DC stage ran open loop and the inverter ran closed loop for the same control design in the above section.

4.2.1 *Island Model*

Fig. 4.2.1 below shows the simulation model for the full inverter. The LV DC input voltage to the system is 36 V and assumed to be stiff due to the bulk capacitance and active control of this link voltage. Since the FB is ran open loop it is recognized that the HV DC voltage average and ripple will vary slightly with loading. Therefore instead of simulating the minimum HV DC input to the inverter, the average value is set to be 375 V. More will be discussed on these effects. The loading of the converters will be the same as in section 4.1.1, and are shown below.

$$\begin{cases} 0 \leq t \leq 0.05\,s \rightarrow NO\ LOAD \\ 0.05 \leq t \leq 0.1\,s \rightarrow 2\,kW\ LOAD \\ 0.1 \leq t \leq 0.15\,s \rightarrow NO\ LOAD \end{cases}$$

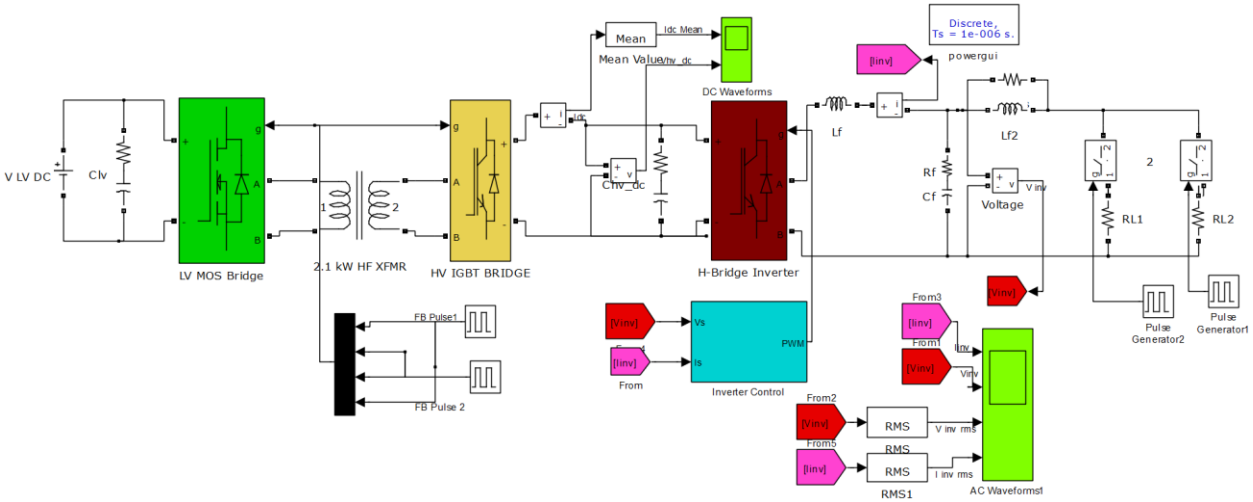

Fig. 4.2.1: Closed Loop Full Inverter Simulation - Islanded - Simulation Model

Fig. 4.2.2 and Fig. 4.2.3 show the low voltage and high voltage DC waveforms for the simulation of the full inverter, respectively. The current drawn from the DC side is obviously not DC. This is due to the high frequency discontinuous currents that are drawn from the switching converters and the large 2nd harmonic current that the single phase inverter draws [26]. This would also result in a large 2nd harmonic to be imposed on the DC link voltage as well which can be seen on the high voltage side. The calculation from data markers verify that the large, low frequency ripple component is very close to the 2nd harmonic, or 120 Hz.

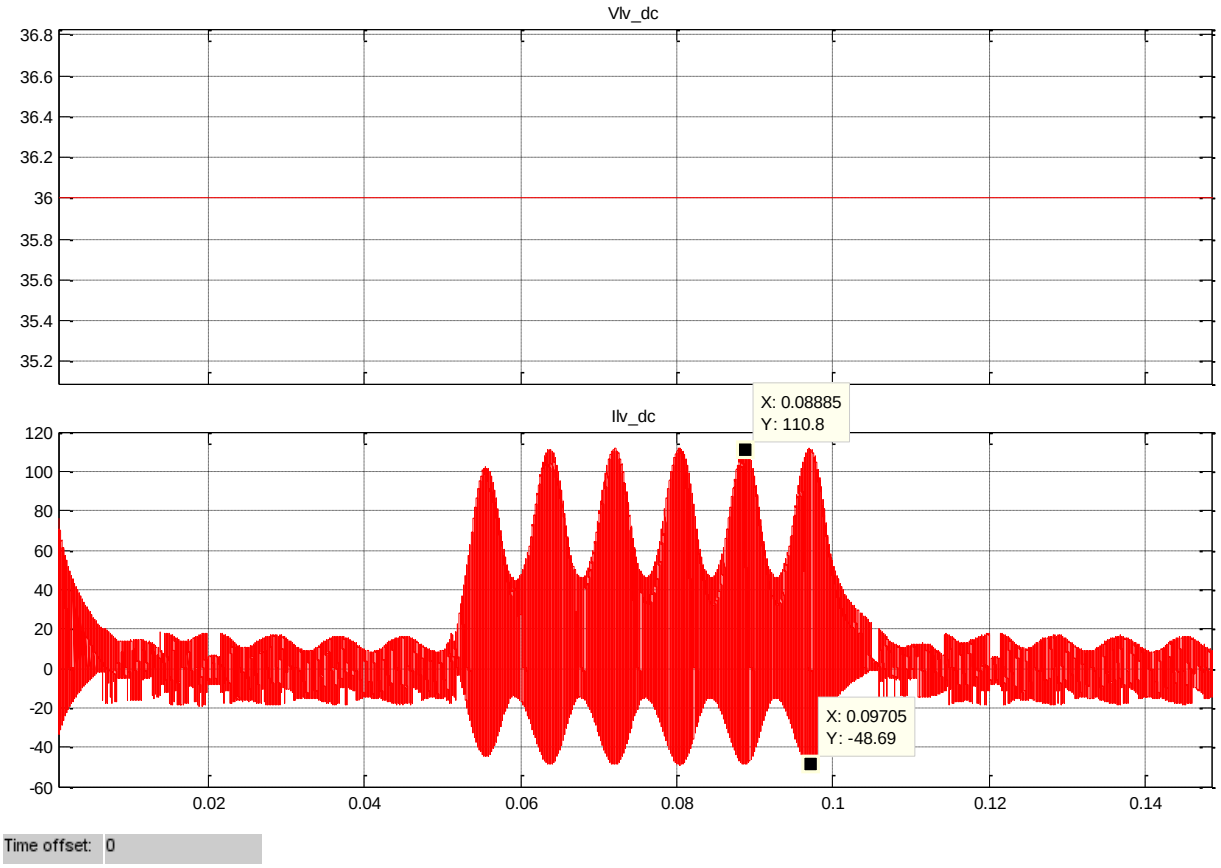

Fig. 4.2.2: Closed Loop Full Inverter Simulation - Islanded - LV DC Waveforms

$$f_{rip,LV} = \frac{1}{\Delta t_{rip,LV}} = \frac{1}{(0.09705\ s - 0.08895\ s)} = 121.95\ Hz \quad (4\text{-}1)$$

$$f_{rip,HV} = \frac{1}{\Delta t_{rip,HV}} = \frac{1}{(0.09695\ s - 0.08866\ s)} = 119.04\ Hz \quad (4\text{-}2)$$

It can be seen in Fig. 4.2.3 that the 2nd harmonic current drawn does indeed induce this same frequency ripple on the HV DC link voltage. As stated above, when the full load is applied the HV DC link voltage's average value is reduced to around 360 V while the ripple is increased to around 15 V. This makes sense as the more current is drawn the magnitude of the ripple current increases and therefore the voltage as well. A 15 V ripple on an average of 360 V is around 4.17% which is greater than the calculated (2.4%) by 1.77%, but is still within an acceptable range.

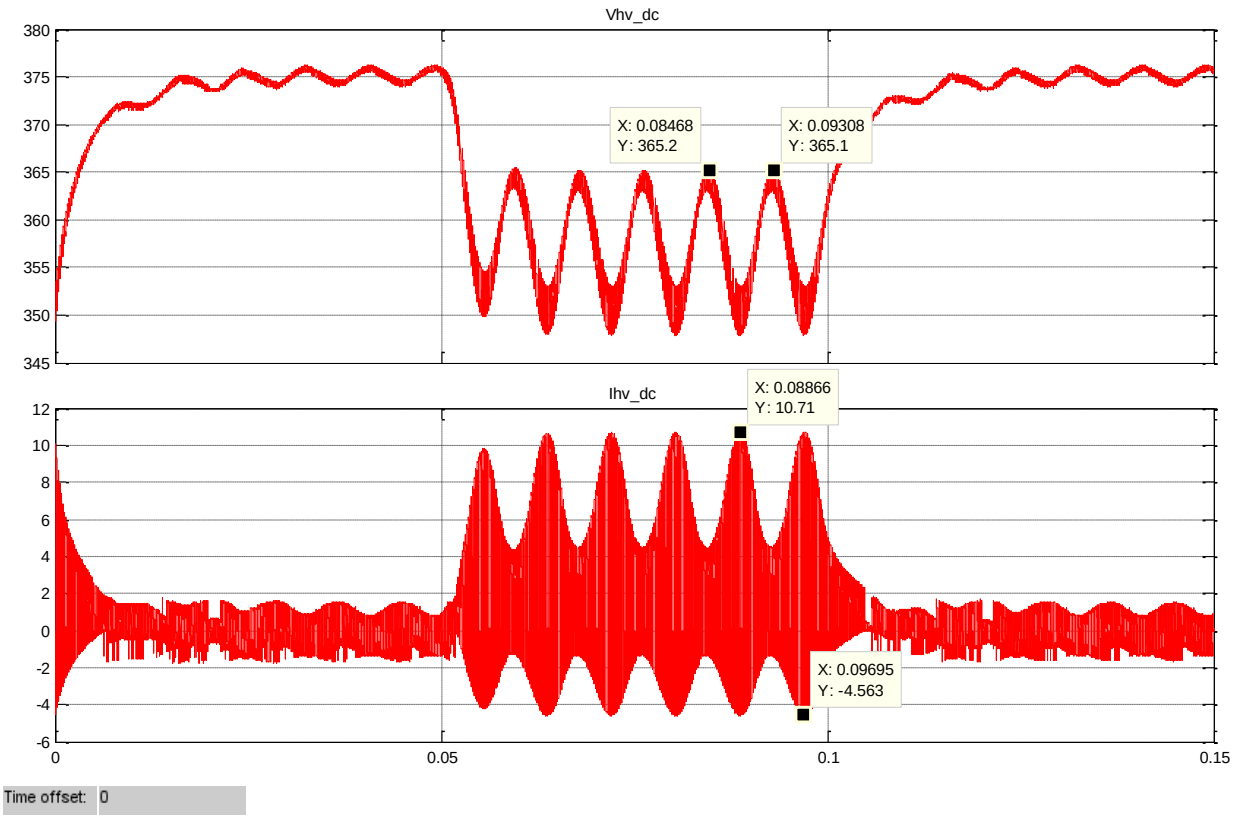

Fig. 4.2.3: Closed Loop Full Inverter Simulation - Islanded - HV DC Waveforms

Fig. 4.2.4 below shows the inverter output current and voltage waveforms. Very similar behavior to the simulation in section 4.1.1 is observed. The controller maintains the RMS voltage output very close to the 240 V RMS reference with a maximum deviation of 242.1 V RMS. This corresponds to a steady state error of 0.875 %.

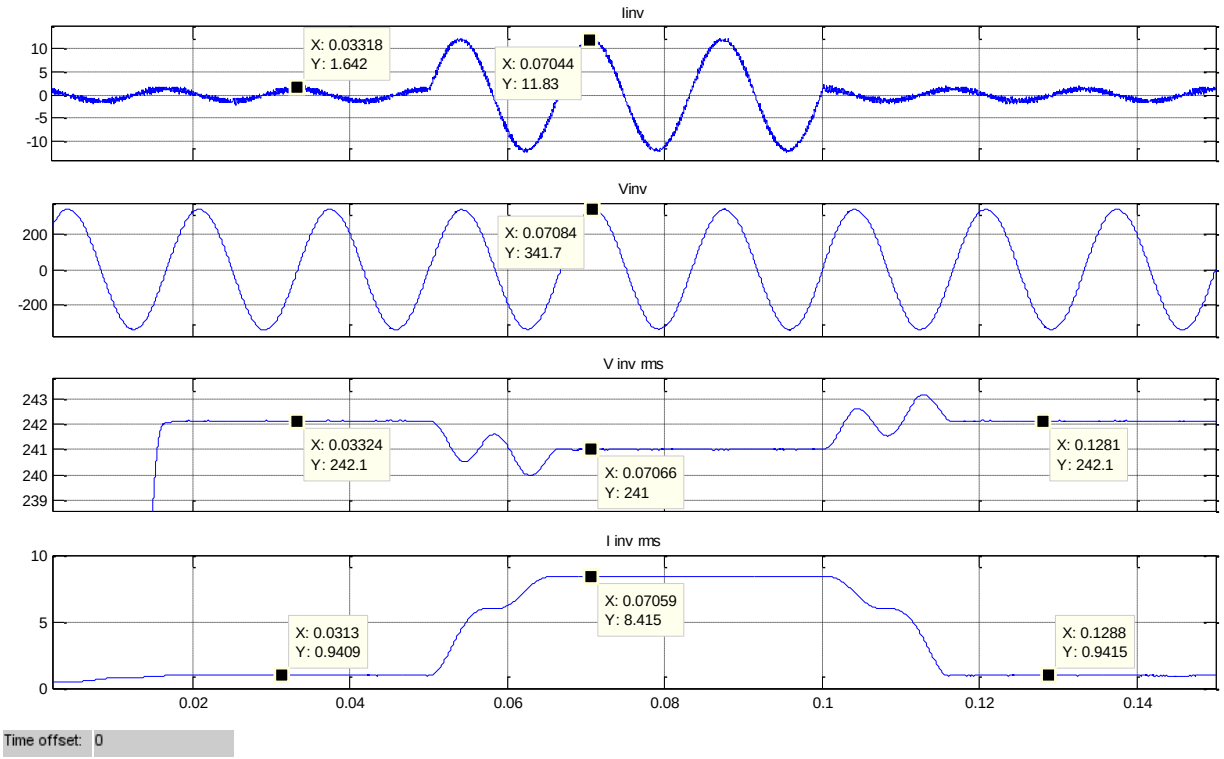

Fig. 4.2.4: Closed Loop Full Inverter Simulation - Islanded - AC Waveforms

Fig. 4.2.5 shows the power outputs from the low voltage DC, high voltage DC, and AC output during load step times. It can be seen that there is a startup transient in which there is an inrush to charge the bulk capacitance in the circuit. More on this will be discussed in the CHAPTER 5 . The simulated efficiency for the full inverter under full load is 92.7 %.

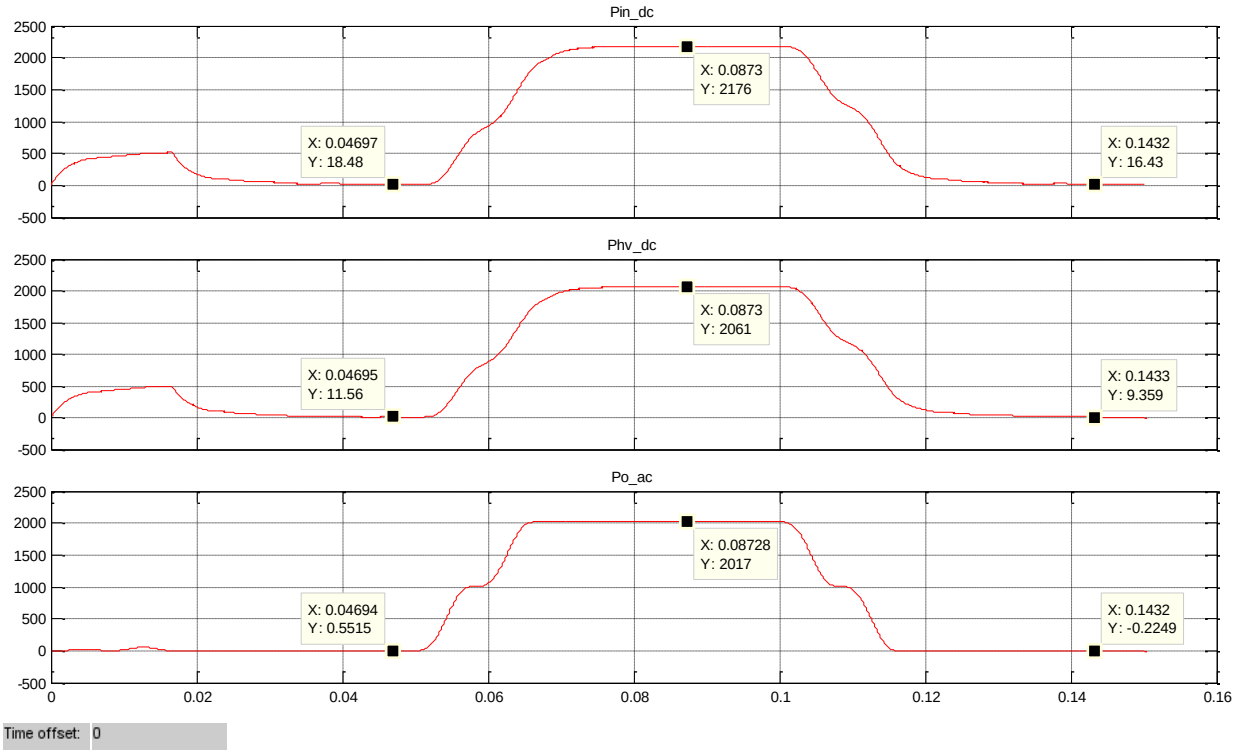

Fig. 4.2.5: Closed Loop Full Inverter Simulation - Islanded - Power Waveforms

4.3 Closed Loop PV Boost Converter with Full Inverter

This section presents the closed loop simulation results of the PV boost converter, full bridge DC-DC converter, and the H-bridge inverter in islanded and grid-connected mode. This simulation will only consist of sending power from the PV converter to the AC bus as well as load sharing with the grid since the PV converter is uni-directional power flow. The PV array is assumed to be at a voltage of 24 V which will be boosted to the 36 V LV DC bus. The FB DC-DC converter boosts this voltage to 375 V nominal and is then inverted to 240 V_{RMS}, 60 Hz, which serves as the AC bus and grid connect.

4.3.1 *Island Model*

Below in Fig. 4.3.1 shows the Simulink simulation model for the first full operation mode of the PV boost converter with the full inverter. To illustrate the figure, the green portions are the PV boost converter, the light grey stage shows the full bridge DC-DC converter, while the light

blue stage is the H-bridge inverter. The controller developed for the boost converter in section 3.4.2 is used with the same inverter controller as presented in above sections.

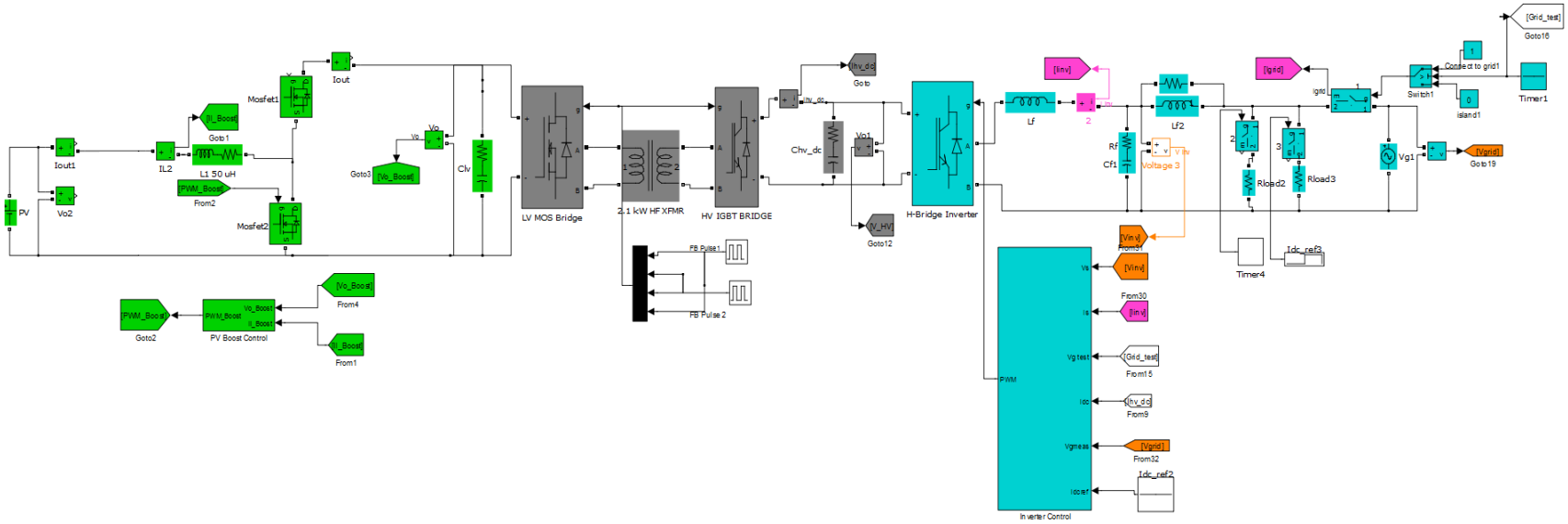

Fig. 4.3.1: Closed Loop PV Boost Converter with Full Inverter Simulation - Islanded - Simulation Model

In order to show the control stability over a wide dynamic load range, the system is stepped from 200 W load, to 1 kW, and back to 200 W. It is known that the boost converter requires a load in order to maintain continuous conduction [12]. At extremely small loads, the boost converter can enter the discontinuous mode of operation when operating standalone. Further, the low frequency 2nd harmonic induced by the inverter complicates this problem. The boost controls were not designed to operate in this mode, therefore a minimum of 200 W is simulated. The switching times and respective loads are summarized below.

$$\begin{cases} t1\text{: } 0 \ \leq t \ \leq 0.1\ s \ \rightarrow 200\ W\ LOAD \\ t2\text{: } 0.1 \ \leq t \ \leq 0.2\ s \ \rightarrow 1\ kW\ LOAD \\ t3\text{: } 0.2 \ \leq t \ \leq 0.3\ s \ \rightarrow 200\ W\ LOAD \end{cases}$$

Below in Fig. 4.3.2 is the low voltage DC microbus voltage, the input current through the boost inductor, and high voltage DC voltage and current, respectively. It can be seen that the boost converter maintains the DC link voltage very close to 36 V through all load transitions and voltage regulated by the boost controller sags briefly during the step load. As expected, there is a corresponding sag in the HV DC bus voltage, but is well within design parameters for normal operation and is therefore acceptable.

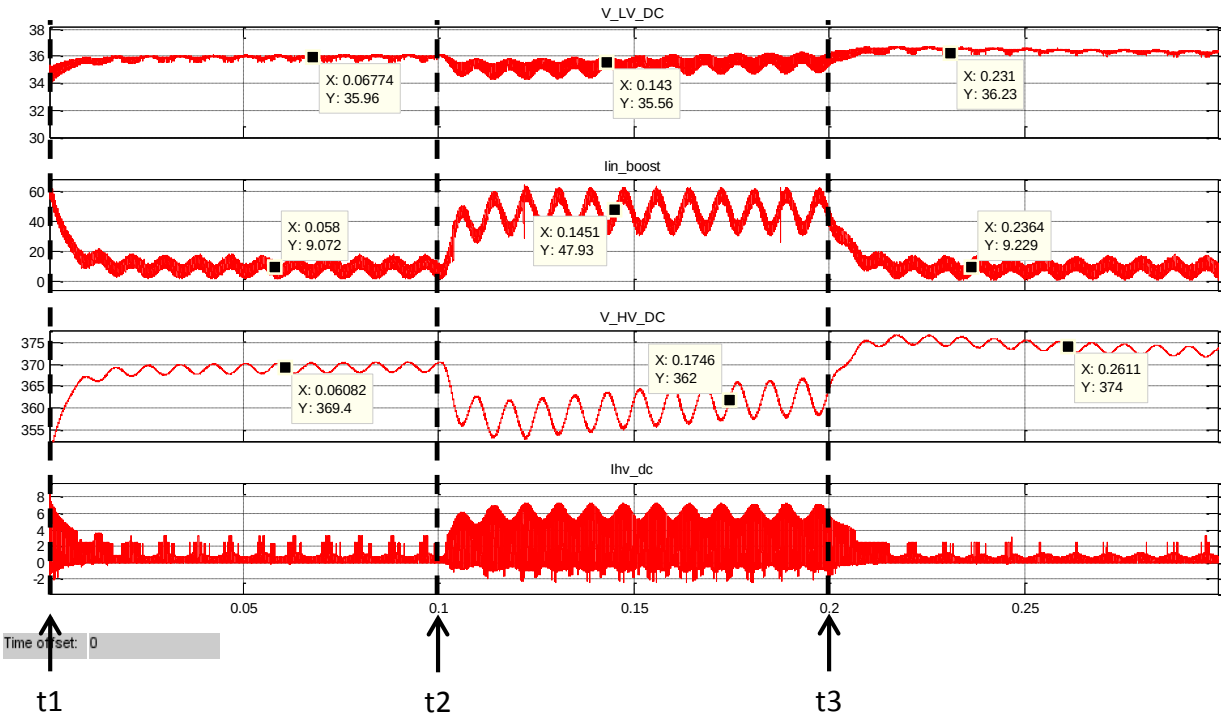

Fig. 4.3.2: Closed Loop PV Boost Converter with Full Inverter Simulation – Islanded - DC Waveforms

The performance criteria for the DC-DC converter stages are summarized below in Table 4.3.1. It can be seen from the specifications put forth in red that the fully loaded PV boost converter passes both dynamic criteria and steady state ripple criteria and similarly for the full-bridge DC-DC converter. It should be pointed out from this analysis that the full system operation will have 2 paralleled DC input converters. Therefore the ripple and voltage sag from load steps should improve.

Table 4.3.1: Closed Loop PV Boost Converter with Full Inverter Simulation – Islanded -DC System Performance

Boost + Full Inverter (Island): DC-DC Performance					
		Max. Spec		**Simulation Result**	
		Voltage	% rated	Voltage	% rated
Sag	LV DC link	3.6 V	10.0%	1.73 V	4.8%

Voltage	HV DC link	37.5 V	10.0%	22 V	5.9%
Ripple Voltage	LV DC link	1.8V	5.0%	1.53 V	4.3%
	HV DC link	37.5 V	10.0%	9.2 V	2.4%

Fig. 4.3.3 shows the inverter waveforms for the full system operation. The controller used for the inverter is the same as above sections. For an average input of around 375 V DC the inverter maintains the output AC voltage at very close to the reference 240 V RMS. The maximum deviation from this value is 2.1 V corresponding to an error of 0.875%. The inverter also shows a good dynamic and stable performance throughout all load changes with a recovery time of less than a quarter of a 60 Hz cycle. It is also important to note that the voltage ripple and voltage sag experienced on the DC system have negligible effects on the AC output.

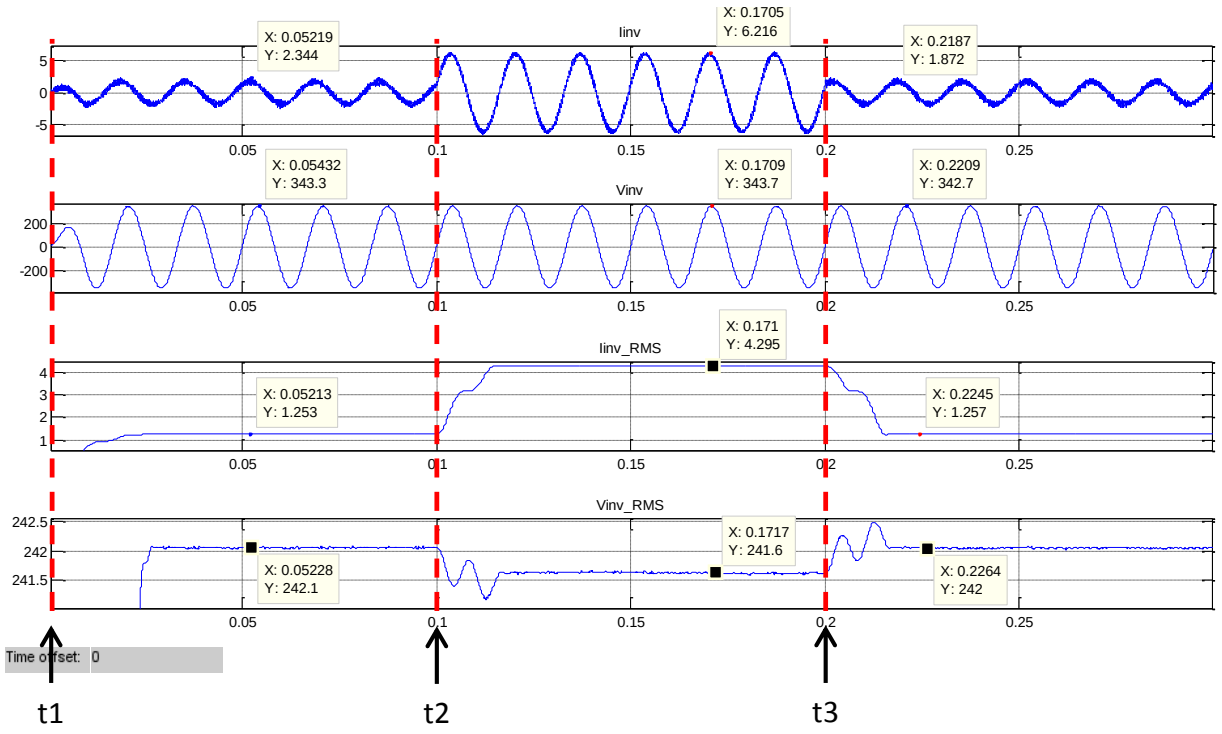

Fig. 4.3.3: Closed Loop PV Boost Converter with Full Inverter Simulation – Islanded - AC Waveforms

Fig. 4.3.4 shows each (averaged) DC power output as well as the delivered power to the AC side. As described for the simulation a step load takes place at 0.1 s from 200 W → 1 kW and at 0.2 s a step load from 1 kW → 200 W again. There is a period at the beginning of simulation where the startup transient take place which is normal for hard starting the system.

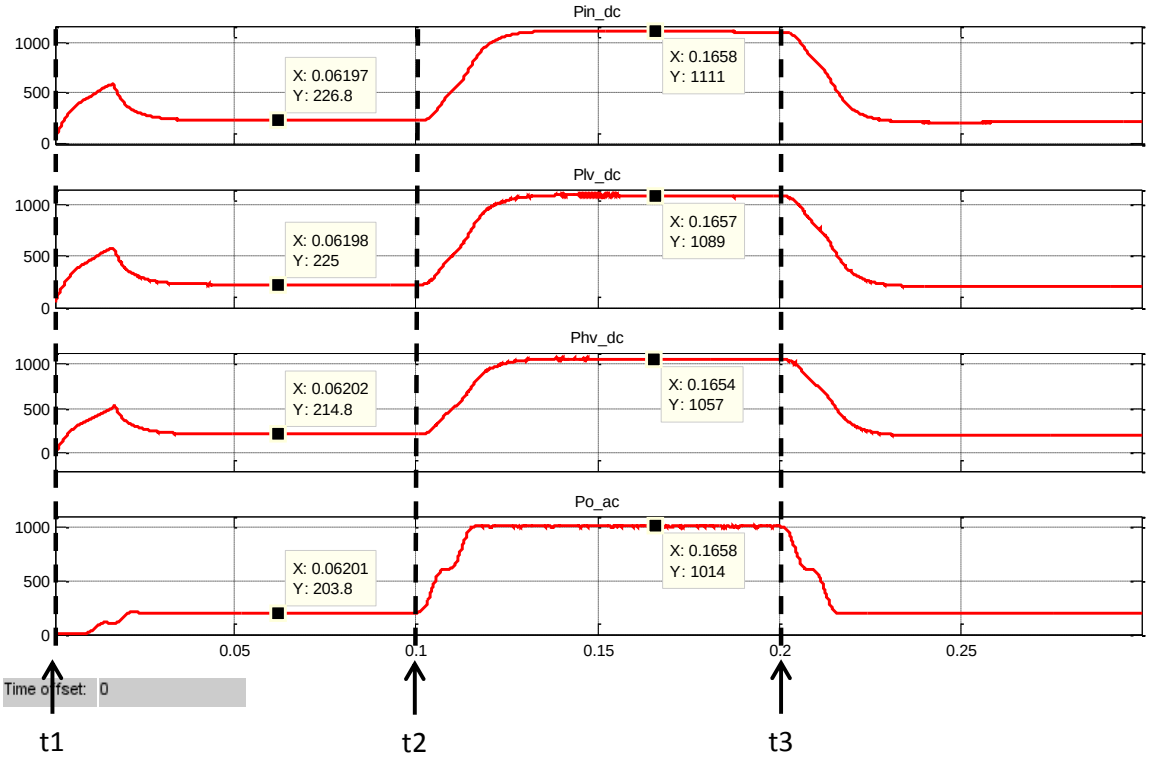

Fig. 4.3.4: Closed Loop PV Boost Converter with Full Inverter Simulation – Islanded - Power Waveforms

Since much of the individual efficiencies were quoted in [11], it is of interest to know the simulated efficiency of each operating mode over power. This simulation was ran plot efficiencies from 50 W to 1 kW (rated power for only the boost converter). These results are stated in Fig. 4.3.5. This graph will also summarize the results found for Fig. 4.3.4. It can be seen that at very low power levels the switching and conduction losses of various devices tend to dominate the total proportion of power that is being supplied. As the power levels are increased, this effect is reversed. From half to full rated power output from the boost converter, the total simulated efficiency from the total system is around 92 %.

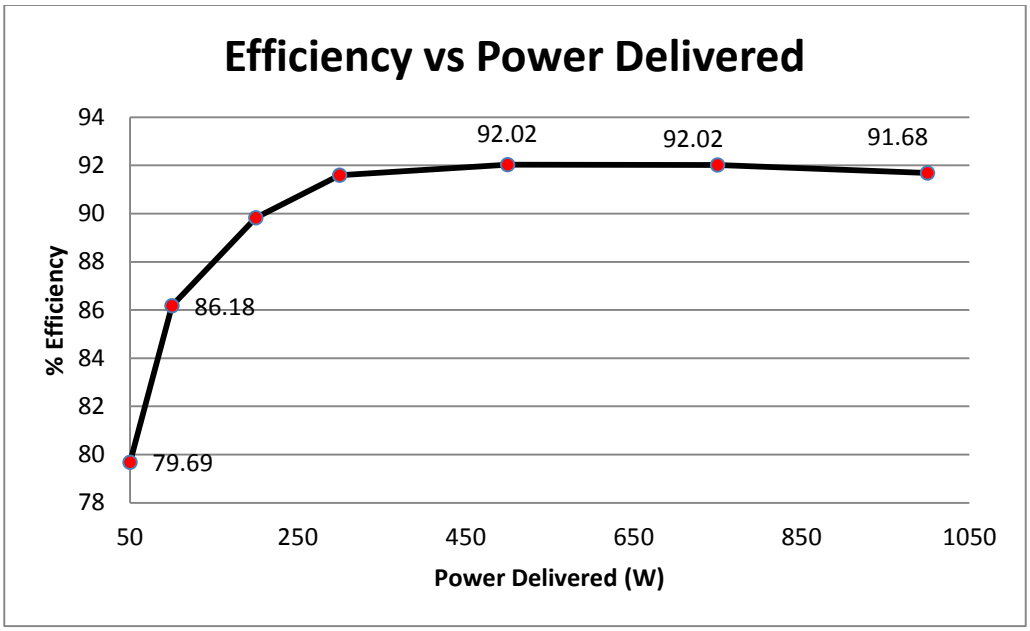

Fig. 4.3.5: Closed Loop PV Boost Converter with Full Inverter Simulation – Islanded - System Efficiency Over Power

4.3.2 *Grid-Connected Model*

This simulation will demonstrate the capability of the SGPN system to synchronize with the grid voltage and supply power in conjunction with the grid. A photovoltaic system does not possess any energy storage capability, so bi-directional power flow does not apply. Thus, only DC-AC power flow can be simulated.

The same simulation model as shown in Fig. 4.3.1 is used here where in island mode operation the grid source was disabled. An example scenario where this operation mode is relevant would be if the SGPN was islanded for an extended period of time such that the batteries were in a deeply discharged state and the grid source has just become available. In order for there to be solar power it is assumed to be sunny outside. It should be noted that in this situation normally the grid would be used to charge the batteries to a usable state. However, this operation mode is key to demonstrating the full functionality of the SGPN, so it is presented here.

For this simulation a 1 kW load is arbitrarily chosen. Note that any additional load above the rating of the PV converter would be served by the grid. After synchronizing with the grid, the inverter initially supplies 0 W, then 500 W, and finally the full load. Practically speaking, the SGPN would never be supplying no load while grid-connected. However, the simulation was set up in this manner to demonstrate AC power sharing while grid-connected, load transitions, and system operation stability during load transitions. These conditions are summarized below in Table 4.3.2.

Table 4.3.2: Closed Loop PV Boost Converter with Full Inverter Simulation - Grid-Connected - Simulation Timeline

Load Contribution by Source and Switching Times			
Time	**Load**	**Grid Power Supplied**	**SGPN Power Supplied**
$0 \leq t \leq 0.025$ s	1 kW	1 kW	0 W
$0.025 \leq t \leq 0.18$ s	1 kW	500 W	500 W
$0.18 \leq t \leq 0.35$ s	1 kW	0 W	1 kW

The DC waveforms for this simulation are shown below in Fig. 4.3.6 which include the LV & HV DC bus voltages, the PV input current, and the HV DC current. From $t_0 \leq t \leq t_1$ it can be seen that the current coming from the boost converter is 0 A indicating that it is supplying no power. The voltages across the output of the LV DC and HV DC link are non-zero which assumes there is some pre-charge across the capacitance. This was done to save some simulation time and cut down on the startup transients experienced through hard-starting the system.

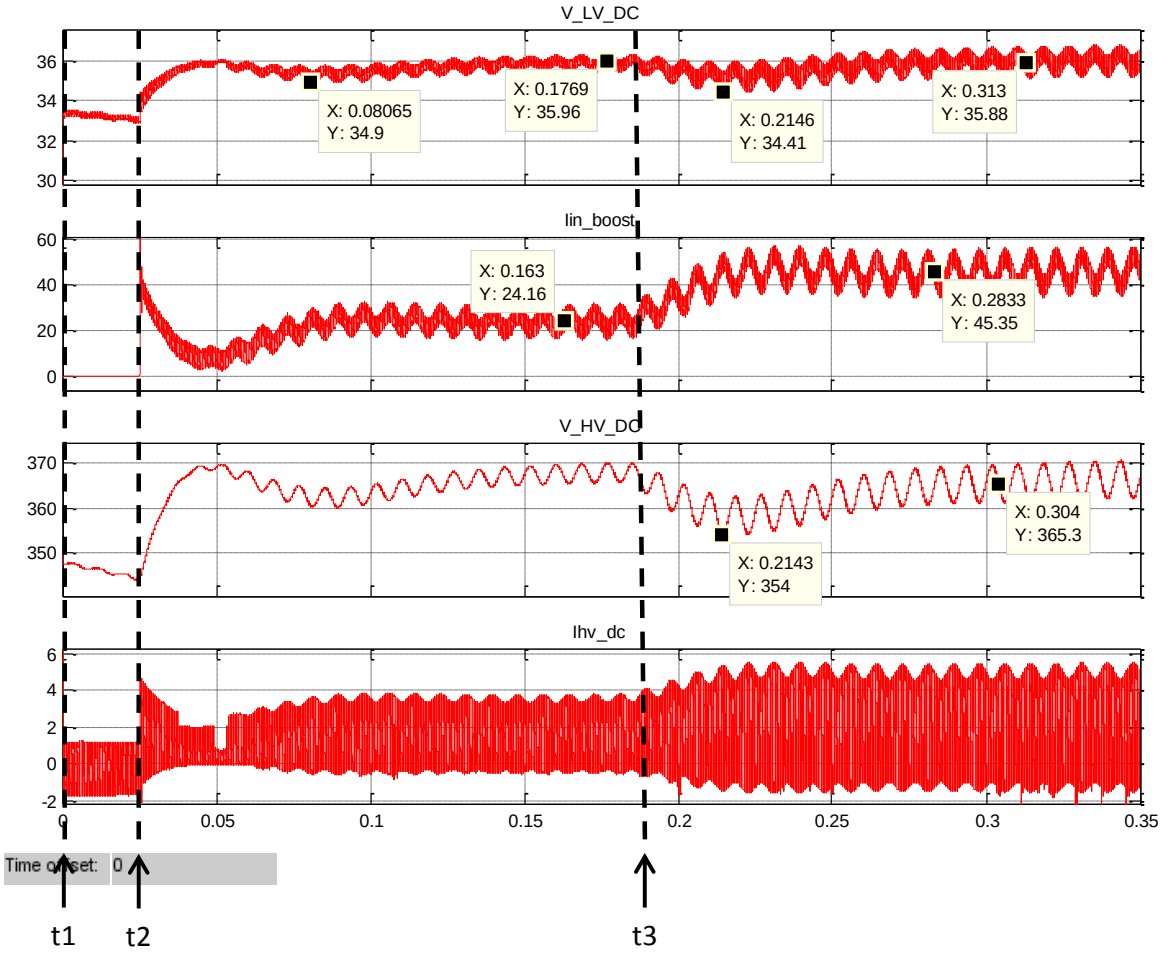

Fig. 4.3.6: Closed Loop PV Boost Converter with Full Inverter Simulation - Grid-Connected - DC Waveforms

At t_2 the boost converter is switched on and begins to supply power shown by the sudden increase in input current. The controller for the boost converter has relatively large gain parameters which help shorten system response time to counteract the effect of bulk capacitance in the system. However, one negative effect of this is that the system has more overshoot for errors between measured values and control targets. Therefore without a ramp function, the controller takes more time to reach steady state – hence the slower settling time.

At t_3 it can be seen that the boost converter supplies an increased current corresponding to the additional 500 W demanded from the SGPN.

Similar to the simulation in island mode, a performance comparison with specifications is given here for the DC-DC conversion stages. The simulated values are well within specifications and very similar to the performance in island mode operation. This illustrates that the controller developed for the boost converter can operate islanded and in conjunction with the grid. In addition, it can supply a constant power to the load or handle step load commands.

Table 4.3.3: Closed Loop PV Boost Converter with Full Inverter Simulation - Grid-Connected - DC System Performance

Boost +Full Inverter (Grid Connected): DC-DC Performance					
		Max. Spec		**Simulation Result**	
		Voltage	% rated	Voltage	% rated
Sag Voltage	LV DC link	3.6 V	10.0%	1.6 V	4.4%
	HV DC link	37.5 V	10.0%	21 V	5.6%
Ripple Voltage	LV DC link	1.8V	5.0%	1.56 V	4.3%
	HV DC link	37.5 V	10.0%	8.2 V	2.2%

Fig. 4.3.7 shows the simulated inverter voltage, inverter output current, and the current coming from the grid. At t_1 there is a small amount of inverter current. Notice that this current is exactly 90° out of phase with the inverter voltage which indicates a reactive power being delivered. This can be explained by the reactive power consumption by the LCL filter components. Meanwhile, the grid current is in phase with the inverter voltage which shows it is sourcing power to the load.

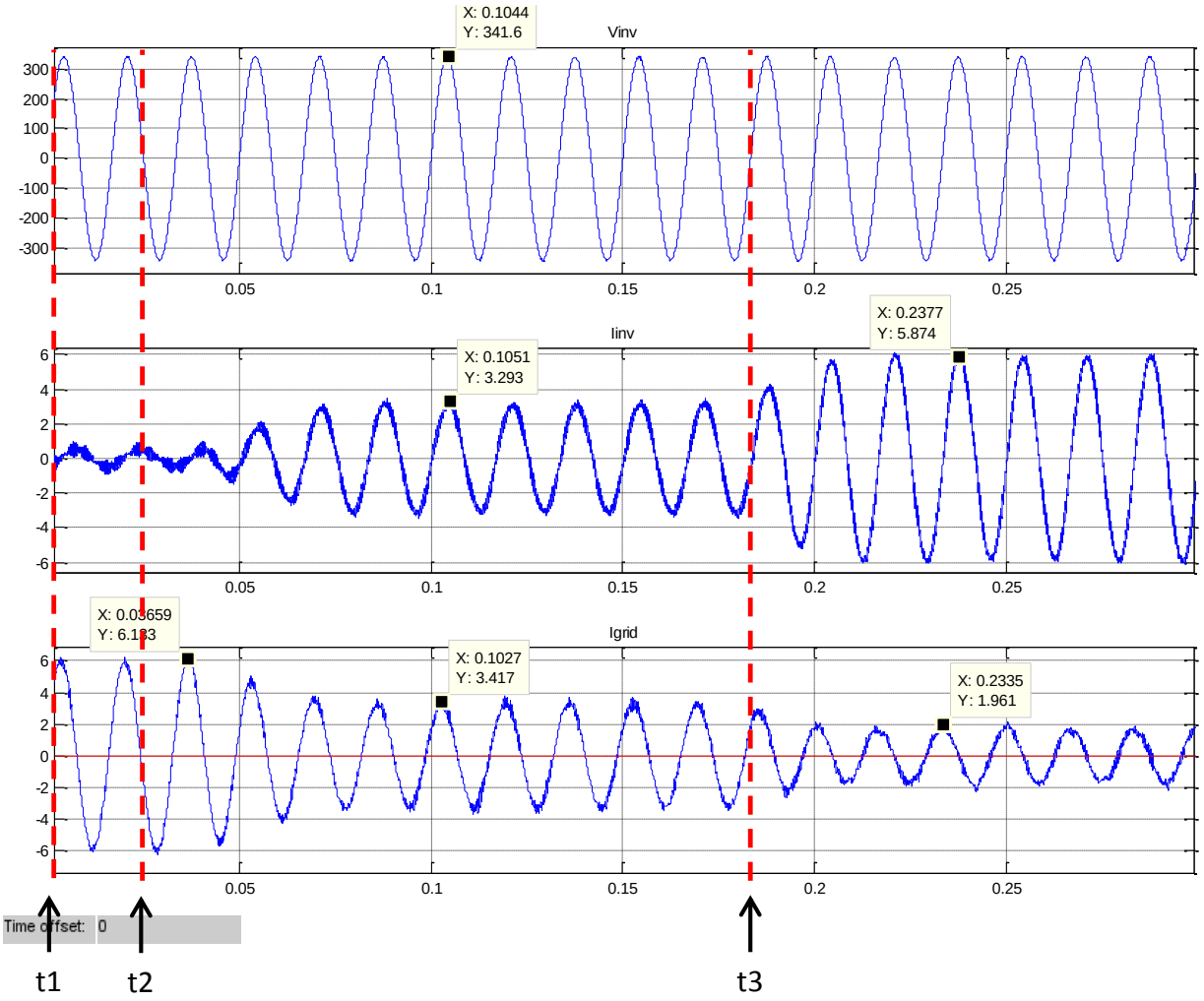

Fig. 4.3.7: Closed Loop PV Boost Converter with Full Inverter Simulation - Grid-Connected - AC Waveforms

At t_2 the inverter grid-connect and PV boost controllers are activated. Notice that the inverter takes almost 3 cycles, or around 58 ms to reach steady state. This is due to the fact that the inverter is syncing with the grid phase. The settling time of the inverter in addition to the boost converter causes a slow system startup on the order of ≈100 ms.

Finally at t_3 the SGPN is commanded to supply all load indicated by the increase in inverter current and decrease in grid current.

The central inverter controls the overall power flow from the SGPN by setting a DC current reference at the HV DC link proportional to the amount of power desired. A positive reference indicates DC-AC power flow while a negative reference indicates AC-DC power flow (battery charging). The DC power flow is regulated through a separate control network.

At transition t_2 and t_3, the DC current reference is updated to increase the power supplied by the SGPN. A diagram showing this control structure is shown below in Fig. 4.3.8. This emulates the system level controller decision about how much and which source the power is coming from. The hardware control layer's job is to respond to the dynamic references in which it is sent.

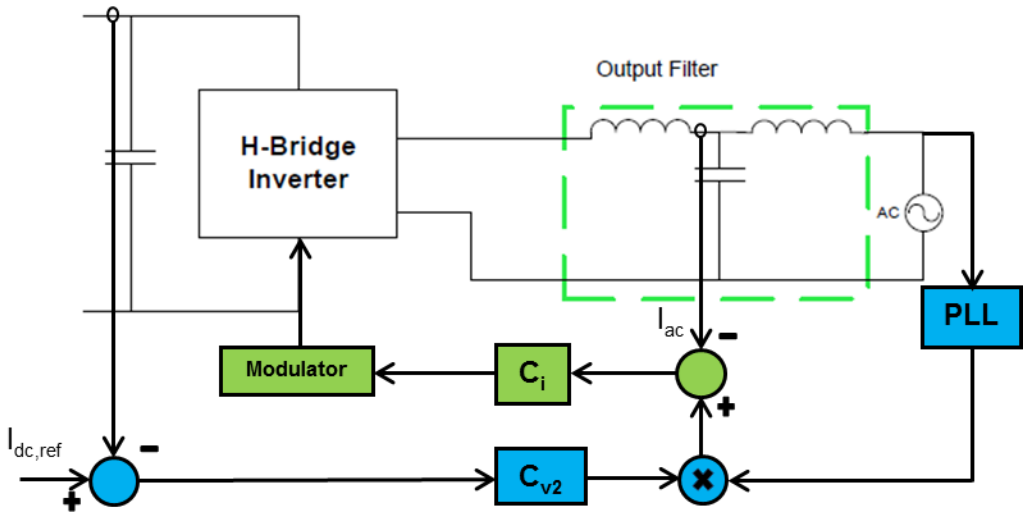

Fig. 4.3.8: Closed Loop PV Boost Converter with Full Inverter Simulation - Grid-Connected – SGPN Power Flow Control Structure [36]

In order to prove the PV converter is sending the correct amount of power as specified by the simulation times in Table 4.3.2 the DC and AC power plots are shown below in Fig. 4.3.9 and Fig. 4.3.10. Before transition time t_1 it can be seen that all DC power is 0 W. At t_2 once

steady state is reached the DC power is being sent to the load. Finally, at t_3 the step load command is accepted and more DC power is sent to the load.

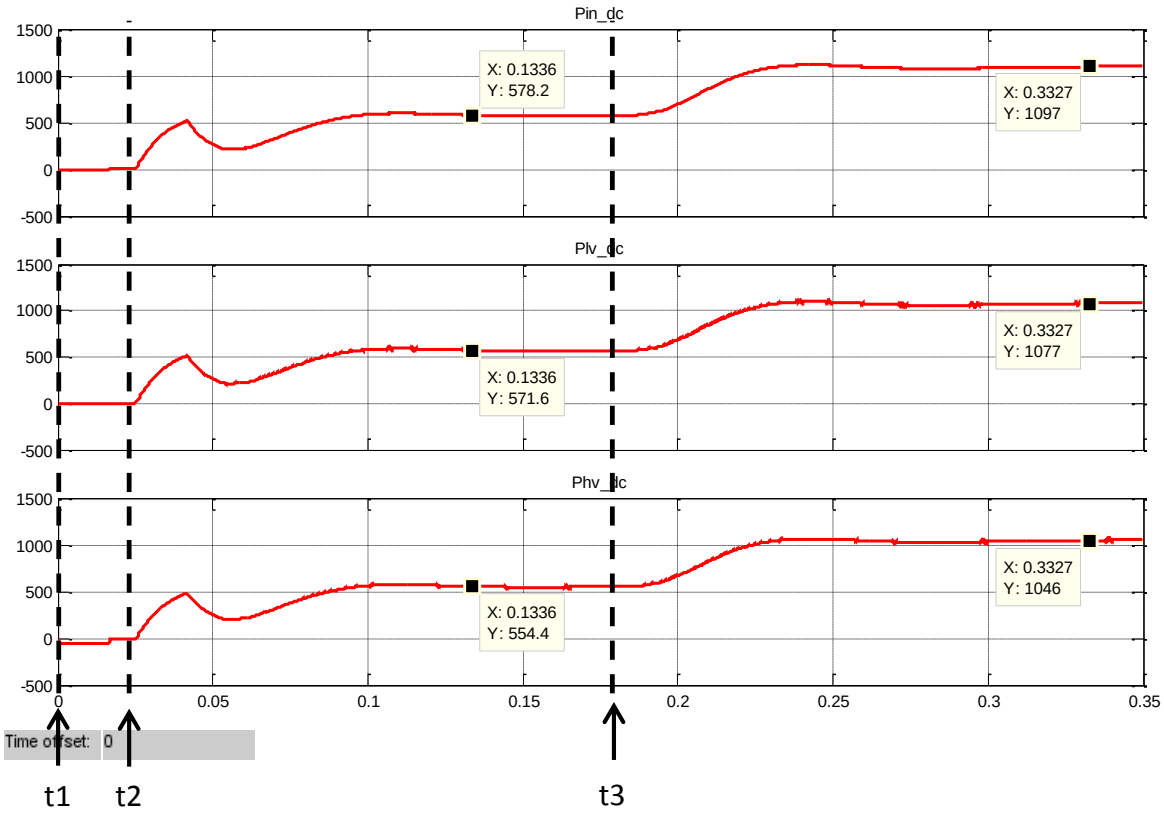

Fig. 4.3.9: Closed Loop PV Boost Converter with Full Inverter Simulation - Grid-Connected – DC Power Waveforms

Similarly, Fig. 4.3.10 shows the power coming from the SGPN, the grid power, and the load power consumed. As can be seen the load is a constant power draw of close to 1 kW. At t_1 the grid supplies the load after a short "ramp" time. In practice the grid would supply power to the load almost instantaneously. At t_2 the SGPN supplies half the load. Finally, at t_3 the SGPN is supplying the full load while the grid power is effectively 0 W.

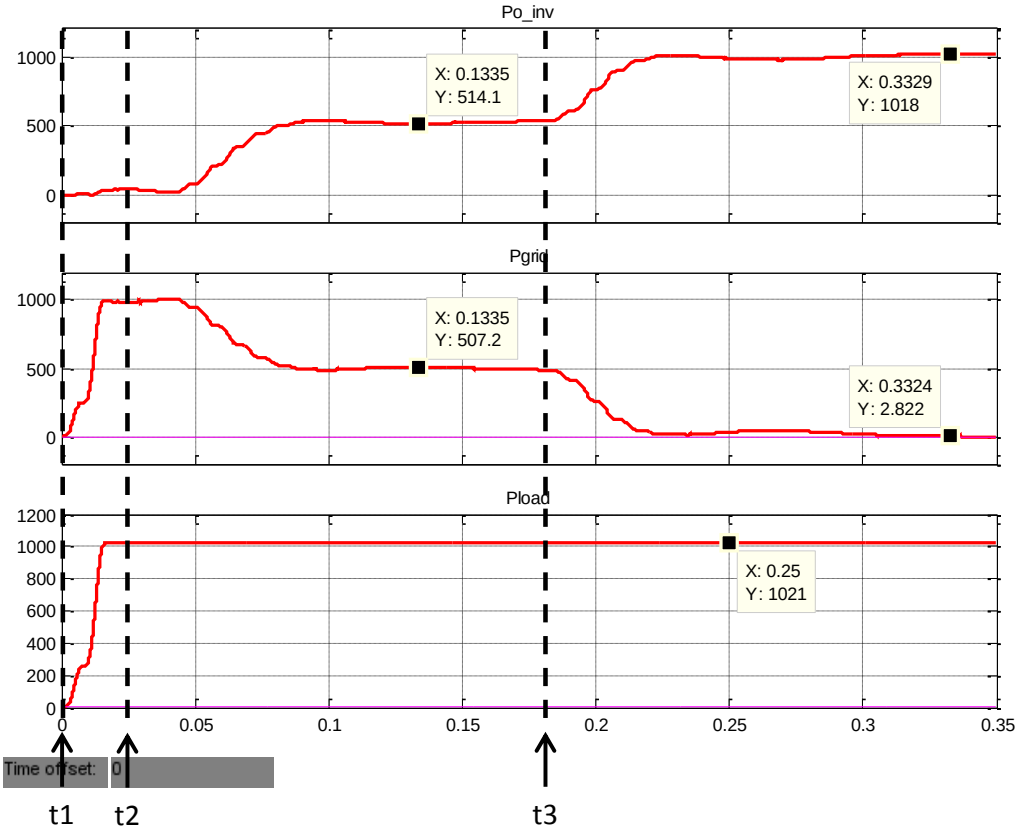

Fig. 4.3.10: Closed Loop PV Boost Converter with Full Inverter Simulation - Grid-Connected - AC Power Waveforms

The efficiency under this operating mode is 92.7%, which is comparable to islanded operation. This is expected since the losses of the SGPN should be independent of operating mode. The SGPN was simulated over power to show the effects of switching and conduction losses vs. load power. This can be seen below in Fig. 4.3.11. The efficiency does increase slightly from 200 W to 1 kW which is due to two things: 1) the switching losses are a smaller percentage of the load power at 1 kW compared to 200 W. 2) the conduction losses increase with increased load power. The net result is a slight increase in efficiency because the effect of the switching losses is less predominant than the conduction loss effect.

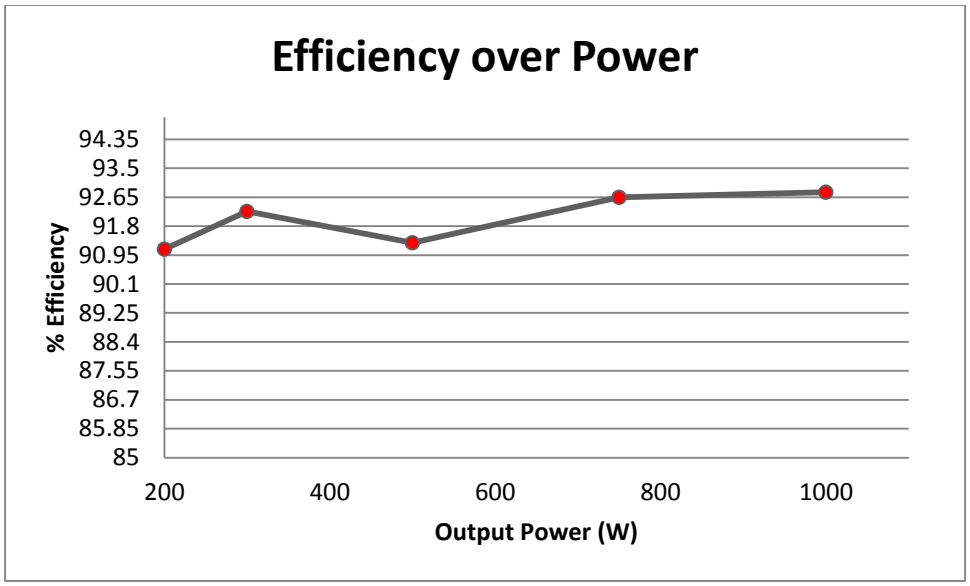

Fig. 4.3.11: Closed Loop PV Boost Converter with Full Inverter Simulation - Grid-Connected - System Efficiency Over Power

4.4 Closed Loop Battery Charge/Discharge Converter with Full Inverter

This section presents the closed loop simulation results of the battery charge/discharge converter, full bridge DC-DC converter, and the H-bridge inverter in islanded and grid-connected mode. Fig. 4.4.1 shows the schematic layout of the simulation. From left to right is the battery charge/discharge converter, the full bridge DC-DC converter, and the H-bridge inverter. To illustrate the figure all PWM outputs are indicated in red, the controller blocks are light blue, and measurements are green.

For the purposes of verifying controller design and system level operation, the battery is considered to be in a healthy state of charge at 90%, which yields a nominal voltage close to 24 V. The battery converter in discharge mode boosts the input to the 36 V at the LV DC bus, which is then boosted to $\approx 385\ V\ DC_{nominal}$ by the FB DC-DC converter. This voltage is then transformed into the 240 V_{AC_RMS} residential AC bus voltage.

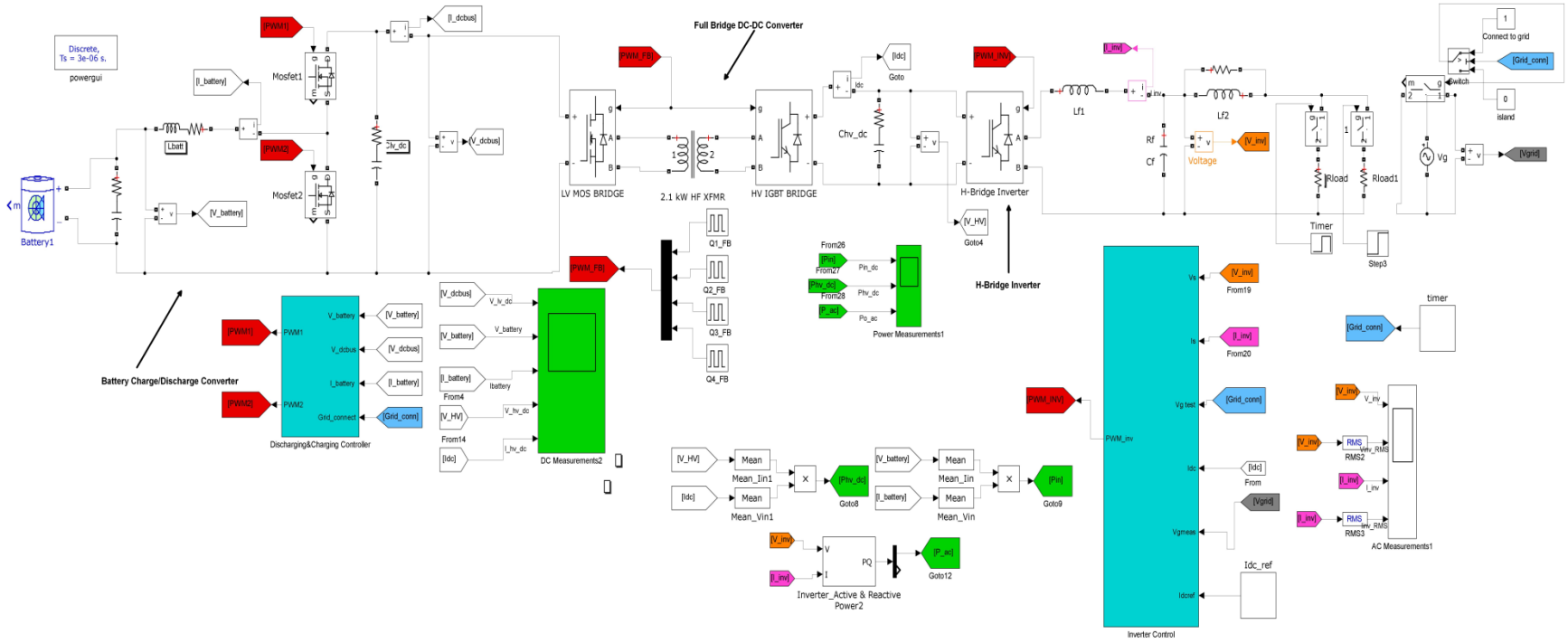

Fig. 4.4.2: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Simulation Model

4.4.1 *Island Model*

In order to demonstrate controller stability over a wide power range and verify step loading, the battery converter is loaded at 50 W, then 1 kW, then back to 50 W. The load changes are summarized below. Theoretically the PV boost converter and battery charge/discharge converter (in discharge mode) are identical in operation (both boost converters). However, there are certain parameter differences between the converters that were modeled into the simulation in order to simulate a more realistic model of the prototype hardware. For example, the characteristics of the standalone diode used in the PV boost converter are different than the anti-parallel diode used in the high side switch of the battery converter. Similarly, an input capacitive filter is placed in shunt across the terminals of the battery to stabilize any low frequency ripple voltage that would degrade battery life and cause heating. This was not present for the PV boost converter.

$$\begin{cases} 0 \leq t \leq 0.1\ s \rightarrow 50\ W\ LOAD \\ 0.1 \leq t \leq 0.2\ s \rightarrow 1\ kW\ LOAD \\ 0.2 \leq t \leq 0.3\ s \rightarrow 50\ W\ LOAD \end{cases}$$

It was mentioned in section 4.3.1 that an input power of 200 W was required to keep the boost converter from entering discontinuous mode operation. However, through simulation it was seen that the battery converter in island mode was able to serve a load as low as 50 W without entering discontinuous mode. By stabilizing the battery input voltage, the battery current experiences less low frequency ripple and therefore can operate at lower power levels without entering discontinuous mode.

The DC waveforms for the above mentioned simulation are shown below in Fig. 4.4.3. From $0 \leq t \leq 0.1\ s$, the output load power is 50 W, at $t = 0.1\ s$ a parallel resistor is switched on increasing the load from 50 to 1000 W. Finally at $t = 0.2\ s$ the load is decreased to the

original 50 W. This simulation demonstrates the ability of the battery converter control to react to a drastic step load changes within the home.

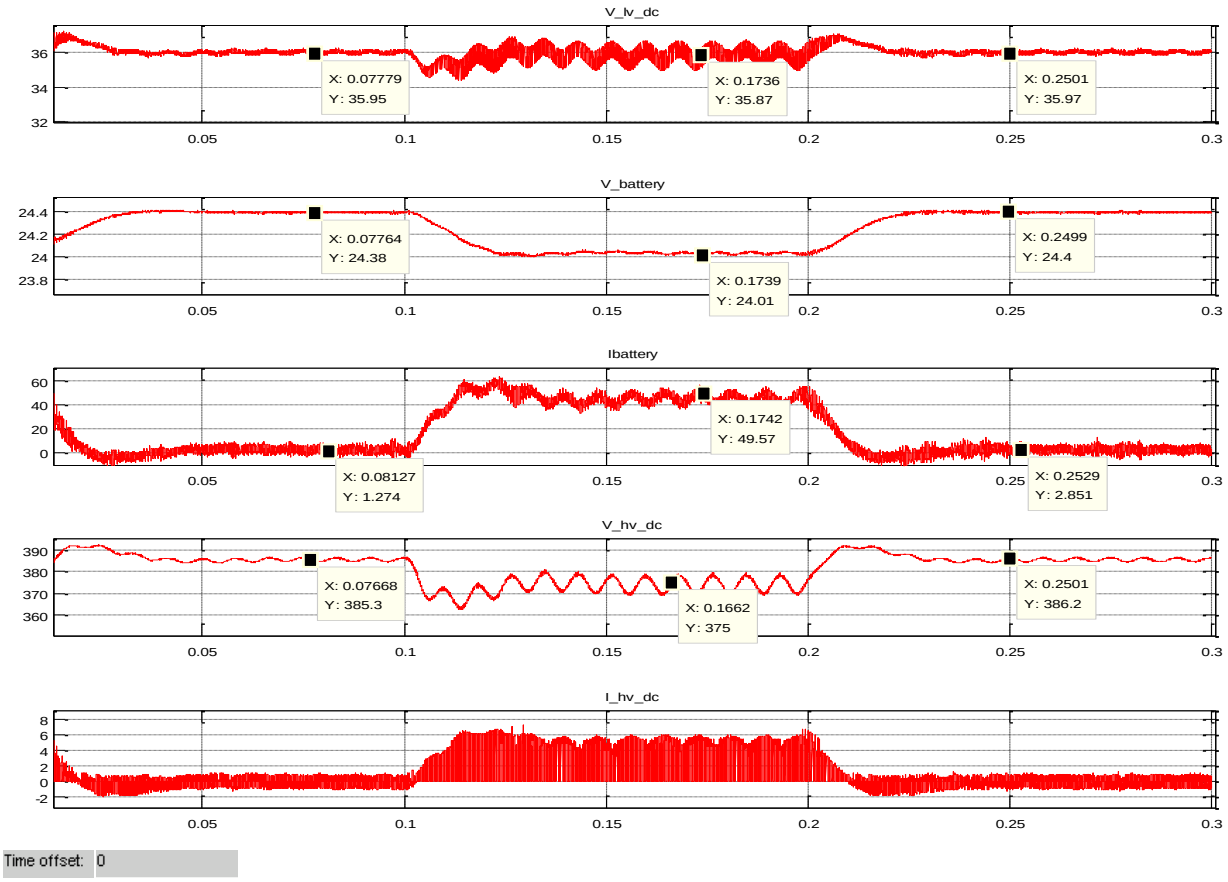

Fig. 4.4.3: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - DC Waveforms

The LV DC bus shows a stable voltage, very close to the desired voltage of 36 V throughout the load changes. Between $0.1 \leq t \leq 0.2\ s$ the 120 Hz ripple is increased with the increased load as well as the input battery current, which is expected. Table 4.4.1 summarizes the ripple performance of the DC system under maximum load. The voltage sag is defined as the lowest point at which the voltages reach during the step load transition from the average value. The voltage ripple is defined as the ripple measured around the average DC voltage under full load. It is recognized that since the full bridge converter is unregulated, there can be large

enough variations in the average DC voltage to cause unreliable operation. However, from Table 4.4.1 it can be seen that the tight regulation of the LV DC bus is sufficient to keep the voltage sage and ripple within specified limits. The DC performance exceeds allowable specifications in all areas.

Table 4.4.1: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - DC System Performance

Battery Charge/Discharge Converter w/ Full Inverter: DC System Performance					
		Spec.		**Simulated**	
		Voltage	% rated	Voltage	% rated
Voltage Sag	LV DC Bus	3.6 V	10%	1.6 V	4.4 %
	HV DC Bus	38.5 V	10%	22.5 V	6 %
Voltage Ripple	LV DC Bus	1.8V	5%	1.6 V	4.4 %
	HV DC Bus	38.5 V	10%	10.1 V	2.7 %

The AC waveforms for this simulation are shown below in Fig. 4.4.4 which include the filtered inverter output voltage, the RMS value of the inverter voltage, filtered inverter current, and RMS value of the inverter current. The inverter voltage and current are shown to have very stable output throughout the loading changes. The inverter voltage has an RMS value of 241.6 V, 241.1 V, and 241.6 V respectively which corresponds to an error of 0.66 %, 0.46 %, and 0.66 % from the nominal output of 240 V_{RMS}. This demonstrates a good control design with very minimal steady state error capable of handling large load swings.

The inverter current can be seen at $t = 0.1s$ to increase with the step load condition to 1000 W, while at $t = 0.2\ s$ it decreases to the original amplitude with the decreased step load condition.

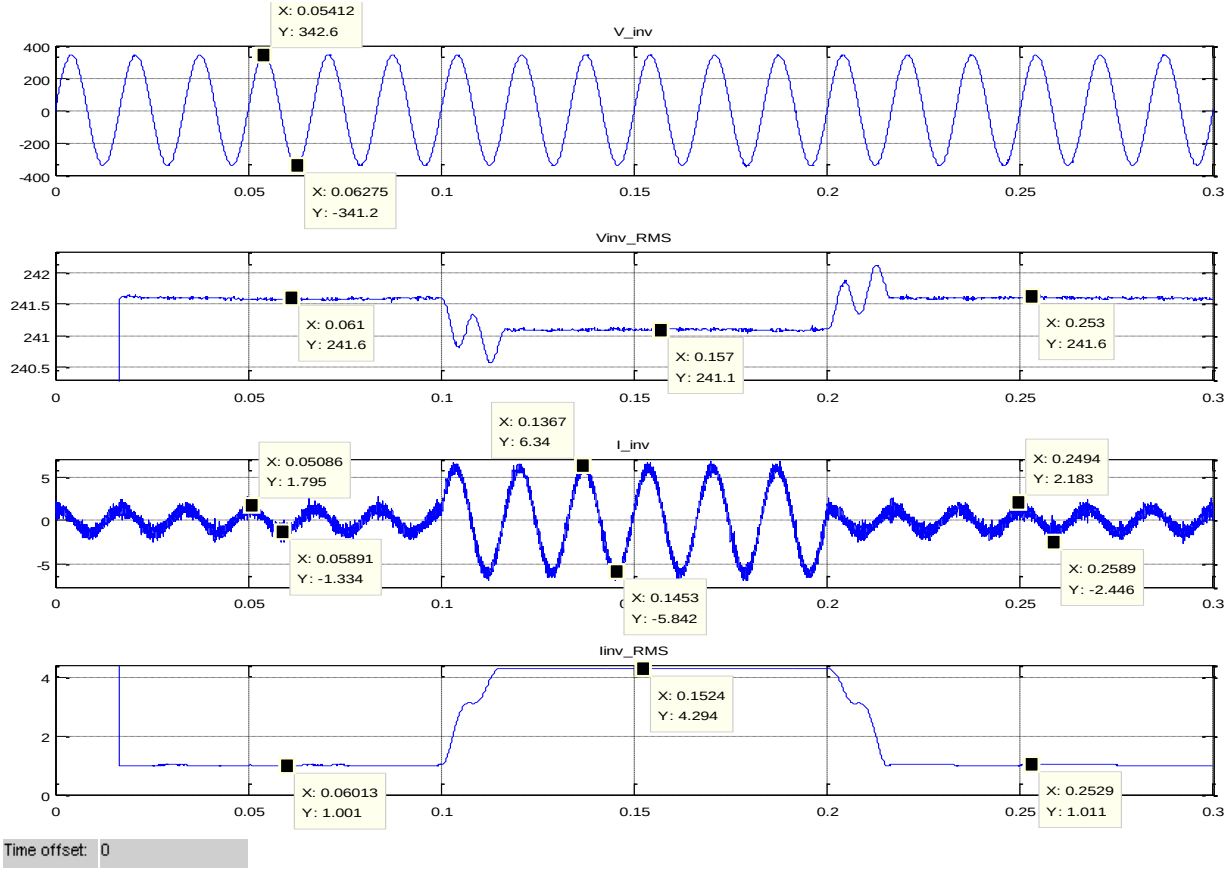

Fig. 4.4.4: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - AC Waveforms

The average power waveforms are shown below in Fig. 4.4.5. These include the input power drawn from the battery, power across the HV DC link, and the output AC power served to the load which shows the power loss from input – output. It can be seen through the pre-defined load transitions, the SGPN supplies approximately 50 W – 1000 W – 50 W.

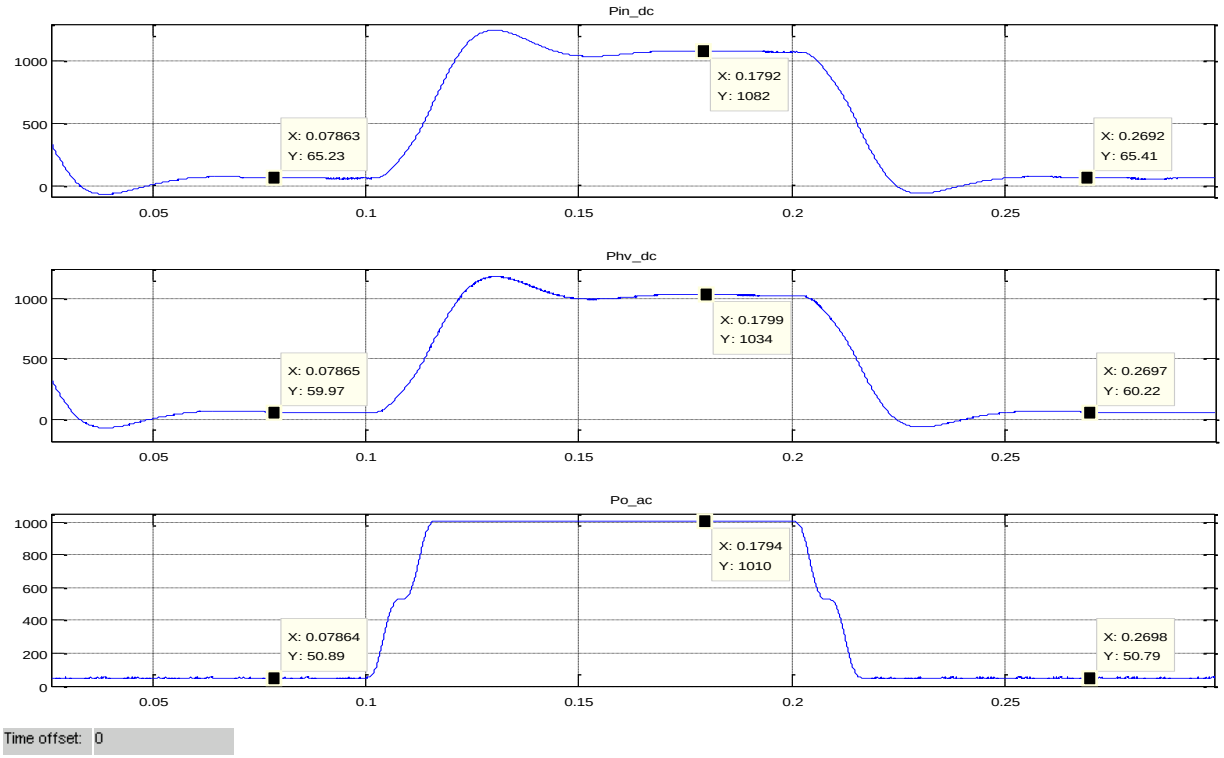

Fig. 4.4.5: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Power Waveforms

The loss summary is presented in Table 4.4.2. During low power operation, the losses tend to dominate a larger percentage of the total power, while at higher powers, this percentage is less. This explains the low efficiency under the 50 W load condition.

Table 4.4.2: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Simulated Efficiency By Stage

Simulated Efficiency Summary		
Nominal Load Wattage	50 W	1 kW
DC-DC Efficiency (%)	90.5	95.56
DC-AC Efficiency (%)	84.85	97.68
Total Efficiency (%)	76.79	93.34

Similar to the PV boost converter, the battery converter was simulated across a wide range of power levels as shown in Fig. 4.4.6. It can be seen that the efficiency is very low at low

powers as expected. The peak is right around 95% at 500 W, while at the rated power of the battery converter, the efficiency decreases slightly to around 93%. This is due to conduction losses (I^2R) increasing with increased current.

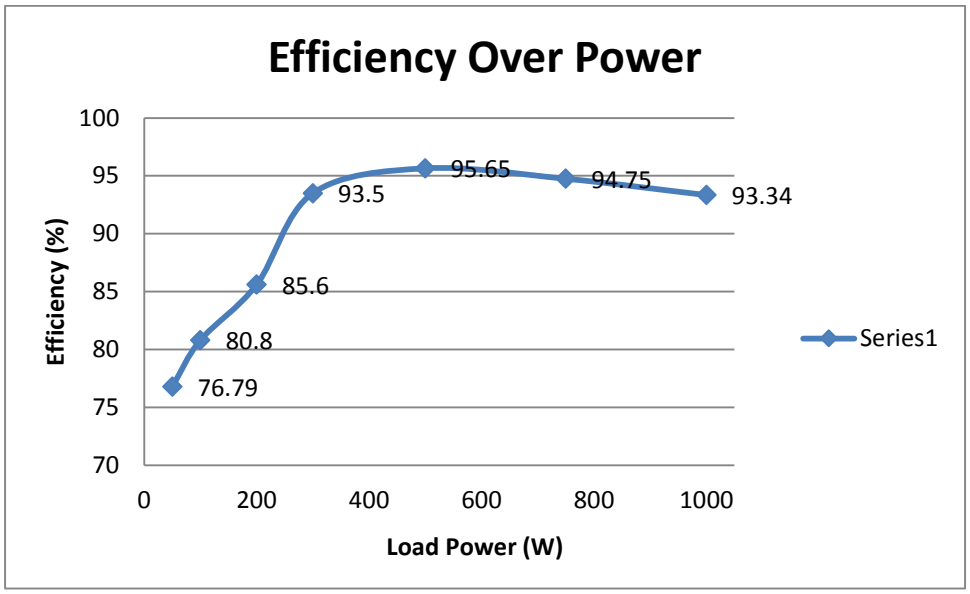

Fig. 4.4.6: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - System Efficiency Over Power

4.4.1.1 THD Analysis

This section presents the THD analysis of the H-bridge inverter in island mode. It is important to maintain an acceptable level of power quality input to the home when the grid source is not available. Injecting a large amount of harmonics into home appliances can cause heating and could potentially damage some equipment.

This analysis was done for the above simulation in which the load is stepped from 50 W at 0.1 s to 1 kW, and back to 50 W at 0.2 s. The voltage was shown to have negligible differences in THD between the load changes, so only one section of the waveform is analyzed. Fig. 4.4.7 shows the screenshot from the FFT Analysis tool in Simulink for the filtered inverter

voltage. It can be seen that the THD for the voltage is 0.71%. This satisfies IEEE 1547, which for interconnection with the grid allows for 1% THD in the voltage.

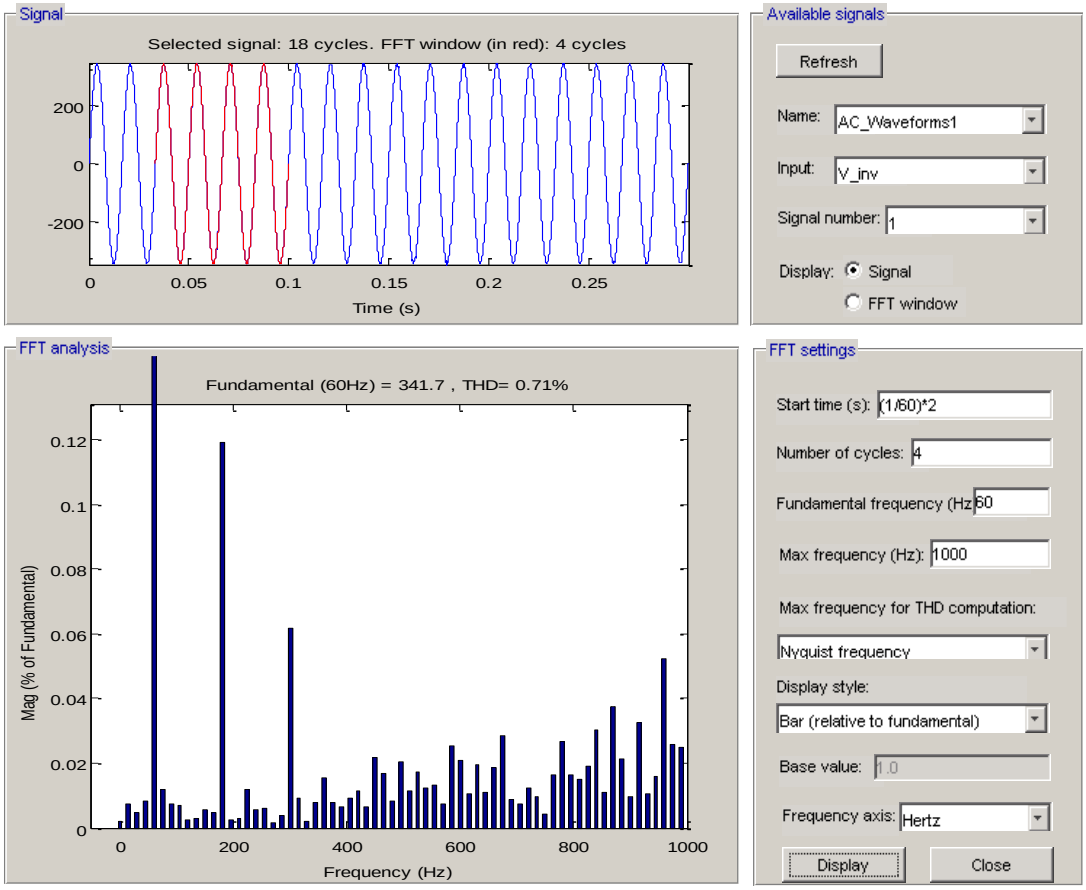

Fig. 4.4.7: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Voltage FFT

The next step is to analyze the current THD of the inverter. In order to not duplicate results, only 1 analysis of the 50 W loads is shown. Fig. 4.4.8 shows the FFT output of the filtered inverter current. It can be seen that for the very light loading the THD is almost 39%. This is obviously an unacceptable performance. IEEE 1547 requires a THD of the current to be less than 5%. This was a known problem as pointed out in [11]. It will be discussed further in CHAPTER 6 .

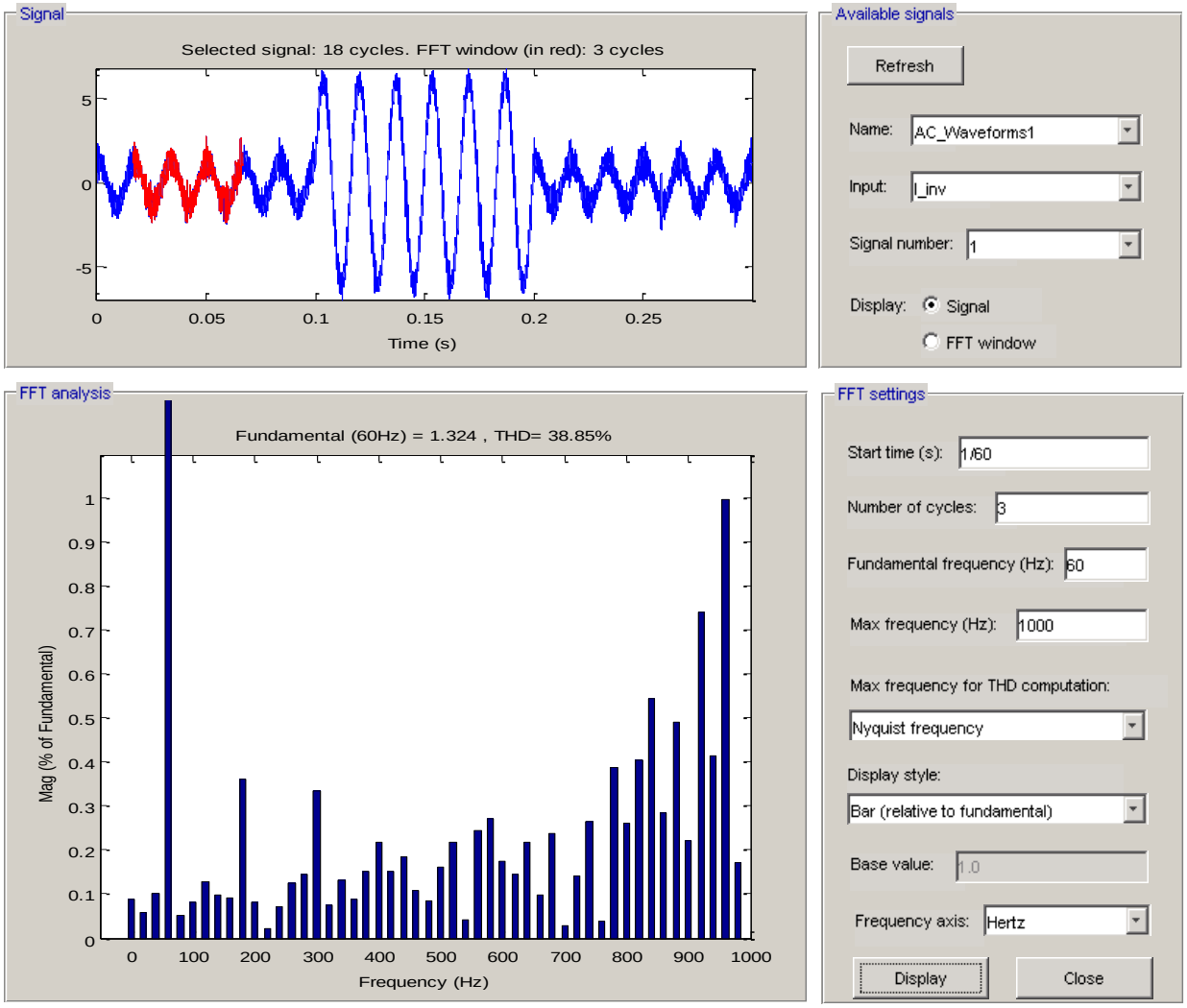

Fig. 4.4.8: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Low Wattage Current FFT

The THD analysis of the inverter current under a 1 kW load is shown below in Fig. 4.4.9. The THD under this loading is 7.84% which is still over the acceptable limit, but a much better performance compared to the 50 W load. This can be explained by the fact that the total harmonic contribution compared to the fundamental is inherently lower at higher currents. Even with the improved performance, the design must be improved to satisfy IEEE 1547 requirements at all power levels.

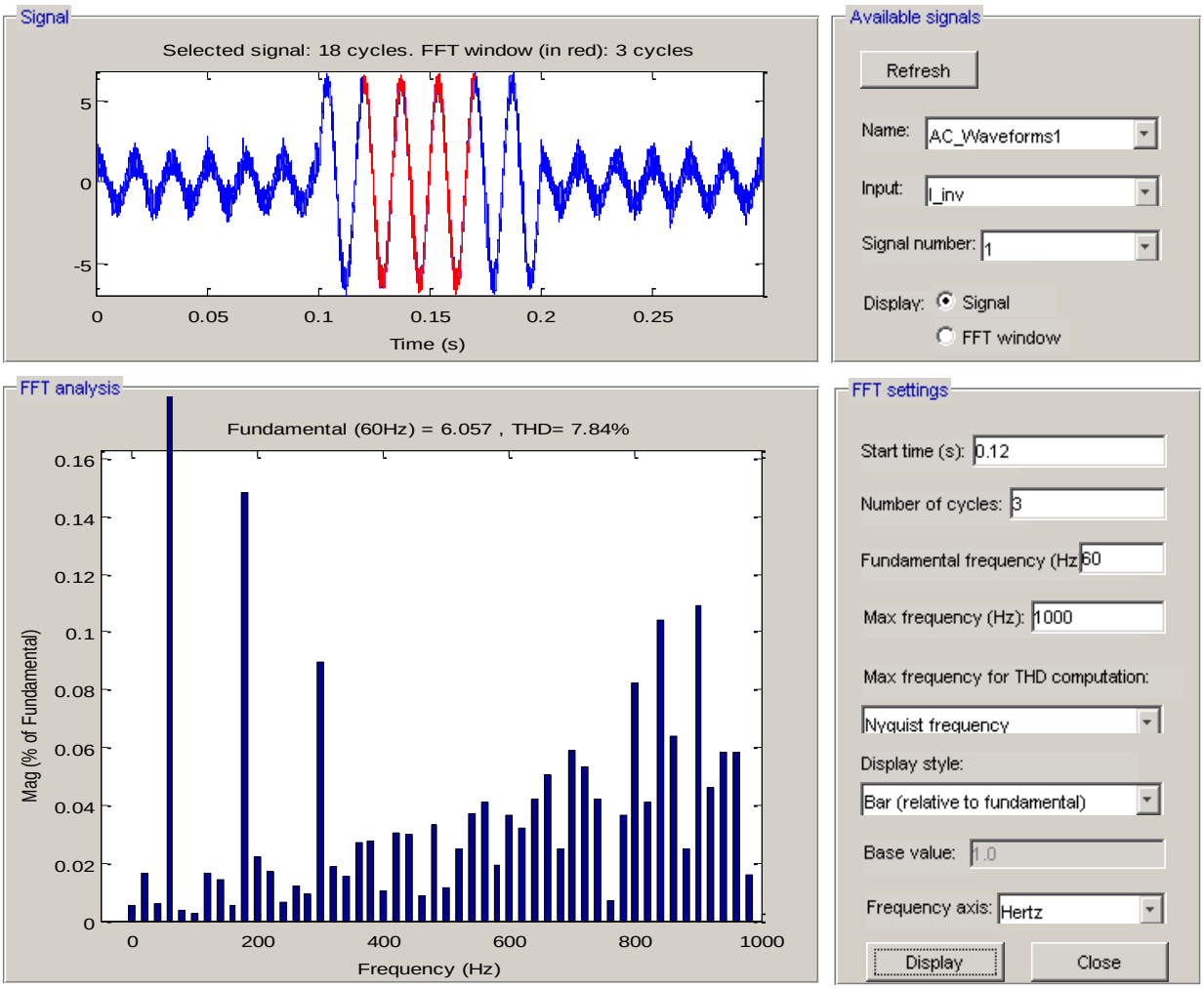

Fig. 4.4.9: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - High Wattage Current FFT

4.4.2 *Grid Connected Model*

This section presents the simulation results for the battery charge/discharge converter with the full inverter grid-connected. Section 4.4.2.1 and 4.4.2.2 demonstrate stable results for DC-AC power flow through load changes, load sharing with the electric grid, and pushing energy onto the grid.

4.4.2.1 DC-AC Power Flow (Battery Discharge to Load)

In order to concisely demonstrate the closed loop stability of the battery charge/discharge converter in grid-connected mode the simulation below shows the battery converter operating serving no load ($0 \leq t \leq 0.1s$), sharing load with the grid ($0.1s \leq t \leq 0.2s$), and supplying full rated load from the batteries ($0.2s \leq t \leq 0.3s$). This simulation assumes a constant 1 kW load at the AC bus. The summary of loading on the batteries and electric grid by simulation time is shown in Table 4.4.3.

Table 4.4.3: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Simulation Timeline

Load Contribution by Source and Switching Times			
Time	**Load**	**Grid Power Supplied**	**SGPN Power Supplied**
$0 \leq t \leq 0.1s$	1 kW	1 kW	0 W
$0.1 \leq t \leq 0.2s$	1 kW	500 W	500 W
$0.2 \leq t \leq 0.3s$	1 kW	0 W	1 kW

At the simulation start time, the battery converter is assumed to have synced with the grid voltage and started grid-connected. Fig. 4.4.10 shows the DC waveforms for this simulation. At time $t = 0\ s$ it can be seen there are startup transients that result in high input currents and a LV DC voltage overshoot. This was seen as well in island mode which can be eliminated by implementing a startup sequence for the system, rather than the "hard start" in simulation. This will be discussed in 5.6.2.

It can be seen that the LV DC bus is a stable average value of around 36 V throughout all load transitions. At $t = 0.1\ s$ the battery current increases as it begins to share the load with the grid. As has been discussed, the 120 Hz ripple voltage can be seen on the DC system from the inverter operation which increases as the load served increases. Similarly at $t = 0.2\ s$ the battery increases to its rated load current as it now serves 100% of the load. At $t = 0.1\ s$ and $t = 0.2\ s$

the battery voltage decreases slightly with each increased load transition which is expected as current draw is increased. This simulation timeframe is too short to exhibit this behavior, but assuming a constant load, the battery voltage will decrease linearly overtime as it continues to discharge.

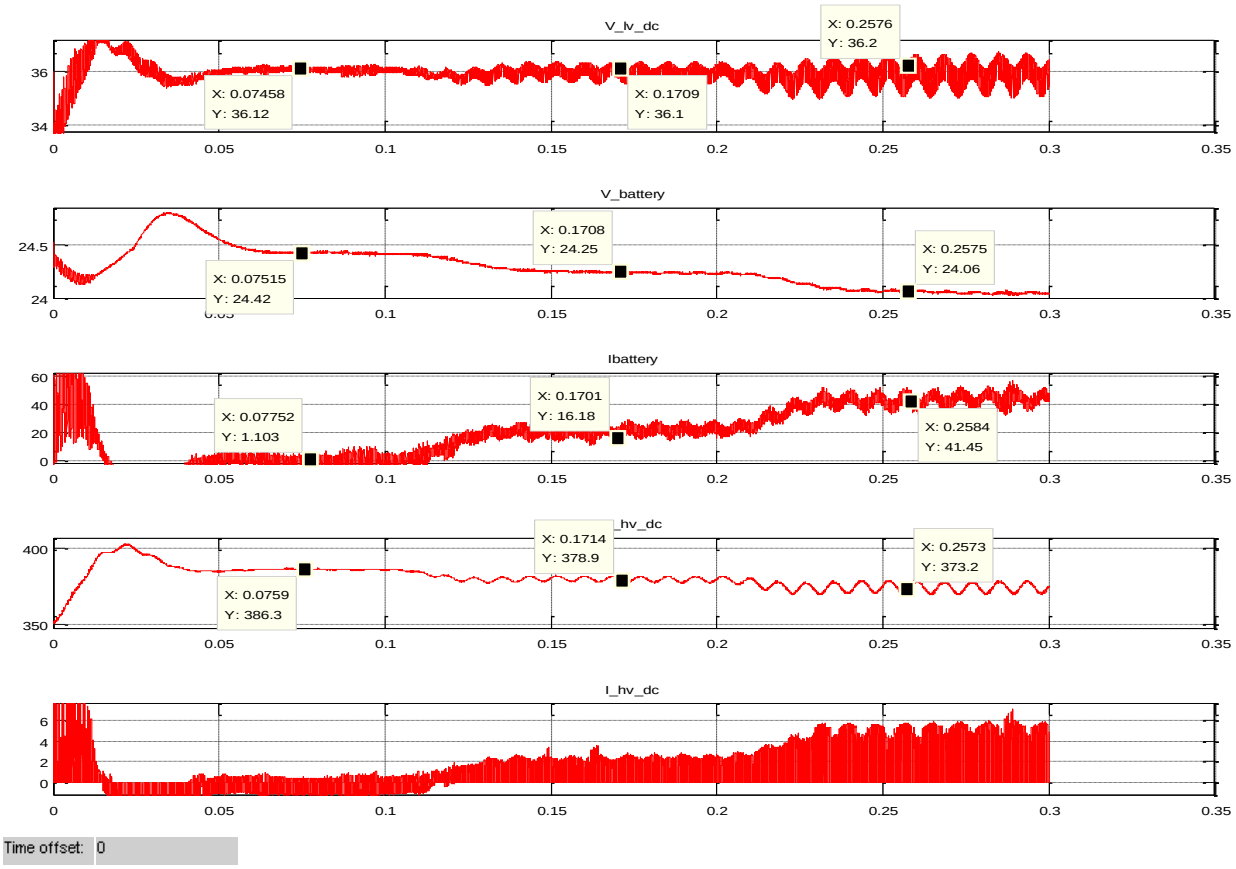

Fig. 4.4.10: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - DC Waveforms

The results for the DC system simulation performance under full load do not change much from island to grid connected model, but it can be seen that the voltage sag and ripple performance on the HV DC bus is marginally improved. The simulated performance has exceeded specifications which are summarized in Table 4.4.4.

Table 4.4.4: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - DC System Performance

Battery Charge/Discharge Converter w/ Full Inverter: DC System Performance					
		Spec.		**Simulated**	
		Voltage	% rated	Voltage	% rated
Voltage Sag	LV DC Bus	3.6 V	10%	1.6 V	4.4 %
	HV DC Bus	38.5 V	10%	14.0 V	3.6 %
Voltage Ripple	LV DC Bus	1.8V	5%	1.6 V	4.4 %
	HV DC Bus	38.5 V	10%	8.5 V	2.2 %

The AC waveforms for the same simulation are shown below in Fig. 4.4.11 which include the inverter voltage, inverter current, and grid current. The inverter voltage is stable through all load changes. The grid source is modeled as an ideal AC voltage source; therefore the inverter voltage should have very minor distortion. At $t = 0\ s$ the same startup transients experience on the DC system are apparent in the AC system as well. At $(t \approx t_0)$ the grid current is in phase with the inverter voltage, thus sourcing power to the load. The minimum of the inverter current is 90° out of phase with the voltage, thus serving reactive power. At $(t \approx t_1)$ the inverter voltage, inverter current, and grid current are in phase and demonstrating that they are sharing the load. Finally at $(t \approx t_2)$ the inverter current is in phase with the voltage sourcing power. The grid current is now non-zero and 90° out of phase with the voltage sourcing the reactive power to the filter.

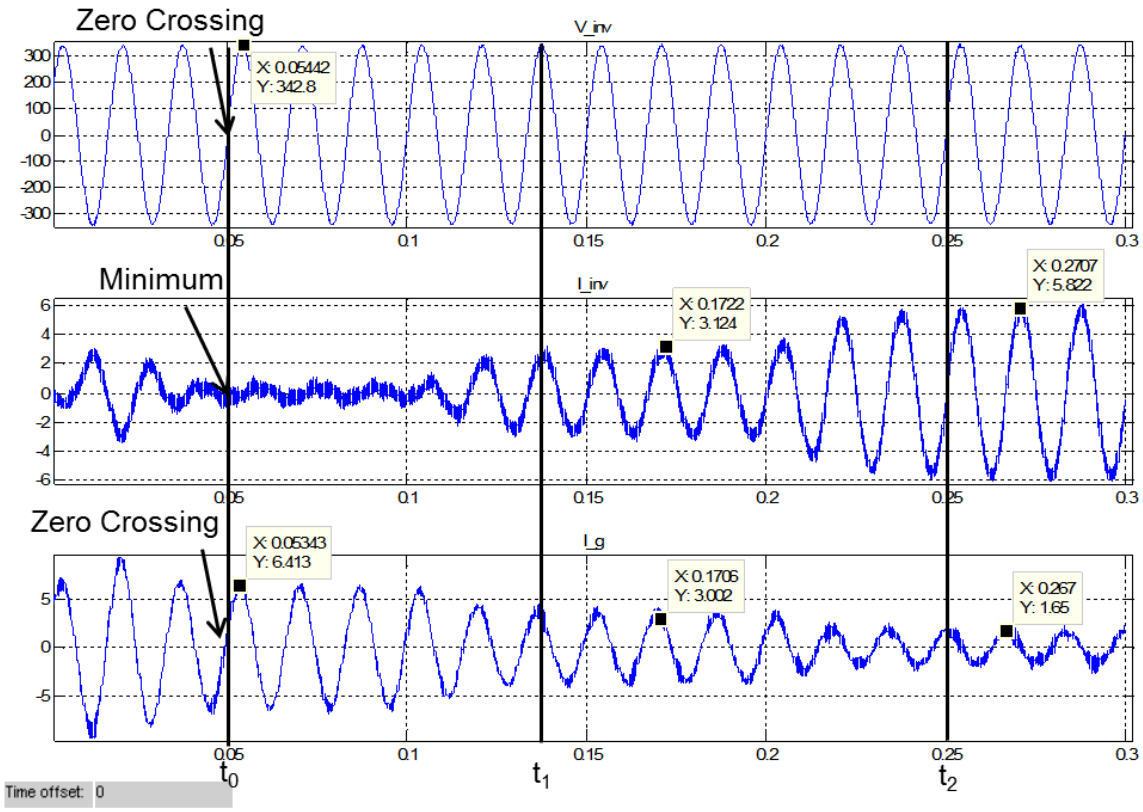

Fig. 4.4.11: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - AC Waveforms

The inverter output voltage was simulated to be 242.4 V_{RMS}, which corresponds to an error of 1% from the nominal voltage. While the grid source was programmed to be 240 V_{RMS} signal, it can be seen the inverter tracks the grid source well, but with slight distortion due to some ripple voltage at the peaks. This is shown graphically in Fig. 4.4.12, where the inverter voltage is in red and the grid source is in blue.

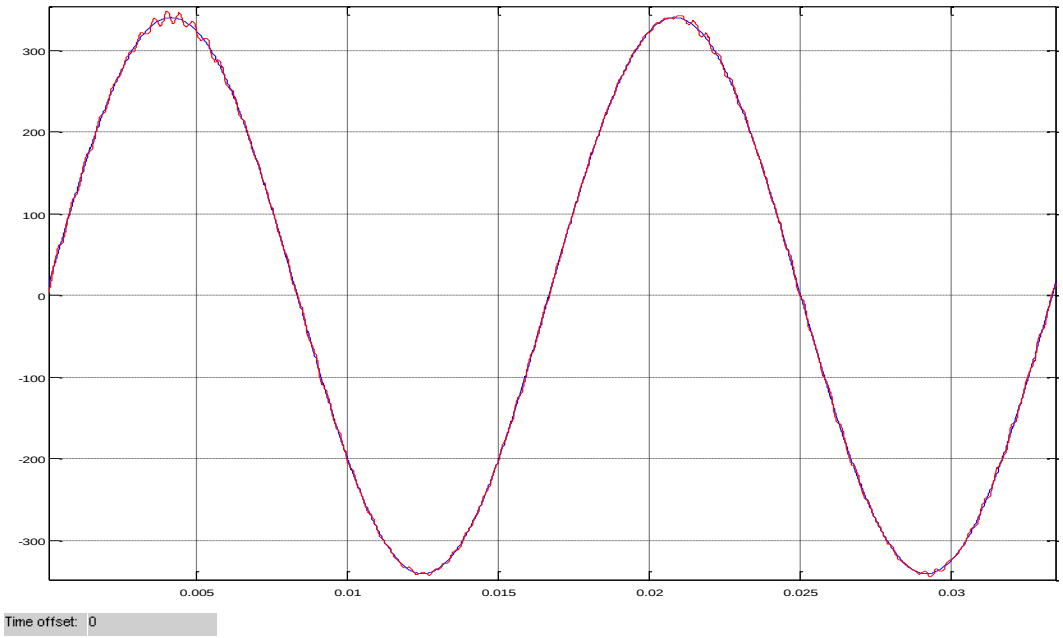

Fig. 4.4.12: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Grid and Inverter Voltage Comparison

The averaged input DC power, AC inverter power, and grid power are shown below in Fig. 4.4.13 for this simulation. As with the DC and AC waveforms, the input transients can be seen at the beginning of the simulation. The grid supplies the load power of 1 kW until $t = 0.1\ s$ which is verified by the zero input and inverter output power. Between $0.1s\ \leq t \leq 0.2\ s$ the output load is shared between the grid and batteries by roughly half. This demonstrates the stability of the battery converter and inverter grid-connect controls to accept dynamic loading commands and maintain stable system operation through load sharing and transitions. Finally, at $t = 0.2\ s$, the last load transition is made and the batteries supply the full load.

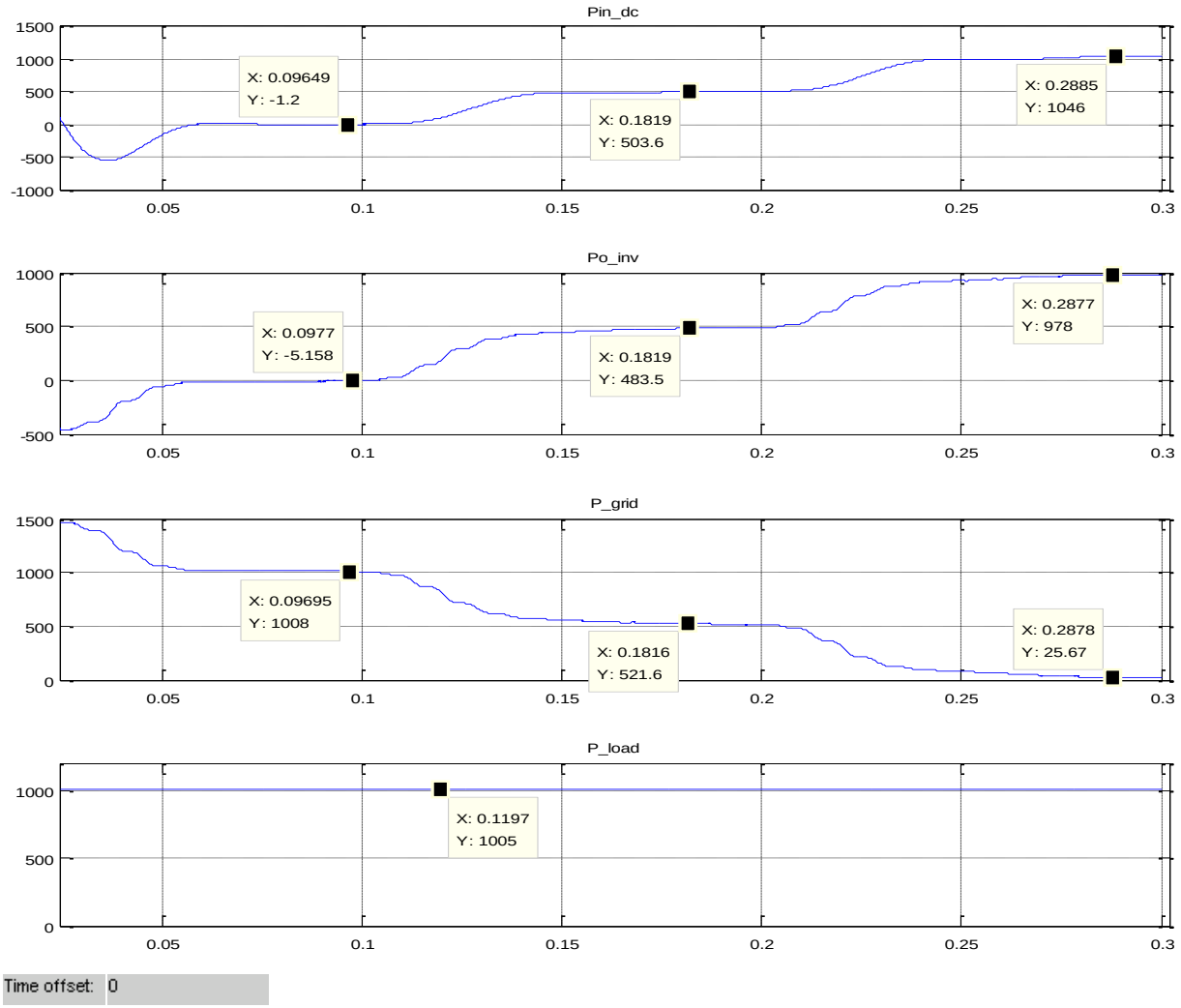

Fig. 4.4.13: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Power Waveforms

The dynamics of the SGPN operation should be very similar between island and grid connected modes, but the inverter controller does have the ability to affect the amount of ripple on the output voltage and current. This in turn can affect efficiency. Therefore the efficiency is simulated with the grid source over power supplied by the SGPN. A constant load will be applied of 1 kW at the AC bus. The power delivered is the contribution made by the SGPN (50 W – 1 kW) which is shown graphically below in Fig. 4.4.14.

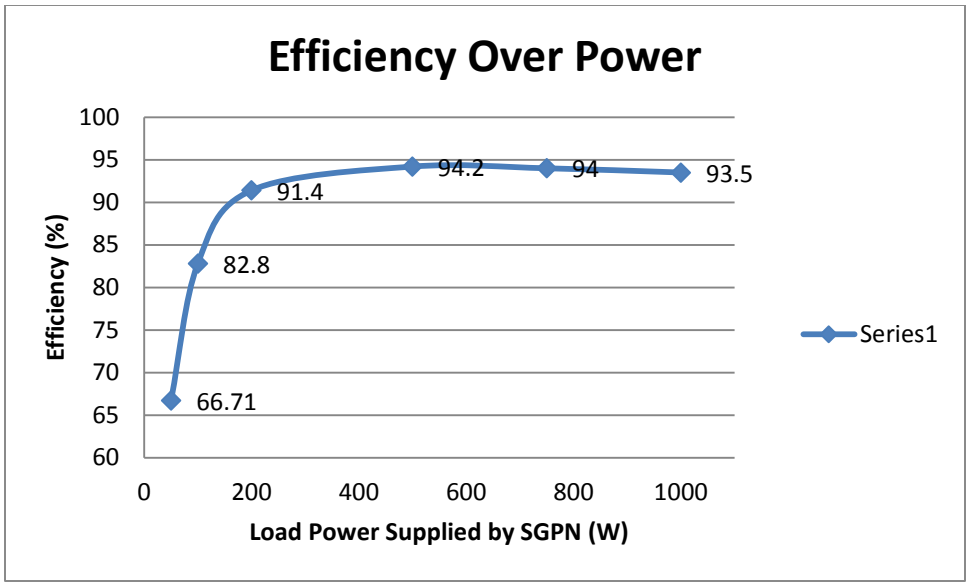

Fig. 4.4.14: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - System Efficiency Over Power

4.4.2.1.1 THD Analysis

Similar to section 4.4.1.1, the THD of the inverter AC voltage and current will be analyzed in this section. Fig. 4.4.15 shows the THD analysis of the AC inverter voltage. The behavior is relatively constant throughout the increased load on the SGPN, so only 1 section of the waveform is analyzed. The THD of the voltage is 0.92%, thus satisfying the requirements by IEEE 1547 for distributed grid-connected systems.

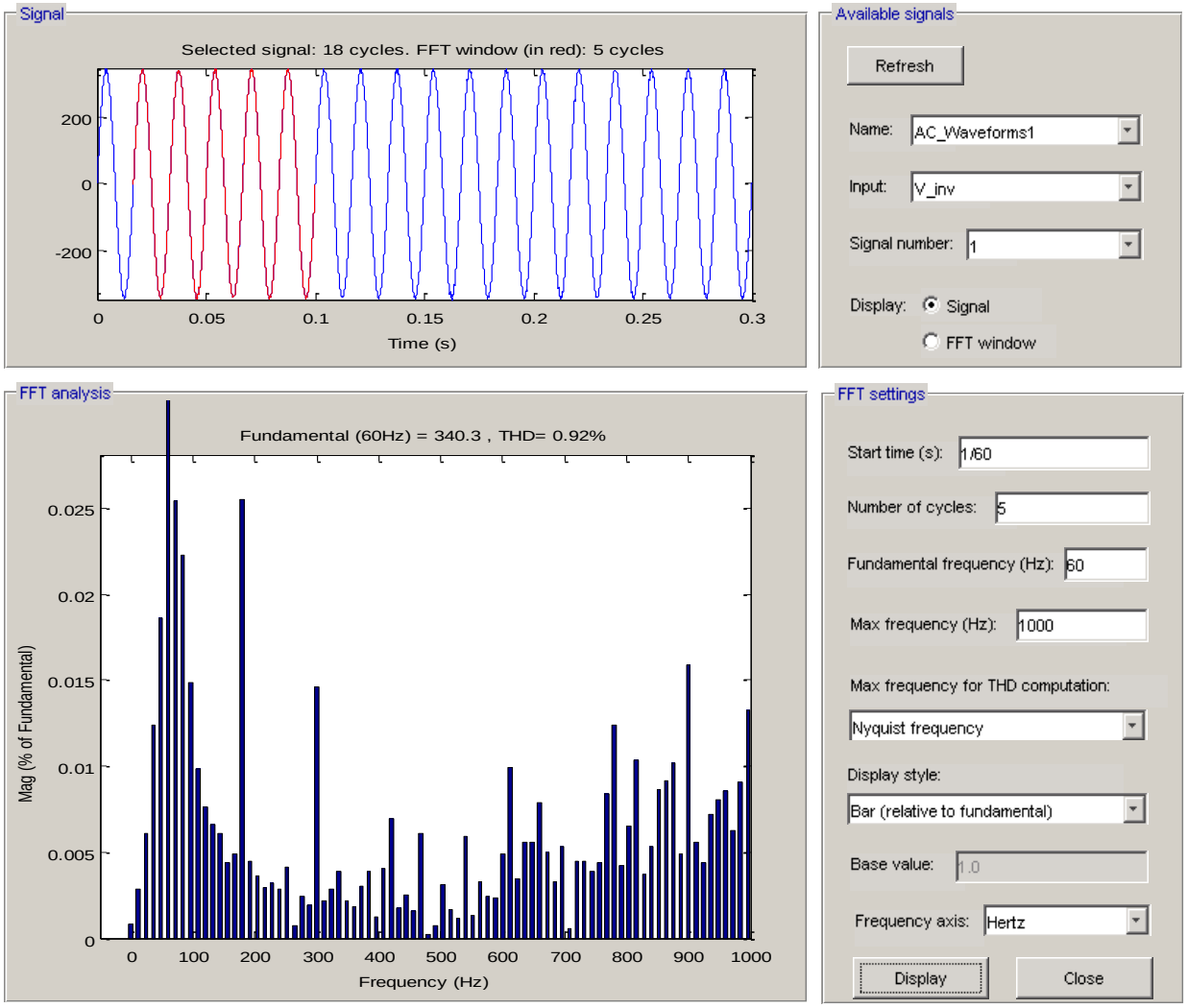

Fig. 4.4.15: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Inverter Voltage FFT

Fig. 4.4.16 shows the FFT analysis of the inverter current during the load sharing stage in which roughly 500 W of power is being supplied by the SGPN. Similar to the island mode operation, the distortion is quite high at almost 12%. This again points to a design improvement which must be made for a commercial development of the SGPN.

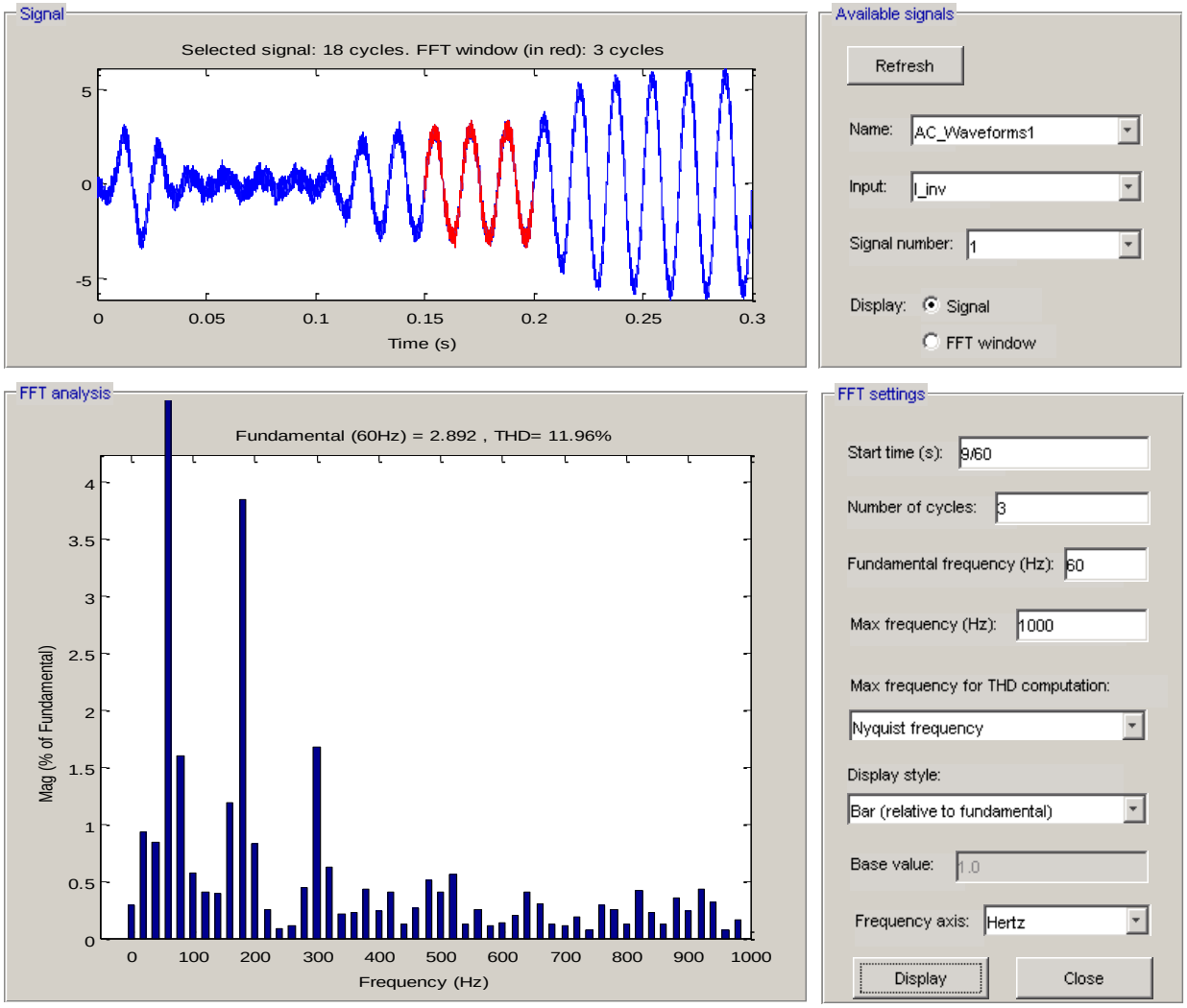

Fig. 4.4.16: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Low Wattage Inverter Current FFT

Finally the inverter current FFT results are shown below in Fig. 4.4.17 for the full 1 kW load being supplied by the SGPN. It can be seen that there is a slightly better performance with the grid-connected simulation on the harmonic injection into the load. In island mode @ 1 kW the current THD was 7.84% falling some 1.55% percent to 6.29% for the grid-connected mode. Again, this is very close to the maximum distortion limits, but still requires improvement.

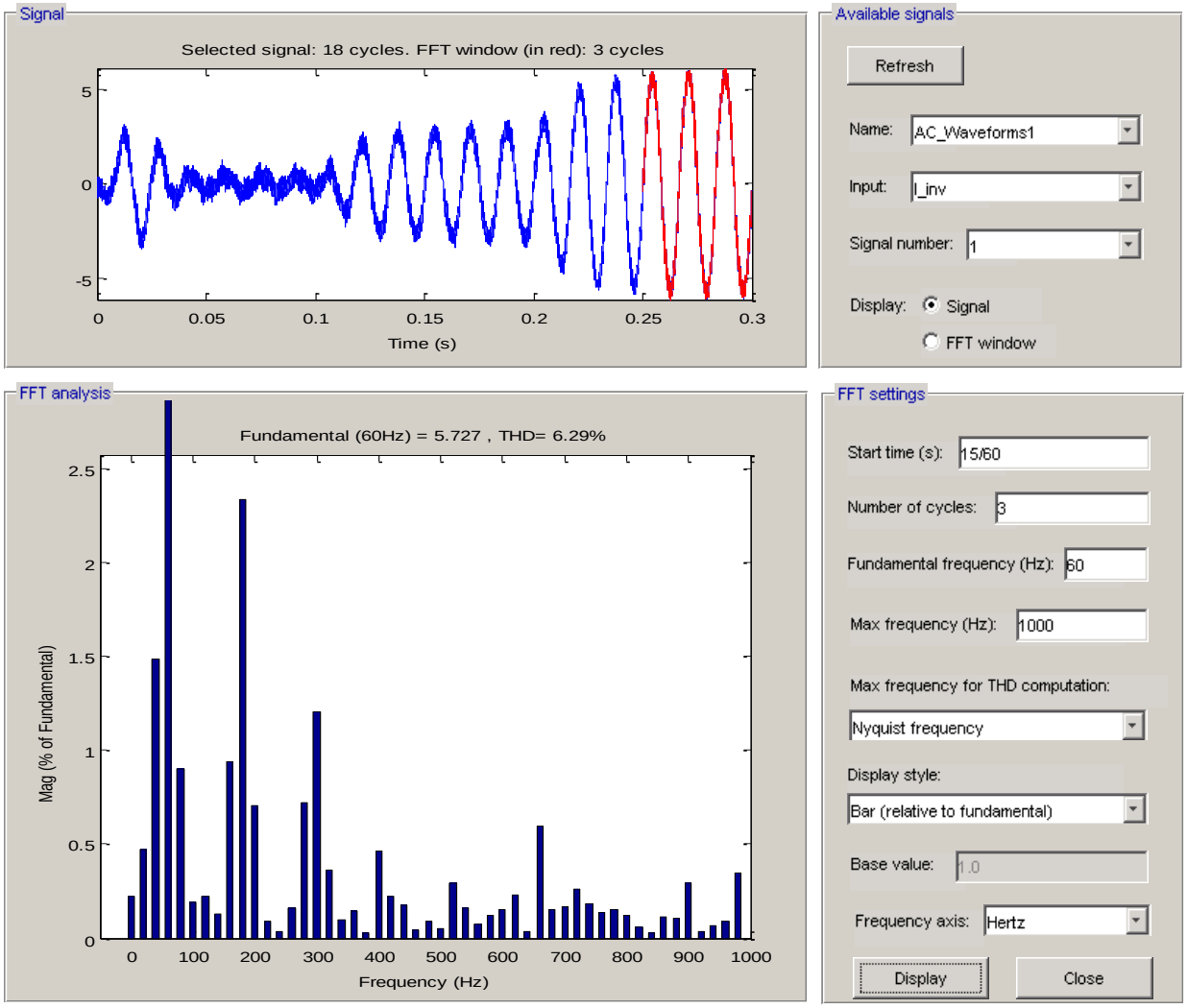

Fig. 4.4.17: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - High Wattage Inverter Current FFT

4.4.2.2 DC-AC Power Flow (Battery Discharge to Grid)

This section presents a simulated peak loading situation where the electric utility requests that energy be back fed onto the grid from the SGPN. This prototype is very low power at 2 kW rated with the battery charge/discharge converter rated at only 1 kW. The amount of power that can be supplied is negligible in the context of a utility's distribution system. However, this functionality is integral to the concept of the SGPN and is therefore demonstrated. Obviously, in a wide-scale deployment or a higher power prototype, this effect would be much more profound.

The simulation timeline is summarized below in Table 4.4.5. A constant load of 500 W is chosen as the home load throughout the simulation. From $0s \leq t \leq 0.15s$ the SGPN is supplying the full load to the home. At $t = 0.15s$ the SGPN continues supplying the 500 W home loads and now pushes 500 W onto the electric grid. The functionality of the inverter controller to sustain a home load and power sharing with the grid has already been presented. This demonstrates its ability to maintain stability through changing phase relationships and source power to the electric grid.

Table 4.4.5: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected(Power to Grid) - Simulation Timeline

Load Contribution by Source and Switching Times			
Time	**Load**	**Grid Power Supplied**	**SGPN Power Supplied**
$0 \leq t \leq 0.15s$	500 W	0 W	500 W
$0.15s \leq t \leq 0.3s$	500 W	-500 W	1 kW

It should be noted that for a practical application, an isolation transformer must be connected between the output of the LCL filter on the SGPN and the electric grid. The isolation barrier provides a crucial safety advantage. Fig. 4.4.18 shows a pictoral representation of this safety barrier. In order to avoid electric shock for accidental contact with a live conductor and the "ground", the isolation prevents the return path to earth ground through the human body. In addition, the leakage inductance of the transformer has an inherent benefit of reducing the high frequency harmonics injected into the grid from the inverter. A THD analysis demonstrating this effect will be presented in section 4.4.2.2.1.

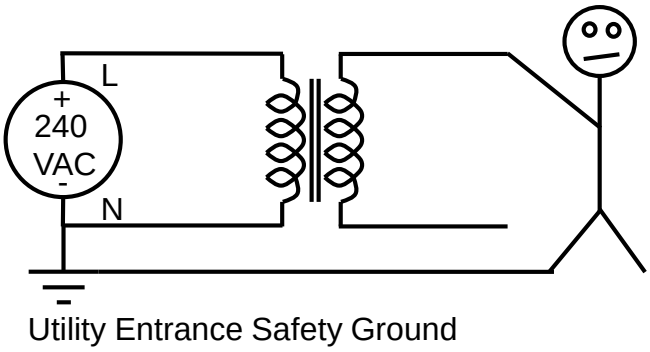

Fig. 4.4.18: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Simplified Safety Isolation Transformer Schematic

For simulation purposes, the isolation transformer is modeled as the equivalent series inductance. A simple leakage reactance calculation was adopted from [39] and is presented below. The leakage reactance is given by eq. $XFMR\ Leakage\ Reactance\ (X) = \frac{kv^2}{MVA}\left(\frac{\%\ impedance}{100}\right) = \frac{0.24\ kV^2}{.005\ MVA}\left(\frac{6}{100}\right) = 0.6912\ \Omega$ (4-3), where a 5 kVA 1:1 isolation transformer is chosen with 6% impedance.

$$XFMR\ Leakage\ Reactance\ (X) = \frac{kv^2}{MVA}\left(\frac{\%\ impedance}{100}\right) = \frac{0.24\ kV^2}{.005\ MVA}\left(\frac{6}{100}\right) = 0.6912\ \Omega \quad (4\text{-}3)$$

Now, a simple transformation to get from reactance to an inductance value yields:

$$L = \frac{X}{2\pi f} = \frac{0.6912\ \Omega}{2\pi * 60\ Hz} = 3.67\ mH \quad (4\text{-}4)$$

The AC waveforms for the above simulation are shown below in Fig. 4.4.19. The inverter voltage is very stable throughout the load transitions and at startup. The DC system performance is identical to section 4.4.2.1, so those waveforms are not repeated here. The transients on the inverter current can be seen at the very beginning of the simulation which was also seen in section 4.4.2.1. Again, the mitigation of this harsh transient situation is addressed in section 5.6.2. Initially, the grid source tries to supply the load while the SGPN is still in its startup state.

At t_0 as the system reaches steady state, the grid current reduces, and the SGPN supplies the load. At t_1 the inverter current is in phase with the inverter voltage thus sourcing power to the load. The grid current during this time period is 90° out of phase supplying the reactive power to the AC filter. For the remainder of the simulation the SGPN sources power to the grid and supplies the home load while the grid is syncing power. This can be seen at t_2 where the inverter current is in phase with the inverter voltage and the grid current is 180° out of phase with the inverter voltage thus the grid is syncing real power.

The grid current can be seen to have a significantly reduced higher frequency harmonic content. This is due to the effect of the leakage reactance of the isolation transformer which will be discussed further in section 4.4.2.2.1.

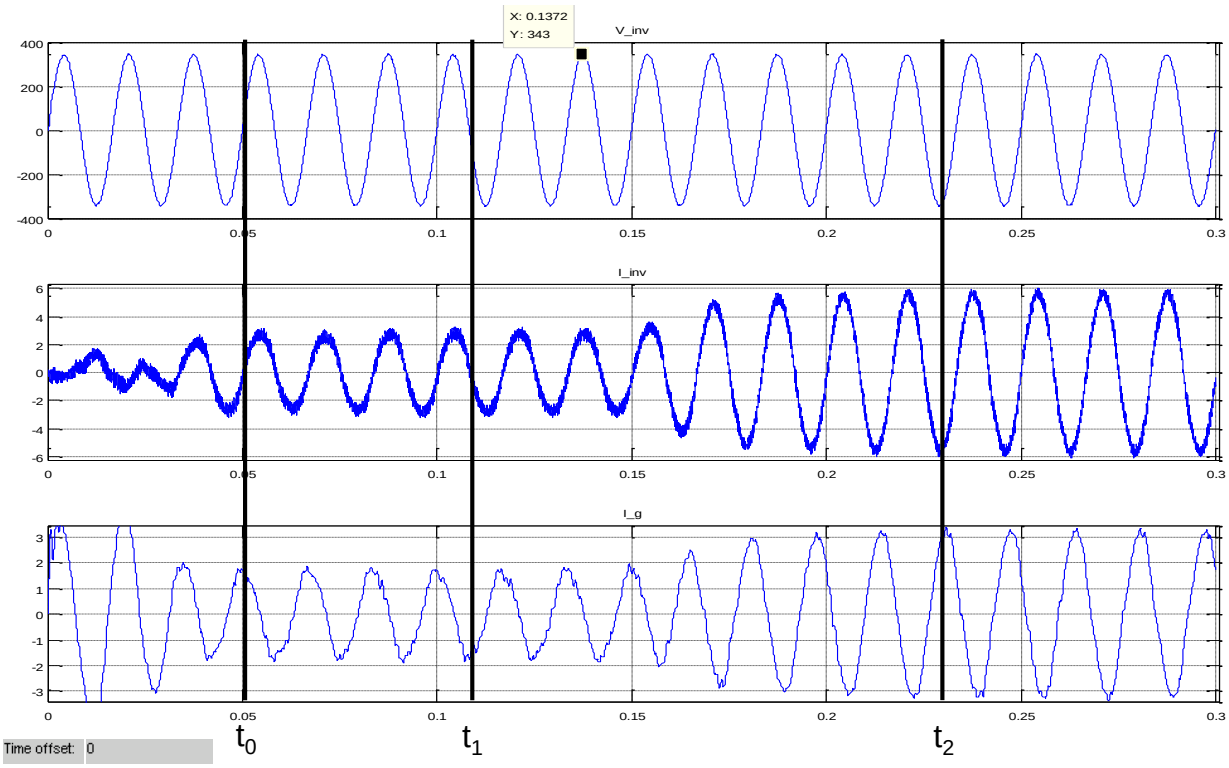

Fig. 4.4.19: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected(Power to Grid) - AC Waveforms

The averaged SGPN (DC and AC) and grid real power waveforms for this simulation are shown below in Fig. 4.4.20. The transient startup is also apparent in this waveform as the initial power from the grid is very high and decreases as the SGPN reaches steady state. As described, the SGPN is supplying 489.6 W which is very close to the expected 500 W at t_1. The grid makes up the difference of 19.81 W giving a total 509.41 W supplied by the two sources. The load power is a constant 509.7 W leaving a 0.5% difference.

At t_2 it can be seen that the input DC & inverter output power increases by about 50% to around 973 W supplying the constant 500 W load, and the 464.2 W to the grid. The grid power is then seen to be negative thus syncing the extra power output from the SGPN.

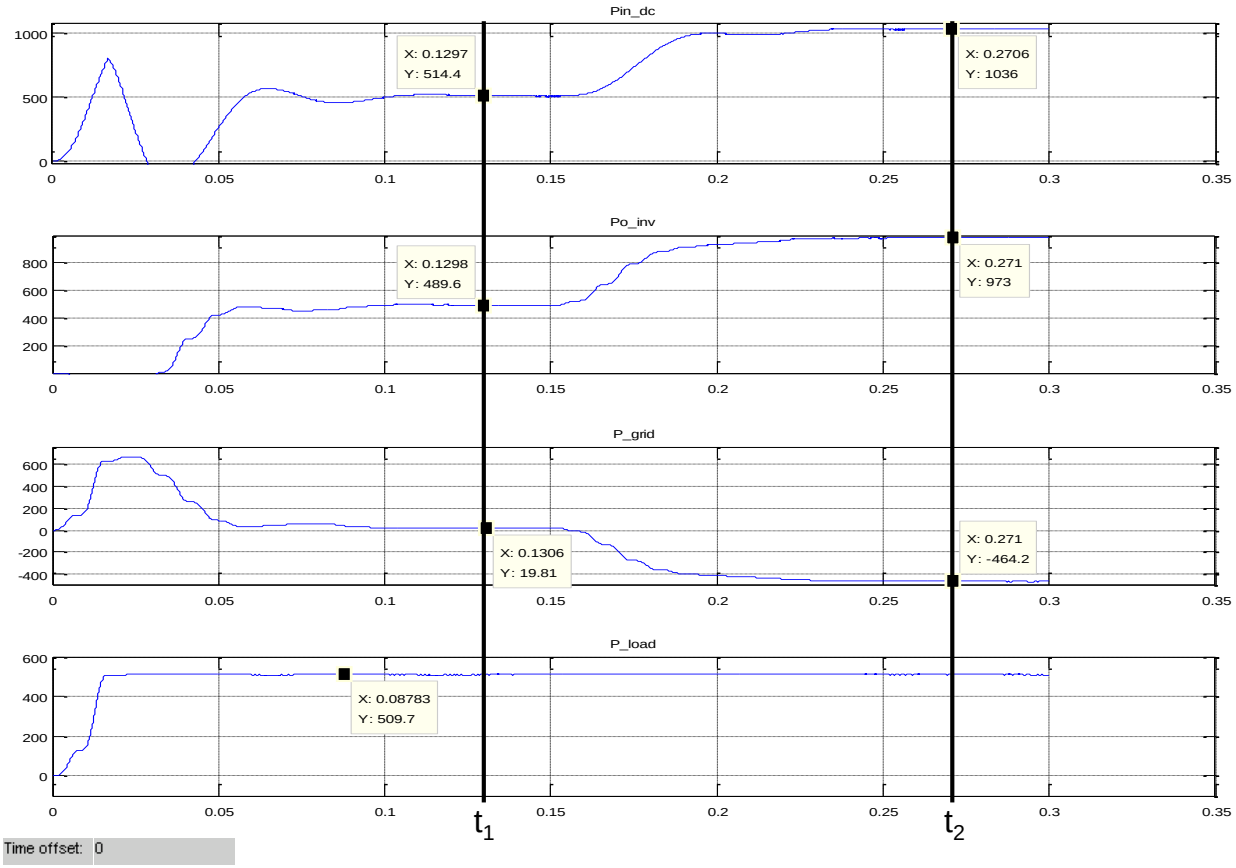

Fig. 4.4.20: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected(Power to Grid) - Power Waveforms

The efficiency of the SGPN is system is presented to determine the effects of pushing power onto the grid from the SGPN, if any. The input power to the system at t_2 is 1036 W with the power delivered being 973 W. This yields an efficiency of 93.9%. This is comparable from previous grid-connected simulations with the battery charge/discharge converter.

4.4.2.2.1 THD Analysis

This section presents the FFT analysis of the inverter and grid currents for the above simulation. The THD of the inverter voltage in grid-connected mode has been presented and is therefore not repeated here. In Fig. 4.4.21 the inverter current harmonics are shown with the full load being supplied and no energy pushed to the grid. At around 500 W, this 12-13% THD range

has been seen. There is a large contribution from the 3rd and 5th harmonics (4.5% and 1.2% respectively) which is a characteristic of the single phase inverter. Also, from inspection there is a large amount of high frequency content present in the inverter current.

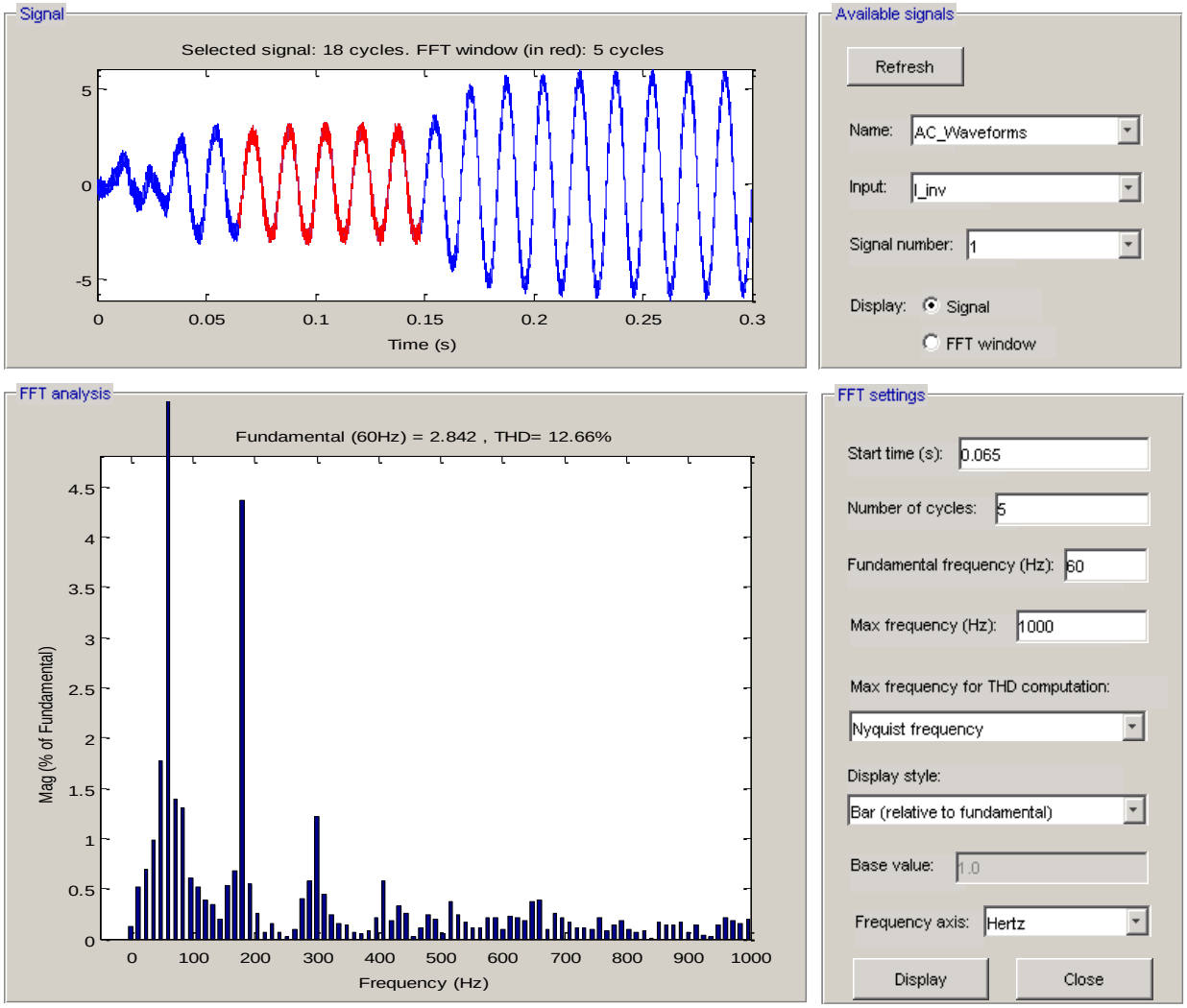

Fig. 4.4.21: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected(Power to Grid) - Low Wattage Inverter Current FFT

There are mitigation techniques that can eliminate these lower order harmonics from the inverter such as additional low pass filtering or programmable harmonic elimination switching. The passive filter required to suppress almost all low frequency harmonics is generally very large, heavy, and bulky which adds cost and space, so more clever techniques are desired.

Programmable harmonic elimination combines the fundamentals of square wave switching and PWM control to eliminate the desired harmonic frequencies [26] such as the 3rd, 5th, and 7th. With the advent of powerful microcontrollers, "notches" at the desired frequencies can be programmed easily to control a switching leg of the inverter in such a manner to eliminate these harmonics [26]. This and other harmonic mitigation techniques will be discussed further in CHAPTER 6 .

Next, the grid current THD will be presented. A simplified illustration of the current measurement points for the inverter and grid are shown below in Fig. 4.4.22. The FFT plot is shown below in Fig. 4.4.23. It can be seen that the high frequency harmonic content is greatly reduced by the leakage inductance of the isolation transformer $L_{isolation}$ and the second filter inductor L_2. However, there is still a dominant 3rd harmonic contribution of (7.5%) injected into the grid source.

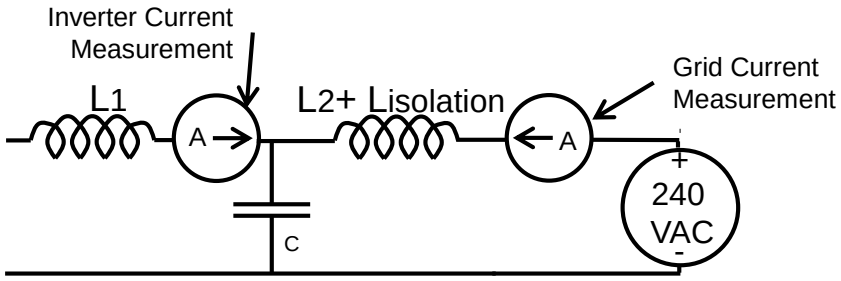

Fig. 4.4.22: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Current Measurement Location Schematic

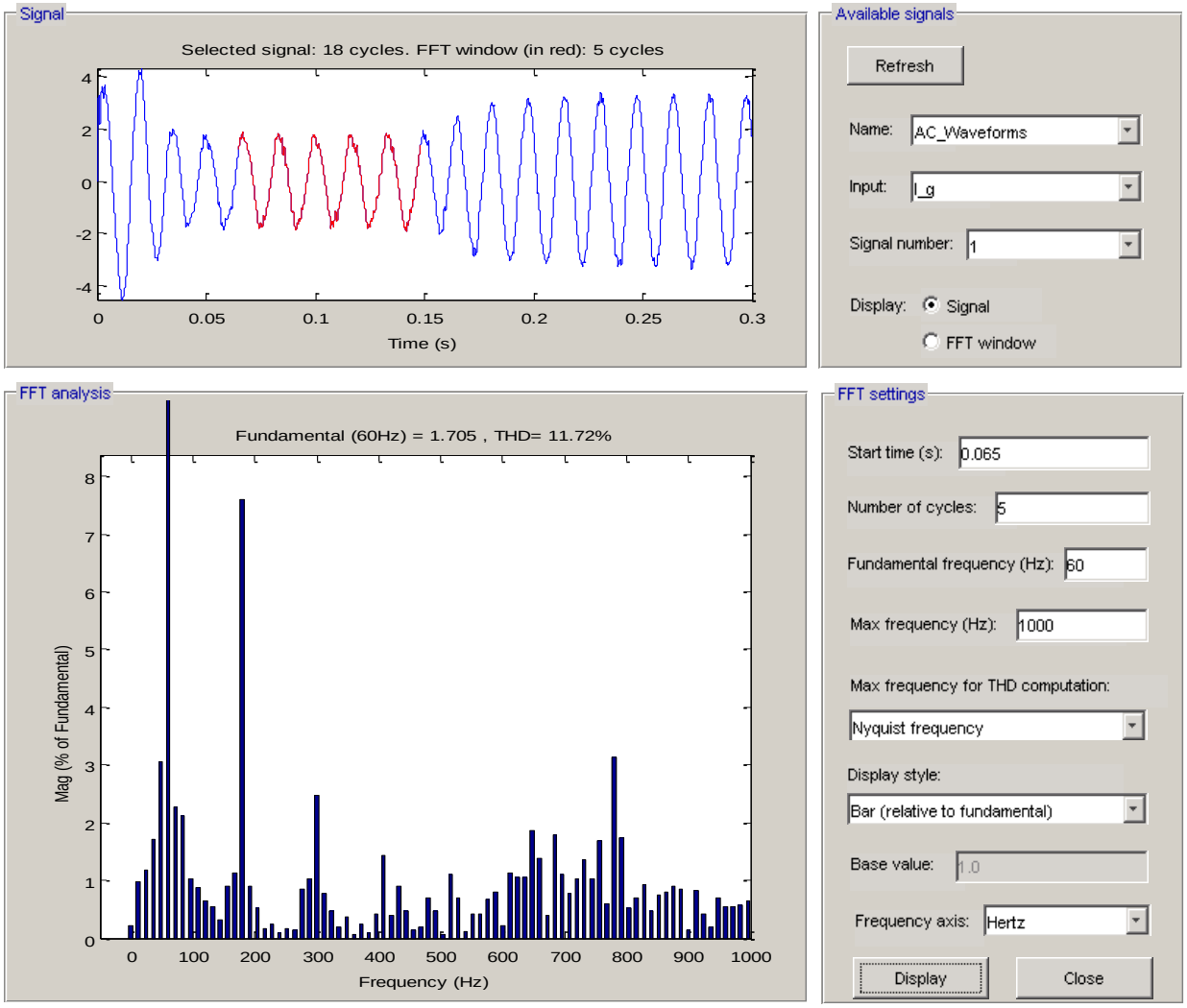

Fig. 4.4.23: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected(Power to Grid) - Low Wattage Grid Current FFT

It appears between Fig. 4.4.22 & Fig. 4.4.23 that the percentage harmonic contribution from the 3rd, 5th, and 7th are larger on the grid current than the inverter current which would seem counterintuitive. However, the fundamental component of the inverter current is 66% larger than the grid current. Therefore the large discrepancy in harmonic contribution can be explained by the fact that any particular harmonic frequency distortion in grid current will be a larger percentage of the fundamental than the inverter. A THD analysis of the grid current under a higher current amplitude is presented below, verifying the above statement.

It should be noted that the grid source was modeled as an ideal AC voltage source. A detailed model of the grid source would give more realistic behavior of the infinite bus, but is beyond the scope of this thesis.

The FFT analysis of the inverter current when supplying full load and pushing energy to the grid is shown below in Fig. 4.4.24. As expected, pushing energy onto the grid has a negligible impact on the THD for the inverter current.

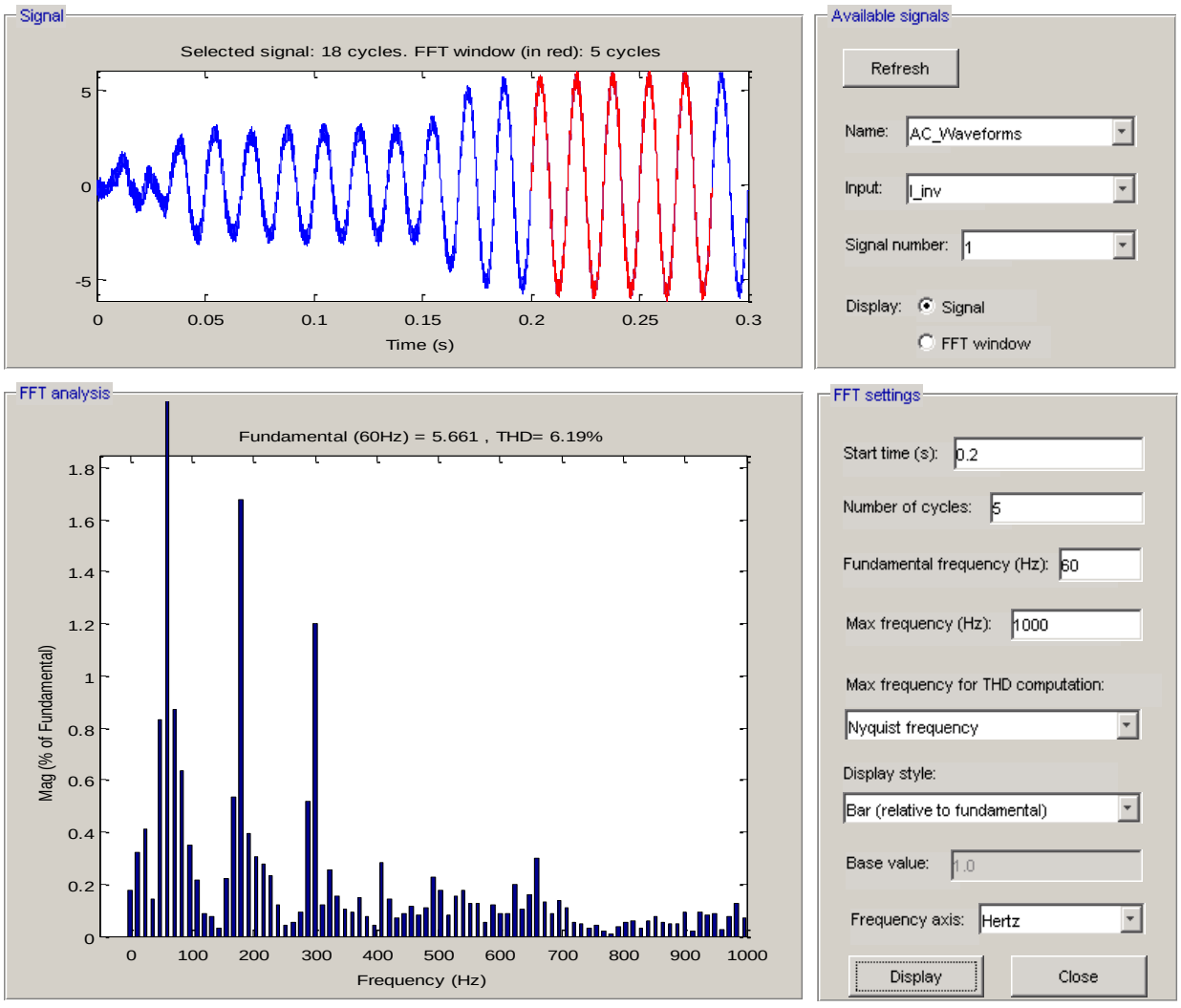

Fig. 4.4.24: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected(Power to Grid) - High Wattage Inverter Current FFT

The THD analysis of the grid current is shown below in Fig. 4.4.25. The THD with the larger amplitude current is much improved at 6.3%. It is expected that with an increased power delivered to the grid, the THD will be very close to IEEE 1547 performance criteria. This will be shown in section 4.5 with the paralleled DC input simulations.

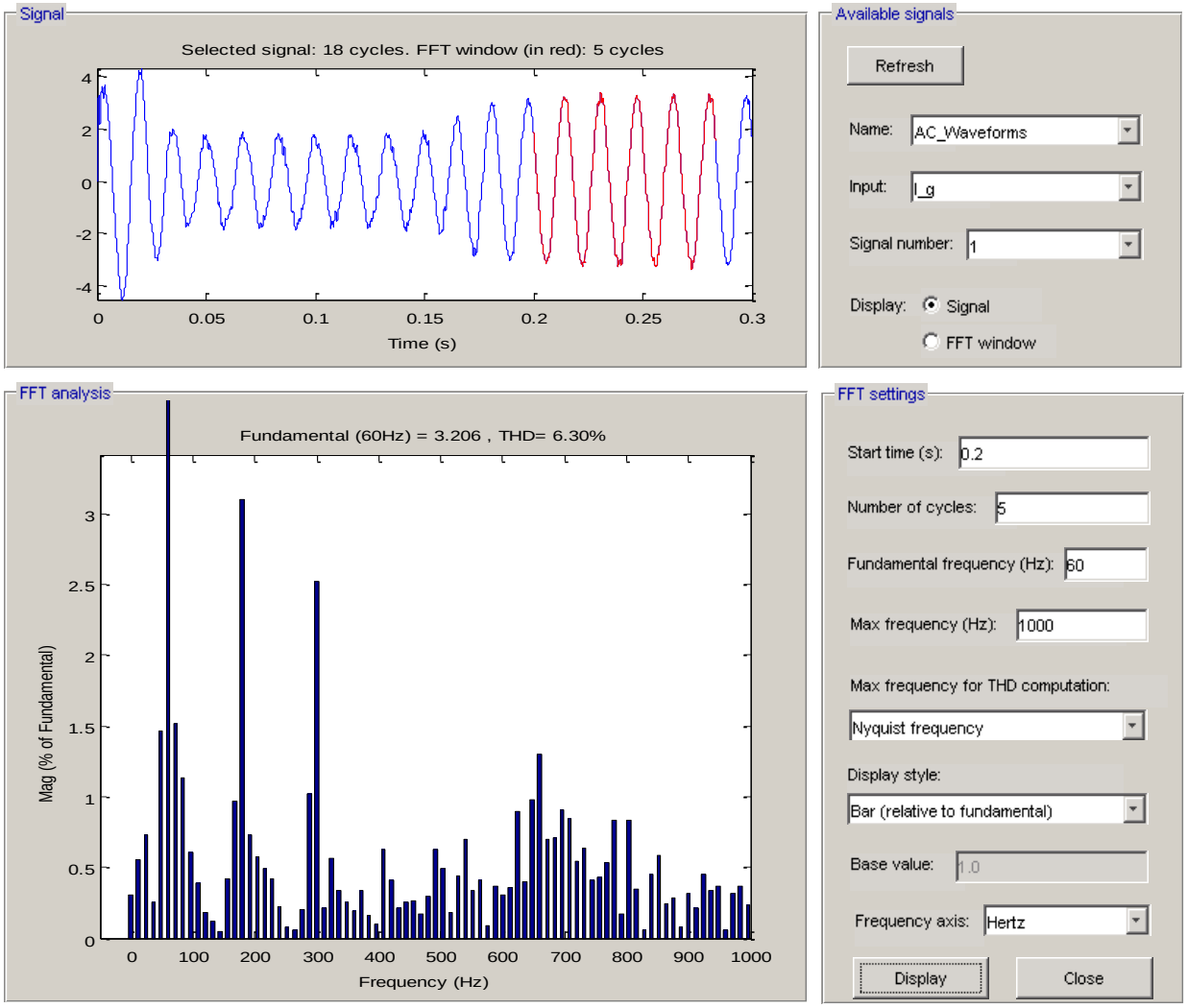

Fig. 4.4.25: Closed Loop Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected(Power to Grid) - High Wattage Grid Current FFT

4.5 Closed Loop Interleaved PV Boost and Battery Charge/Discharge Converter with Full Inverter

This section presents the fully integrated SGPN hardware with the paralleled PV boost converter & battery charge/discharge converter + full inverter. First, the results will demonstrate the ability of the SGPN to power share in island mode and handle step loading conditions during operation. Next, the SGPN will be grid connected with paralleled DC inputs to show power sharing between DC-DC converters and the grid, and step loading while grid connected. The

system level functionality of individual DC inputs has been demonstrated in previous sections. For example, the operation of pushing energy onto the grid source (emulating selling energy to the utility) is independent of the DC system, so these results are not reiterated. This section will focus only on the functions required for paralleled inputs.

4.5.1 *Island Model: Power Sharing Static Load*

This section demonstrates the closed loop controls of the PV Boost & battery charge/discharge converter integrated with the full inverter in island mode. For paralleled DC inputs a power sharing network is required in order to control the contributed power flow between each source converter. The design for the power sharing network is detailed in [11], but an explanation is needed here to facilitate the simulation results.

The overall control structure for the power sharing network is shown below in Fig. 4.5.1. Each DC-DC converter has its own independent control loops containing the outer voltage loop ($C_2(s)$) and the inner current loop ($C_1(s)$) which are both controlling the duty cycle of their respective switches to regulate the LV DC link (V_o). The power flow control block senses the current being supplied by each converter which is proportional to the load demanded at the LV DC link. The output of the power flow control block serves as an additional current reference (positive or negative) to the respective independent controllers. Through adjustment to this additional current reference to each control network, the power output from each converter is controlled.

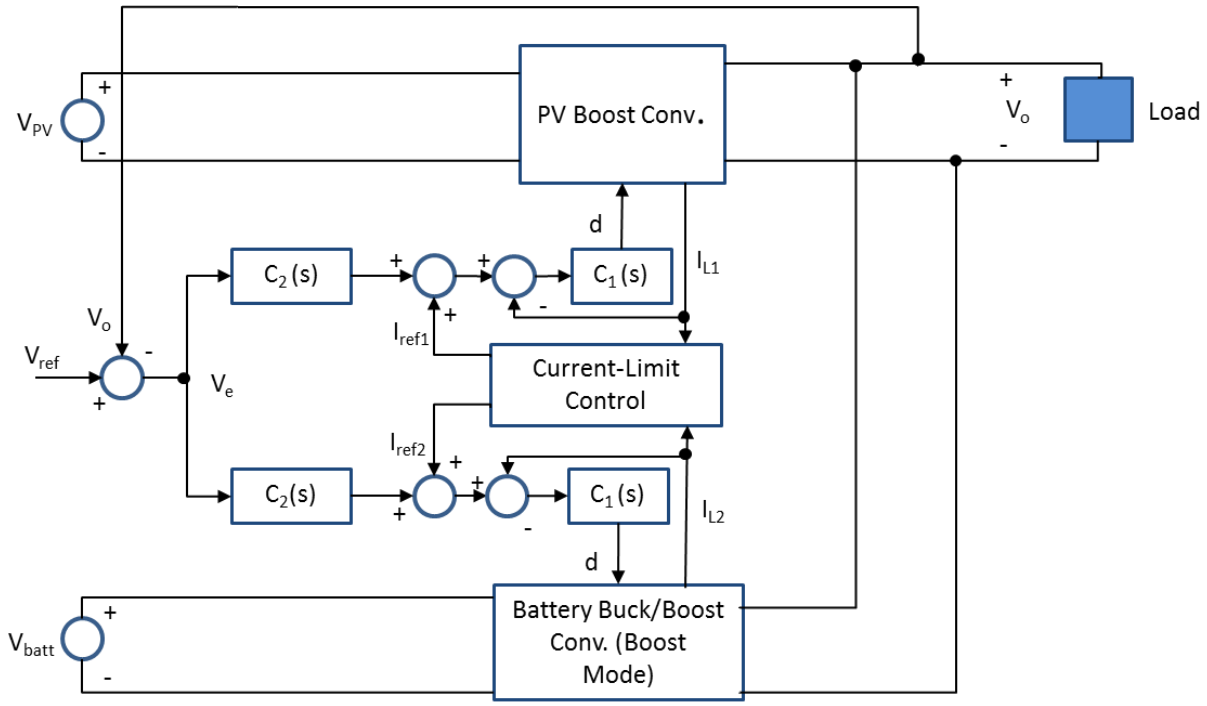

Fig. 4.5.1: DC Power Sharing Network - Courtesy of Brian P. Stalling

A model of the power flow control module is shown below in Fig. 4.5.2. The current from the PV converter and battery converter are first summed at the input thus accounting for the full power demanded at the LV DC link. The load current is then split at the desired proportion between the two converters and subtracted from the current already supplied by that converter. The result is a "net" current reference to be output to the respective control blocks. This model shows a static gain block as the split ratio. Obviously in a real world situation this is not practical as the PV source fluctuates and batteries get discharged.

However in full system integration the system level controller would be monitoring all input status, load demand, etc. and send dynamic current references to the power flow control block - thereby actively controlling the power contribution from the batteries and PV source.

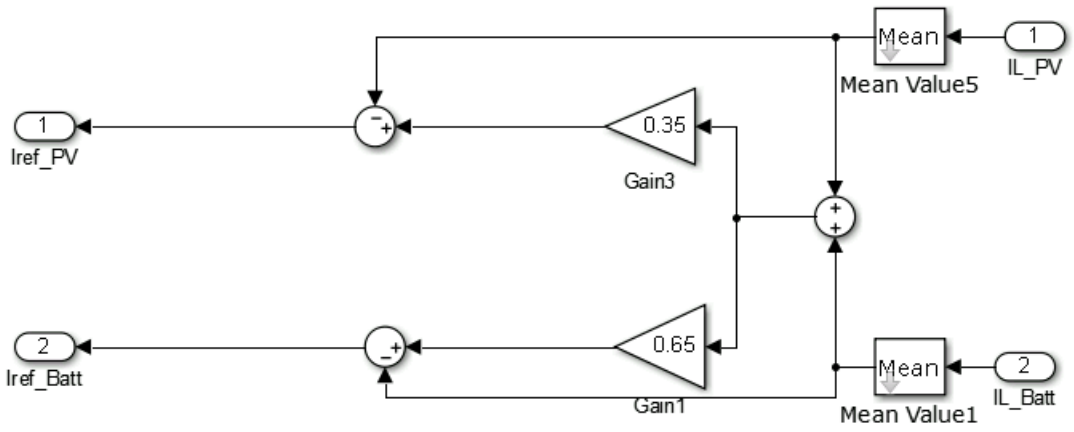

Fig. 4.5.2: DC Power Sharing Network Current Limiting Control

The simulation timeline is summarized below in Table 4.5.1. A constant load of 1 kW is connected to the output of the inverter with the disconnect switch to the grid open. Initially, from $0s \leq t \leq 0.1s$ the batteries are supplying the home load. At $t = 0.1s$ the power flow controller is initiated and the PV converter splits the load by half with the batteries. This demonstrates the ability of the fully integrated SGPN to share power with interleaved DC inputs with the power flow control described above for a static load.

Table 4.5.1: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Static Load - Simulation Timeline

Load Contribution by Source and Switching Times			
Time	**Load**	**PV Power Supplied**	**Battery Power Supplied**
$0 \leq t \leq 0.1s$	1 kW	0 W	500 W
$0.15s \leq t \leq 0.3s$	1 kW	500 W	500 W

The waveforms for the DC system are shown below in Fig. 4.5.3. Initially the PV converter is supplying no load as the input current is effectively 0 A, while the battery current is non-zero. The HV and LV voltages maintain stability with a slight 120 Hz ripple voltage induced by the inverter. At $t = 0.1s$, the power share pulse is asserted which engages the power sharing

network and the PV converter controller. The battery current decreases while the PV current increases, hence the two converters sharing the load at the LV DC bus.

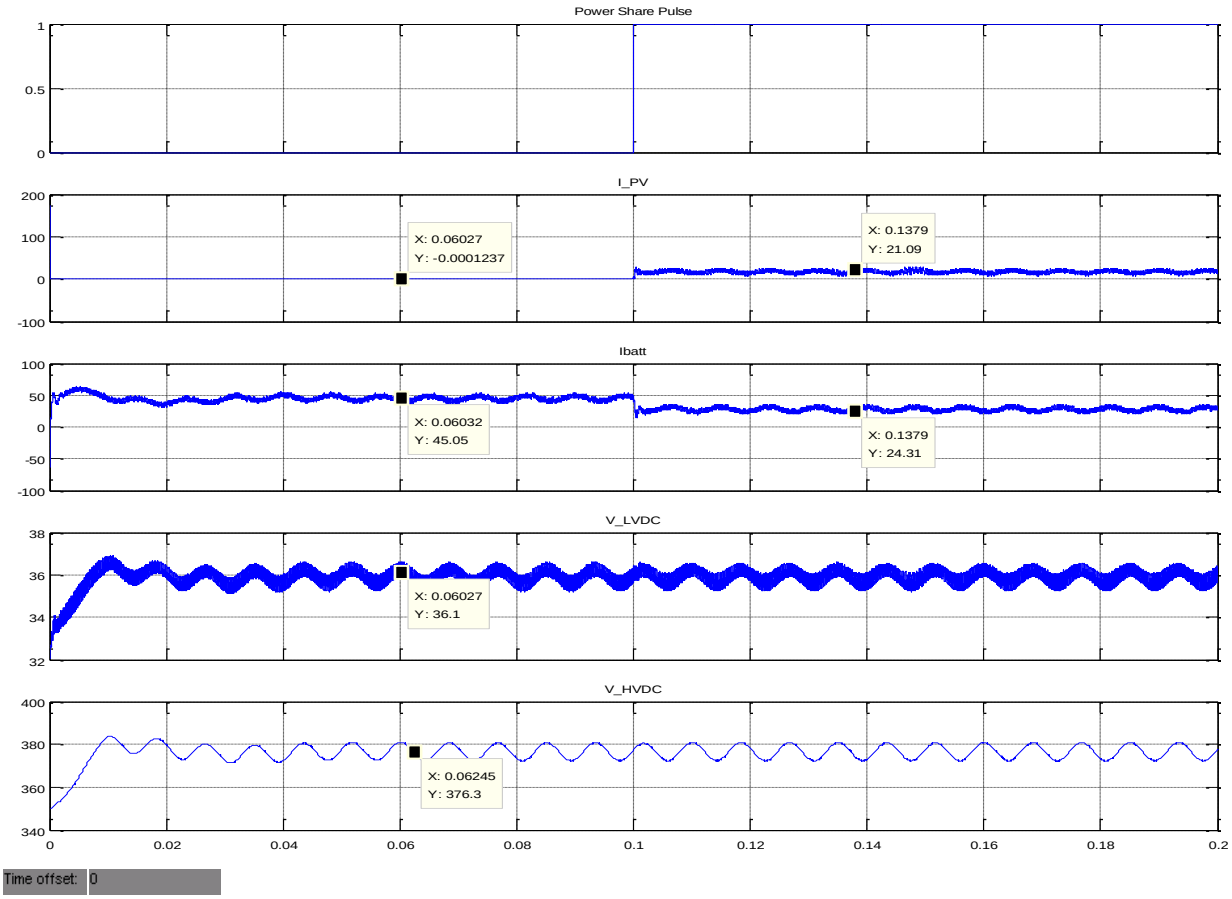

Fig. 4.5.3: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Static Load - DC Waveforms

The AC waveforms for the islanded parallel DC input simulation are shown below in Fig. 4.5.4. The system reaches steady state quickly in approximately 10 ms. The inverter voltage and current are stable showing no change in amplitude after steady state – hence the static loading condition. At $t = 0.1s$ the inverter RMS voltage and RMS current are shown to be virtually undisturbed by the power sharing on the DC side, which is a very desirable behavior. The inverter voltage is a 241.6 V which is an error of 0.67% from the reference 240 V_{RMS} fed to the inverter controller.

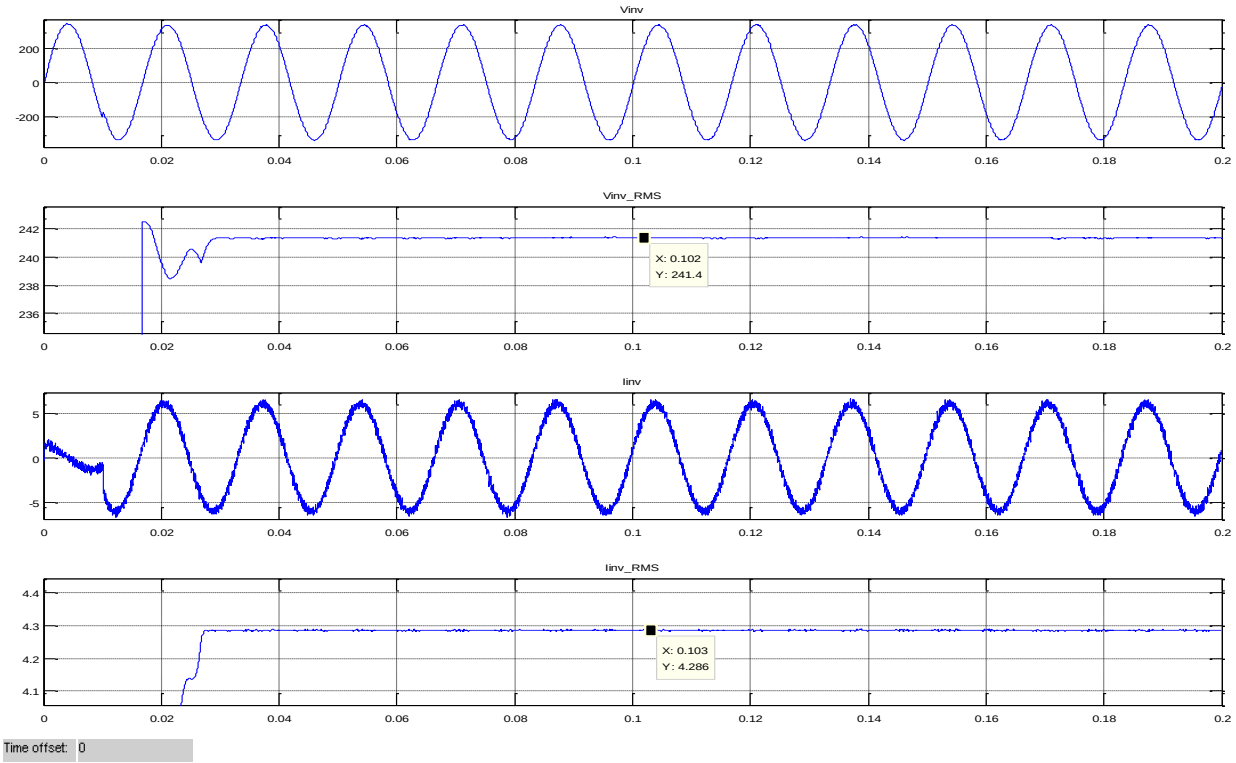

Fig. 4.5.4: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Static Load - AC Waveforms

The averaged power plots for the same simulation are shown below in Fig. 4.5.5. At t_1 while the battery is serving the full load, it can be seen the input power equals the power discharged from the battery and the PV converter is supplying nothing. At $t = 0.1s$ the power sharing network is initiated which is shown by the subsequent increase in PV power and decrease in battery power. Notice, the PV contribution of 521.4 W and the battery contribution of 551.8 W is equal to the total input power of 1073 W. As stated above, the output power served to the load is virtually undisturbed.

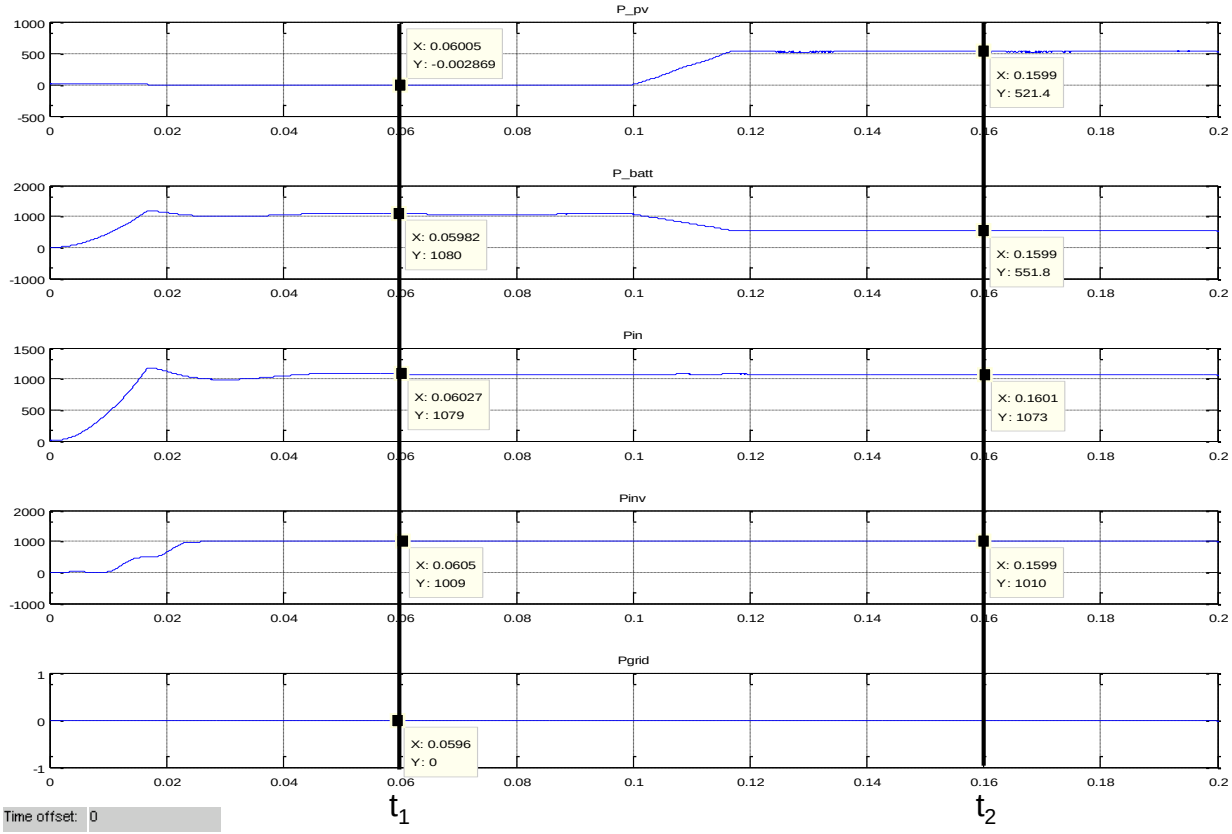

Fig. 4.5.5: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Static Load - Power Waveforms

The efficiency of the SGPN while the battery converter is supplying the full load is approximately 93.5% while the efficiency with the load shared by both converters is 94.1 %. Even though another switch was added into the system which increases switching losses, the decrease in conduction losses of the 2 switches ($2*I^2R$) in the battery converter compared to the conduction losses in the 1 switch of the PV converter was enough to boost the efficiency.

4.5.1.1 THD Analysis

This section presents the THD analysis of the inverter current and voltage for the fully integrated system in island mode with paralleled DC inputs. It should be noted that the paralleled DC inputs should have a very small effect on the THD performance of the inverter since the loading conditions are the same as section 4.3.1 & 4.4.1, but are shown here for completeness.

Fig. 4.5.6 shows the FFT of the inverter voltage which has similar performance to other simulations with a THD of 0.77%.

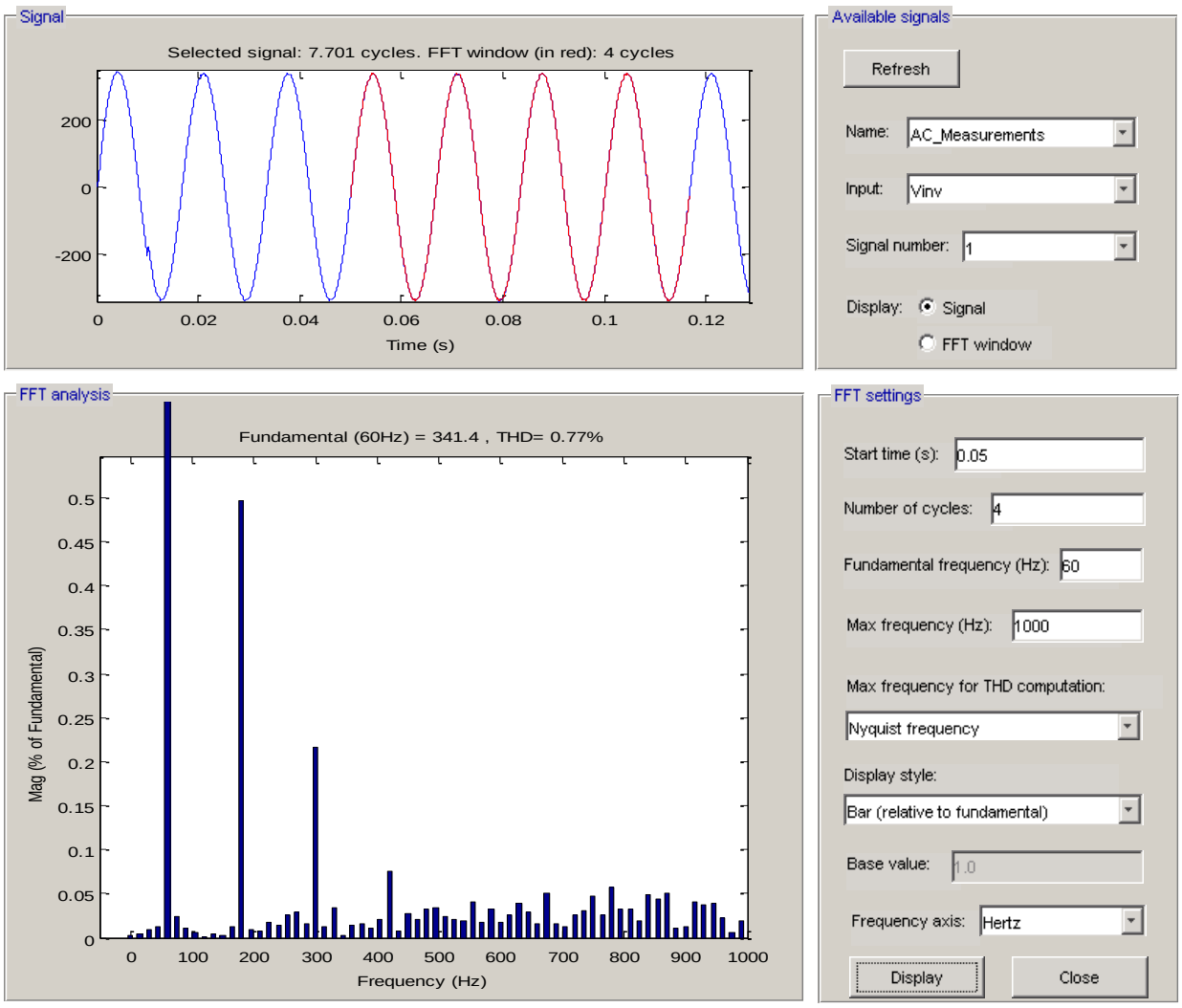

Fig. 4.5.6: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Static Load - Voltage FFT

The FFT plot for inverter current is shown below in Fig. 4.5.7. It can be seen that the THD of the inverter current is reduced by around 0.5%. This is very close to similar simulations for the island mode inverter results.

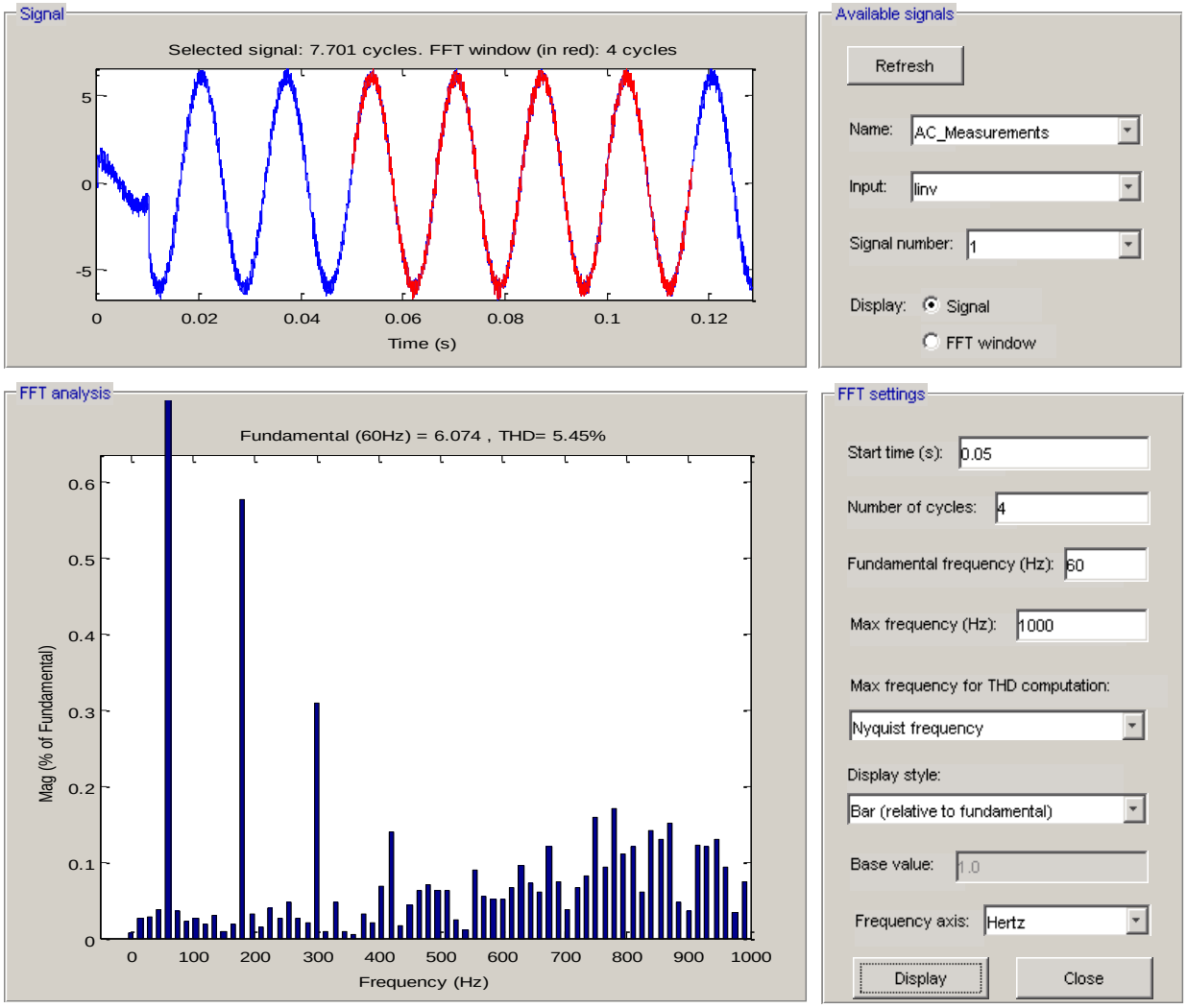

Fig. 4.5.7: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Static Load - Current FFT

4.5.2 *Island Model: Power Sharing Step Load*

This section demonstrates the ability of the SGPN system to power share between paralleled DC inputs and handle step loading conditions while power sharing in islanded operation. This emulates the home owner adding a significant load to the system while the grid is not available. The simulation timeline is summarized below in Table 4.5.2.

Table 4.5.2: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Step Load - Simulation Timeline

Load Contribution by Source and Switching Times

Time	Load	PV Power Supplied	Battery Power Supplied
$0 \leq t \leq 0.1s$	1 kW	0 W	1 kW
$0.1s \leq t \leq 0.2s$	1 kW	500 W	500 W
$0.2s \leq t \leq 0.3s$	2 kW	1 kW	1 kW

The beginning of the simulation assumes a static load that the batteries are initially supplying. Similar to section 4.5.1, the solar source shares the load at t_1. At t_2 an additional load is switched in parallel where the SGPN system is supplying its fully rated load of around 2 kW. It should be noted that the step load is shared by each converter equally after t_2. This is due to the loading on the converters during the simulation. If no updated reference is given to the power sharing block, it will split equally. However, the system level controller has the ability to divide the load in whatever proportion is needed granted the ratings of any given converter are not violated.

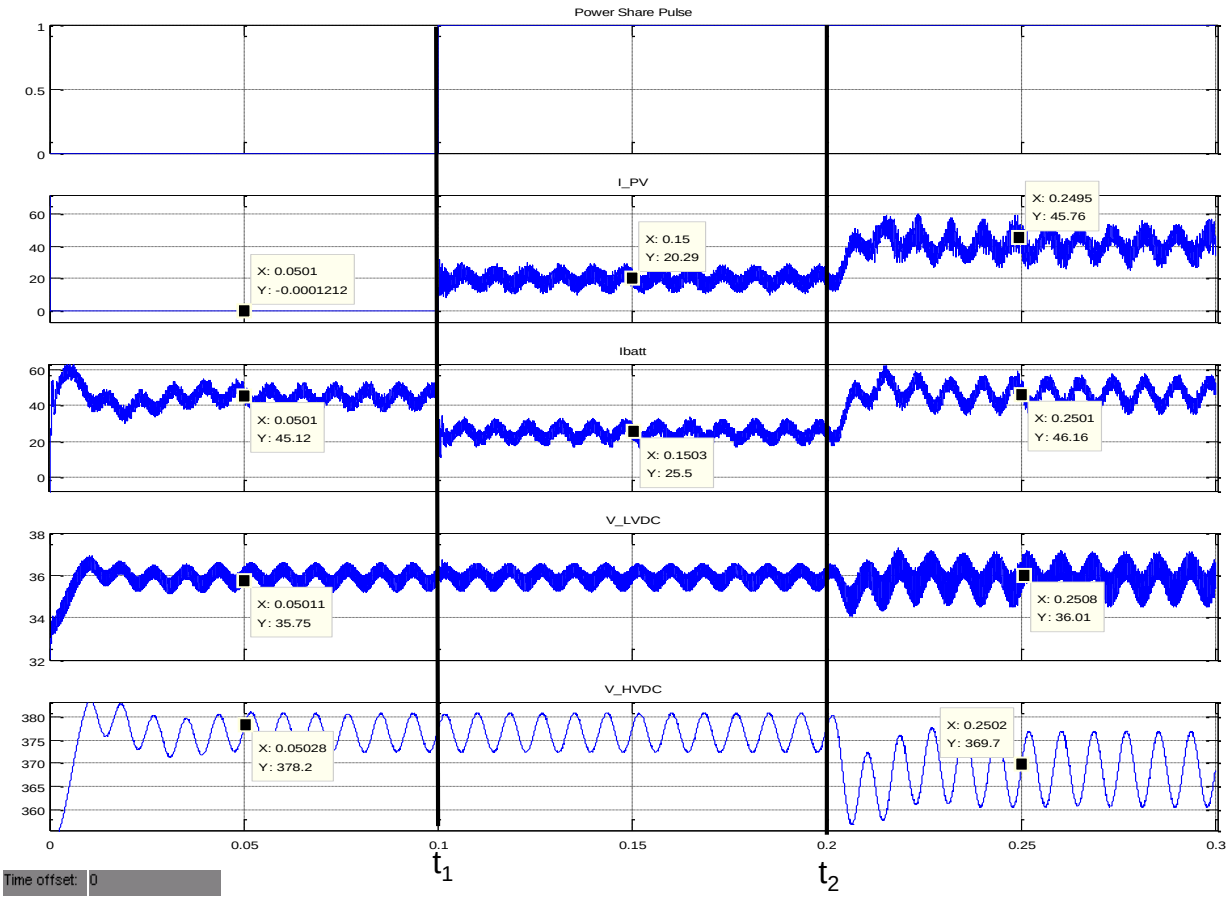

Fig. 4.5.8: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Step Load – DC Waveforms

It can be seen the DC system after t_2 has a relatively high ripple content at 2 kW. The increased ripple is expected with the increased loading on the system. The minimum voltage allowable on the HV DC link is 340 V to maintain a linear modulation of the inverter. It can be seen the minimum value is still above 360 V at full load. The low frequency ripple current experienced on the input inductors from the battery and PV source is very high when serving their rated load. This oscillating current will cause unnecessary heating of the input inductors which increase losses, decrease the life of the equipment, and will add to thermal management expenses. Therefore this must be improved in a commercial development (see CHAPTER 6).

The DC system performance is summarized below in Table 4.5.3 for the full rating of the SGPN system. It can be seen that the DC bus percentage ripple voltage has increased which is expected with the load on the system. The LV DC bus ripple marginally exceeds the maximum specification by a fraction of a percentage, but is very close. Since the overall system is not affected, this is an acceptable margin.

Table 4.5.3: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Step Load - DC System Performance

PV & Battery Charge/Discharge Converter w/ Full Inverter: DC System Performance					
		Spec.		**Simulated**	
		Voltage	% rated	Voltage	% rated
Voltage Sag	LV DC Bus	3.6 V	10%	2.0 V	5.56 %
	HV DC Bus	38.5 V	10%	27 V	7.01 %
Voltage Ripple	LV DC Bus	1.8V	5%	2.1 V	5.83 %
	HV DC Bus	38.5 V	10%	16.0 V	4.15 %

The AC waveforms are shown below in Fig. 4.5.9 which include the inverter voltage and inverter current. The inverter voltage shows stable behavior throughout the single source ($t \leq t_1$), power sharing ($t_1 \leq t \leq t_2$), and step load times ($t \geq t_2$). The inverter voltage is 241.4 V & 235.4 V_{RMS} in the power sharing and step load times, respectively. This corresponds to an error of 0.6% and 1.9% from nominal. Utilities are governed by ANSI C84.1 which specifies the voltage regulation of $\pm$5% from the nominal 240 V_{RMS} residential service voltage [40]. Therefore, the 1.9% deviation by the SGPN is an acceptable performance.

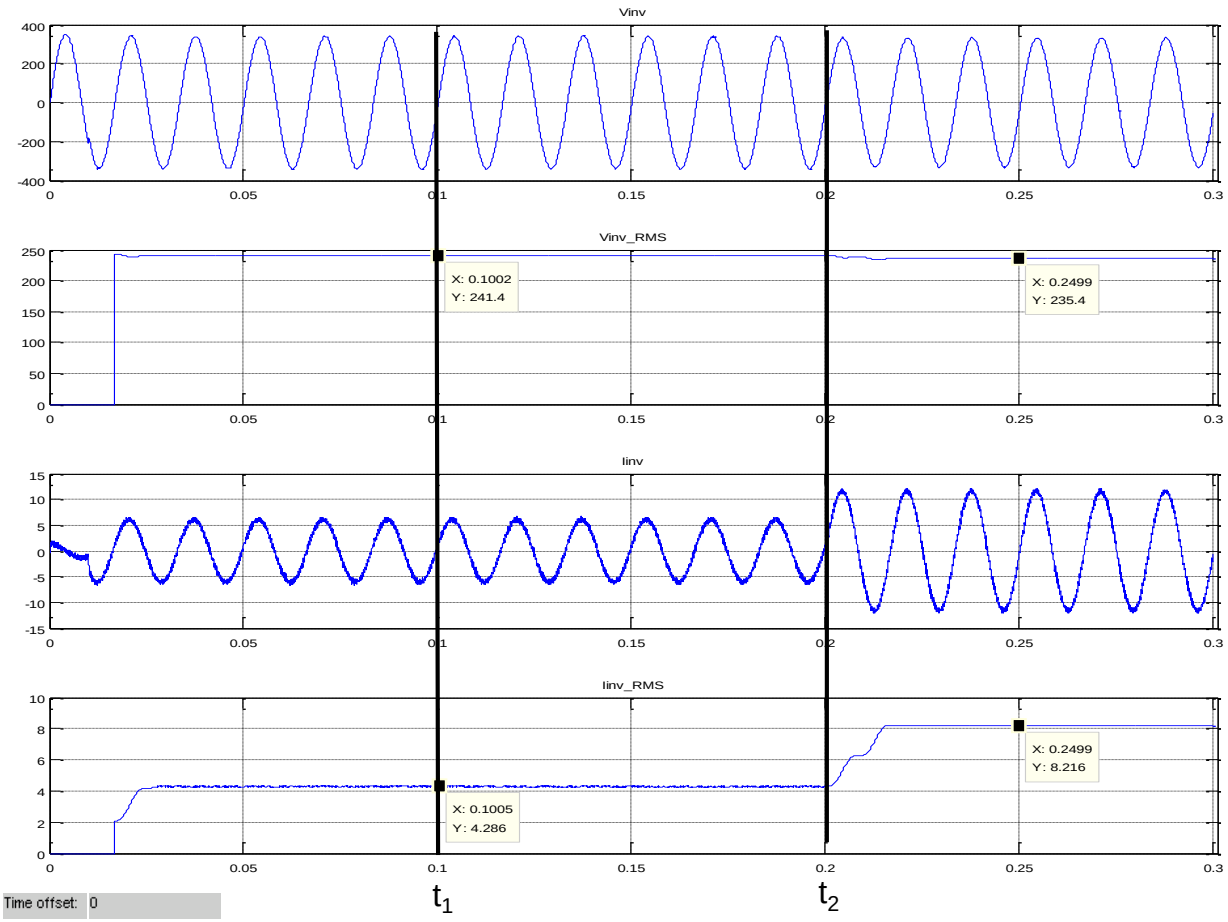

Fig. 4.5.9: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Step Load - AC Waveforms

The averaged power waveforms for the DC and AC systems are shown below in Fig. 4.5.10 which include the input power from the batteries and PV source, the total DC input power, and the output AC power. It can be seen that between time $(0 \leq t \leq t_2)$, the load power and input power is kept constant. Between $(t_1 \leq t \leq t_2)$ the input power is split between the PV and battery input power, thus sharing the load between the two converters. Finally, at (t_2) the step load is switched on and the 2 converters both contribute their rated power.

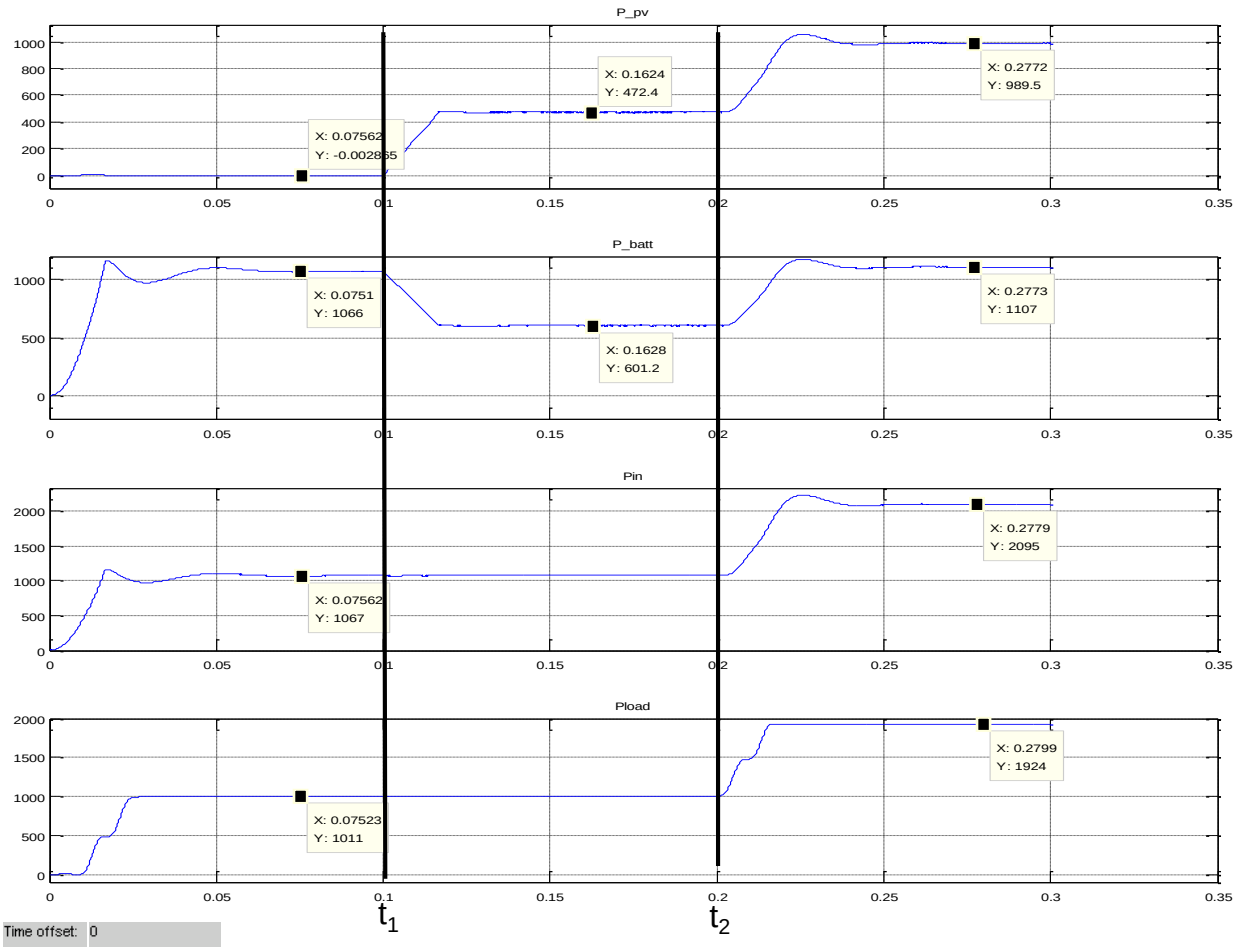

Fig. 4.5.10: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Step Load - Power Waveforms

The efficiency of the full SGPN at rated power is 91.8 %. This is quite a bit lower than the quoted average for a single source at 1 kW load. This is due to the fact that there are more switches in the system with interleaved inputs, which increases the switching losses. Additionally, the conduction losses through the FB DC-DC converter and inverter (12 switches) are increased with the additional 1 kW of load power demanded. These effects combined decrease the overall efficiency of the system.

4.5.2.1 THD Analysis

This section presents the FFT analysis of the SGPN system operation with interleaved DC inputs. The THD for the voltage is not expected to change with the increased load, but is

presented for completeness. This is shown below in Fig. 4.5.11. It can be seen the harmonic performance for the inverter voltage is very typical to what has been seen with similar simulations with a THD of 0.71%.

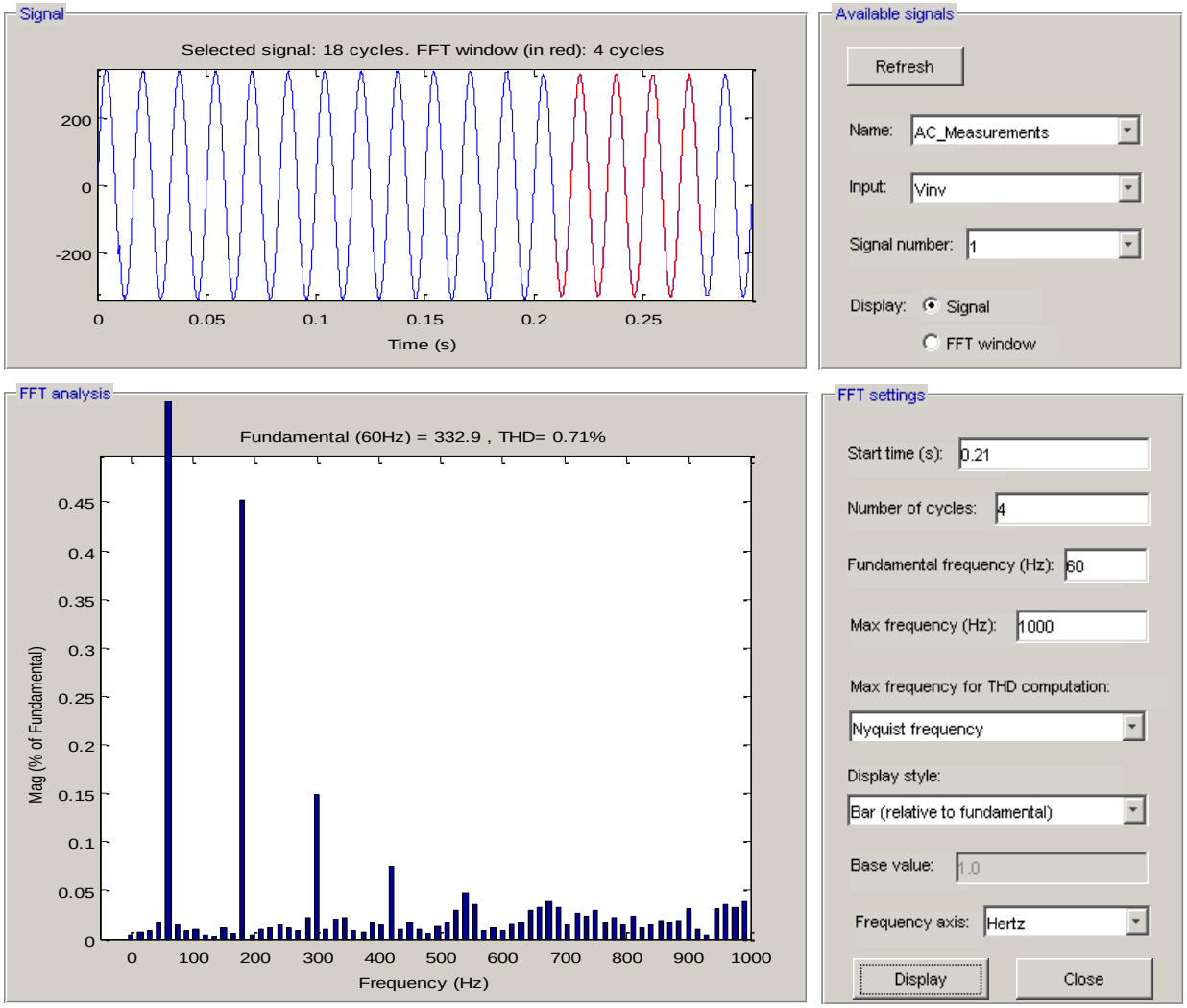

Fig. 4.5.11: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Step Load - Voltage FFT

The inverter current harmonic analysis for a 1 kW load has been presented, so those results are not restated. Only the FFT plot of the current for a 2 kW load is shown below in Fig. 4.5.12. It can be seen that for the rated load on the SGPN, the inverter passes the limits for harmonic distortion set forth by IEEE 1547. This prototype was a proof of concept and would be

scaled significantly in power level for a commercial product. It is unlikely the system would ever be so lightly loaded as examined in previous sections. Therefore the SGPN could pass requirements of IEEE 1547 with a certain minimum loading such as 2 kW. However, in order to be compliant, a solution to this problem should be implemented to meet THD requirements at lower power levels.

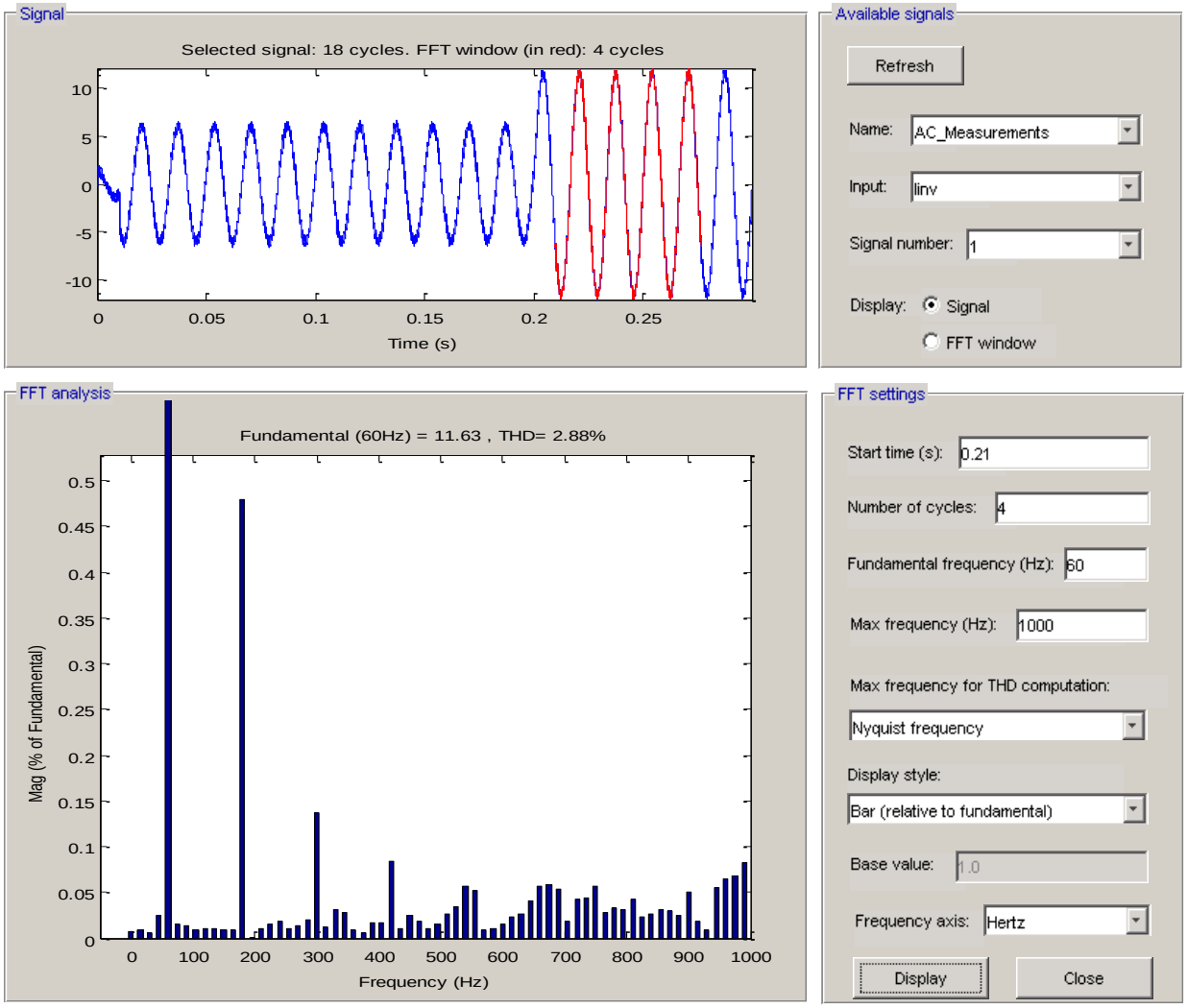

Fig. 4.5.12: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Islanded - Step Load - Current FFT

4.5.3 *Grid Connected Model: Power Sharing Static Load*

This section presents the simulation results for paralleled DC inputs power sharing with the full inverter in grid-connected mode. The power sharing network operation is independent whether islanded or grid connected. Therefore the same operation as in section 4.5.1 is applied here. This simulation demonstrates the ability of the hardware control network to distribute power flow throughout the SGPN, from each on-site resource input, and the grid. To demonstrate the basic full system operation fundamentals in grid-connected mode, a static load of 2 kW is assumed. While the SGPN is limited by its power rating of 2 kW, this load choice is arbitrary since the grid would serve any additional load which is shown in section 4.5.4.

The simulation timeline and source contribution is summarized below in Table 4.5.4. The SGPN was chosen to serve a constant 1 kW to the load with the grid serving the other 1 kW throughout the simulation. From $t_0 \leq t \leq t_1$ the batteries assume the full 1 kW load from the SGPN. At t_1 the power sharing network is initiated and from $t_1 \leq t \leq t_2$ the PV converter shares the 1 kW SGPN contribution by roughly half. At t_2 the PV converter shuts down (emulating a loss of solar power) and the batteries reassume full loading from the SGPN.

Table 4.5.4: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Static Load – Simulation Timeline

Load Contribution by Source and Switching Times				
Time	**Load**	**PV Power Supplied**	**Battery Power Supplied**	**Grid Power Supplied**
$0 \leq t \leq 0.1s$	2 kW	0 W	1 kW	1 kW
$0.1s \leq t \leq 0.2s$	2 kW	500 W	500 W	1 kW
$0.2s \leq t \leq 0.35s$	2 kW	0 kW	1 kW	1 kW

The DC waveforms for the above simulation are shown below in Fig. 4.5.13 which include the PV current, battery current, LV DC bus voltage, HV DC bus voltage, and the pulse that initiates the power sharing between the batteries and solar array. It can be seen the system takes roughly 80 ms to achieve steady state operation. This is due to the fact the load was applied

from t_0 with no soft start of the SGPN. This has been addressed in previous sections. The DC bus voltages exhibit stable behavior with transparent transitions through power sharing stages which means the system will operate seamlessly independent of source contribution. As indicated from table Table 4.5.4, prior to t_1 the batteries are supplying the full load as indicated from the zero PV input current. From $t_1 \leq t \leq t_2$ the load is shared which can be seen from the reduction in battery current and the increase in PV current. Finally, after t_2 the batteries resume the full load contribution from the SGPN.

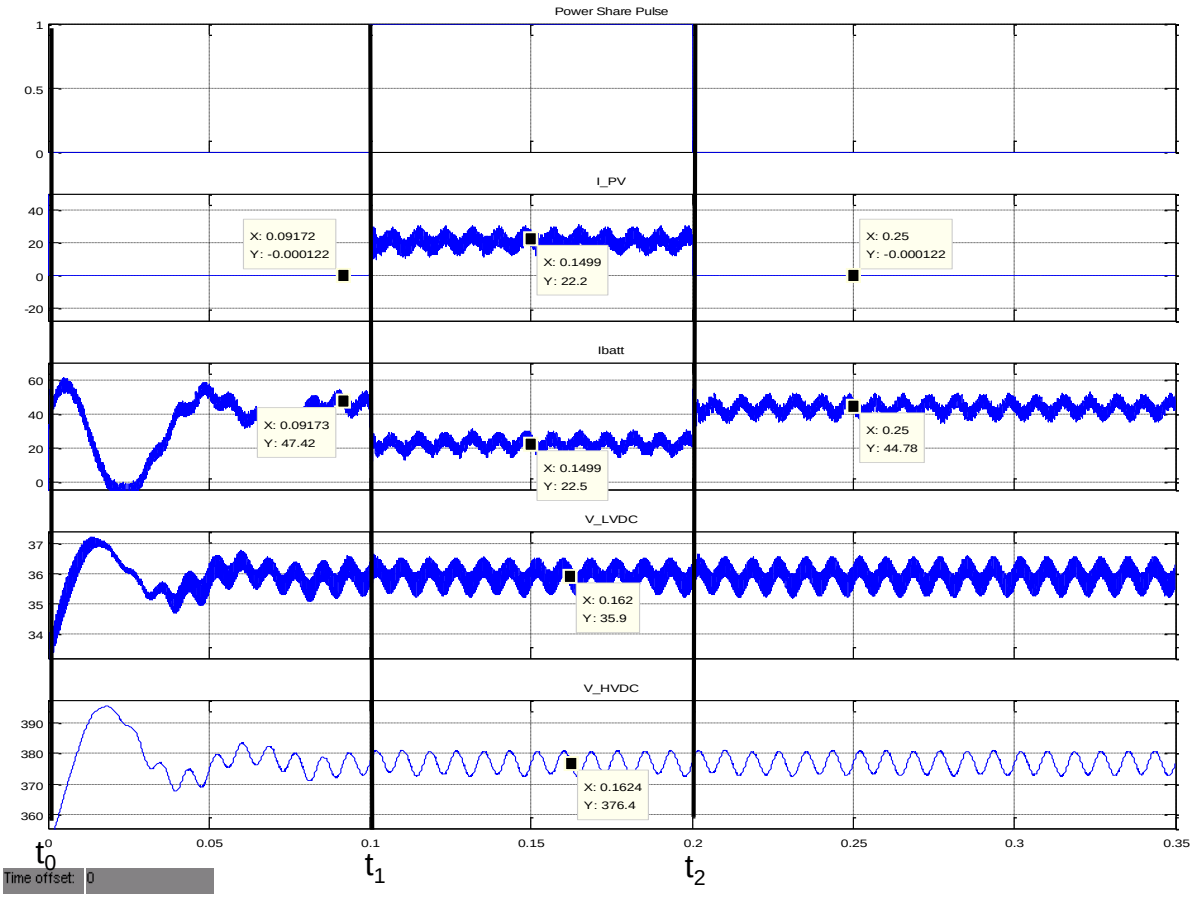

Fig. 4.5.13: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Static Load - DC Waveforms

The AC waveforms for this simulation are shown below in Fig. 4.5.14 which include the inverter voltage, inverter current, and grid current. The constant load of 2 kW is shared by the

grid and the SGPN equally (roughly). After t_0 when the system reaches steady state, it can be seen that the power sharing changes through t_1 & t_2 have negligible effects on the operation of the inverter. The inverter voltage has a value of 241.8 V_{RMS} (342 V_{pk}) which corresponds to an error of 0.75% from the ideal AC bus voltage of 240 V_{RMS}.

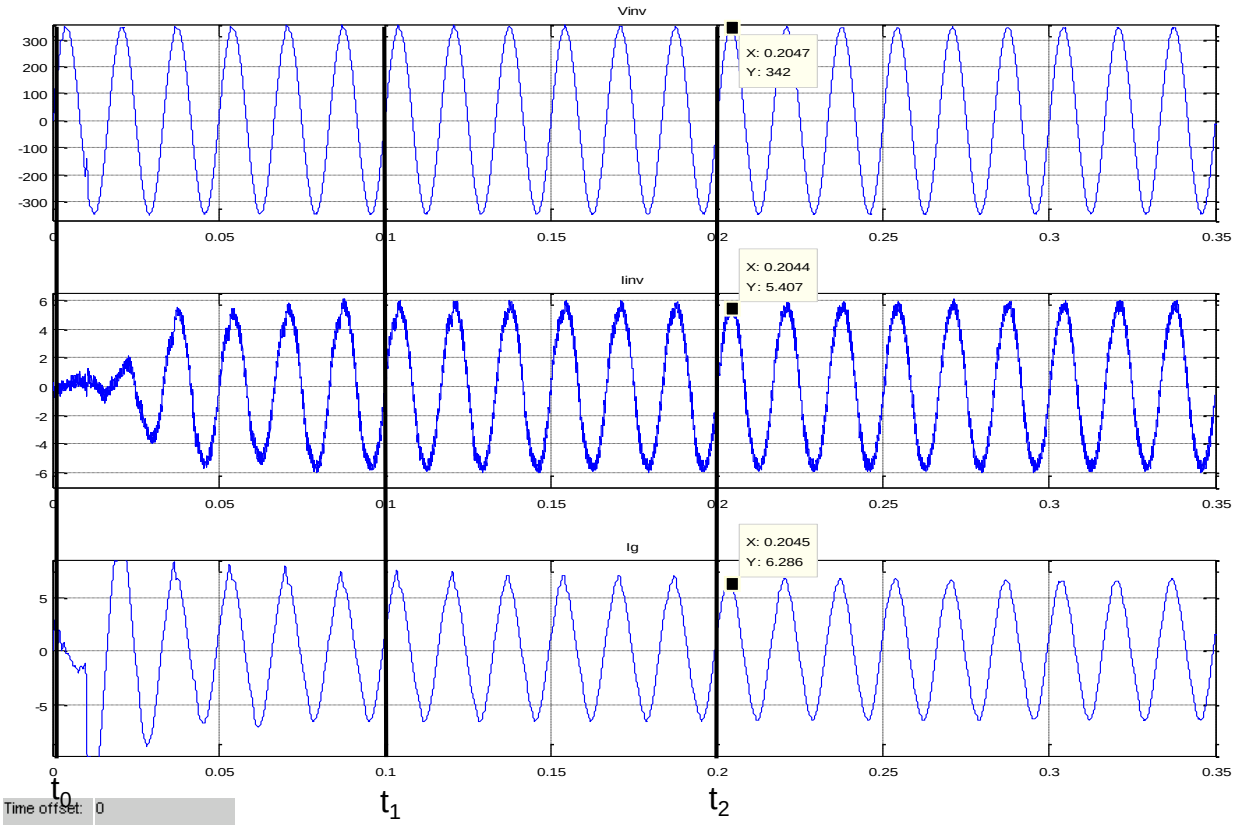

Fig. 4.5.14: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Static Load - AC Waveforms

The averaged power waveforms for this simulation are shown below in Fig. 4.5.15 which include the input power from the PV & batteries, the aggregate input power, AC power from the SGPN, and the grid power. From $t_0 \leq t \leq t_1$ the batteries and grid carry the load (after steady state). It can be seen that the grid initially serves the load while the SGPN is in its transient state, but quickly decreases as the SGPN recovers.

From $t_1 \leq t \leq t_2$ the batteries and PV share the 1 kW load contributed by the SGPN while the grid continues to serve the other 1 kW. Finally, the PV converter shuts down and the batteries resume the full 1 kW from the SGPN.

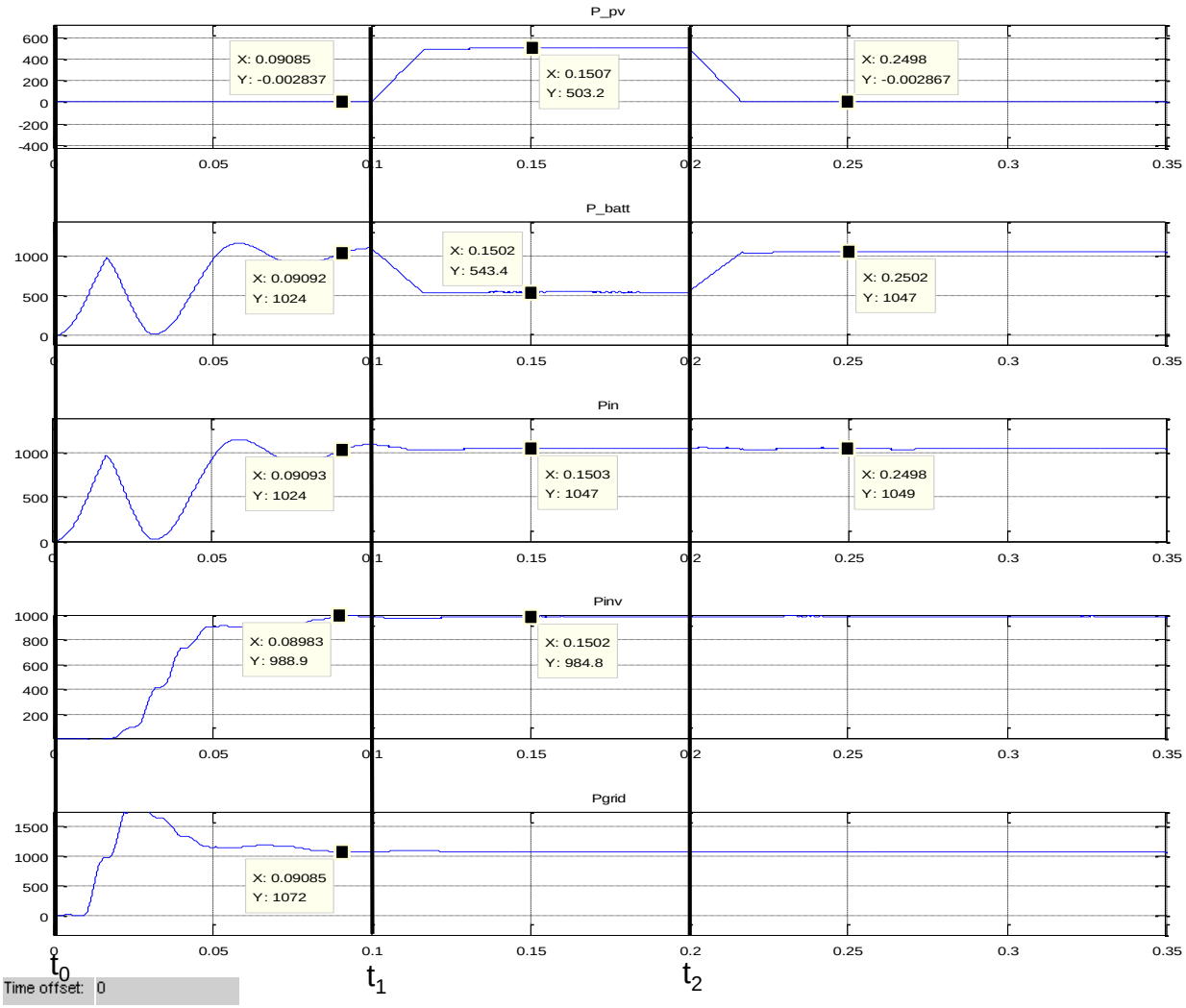

Fig. 4.5.15: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Static Load - Power Waveforms

The efficiency of the SGPN serving 1 kW of load from both on-site resource inputs is $Eff. = \frac{P_o}{P_i} * 100\% = \frac{984.8\,W}{1047\,W} * 100\% = 94.05\,\%$. This is comparable to the efficiencies quoted for the individual DC inputs with the full system. Even though there are losses added by

an extra switch in the system, the conduction losses are reduced compared with a single source converter. Thus, the effect is the efficiencies are very close to each other.

4.5.3.1 THD Analysis

For this simulation, the THD analysis of the inverter voltage and current under a 1 kW load are identical to section 4.4.1.1 & 4.4.2.1.1 therefore those results are not restated.

The FFT plot of the grid current is shown below in Fig. 4.5.16. Prior to this point, the grid current under a 500 W load condition was shown. It was seen that under that light load, the injected harmonics were unsatisfactory to IEEE 1547. It was discovered through simulation that at 1 kW, the grid harmonic content was reduced enough to pass the requirements of IEEE 1547 with a THD of 4.14 %, thus a minimum loading of 1 kW should be maintained in order to be in compliance.

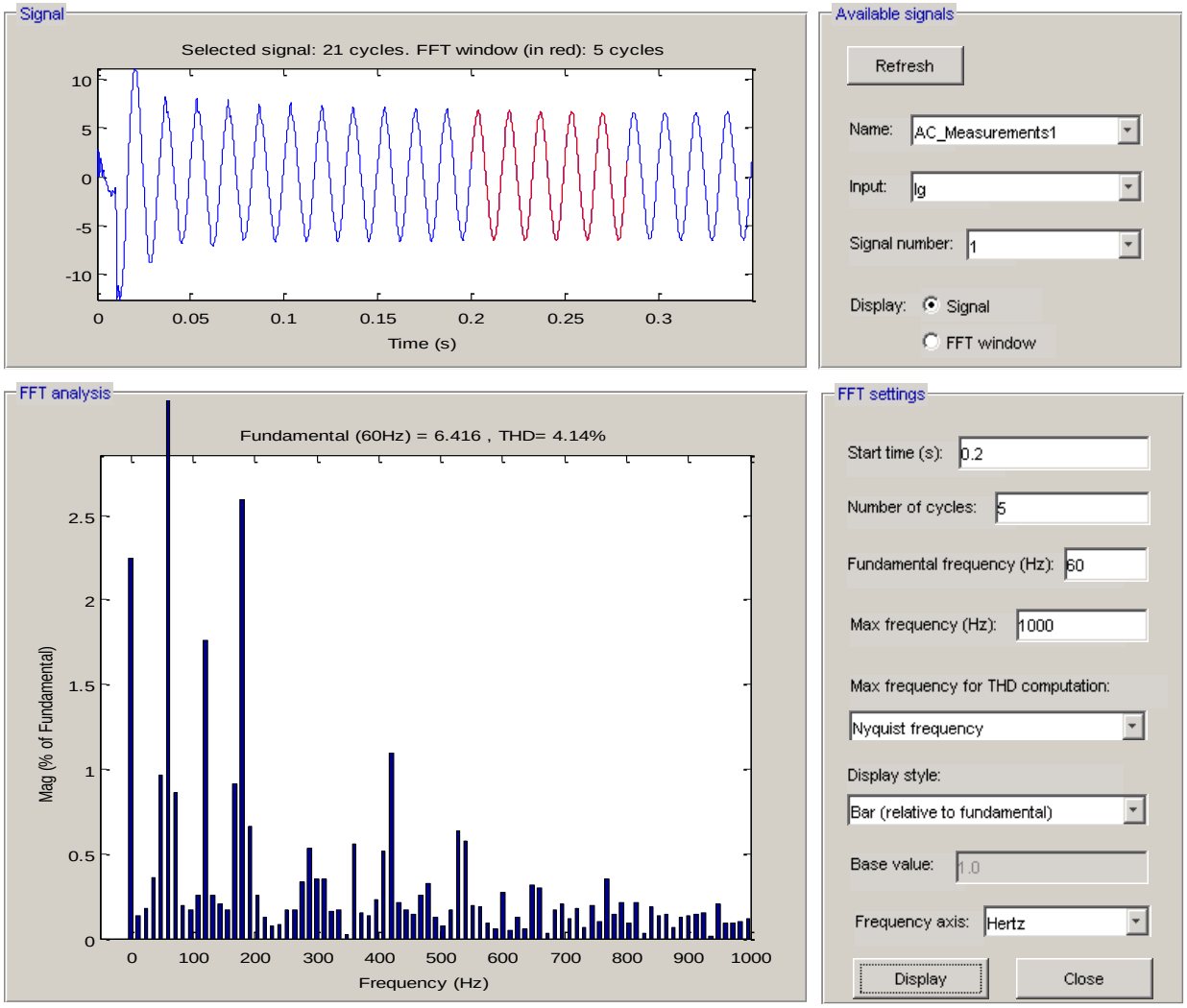

Fig. 4.5.16: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Static Load - Grid Current FFT

4.5.4 *Grid Connected Model: Power Sharing Step Load*

This section presents the interleaved DC inputs & full inverter grid-connected with power sharing and a step loading condition. This simulation shows the abilities of the hardware control network to handle DC power sharing, step loading, and power sharing between the electric grid & SGPN. It also verifies the claims made in section 4.5.3. The SGPN responds to dynamic power contribution references sent to its control network providing additional power, or reducing power output as commanded. Any additional loading experienced by the home will be supplied

by the grid. For example, at $t = 0.2s$ a step load of 3 kW is added to the 2 kW present. The SGPN is commanded to supply only an additional 1 kW.

The simulation timeline is summarized below in Table 4.5.5. Initially, the home load is 2 kW which is supplied by the batteries and grid equally. At $t = 0.1s$ DC power sharing is implemented in which the 1 kW from the SGPN is shared by the batteries and PV and the grid continues to supply 1 kW. Finally, at $t = 0.3s$ a step load of 3 kW is switched on where the grid supplies 2 kW and the SGPN supplies the remaining additional 1 kW.

Table 4.5.5: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Step Load – Simulation Timeline

Load Contribution by Source and Switching Times				
Time	**Load**	**PV Power Supplied**	**Battery Power Supplied**	**Grid Power Supplied**
0 ≤ t ≤ 0.1s	2 kW	0 W	1 kW	1 kW
0.1s ≤ t ≤ 0.2s	2 kW	500 W	500 W	1 kW
0.2s ≤ t ≤ 0.35s	5 kW	1 kW	1 kW	3 kW

The DC waveforms for this simulation are shown below in Fig. 4.5.17 which include the PV and battery current, LV DC bus voltage, HV DC bus voltage, and the pulse that initiates the DC power sharing network. This simulation is very similar to section 4.5.3 up to t_2 where the batteries supply the SGPN contribution to the load. At t_2 the 3 kW step load is applied in which the batteries and PV supply a combined 1 kW. This extra load is supplied equally since the maximum rating for each converter is 1 kW.

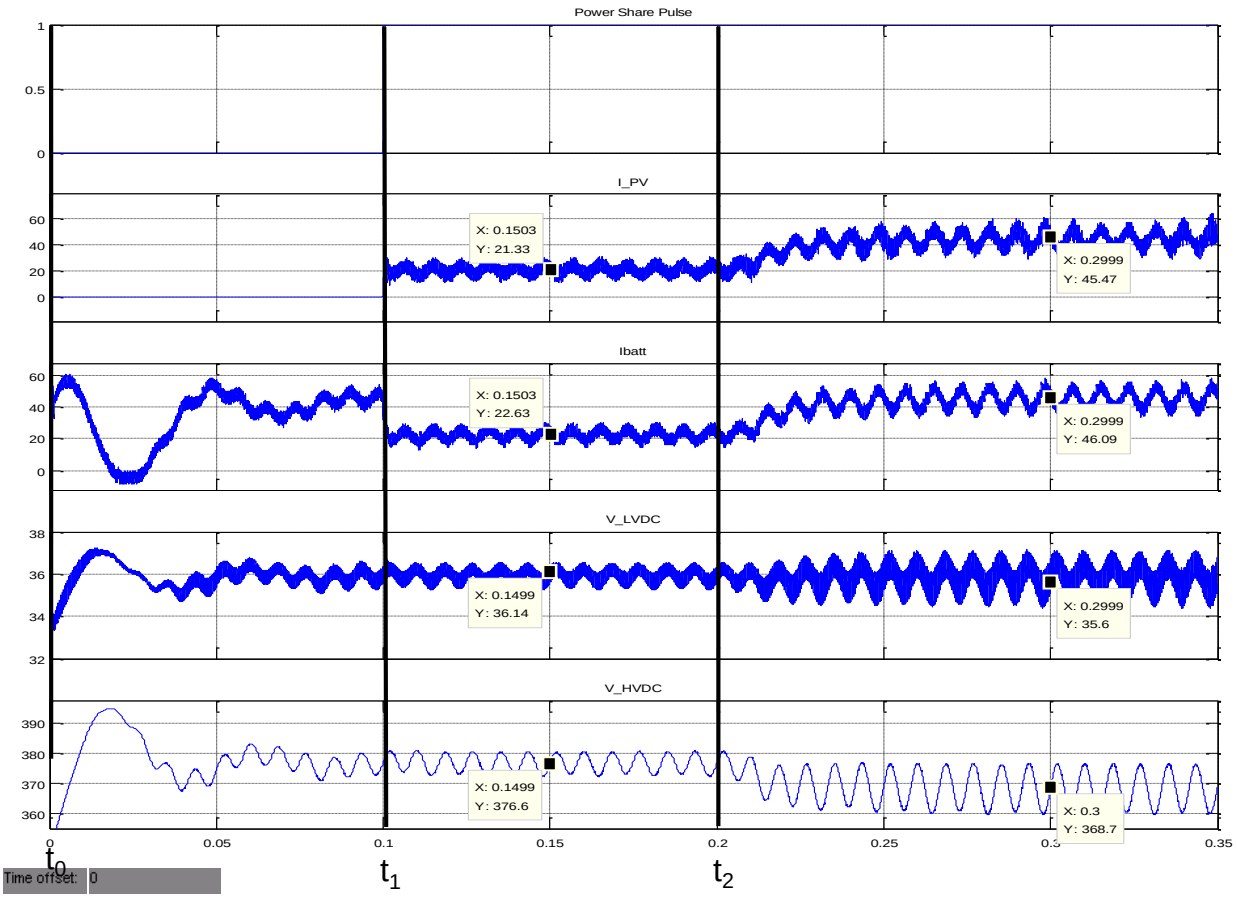

Fig. 4.5.17: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Step Load - DC Waveforms

The AC waveforms for this simulation are shown below in Fig. 4.5.18 which include the inverter voltage and current and the grid current. It can be seen from $t_0 \leq t \leq t_2$ the load remains constant, while at t_2 the step load is switched on. From inspection, after the step load the grid appears to immediately serve all additional loads. This is due to the fact that the SGPN controls require a brief transition period of time to reach steady state. For individual converters, this time period is very small and might go unnoticed. However, the full system operation incorporates many more individual controllers which make the delay more apparent. Nonetheless, after about 1 cycle the load distribution is as expected between the grid and SGPN.

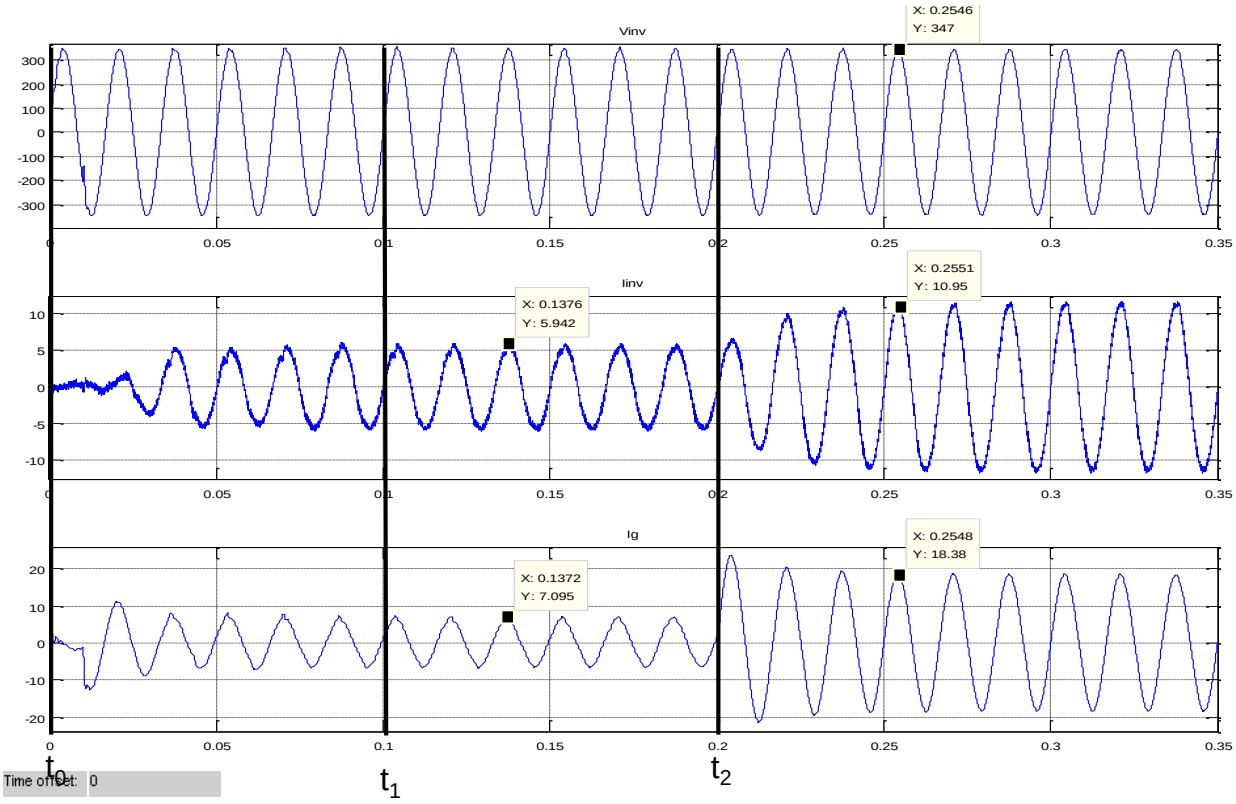

Fig. 4.5.18: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Step Load - AC Waveforms

The power waveforms that consist of input battery and PV power, total input power, SGPN delivered power, and grid power for this simulation are shown below in Fig. 4.5.19. Note throughout the simulation the input power equals (roughly) the sum of battery and PV input powers. Similarly, the load power from Table 4.5.5 is roughly equal to the inverter delivered power and the grid power.

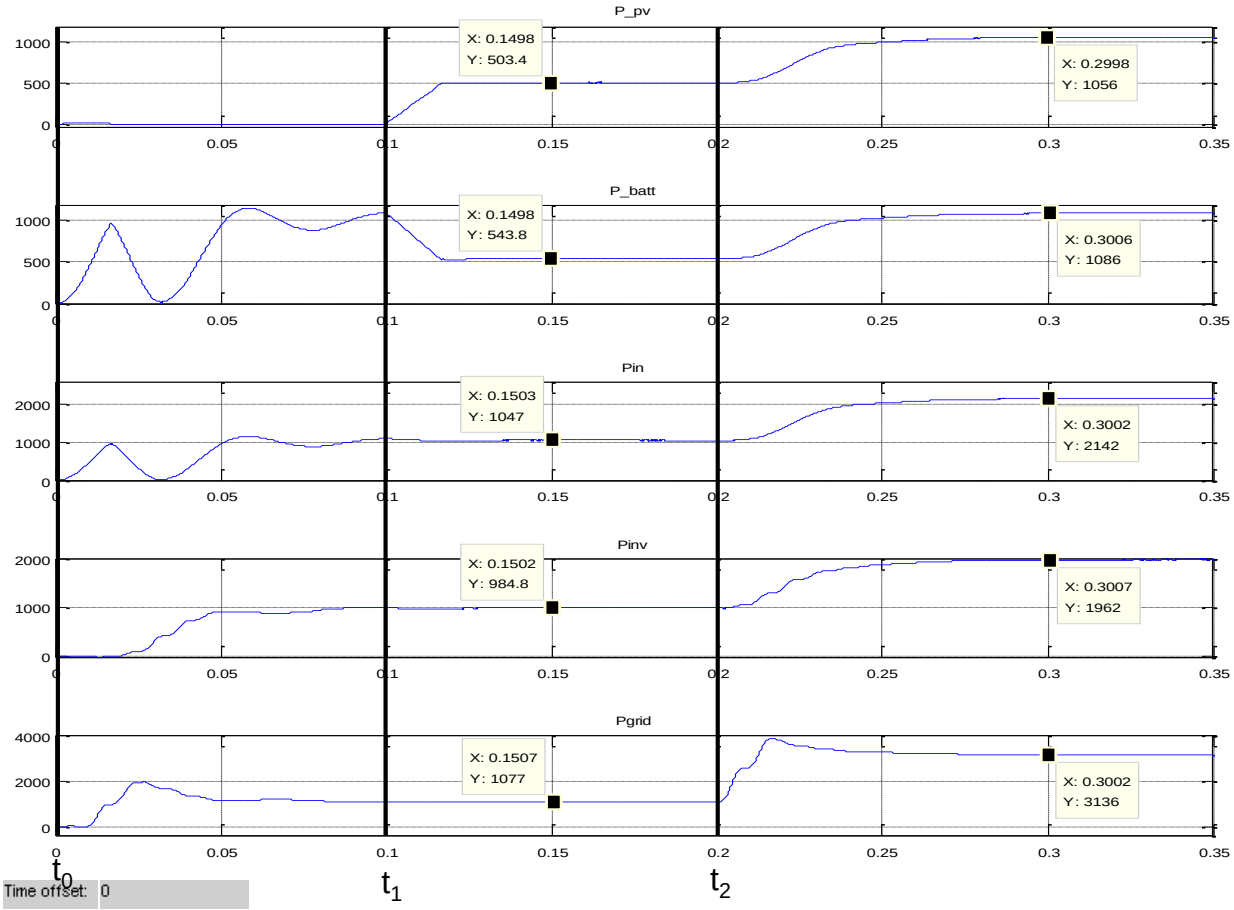

Fig. 4.5.19: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Step Load - Power Waveforms

It can be seen that the PV source supplies no power from $t_0 - t_1$ and the load is supplied by the batteries and grid only. At t_1 the PV shares the same 1 kW load from the batteries demonstrating power sharing. Finally at t_2 the step load is 3 kW making the full load of 5 kW in which the SGPN is supplying its rated 2 kW and the grid 3 kW. The net increase from the SGPN from $t_1 - t_2$ is 1 kW, while the net increase for the grid is 2 kW. This illustrates the SGPN's ability to accurately respond to dynamic power demand references while power sharing between DC-DC converters, the grid, and independent of step loads on the system.

The efficiency of the SGPN for this simulation is $Eff. = \frac{P_o}{P_i} * 100\% = \frac{1962\ W}{(1056\ W + 1086\ W)} * 100\% = 91.6\ \%$.

4.5.4.1 THD Analysis

The THD analysis of the inverter voltage and inverter current under these loading conditions has been presented and will not be repeated here. This section presents the harmonics injected into the grid under a higher loading condition. It was stated that the harmonic performance of both the inverter and grid currents were negatively affected under light loading conditions (smaller current amplitude) since the percentage of harmonic content on the fundamental was higher. The FFT plot for the grid current shown in Fig. 4.5.20 is taken when the grid is serving approximately 3 kW of load. It can be seen that the THD is 2.13% under this loading condition compared to 6.3% in section 4.4.2.2.1 when the grid was serving approximately 1 kW of load. This confirms the claim that with increased load the harmonic performance is improved because the distortion is a lower percentage of the fundamental at higher amplitudes.

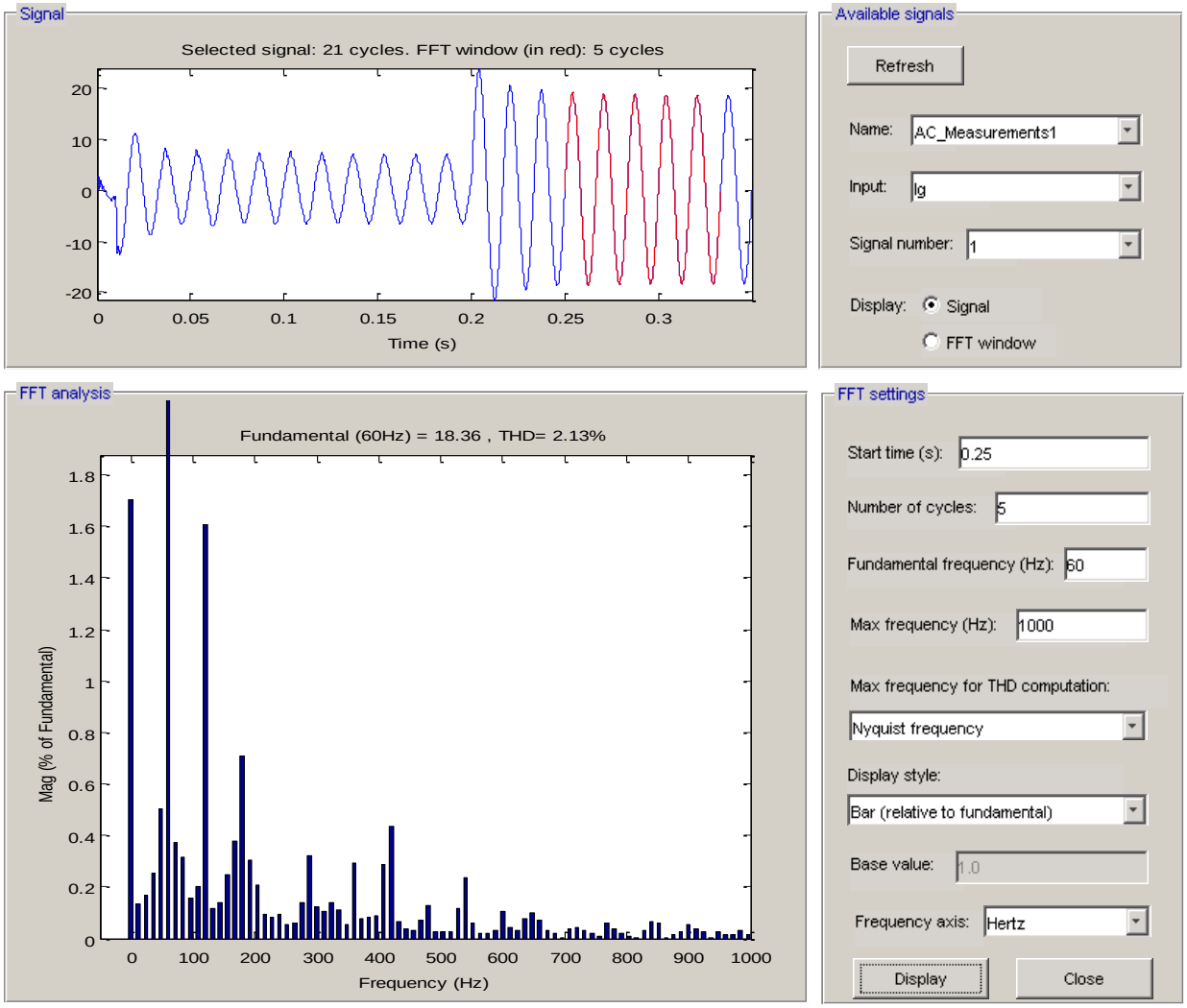

Fig. 4.5.20: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Grid-Connected - Step Load - Grid Current FFT

4.6 Operating Mode Transitions

Thus far the SGPN has demonstrated the ability for all individual closed loop converters to operate independently and handle step loading conditions. All closed loop sub-integration including the paralleled DC-DC converters with power sharing [11], and full inverter (FB DC-DC converter and H-bridge inverter) has been demonstrated with the full inverter operating in islanded and grid-connected modes. Full system operation including the PV boost converter + full inverter (islanded and grid-connected mode), battery charge/discharge converter + full inverter (islanded and grid-connected mode), and paralleled DC input converters (with power

sharing) + full inverter (islanded and grid connected mode) have also been demonstrated. All sub-integration and fully integrated simulations have shown the ability of the SGPN to handle static load, step load, grid power loading, and grid power sharing.

This section will present the SGPN during step loading commands, AC power sharing with the grid, DC power sharing between on-site inputs, as well as operating mode transitions. This not only demonstrates the above, but also emulates a sudden loss of grid power and re-connection to the grid once power is restored without a discernable load interruption.

4.6.1 *Islanded - Grid Connected - Islanded Operation Mode Transitions with Interleaved DC Inputs*

This simulation also combines many of the functionalities previously presented with mode transitions including DC power sharing, power sharing with the grid, dynamic power flow commands, and step loading. These results will be presented in the context of an example scenario that could apply during normal operation of the SGPN. It is recognized that the times quoted for some of the transitions operation are not practical. However, in order to show sufficient waveform detail in a single simulation, these are shortened to the "millisecond" timeframe. In actuality, these times would be much more extended.

The simulation timeline is summarized below in Table 4.6.1. Initially the system starts in islanded mode which assumes there has been a fault on the distribution system and either a distribution protection breaker has opened, a recloser has opened, or a protective fuse has blown. Prior to this event and from $t_0 \leq t \leq t_1$ the cloud cover has made the solar source unavailable as a power source. Additionally, the SGPN has already shed load to reduce the demand. During this first timeframe the batteries carry the load to the home of 1 kW.

Table 4.6.1: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Operating Mode Transition - Simulation Timeline

Load Contribution by Source and Switching Times					
Time	**Operating Mode**	**Load**	**PV Power Supplied**	**Battery Power Supplied**	**Grid Power Supplied**
(t_0) $0 \leq t \leq 0.05s$	Island	1 kW	0 W	1 kW	NA
(t_1) $0.05s \leq t \leq 0.15s$	Island	2 kW	1 kW	1 kW	NA
(t_2) $0.15s \leq t \leq 0.25s$	Grid-Conn.	3 kW	0.75 kW	0.75 kW	1.5 kW
(t_3) $0.25s \leq t \leq 0.35s$	Island	2 kW	1 kW	1 kW	NA

At t_1 the clouds have passed and the SGPN enters DC power sharing mode with the batteries and shares load. At the same time, the homeowner switches on an additional (step) load of 1 kW. The load is shared equally by half between $t_1 \leq t \leq t_2$. At t_2 the utility protective relaying or recloser applies the grid source after a temporary fault appears to have cleared. During this time the user preferences in the SGPN automatically engages more load since the primary (grid) source is restored. High level decisions by the system level controller dictate that the SGPN shares the load with the grid between $t_2 \leq t \leq t_3$. Finally, at t_3 the fault reappears and the SGPN islands from the grid when the outage is detected. During this scenario, the recloser or distribution circuit breaker is in its lockout state and will no longer reclose. Once again, the load is reduced to the rating of the SGPN through commands by the high level controller.

The DC waveforms associated with this simulation are shown below in Fig. 4.6.1 which include the battery and PV input current, LV and HV DC bus voltages, and the pulse that initiates power sharing between the DC-DC input converters. The system experiences some startup transients but settles to steady state just before t_1 in which the batteries are carrying the load indicated by the zero PV current. At t_1 the power share pulse is asserted while

simultaneously the step load of 1 kW is initiated (2 kW total). This is a special case since the very instant that PV power is available a step load condition is encountered. However, this shows the robust operation of the SGPN during this condition.

At t_2 the first reclose operation of the distribution system protection is initiated in which the grid source is now available. Three dynamic operations are being handled by the SGPN hardware here:

1. An operating mode transition is taking place from islanded to grid-connected mode.
2. A step load from 2 kW to 3 kW is happening.
3. The SGPN hardware control network is sent an updated power flow reference.

It can be seen the PV and battery current temporarily go to zero before supplying their updated power as commanded. The reason for this will be discussed below.

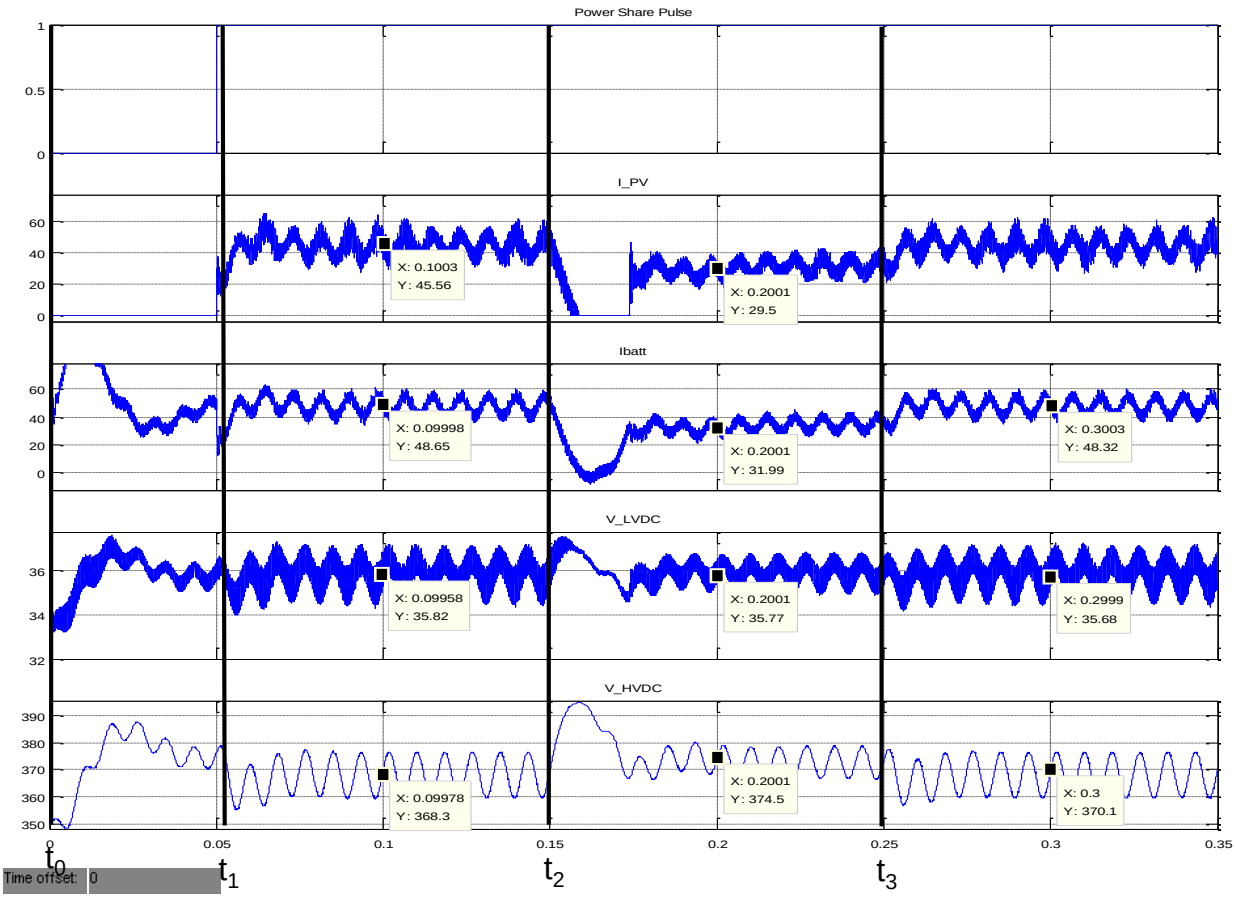

Fig. 4.6.1: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Operating Mode Transition - DC Waveforms

Finally, at t_3 the grid source is tripped off and the breaker or recloser locks out. During this transition the SGPN is again experiencing a mode transition as it islands from the grid. Additionally, the control network simultaneously processes a dynamic power demand reference and step load change.

The AC waveforms are shown in Fig. 4.6.2 below which include the inverter voltage and current and the grid current. The constant load from $t_0 \leq t \leq t_1$ can be seen as explained above. At t_1 the power sharing is initiated between the PV boost and battery converter while the step load is applied as indicated by the increase in inverter output current. From $t_0 \leq t \leq t_2$ it can be seen the system is islanded since there is no grid current.

At t_2 the system encounters the first step load as well as a mode transition to grid-connected. It can be seen that for a short period of time the inverter current is reduced to zero while the grid current temporarily has large amplitude. This is due to the fact the inverter controller is now using a reference that is in phase with the grid. Another source of this transient behavior could be the time delay associated with the grid-connected controls reaching steady state. As alluded to above the reason the DC input current goes to zero, during this timeframe is due to the transient state between the island → grid-connected transition.

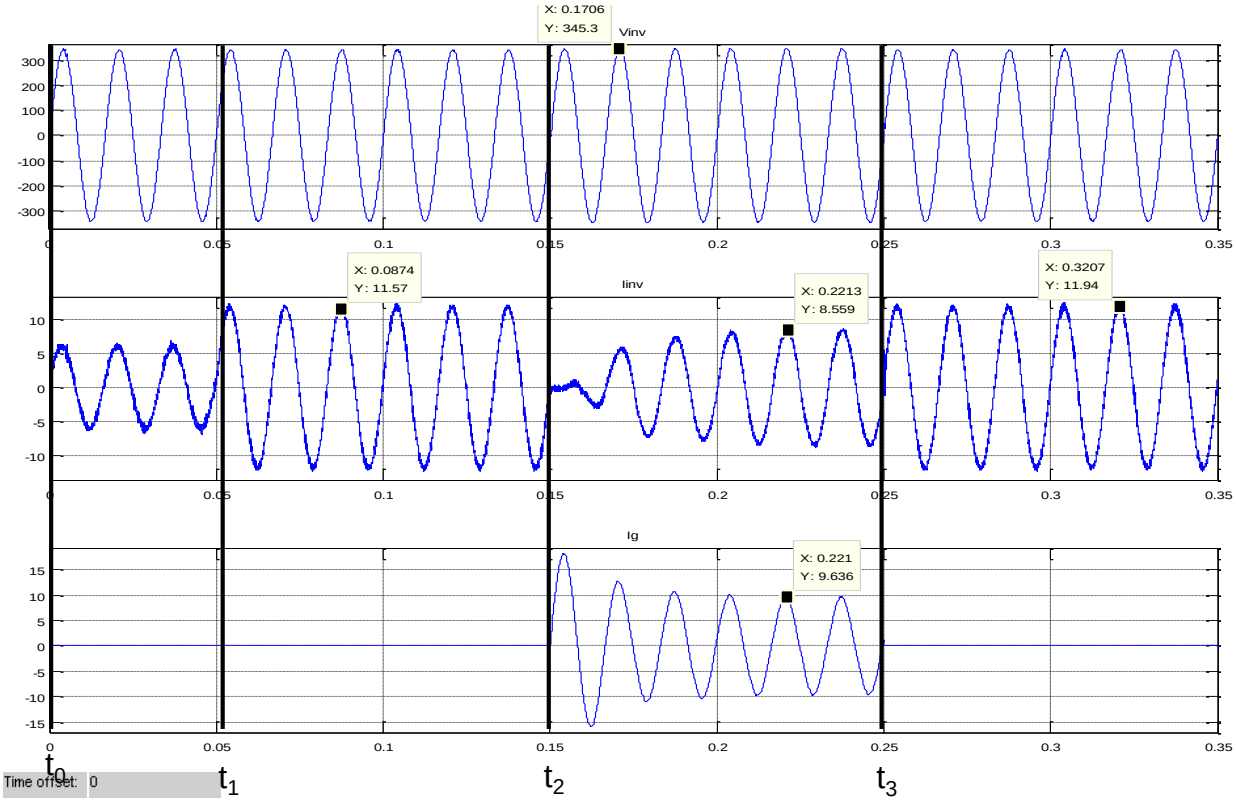

Fig. 4.6.2: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Operating Mode Transition - AC Waveforms

Finally at t_3 the grid trips off and the system resumes islanded operation. The transition from grid connected→ islanded operation is much smoother than the reverse transition. This is due to the fact that the load has no "preferred" phase relationship to the source. However, the grid phase synchronization is paramount to reduce the potential for damaging currents to the

SGPN hardware. As seen during other paralleled DC input system operation, the effect of a step load and updated power flow contribution is negligible on the output.

The power flow waveforms for this simulation are shown below in *** which include the battery and PV input power,, the aggregate input power from both sources, the SGPN total AC output power, and the grid power. This waveform is mainly shown to verify the power contributions and loading conditions set forth in Table 4.6.1. It should be noted that the total load power is the sum of grid and inverter output power. Similarly, the total input power is the sum of the battery and PV power.

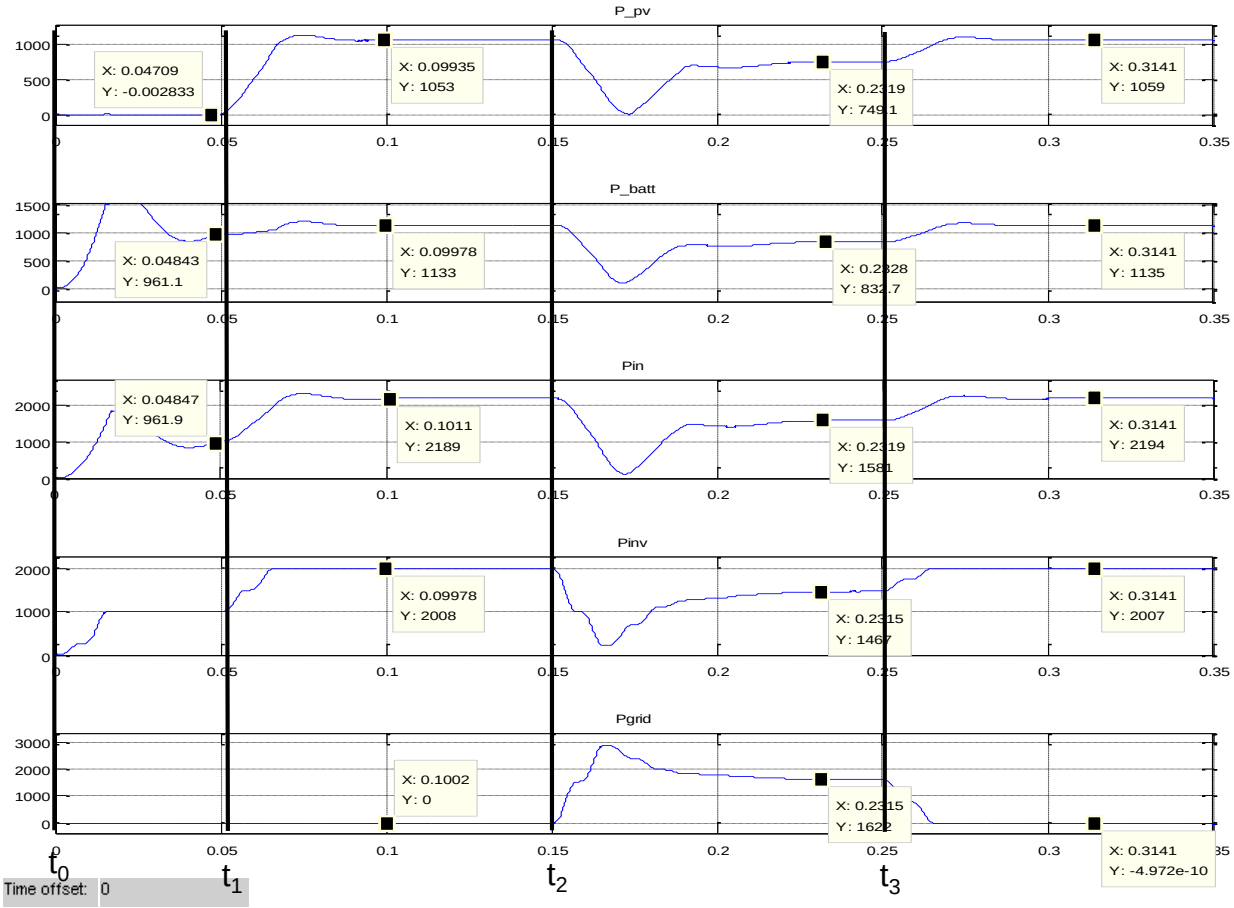

Fig. 4.6.3: Closed Loop PV Boost & Battery Charge/Discharge Converter with Full Inverter Simulation - Operating Mode Transition - Power Waveforms

During $t_0 \leq t \leq t_1$ the battery, input, and inverter power are roughly equal while the PV and grid power are zero meaning the load is served solely from the batteries. During $t_1 \leq t \leq t_2$ the load is increased from 1 kW to 2 kW. Since the grid power is still zero, and the total input power roughly equals the inverter power, this means the system is still islanded and the two DC inputs are sharing load. Similarly, from $t_2 \leq t \leq t_3$ all three sources share the load equally. That is, the SGPN total power supplied is roughly equal to the grid power serving the 3 kW load. Finally, after t_3, the grid power returns to zero, the load is reduced to 2 kW, and is served by the batteries and PV.

CHAPTER 5

CLOSED LOOP HARDWARE EXPERIMENTAL RESULTS AND DISCUSSION

This section contains the relevant experimental results obtained for the remaining individual and integrated Smart Green Power Node hardware in addition to design changes based on issues encountered through testing. Note all open loop converter test results and most closed loop individual converter test results were completed in [11] which should be referenced for detailed analysis of those results.

5.1 Isolation Board

Through initial fully integrated testing of the SGPN, a significant vulnerability was discovered that resulted in failure of some hardware components including the power control platform used to do sensing and signal processing, as well as several power devices. Testing of individual converters and even some sub-integration had been completed without any indication of issues. However, after much investigation, it was determined that switching operation of the full system produced and propagated large enough amounts of EMI to cause device failure.

The early version of USC's universal power control platform used for the SGPN did not include any isolation or protection on board. Therefore the control board circuitry was directly exposed to noise on the power circuit boards. EMI induced large enough voltages on the control signals to cause unintentional switching transitions leading to device failure as well as destruction of control board components.

Isolation is an important requirement with any power management system which should be carefully handled. The multiple signal types required for the SGPN system such as switching power supplies, low-signal analog, and digital presents a very high susceptibility of signal interference. It was determined a digital isolation board was necessary to protect hardware. Ferrite cores were also attached to the signal leads on the power device side of the isolation to

mitigate whatever noise was being induced on control signals after the isolation barrier. In addition to protecting hardware, isolation results in better switching performance and more stable output waveforms.

Fig. 5.1.1, taken from [11], is a standalone test of the MOSFET gate drivers used for the FB low side devices. Two MOSFETS were arranged in a half bridge configuration and the gate drivers were driven at a constant duty cycle. CH1 (yellow) shows V_{GS_LS}, CH3 (purple) shows V_{GS_HS}, and CH4 (green) shows the bootstrap capacitor voltage for the gate driver (used to drive the high side device). The over-voltages seen in Fig. 5.1.1 below are a result of EMI caused from the switching transitions and parasitic inductance loops from this simple test. It is easy to see how EMI can become a significant problem in a complex system with multiple power stages. Therefore there is a need for isolation and mitigation techniques.

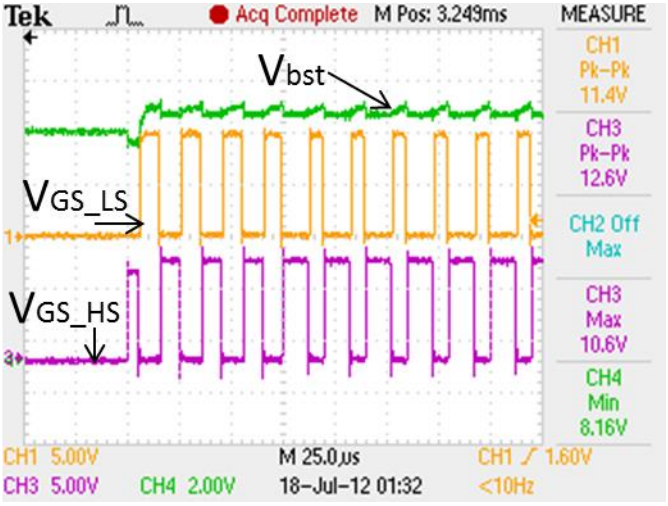

Fig. 5.1.1: Half-bridge Configuration Device Switching - No Isolation

An example showing the benefits of isolation for signal integrity is shown below in Fig. 5.1.2. These are the FB DC-DC converter PWM waveforms output from the control board to the isolation board during a fully integrated test. It can be seen that the signal integrity is excellent since all noise from the power side is isolated from control signals.

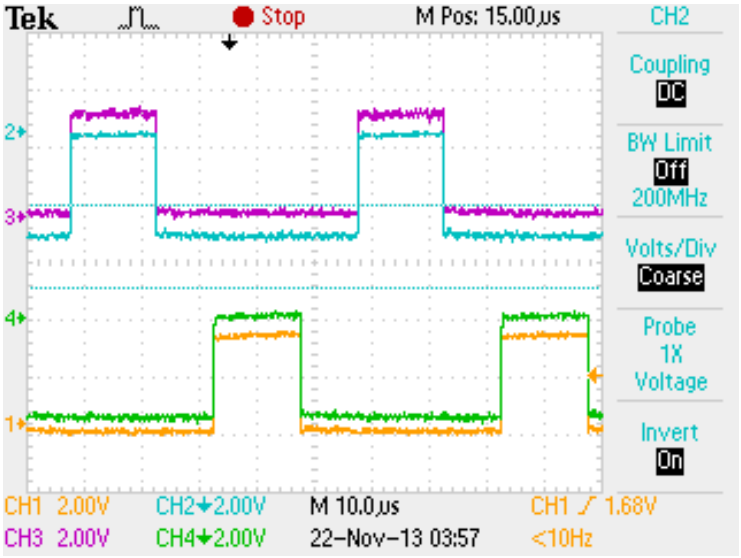

Fig. 5.1.2: Full-bridge DC-DC Converter Device Switching Drive – with Isolation

Fig. 5.1.3 shows the gate signals of the low voltage MOSFET devices on the FB for the same test setup as Fig. 5.1.2. It can be seen that the benefits from the ferrite core suppression of EMI and isolation yield drastically cleaner control signals and thus device switching. Another mitigation technique is to reduce the turn on time ($\frac{dv}{dt}$) of the device. This was implemented by adding a gate resistance in series to the device. However, this technique increases switching losses. There is a design tradeoff here between efficiency and signal integrity.

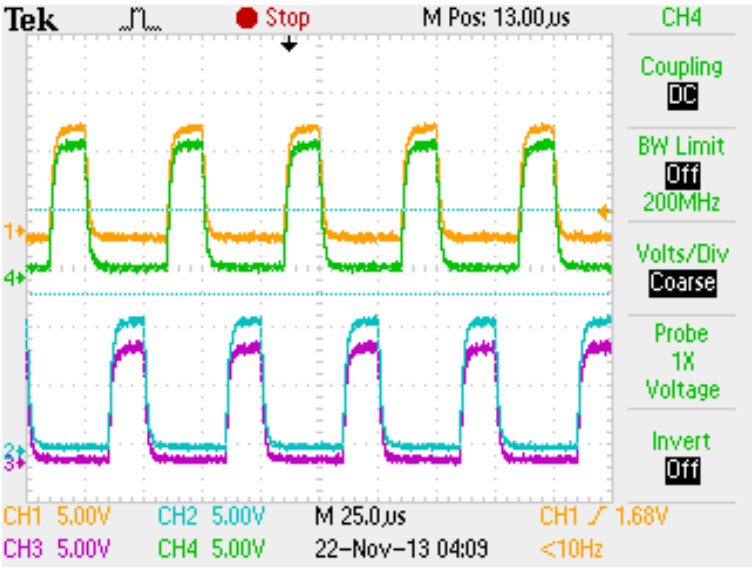

Fig. 5.1.3: FB DC-DC Converter Device Gate Signals - with Isolation

An in depth discussion on all possible causes and effects of EMI is beyond the scope of this thesis. However, there are several key factors that could be improved to improve the EMI performance of the system. A re-design of the power layout might be a more effective solution by reducing parasitic loops. For example, dedicated layers should be designated for sensitive signals such as digital control and measurement signals, separate from switching currents. This can reduce both radiated and conducted emissions. Another topic of EMI consideration is the physical connection between hardware. For instance, proper use of twisted “go and return” pairs and shielding will have a huge impact on EMI performance.

5.2 Full-Bridge DC-DC Converter

[11] showed the experimental results of the conventional full bridge PWM switching scheme and documented the limitations. This section will show the implementation of the phase shifted PWM switching scheme and demonstrate the ability to control the duty cycle across the transformer.

5.2.1 *Phase-Shifted Gate PWM signals*

The device gate waveforms for the phase-shifted PWM switching scheme where CH1(yellow) is V_{gs_Q1}, CH2 (blue) is V_{gs_Q2}, CH3 (purple) is V_{gs_Q3}, and CH4 (green) is V_{gs_Q4} is shown in Fig. 5.2.1.

It can be seen that the principle of phase shifted PWMs is implemented here. From "t_0" to "t_1" Q_1 and Q_4 are both high thus applying the DC link voltage across the transformer. From "t_1" to "t_2" the two high side devices (Q_1 and Q_3) are shorted forcing the voltage across the transformer to 0 V. Similar functionality is applied for the negative half cycle where Q_2 and Q_3 conducting will apply the negative DC link voltage to the transformer and shorting Q_2 and Q_4 will force the zero voltage across the transformer. In this way, changing the phase delay between the respective switch PWMs, the duty cycle across the transformer is controlled.

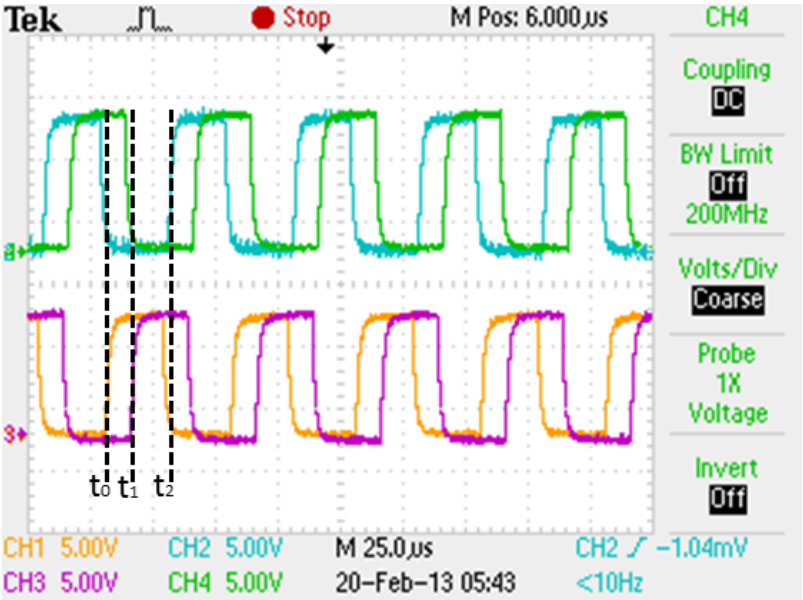

Fig. 5.2.1: Phase-shifted Gate Signals to FB DC-DC Converter

Fig. 5.2.2 shows a similar waveform to Fig. 5.2.1 with the same signal definitions. It more clearly shows that both top and bottom switches of a single half bridge are never turned on

at the same time, illustrating that this phase-shift control is implemented without violating the basic operation principles of an H-bridge.

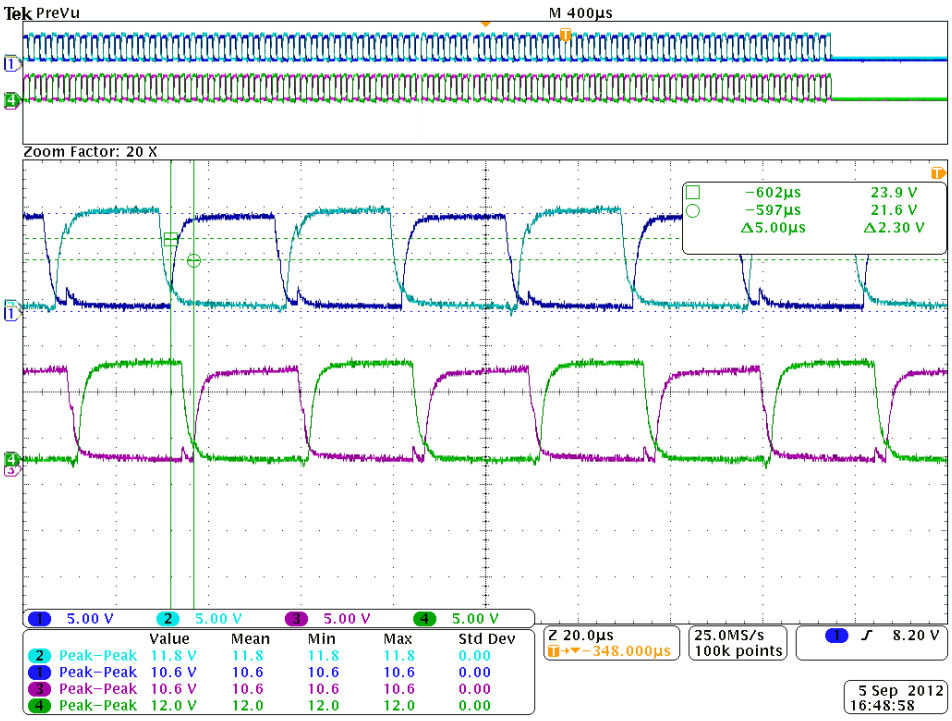

Fig. 5.2.2: FB DC-DC Converter Device Switching - Phase-shifted

5.2.2 *Phase-Shifted PWM Dual Full Bridge DC-DC Converter Test Results*

This section presents the waveforms for the phase-shifted PWM control of the dual FB DC-DC converter. To verify this operation a DC supply was connected to the LV DC microbus with a light resistive load connected at the HV DC bus. This test could have been run with no load on the converter, but in order to recreate the problem noted in section 3.2.1, a load resistor of 1000 Ω was chosen. The average power dissipated in the resistor at 350 V is simply $P_{Rdc} = \frac{V^2}{R} = \frac{350V^2}{1000\,\Omega} \approx 123\,W$ thus satisfying the "light load" condition.

The MSO400 series scopes from Tektronix have grounded probes and cannot be directly used for measuring differential signals. Channels 1 & 2 are measuring the negative – GND

potential and positive – GND potential on the secondary output of the transformer, respectively. The math function (red) of the scope is then applied to give the differential voltage.

The manufacturer of this HF transformer, Payton Group, only guarantees the transformer will achieve the minimum specified secondary voltage under full load which accounts for losses in the windings. Under light loading conditions, the losses are less and therefore the output voltage is larger. The calculation of the HV DC voltage is given by eq.$V_{HV_{DC}} = V_{LV_{DC}}[N * 2D]$ (5-1).

$$V_{HV_{DC}} = V_{LV_{DC}}[N * 2D] \tag{5-1}$$

where N is the turns ratio of the transformer and D is the duty cycle applied across the transformer.

The waveforms for this test are shown below in Fig. 5.2.3. It can be seen that the duty cycle applied across the transformer is well below the 0.45 seen with the conventional switching scheme [11]. For an input of 31.4 V the HVDC link is around 356 V which yields an effective "N" of around 11.35. This is adjustable by changing the delay time between the respective switches. This is a significant reduction from the "N" of 13.7 observed for the conventional switching scheme. This test demonstrates that the new switching scheme can reduce the resulting output DC voltage to a safe level, thus reducing the danger of damaging the hardware. Further, this solution was achieved purely through a software change which adds no cost to the prototype.

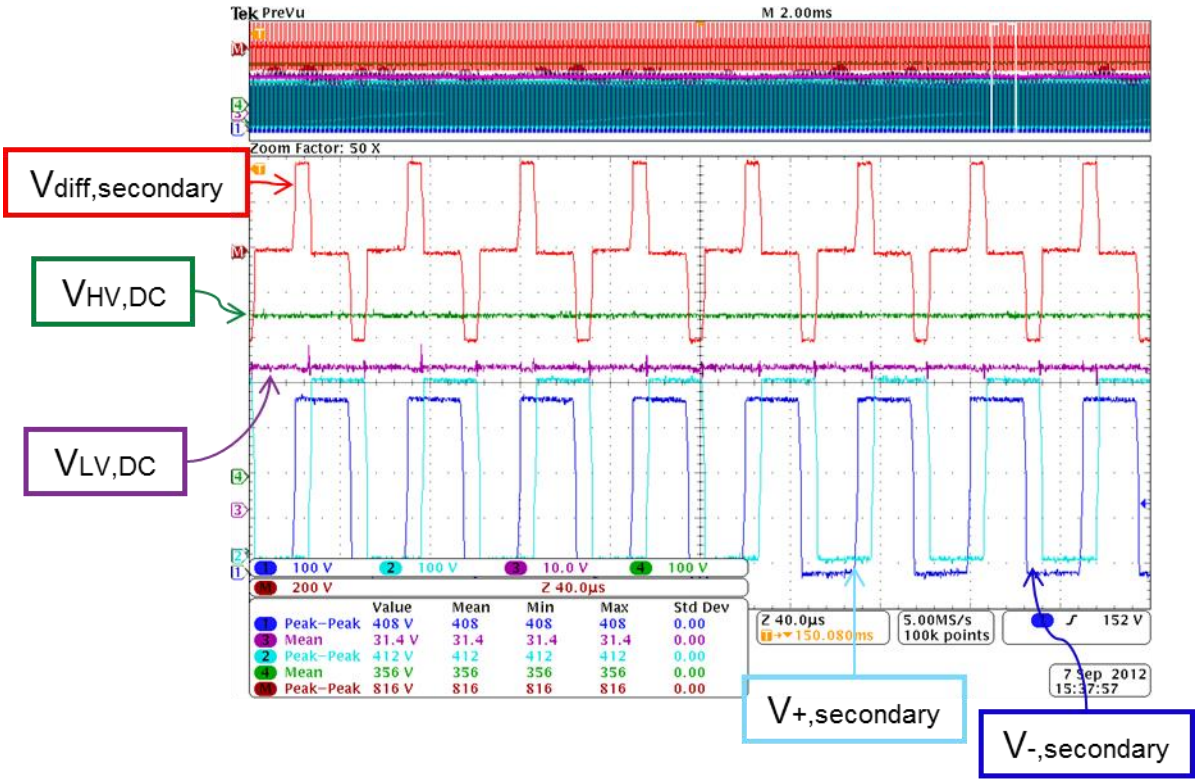

Fig. 5.2.3: Phase-sifted FB DC-DC Converter Test Waveforms

5.3 H-Bridge Inverter (Island Model)

Waveforms demonstrating the closed loop operation of the inverter are shown below in Fig. 5.3.1. In order to safely verify closed loop stability for initial testing, the inverter was operated at a reduced voltage. The full scale functionality of the inverter will be demonstrated in section 5.4 .

A DC supply was connected to the HV DC bus with a simple resistive load at the output to conduct the standalone inverter test. The input DC voltage to the inverter is shown in blue (CH2), the output voltage is shown in yellow (CH1), the output current is shown in green (CH4), and the unfiltered output voltage is shown in purple (CH3).

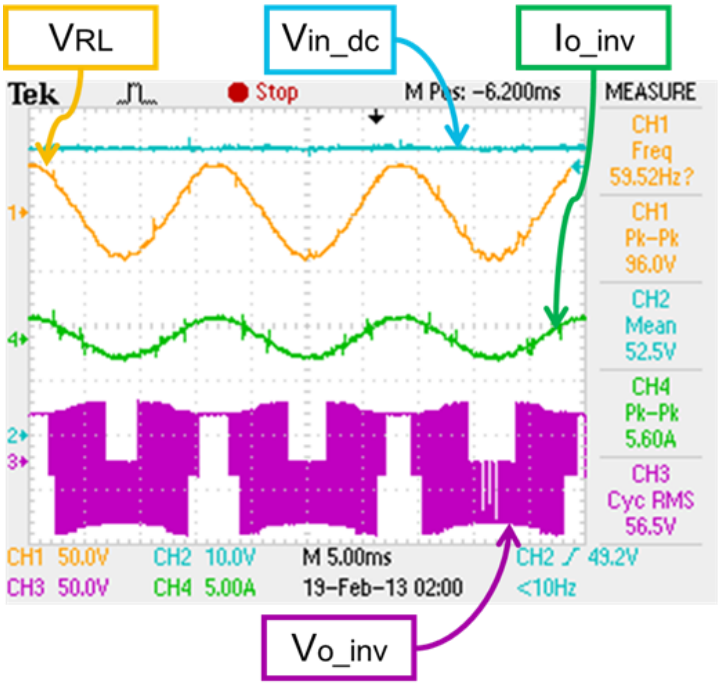

Fig. 5.3.1: Closed Loop H-bridge Inverter Test Waveforms – Static Load

It can be seen that the sine modulated PWM output voltage measured before the LCL filter has a large amount of high frequency switching noise, as expected. The filtered output voltage and current have a very low THD thus showing low noise propagation. From inspection, the output voltage does not exactly match the reference amplitude (100 V_{pk-pk}) entered into the control loop.

This can be explained by 3 things. First, when a sinusoidal varying reference is given, a simple PI controller cannot track with 0% error as with DC signals. Thus, the output will always lag the reference voltage by some amount. Second, the tolerances used in the scaling resistive divider for sensing will affect the accuracy of the sensed output voltage. Third, the voltage drop from the point of measurement to the input of the ADC in the DSP will have an effect on accuracy. These factors can all introduce error into the experiment which will be discussed further in 5.3.1. Eq. $\%error = \frac{V_{ideal}-V_{measured}}{V_{ideal}} * 100\% = \frac{50\,V_{pk}-48V_{pk}}{50\,V_{pk}} * 100\% = 4.0\%$(5-2)

shows the error between reference and measured voltage. It should be noted this is a great illustration of the difference between theory, simulations, and practical implementation.

$$\%error = \frac{V_{ideal} - V_{measured}}{V_{ideal}} * 100\% = \frac{50\,V_{pk} - 48V_{pk}}{50\,V_{pk}} * 100\% = 4.0\% \qquad (5\text{-}2)$$

The next step in verifying the closed loop stability of the inverter is to perform a load transition. Waveforms illustrating the overall step loading behavior over several cycles are shown in Fig. 5.3.2. Before "t_{step}" the inverter is supplying a constant resistive load of 20Ω. Utilizing one of the SGPN's load disconnect switches, to emulate step loading/load shedding, at "t_{step}" another 20 Ω resistor is switched on in parallel (R_{eq} ≈10 Ω).

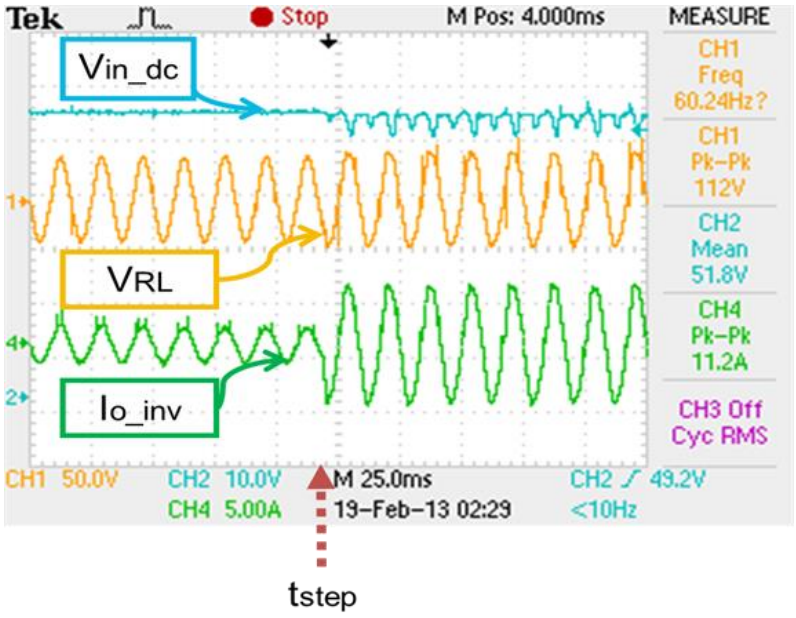

Fig. 5.3.2: Closed Loop H-bridge Inverter Test Waveforms - Step Load

Fig. 5.3.3 shows detailed waveforms for an identical test. It can be seen the inverter controller responds to this step load in approximately 200 µs (< 1% of one 60 Hz cycle) which is an excellent response time for this application. This demonstrates that the controls are closed loop stable and can handle step loading.

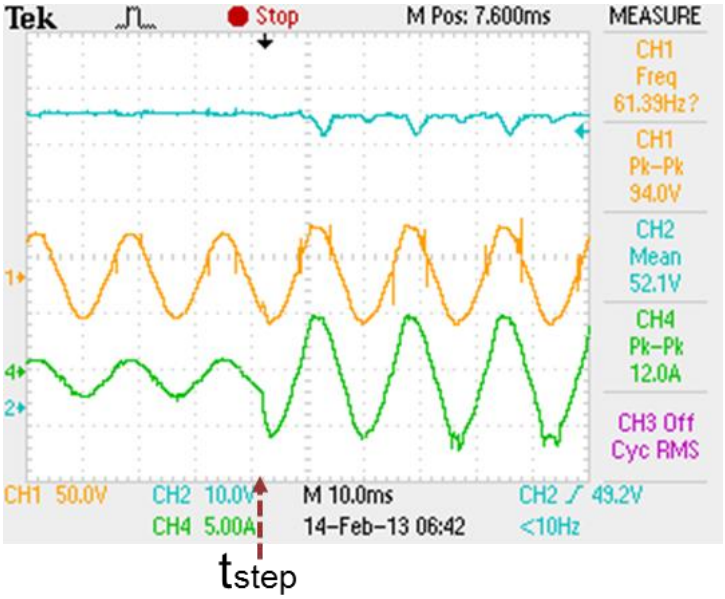

Fig. 5.3.3: Closed Loop Inverter Step Load - Zoomed In

It should be noted that after the step load the input DC voltage dips at the peaks of the output voltage waveform. This is due to two things: First, the output power rating of the DC supply being used at the time was approaching its maximum, thus when the "peak" current was drawn, the voltage dipped slightly. Second, this test was performed with the undersized capacitor of the original design. The energy storage capability of this small capacitor did not have the capacity to supply this momentary amount of energy.

5.3.1 *Experimental Testing Consideration and Analysis*

Initial testing of the closed loop inverter presented an interesting challenge. A significant difference in the set reference voltage amplitude and measured output voltage amplitude was noticed. In control system design, it is not uncommon to tune the initial design to actual hardware dynamics in testing, so inverter controls were manipulated in an attempt to find better suited control values. However, the desired signal was never achieved through this method alone.

Further investigation was conducted revealing testing conditions that were not previously taken into consideration.

The sine generator for the inverter outputs a reference signal between (-1,1) at the frequency programmed (60 Hz). Therefore, in order to achieve the correct output voltage, a gain must be applied to that signal directly proportional to the desired output voltage. Eq. $V_{o_{inv}} = KV_{sin}$ (5-3 shows this very simple calculation where K = 50 for this test.

$$V_{o_{inv}} = KV_{sin} \tag{5-3}$$

For feedback control, the voltages and currents of the inverter must be measured. The DSP can only sense signals within its power supply rails. If an AC signal is input directly to the DSP, it will clip the negative half cycle at 0 V. Therefore, signal conditioning stages that scale and level shift the original signals are necessary. It was discovered that the error introduced from resistance of cabling, tolerance values of scaling resistive networks, and inaccuracy of the sensing network were significant enough to affect the performance of the control network and thus the inverter.

Measurement error being constantly fed back to the control network was introducing steady state error on the output waveform. All else equal, the mismatch remains constant and can be accounted for using a simple compensation. This was accomplished in 2 main steps.

First, the ideal calculations for designing the AC voltage sensor design were used in testing code. This assumes that all DC regulators, passive components, etc. are perfect. In actuality, these values could vary on the order of $\pm$10% which could drastically affect the measurement. In order eliminate this unknown variance, several different DC voltages were applied to the input of the sensor, the output was measured, and the results averaged. In this way a transfer function of the voltage sensor was obtained. Table 5.3.1 shows the results of the test.

Table 5.3.1: Sensing Board Experimental Model

Vin_sense (V)	Vo_sense (V)	K	K_avg
0.006	1.499		
1.006	1.309	0.19	
2.007	1.119		
3.007	0.929	0.19	0.19
4.008	0.738		
5.008	0.548	0.19	
6.009	0.357		
7.008	0.167	0.19	

Fig. 5.3.4 shows the basic schematic of the AC voltage sensor. It is designed to scale and level shift the measurements such that at the zero crossing, V_{DSP} is 1.5 V (the mid-point of the DSP supply), at the positive peak V_{DSP} is 3 V, etc. Employing the logic above, Fig. 5.3.4 reduces to Fig. 5.3.5.

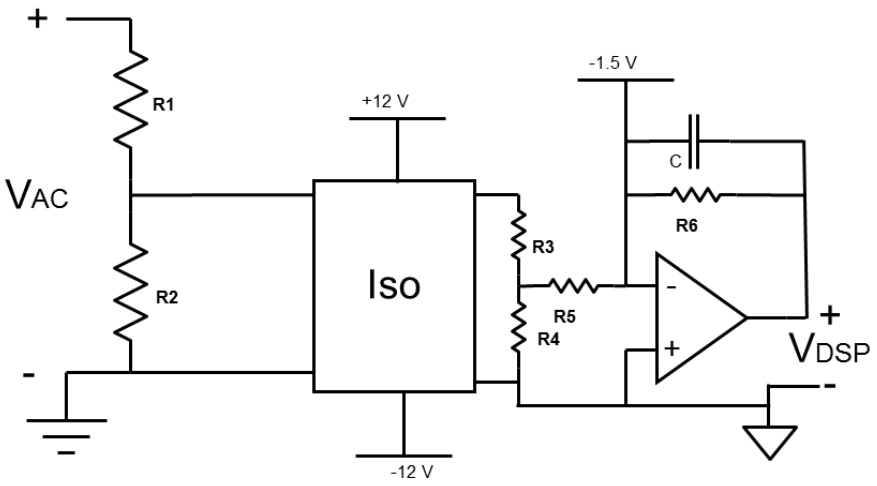

Fig. 5.3.4: Measurement Board Experimental Model Schematic

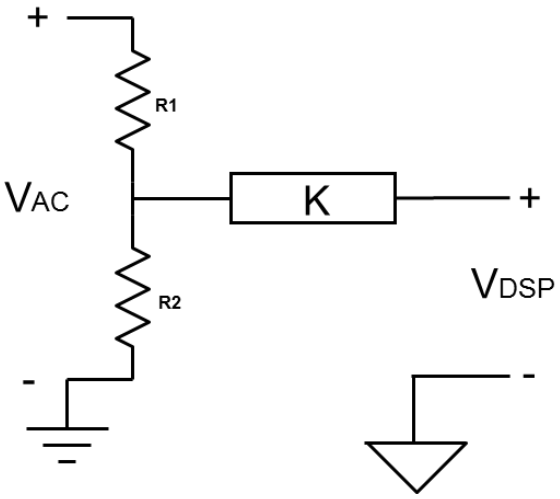

Fig. 5.3.5: Measurement Board Simplified Schematic

Then, the transfer function can be used to "back calculate" the actual measured voltage in the DSP for control by eq. $V_{AC} = \left(\frac{V_{DSP}}{K} - V_O max\right) * \left(\frac{R_1+R_2}{R_2}\right)$ (5-4), where V_0max is the maximum voltage that can be input to the voltage sensor before the isolation amplifiers saturate, and R_1 and R_2 are a scaling resistive divider.

$$V_{AC} = \left(\frac{V_{DSP}}{K} - V_O max\right) * \left(\frac{R_1+R_2}{R_2}\right) \quad (5\text{-}4)$$

Second, assuming there is not a significant amount of noise induced in the measured voltages and currents, the impedance of the measurement cable can be assumed constant. Therefore the voltage drop along that cable is constant. A test was conducted in which the calculated DSP inverter output voltage was compared with the actual output voltage of the inverter (on an O-scope) in order to determine the remaining net measurement error. Then, a constant compensation was added in code to account for the mismatch. These two combined steps significantly reduced the induced measurement error thus improving the performance and accuracy of the inverter control.

5.4 Full Inverter (Island Model)

The waveforms for the closed loop full inverter are shown below in Fig. 5.4.1. This test was conducted by applying a DC voltage on the low voltage DC bus (input to full bridge DC-DC) with a resistive load on the output of the inverter. "V_{hv_dc}" in purple shows the HV bus voltage, "V_{RL}" in yellow shows the inverter output voltage, and "V_{lv_dc}" in light blue shows the LV bus voltage.

Immediately it can be seen that there is significant ripple on both the LV and HV DC bus. This stage of integration was when the bus capacitance sizing concern was discovered. The low frequency ripple caused by the inverter load on the full-bridge had simply not been observed to this point. As can be seen the ripple on the HV DC bus is ≈35 V which is about 9.5% of the DC mean value. Section 3.4.3 discusses the design and solution.

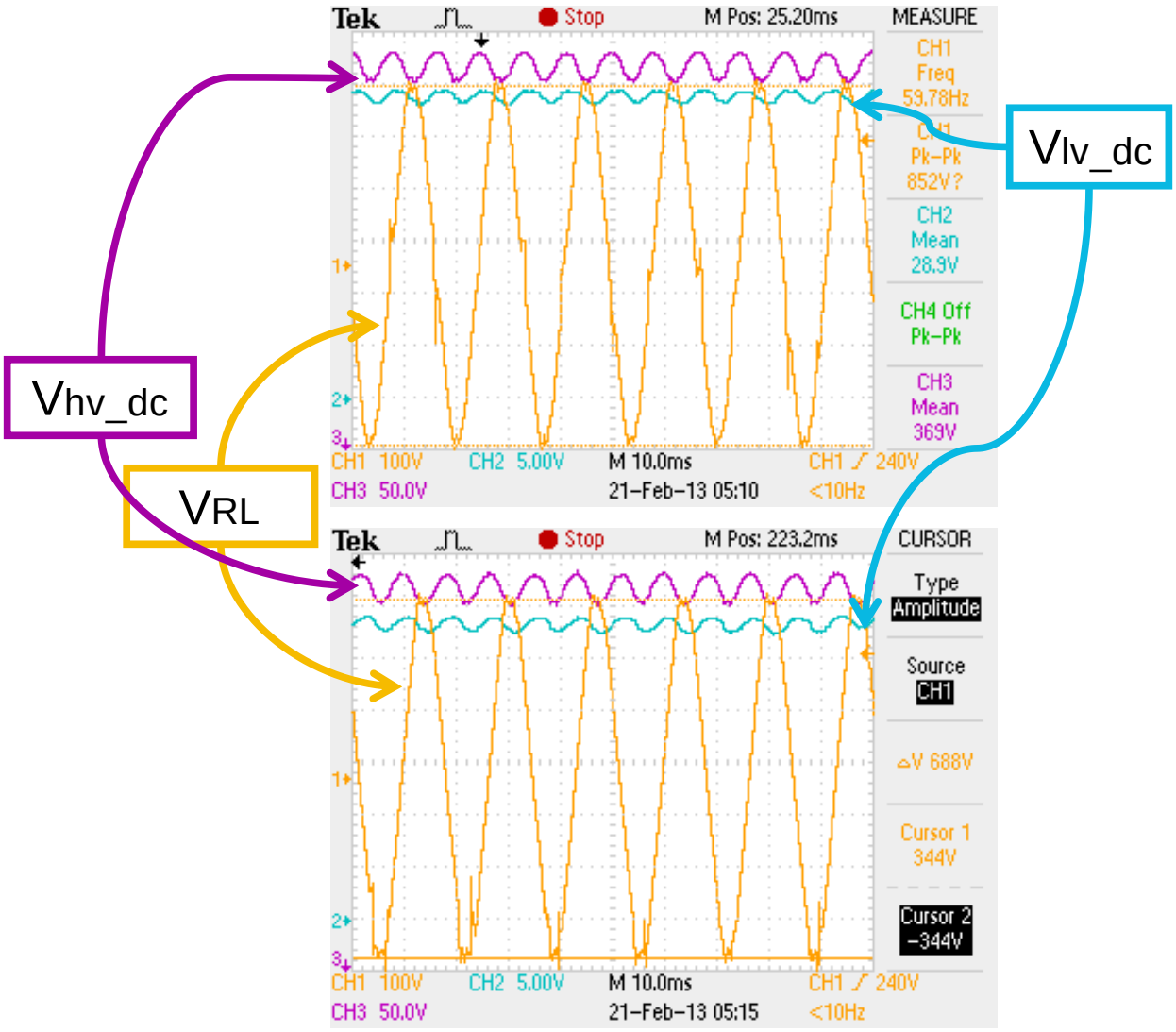

Fig. 5.4.1. Closed Loop Full Inverter Experimental Waveforms (a)-top, (b)-bottom

Fig. 5.4.1(a) shows the O-scope measured values detailing the DC average voltages and the frequency of the output sine wave voltage. The residential 240 V_{RMS} service voltage has a pk-pk value of ≈ 679 V. It can be seen in Fig. 5.4.1(a) it appears the pk-pk voltage is 852 V. This is due to a harmonic spike measured by the O-scope. Fig. 5.4.1(b) shows the full inverter closed loop operation with amplitude cursors on the inverter voltage. It can be seen the amplitude of the fundamental frequency is 688 V which corresponds to an error of 1.3% (eq. $\% \, error = \left|\frac{679\,V - 688\,V}{679\,V}\right| * 100\% = 1.3\,\%$ (5-5).

$$\% \, error = \left| \frac{679\,V - 688\,V}{679\,V} \right| * 100\% = 1.3\,\% \tag{5-5}$$

5.5 PV Boost Converter with Full Bridge DC-DC Converter

This section discusses the integration of the PV boost converter and full bridge DC-DC converter. This experiment was conducted after the appropriately sized DC link capacitor was designed. Increased bulk capacitance in the system has tradeoffs; while it reduces DC ripple voltage it also slows the natural response of the system as well as increases the inrush current required from the input.

5.5.1 *PV Boost and Full Bridge Integrated Results and Discussion*

A startup procedure was developed for this stage of integration given the concern of inrush currents that would be experienced from "hard-starting" the system. The test procedure given below was automated through software to emulate a startup sequence for the SGPN in real operation. This will be expanded for full system operation detailed in sections 5.6.3 and 5.6.4.

The startup procedure is as follows:

1. The PV boost converter will remain off until the input voltage is increased to a value of "$V_{in\_BTHRESH}$". Thus, the input voltage will equal the LV DC link voltage (minus diode losses, series resistance of the input inductor, etc).
2. Once a sensed voltage of 5 V is reached on the LV DC bus, the FB converter switches - pre-charging the HV capacitor. This limits the amount of $\frac{dv}{dt}$ that is seen across the system capacitance and thus the inrush current at startup.
3. Once the input voltage threshold has been reached (t_0), the boost converter operates and the system reaches full scale output.

Fig. 5.5.1 shows the startup transient waveforms of the PV boost and FB integrated test. CH1 (yellow) is V_{in_boost}, CH2 (blue) is V_{LV_DC}, CH3 (purple) is V_{HV_DC}, and CH4 (green) is

I_{in_boost}. The soft-start sequence given above was fundamental in protecting the hardware from over-currents that would damage devices. Initially, with the pre-charge stages alone as the startup sequence the inrush current observed was on the order of 40 A which is within ratings of the low side devices, but can be improved.

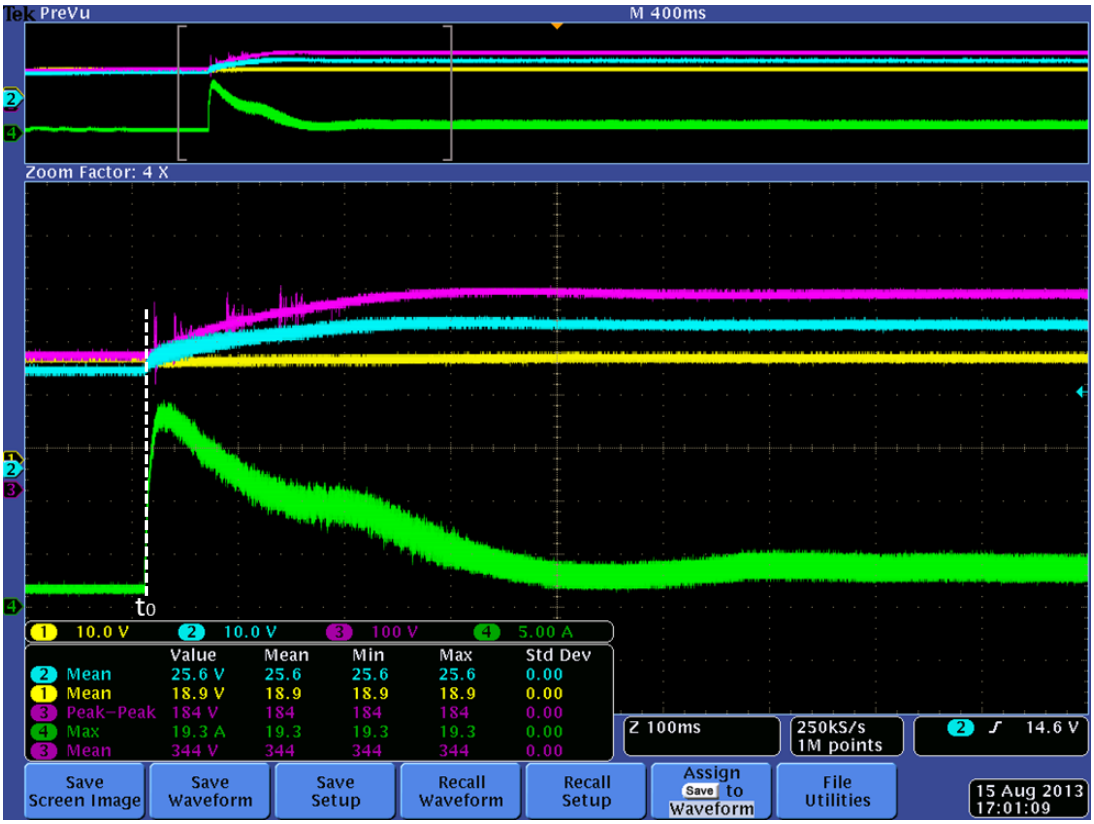

Fig. 5.5.1: Closed Loop PV Boost & FB DC-DC Converter Experimental Waveforms

Instead of the PI control for the boost converter shown in section 3.4.2, a PID controller was implemented. The derivative term in the control loop arrests sharp changes in control target values (i.e. input current) [33]. Thus through control, the inrush current through the boost inductor can be reduced. The introduction of this more complex control reduced the inrush current by about 50% to 19 A from the previously seen 40 A which is much more reasonable.

Fig. 5.5.2 shows the FB waveforms of the PV boost and FB converter integrated test in steady state. CH1 (yellow) is V_{DS_Q1}, CH2 (blue) is V_{XFMR_S}, CH3 (purple) is V_{DS_Q2}, and CH4

(green) is V_{CE_IGBT1}. In order to show sufficient detail, the waveforms only show 100 µs (4 switching cycles). Therefore only the steady state is captured here. The signal integrity gained from the isolation board can clearly be seen through this waveform. Notice there are virtually no over-voltages seen across the high side or low side devices.

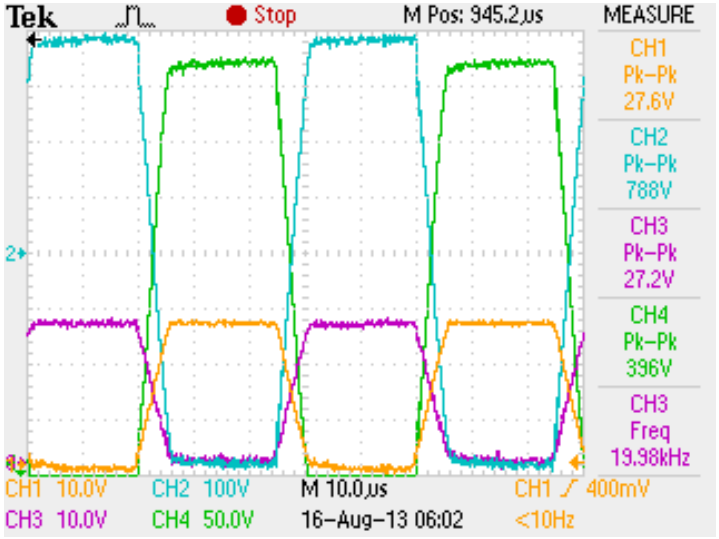

Fig. 5.5.2: Closed Loop PV Boost & FB DC-DC Converter - FB Switching Detail Waveforms

Fig. 5.5.3 shows the steady state waveforms of the PV boost and FB converter integrated test. All signal definitions are the same as Fig. 5.5.1. It can be seen all signals are a stable, low noise DC value. This test was run with the re-designed capacitance value on the HV DC link.

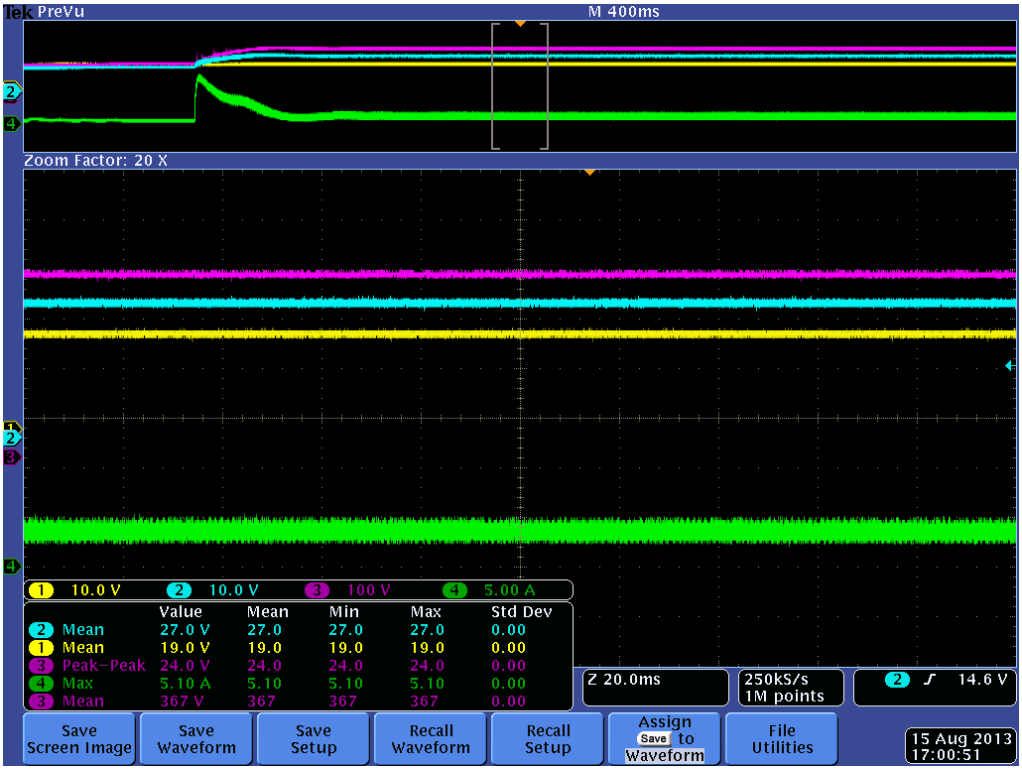

Fig. 5.5.3: Closed Loop PV Boost & FB DC-DC Converter Experimental Waveforms (Steady State)

At this point, it should be noted that each new stage of integration brings unique design and operational problems that must be solved. As will be discussed in section 5.6.3, the integration of the inverter stage caused the PID controller developed here to become unstable. Instead, the controller design of section 3.4.2 was implemented and a more elaborate startup procedure was developed. The PV boost converter ramp function addressed the concerns of inrush current without the increased controller complexity. Each problem encountered and the solutions at each stage of integration are discussed because this is an integral part to illustrating the learning process and documenting the integration of this system.

5.6 Integrated Hardware Test Results

This section shows the first fully integrated closed loop test results of the SGPN hardware in islanded operation. One of the most critical and most difficult aspects of obtaining these

results is system startup. Startup dynamics of each power stage or the system as a whole can cause instability and potentially damage the hardware. This is the reason for the systematic testing of individual converters, the different levels of sub-integration, and finally full system integration. Certain stages of startup were implemented in the sub-integration portion such as the bulk capacitance pre-charge. The following sections will present and discuss full system test results, the integration of low level hardware control modules, and the development of system startup.

5.6.1 *Integration of Low Level Hardware Controls*

It should be noted that each converter performs individual power flow control, paralleled converters have a power sharing control, and the central inverter provides the overall power flow control for the system. [11] presented closed loop results of the DC-DC converter paralleled operation which is an example of hardware control integration as well as the above mentioned power sharing controller. In order to have an "installation ready" prototype, this functionality will need to be implemented along with what has been developed here (more on this in CHAPTER 6).

Since the control integration of the PV boost and battery charge/discharge converter with the full system is identical, the discussion here is applicable to both.

The integration of separate hardware controllers starts with a code structure that allows for information to be passed and acted upon by each block. Intuitively, object oriented programming lends itself to this structure. For example, the PV boost converter controller is a separate function in which its arguments are passed from the main program (e.g. measured voltages and currents, PWM output signal, etc.). Similarly, the battery charge/discharge converter control is its own function. The power sharing network is its own function, and so on.

It is important to lay this framework for future full integration with the system level controller. The system level control requires basic information from low level controllers such as power flow ("V's" and "I's"), load demand, status of on-site resources, etc. to perform its critical functions. Being able to pass this data between control layers and individual control modules is therefore critical.

In addition to control integration, certain software fault condition protections were coded in order to protect the system hardware in the case of unexpected operation or component failure. These include OV and OC protection on the LV DC bus, OV and OC protection on the HV DC bus, and UVLO on the PV input. For example, if there was a control instability causing the LV DC link voltage to increase without bound, the SGPN will shut down that stage (or potentially the whole system depending on configuration). As another example, picture the batteries serving home load on a cloudy day and they approach a deeply discharged level (a pre-determined low threshold); the SGPN will discontinue discharging the batteries by either disconnecting the battery converter, or charging them from the grid. Similar "check" conditions were integrated into the code using the various sensed voltages and currents throughout the SGPN.

This is done for several reasons, but primarily to protect hardware/resources and more importantly safety (prevent back-feeding the system if connected to the electric grid) for anyone that might be troubleshooting a problem. It would be tedious to list every conceivable example, but for the purposes of this prototype, hardware protection is the focus. In a commercial development there would be a focus on owner/operator safety as well as protecting the hardware.

5.6.2 *System Startup Sequence*

As mentioned, startup sequencing is paramount for reliability and stable operation. Through testing and integration there were certain system behaviors, required design changes,

and lessons learned about the SGPN system topology that influenced and helped shape the startup sequence.

The control integration and operation of integrated power stages were fundamental in developing system startup as well as debugging and refining the code. Since each power stage is cascaded the startup sequence follows this natural flow from input to output.

The startup sequence for SGPN when the PV boost converter is supplying home load in island mode is detailed in the below steps. A basic flowchart showing the startup sequence is show in Fig. 5.6.1.

1. Apply 12 V DC input to DC regulator circuitry, gate drivers, IGBT modules, voltage sensor board, current sensors, and disconnect switches.
2. Apply 5 V DC input to control board (isolation board is powered from control board power supply). This stage starts the sensing and automated software start sequence housed inside the DSP control platform.
3. From section 5.2.2 the DSP constantly polls the input voltage to the system which is sensed through the SGPN voltage sensor. As long as the input voltage is below the threshold "$V_{inbthresh}$" the PV boost converter remains idle and all other power stages are off. Therefore, the input voltage to the system $V_{in} \approx V_{LVDC}$.
4. Once V_{LVDC} reaches threshold "$V_{LVThresh}$" (around 5 V) the FB converter switches boosting the LV DC link to a higher voltage on the HV DC link with the PV boost and inverter still off. This is known as the bulk capacitance pre-charge stage.
5. Once "$V_{inbthresh}$" is reached the PV boost converter operates under closed loop control boosting to the final LV DC link voltage. Since the FB converter is already switching the full scale DC output is reached. It should be noted, that the

PV boost converter is extremely unstable and difficult to control with no load at the output. Therefore, a pre-insertion resistor was added across the HV bus as a load for the boost converter during startup.

- A ramp function was implemented on the boost converter in order to again, limit the $\frac{dv}{dt}$ across bulk capacitance in the system to control the inrush current during final stages of startup.

6. The final startup sequence is the inverter. A delay function of about 3 s was implemented after the boost converter was started to allow sufficient time for the system to reach steady state conditions before starting the inverter. In reality, this time could be reduced to the "ms" timeframe. It was determined through testing the inverter was unstable when hard started. Therefore a ramp function of the output reference voltage was implemented to allow a smooth inverter startup.

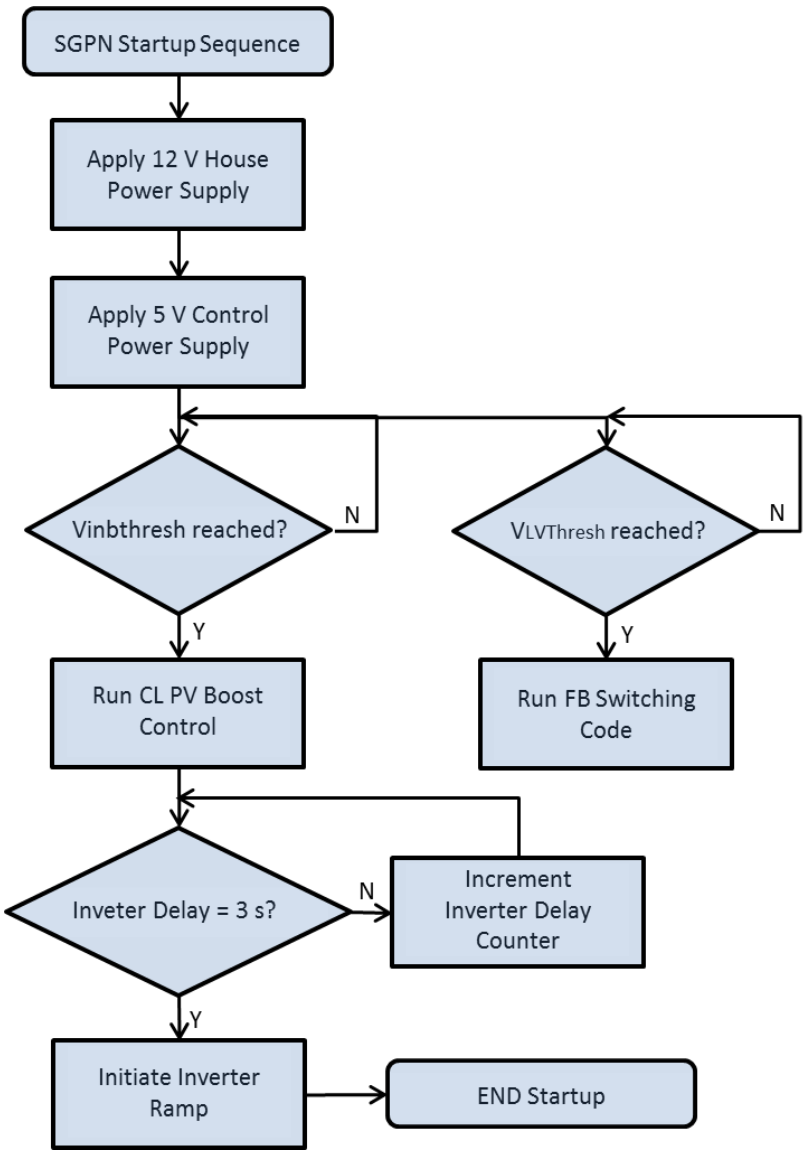

Fig. 5.6.1: SGPN Startup Sequence Example Flowchart

It should be noted this startup sequence was for a specific application – the PV boost serving home load in island mode operation. There are multiple possibilities for a startup sequence depending on the available inputs, loading, and system configuration. For example, the battery bank will maintain a relatively constant DC voltage. Therefore, a different pre-charging stage might be necessary to limit inrush current. A ramp function of the full bridge converter could be implemented since the "$V_{LVThresh}$" can never be below 12 V (assuming a single car

battery for simplicity). The condition for starting the battery converter, then, would no longer be dependent on the input voltage to the system since it is fixed. The battery boost converter ramp function would be triggered based on the FB converter voltage.

A grid-connected system would have its own set of unique startup considerations. First, to avoid damaging currents, the SGPN inverter must sense and synchronize with the utility grid voltage before connecting. In that case, (assuming the PV boost converter only as the input for simplicity) the startup sequence would look very similar to Fig. 5.6.1, except the inverter would synchronize with the grid voltage before the disconnect switch would be commanded to close.

There are many different examples that can be conceived that would require a unique solution such as a mode transition between grid-connected to island, or vice versa. There is more discussion on startup sequencing in CHAPTER 6 .

5.6.3 *PV Boost Converter with Full Inverter (Island Model)*

The schematic for this test is shown below in Fig. 5.6.2: PV Boost Converter with Full Inverter Schematic - Islanded Mode.

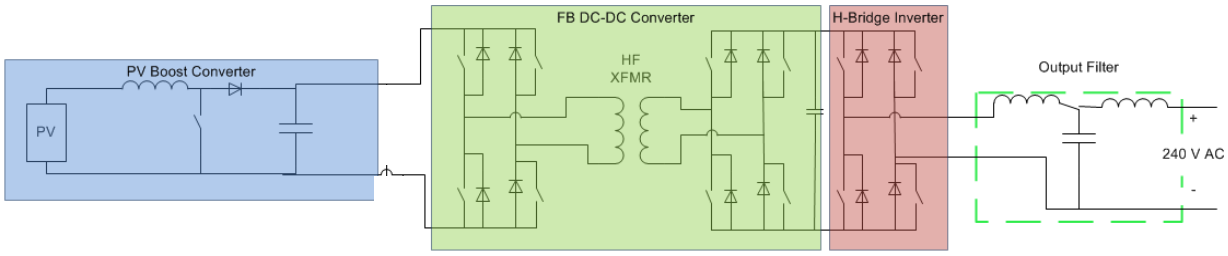

Fig. 5.6.2: PV Boost Converter with Full Inverter Schematic - Islanded Mode

Fig. 5.6.3 shows startup DC waveforms for the first fully integrated closed loop test of the SGPN hardware. CH1 (dark blue) = V_{in_bst}, CH2 (light blue) = V_{LVDC}, CH3 (purple) = V_{HVDC}, and CH4 (green) = I_{in_bst}. In order to capture enough detail, only startup sequence steps 4-6 listed

in section 5.6.2 could be shown in a single capture. The test conducted consists of an independent DC supply connected to the PV boost converter (to emulate the solar panel output), the FB DC-DC converter, and the central inverter with a 405 Ω resistor connected at the output emulating some home load. In steady state operation, the input voltage to the system is ≈ 30 V DC, the HV DC voltage is about 380 V mean, and the output is a split-phase 240 V_{rms} 60 Hz AC voltage in order to be compatible with a typical US residential service.

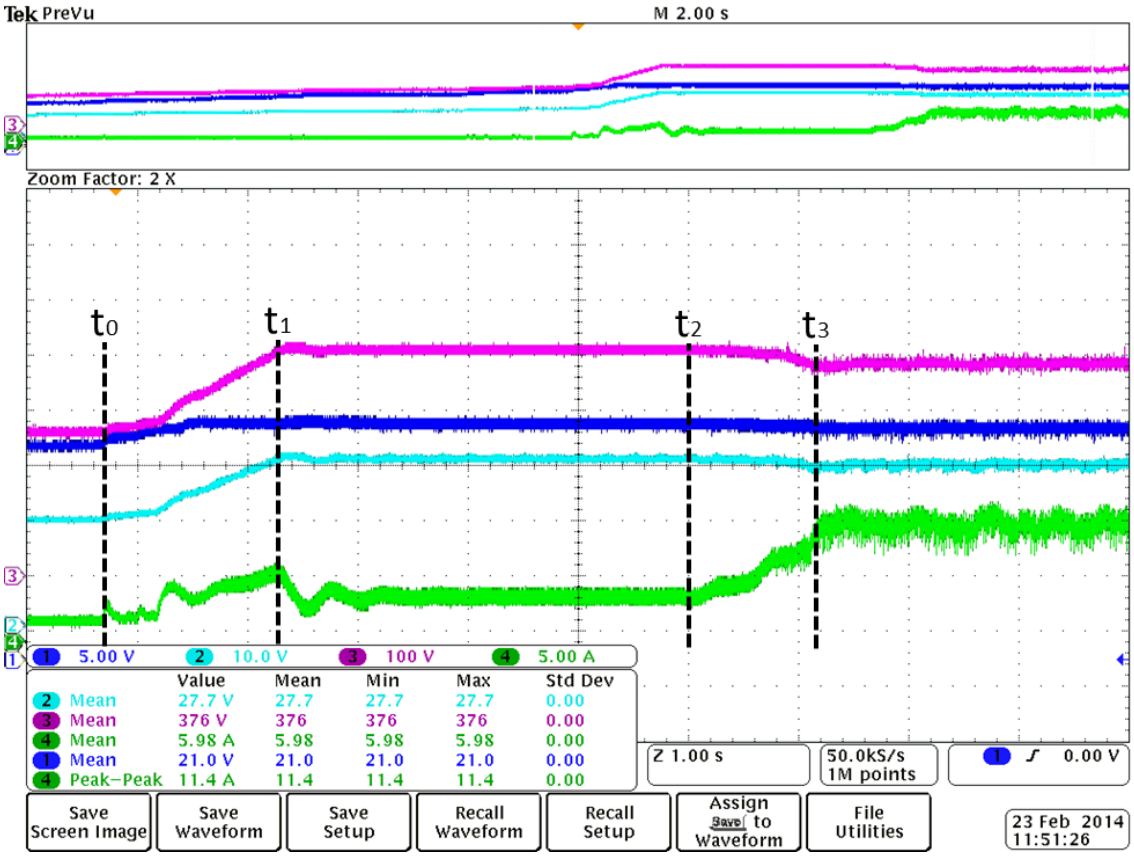

Fig. 5.6.3: Closed Loop PV Boost with Full Inverter - Islanded - Startup DC Waveforms

Prior to t_0 startup stages 1-3 are taking place – all regulating and supporting circuitry has been powered on and the FB converter is switching, boosting the input/LV link from around 20 V to 275 V DC. At t_0, "$V_{inbthresh}$" is met triggering the boost converter to switch. Between $t_0 \leq t \leq t_1$ the boost converter ramp function is implemented. It can be seen that the inrush current

experienced in section 5.2.2 is reduced from ≈19 A to ≈7 A, a 63 % reduction. Thus, the addition of the ramp function gives much more desirable performance. After t_0 the DC system of the SGPN is full scale. Between $t_1 \leq t \leq t_2$ is the time delay function ensuring DC steady state operation before the start of the inverter (note: this could likely be reduced). Between $t_2 \leq t \leq t_3$ the inverter ramp function is initiated. Beyond t_3 is the output of the island mode SGPN fully integrated system in steady state.

Now that the system startup sequence has been demonstrated experimentally, steady state DC waveforms in Fig. 5.6.4 are shown. It can be seen that the input current waveform has some low frequency noise induced as noted in CHAPTER 4 . It is speculated the controller is exhibiting some marginal stability issues at these reduced power levels, thus the imperfect current waveforms. It should be noted that in a commercial deployment, elimination of this noise would be important to reduce unnecessary losses and heating in the boost converter inductor (more on this in CHAPTER 6). Contrary to results presented in section 5.4 , the re-designed larger capacitor on the HV DC link suppresses almost the entire 120 Hz voltage ripple induced by the operation of the inverter.

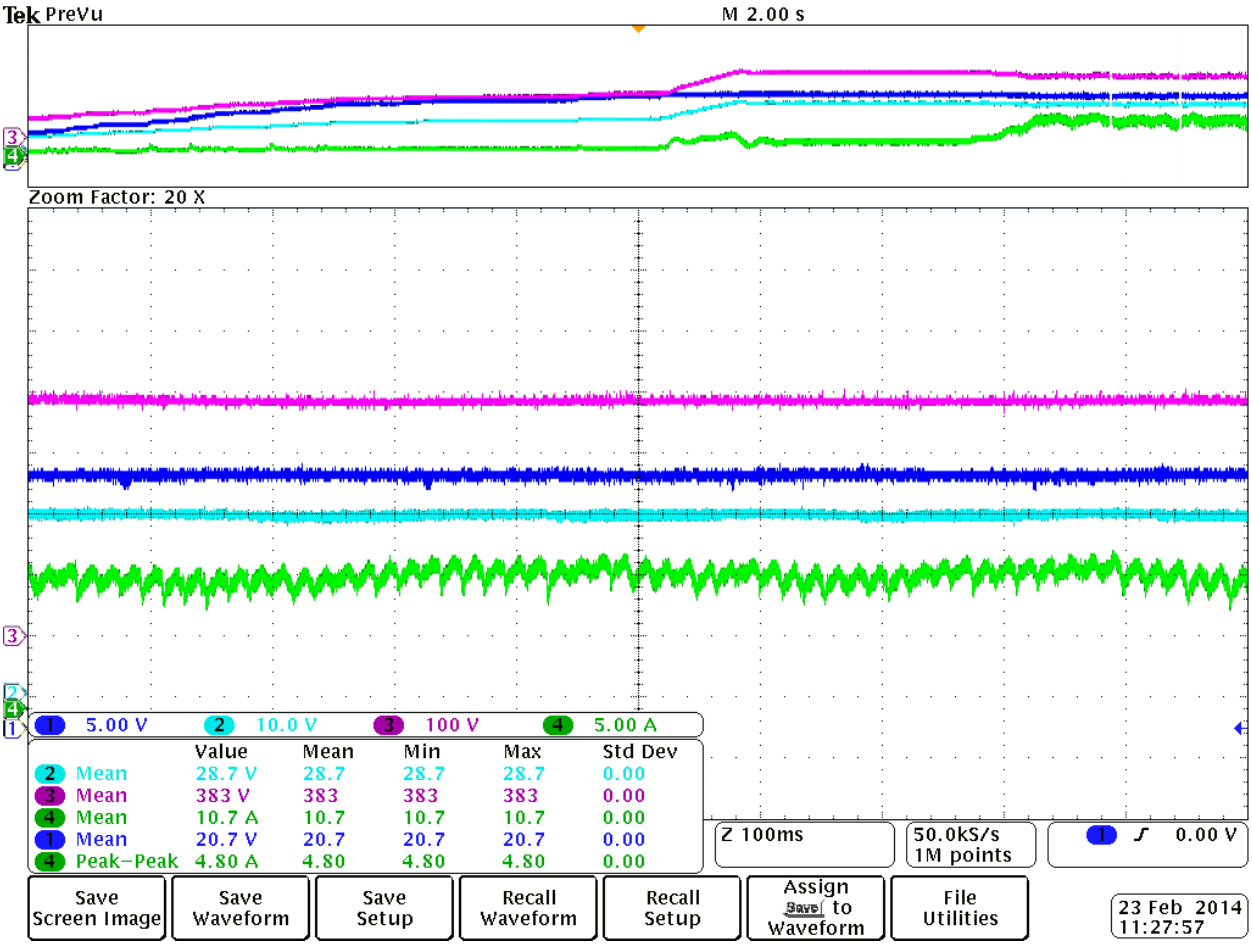

Fig. 5.6.4: Closed Loop PV Boost with Full Inverter - Islanded - Steaady State DC Waveforms

Fig. 5.6.5 shows the AC waveforms for the same test above, where CH1 (yellow) = V_{AC_out} and CH4 (green) = I_{AC_out}. Immediately it can be seen that there is a large amount of high frequency noise on the AC current waveform. As discussed in [11], the poor current filtering at low power levels was a known issue. Part of the suggested work is to re-design or look for ways to improve current filtering.

After investigation of EMI related problems, it is expected that propagated noise in the fully integrated circuit is compounding the poor harmonic performance at the output. During the standalone inverter test in section 5.3 the current waveforms produces a much lower THD, thus indicating this is a valid assumption. In order to comply with the standards set forth in IEEE

1547, PC board layouts must be improved to reduce undesirable noise or the LCL filter must be re-designed to achieve better performance. Due to time constraints, this issue was not solved and still needs to be addressed which will be discussed further in CHAPTER 6 .

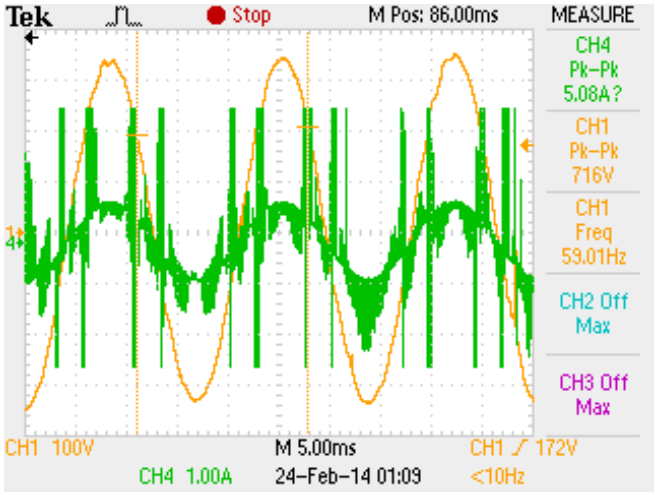

Fig. 5.6.5: Closed Loop PV Boost with Full Inverter - Islanded - AC Waveforms

Fig. 5.6.6 shows the inverter AC output voltage without the current waveform for clarity. The voltage waveform is approximately 676 $V_{pk\text{-}pk}$ @ 60 Hz. This yields a V_{rms} = 239.002 V which is an error of 0.42 % from the reference voltage of 240 V_{rms} set for the inverter controls. Unfortunately, the resolution of the Tektronix 2024 is not fine enough to get a good frequency reading at this scale. However, it can be seen the waveform frequency is essentially at 60 Hz.

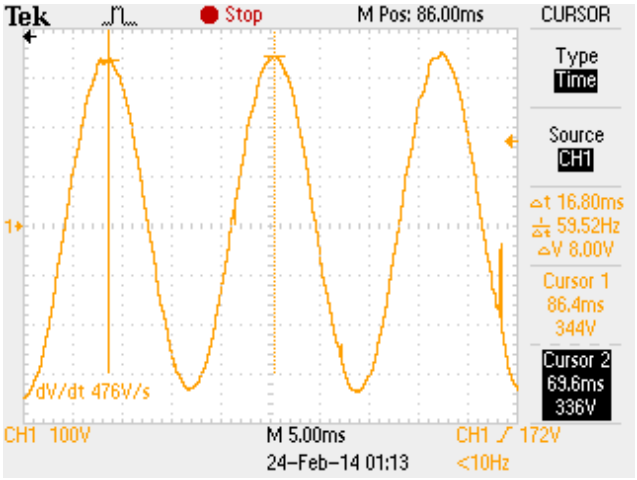

Fig. 5.6.6: Closed Loop PV Boost with Full Inverter - Islanded - AC Waveforms with Data Cursors

After investigation and witness to the sensitivity of the power electronics to EMI, the experimental test setup was "cleaned up" reducing the length of measurement wires and adding ferrite cores to signal leads. One benefit was reduced exposure to measurement noise which results in a much cleaner output voltage waveform. In addition, as was demonstrated in section 5.1 the isolation barrier also improves the signal integrity. This is clearly illustrated by comparison of inverter test results in this thesis (section 5.3 and 5.4).

The noise induced on the AC current waveform is still compounded by interference which could be improved with additional filtering or increasing the load on the system. However, there are tradeoffs with additional filter inductors such as cost, size and losses. Optimizing the power layout would help with the noise contribution in addition to harmonic injection reduction techniques. This is discussed in CHAPTER 6 .

5.6.3.1 Discussion on Efficiency

It is well known that IGBTs can be undesirable in high switching frequency applications due to their high tail current at turn off resulting in very high switching losses [41]. In [11], it was presented the efficiency of the FB converter itself was around 43 %, which would make the

efficiency of the overall system very low. However, this was at an output power close to 20 W. At this extremely low power, the switching and conduction losses of the IGBTs and MOSFETS make up a much larger percentage of total power – hence the low efficiency.

Even though full system testing was still at low power, it was determined that the analysis on efficiency of the SGPN based on the FB converter was overly conservative. As mentioned, there was a resistor placed across the HV DC terminals for startup considerations. Therefore this needs to be taken into consideration for efficiency calculations. For the quoted efficiency of the inverter at 91%, a resistor value of 2500 Ω, and a DC voltage of 383 V, the equivalent AC power drawn taking into account losses of the inverter is $P_{RDC-AC} = Eff.* \frac{{V_{DC}}^2}{R} = 0.91 * \frac{383\ V^2}{2500\ \Omega} = 53.4\ W$. For the test in section 5.6.3, $P_{in} = 20.7\ V * 10.7\ A = 221.5\ W$ and $P_{out} = P_{RDC-AC} + P_{AC} = 53.4\ W + \left(\frac{676\ V_{pk-pk}}{2\sqrt{2}} * \frac{1.54\ A_{pk-pk}}{2\sqrt{2}}\right) = 183.53\ W$. Therefore the efficiency of the full system is $Eff.= \frac{P_{out}}{P_{in}} * 100\% = \frac{183.53\ W}{221.5\ W} * 100\% = 82.8\ \%$.

From the above analysis and Fig. 5.6.7, it can be seen that the tested efficiency is relatively close to the simulated efficiency of 89.82 %, an error of about 7 %. As the power drawn increases, the switching losses become an increasingly smaller portion of total power. However, the conduction losses increase. The losses of 17.2% are with a system switching 13 switches. This could be improved through ZVS or ZCS switching, or a reduction in the overall number of switches.

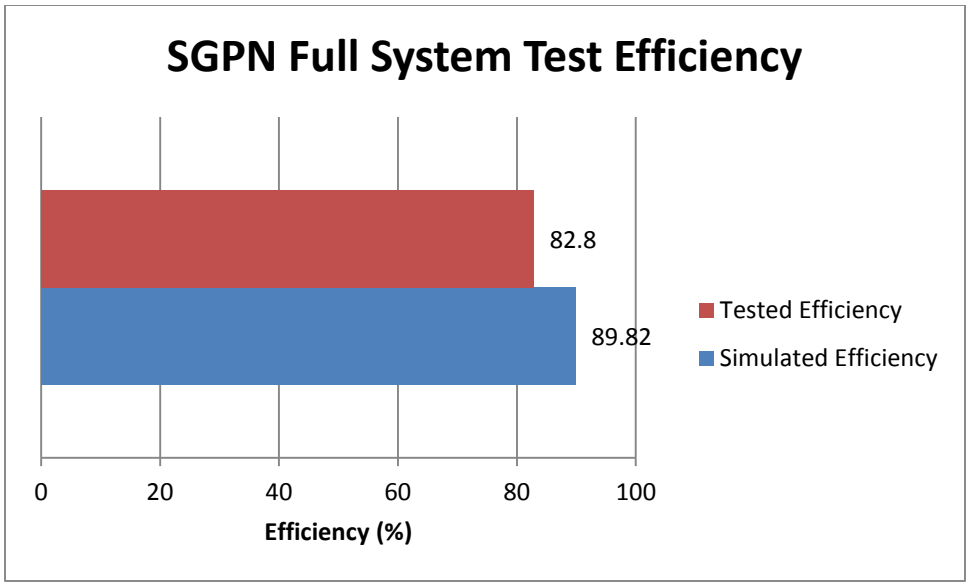

Fig. 5.6.7. Simulated vs. Tested Efficiencies

5.6.4 *Battery Charge/Discharge Converter with Full Inverter*

The schematic for this test is shown below in Fig. 5.6.8.

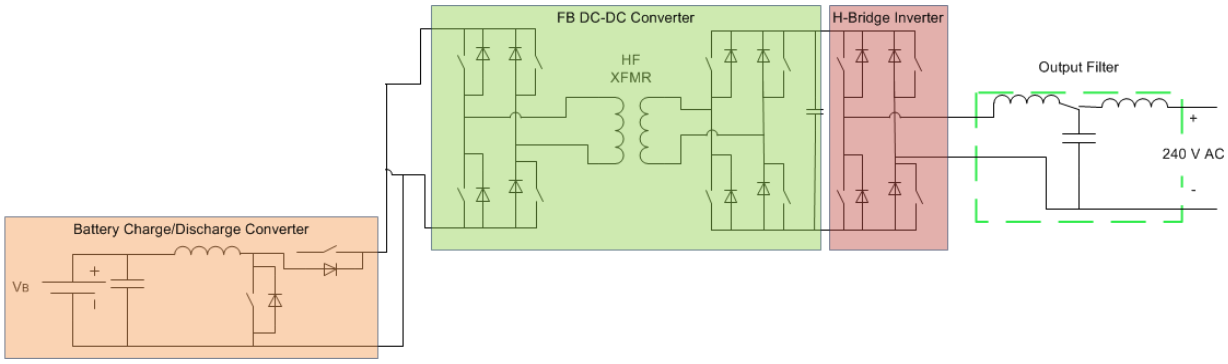

Fig. 5.6.8: Battery Charge/Discharge Converter Schematic - Islanded Operation

Since the battery charge/discharge converter in discharge mode is the same in operation to the PV boost converter, the test results obtained for the full system are likewise very similar. The test setup is a transplant from section 5.6.3 with the battery charge/discharge converter as the input DC-DC converter. A DC supply is used to emulate the battery input with the FB DC-DC converter and inverter cascaded to the output with the same resistive load of 405 Ω connected to the AC output. Fig. 5.6.9 shows the startup DC waveforms associated with this test

where CH1 (dark blue) = V_{in_batt}, CH2 (light blue) = V_{LV_DC}, CH3 (purple) = V_{HV_DC}, and CH4 (green) = I_{in_batt}.

Prior to t_0 the startup sequence involving powering supporting regulator circuitry, starting the control code, and initial circuit pre-charge was initiated. At t_0 the "$V_{inbbthresh}$" condition was satisfied and with the FB already switching, the battery converter ramp function is implemented from $t_0 \leq t \leq t_1$. At t_1 the DC system reaches full scale output. Between $t_1 \leq t \leq t_2$ the time delay function to ensure steady state operation is implemented before inverter startup. Between $t_2 \leq t \leq t_3$ the inverter ramp function is implemented where after t_3 the full system is in steady state operation. It can be seen that there is some small variation in startup behavior from section 5.6.3 which is expected due to different parasitic loops in the board layout and different converter dynamics, but the startup procedure is identical to the PV boost converter.

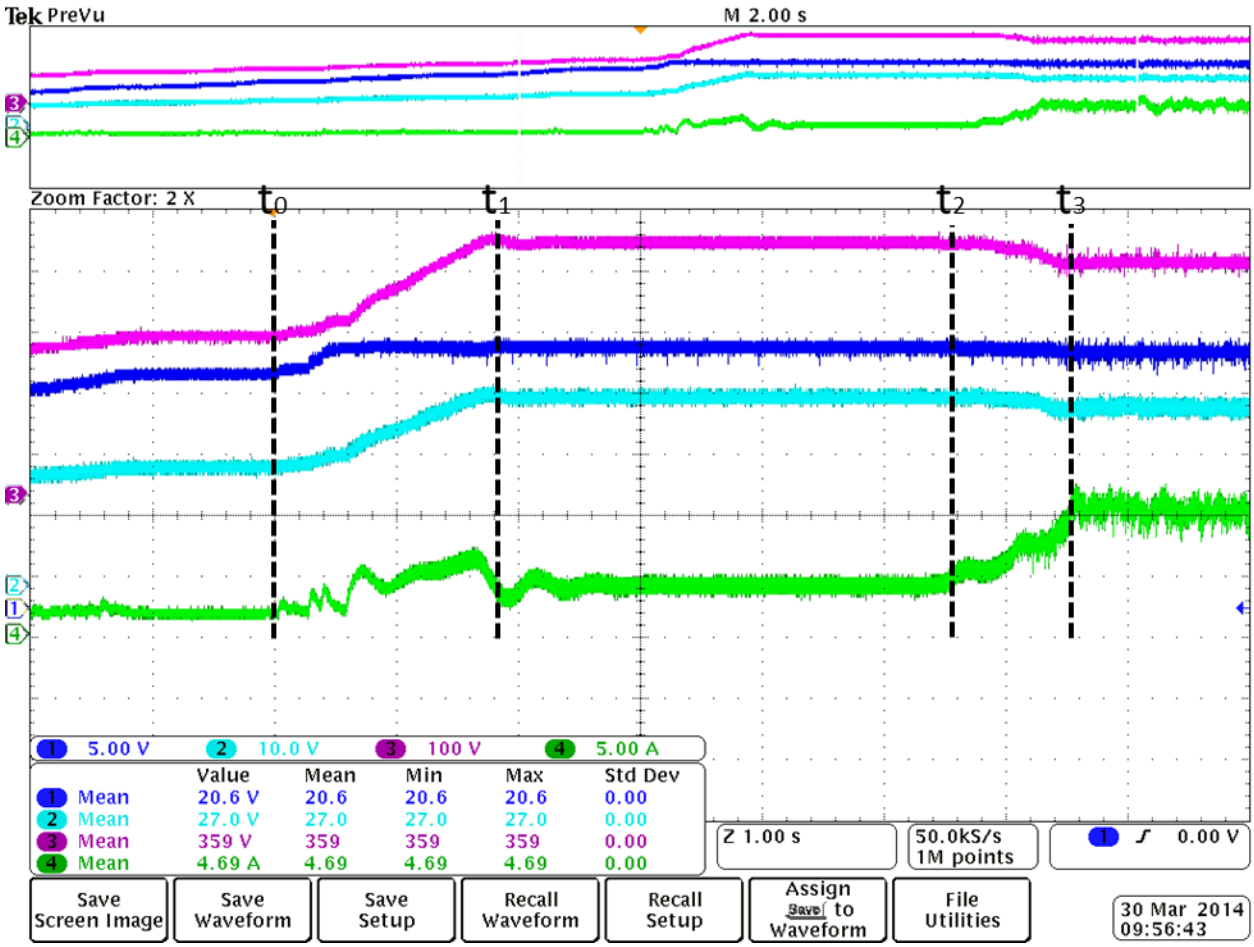

Fig. 5.6.9: Closed Loop Battery Charge/Discharge Converter with Full Inverter - Islanded - Startup DC Waveforms

The steady state operation of the closed loop battery converter with full inverter is shown below in Fig. 5.6.10 for the same test as in Fig. 5.6.9. The 120 Hz induced ripple voltage on the HV and LV DC link voltages can be seen to be almost negligible. There are some harmonic spikes that are recorded, but do not significantly affect the quality of output from the SGPN system. The “ripple” analysis of the DC system is shown in Table 5.6.1.

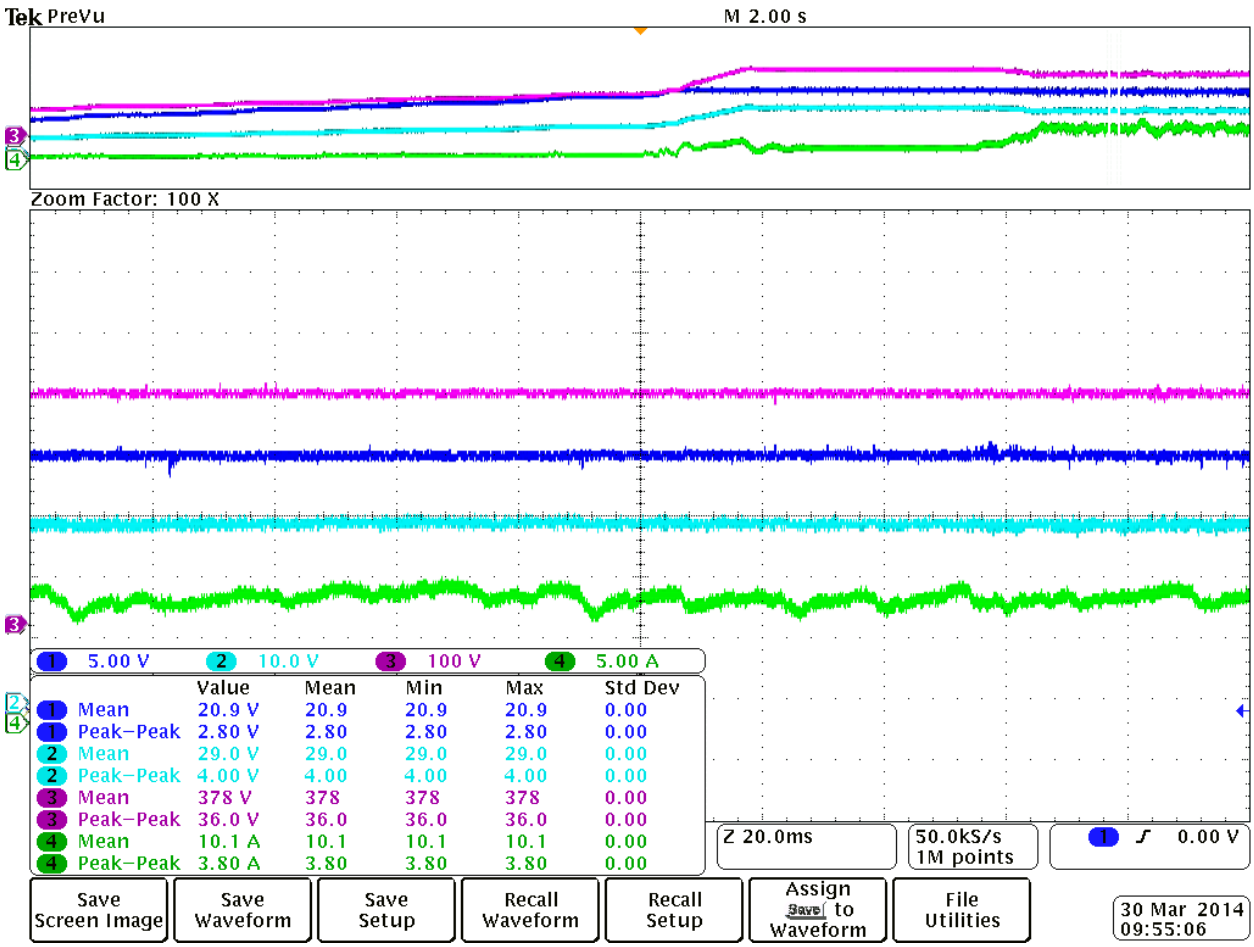

Fig. 5.6.10: Closed Loop Battery Charge/Discharge Converter with Full Inverter - Islanded - Steady State DC Waveforms

The performance of the LV DC link and input voltage deviated from the maximum allowable ripple specification by 3.6% and 3.04%, respectively. The HV DC link performance was within allowable specifications. The deviation can be explained for both by the relatively small ripple voltage it takes to constitute 10 % of the mean value, but a difference of 3-4% is very close to specifications. A re-design of the power board layout to reduce parasitic inductance will help alleviate noise in the system. Additionally, a soft switching scheme will help reduce conducted high frequency noise, and also help improve the signal to noise ratio.

Table 5.6.1: Closed Loop Battery Charge/Discharge Converter with Full Inverter - Islanded - DC System Performance

Battery Converter + Full Inverter (Island): DC-DC Performance					
		Measured Result		**Max Spec.**	
		Voltage	% rated	Voltage	% rated
Ripple Voltage	LV DC link	4.0V	13.6%	2.9 V	10%
	HV DC link	36 V	9.5%	37.8 V	10%
	Input DC link	2.8	13.04%	2.1 V	10%

The steady state AC waveforms for the same test above are shown in Fig. 5.6.11, where CH1 (yellow) is V_{AC} and CH4 (green) is I_{AC}. Similar to section 5.6.3 the current waveform has a large amount of THD and is unacceptable according to IEEE 1547 (see CHAPTER 6). The inverter output voltage however has a very small THD with amplitude of 676 V. Eq. $\%Error_{frequency} = \frac{60\ Hz - 59.52\ Hz}{60\ Hz} * 100\% = 0.8\%$ (5-7 shows the error calculation.

$$\%Error = \frac{(240\ V_{RMS} - 239\ V_{RMS})}{240\ V_{RMS}} * 100\% = 0.42\% \quad (5\text{-}6)$$

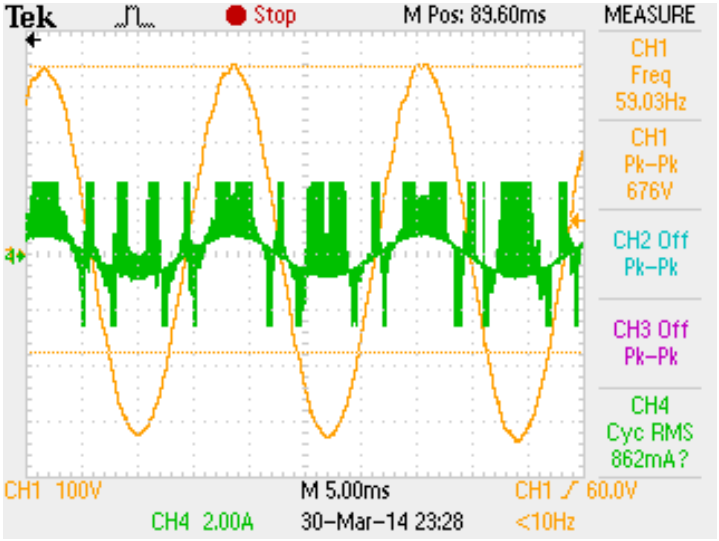

Fig. 5.6.11: Closed Loop Battery Charge/Discharge Converter with Full Inverter - Islanded - AC Waveforms

The frequency cursors were utilized to show the true output voltage frequency of the system. This is shown in Fig. 5.6.12. As previously mentioned the O-scope resolution is not fine enough to get an exact measurement. At the 5 ms scale the jump is on the order of 0.5 Hz. The cursors measure a frequency of 59.52 Hz with a reference frequency of 60 Hz. The error is calculated below.

$$\%Error_{frequency} = \frac{60\ Hz - 59.52\ Hz}{60\ Hz} * 100\% = 0.8\% \quad (5\text{-}7)$$

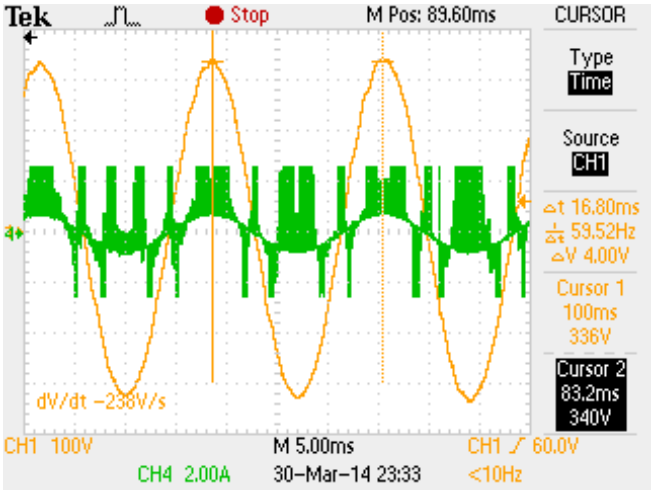

Fig. 5.6.12: Closed Loop Battery Charge/Discharge Converter with Full Inverter - Islanded - AC Waveforms with Data Cursors

Similar to the PV boost converter full system test, the battery converter in discharge mode requires a pre-insertion resistor for stable startup as well. Therefore this power must be factored into efficiency calculations. Using a HV DC voltage of 378 V, a R_{DC} = 2500 Ω, and a quoted inverter efficiency of 91%:

$$P_{DC-AC} = 0.91 * \frac{378\ V^2}{2500\ \Omega} = 52\ W \quad (5\text{-}8)$$

$$P_{out} = P_{RDC-AC} + P_{AC} = 52\ W + \left(\frac{676\ V_{pk-pk}}{2\sqrt{2}} * \frac{1.4\ A_{pk-pk}}{2\sqrt{2}}\right) = 170.3\ W \quad (5\text{-}9)$$

$$P_{in} = 20.9\ V * 10.1\ A = 211.09\ W \quad (5\text{-}10)$$

$$Eff. = \frac{186.35\ W}{211.09\ W} * 100\% = 80.7\% \quad (5\text{-}11)$$

Compared with the analysis for the PV boost converter, the battery charge/discharge converter has slightly higher losses. Since the number of switches is the same as the full system test with the PV boost converter (13) this can be explained due to the higher losses in the anti-parallel diode of the battery converter's MOSFET used as the diode in the converter topology (in discharge mode). In addition there could be some additional losses due to board layouts and the ESR of the battery converter's input capacitor. Under similar loadings of 200W the tested efficiency above compares to the simulated efficiency of 88.7%, an error of 8.0%. This difference is somewhat large, but could be explained due to the additional harmonics (which increase losses) experienced with the tested prototype.

CHAPTER 6

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

This chapter will present the conclusions obtained from integration of the SGPN hardware and control. It will also present the issues and challenges encountered through testing as well as the additional work that must be completed for the fully integrated system verification. Recommendations for future work based on lessons learned are presented to expand the functionality of the SGPN and improve upon the design for a more robust system.

6.1 SGPN Hardware Integration Summary

This thesis has presented the integration of the hardware and hardware control for a next generation smart energy management system that offers alternatives to grid energy and has the potential to yield economic benefit for the home owner and the utility. CHAPTER 1 introduced the interest in energy management systems and alternative energy sources citing rising electricity costs, decreasing cost of power electronics, increasing automation and control capabilities with advanced microcontrollers, and penetration of distributed generation resources into the market.

It gave an overview of some commercial products that integrate renewable and on-site generation resources through power electronic systems in conjunction with the electric grid to power the home. However, these systems did not explore the level of data acquisition, high level intelligence, flexibility, and automation that the SGPN is specifically designed to address which is the novelty of this system.

CHAPTER 2 presented the relevant technical background needed to understand and recreate the work established in this thesis. This chapter is supplemental to the background contained in [11], [9], and [10] which includes much of the previous and collaborative work that makes up the full project.

CHAPTER 3 presented the designs that were necessary to complete the integration of the hardware as well as design changes that were incorporated throughout the full system simulation and prototype integration. For example, the inverter controls were re-designed to tune them to hardware dynamics. Similarly, the PV boost controls were altered to take into account the full system operation dynamics.

A phase-shifted PWM generation technique was designed for the FB DC-DC converter as mentioned in [11]. This was necessary to control the duty cycle across the HF transformer and thus the HV DC link voltage (to avoid damaging devices). A control isolation board was also designed to protect the sensitive components from damaging noise induced by current carrying traces on the power boards. This protected the control hardware and improved control signal fidelity – thus improving the switching performance of the entire system.

CHAPTER 4 has presented the closed loop simulations of all designs in CHAPTER 3 In addition, it showed the full functionality in all operating modes with DC power sharing, AC power sharing, step loading, and the ability to respond to dynamic power flow commands. The transition between islanded – grid-connected – islanded operation with dynamic loading was also presented. Time constraints did not allow the experimental verification of all operation modes, but the simulating fully integrated hardware and hardware control is important for future development of the SGPN.

CHAPTER 5 has presented the closed loop test results for the inverter in island mode, FB DC-DC converter with phase shifted PWM operation, the closed loop sub-integration (full inverter (islanded) and PV boost converter + FB DC-DC converter), and two fully integrated closed loop operation modes – the PV boost converter + full inverter (islanded) and the battery charge/discharge converter + full inverter (islanded). A full system startup mode was also

developed. This is critical for protection of hardware due to the damaging inrush currents that can be experienced as a result of the bulk capacitance in the system.

After solving issues encountered through testing, the results obtained are consistent with the design goals set forth for the SGPN. Finally, all test results obtained thus far indicate the SGPN can operate under all functional operating modes that were designed with the following future work and recommendations.

6.2 Recommendations and Future Work

This section presents the recommendations for future work based on experiences encountered through the development of the SGPN. It will also incorporate the context of the work presented in this thesis as it pertains to the recommendations.

6.2.1 *Future Local Resources: Topology and Control Considerations*

The topology of the SGPN was designed to support multiple local DC and AC resources such as a wind turbine or an AC generator. This prototype was a proof-of-concept and therefore testing these additional sources was beyond the scope of this thesis. However, there are some important considerations for this added functionality that need to be addressed for future versions. An AC diesel or gasoline generator is a very common means for temporarily restoring power to a home during an extended utility outage. With the data processing and intelligence of the SGPN, these and other resources could be utilized more efficiently.

First, the use of an AC generator would only be needed during islanded operation, which simplifies the analysis and design. When the grid source is available, it is simply impractical to be running a generator as burning diesel or gasoline for electricity would be much more expensive than just using grid energy. This might seem like common sense, but it has important implications regarding the complexity of inverter controls. Further, there is no feasible way to

control the phase of the voltage that is output by the generator (much like this is not possible for the grid). Passive loads in the home "do not care" what the voltage phase is and will remain unaffected, regardless. However, if a generator closes in on the service entrance with a difference in voltage phase than the grid, significantly high inrush currents will circulate between the generator and the grid [42]. This is obviously dangerous and can cause damage to equipment.

To accommodate this extra resource, the SGPN inverter controls will have to be programmed such that only the grid source OR the AC generator source even has the ability to be switched into service at any given time, not both. An assumption made here is that the output of the generator will be routed through an SGPN disconnect switch where it can control whether or not power flows into the home. A disconnect on the existing board would need to be utilized, or if higher ratings are needed, a slight modification to the system topology would be needed. This will eliminate the potential safety hazard mentioned above.

When connecting to an AC generator, the inverter must operate in a similar fashion as though it were connecting to the grid. That is, the inverter must sync with the generator voltage before closing the relay and connecting at the AC bus. This should add no cost to the SGPN design. Rather, the future research would be software upgrades to include this functionality. Further discussion is presented on the control design in section 6.2.2.

6.2.2 *Synchronization with the Electric Grid/AC Generator*

In order to facilitate connections to the grid or a generator, there is future work needed in developing a code structure to support it. Currently, the full system has only been tested in islanded operation. The interaction between the DC-DC converters will be similar, but the control sequence will need to be modified for the inverter in grid-connected mode.

As mentioned, the inverter must synchronize with the grid before connection. TI provides a PLL function in ControlSUITE™ [29] that will alter the phase relationship of its output to

match the reference (the grid or AC generator voltage in this case). It is recommended that a "hybrid" islanded/grid-connected control case be integrated into the software. Based on certain qualification criteria, a specific control case is internally selected ("hybrid" mode, islanded, grid-conencted, start-up, etc.). This is a clean way of preserving the operation of each mode while providing the means for seamless mode transitions.

In islanded operation a voltage reference is generated internally to control the output of the SGPN. However, in this hybrid mode, that reference would be the generator or grid voltage. Prior to connection, this "hybrid" control state will be entered. The reference is taken from the grid and ran through the PLL thereby adjusting the phase of the inverter to match the other AC source while still islanded from it. After a minimum phase angle requirement between the two source voltages is met, the disconnect switch can be closed and the two combined at the AC bus.

It is a difficult task to take a written procedure and translate that into a working complex system. There will be much testing and due diligence to make sure there are no unaccounted variables. This is a key function that must be completed before a fully functional system can be obtained.

6.2.3 *Human Machine or Graphical User Interface*

As mentioned, with the amount of data collected and processed by the SGPN, a Graphical User Interface (GUI) will have to be developed to provide the home owner SGPN performance data, grid energy price, home load demand, individual load demand, alarms for showing device failures, graphical indication of presence of grid source, and a settings page for load prioritization/preferences. This presents the user with a breakdown of energy costs and a wealth of other data that might not otherwise be available. A remote control could be built in the gives the owner the option to disconnect the SGPN at any time. Further, open communications with the utility could serve as a platform for the service provider to get critical real-time information

about the distribution system at various points along the feeder (assuming a wide-scale deployment).

This module would also have to have communications capabilities through an internet connection to download weather data for the system level controller to calculate the projected PV power output. Many tools are available such as National Instrument's LabVIEW that can serve as the development software for this interface. However, this would require a computer to run which would be very impractical since the SGPN was designed to be a self-contained piece of equipment. Therefore some type of web-based application will need to be established. This would eliminate the need for a computer and all data could be processed through a compact communications card.

6.2.4 *Improving Low Frequency DC Voltage and Current Ripple*

It was seen through simulation of the full system that there was a sizable ripple voltage and ripple current on the input of the batteries and PV systems as well as the DC link voltages. This will cause unnecessary heating of the input inductors, link capacitors, batteries, and solar hardware itself. This heating will degrade battery life and the life of SGPN hardware. In addition, the size and weight of the thermal management system must be increased, which increases the size, weight, and cost of the whole system.

There are several techniques to mitigate this effect such as an input low-pass filter to the converter. However, again, this increases the size, weight, and cost to the system. There are control techniques such as [43] that incorporate a voltage suppression block that would eliminate the 120 Hz induced ripple from the inverter. It isolates the ripple content through a high pass filter. Then an inverting unity gain block is utilized inside a feed-forward network producing a compensation value exactly 180° out of phase with the ripple voltage. This would be

supplemental to the existing control structure. Implementing such a system to the DC control network would suppress this ripple voltage and thus reduce heating and improve hardware life. An investigation needs to be conducted to see if this feed-forward network can be integrated with existing control loop structure. This could also change the dynamics of the control design, so a re-design of the boost controls might be needed. If feasible, this is a desirable solution since it requires no additional hardware or cost.

The same heating concerns for the batteries are present for the electrolytic DC link capacitors as well. However, since the FB DC-DC converter is currently run open loop, this technique would require closed loop controls to be developed for the FB converter as well as part of the future work. There are other techniques that are possible discussed in section 6.2.5.

6.2.5 *Harmonic Filtering & Harmonic Mitigation Techniques*

It has been mentioned that through simulations, experimental testing of the full system, and in [11] the LCL filter does not meet the THD requirements of IEEE 1547 under light loading conditions. This can attributed to the filter design and the fact that the harmonic content is simply a higher percentage of the current amplitude at low power levels. It is unlikely the SGPN would ever be run at extremely low power levels (≈100's of Watts). However, it is important for a robust design that it meets these requirements at virtually all power levels.

In CHAPTER 4 , an isolation transformer was modeled for grid-connected operation in which the leakage inductance helped filter out higher order harmonics left from the sine-modulated output from the inverter. This will be a crucial design change that should be integrated into future versions for safety in connecting to the grid. In this way, the harmonic suppression benefit of the isolation transformer will be extended to islanded operation as well.

Proper testing will need to be conducted to determine the amount of harmonic reduction is accomplished by this method and if additional solutions are required.

There are many other methods of simple, passive filtering of harmonics such as line reactors (same principle as the leakage inductance of the isolation transformer), K-factor transformers, and tuned harmonic filters. K-factor transformers are typically a Delta-Wye connected transformers that help reduce triplen harmonics through circulating them in the delta [39]. However, these are generally more expensive (on the order of 2x cost [39]) because they are constructed to withstand the extra heating from harmonic currents and have higher rated neutral conductors. Tuned harmonic filters can be used to eliminate a single harmonic frequency. For example, the resonant frequency of a LC circuit can be designed to be right at the 3rd harmonic (180 Hz) since it is the most significant from a single phase inverter. These methods all add weight, space, and cost to the prototype. However, given the isolation transformer benefits and necessity for safety, it is recommended the research and testing be done for future versions.

It is unlikely that a single one of the methods of harmonic mitigation mentioned above will be the ideal solution. An in depth investigation is needed into the severity of the problem after the further testing of the prototype is completed. Then a combination of the techniques will need to be analyzed based on standards requirements, cost, size, weight, and complexity to determine the best solution.

6.2.6 *Future Work on SGPN Startup Sequence*

In section 5.6.2 a startup sequence was presented for the PV boost with full inverter in island mode operation. Through each step of integration there were challenges encountered that drove decisions for shaping the system startup. However, there are many different scenarios can affect the SGPN startup. More research is needed into the different factors that should be taken into consideration and the effect it could have on the operation of the system.

For example, the PV boost converter involved setting checks for a minimum input voltage before certain stages of the system were activated given the non-constant nature of the PV input. The battery charge/discharge converter has a relatively constant input voltage to the system, so the same startup procedure might not be well suited. Similarly, when the two converters are interleaved at startup, the procedure might deviate further.

One option would be to have a startup mode for each specific condition, but this would be tedious and make the programming even more complicated. A universal startup mode might be a better solution where the SGPN would start in a "default" mode regardless the inputs available, then transition to a steady state operating mode. Since the batteries are a stable input source (which assumes they are not deeply discharged), and the PV input is intermittent by nature, the battery converter could be used as the default input converter in startup mode. A pre-insertion resistor would be required to start the battery converter with a temporary load to ensure a stable startup. The full inverter would then be started to reach a steady state output. Once certain "check" conditions have been met, the SGPN could either serve load (island mode) or enter the "hybrid" control mode (section 6.2.2) and sync with the grid (grid-connected mode or AC generator). After determining whether to be islanded or grid-connected, the decision to enter DC power sharing mode (dependent on if the PV source is available) would be made.

There are many different scenarios that could be conceived. Further research of similar systems and testing is needed to determine what would be the best way to approach this problem. Additionally, this would have to seamlessly integrate with the system level controller. The system level controller could be disabled during system startup for example. Regardless, the work done through integration to this point gives a good base for future development.

6.2.7 *Recommendation for Improving Efficiency*

The efficiency quoted for the full system operation at around 200 W was 82.8% & 80.7% for the PV input and the battery input, respectively. This is expected to increase with increased loads, but there is much room for improvement. At turn off in "hard-switching", as the gate voltage is removed, there is a transition period when the voltage across the device increases and the current flowing through the device decreases which is known as the switching loss. At turn on, the opposite happens in addition to the diode reverse recovery power loss during a similar transition.

"Zero voltage" or "zero current" switching offer some benefits in reducing the switching losses of the system. However, this includes complex design techniques in which the resonance point between the gate capacitance of the switching device and the leakage inductance of the transformer is used to achieve the ZVS or ZCS. Typically ZVS is used for MOSFET devices since they are voltage controlled. Similarly, due to high tail currents for IGBTs, ZCS is typically preferable.

This prototype was a proof-of-concept version, and efficiency was not the main focus. Therefore the extra design complexity was not attempted. However, efficiency is obviously a major concern. Future design work is needed to determine what modifications need to be made to the SGPN to incorporate soft switching.

During hard switching, the sudden large dv/dt and di/dt across switching devices also produces high frequency ringing due to the parasitic capacitance and inductance in the circuit. This causes large amounts of EMI. Soft switching reduces the negative effects of parasitics in the power board layout by significantly reducing the dv/dt and di/dt during switching transitions. This will not only boost the efficiency of the system, but also reduce EMI. Less conducted EMI through the circuit will also reduce the high frequency harmonics injected into the output inverter

current. In addition, the power layout can be improved to reduce the effects of EMI. This is an extremely important topic that should be researched for future developments.

6.2.8 *Improving Efficiency & Performance of the Full Bridge DC-DC converter*

The phase-shifted PWM switching scheme that was implemented for the full-bridge DC-DC converter achieved the desired control over the duty cycle implemented across the high frequency transformer and thus the HV DC voltage in open loop operation. However, the converter still suffers from the low frequency 120 Hz ripple voltage induced on the DC system from the H-bridge inverter. The increased DC bus capacitor size reduced this effect to a manageable level, but the ripple can cause undue heating and reduce the lifetime of the capacitor which in turn reduces the reliability of the system.

The phase-shifted PWM modulation basics are commonly used in closed loop control of the dual full-bridge DC-DC converter and can easily be designed. The phase-shift modulation is used with resonant tank circuits to achieve ZVS which increases the efficiency [44]. However, at operating voltages on the primary and secondary with a large deviation from the nominally designed voltages, the conduction losses of the semiconductor devices, and transformer losses increase dramatically – thus eliminating the efficiency gains of ZVS [45]. Therefore a new modulation scheme should be considered to increase the efficiency of the converter.

In [46], a novel efficiency-optimized modulation scheme is developed for a Dual Active Bridge DC-DC converter that has a proven efficiency of >90 % for a 2 kW rated converter. It is based on the principle of reducing the amount of RMS currents in the high frequency transformer and extending the range of ZVS switching to very small loading as well as very high loading. This type of control is an example that future versions could incorporate to increase system efficiency through software (without changing hardware) – thus a zero cost improvement.

6.2.9 *Possibility of D-Q Control*

The current control of the H-bridge inverter uses PI controllers in a double loop system. Since the reference for the sinusoidal output voltage of the inverter is constantly changing, there will always be a lag with a PI controller. That is, a PI controller is incapable of tracking a changing reference with zero steady state error [36]. In turn, there is a possibility for a sizable error between the reference and output voltage.

Instead of constantly "chasing" a varying reference signal, a synchronous frame D-Q controller converts this reference into a constant signal. Therefore simple PI controllers can be designed to yield a 0% steady state error. This will help the SGPN to better respond to dynamic conditions within the system and thus maintain a stable output to home loads.

Synchronous D-Q control does involve some extra complexity given the math transformations of "real-world" values to the rotating D-Q frame. This will need to be explored in how to program these to a DSP. Given the available benefits of D-Q control over linear control for inverters, this improvement should be designed and implemented with future versions.

6.2.10 *Future Verification & Full System Integration with System Level Controller*

Thus far the PV boost converter, battery charge/discharge (in charge and discharge modes) converter, full bridge DC-DC converter, and PV boost + battery charge/discharge converters with power sharing have been tested closed loop in [11]. This thesis has presented the PV boost + full bridge DC-DC converter, H-bridge inverter, full bridge DC-DC converter + H-bridge inverter (full inverter), PV boost + full inverter, and battery charge/discharge converter + full inverter tested with closed loop control in island mode.

The power sharing between input DC-DC converters with the full inverter must still completed. In addition, all grid-connected tests must be performed with mode transitions. These

tests are critical to proving the full functionality of the SGPN hardware and must be conducted for future work. For clarity, a graphical representation showing the complex interactions between the hardware and hardware control has been developed and is shown below in Fig. 6.2.1.

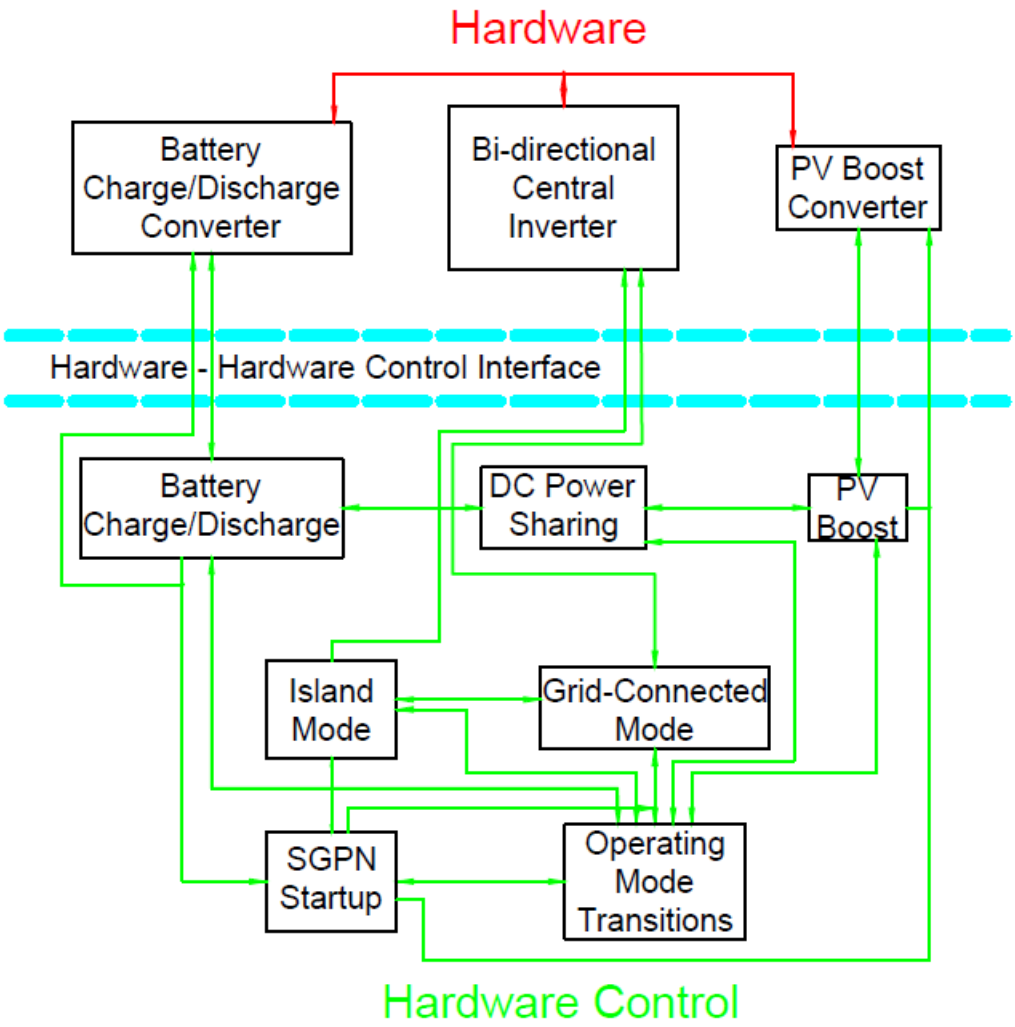

Fig. 6.2.1: SGPN Hardware and Hardware Control Interaction Block Diagram

Testing of the fully integrated prototype is the key to closing the prototyping phase and drawing conclusions about the overall system as a whole. This would include the integrated hardware/hardware control, communications to the GUI/user interface, and the system level controller. The integrated hardware must be tested in all conceivable operating conditions to

solve any unexpected issues before plugging high level commands to the switching control block. Functional tests can then be conducted including the active control of home loads/load shedding, cost savings analysis, “smart” islanding/re-connecting to the grid, responding to commands remotely through the GUI, etc. Once completed, a high level analysis on the long term practicality of this system can then begin such as determining the scalability, collective effect of a wide-scale deployment such as becoming a real-time information asset for improving grid quality/reliability, effectiveness as a peak shaving device, and the economic appeal to consumers based on their geographical location.

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