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A Reconfigurable Digital-to-Analog Converter with Supply Invariant Linearity

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By

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University of Arkansas
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ABSTRACT

A novel reconfigurable digital-to-analog converter (DAC) with supply independent linearity is presented. The process agnostic converter achieves wide supply range operation and re-configurability by being charge based. This converter consists of a 7-bit parallel digital input control core and an analog "summing" core utilizing charging capacitors with an operational transconductance amplifier in a voltage-follower configuration. This topology is highly configurable to allow for optimization across process voltages, step sizes and low power operation. The specification of the DAC is (1) supply independence (2) low power operation (3) operation up to 200 kHz and (4) conversion control through a DAC enable signal. Supply independence is achieved through the use of a charge-based approach in the analog core utilizing a finite stepping voltage derived from another, much smaller, voltage reference. This voltage reference in turn determines the resolution of the DAC. The DAC will thus create a "stair-stepping" analog output until digital input is met or the voltage supply is reached. Feedback is utilized when either of these events occurs notifying the DAC to wait until another sample is requested. Low power is achieved by using static CMOS logic and the inclusion of a "sleep mode" in the analog core which can be used after the desired output is achieved. This design was implemented across two different processes with different power supplies to confirm the architecture.

ACKNOWLEDGEMENTS

Countless thanks are due to Dr. H. Alan Mantooth and Dr. A. Matt Francis for all of their support and guidance in the author's pursuit of a master's degree. Added thanks are to be given to Dr. Randy Brown and Dr. Jia Di for their expertise and advice.

Great thanks are given to all of the author's colleagues and classmates for all of their added advice and instructions, the experience that was shared is priceless.

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DEDICATION

This thesis is dedicated to my family whose support in my educational pursuits has motivated me to work harder every day, also, to my wife, Erin, who has been my rock throughout this journey.

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CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DFF	D-Type Flip Flop
DNL	Differential Non-Linearity
DRC	Design Rule Check
FSR	Full Scale Ramp
HiDEC	High Density Electronics Center
INL	Integral Non-Linearity
LED	Light Emitting Diode
LVS	Layout vs. Schematic
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSCAD	Mixed-Signal Computer-Aided Design
NFET	N-Type Field Effect Transistor
Op-Amp	Operational Amplifier
PCB	Printed Circuit Board
PDK	Process Design Kit
PEX	Parasitic Extraction
PFET	P-Type Field Effect Transistor
SBIR	Small Business Innovation Research
TFF	T-Type Flip Flop
TSMC	Taiwan Semiconductor Manufacturing Company
VLSI	Very Large Scale Integration

CHAPTER 1 – INTRODUCTION

1.1 Project Motivation

Data converters are an important element in any system that requires the need to interface digital control with analog signals. Data converters can be discrete or integrated with other functions. The application presented is of a maintenance use (e.g. battery monitoring). The University of Arkansas (UA) was approached in August of 2011 about consulting on a project with Ridgetop Group from Tucson Arizona, SBIR Phase II W31P4Q-11-C-0068. The project scope was to design and simulate a digital to analog converter with the specifications as given in Table 1.1. Ridgetop Group would then construct the layout of the design provided by the UA.

TABLE 1.1. DESIGN SPECIFICATIONS OF BOTH PROCESSES.

Design Specifications	**XFAB**	**TSMC**
VDD	1.5V – User Input (15V at most)	0V – User Input (5V at most)
V_{ref}	1.05V	34mV
Offset	1.5V	0V
V_{out} Range	1.5V (0000000) – VDD or Binary Value	0V (0000000) – VDD or Binary Value
Power Consumption	100 µW conv. 100 nW sleep	N/A
Conversion Time	<1.28 ms	<1.28 ms
Sampling	Hold output for 10min within half LSB.	Hold output for 10min within half LSB.

The two most challenging specifications include the supply range and power requirements. First the DAC must operate over a wide voltage supply range; from 1.5 V to 15 V. Second, it requires two low-power operating modes. It must consume less than 100 µW during a conversion and less than 100 nW during sleep mode.

The design of the DAC was performed in Cadence 6.1 using the XFAB 0.6 μm process design kit [1]. Since the power supply range of the DAC requires high potential devices, high voltage MOSFETs were used (45 V). These devices have a minimum feature size of 3μm. The design is novel in two ways. First, it operates linearly over the voltage supply range, causing its resolution to change as the supply voltage changes. Second, it has two low-power modes: running mode and sleep mode. Common to DACs, there are both digital and analog portions of the design. Both parts are constructed from the bottom up using MOSFETs with a higher blocking voltage than typical CMOS transistors, along with high voltage passive elements such as resistors and capacitors. After successful fabrication in the XFAB process, the DAC was implemented in one other Si process; the TSMC 0.35 μm process [2]. This process utilizes 5 V devices. This version was designed in Cadence 5.1 with the aid of Spectre, for simulation, and Calibre for DRC, LVS and PEX. The minimum feature size for the TSMC kit is 0.35 μm for the 3.3 V devices. The 5 V devices have a minimum feature size of 0.5 μm. The ratio of threshold to total voltage range of these MOSFETs is different than the XFAB devices and will verify the DAC architecture; if operational.

1.2 System Overview

In order to fully understand the specifications of the DAC presented, the full system around this DAC must be explained. The application of the full system is for low power battery monitoring for mobile backpack units. The goal is to monitor the battery voltage in order to make the user aware of how much power is left in his/her mobile unit. This will alert the user of how much time he/she has before running out of power. The battery monitoring system must be low power as to not draw significant power itself for monitoring the battery.

CHAPTER 2 – SURVEY OF DIGITAL-TO-ANALOG CONVERTERS

2.1 Converter Overview

Data converters are essential for processing information. Processing is much simpler in the digital realm. However, information does not exist naturally in a digital format. Therefore the need to convert between the two is essential. There are many data converter designs, however, the need for low-power applications has pushed innovation in all areas of semiconductor manufacturing, not excluding hardened converter designs.

Data conversion can be achieved in different ways. There are several designs that provide differing advantages depending on the application. Typically, data converters are used in a system that requires sensing, processing, and output of processed data as seen in Fig. 2.1.

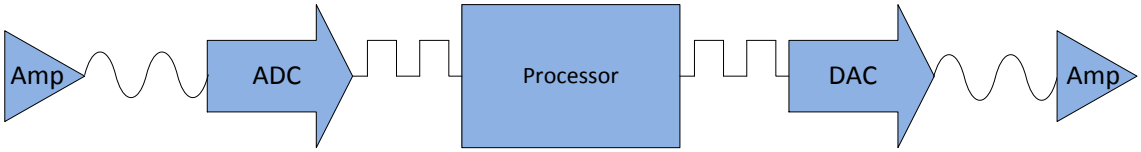


Fig. 2.1. Data conversion system.

The processor represents a full digital system, wherein signal processing occurs in a digital signal processing core. After sampling and processing, it is often required to have the processed data output as an analog signal as well. This is where digital to analog converters play an important role.

Digital to analog converters, as all electronic systems, have standard elements of validation or ways of measuring its performance. There are two important standards of error measurement for data converters; they are integral nonlinearity (INL) and differential nonlinearity (DNL) [3]. DNL is the difference of an ideal voltage increment as compared to a non-ideal (measured) voltage increment in the output characteristics as seen in Fig. 2.2.

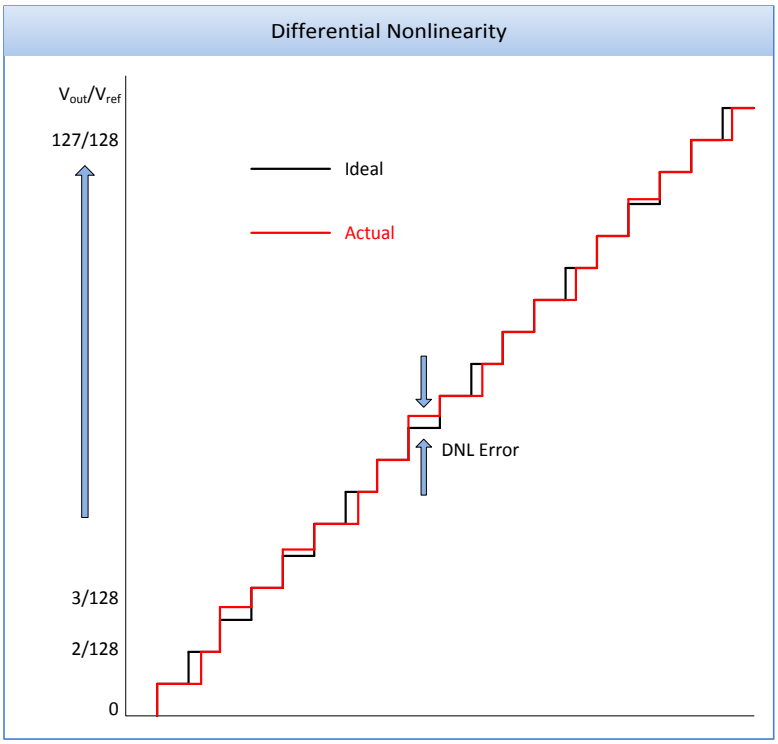


Fig. 2.2. Illustration showing differential nonlinearity.

INL is the measurement of error on a full scale range. It measures the accuracy of the output curve as a whole. There are two types of INL measurements, best straight line and end point line. The best straight line is most commonly used, seen in Fig. 2.3.

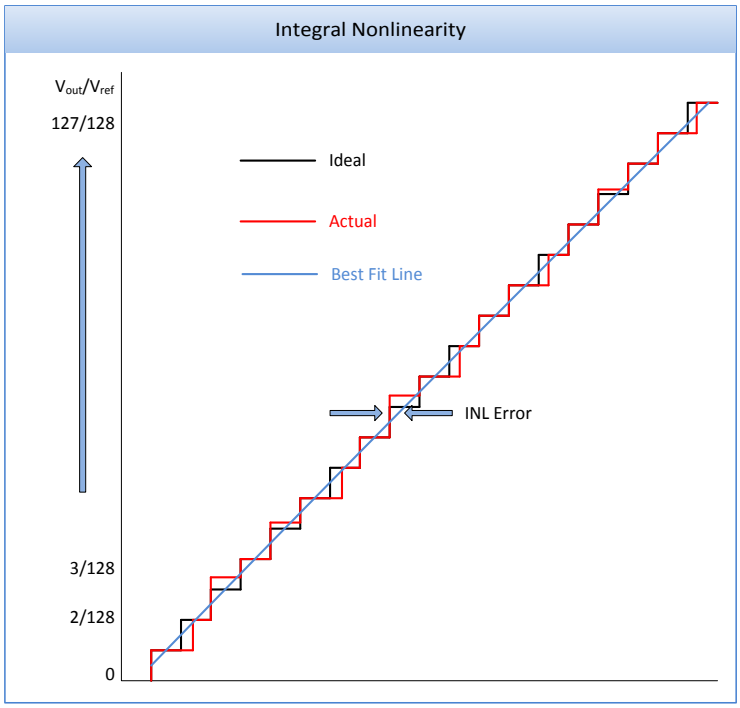


Fig. 2.3. Illustration showing integral nonlinearity.

2.2 Application

Data converters are used in mixed-signal applications. This is a system in which both digital and analog circuits are present. An example of the use of data converters is in the music industry. The use of digital signal processing is found more throughout the instruments that artists are utilizing today. An example of this application is the auto-tuned effect. Its goal is to manipulate off-key pitches to match the closet pitch. It samples the analog input of the singer, processes the digital interpretation of said signal, and outputs an analog signal that has been shifted to match the closest pitch. The basic system diagram can be seen in Fig. 2.4 [4].

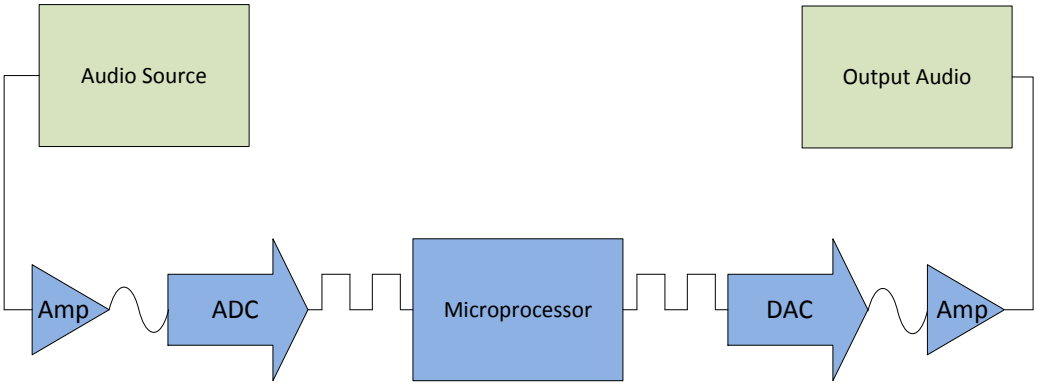


Fig. 2.4. Data converter application.

2.3 Digital-to-Analog Converters

DACs can be grouped into two main categories: passive (static) or recursive (cyclic). A popular example of a passive DAC is the R-2R ladder. This method uses a series of resistor divider networks connected to an op-amp in order to generate an analog value. The R-2R architecture can be seen in Fig. 2.5 [5].

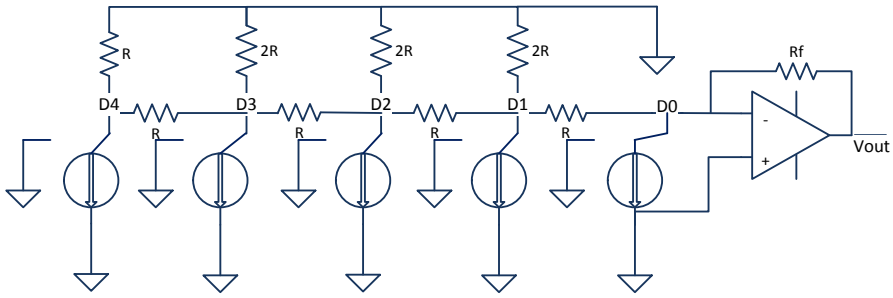


Fig. 2.5. R2R digital to analog converter.

The branches on the ladder are enabled/disabled by the DAC's binary input signals. While simple, reliable and accurate, the shortcoming of this approach is the power consumption of the resistors.

An example of a cyclic DAC is any sample and hold circuit. This topology uses a few conceptually simple blocks to either add or subtract a reference voltage to achieve the desired analog value (Fig. 2.6) [5]. The advantage of this topology is its low power requirement. The

disadvantage, however, is the complexity introduced by the digital controls. For the non-linear, supply invariant design presented, a converter loosely based on the cyclic approach has been adopted.

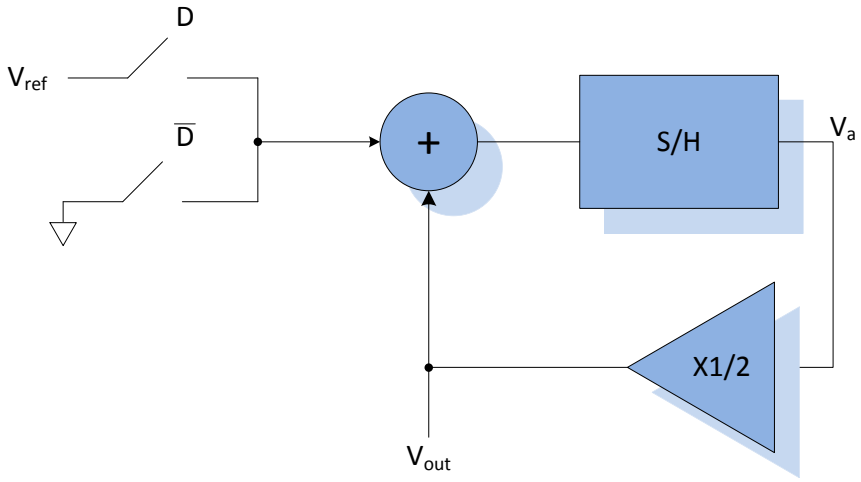


Fig. 2.6. Cyclic DAC architecture.

CHAPTER 3 – RECONFIGURABLE DIGITAL-TO-ANALOG CONVERTER DESIGN

3.1 Top Down Design

Given that the specifications for this DAC lend themselves to a new, novel topology, a top down model based approach was implemented in order to verify first principles of operation and find the correct progression to a working architecture [6]. The top down model based approach is one that uses the idea of decreasing levels of abstraction (from a high-level model in the design stage to a fully transistor-based schematic at the implementation stage) to simulate the behavior of the final design incrementally. This allows one to confirm higher level ideas before diving into the transistor-level design of specific components. In order to take the most optimum path to the final design it is critical to verify the operation of the model from the very beginning in order to make sure the fundamental architecture is valid. The design and verification process can take many paths but is essentially comprised of increasing levels of detail beginning with a functional behavioral specification, down to transistor level design, and finally ending with functional verification again back at the highest level. High level specification therefore leads into the "skeleton" of the design or the architecture. Once the architecture has been verified some form of implementation will take place in a design tool or on a bench top test. The next step in the design process will be some form of block level simulation. What is defined as a "block" is a freedom for the designer to define. These blocks will then be designed to satisfy the final implementation and the entire system will be completed. Verification is the process of working back from the lowest level (transistor implementation) back to the highest level (functional) to verify system performance and correctness. As it pertains to the DAC; simulation of the physical design will be the final verification step. It will fall under IC verification. The process just described follows an approach called the "V" diagram shown in detail in Fig. 3.1. During the

progression in detail down the left hand side of the “V” diagram, recursive loops to validate the design where utilized.

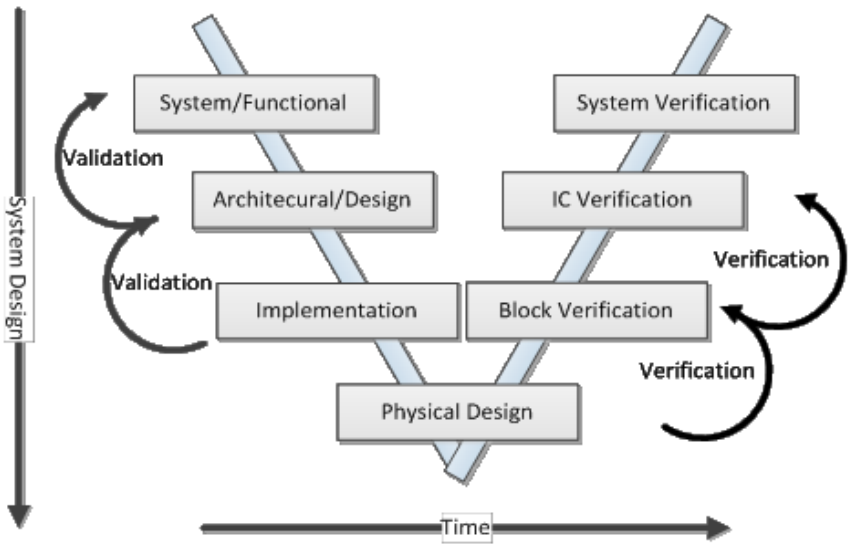


Fig. 3.1. V diagram for design.

3.2 System/functional

What follows is the first step in model based design; the System/Functional step highlighted in Fig. 3.2. The main concept in this step is the high level validation of the design. This step is crucial; if the top level model does not work, major design changes to the system must be made and significant time would be wasted if implementation began. This high-level model allows the designer to verify top level ideas before more moving parts are added to the design.

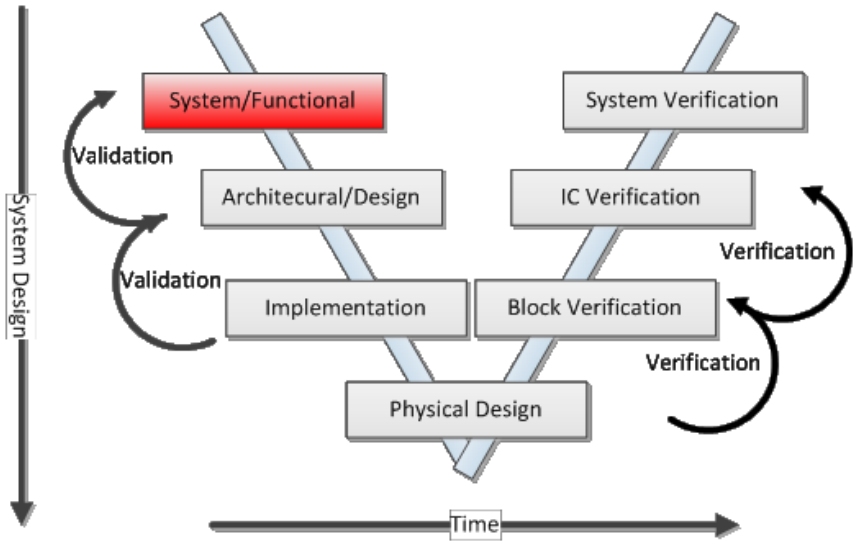


Fig. 3.2. V diagram with system/functional highlighted.

Based on the specifications given the design chosen for the DAC was first implemented using high-level models as a charge pump based system that uses two ideal capacitors and an ideal op-amp in its core to "pump" 105 mV increments onto each capacitor at alternating clock edges as shown in Fig. 3.3.

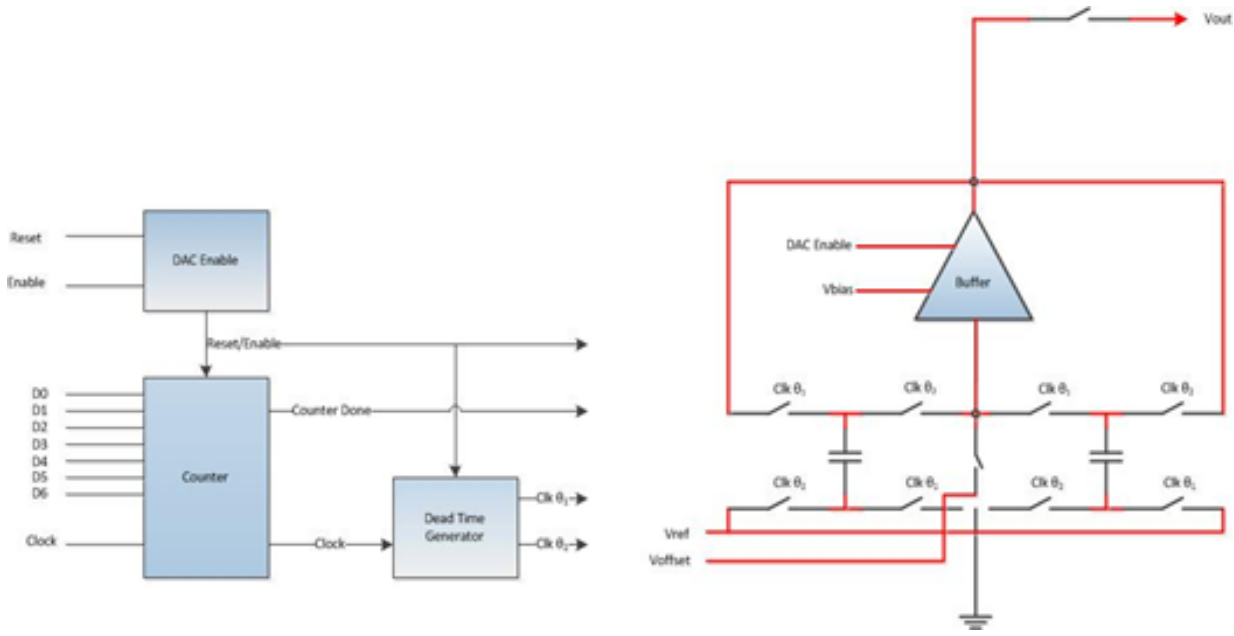


Fig. 3.3. DAC system model.

In this design the op-amp serves as a unity-gain buffer to supply a reference to the capacitor being increased in voltage value, while the other capacitor serves as a reference (the last stored value). The main components of the design are a counter, a dead-time generator, an op-amp, and the entire analog core (op-amp, capacitors and switching devices). Simulation of the high-level model shows that it is dependent on good symmetry as well as matched dead time in the clock signal (Fig. 3.12). Since there is much switching that will occur within this approach, some noise will be introduced during conversion time. Another consideration that is vital to this design is the op-amp. It must meet the low power specifications and be capable of saturation within 98% of VDD to meet accuracy requirements. To produce a consistent result for each 105 mV charge pump step the settling time of the op-amp system is desired to be within half of a clock pulse. For the given 200 kHz clock this works out to be approximately 2.5 μs.

To meet sleep mode requirements the system is designed to be dormant until the user-accessible input DAC_EN is asserted. At this point the counter block will pass the 200 kHz system clock signal to the dead time generator. The counter will then begin incrementing. Meanwhile the voltage on the core capacitors increases in 105 mV steps. After the user supplied binary value is matched within the counter, the clock is cut-off to the core and sleep mode will be asserted after latching the output value.

As previously mentioned, the main system level blocks were implemented at the top level. These blocks use behavioral logic gates and ideal switches to verify the operation of the architecture. The counter is the main control logic for the DAC. It utilizes an array of toggle flip flops tied to one input of an XOR gate. The other input is tied to the user binary input. When the signal is exclusively matched the outputs of the XOR gates are fed into a latch. This disables the

clock to the system once a match has occurred. The counter operates at 200 kHz and can be seen in Fig. 3.4.

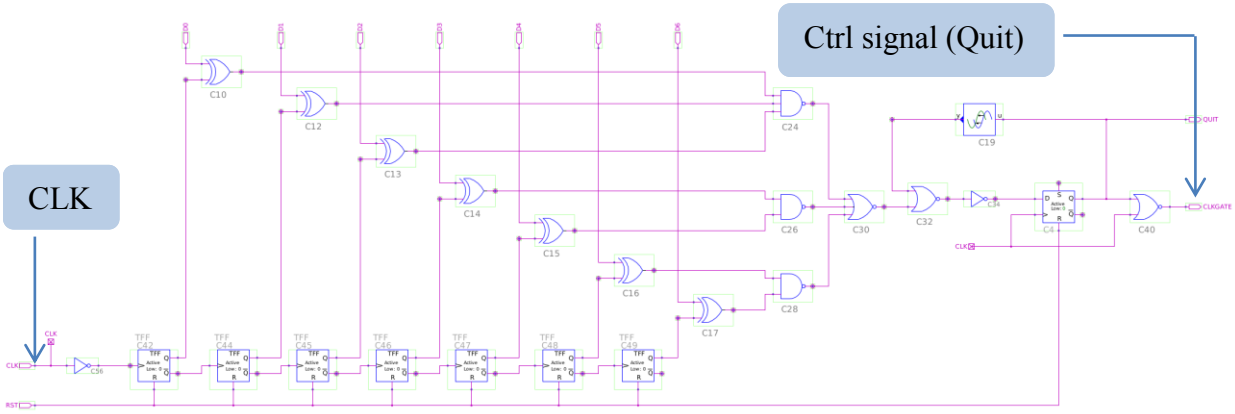


Fig. 3.4. Counter model with ideal gates.

The core of the DAC, as shown in Fig. 3.5, is the bulk of the analog portion of the design. It contains the op-amp buffer, the capacitors, and the transmission gates used for switching the charge pump topology. The core takes in different digital control signals along with analog power and ground. The minimum step size is set with a reference of 105 mV. This 105 mV reference is generated by using large resistors to divide the 1.05 V source by 10. Many design implementations where evaluated for generation of the 105 mV reference. One design evaluated utilized a switched capacitor divider topology. While somewhat successful, this design was disregarded when it became clear that the size of the capacitors required for the divider to provide a rigid 105 mV reference for the target DAC capacitors was far too large to be reasonably fabricated. The resistor divider approach using high-power, high resistance (3.5 kΩ/□) resistors was sized to provide the most rigid reference over temperature with minimum impact on layout size.

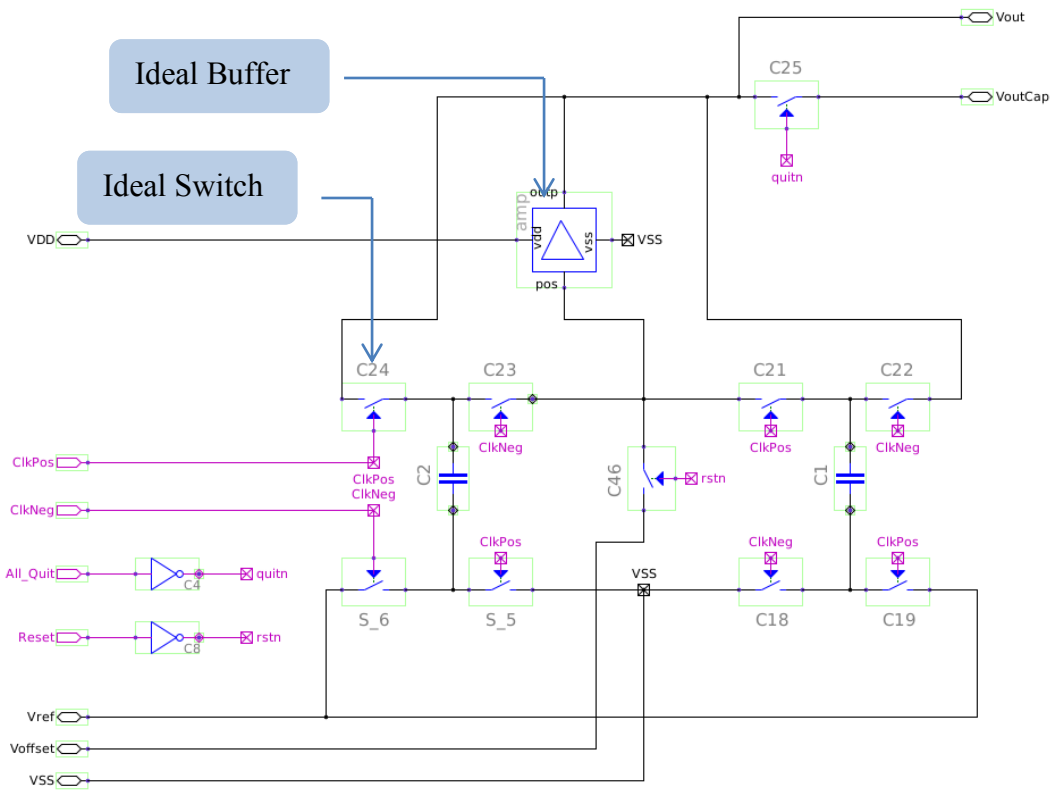


Fig. 3.5. System DAC core model with ideal switches and capacitors.

At the system model level the two phase clock generator is simply two identical clock generator models 180 degrees out of phase. These two clocks are set to pulse at 200 kHz in order to match the design specifications.

3.3 Operation

Operation of the DAC begins with the core. The function of the core is to make the ramping action occur on the output of the DAC. The circuit diagram illustrating the state of the core after the first phase of operation is included in Fig. 3.6 below. As C1 and C2 are at 0 V for the first phase, the capacitor in series with the input of the Op-amp, (C1), charges until 105 mV (provided by the reference voltage) appears on the input of the buffer. This in turn drives 105 mV on the capacitor connected in series with the output of the buffer. Fig. 3.7 illustrates the active branch during this first phase.

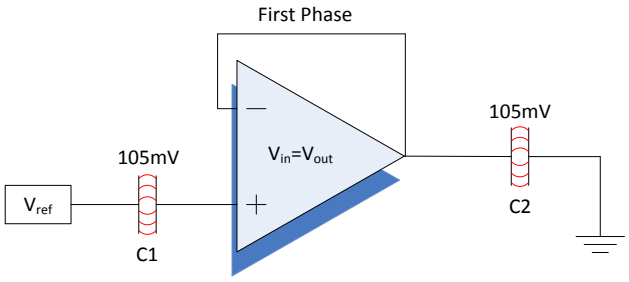


Fig. 3.6. Model of first clock phase.

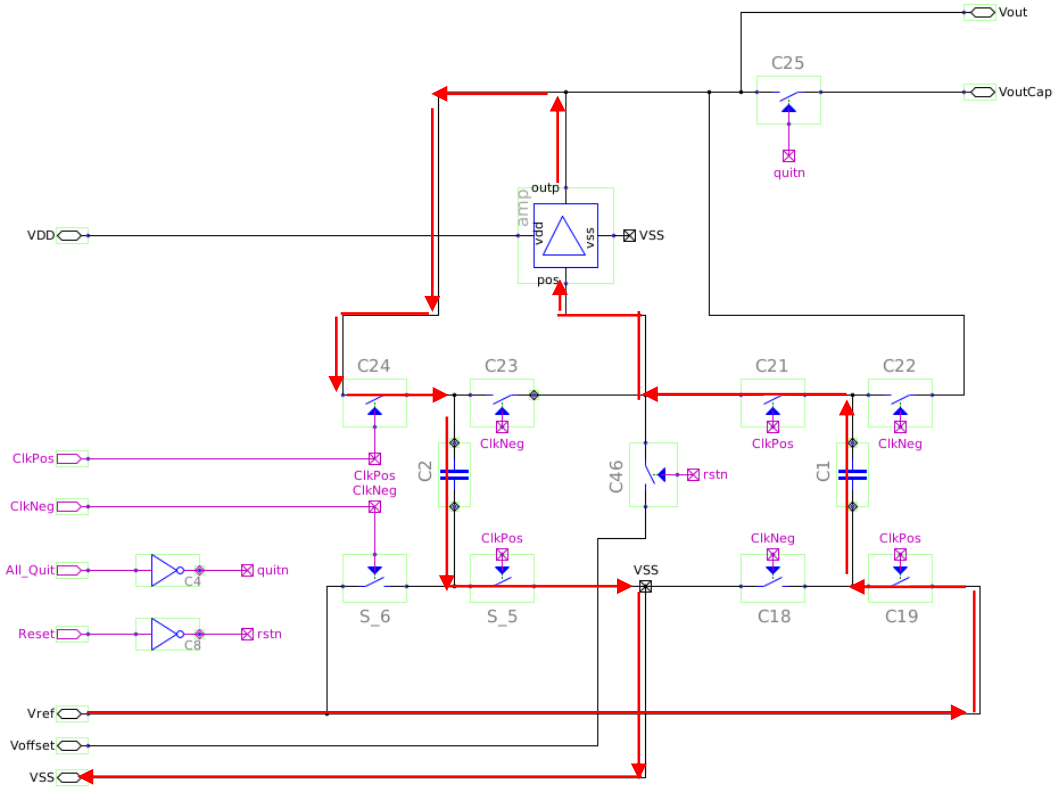


Fig. 3.7. DAC core with charge path during phase one highlighted.

After this first clock phase the signal begins to fall and the second clock phase will begin to rise, turning on the opposing half of the core architecture. Fig. 3.8 illustrates the circuit state after this occurs. The reference remains at 105 mV as a result of using the output buffer. The capacitor C2, now connected to V_{ref}, has 105 mV stored from the previous cycle. This drives the voltage at the input of the buffer to 210 mV with respect to ground. The buffer in turn increases

the charge on the capacitor connected at its outputs (now C1) until 210 mV is obtained. Fig. 3.9 illustrates the active branch during this second phase; notice the symmetry of the analog cores operation. Because of this symmetry, it is crucial to make sure that these two phases are never on at the same time.

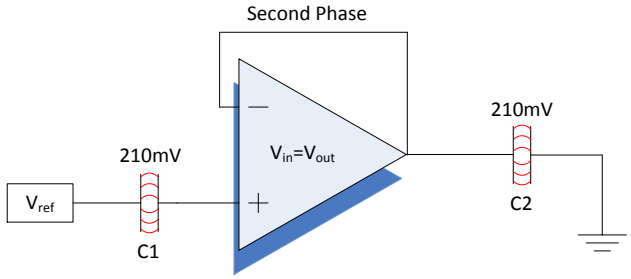


Fig. 3.8. Model of second clock phase.

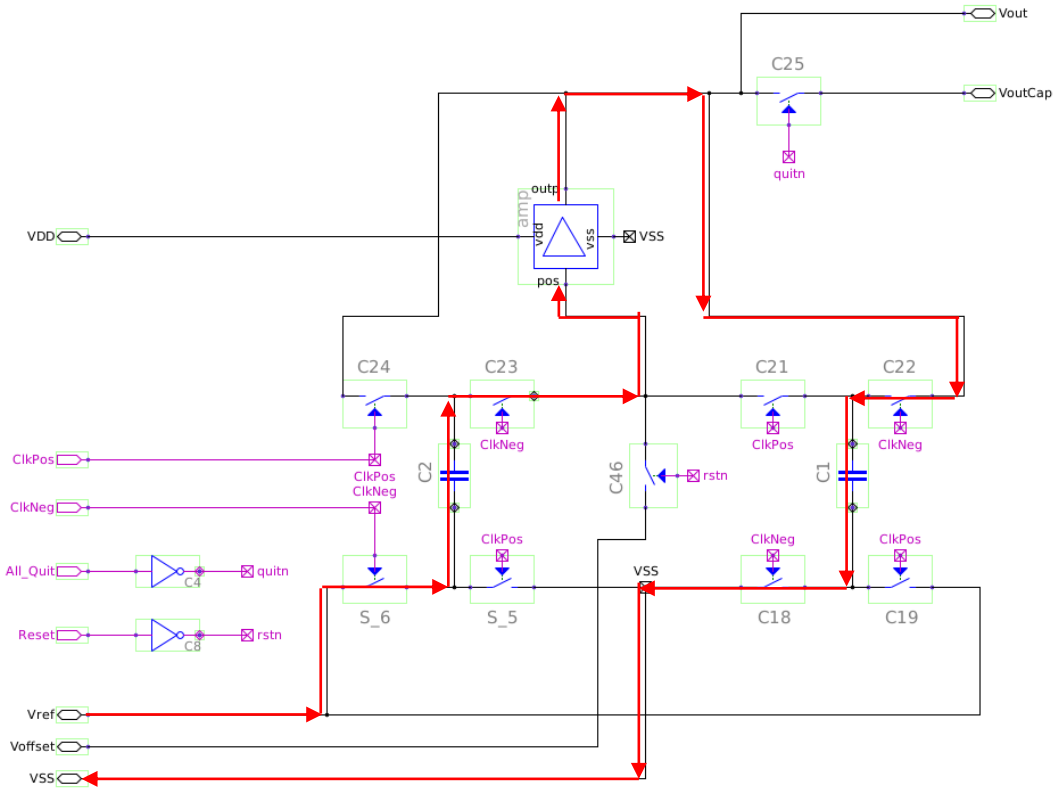


Fig. 3.9. DAC core with charge path during second phase highlighted.

Note that the buffer does not directly provide a voltage increment of 105 mV; as a 1:1 buffer it simply provides the drive strength to charge the capacitor on its output at its respective clock phase. This operation is repeated until either the op-amp saturates or the binary value is met and the counter disables the clock to the core. This charge pump action is possible, without charge distribution on the capacitors, because of the driving force of the buffer.

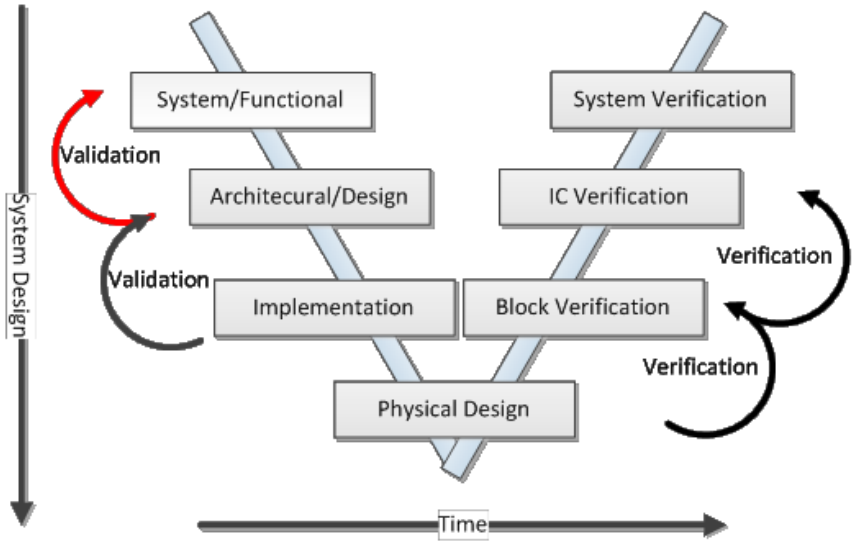


Fig. 3.10. V diagram with validation of system highlighted.

Validation of the top level operation is given below. Fig. 3.11 shows the test bench that implements the analog and digital core of the models introduced previously. This test bench utilizes ideal clock signals and ideal voltage sources.

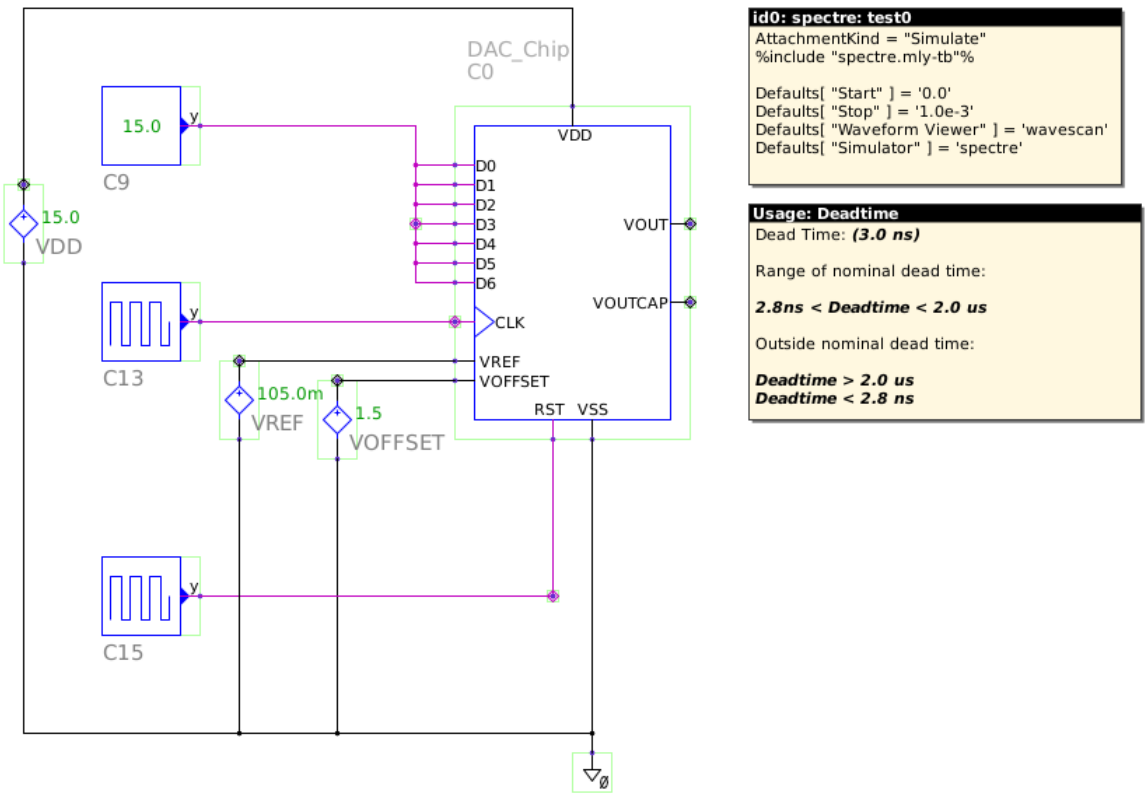


Fig. 3.11. Top model test bench of DAC with ideal clock and voltage sources.

This step is necessary before progression down the left side of the "V" diagram can continue (Fig. 3.10). The simulations demonstrate the three main operations required. The full scale ramp can be seen in Fig. 3.12, where the model validates the operation of the DAC from 1.5 V to 15 V. The binary match from user input can be seen in Fig. 3.13, which validates the operation of the DAC to a user input value. The power supply saturation is given in Fig. 3.14, where the DAC ramps until it saturates the internal op-amp at the power supply.

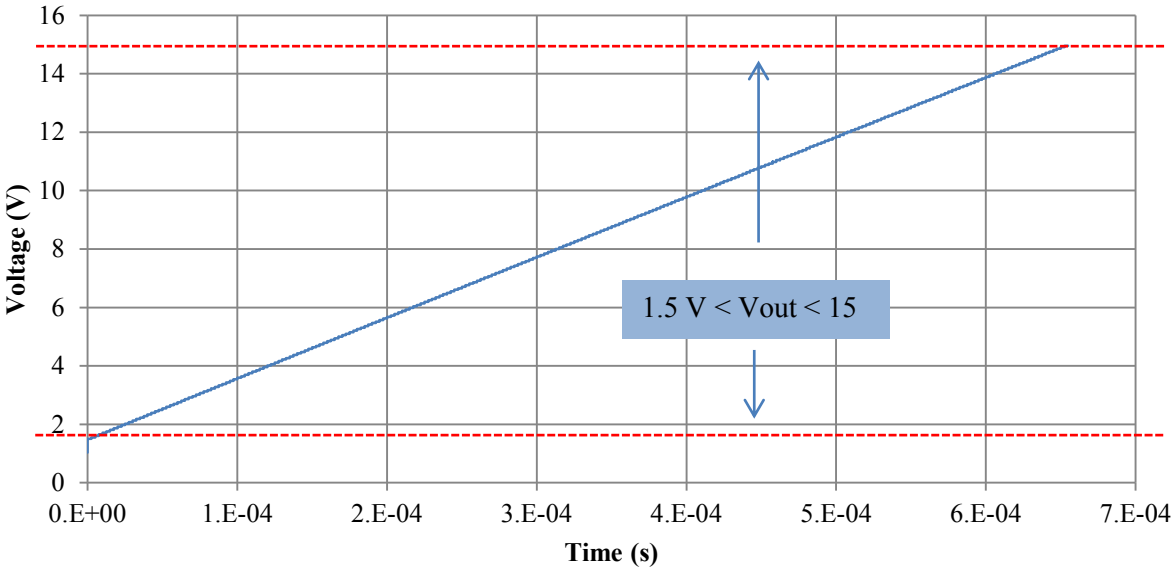


Fig. 3.12. Full scale ramp of DAC output from 1.5 V to 15 V.

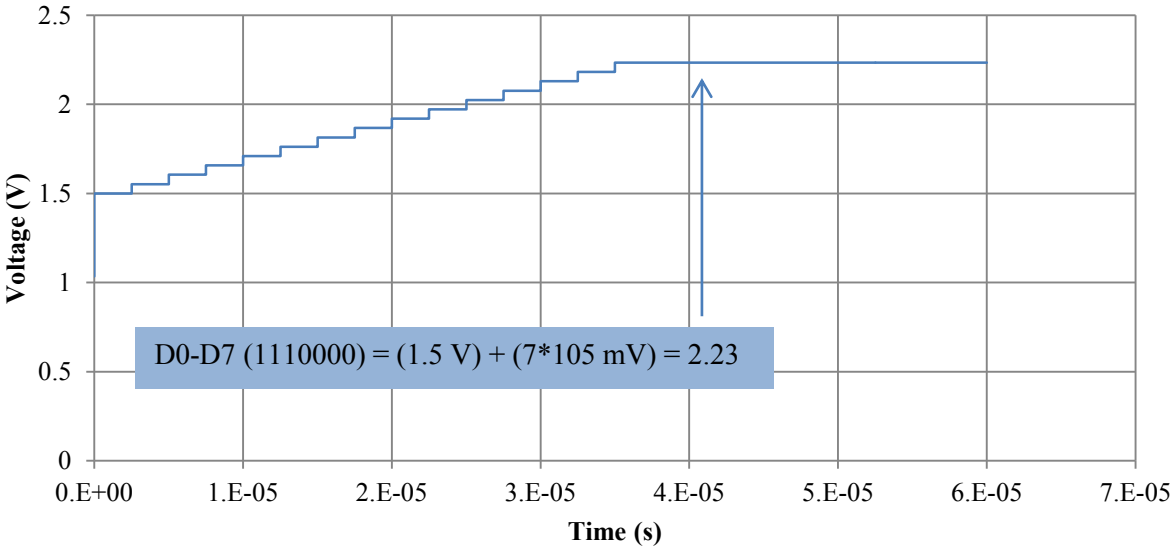


Fig. 3.13. Binary match of DAC given a user input.

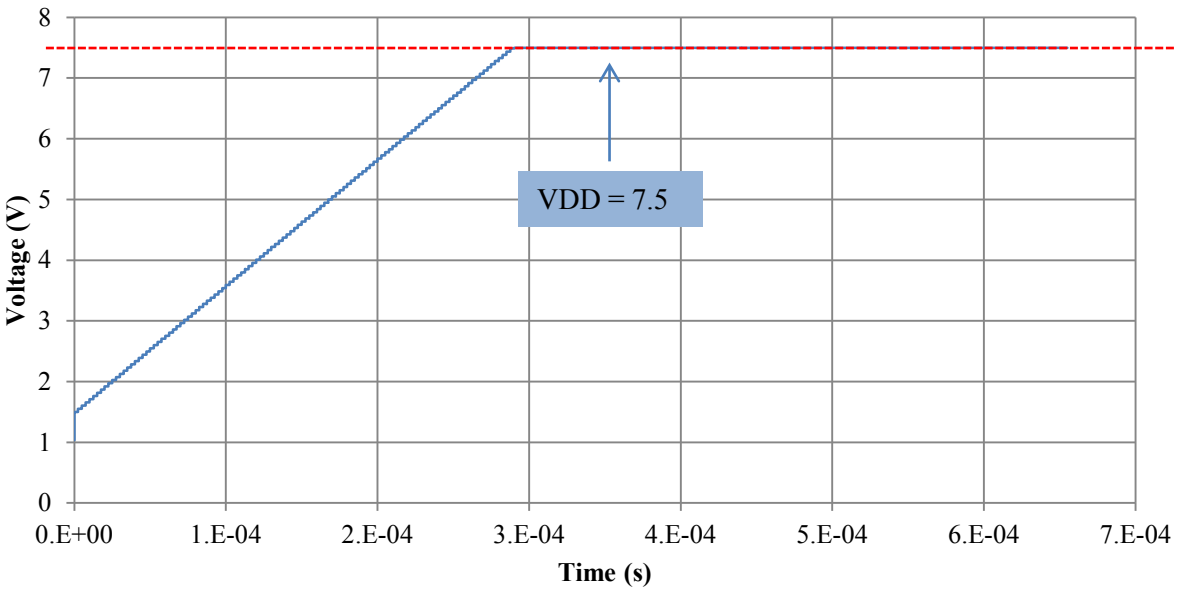


Fig. 3.14. Power supply saturation of DAC output with VDD set to 7.5 V.

3.3.1 Dead Time

The charge based approach this DAC utilizes depends heavily on the two main phases of the clock. These two phases must always have the proper amount of dead time between them in order for the DAC to perform within the specifications. The dead time generator takes advantage of feedback to fix the clock signal based on the other. Fig. 3.15 shows the model of the dead time generator.

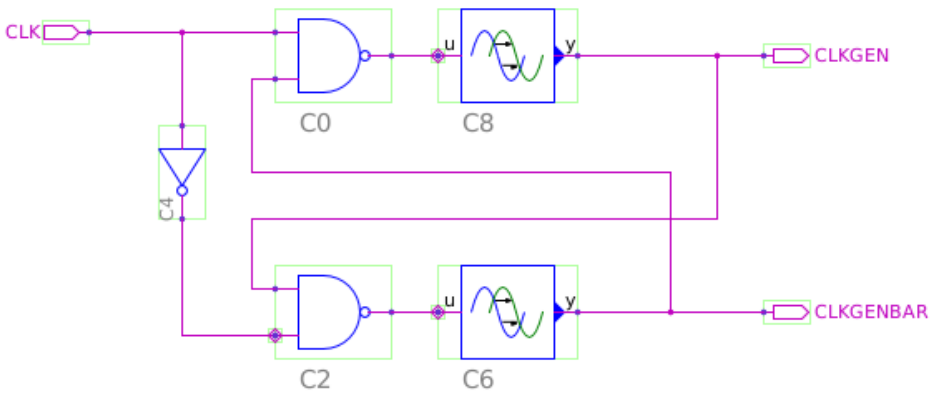


Fig. 3.15. Dead time generator model.

If the two phases of the clocks do not have dead time, the output of the DAC will short to ground momentarily thus voiding the proper analog equivalent of the digital input. Fig. 3.16 shows a waveform output of the model with no dead time.

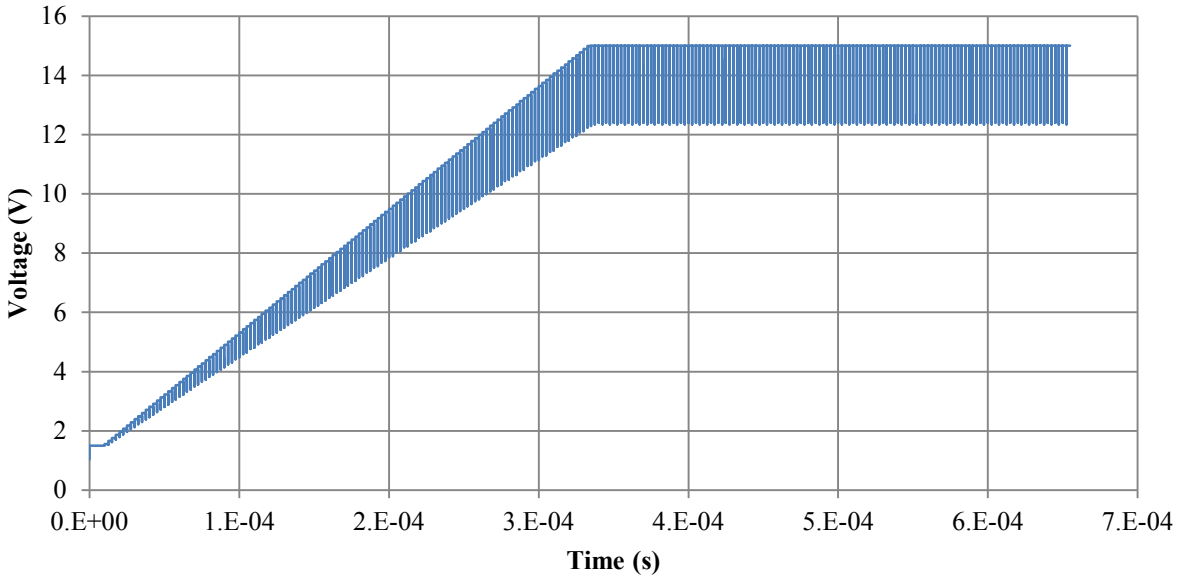


Fig. 3.16. Full scale ramp of DAC output with no dead time.

3.4 Architectural/Design

The next step in the model based design process is Architectural/Design process, highlighted in Fig. 3.17.

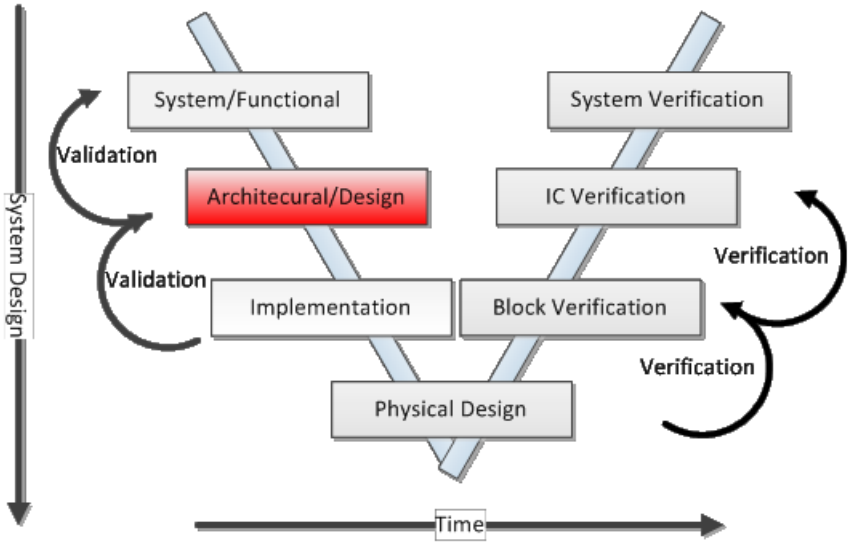


Fig. 3.17. V diagram with architectural/design highlighted.

What follows is the definition of the architecture of the DAC in both processes; XFAB and TSMC. It will be presented in parallel to show the similar yet diverse modifications to both.

3.4.1 Architecture/Design of DAC Core

The final architecture of the DAC core in the XFAB process includes the DAC_EN control input, allowing it to have the sleep mode option as required by the specifications. The schematic for the DAC core can be seen in Fig. 3.18.

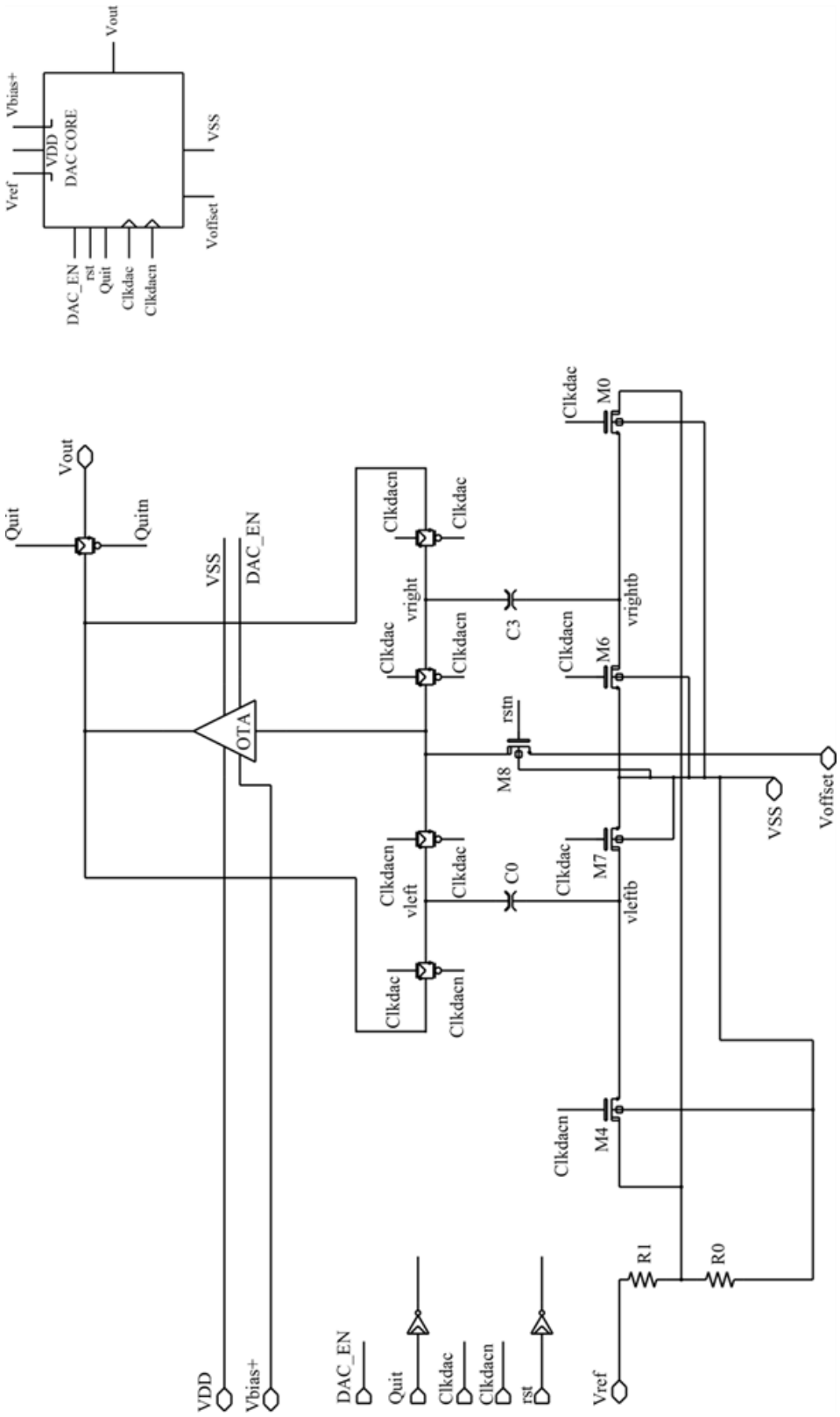


Fig. 3.18. DAC core schematic of the XFAB process.

The final architecture of the DAC core in the TSMC process has the same basic elements of the XFAB DAC. Much of the same design approach was taken from the XFAB DAC and carried into the TSMC implementation. Apart from using a different process and creating a new library of components the only major behavioral difference is the removal of the DAC enable signal. The architecture of the TSMC DAC core is shown in Fig. 3.19.

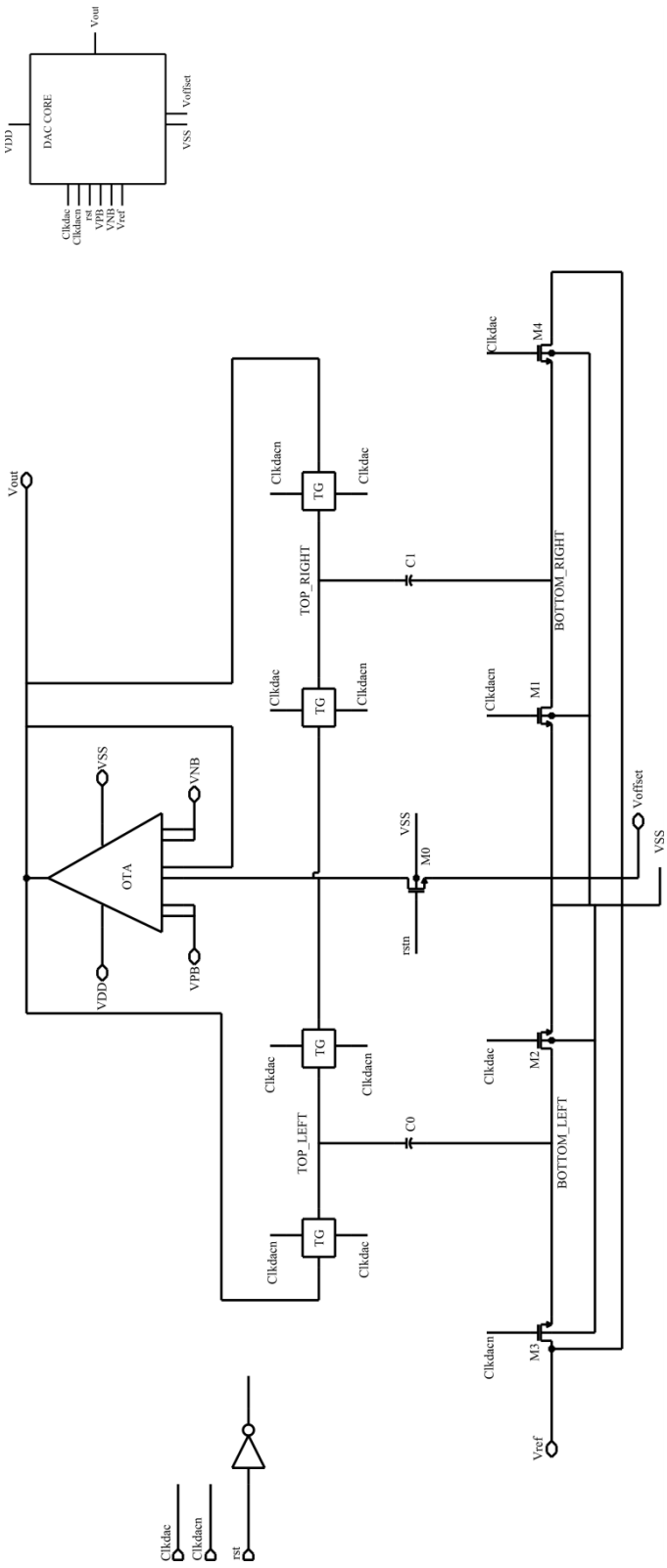


Fig. 3.19. DAC core schematic of the TSMC process.

3.5 Implementation

In the step following architectural/design, the designer now has a validated system/architectural model with detailed design and is ready for implementation. This step in the "V" diagram can be seen in Fig. 3.20.

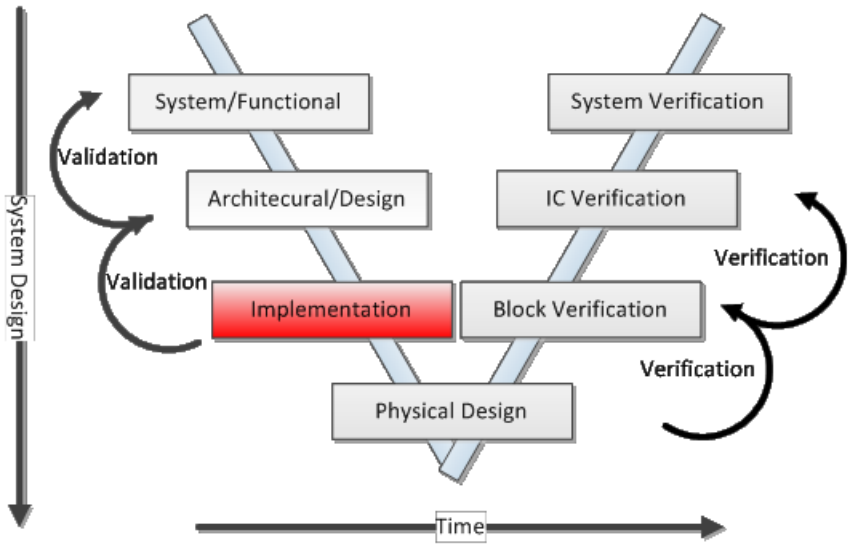


Fig. 3.20. V diagram with implementation highlighted.

The architectural specification generates a list of fundamental building blocks needed to construct the design in a process specific design kit. As in the previous sections, the circuits that follow, both digital and analog, will be introduced in parallel from both processes.

3.5.1 Digital Building Blocks

There were no high voltage digital gates in the XC06 PDK libraries provided; therefore they had to be created from scratch. These new digital cells utilize the "HV" or high-voltage MOSFETs provided by XFAB which can withstand a voltage of 0 – 45 V by utilizing a thick gate oxide. The minimum feature size for these devices is 3 µm to maintain needed current densities without damaging the device. The sizes for the digital cells were chosen to be a typical 2:1 ratio (pull up to pull down) as is commonly used for silicon digital CMOS logic [7]. The

main requirement for the digital logic was to minimize power consumption and area as conversion speed is limited by the analog core. Therefore the minimum feature size was chosen for all gates as the basis for the sizing. Table 3.1 below shows a list of the cells that were created for the DAC in the XFAB process. For the TSMC process space was less of a concern. Strength and stability of the architecture was the goal for this second pass. Table 3.2 below shows the sizes chosen for this pass. As seen, two more inverters, with more drive strength, were added to the digital library for better fan-out capability. Minimum gate length for the 5 V MOSFETs in this process is 0.5 µm. The transconductance of the PFET to NFET is roughly five times worse. This was not the case for the XFAB devices. Therefore the $\left(\frac{W}{L}\right)$ for the pull-up network are about five times that of the $\left(\frac{W}{L}\right)$ ratio for the pull-down network. As seen, the sizes are not exact; this is due to design rule constraints. The grid step size of the gates has to be multiples of the minimum feature size, 0.35 µm, of the PDK, as the TSMC 035 process is tailored for a minimum gate length of 0.35 µm. The programmable cells derive the contact location based off the 0.35 µm devices. If the gate length is not a multiple of this size, it will display an off-grid error in the design rule check. Therefore, all gate lengths where increased to the nearest multiple of 0.35 µm. The sizes for all the digital cells in both designs are displayed in Table 3.1 and Table 3.2.

TABLE 3.1. XC06 DIGITAL CELL SIZES

Cell Name	Sizes
Inverter (my_invrk)	Pull-Up = 6 µm/3 µm Pull Down =3 µm/3 µm
2 input NAND (my_nand2k)	Pull-Up = 6 µm/3 µm Pull Down =3 µm/3 µm
3 input NAND (my_nand3k)	Pull-Up = 6 µm/3 µm Pull Down =3 µm/3 µm
2 input NOR (my_nor2k)	Pull-Up = 6 µm/3 µm Pull Down =3 µm/3 µm
3 input NOR (my_nor3k)	Pull-Up = 6 µm/3 µm Pull Down =3 µm/3 µm
Transmission Gate (my_tgatek)	Pull-Up = 6µm/3 µm Pull Down =3 µm/3 µm
2 input XOR (XOR)	Combination of previous gates
D Type Flip Flop (DFF)	Combination of previous gates
T type Flip Flop (TFF)	Combination of previous gates

TABLE 3.2. TSMC DIGITAL CELL SIZES

Cell Name	Sizes
Inverter (INV)	Pull-Up = 2.8 µm/0.5 µm Pull Down =1.75 µm/0.5 µm
2 X Inverter (INV2)	Pull-Up = 2.8 µm/0.5 µm Pull Down =1.75 µm/0.5 µm Fingers = 2
4 X Inverter (INV4)	Pull-Up = 2.8 µm/0.5 µm Pull Down =1.75 µm/0.5 µm Fingers = 4
2 input NAND (NAND2)	Pull-Up = 2.8 µm/0.5 µm Pull Down =1.75 µm/0.5 µm
3 input NAND (NAND3)	Pull-Up = 2.8 µm/0.5 µm Pull Down =1.75 µm/0.5 µm
2 input NOR (NOR2)	Pull-Up = 2.8 µm/0.5 µm Pull Down =1.75 µm/0.5 µm
3 input NOR (NOR3)	Pull-Up = 2.8 µm/0.5 µm Pull Down =1.75 µm/0.5 µm
Transmission Gate (TGATE)	Pull-Up = 4.9 µm/0.5 µm Pull Down =1.05 µm/0.5 µm
2 input XOR (XOR)	Combination of previous gates
D Type Flip Flop (DFF)	Combination of previous gates
T type Flip Flop (TFF)	Combination of previous gates

Before diving into individual digital cells, it is important to show the main digital core of the system, the counter. The counter was implemented using the architecture validated with the system level model by using gates pulled from the following digital libraries. The operation of the counter is a simple one. Binary inputs from the user are driven externally onto one input of the XOR gate while the clock steps through all 128 binary combinations; the XOR gate will send a logic "1" when the right count is met. Until this event occurs, a clock pulse is passed out of the counter and into a two phase clock generator. Once the counter reaches a matched value, the clock is stopped via a D-type flip flop. This event is called a Binary Match. This indicates that the value the user desired was matched. Fig. 3.21 shows the schematic of the counter in the XFAB process. This architecture is exactly the same in the TSMC version; therefore it will not be shown twice.

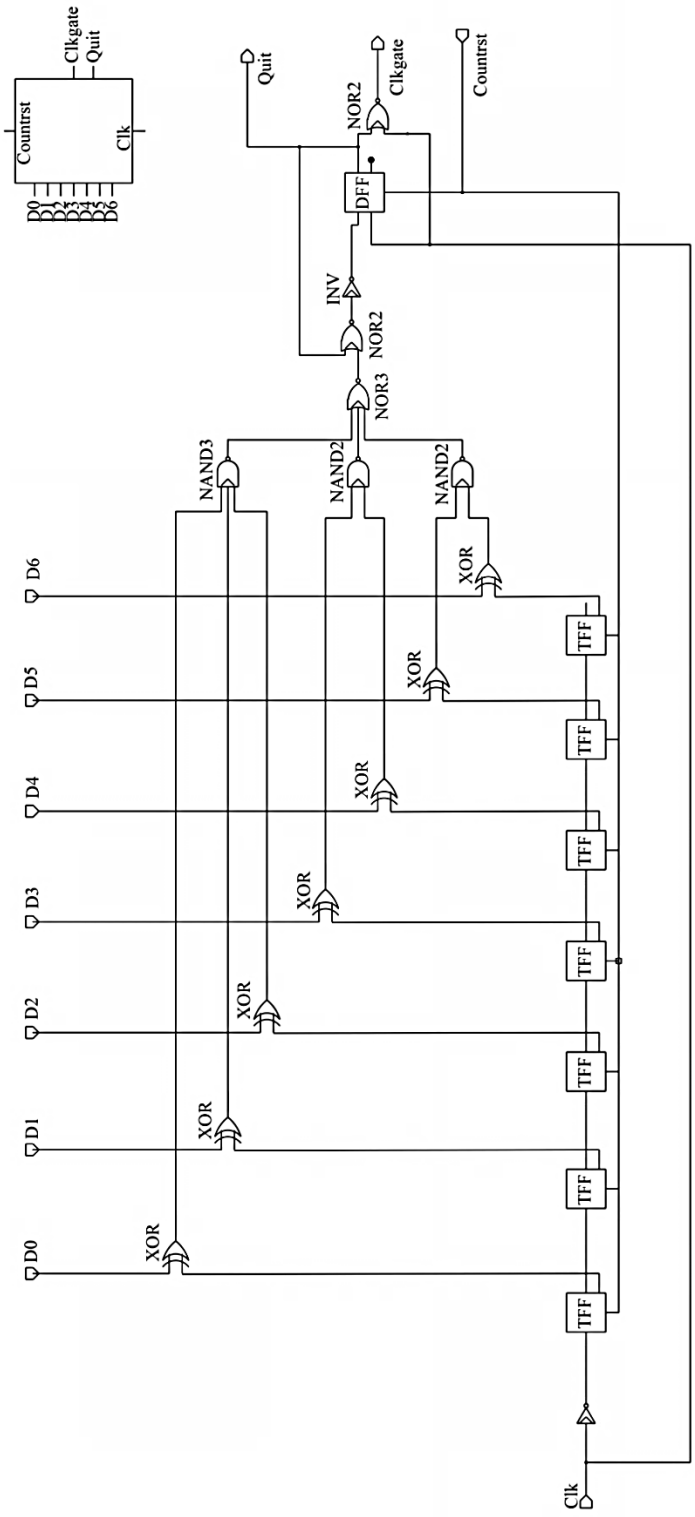
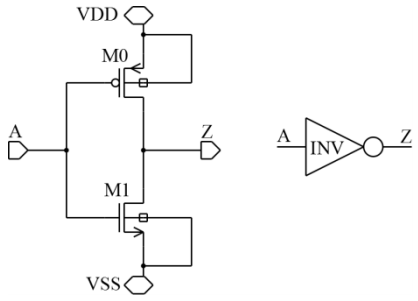
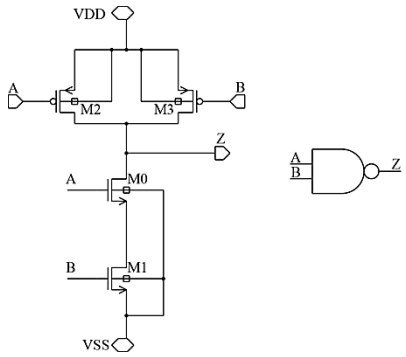


Fig. 3.21. Counter schematic for both the XFAB and TSMC processes.

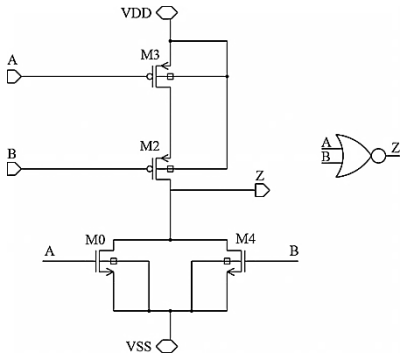
The schematics of the Inverter, NAND2 and NOR2 the digital cells are given in Fig. 3.22 for completeness.



(a)



(b)



(c)

Fig. 3.22. Digital cell schematics of both the XFAB and TSMC process.

The next structure required in this system is the XOR gate. This XOR implementation is a gate level XOR gate composed of two input NAND gates in combination (Fig. 3.23). This will provide sufficient drive strength for the counter.

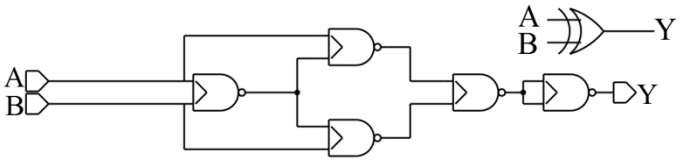


Fig. 3.23. XOR gate schematic.

The next digital blocks required are flip flops. A T-type flip flop and a D-type flip flop are both needed to complete the counter. Both of the architectures are gate level, and the T-type flip flop is built using the D-type flip flop. The D-type flip flop is constructed of only NAND gates and inverters and is resettable. The schematic is given in Fig. 3.24.

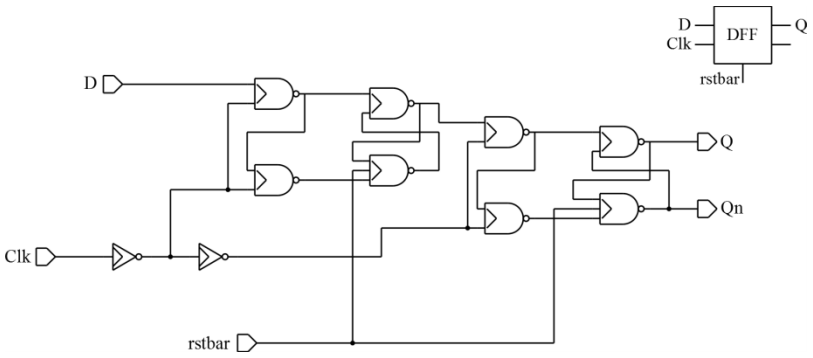


Fig. 3.24. D-type flip flop.

Speed is not critical with this design; therefore an architecture with only NAND gates and inverters offers simplicity in construction and good drive strength. The T-type flip flop is simply the D-type with feedback, therefore making it simple to construct as illustrated in Fig. 3.25.

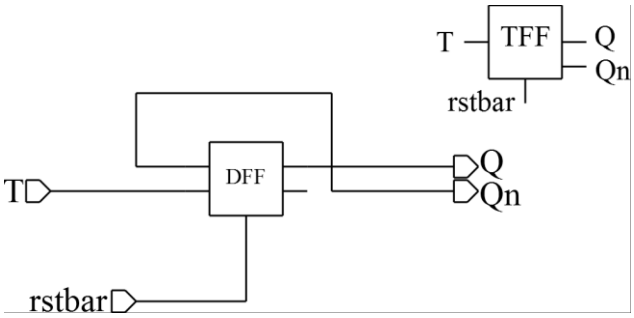


Fig. 3.25. T-type flip flop.

As previously described, during the counting process the clock output of the counter is passed through a non-overlapping clock generator that splits the one input clock signal into two non-overlapping clock signals needed to operate the two phases for the analog switching core. In the XFAB process, the non-overlapping clock generator utilizes a TFF and inverters for buffering as shown in Fig. 3.26.

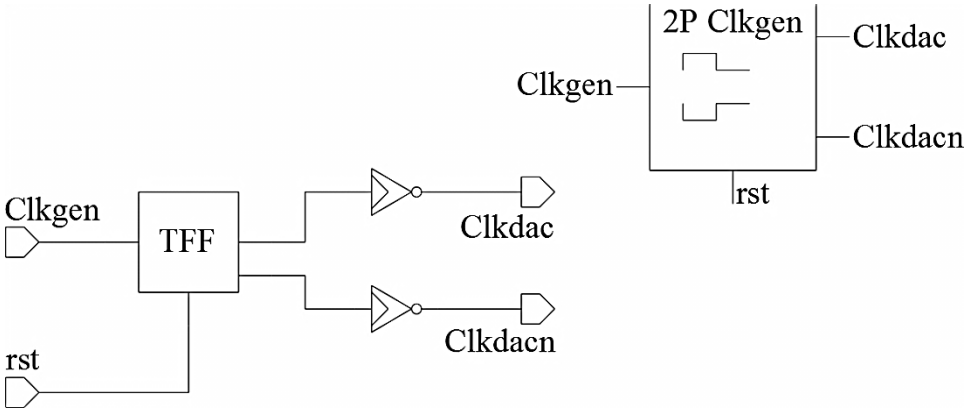


Fig. 3.26. Two phase clock generator in the XFAB process.

A different architecture for the non-overlapping clock generator was chosen for the TSMC process. This architecture is based on feedback and by design will never allow the two clock signals to overlap; the schematic can be seen in Fig. 3.27. In order to create delay, additional buffers can be added [7]. The interface between the two phase clock generator and the analog core requires more drive strength in response to the large fan-out of the switches. The two

phase clock generator outputs are each driving eight transmission gates in the analog core. Therefore, the 2X and 4X inverters that where constructed are used here. This creates a very strong, sharp signal for the transmission gates.

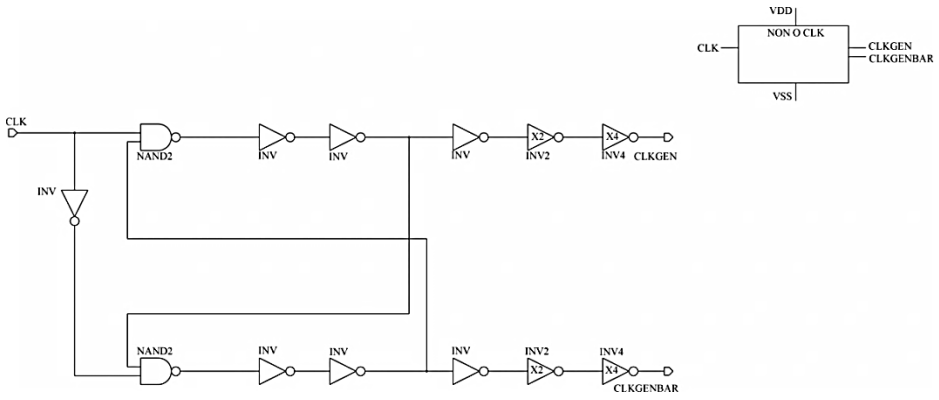


Fig. 3.27. Non overlapping clock generator schematic in the TSMC process.

3.5.2 Analog Building Blocks

Like all digital to analog converters, there is a crossover from digital to analog. What follows is the analog core design, including the detailed design of both operational amplifiers utilized in the two DAC implementations (XFAB and TSMC). Each design will be described, in full, one after the other. Referring back to Fig. 3.18, at the center of the analog core is the op-amp. Next, transmission gates control the charging of the storage capacitors for the different phases and a reset MOSFET is used to set the offset (starting value) of the DAC. Since the bottom half transmission gates in this design see only the value of V_{ref} at all times at their inputs (well below VDD in both implementations), only NFETS where used. Also, the capacitors for the charge stepping are also seen in the center. As the design of the majority of these core parts have been discussed, only the design of the op-amp remains.

3.5.3 Transmission Gates

Transmission gates are needed to direct the reference voltage during different phases of the charge pump process. Design of the transmission gates is taken from the procedure of Weste

and Harris [7]. They are critical in the overall structure of the core and how well the core will function as they strongly influence the phase change between clock cycles. Since these transmission gates will not be passing just logic values (logic "1" and "0") but a variety of voltages, an analog design procedure is appropriate. The transmission gates have two phases, both "on" or both "off" in their respective states. A CMOS transmission gate is appropriate in this case due to the need to pass values close to ground ranging towards values much higher than ground. The transmission gate can be modeled in its respective states as two resistors in parallel. The equivalent resistance, during either the "on" or "off" state, is what the designer has control over. Ideally the equivalent resistance of a CMOS gate during its "off" state is infinity, and during its "on" state is zero. However, MOSFETS do not form an ideal switch. There is a finite resistance when the transistors in the switch are on or off. R_p is the resistance of the PFET and R_n is the resistance of the NFET.

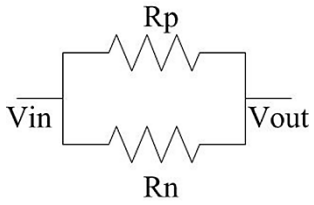


Fig. 3.28. Transmission gate model with resistors modeling the transistors.

Fig. 3.28 represents the equivalent circuit of the transmission gate either during its off or on state. The equivalent resistance of this circuit can be calculated as

$$R_{eq} = R_P || R_N \qquad [3.1]$$

This equivalent resistance does change, however, as the input voltage increases. Fig. 3.29 illustrates the relationship of the resistance based on the input voltage.

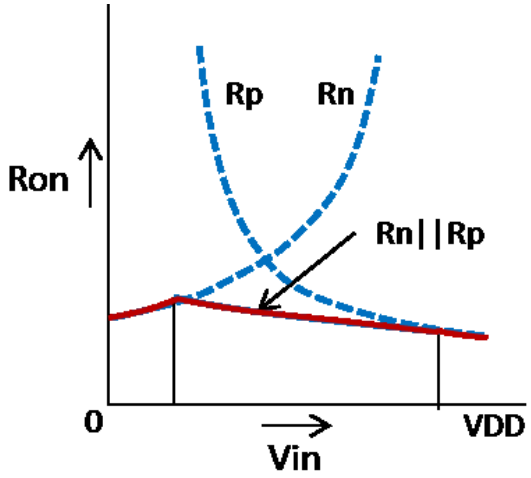


Fig. 3.29. Resistance of a transmission gate as a function of input voltage.

This equation will determine how the voltage will transfer from V_{in} to V_{out}. If, for example, the equivalent resistance of the transmission gate while off is R||4R, this has an equivalent resistance of $\frac{4}{5}R$. If the equivalent resistance of the transmission gate while on is 2R||2R then the equivalent resistance is R. Therefore, it is common practice to simply design transmission gates to be of minimum size depending on what process is chosen. Table 3.3 shows the sizes chosen in both designs. Fig. 3.30 shows the basic structure the transmission gate.

TABLE 3.3. TRANSMISSION GATE SIZES

XFAB		TSMC	
Cell Name	**Sizes**	**Cell Name**	**Sizes**
my_tgatek	P_{FET}(W/L)=3/3µm	TGATE	P_{FET}(W/L)=4.9/4.9µm
	N_{FET}(W/L)=3/3µm		N_{FET}(W/L)=1.05/1.05µm

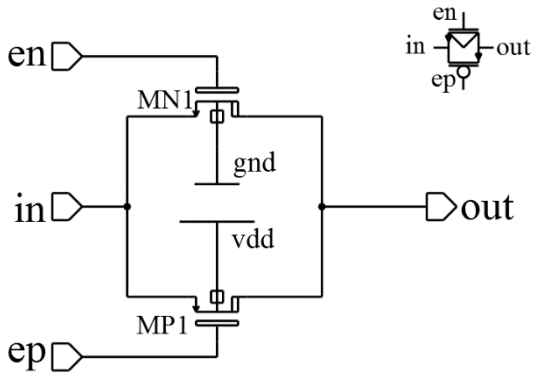


Fig. 3.30. Transmission gate schematic with transistors.

3.5.4 Operational Amplifiers

1. XFAB Op-Amp Design Procedure

The design of the XFAB op-amp will be presented first. The design procedure used is from Allen and Holberg's, *CMOS Analog Circuit Design second edition* [8]. This is a two-stage unbuffered op-amp with second stage compensation, given in Fig. 3.31 below. It is composed of seven high voltage MOSFET transistors with a minimum feature size of 3 μm. The high voltage MOSFET models are employed in the XFAB XI10 kit used in Cadence 6.1 [1]. The reason for using these particular MOSFET is due to their wide power supply capability (0-45 V) as the application for this variation of the DAC design requires a power supply range of 1.5 V to 15 V. The main constraint with this design is the power budget. The power budget is calculated based on the voltage supply. Since P=IV, the voltage is 15 V therefore current is 6 μA. This op-amp can draw no more than 6 μA to stay under the power specification of 100 μW during operation. It is also designed to drive a 1 pF capacitive load as required by the given system specification.

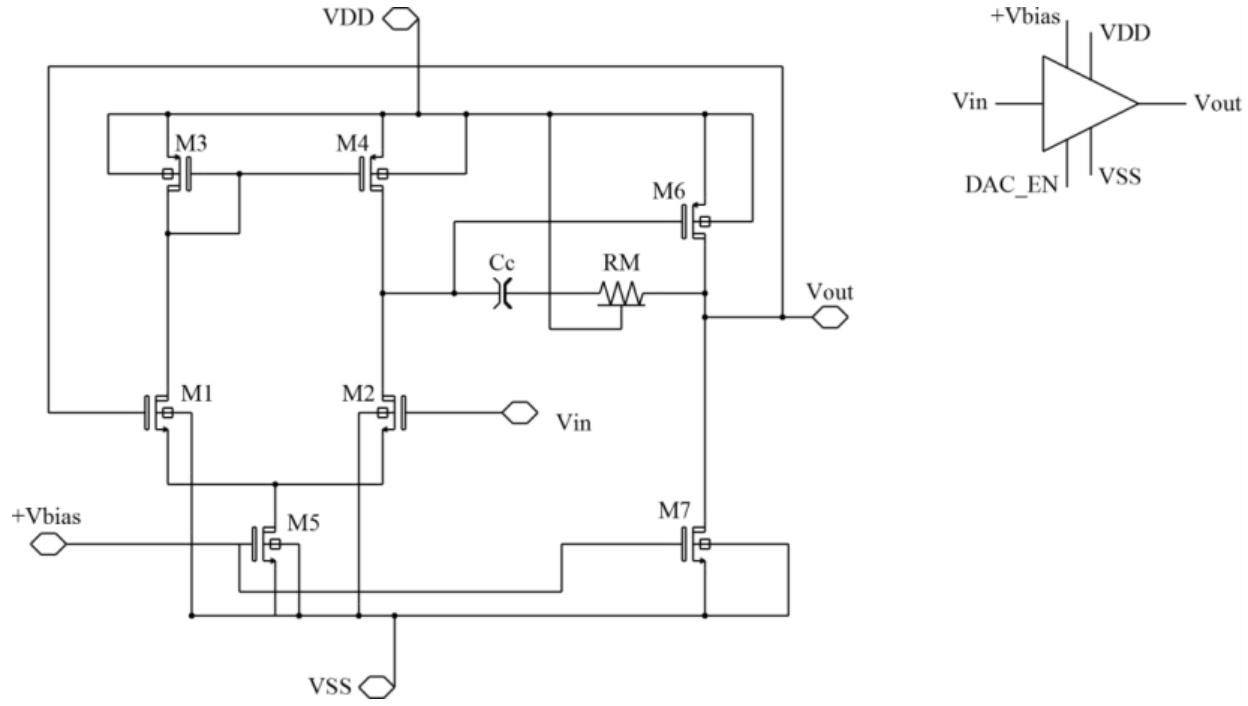


Fig. 3.31. Operational Amplifier schematic in the XFAB process.

In order to evaluate the sizes for this unbuffered op-amp, specifications for its use and parameters from the devices must be defined. The design procedure is specifically tailored to be based off of these parameters. Table 3.4 shows the measured parameters of the high voltage PFET and NFET from the XFAB 0.6 µm process using a parameter extraction recipe [9].

TABLE 3.4. XFAB XI10 DEVICE PARAMETERS

K'_N	16.01 uA/V
K'_P	9.375 uA/V
V_{TN}	0.95 V
V_{TP}	-0.98 V

This op-amp is used in a unity gain, closed loop configuration as demonstrated in Fig. 3.32. This is desired due to its voltage following ability. Table 3.5 shows the specifications based on operation.

TABLE 3.5. SPECIFICATIONS FOR DESIGN

A_V	70 dB
A_{OV}	0 dB
GB	50 MHz
ICMR	1.5 to 15 V
C_L	1 pF
SR	>10 V/µs
P_{DISS}	≤100 µW

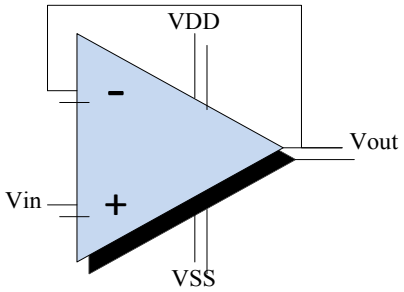


Fig. 3.32. Unity gain configuration of the op-amp utilized in the DAC core.

The design procedure starts by calculating the required compensation capacitance.

$$C_C > \left(\frac{2.2}{10}\right) C_L \qquad [3.2]$$

This equation will give a phase margin of approximately 60°. This is due to the ratio of $\left(\frac{2.2}{10}\right)$; in other words, the compensation capacitance must be at least 22% more than the load capacitance for a desired phase margin of 60°. Since the load capacitance is 1 pF, then C_C was chosen to be 0.25 pF. Next, the size of device M3, which is equal to device M4, can now be evaluated:

$$S_3 = \left(\frac{W}{L}\right)_3 = \frac{I_5}{K'_3[V_{DD} - V_{in(\max)} - |V_{T3(\max)}| + V_{T1(\min)}]^2} \qquad [3.3]$$

$$S_3 = \left(\frac{W}{L}\right)_3 = \frac{2(1.25uA)}{(9.3.75u)[2.0V - 1.5V - |-1.05V| + 0.67V]^2} = 18.5$$

The transconductance (gm) of device M1 is now calculated and applied to equation [3.5] to find the size of devices M1 and M2.

$$gm_1 = GB(C_C) \quad [3.4]$$

$$gm_1 = 50\ M(0.25\ p) = 12.5\ \mu S$$

$$S_1 = S_2 = \left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{2K'_N I_1} \quad [3.5]$$

$$S_1 = S_2 = \left(\frac{W}{L}\right)_1 = \frac{12.5\ u}{2(16.01\ u)(1.25\ u)} = 4.06$$

Next, the size of device M5 is calculated. This calculation is dominated by the amount of tail current or current through device M5.

$$S_5 = \frac{2I_5}{K'_5[V_{DS5(sat)}]^2} \quad [3.6]$$

$$S_5 = \left(\frac{W}{L}\right)_5 = \frac{2(2.5\ u)}{(16.01\ u)[.33\ V]^2} = 3.0$$

After calculating the size of device M5, the bias voltage for that device (the voltage bias for the op-amp) is chosen to be 1.2 V. After this has been evaluated the size of device M6 can be calculated. This expression uses a transconductance relationship of device M4 for sizing:

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} \quad [3.7]$$

$$S_6 = \left(\frac{W}{L}\right)_6 = 18.5 \frac{110\ u}{20.8\ u} = 98$$

This value is much larger than desired, so another approach was adopted at this point. Since the main focus is the power budget the use of current references is another way of sizing devices. The total current to be used is 6 µA. Since 2.5 µA is already being used at device M5, the current through device M6 can be no larger than 3 µA to be comfortably under the power budget. Now that the current through device M6 is known, a relationship can be used to size this device.

$$\frac{I_4}{I_6} = \frac{S_4}{S_6} \quad [3.8]$$

This leads to a new sizing for device M6 of:

$$S_6 = (\frac{W}{L})_6 = 45$$

This same current relationship was used to calculate the size of device M7.

$$S_7 = \left(\frac{W}{L}\right)_7 = \left(\frac{I_6}{I_5}\right) S_5 \quad [3.9]$$

$$S_7 = \left(\frac{W}{L}\right)_7 = \left(\frac{3\ u}{2.5\ u}\right) 3 = 3.5$$

The design procedure for the output devices M6 and M7 are focused towards a ratio of the tail current device M5. With the power budget in mind, the bias current for these devices is not typical for an output stage. This will result in some systematic offset due to lower gain. ack capacitance and resistance. The nulling resistor is put in series with C_C and sized to be placed above the highest non-dominant pole.

Table 3.6 lists the sizes and currents of all the gates as well as the feedback capacitance and resistance. The nulling resistor is put in series with C_C and sized to be placed above the highest non-dominant pole.

TABLE 3.6. SIZES XFAB OPERATIONAL AMPLIFIER

Device	$(\frac{\mathbf{W}}{\mathbf{L}})$	I
M1	4.06 = 12.18 µ/3 µ	.75 µA
M2	4.06 = 12.18 µ/3 µ	.75 µA
M3	3 = 9 µ/3 µ	.75 µA
M4	3 = 9 µ/3 µ	.75 µA
M5	1 = 3 µ/3 µ	1.5 µA
M6	15 = 45 µ/3 µ	1.6 µA
M7	1.06 = 3.18 µ/3 µ	1.6 µA
Cc	.68 pF	N/A
Rc	70 kΩ	N/A

2. TSMC Operational Amplifier Design

The operational amplifier topology chosen for the TSMC design variation is an NFET input folded-cascode op-amp. Traditionally op-amps use a voltage to current and current to voltage transition between stages. This op-amp uses a current to current relationship from the input stage to the output stage. The output is still a voltage output making it an operational amplifier. The schematic can be seen in Fig. 3.33.

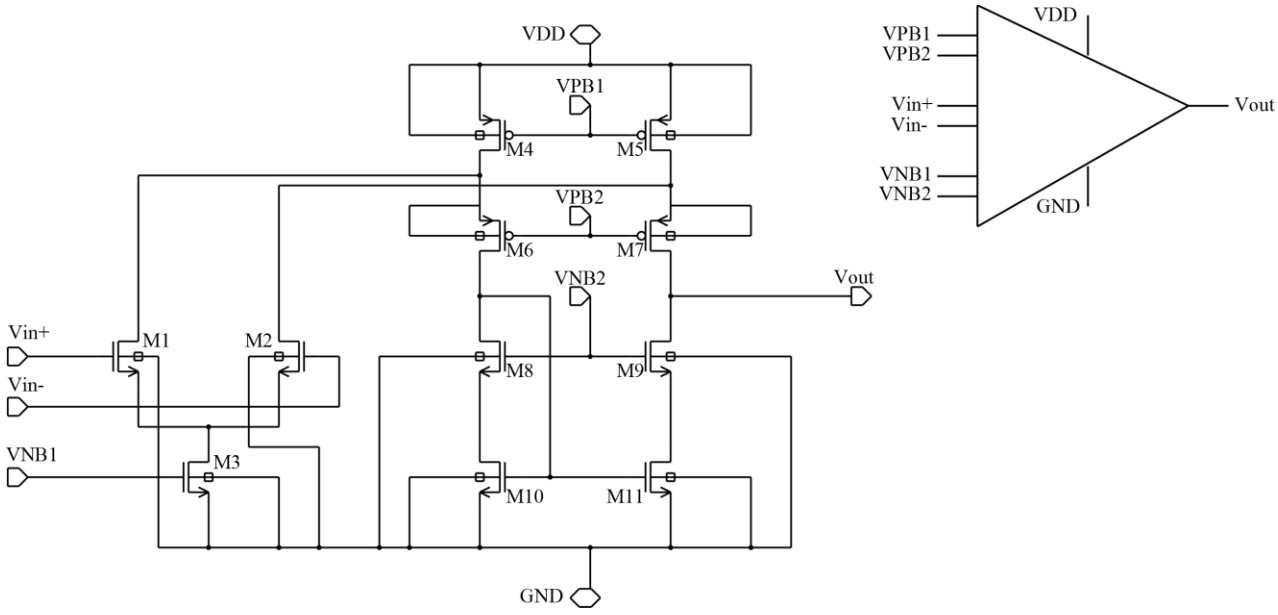


Fig. 3.33. Folded cascode operational amplifier schematic used in the TSMC process.

The design procedure for this folded cascode op-amp is unique. The need for a general purpose op-amp across two applications drove the specifications and sizes. One application was for the DAC and the other for a series of active filters designed by the Electronics II Laboratory Spring 2012 at the University of Arkansas. Instead of designing two different op-amps, one general purpose op-amp was designed to meet the required performance for both applications. The DAC will need to drive a 10 pF active probe tip within a 200 kHz clock cycle. This

parameter will set the slew rate. The electronics lab requires an op-amp with a minimum low pass filter band-width of 2 MHz and gain of 50 dB for filter use.

The design procedure that follows is an adaptation to the design procedure outlined in Allen and Holberg [8]. For the TSMC design, the supply range is 5 V. It is important to note that there are not as many constraints with this op-amp design as there were in the first pass with the XFAB process. This is due in part by second pass validation, different supply range, and the need for compatibility with both applications. This op-amp is also be used in a unity gain, voltage follower configuration for the DAC. Since the transition from stage one to stage two is a current-current relationship, Miller feedback compensation is not needed. To support this claim the small-signal model is presented in Fig. 3.34.

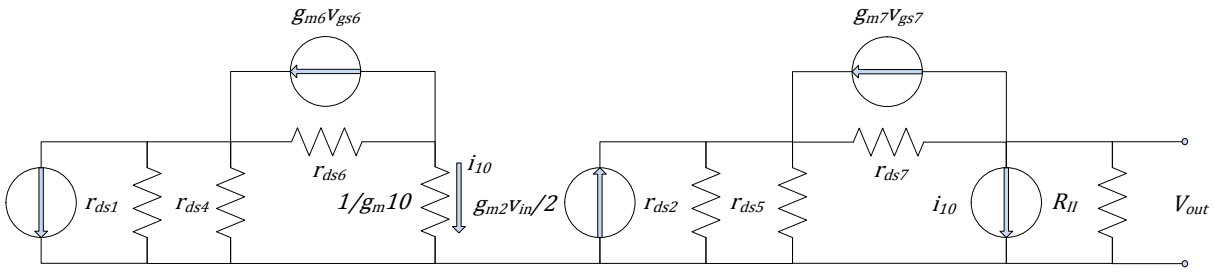


Fig. 3.34. Folded cascode small-signal model.

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Table 3.7 lists the measured parameters extracted from the models provided by the TSMC PDK.

TABLE 3.7. TSMC DEVICE PARAMETERS

K'_N	80 uA/V
K'_P	22.9 uA/V
V_{TN}	0.8 V

V_{TP}	-1.00 V

The folded cascode op-amp, by its topology, provides several desirable features, including good input common mode range and self-compensation. The input common mode range is a result of separately biasing the gates of the current mirrors in the second stage. This allows the drop from VDD to be much lower. Self-compensation is a result of current balancing provided by the cascoded current mirrors. In order to properly bias each transistor in saturation the bias currents for each transistor must be carefully evaluated.

The current through device M3 must be evaluated first. This current (I3) is derived from the desired slew rate during operation. The slew rate is in turn derived from the target operating frequency of the DAC. Inheriting the specifications from the previous design this op-amp will be operating with a 200 kHz clock signal.

$$SR_{200\,kHz} = \frac{5\,V}{5\,\mu s} = \frac{1\,V}{1\,\mu s} \qquad [3.10]$$

In order to drive a realistic outside load (i.e. scope probe) a high load capacitance in conjunction with a high slew rate is desired; this is the main design constraint for the DAC application. In order to tailor the op-amp for the electronics lab, the need for a minimum gain bandwidth is introduced. design constraints.

Table 3.8 lists the combined design constraints.

TABLE 3.8. OP-AMP SPECIFICATIONS

SR	20 V/µs
C_L	50 pF
GB	8 MHz

First, bias current I3 is calculated from SR and C_L.

$$I_3 = SR * C_L \quad [3.11]$$

$$I_3 = 20E6 * 50E - 12 = 1\ mA$$

Once I3 is evaluated the currents I4 and I5 can be set at slightly more than half of current I3. This is due to the need to have excess current flowing to devices M6 through M11 to account for enough current in all branches to maintain biasing. The currents I4 and I5 are thus calculated as:

$$I_4 = I_5 = (I_3/2) * 1.10 \quad [3.12]$$

$$I_4 = I_5 = \left(\frac{1\ mA}{2}\right) * 1.10 = 550\ \mu A$$

Now that the bias current is known for devices M4 and M5, their sizes can also be calculated. Before they are calculated, it is important to evaluate the total drop across both M5 and M7. At this step in the design procedure, the total drop across M5 and M7 are considered based on the case in which all of the current will be concentrated through one side of the output stage. As the DAC application of the op-amp will be configured for voltage following, the negative node will always be tied to the output, VOUT. Therefore, this op-amp design is for current balance use, leading to half of the current requirement through the devices M5 and M7. This is desirable for power savings as well. In order to guarantee that devices M5 and M7 stay in saturation the total voltage drop is designed for the addition of the drain to source voltage in the saturation region of both devices.

$$Total\ Vdrop\ Across\ M5\ \&\ M7 = VDD - V_{OUT(MAX)} \quad [3.13]$$

$$Total\ Vdrop\ Across\ M5\ \&\ M7 = 5\ V - 2.5\ V = 2.5\ V$$

Both devices will share this drop. This is a problem however because the DAC application needs to be able to drive the output voltage close to supply. The minimum V_{DS} for M5 can utilize 1.0 V of that 2.5 V range, leaving 1.5 V for device M7. This is good based on the fact that the devices M6 and M7 must always stay in saturation. If the devices M4 and M5 start falling into the triode region, a bias current will still be produced, which is the only important function for these devices; the model of the folded cascode op-amp demonstrates this fact and can be seen in Fig. 3.35.

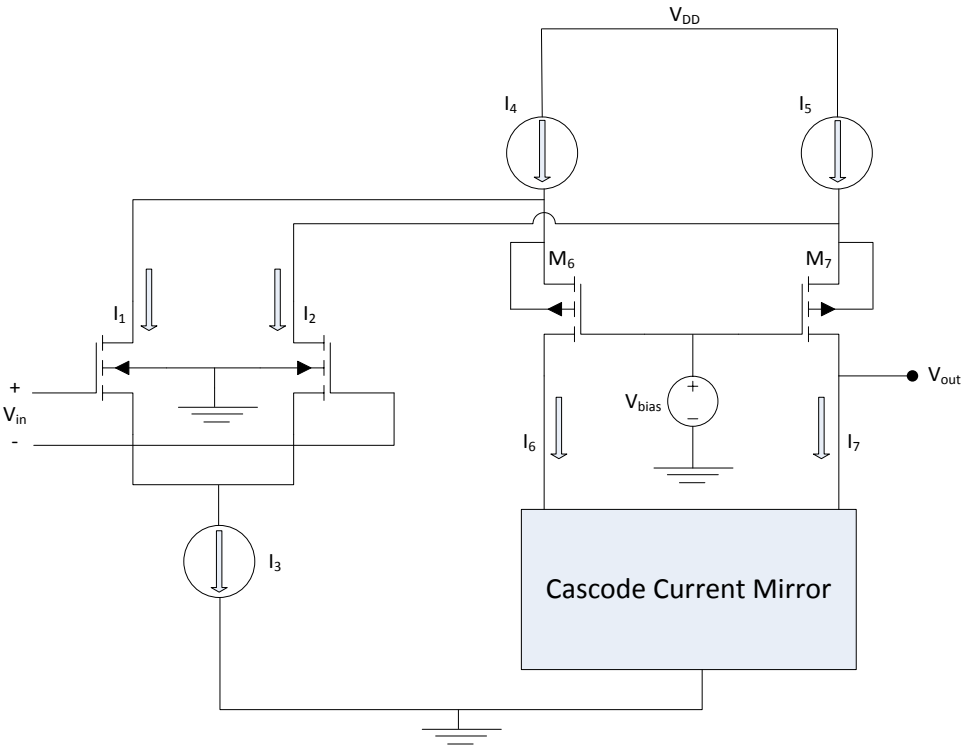


Fig. 3.35. Folded cascode op-amp model.

In fact, to increase $V_{OUT}(max)$ the devices M4 and M5 could be put into the triode region. If the drop across M5 is 1.0 V this will also help determine what the gate voltage needs to be, or in other words V_{PB1}.

$$V_{SD(SAT)} = V_{SG} - |-V_{TP}| \quad [3.14]$$

Solving for the gate voltage results in the bias voltage.

$$V_{SG} = V_{SD(SAT)} + |-V_{TP}| \quad [3.15]$$

$$V_{SG} = 1.0\,V + 1.0\,V = 2.0\,V$$

This will result in a 2.0 V drop from VDD which makes V_{PB1} = 3.0 V. Knowing the drain, gate, and source node voltages, the sizes for M4 and M5 can be calculated.

$$S_4 = S_5 = \frac{2*I_5}{K'_p*V_{SD5}^2} \quad [3.16]$$

$$S_4 = S_5 = \frac{2*550\ \mu A}{20\ \mu*1^2} = 55 \cong 60$$

Next, the sizes of devices M6 and M7 are needed. In order to predict the appropriate size of M6 and M7 it is important to observe the behavior of each source node. As previously mentioned, anticipation of devices M4 and M5 slipping into the triode region during operation is an important consideration to the sizing of devices M6 and M7. Calculating the worst case for each source node is thus necessary. The equation for the devices in the triode region will more accurately solve for V_{SD} across devices M4 and M5.

$$I_5 = K'_P(S_5)\left\{(V_{SG} - V_{TP}) - \left(\frac{V_{DS}}{2}\right)\right\}V_{SD} \quad [3.17]$$

$$550\mu A = 20\ \mu(60)\left\{(2\,V - 1\,V) - (\frac{V_{DS}}{2})\right\}V_{SD} \quad [3.18]$$

Solving for V_{DS}:

$$V_{DS} = 0.711\,V$$

The only node that is not known in order to calculate the size of the devices M6 and M7 is the value at their gates. For simplicity, the voltage reference used for VPB1 of 3.0 V will be used on the gates of these devices as well. This gives the final variable needed to calculate the sizes of

M6 and M7. The current flowing through these devices is the 10% of the total current that was designed earlier.

$$I_6 = I_7 = I_5 - (I_3/2) \quad [3.19]$$

$$I_6 = I_7 = 550\ \mu A - \left(\frac{1\ mA}{2}\right) = 50\ \mu A$$

Now that the current going through the devices M6 and M7 are known, the sizes can be evaluated.

$$S_6 = S_7 = \frac{2*I_6}{K_p'*V_{SD5}^2} \quad [3.20]$$

$$S_6 = S_7 = \frac{2*50\ \mu A}{20\ \mu*(4.3-3.0-1.0)^2} = 55.5 \cong 60$$

Since the ratios for devices M4 – M7 are very similar, making all *W/L* ratios equal to 60 is preferable for layout simplicity.

Next evaluation for the NFET cascode current mirror on the bottom half of the second stage is evaluated. As in the design of the top two devices M5 and M6, it is important to make sure the drop across devices M9 and M11 are large enough to keep them in saturation. The drop across these devices is evaluated from $V_{OUT}(min)$ and VSS.

$$Total\ Vdrop\ Across\ M9\ \&\ M11 = V_{OUT(MIN)} - VSS \quad [3.21]$$

$$Total\ Vdrop\ Across\ M9\ \&\ M11 = 2.5\ V - 0 = 2.5\ V$$

In order to make sure device M9 stays in saturation 2/3 of this drop will be dedicated to it. This will make the drop across M9 1.5 V; leaving 1.0 V for M11. Much like before, in order to increase the voltage at V_{OUT} of the DAC, the devices M10 and M11 will be pushed to the edge of saturation. This will make the drop across its drain to source 0.8 V instead of 1.0 V. In order to alleviate the need to multiple voltage reference in this design, the bias point for V_{NB2} is set to be a 2.0 V voltage difference, mirroring the values used for the top PFET devices. At this point it is

important to note that this is not a twin well process. This means that any NFET cascoded devices will have a body effect as they body cannot be biased independently from the common substrate value of V_{SS} (0 V). This body effect plays a role in sizing of devices M8 and M9. The body effect will increase the effective voltage threshold of the devices. In order to find the proper voltage threshold, device analysis is performed in simulation on an NFET with a source voltage of 0.8 V and a body voltage of 0.0 V. The result of this analysis is that the voltage threshold for these NFET devices moves from 0.8 V to 1.075 V. With the proper threshold is the sizes of devices M8 and M9 (as well as the mirrored devices M10 and M11) can be evaluated. As

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2*I_9}{K_N^{\prime}*V_{DS9}^2} \quad [3.22]$$

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2*50\ \mu A}{80\ \mu*(2-0.8-1.075)^2} = 80$$

Now that all the output devices have been sized, the sizes for the remaining devices M1, M2 and M3 can be determined. M1 and M2 are sized based on the desired bandwidth of the op-amp. The equation that dominates those sizes is based on the transconductance of devices M1 and M2.

$$S_1 = S_2 = \frac{GB^2 C_L^2}{K_N{}' I_3} \quad [3.23]$$

$$S_1 = S_2 = \frac{(8\ MHz*2\pi)^2 (50\ pF)^2}{(80\ \mu)(1.099\ mA)} = 71.84 \cong 75$$

The next step is to size the device M3. The size of this device will depend on the minimum input voltage that the op-amp will receive.

$$S_3 = \frac{2I_3}{K_N{}'\left(V_{IN}(\min) - V_{SS} - \sqrt{\frac{I_3}{K_N{}'*S_1}} - V_{T1}\right)^2} \quad [3.24]$$

$$S_3 = \frac{2*1.099\ mA}{80\ \mu\left(2.5-0-\sqrt{\frac{1.099\ mA}{80\ \mu*74.7}}-0.8\right)^2} = 17 \cong 20$$

Now that the sizes of all the devices have been evaluated, the small-signal voltage gain is observed. Before that equation can be used several small-signal model parameters must be

calculated first. The equations that are evaluated from the small-signal model are output resistance (R_{out}), Gain ($\frac{v_{out}}{v_{in}}$), the output pole (P_{out}), and gain bandwidth (GB).

To evaluate R_{out} the small-signal model parameters must be used to calculate the small-signal conductance of each device g_m and g_{ds}..

$$g_m = \sqrt{2K' I_D \frac{W}{L}} \quad [3.25]$$

$$g_{ds} = \lambda I_D \quad [3.26]$$

These equations give the conductances in the saturation region. For devices M4 and M5 g_{ds} in the triode region must be determined.

$$g_{ds} = \beta(V_{GS} - V_T - V_{DS}) \quad [3.27].$$

Table 3.9 lists all the necessary values needed for calculation.

TABLE 3.9. SMALL-SIGNAL CONDUCTANCE VALUES

Device	gds	gm
M4,M5 (Triode)	240 µS	Not Needed
M6,M7	328 µS	2.7 µS
M8,M9,M10,M11	760 µS	1.8 µS
M1,M2	2564 µS	23.8 µS

Now that all the necessary values for the small-signal analysis are known, Rout can be evaluated.

$$R_{out} \approx (g_{m9} r_{ds9} r_{ds11}) || [g_{m7} r_{ds7} (r_{ds2} || r_{ds5})] \quad [3.28]$$

$$R_{out} \approx \left(760\,\mu \left(\frac{1}{1.8}\mu\right)\left(\frac{1}{1.8}\mu\right)\right) || \left[328\,\mu \left(\frac{1}{2.7}\,\mu\right)\left(\frac{1}{23.8}\mu \,\middle|\middle|\, \frac{1}{240}\,\mu\right)\right] = 0.45\ M\Omega$$

Rout is then used to evaluate the gain.

$$\frac{v_{out}}{v_{in}} = \left(\frac{2+k}{2+2k}\right) g_{ml} R_{out} \quad [3.29]$$

The equation for the gain has a unique constant called *k*. This constant *k* is called the low-frequency unbalance factor, and it is defined as:

$$k = \frac{R_9(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}} \quad [3.30]$$

The only remaining variable needed to evaluate this equation is R_9. R_9 is the effective small-signal resistance of device M9. It dominates the resistance seen by device M7 and is lumped with device M11 as seen in the equation Eq. [3.31].

$$R_9 \approx g_{m9}r_{ds9}r_{ds11} \quad [3.31]$$

$$R_9 \approx 760\ \mu\left(\frac{1}{1.8}\ \mu\right)\left(\frac{1}{1.8}\ \mu\right) = 234.56\ M\Omega$$

Using Eqs. [3.30] and [3.19], the gain is calculated as:

$$k = \frac{234.56\ M(23.8\ \mu+240\ \mu)}{328\ \mu\left(\frac{1}{2.7}\mu\right)} = 509.35$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{2+509.35}{2+2*509.35}\right)(2564\ \mu)(0.45\ M) = 578.03\ \frac{V}{V} = 55.23\ dB$$

To determine where the gain will begin to roll off we must calculate the first dominate pole, P_{out}.

$$P_{OUT} = \frac{-1}{R_{OUT}C_L} \quad [3.32]$$

$$P_{OUT} = \frac{-1}{(0.45\ M)(50\ p)} = 44{,}444\frac{rads}{s} = 7.07\ kHz$$

Knowing the first dominant pole and the gain, the gain bandwidth can be evaluated.

$$GB = \left(\frac{v_{out}}{v_{in}}\right)(P_{OUT}) \quad [3.33]$$

$$GB = (578.03)(44{,}444.00) = 25.69\ \frac{Mrads}{s} = 4.08\ MHz$$

As seen the gain bandwidth is less than desired but it is still well over the bandwidth needed. ration before layout can begin.

Table 3.10 shows the sizes of all the devices. At this point in the design, simulations are run in order to verify correct operation before layout can begin.

TABLE 3.10. DEVICE SIZES OP-AMP TSMC

Device	$(\frac{W}{L})$	I
M1,M2	149.92 µm/2 µm	1.00 mA
M3	40 µm/2 µm	1.00 mA
M4,M5,M6,M7	60 µm/1 µm	500 µA
M8,M9,M10,M11	80.4 µm/1 µm	50 µA

CHAPTER 4 – SIMULATION

Once the architecture/design has been completed, the next progression in the "V" diagram is to validate the schematic before physical implementation can begin as seen in Fig. 4.1. Chapter 4 illustrates the validation of the major blocks and integrated DAC design using circuit simulation. Simulations from both designs (XFAB and TSMC) are presented in parallel. Both will encompass digital validation, analog validation, and system (DAC) validation.

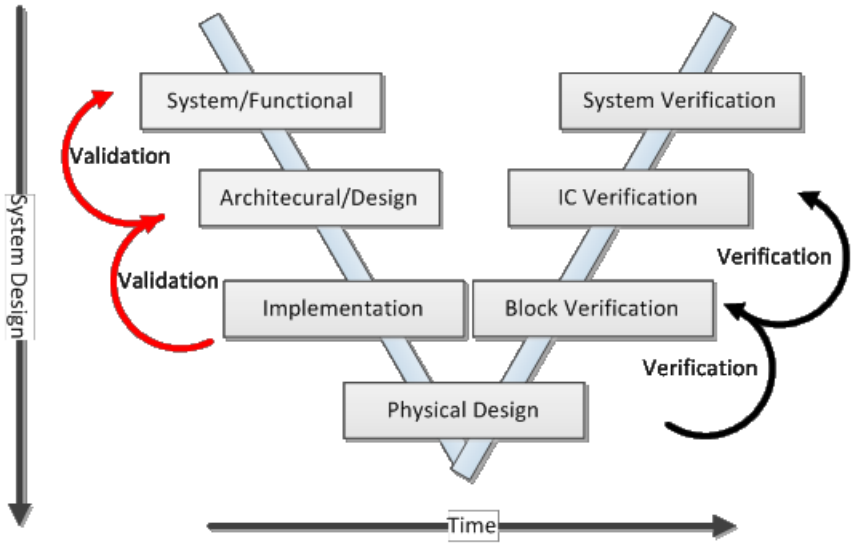


Fig. 4.1. V diagram with validation of schematic design highlighted.

4.1 Tool Flow

Designing both the TSMC and XFAB DAC's required the use of different tools. Described is the tool flow for both runs starting from the top (model) to the physical design where it applies. The model of the DAC system was constructed in ModLyng [10]. Next, the library of building blocks was captured in Cadence Virtuoso IC6 for the XFAB version [11]. The TSMC version was captured in Cadence Virtuoso 5.1 [12]. Simulation of both versions was performed in Spectre [13]. Once the schematic was validated layout of the library of building blocks for the TSMC version was performed in Cadence Virtuoso 5.1. Upon completion of the

layout DRC, LVS and PEX was performed in Calibre Interactive v2009.2_36.21 [14]. Fig. 4.2 illustrates the tool flow mentioned.

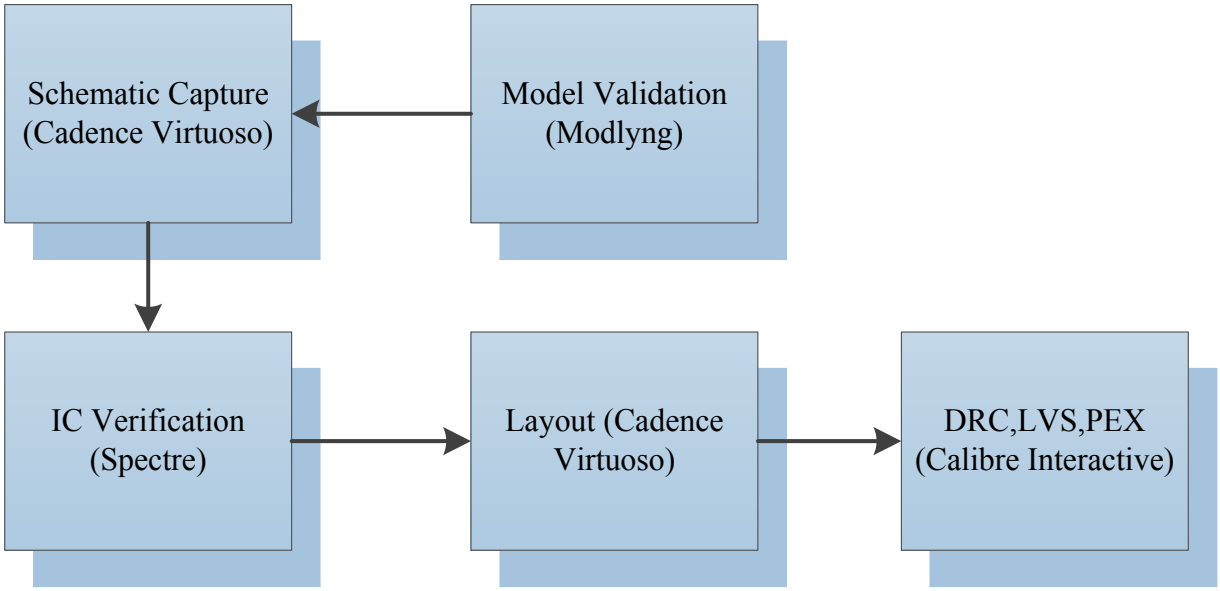


Fig. 4.2. Tool Flow

4.2 Digital Simulations

Digital simulation validation was performed on the basic digital building blocks of the DAC including the digital gates, digital counter, and clock generator. The simulation of the digital gates begins with the NAND gate.

4.2.1 Digital Gates

The digital gate test bench is designed to test the gate in the time domain. Two in-phase clock signals are used to drive each input and the change at the output observed. A 200 kHz clock signal was used with a 1 pF load capacitance to emulate the largest fan-out any gate is expected to encounter. The test bench can be seen in Fig. 4.3.

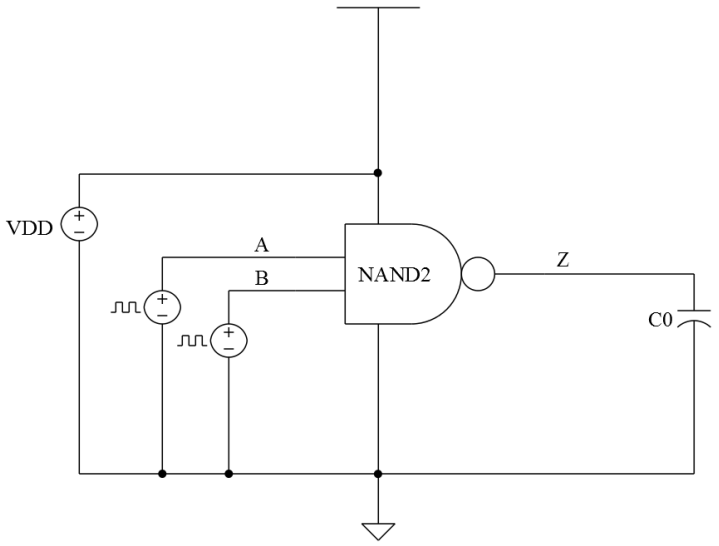


Fig. 4.3. NAND2 test bench schematic.

The output of this test bench can be seen below in Fig. 4.4. This simulation shows the clock signals at both inputs propagating through the NAND gate and asserting the correct output at node Z. Table 4.1 displays the rise and fall times for both the XFAB and TSMC Boolean gates. These results are well within the requirements for asserting the proper logic signal within the 200 kHz clock input.

Table 4.1. Rise and Fall Times for Boolean Gates

Rise/Fall	XFAB	TSMC
Rise Time	12.5 ns	4.9 ns
Fall Time	29.1 ns	9.1 ns

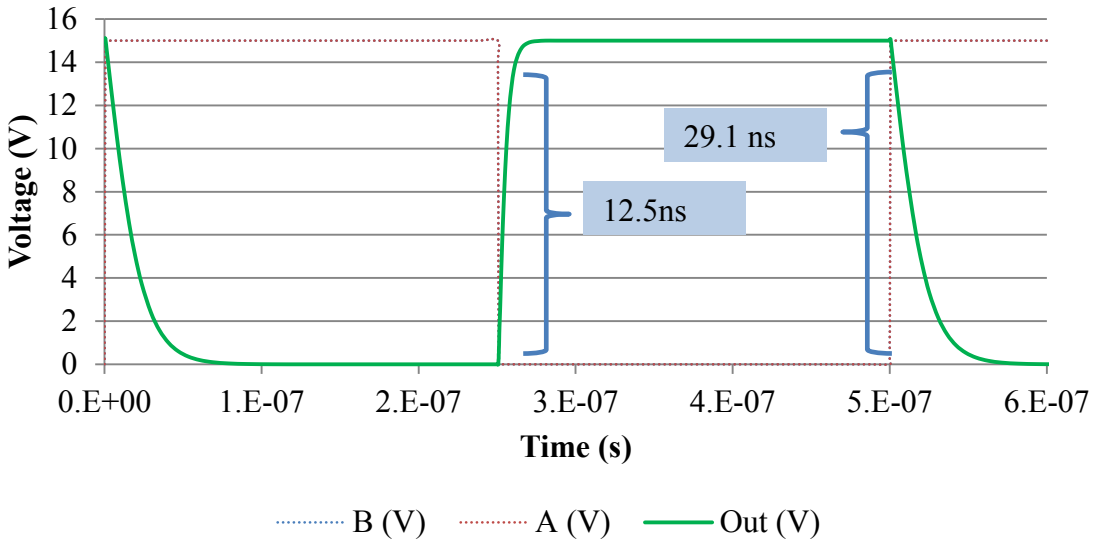


Fig. 4.4. NAND gate transient analysis for rise and fall times in the XFAB process.

Fig. 4.5 shows the simulation results in the TSMC process. Similar to the NAND gate in the XFAB process, the clock signals on the input propagate correctly to the output Z. The difference is the power supply voltage.

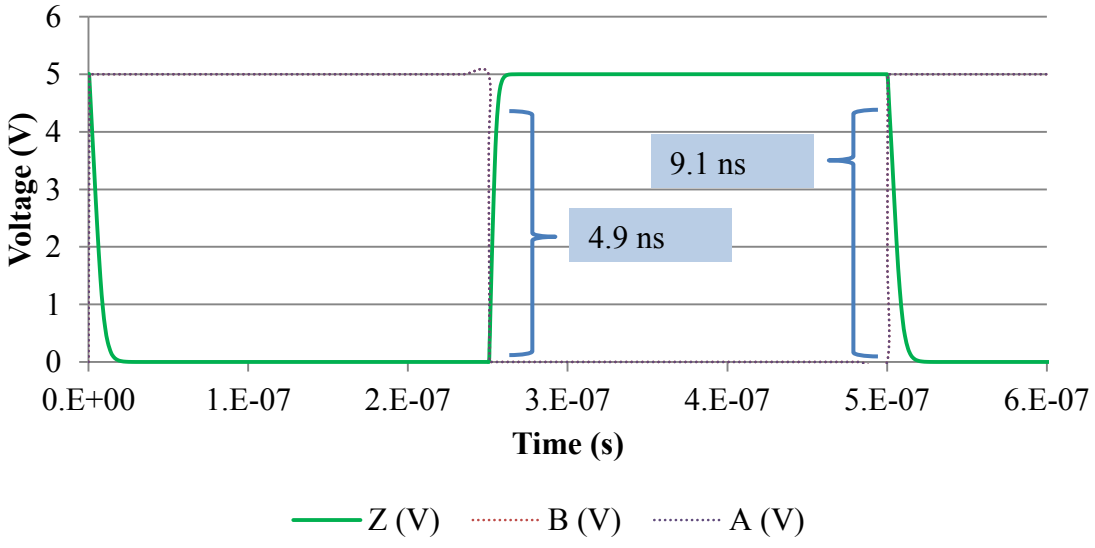


Fig. 4.5. NAND gate transient analysis for rise and fall times in the TSMC process.

4.2.2 Counter

After functionality of the basic digital blocks is verified, the next level of verification in the system path is the counter. The counter encompasses a large portion of the digital design and is the control core of the DAC. The test bench models system stimulus of a 7-bit binary input with the 200 kHz clock signal. The test bench is designed to verify that the clock signal passes through the counter correctly. The test bench for the counter can be seen in Fig. 4.6.

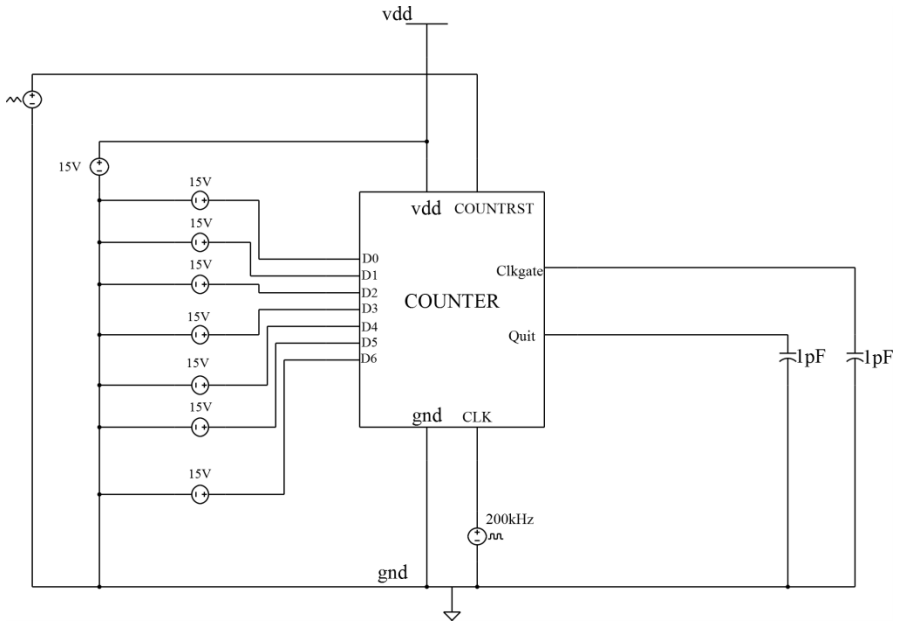


Fig. 4.6. Counter test bench schematic.

The simulation results for the XFAB process are given in Fig. 4.7. As seen, the clock signal propagates correctly based on the value of DAC_EN. The clock signal is properly gated at 40 μs and the quit signal is asserted.

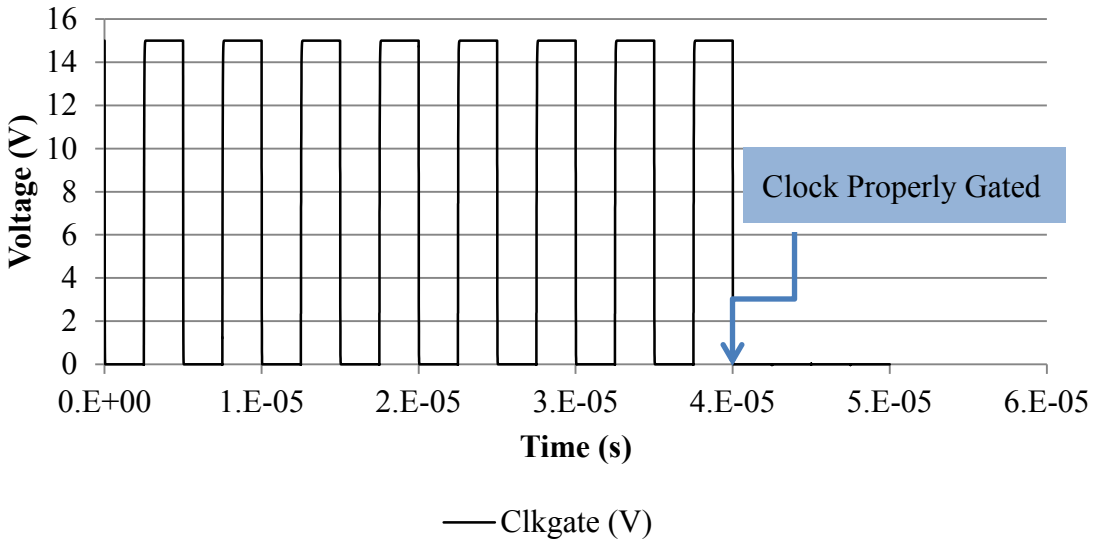


Fig. 4.7. Counter transient analysis results showing proper gating of clock signal in the XFAB process.

The simulation results for the TSMC process can be seen in Fig. 4.8. Again, the clock signal propagates correctly.

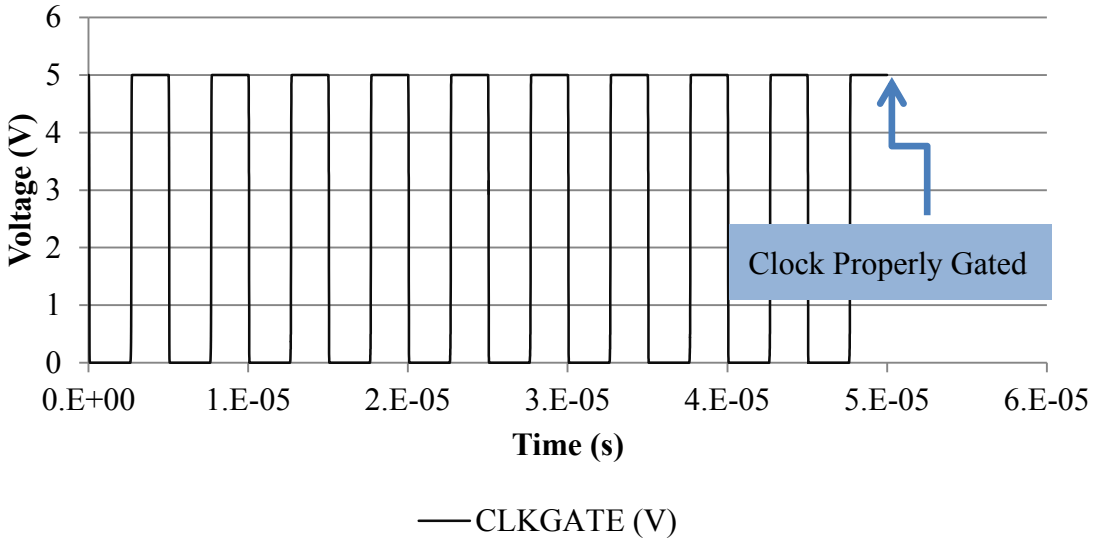


Fig. 4.8. Counter transient analysis results showing proper gating of clock signal in the TSMC process.

4.2.3 Two Phase Clock Generator

Once the clock signal is generated from the counter, it needs to be split into two signals shifted 180° out of phase from each other. It is also important that these two out-of-phase clock signals have minimum crossover to avoid a simultaneous connection of switches in the core; the switching between the two phases in the core must occur exactly 180° from each other. The architecture of the two phase clock generator is different for the two process implementations. In the XFAB process a T-type flip flop was used. It implements an S-R latch at its core which creates the desired 180° phase shift. The buffers on the output then increase the drive strength. The test bench for both takes an input clock signal from the counter and outputs the two clock signals that are 180° out of phase. Fig. 4.9 shows the simulation results for the XFAB process. The simulation shows a small crossover of the two signals at 2.5 µs.

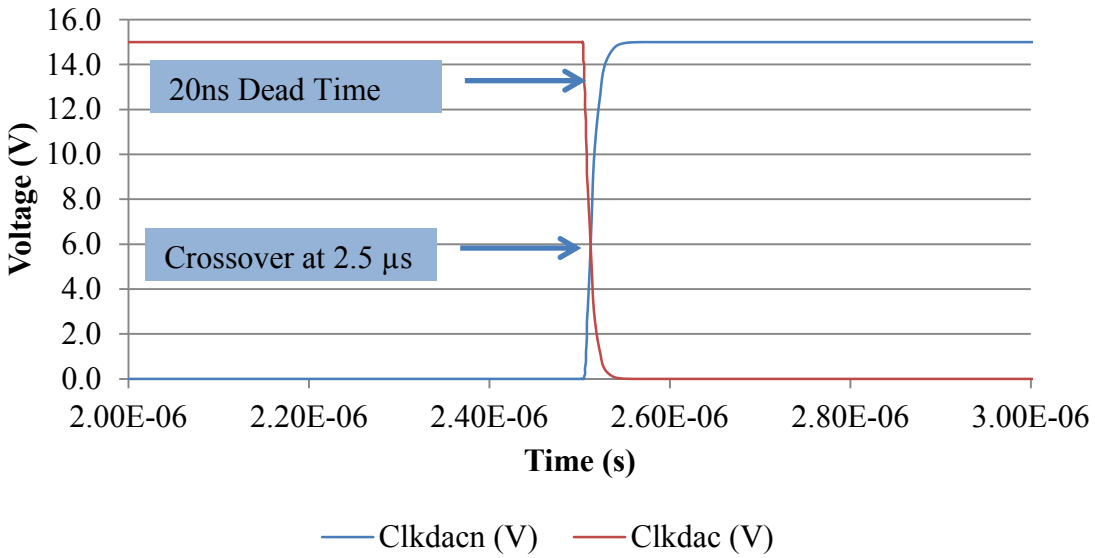


Fig. 4.9. Two phase clock generator demonstrating sufficient non-overlap in the XFAB process.

The two phase clock generator in the TSMC process implements a more basic architecture. It uses feedback from two 2-input NAND gates. Dead time is created by adding

inverters in the feedback path. The output is then enhanced by the increase in drive strength of the buffers. Fig. 4.10 shows the simulation results for the TSMC process. This simulation shows a minimum crossover of the two signals at 5.0 µs.

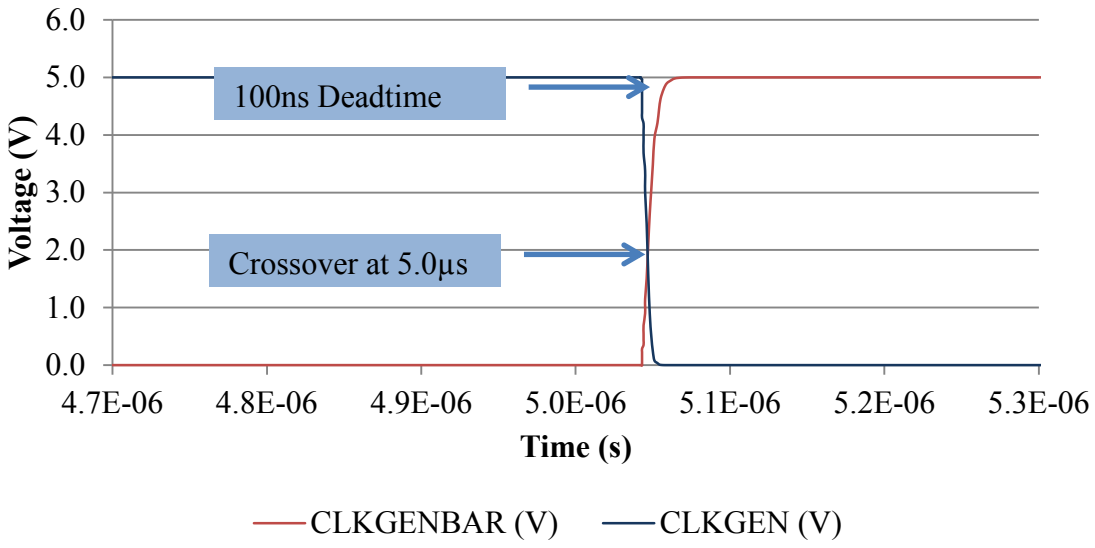


Fig. 4.10. Two phase clock generator demonstrating sufficient non-overlap in the TSMC process.

The combination of the counter and the two phase clock generator create the entire digital system. The entire digital system has been verified to work properly before adding the mixed-signal core. In order to simplify the system before full integration, the mixed-signal portion of the system must be confirmed.

4.3 Analog Simulations

This section consists of the verification of the analog portion of the system. The operational amplifier must be implemented to verify its capabilities before integration into the full system is done.

4.3.1 Operational Amplifier

The two operational amplifiers designed are verified over three regions: (1) DC, (2) small-signal frequency and (3) transient. The following simulations illustrate the op-amp's performance over a swept DC input for both processes. Fig. 4.11 shows the output range of the XFAB op-amp. The op-amp shows a wide output range of 0 V to 15.66 V which is the full range needed for operation.

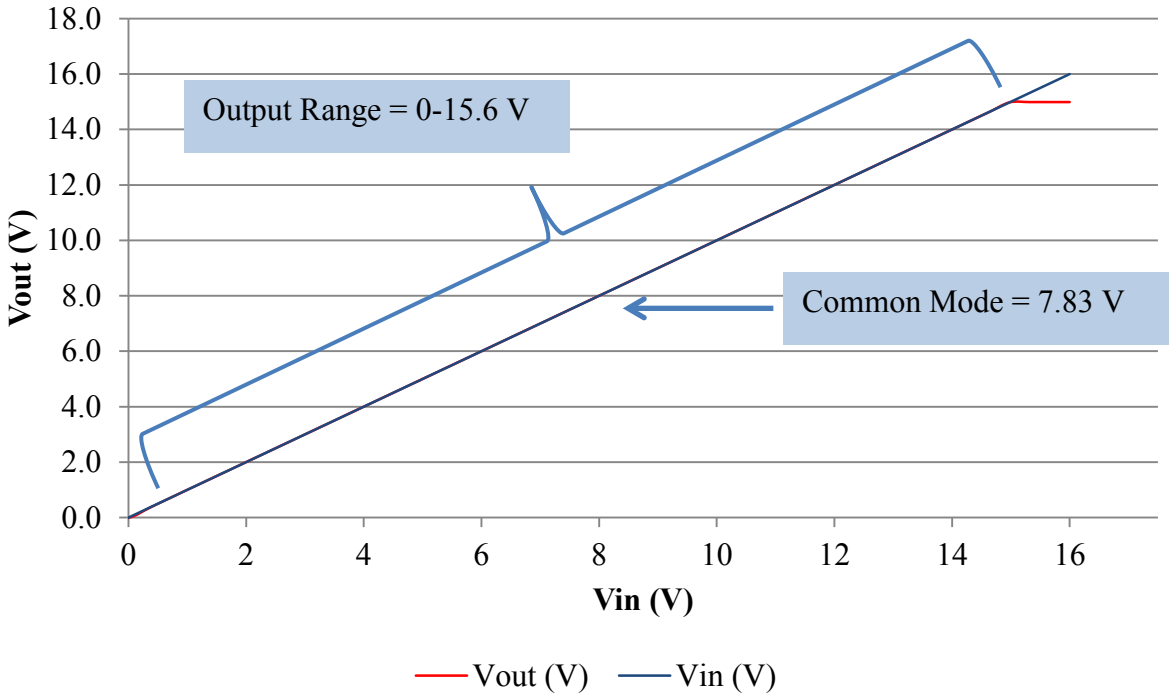


Fig. 4.11. Input vs. output common mode range of the op-amp in the XFAB process.

Fig. 4.12 shows the output range of the op-amp in the TSMC process. The output range of the op-amp is 0.73 V to 4.8 V which accounts for a larger voltage threshold to full voltage rail ratio in this process. This range is the maximum allowable range in order to maintain minimum saturation of all transistors. If the range extended further towards the rails, the devices that most strongly influence the maximum output voltage (M4 and M5) will fall too far into the triode region.

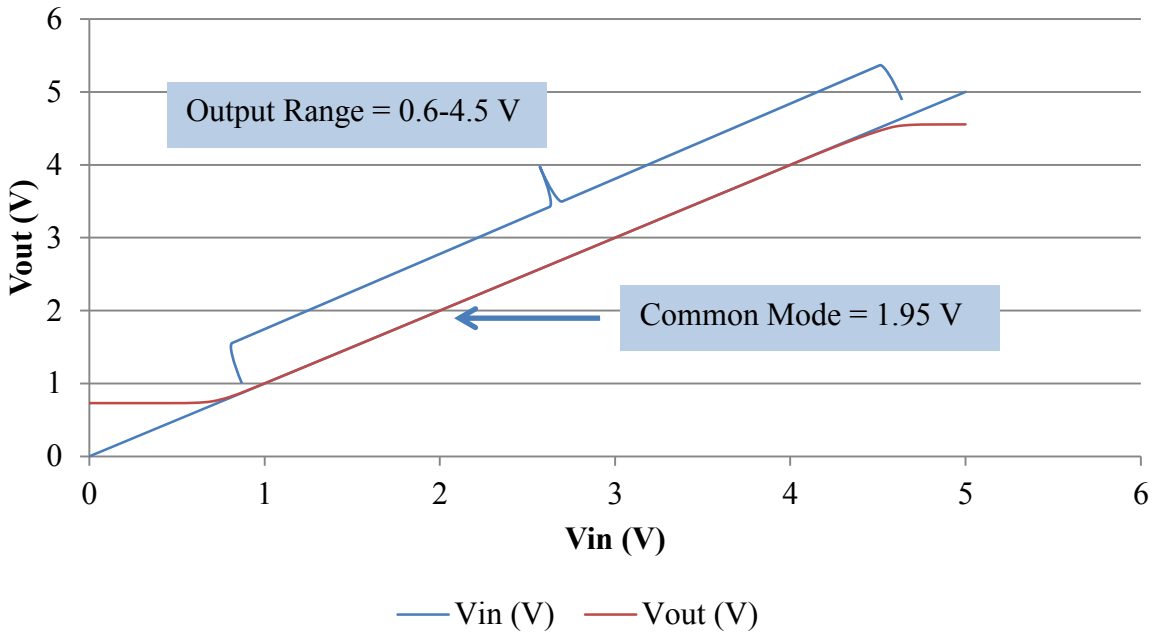


Fig. 4.12. Input common mode rage of op-amp in the TSMC process.

Frequency analysis is the next operation to confirm for the op-amps. Fig. 4.13 shows the frequency bandwidth and phase of the op-amp in the XFAB process. Table 4.2 shows the results of this Bode plot.

TABLE 4.2. XFAB OP-AMP BODE PLOT

Gain	83 dB
-3 dB frequency @ -80 dB	1 kHz
Gain Bandwidth	2.35 MHz
Phase Margin	65°

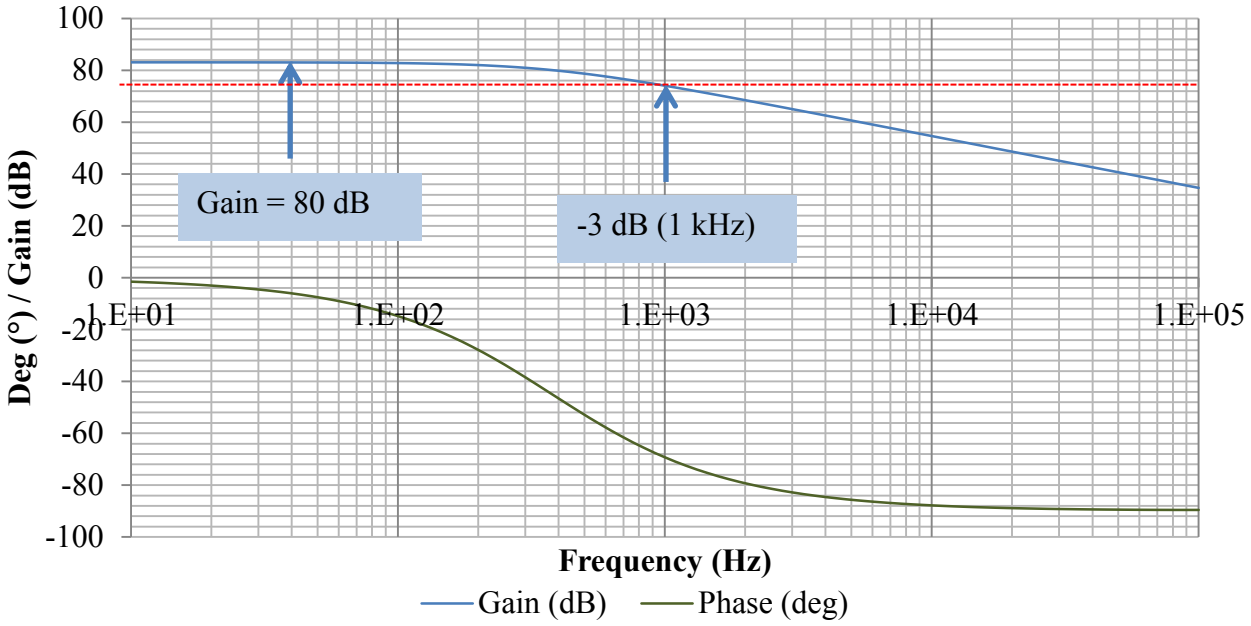


Fig. 4.13. Op-amp bode plot in the XFAB process.

Fig. 4.14 shows the bode plot for the op-amp in the TSMC process. Table 4.3 shows the results of this Bode plot. As shown, it exceeds the specs introduced for a low pass filter band-width of 2 MHz and gain of 50 dB.

TABLE 4.3. TSMC OP-AMP BODE PLOT

Gain	60.25 dB
-3 dB frequency @ -57 dB	6.3 kHz
Gain Bandwidth	5.5 MHz
Phase Margin	87°

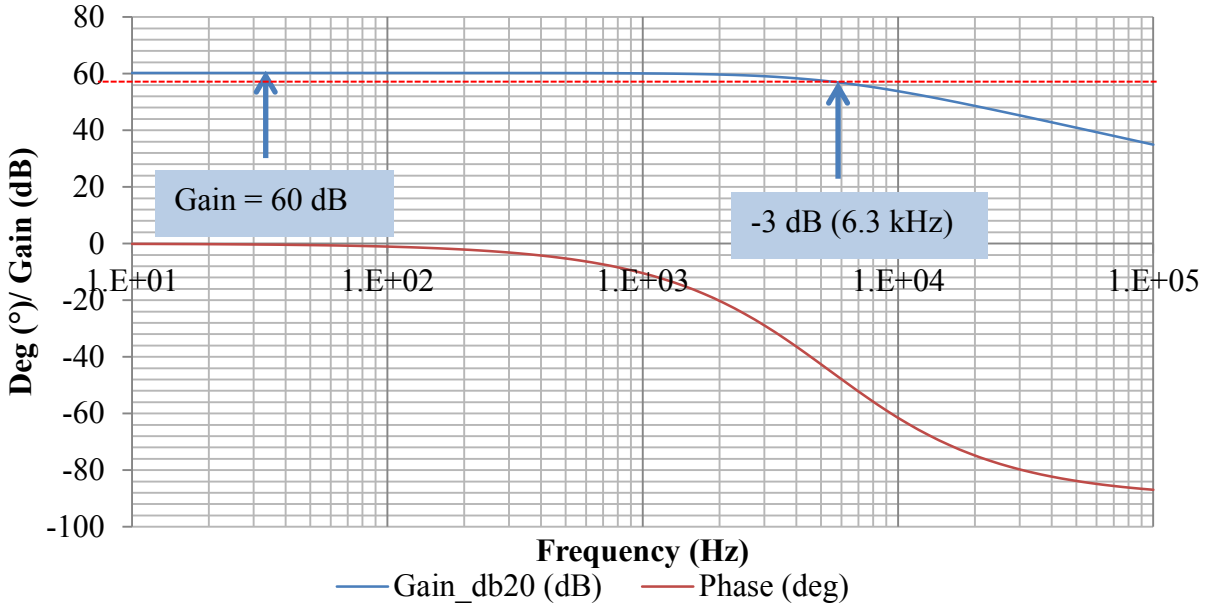


Fig. 4.14. Op-amp bode plot in the TSMC.

The transient analysis for the op-amp is designed to observe the settling time of the output with the op-amp in voltage following configuration. If the settling time is too large the system will not be able to operate within the designed frequency range. The settling time is strongly influenced by the phase margin. Fig. 4.15 shows the transient response of the op-amp in the XFAB process. The settling time is less than 0.6 µs; this is less than the 200 kHz clock signal.

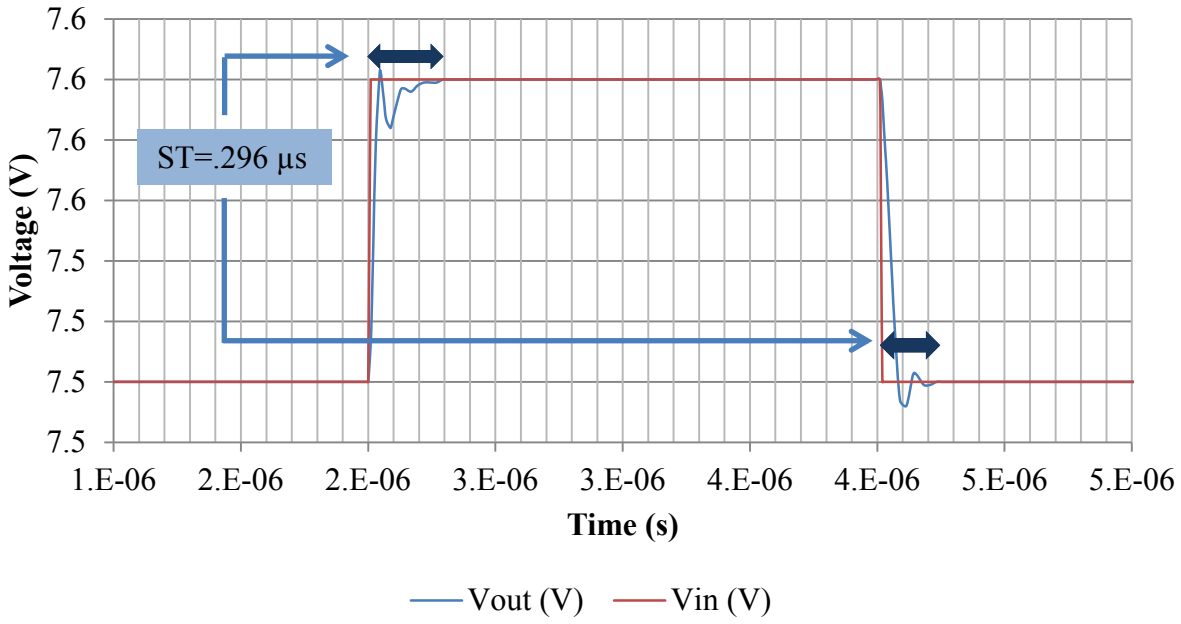


Fig. 4.15. Op-amp output settling time in the XFAB process.

Fig. 4.16 shows the transient response of the op-amp in the TSMC process. The settling time is less than 0.4 µs; this is also less than the minimum clock frequency of 2 kHz. The phase margin predicts an over damped behavior which can be observed in this plot.

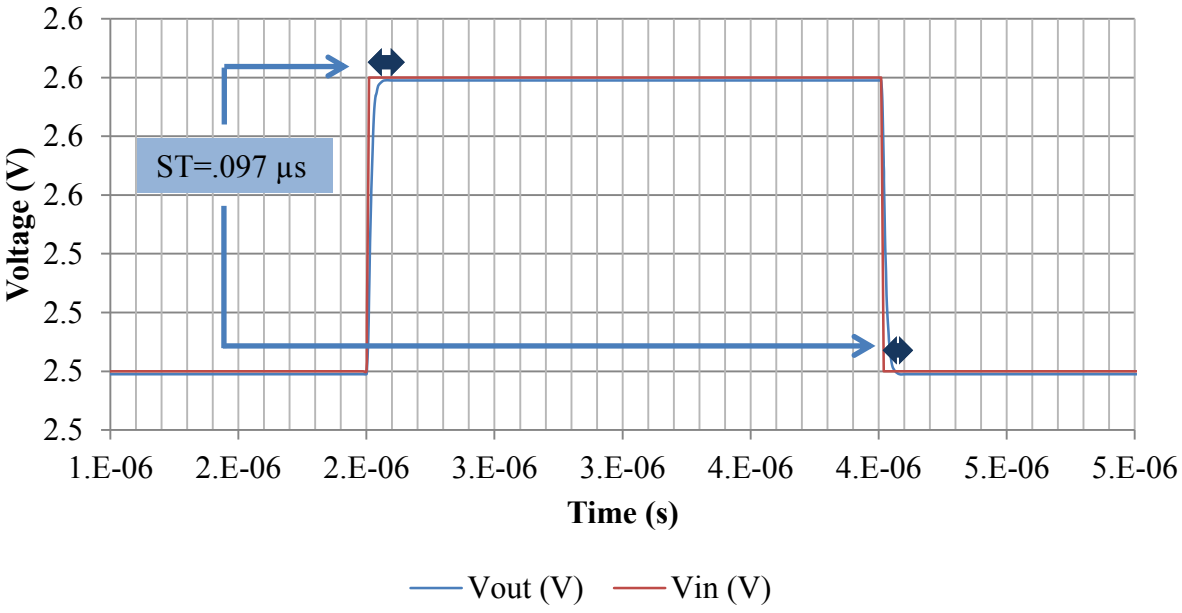


Fig. 4.16. Op-amp output settling time in the TSMC process.

4.4 DAC Integrated Circuit

After block verification has been implemented the full integration can begin. Once the system was fully integrated, full IC/System verification is confirmed. There are four key simulations to determine proper functionality of this digital to analog system. These four are presented in parallel for both processes and verify the specified operation of the DAC. According to the specifications, the DAC must, at minimum, perform three tasks: first, it must receive a binary user input and ramp the output to that desired digital input; second, it must ramp the analog output to the power supply if the user input is greater than the unknown power supply at that time; and third, it must ramp the analog output full scale. A fourth simulation, beyond the specification, is error checking. The error checking will comprise of INL and DNL. Fig. 4.17 shows the test bench for the full system.

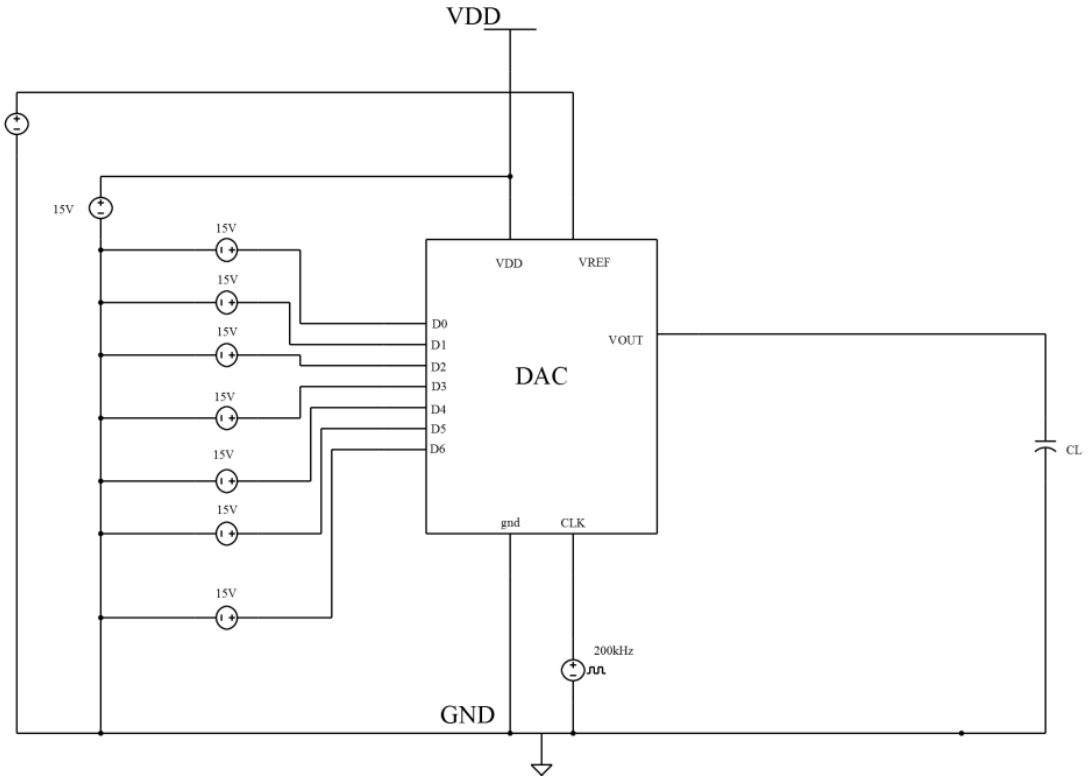


Fig. 4.17. DAC test bench schematic utilized in Cadence.

4.5 XFAB Simulation Results

Fig. 4.18 shows simulation results of the binary match specifications. The seven bit input is (0001000). This is equivalent to eight steps.

$$V_{OUT} = (8steps * 0.105\,V) + 1.5\,V = 2.34\,V$$

The simulation demonstrates that the output of the DAC ramped to a specified voltage and asserted V_{out} to hold this voltage.

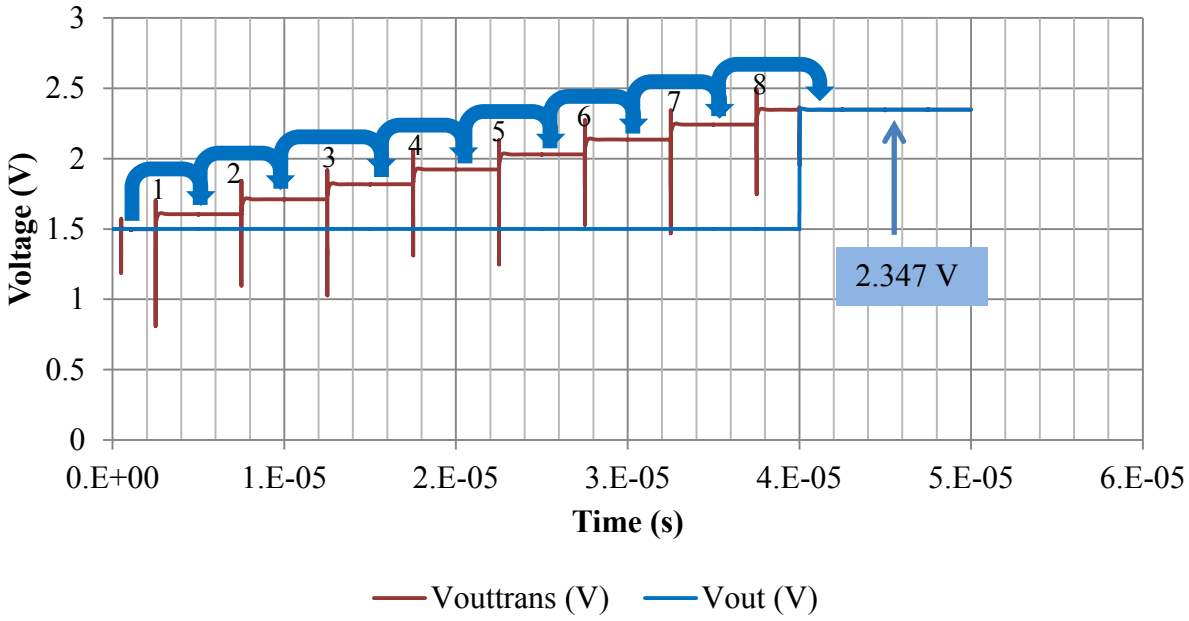


Fig. 4.18. Binary match of the DAC output in the XFAB process.

Fig. 4.19 shows simulation results of the DAC ramping to a power supply that is lower than what the user has requested. The power supply is set at 7.5 V; the simulation shows the output ramping to this voltage and holding its output.

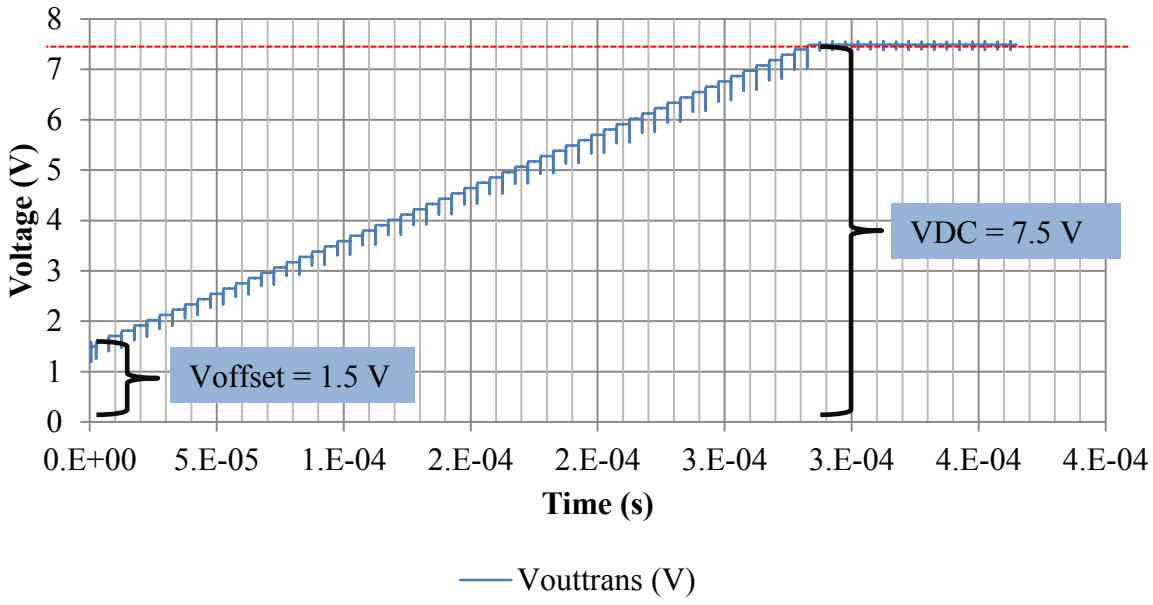


Fig. 4.19. Analysis showing power supply cut-off in the XFAB process.

Fig. 4.20 shows simulation results of the DAC with the full power supply and user input for the full scale. The simulation shows all 128 steps of the 7-bit binary input value increasing in succession ending at the designed output of 15 V.

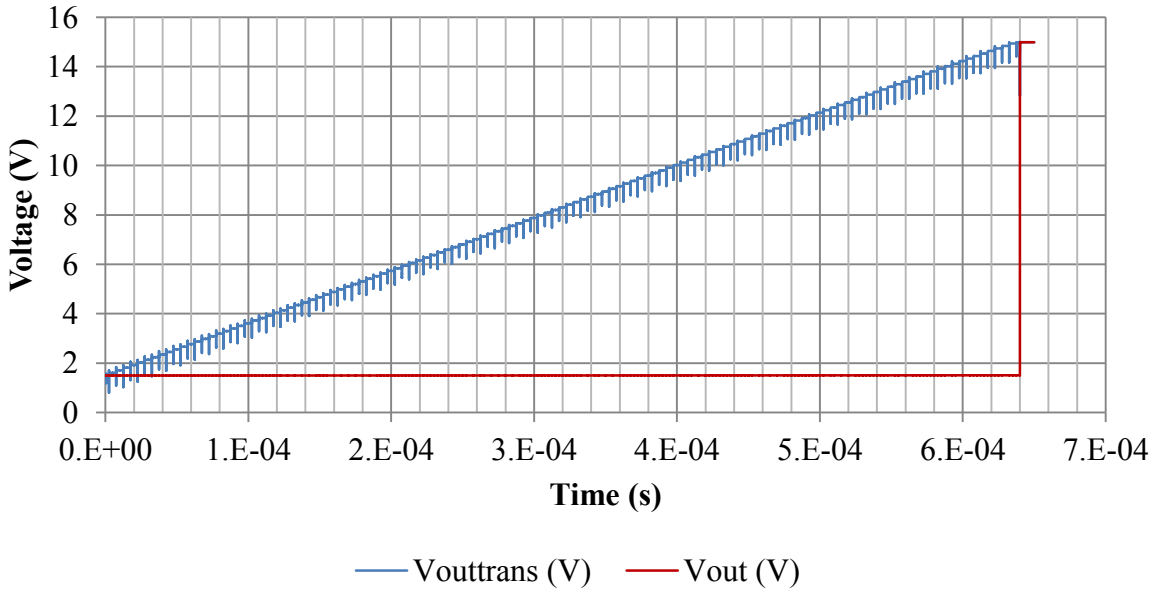


Fig. 4.20. Analysis showing the full scale output of the DAC in the XFAB process.

4.6 XFAB Temperature Simulation Results

The final verification needed as pertaining to the specifications for the XFAB version is over temperature. The process temperature range specified is -50° C to 85° C. The simulations are from the temperature models in the netlist. There are four corners that the DAC was simulated over. Fig. 4.21 is of the DAC in the nominal case over temperature. The simulations show ideal performance over the full scale ramp. The four corners wp, wz, ws, and wo can be found in Appendix A.

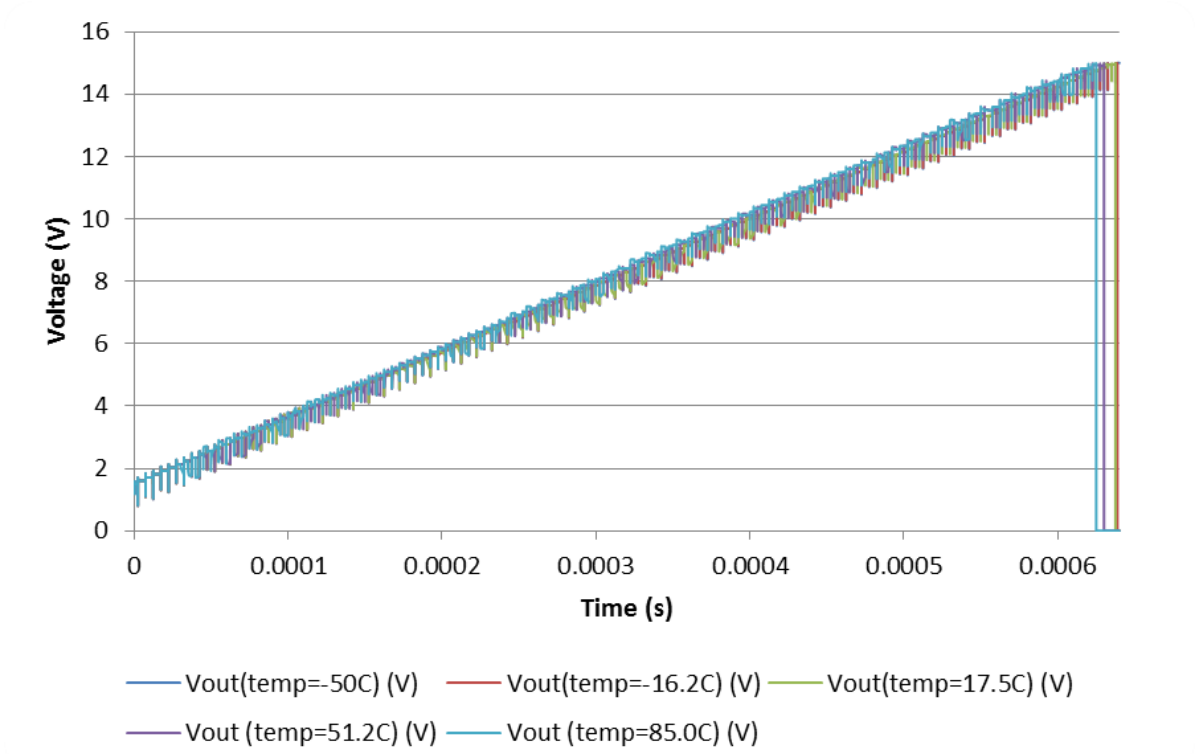


Fig. 4.21. Simulated results of the DAC's full scale ramp over temperature in the XFAB process.

4.7 TSMC Simulation Results

The DAC in the TSMC process has a power supply of 5 V. Maintaining the seven bit parallel input; the DAC will still have a resolution of 128 steps. Fig. 4.22 shows the simulation

results of the binary match specifications. The seven bit parallel input is set to (D1111000). The DAC counts sequentially for 15 steps resulting in an output of 1.028 V. The small "droop" in the output voltage between the first and second step is a result of the transmission gates lower resistance at such a low voltage. However, the capacitors still charge to the proper voltage and the op-amp drives this voltage on the output.

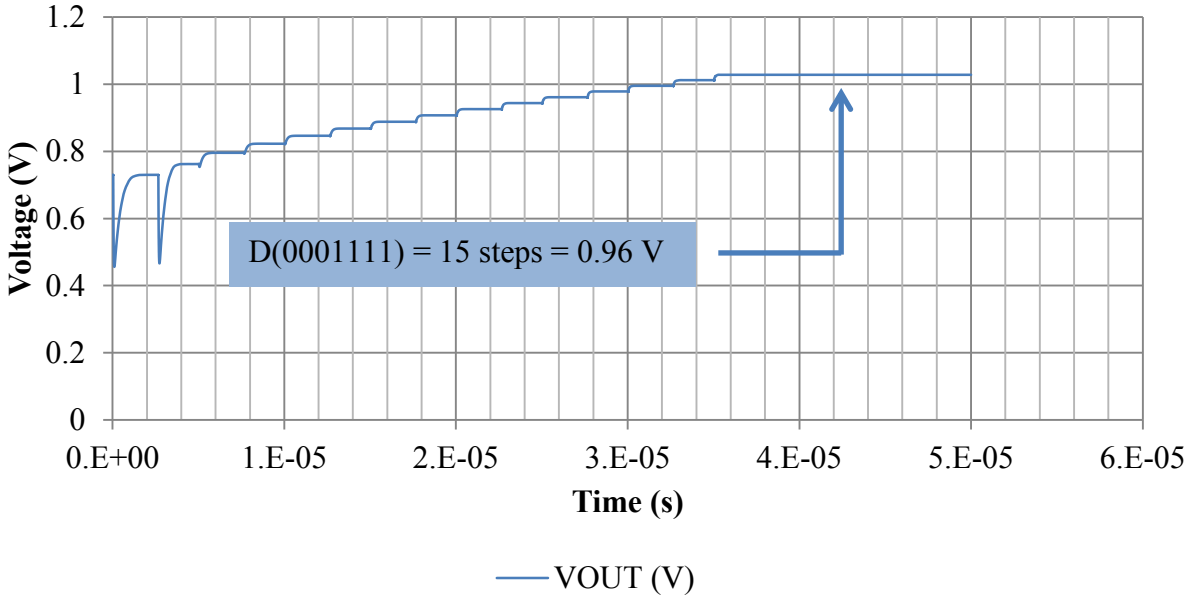


Fig. 4.22. Binary match of the DAC output in the TSMC process.

Fig. 4.23 shows the simulation results when the power supply is set to 4.75 V. The power supply is much closer to the threshold in this process; this results in a less than desirable output for a decreasing power supply. The models do not predict an ideal behavior when the power supply begins to decrease for the entire system. The DAC saturates at 0.86 V. Bench top test could potentially show a different result.

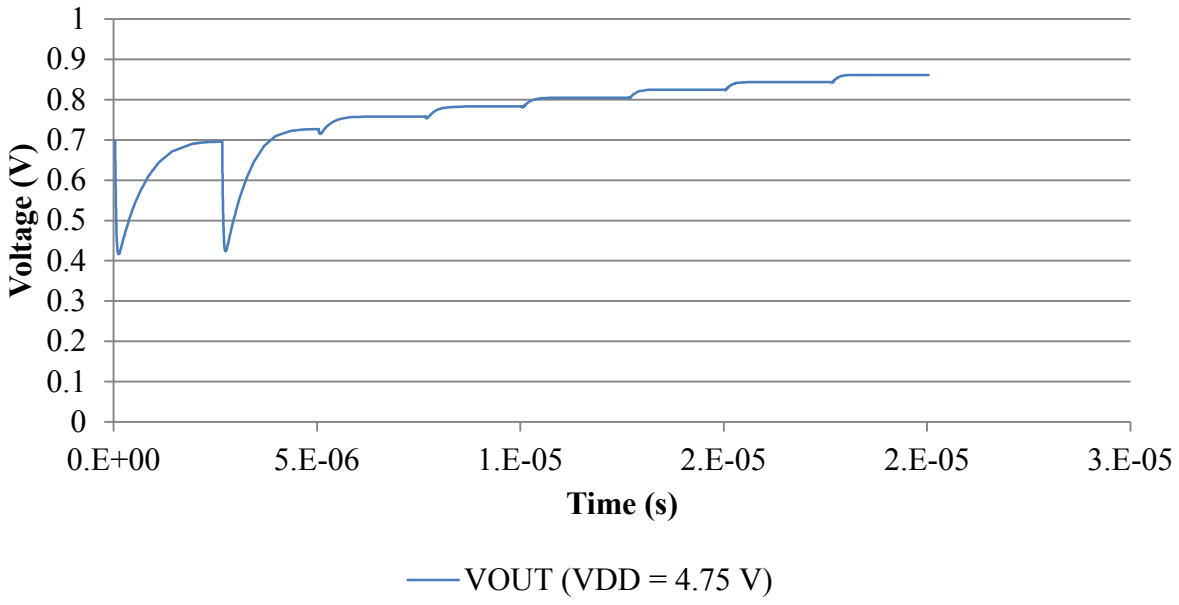


Fig. 4.23. Analysis showing power supply cut-off in the TSMC process.

Lastly, Fig. 4.24 shows the simulation results when the binary request is full scale with the power supply at full range (5 V). The simulation demonstrates proper full scale range (128 steps) with the known output range of the op-amp.

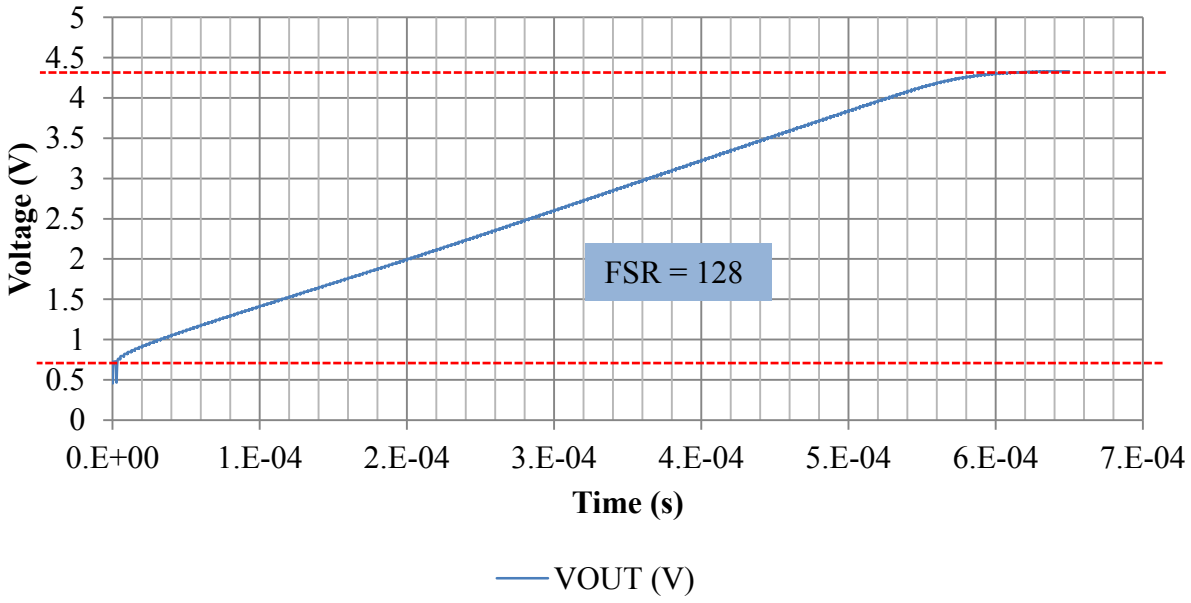


Fig. 4.24. Analysis showing the full scale output of the DAC in the TSMC process.

4.8 Error Checking

In order to fully verify the performance of the functionality validated DAC, INL and DNL error is next evaluated.

4.8.1 DNL

To properly compare the DAC's DNL, the simulator must be set up to sample the output waveform at the exact switching points for the 128 steps. Once this waveform is acquired, it is compared to an ideal step size. The difference, per step, gives the resulting DNL. The resolution of the DAC in the XFAB process is 1.5 V – 15 V over 128 steps resulting in a 105 mV stepping size. Fig. 4.25 shows the DNL of the XFAB process. DNL is represented in LSB vs. the input binary code. Worst case DNL is 0.095 V as compared to one LSB of 105 mV. This confirms a monotonic transfer of data.

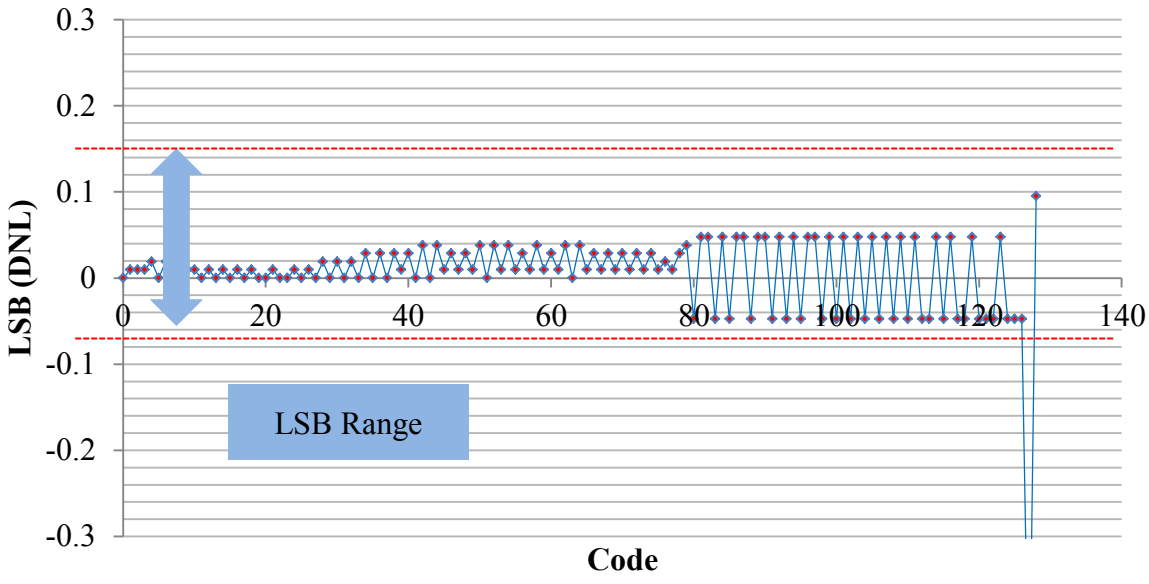


Fig. 4.25. DNL error of the DAC system in the XFAB process.

The output range of the op-amp in the TSMC varied is between 0.73 V – 4.45 V. This range is evaluated when choosing the resolution of the DAC. This step size is 0.029 mV. Fig. 4.26 shows the DNL of the TSMC process. The worst case DNL is 0.08 V compared to one LSB.

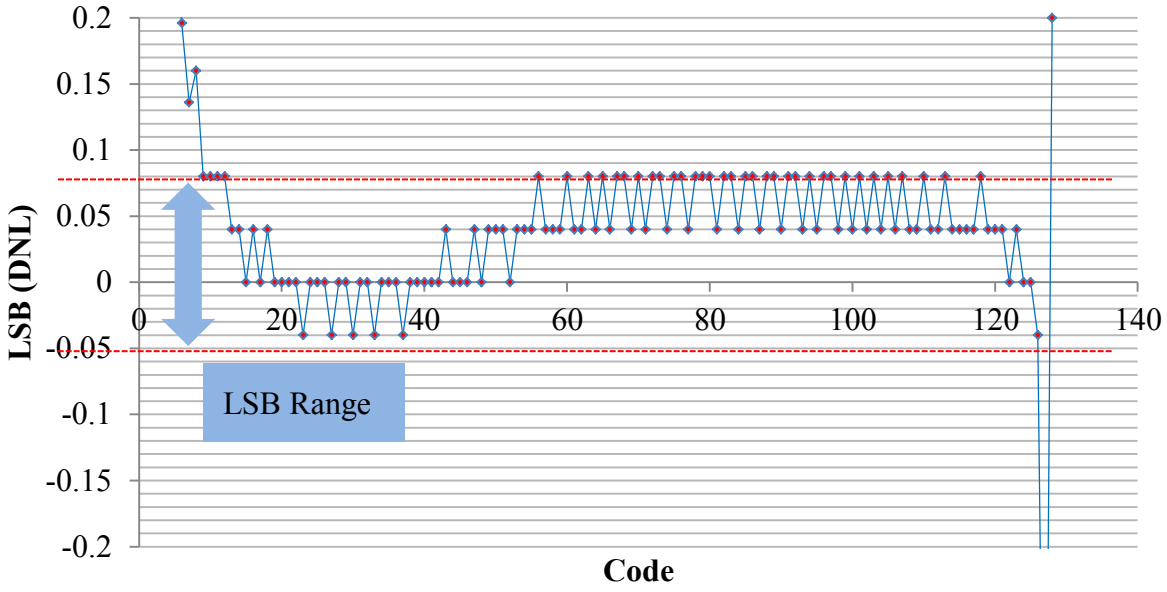


Fig. 4.26. DNL error of the DAC system in the TSMC process.

4.8.2 INL

INL error is evaluated using the same waveform. The difference from DNL is in how it is evaluated. INL observes the error over the full scale range, as opposed to step by step. As described in Chapter 2, a best fit line INL is evaluated. Fig. 4.27 shows the INL error of the XFAB implementation DAC. Visually, the simulation shows the deviation over the full scale range of the simulated data as compared to an ideal best fit line.

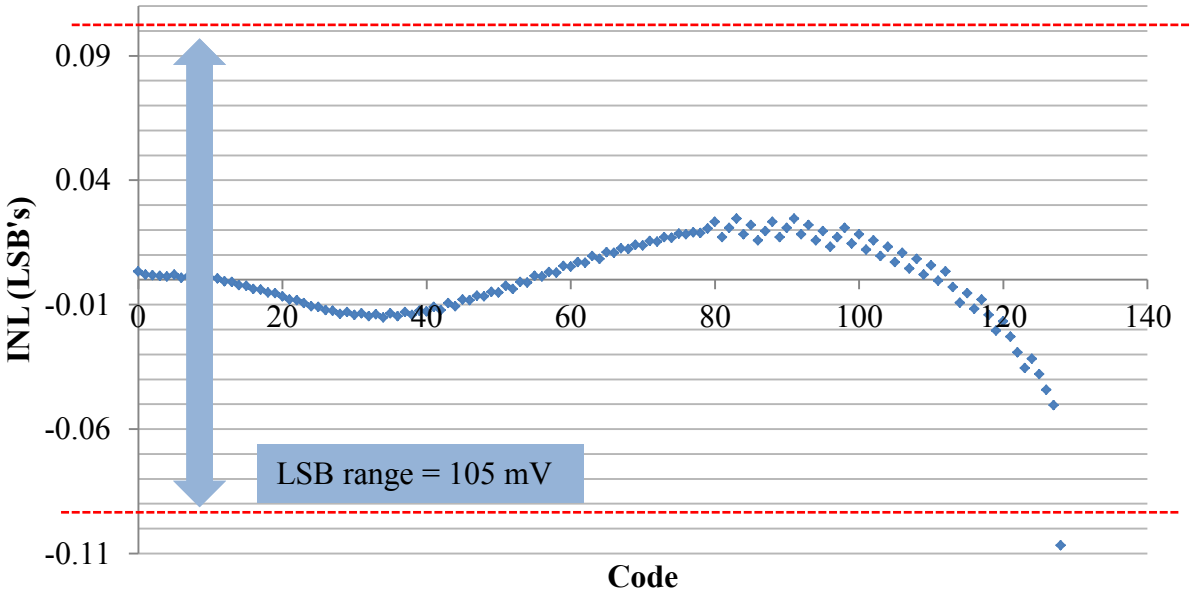


Fig. 4.27. INL error of the DAC system in the XFAB process.

Fig. 4.28 shows the INL error of the TSMC process

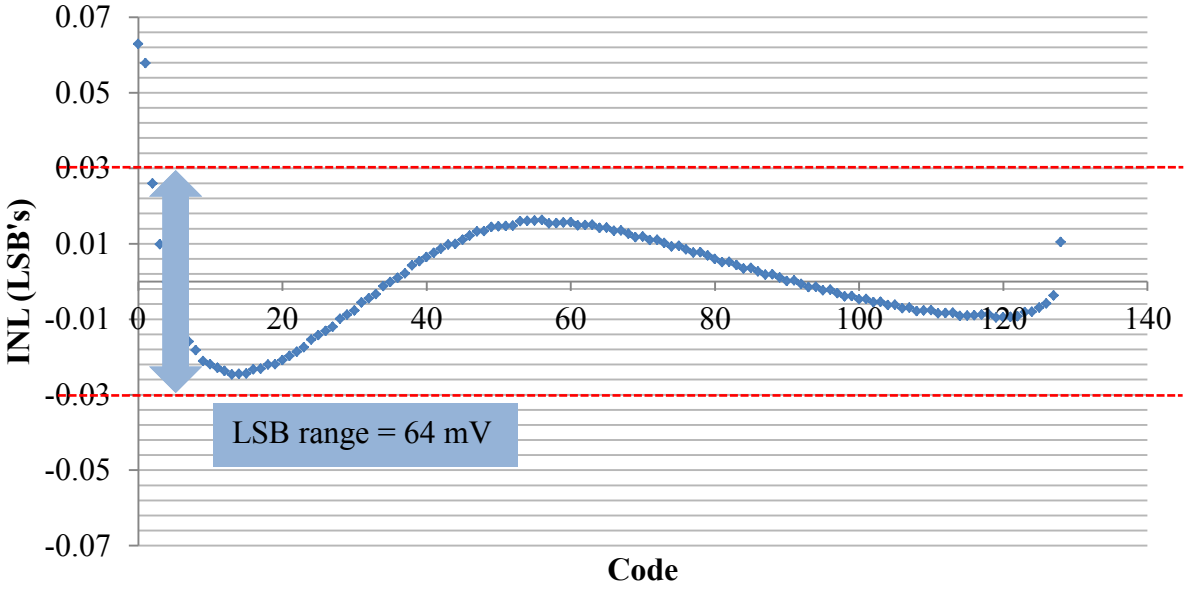


Fig. 4.28. INL error of the DAC system in the TSMC process.

CHAPTER 5 – PHYSICAL DESIGN

The next step in the "V" diagram is the physical design; highlighted in Fig. 5.1.

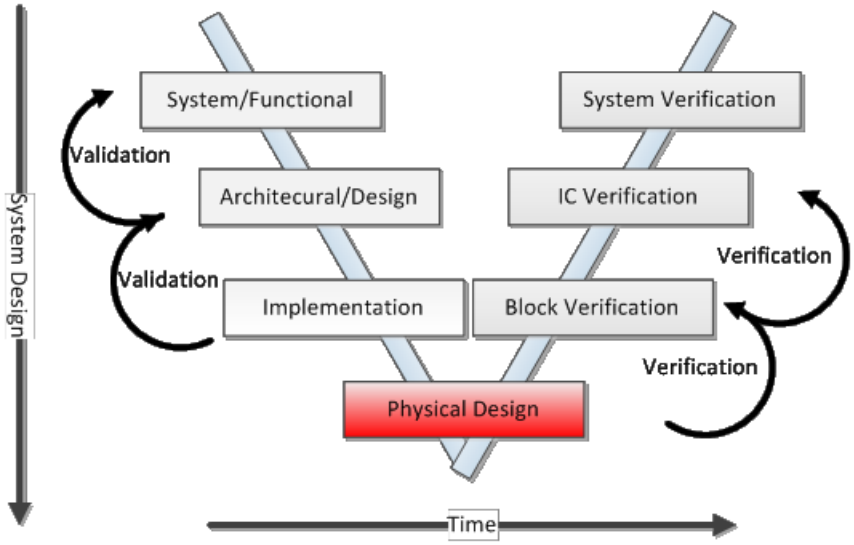


Fig. 5.1. V diagram with physical design step highlighted.

The physical design can change the performance of the schematic based design. Therefore, it is important to consider the effects of layout on the designed system. The process of laying out transistors is not a simple one. Many of the steps involved can change the performance of the system the designer intends on receiving. Both of the processes involved are considered bulk silicon. Bulk silicon processes have great reliability; however, this is not to say that they are without complications. The good news is many of these complications can be avoided by construction. Intelligent layouts can be reliable and immune to the photolithography-induced variation if done correctly. Within this system, there are two main considerations: one, digital gates, two, analog gates.

5.1 Digital Layout

A digital CMOS gate design is relatively simple to layout. Since the devices share a p-n junction, all digital CMOS gates are complementary. This means that the layout lends itself to

symmetry. The designs for all the digital gates are based off of the sizes chosen in the design portion. What follows is the digital cell library that was constructed. All of the gates were constructed in Cadence 5141. All of the verification including design rule check and layout verses schematic were executed in Calibre. The process design kit is provided by TSMC [2]. The physical design of the digital cells followed a basic procedure that can be found in CMOS VLSI Design by Westie and Harris [7]. The procedure follows this simple design; the power rails run horizontally on metal one. The poly gates run vertical allowing the designer to connect through the gate. Fig. 5.2 shows a stick diagram of an inverter to convey the idea.

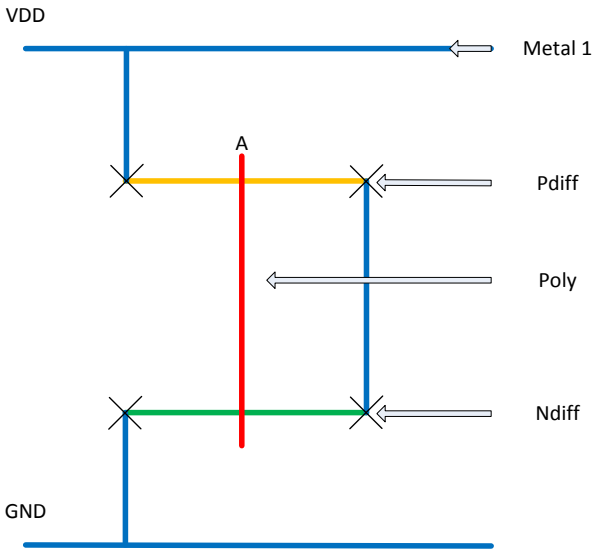


Fig. 5.2. Inverter layout stick diagram with layers defined.

Following this basic methodology, the entire digital gate library was laid out. Fig. 5.3 demonstrates a layout of an inverter using this concept. Referring to the stick diagram design procedure, it is clear to see how the gate is constructed. The metal rails on top and bottom represent the power and ground rails for the gate. The red poly in the middle that is vertical represents the gate and the yellow contacts show how the device will interact within the layout.

Sharing power and ground rails also allow for connection by abutment. This will create a compact design. Table 5.1 shows the layer map for the TSMC process.

TABLE 5.1. LAYER MAP

Light Blue	Metal 1
Purple	Polysilicon
Red/Dark Blue	Pdiff/Ndiff (Active Region)
Yellow	Contacts

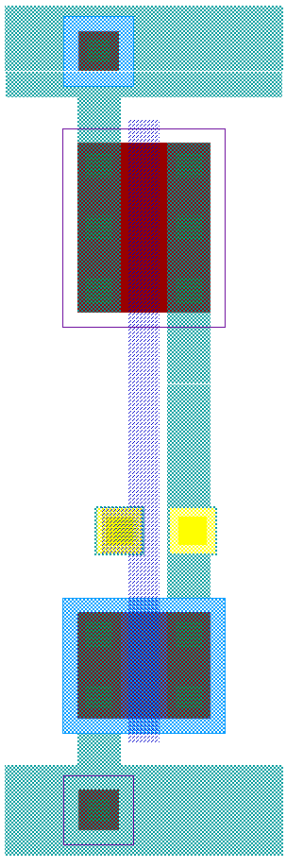


Fig. 5.3. Inverter gate layout in the TSMC process.

5.1.1 Counter Layout

The counter is the bulk of the digital portion of the entire system. It is comprised of all the digital gates designed in the cell library. Table 5.2shows a list of all the digital cells in the counter.

TABLE 5.2. COUNTER PART LIST

Gate Name
T-Type Flip Flop
Inverter
XOR
NAND2
NAND3
NOR2
NOR3
D-Type Flip Flop

Fig. 5.4 shows the layout of the counter. The aspect ratio is 144 μm × 104 μm.

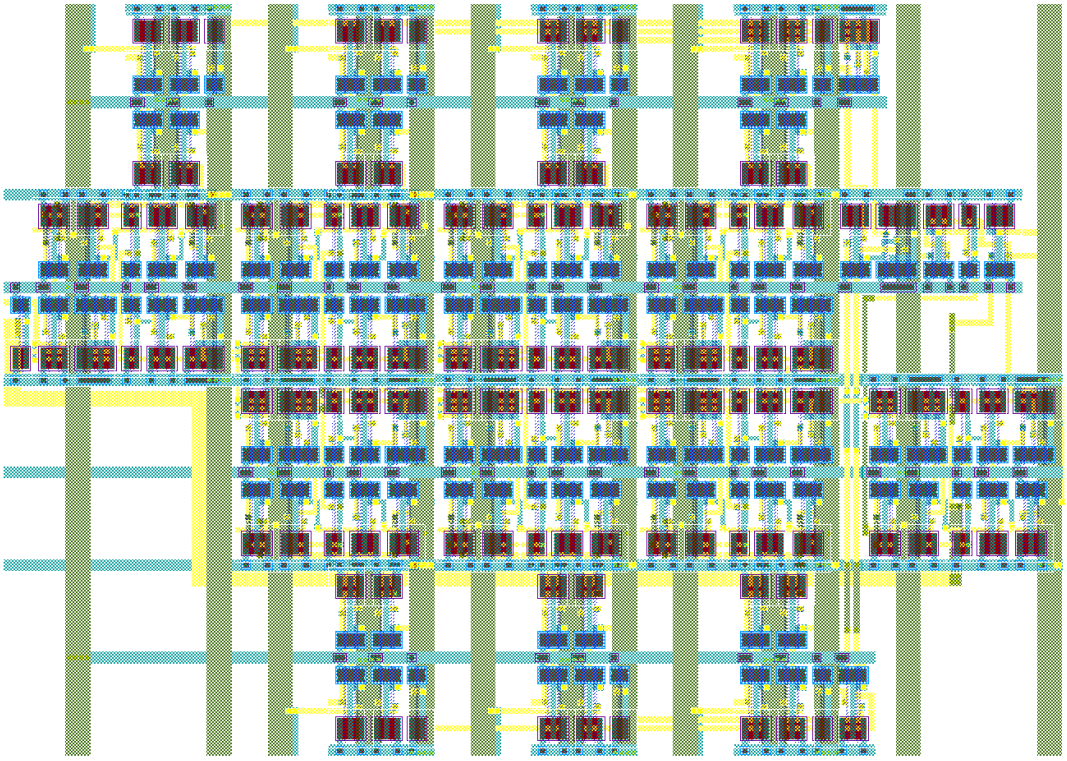


Fig. 5.4. Counter layout in the TSMC process.

5.1.2 Two Phase Clock Generator Layout

The two phase clock generator is fed a clock signal from the counter. Its main goal is to then generate two clock signals that are 180 degrees out of phase as well as non-overlapping. The delay is created by adding inverters in the feedback network. The fan out of this cell is critical. The output of the two phase clock generator will feed the input of the internal gates within the DAC core. Therefore, output buffering is added. Table 5.3 shows a list of the cells used in the two phase clock generator.

TABLE 5.3. TWO PHASE CLOCK GENERATOR CELL LIST

Gate Name
Inverter
Inverter 2
Inverter 4
NAND2

Fig. 5.5 shows the layout of the two phase clock generator. Its aspect ratio is 32 µm × 26 µm.

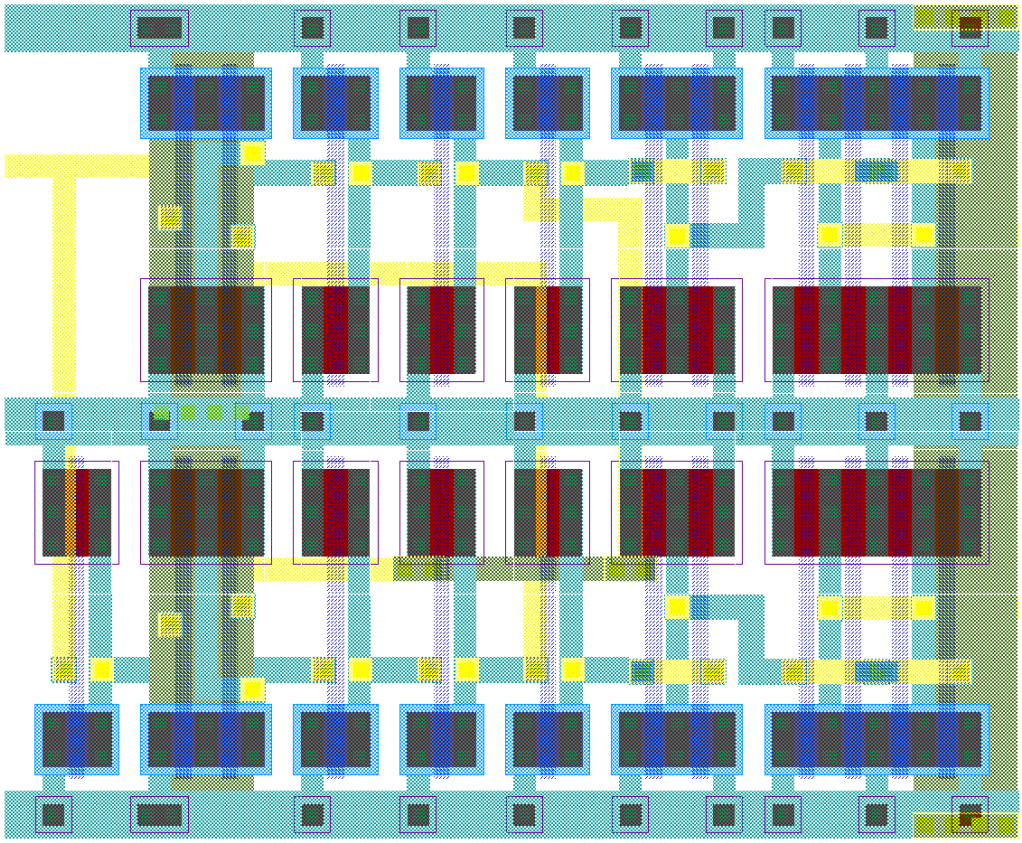


Fig. 5.5. Two phase clock generator layout in the TSMC process.

5.1.3 Digital Core

The digital core is the integration of the counter and the two phase clock generator. Fig. 5.6 shows the layout of the digital core.

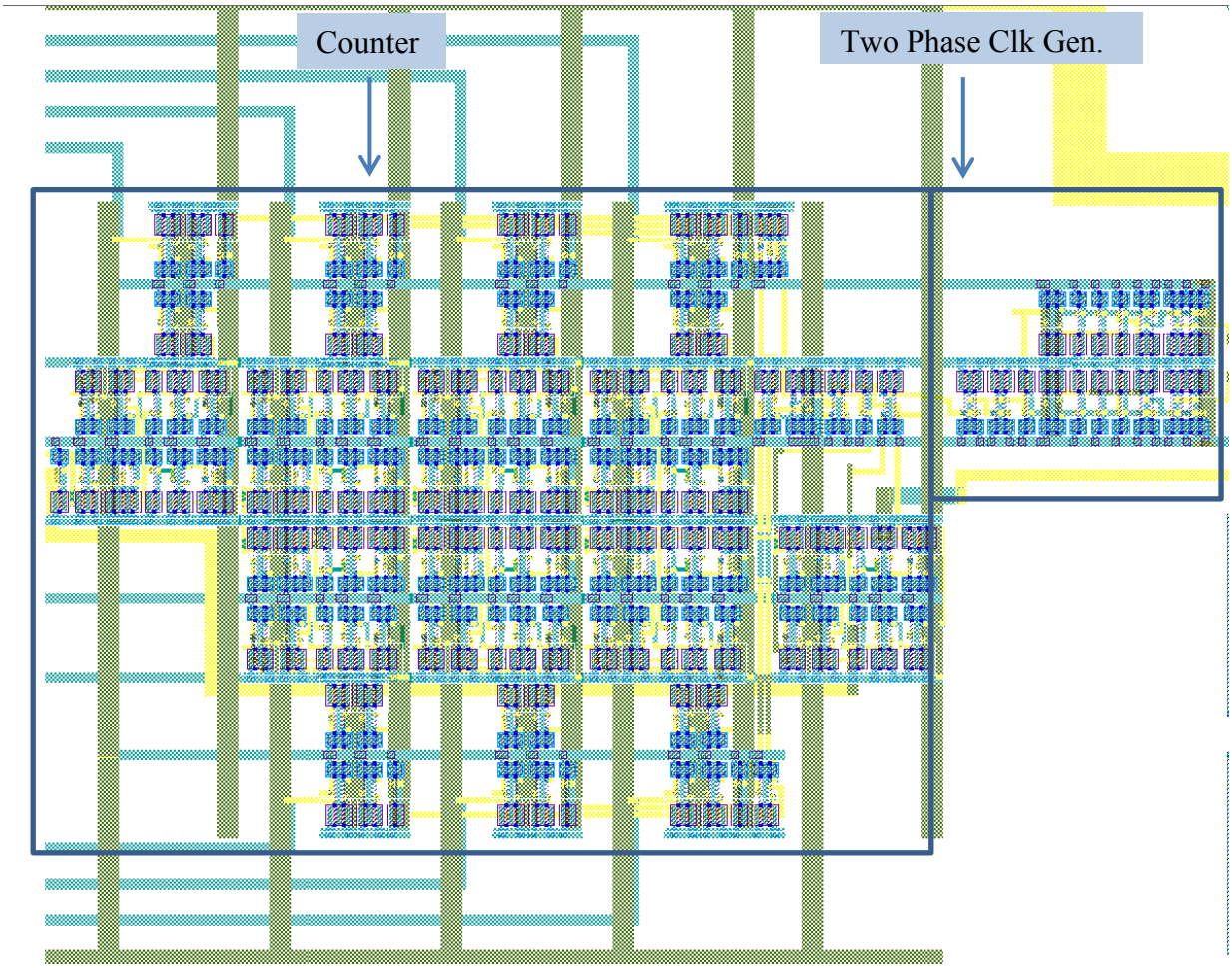


Fig. 5.6. Digital core layout in the TSMC process.

5.2 Analog Layout

The rest of the system will contain analog layout considerations. Analog layout has more considerations as compared to digital; this is due to the need of having to operate in all ranges of the power supply. Predictability is not as simple as either on or off. Therefore, design and layout are critical for analog.

5.2.1 Operational Amplifier

The operational amplifier is the heart of the mixed-signal core. It provides the necessary drive strength to charge the internal capacitors to the 105 mV needed for each bit. The layout of the operational amplifier follows traditional analog considerations [15]. A few of these considerations are: doubling the W/L of the input devices, using dummy gates on the edge of the gates to account for processing, and using common centroid symmetry.

Doubling the W/L of the input devices lowers the risk of offset from processing, due to longer devices having better matching capabilities. The use of dummy gates is important in analog design. The etching of a gate when it is surrounded by other gates creates a different profile then gates that do not. In order to guarantee that each gate cross-section is identical an extra gate is added at the end of each device to ensure consistence processing. Common centroid is a method used to account for gradient induced mismatches. If the transistors are laid out in a way that the common point is exactly in the middle, this will account for linear changes in the process and cancel out that effect. Devices that share gates and sources need only fingers to create the necessary W/L ratio. Devices that do not share gates or sources will need fingers and multiplicity to achieve the necessary W/L. Fig. 5.7 shows the layout of the operational amplifier. Its aspect ratio is 94 μm × 56 μm.

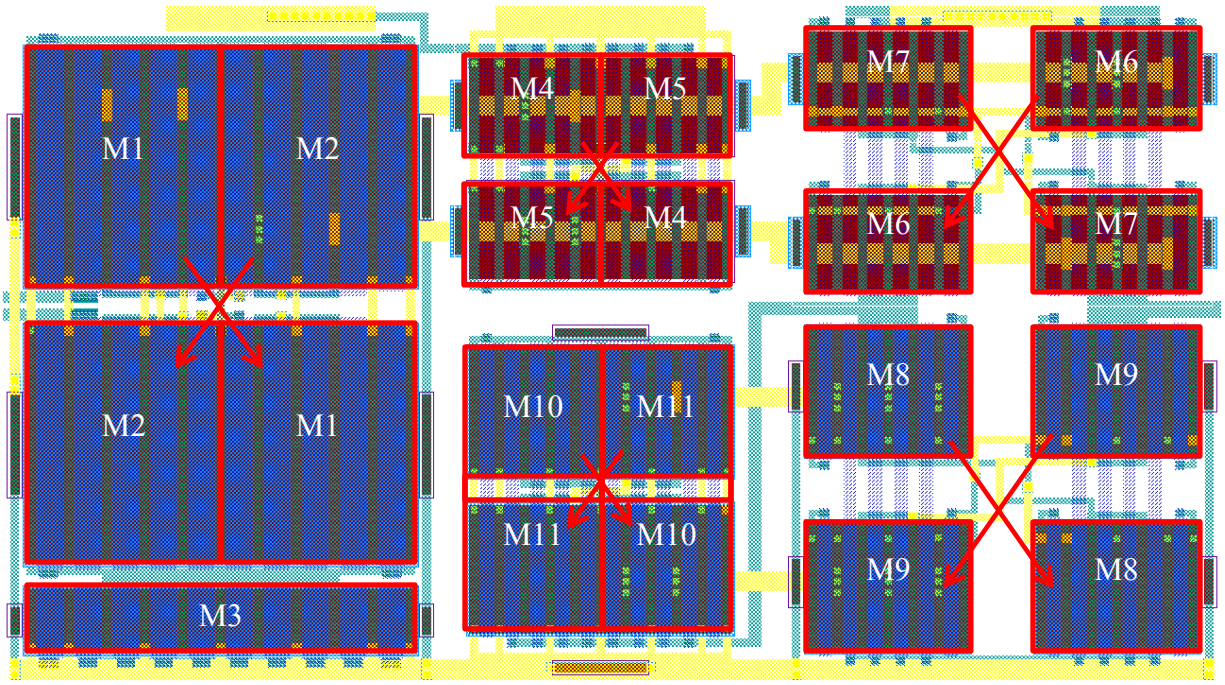


Fig. 5.7. Operational amplifier layout in the TSMC process.

5.2.2 Mixed-Signal Core

The mixed-signal core is where the two phase clocks in combination with the capacitors and op-amp generate the output stair stepping effect. The layout of the mixed-signal core depends on symmetry. This is due to the nature of its operation. The mixed-signal core is considered one level higher in the design from the operational amplifier. The integration of the op-amp with the capacitors and transmission gates comprise the parts for the mixed-signal core. Fig. 5.7 shows the layout of the mixed-signal core. Its aspect ratio is 338 µm × 198 µm.

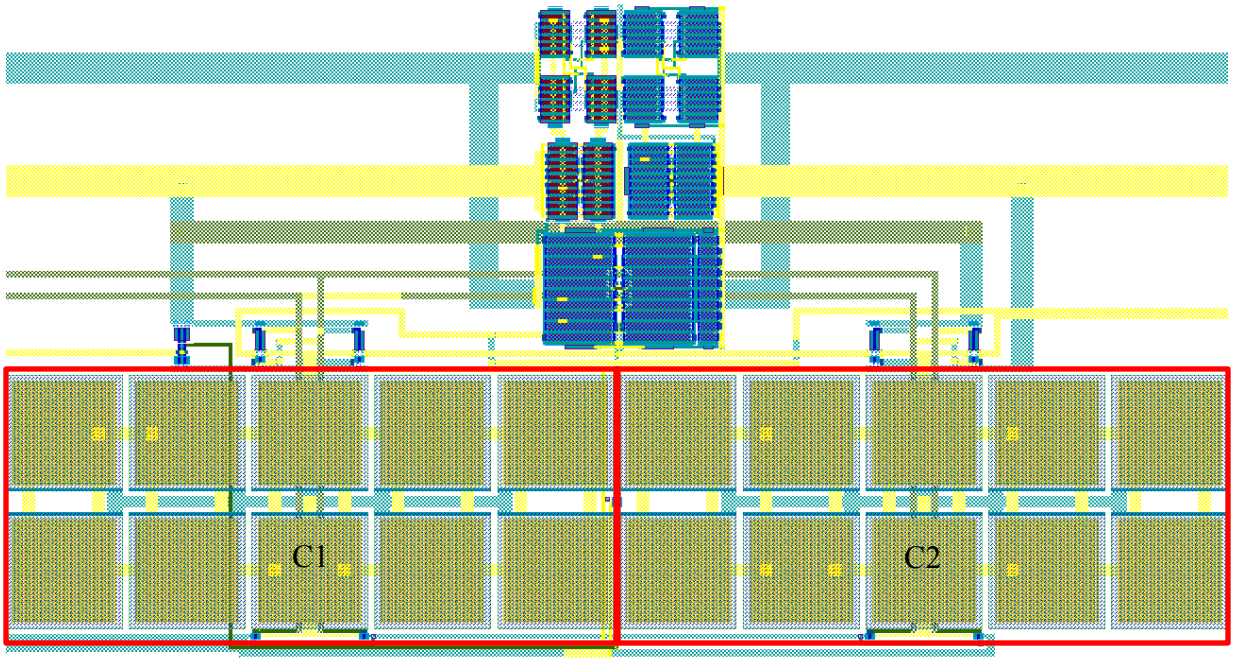


Fig. 5.8. Mixed-signal core layout in the TSMC process with capacitors highlighted.

5.3 Full Chip Layout

Different parts of this system were padded out in order to prepare for in-depth risk analysis. Each cell that had a pin count too high to probe on the probe station was given a custom ESD pad ring. Each pad ring was designed to fit within a standard 16 pin dip package. Each pad is large enough to account for a bond wire attachment.

5.3.1 Digital Core

Fig. 5.9 shows the layout of the digital core with a custom pad ring. The pads are 100 µm × 100 µm. The total aspect ratio is 1,008 µm × 852 µm.

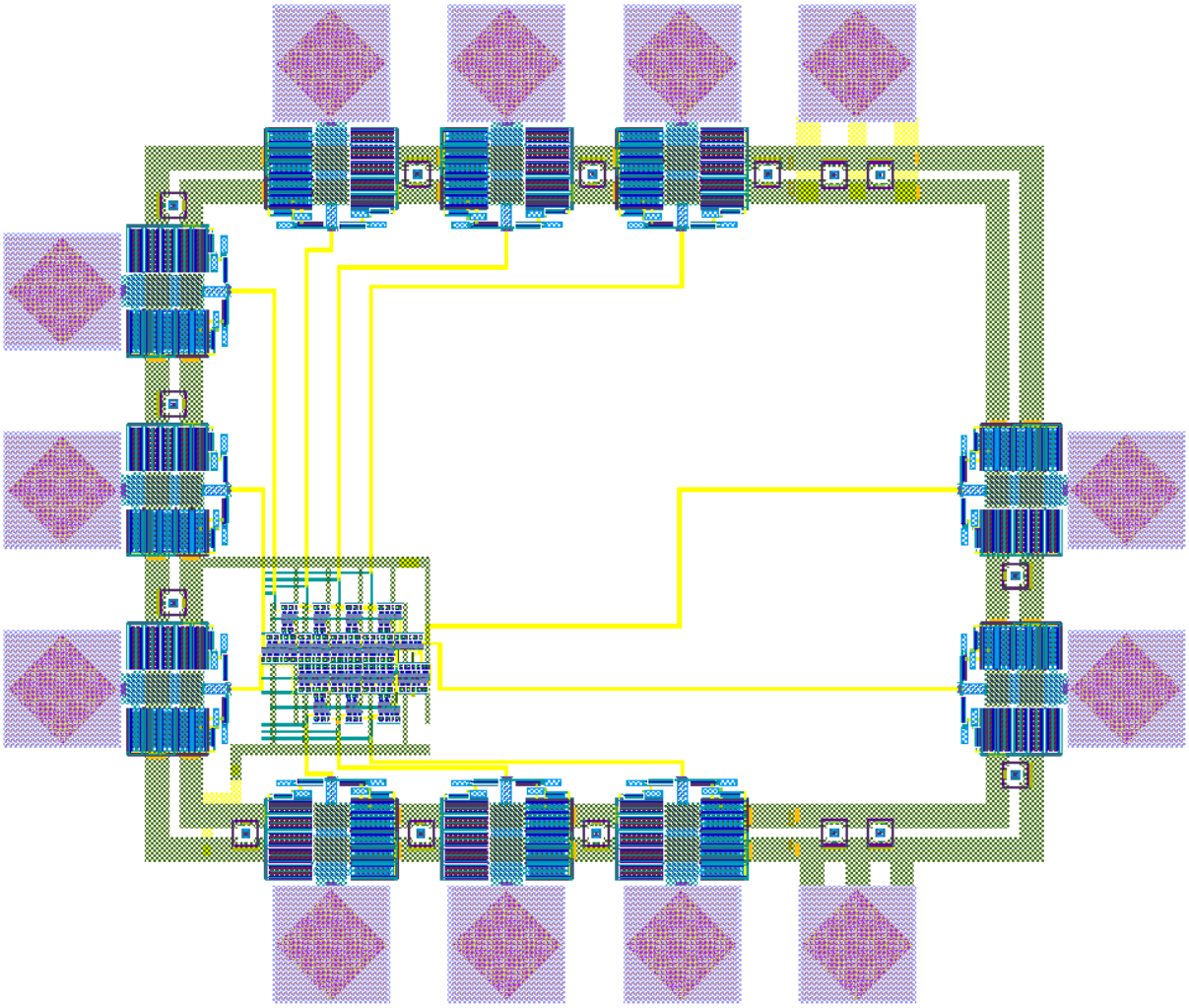


Fig. 5.9. Digital core layout with pad ring and interconnect.

5.3.2 Analog Core

Fig. 5.10 shows the layout of the analog core with pad ring. The total aspect ratio is 1,008 µm × 852 µm.

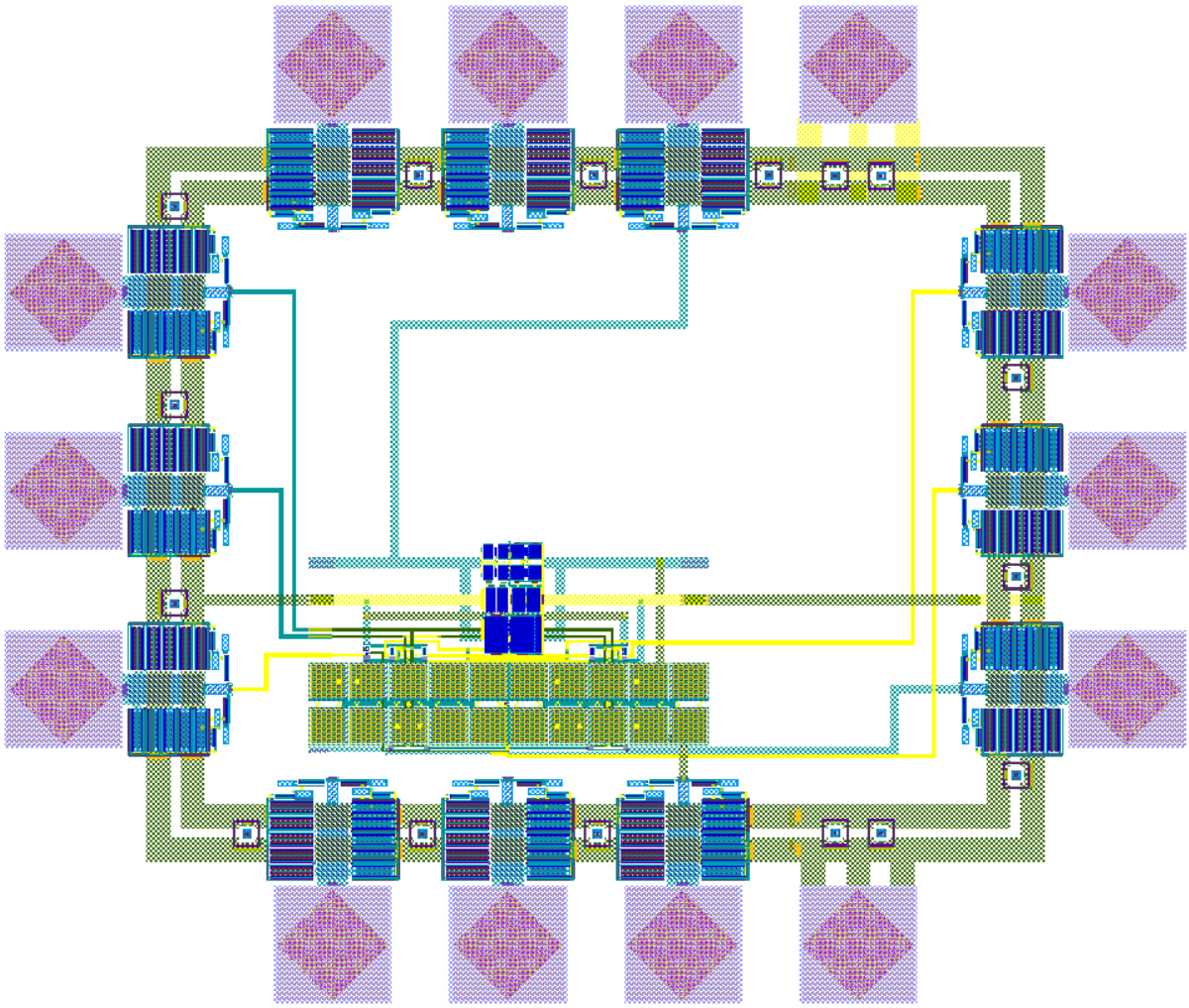


Fig. 5.10. Analog core layout with pad ring and interconnect.

5.3.3 DAC with no Voltage Reference

There are two versions of the top level layout of the system. One is with a built in voltage reference for biasing and the other is without an integrated voltage reference. The voltage reference in this case is provided off chip. Fig. 5.11 shows the layout of the entire system without the built in voltage reference. Its aspect ratio is 532 µm × 180 µm.

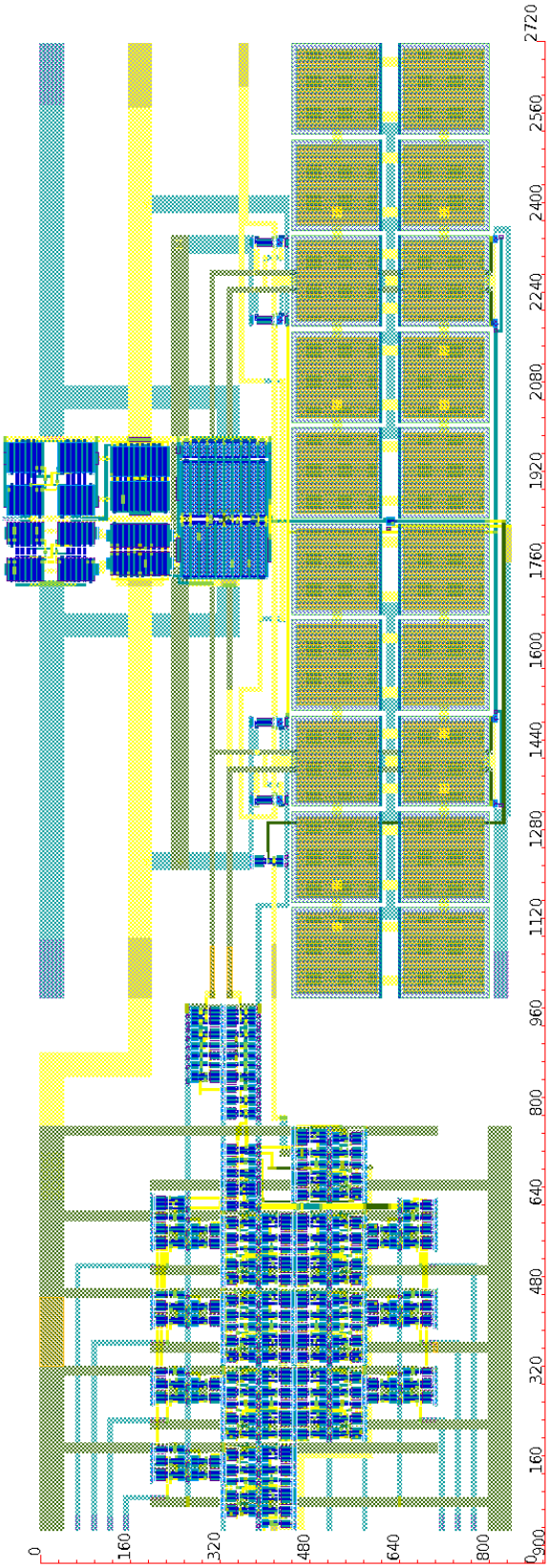


Fig. 5.11. DAC layout with no voltage reference and no pad ring.

Fig. 5.12 shows the layout of the entire system with pad ring. Its aspect ratio is 1160 µm × 852 µm.

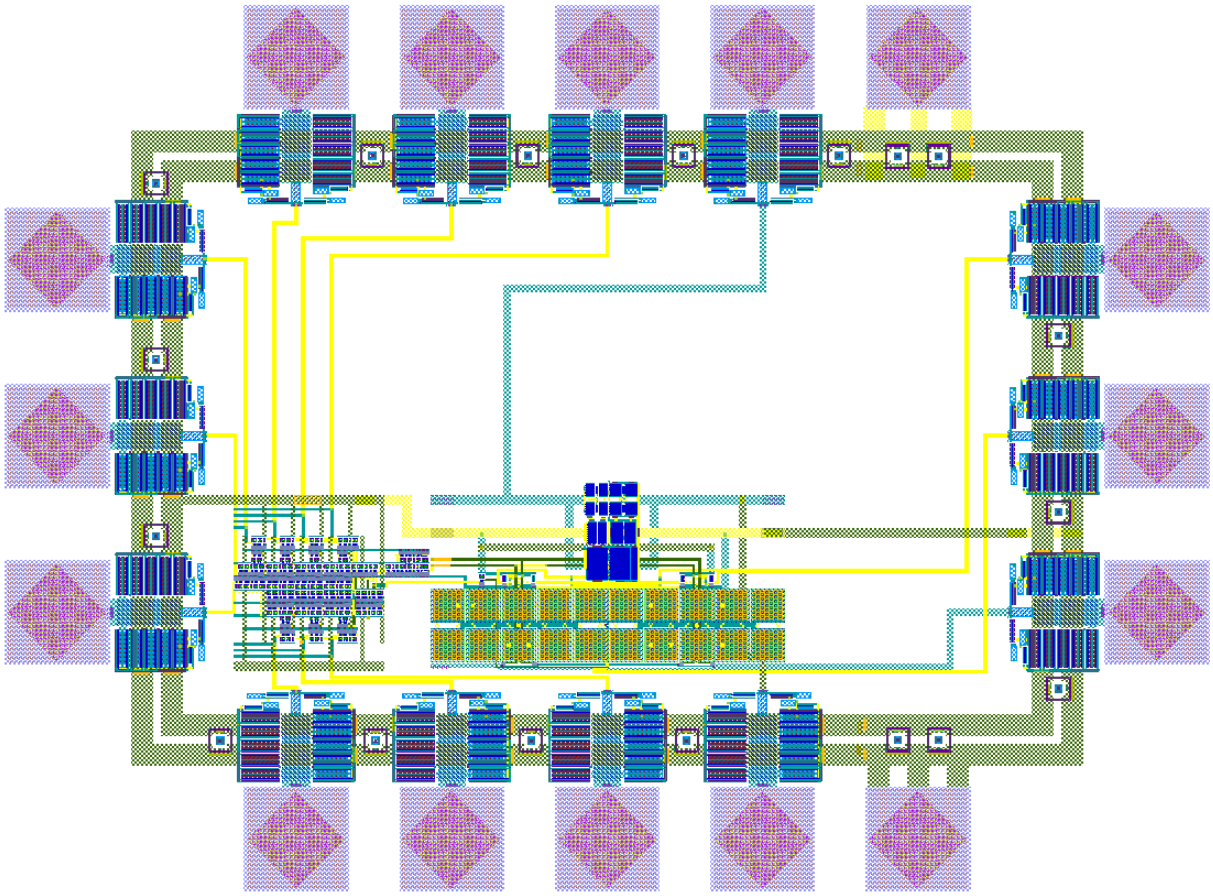


Fig. 5.12. DAC layout with no voltage reference, with pads, and interconnect.

5.3.4 DAC with Voltage Reference

Fig. 5.13 shows the layout of the entire system with the voltage reference and pads. Its aspect ratio is 1,008 µm × 852 µm.

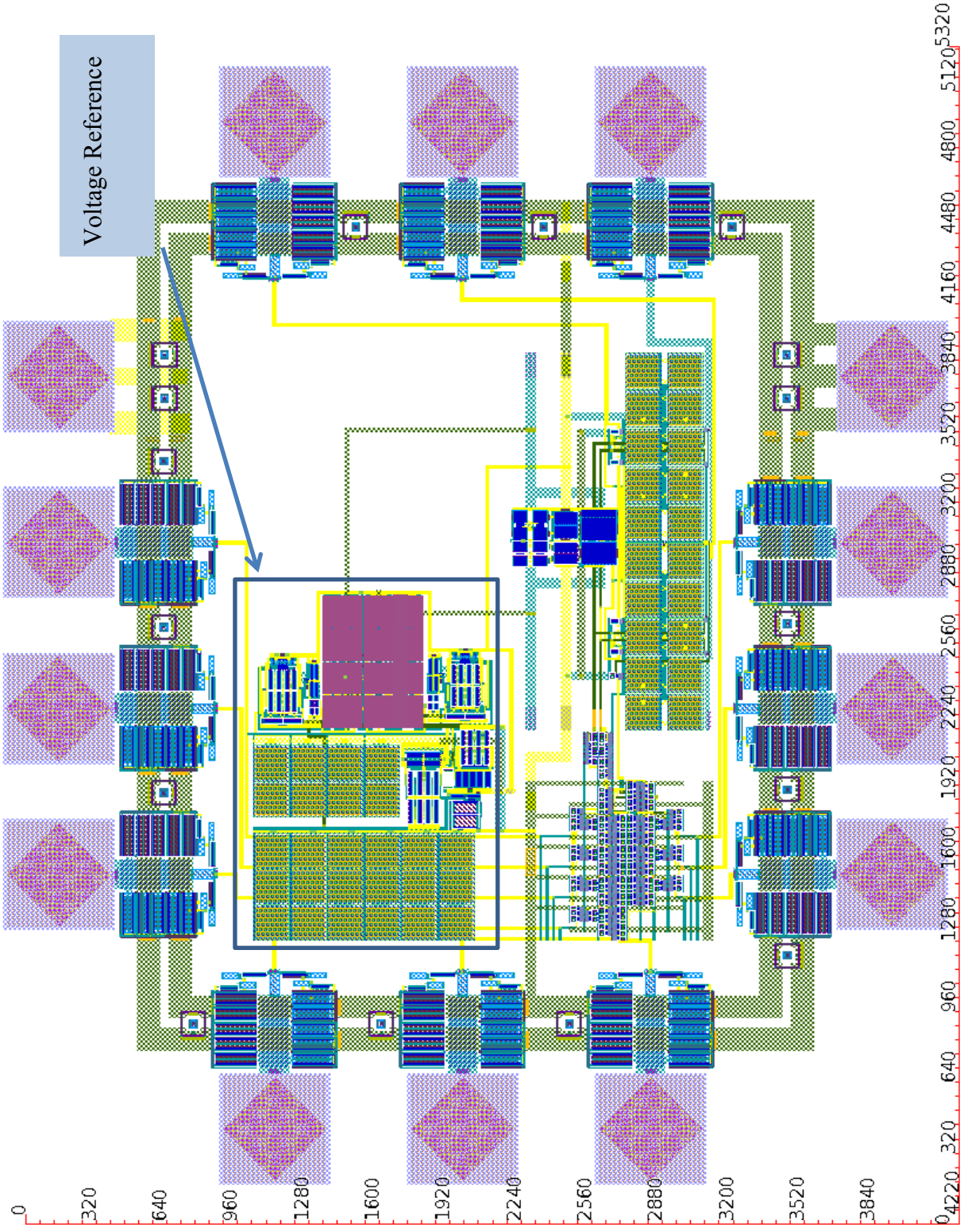


Fig. 5.13. DAC layout with voltage reference, pad ring, and interconnect.

CHAPTER 6 – VERIFICATION AND TESTING

Verification of the physical design is necessary before tape-out can occur. This is also the next step in the "V" diagram, highlighted in Fig. 6.1. This process utilizes layout verification tools such as DRC, LVS and PEX.

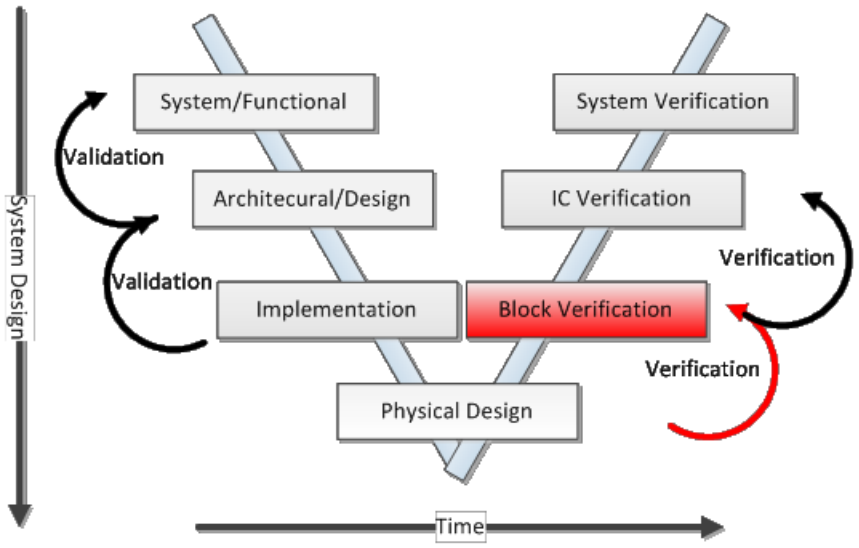


Fig. 6.1. V diagram with verification of physical design highlighted.

Parasitic simulation was only available on the TSMC run due to access to the GDSII. Fig. 6.2 shows the parasitic simulation of the full scale ramp output. The simulation results verify working physical design based on the models given. The parasitic simulation has a lower slope as compared to the schematic only simulation. The change in slope occurs when parasitics are considered in the DAC due to a non-ideal "stepping" of the output. This circuit is heavily dependent on symmetry. In addition; it is also charged based. If non symmetrical charging paths are seen by the op-amp due to parasitics, it can cause the step to miss and therefore be off the ideal slope for the remainder of the ramp. Fig. 6.3 is a close up of the two outputs; in order to observe this effect. This slope can be changed in real time and will be available off chip for

testing. The output ramps to 4 V in the same time the schematic simulation ramps to 4.3 V. This result verifies operation.

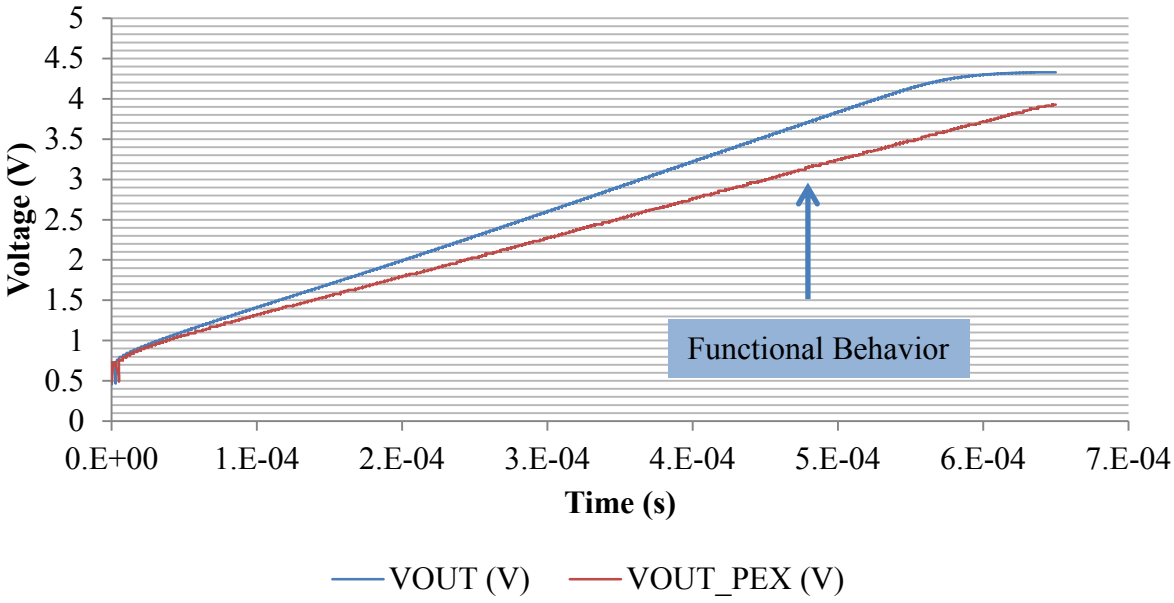


Fig. 6.2. PEX simulation results of DAC output showing basic functional behavior.

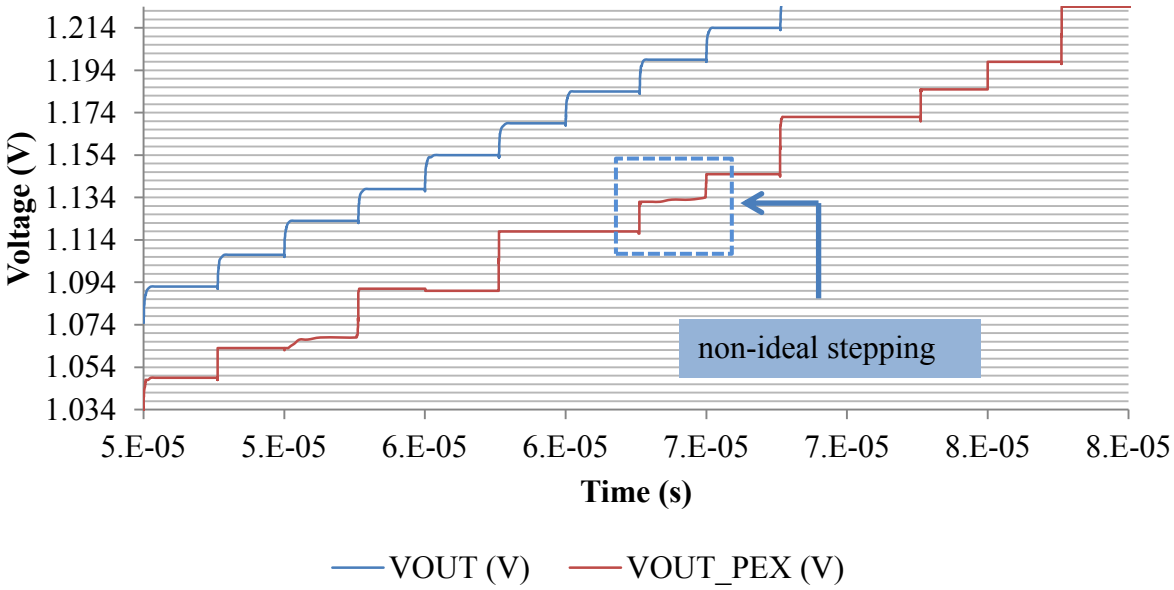


Fig. 6.3. Close up of DAC output with and without PEX.

Physical design verification was successful and the layout was sent for fabrication. Upon return of the IC, bench top testing was performed. This is the next progression in the "V" diagram, highlighted in Fig. 6.4.

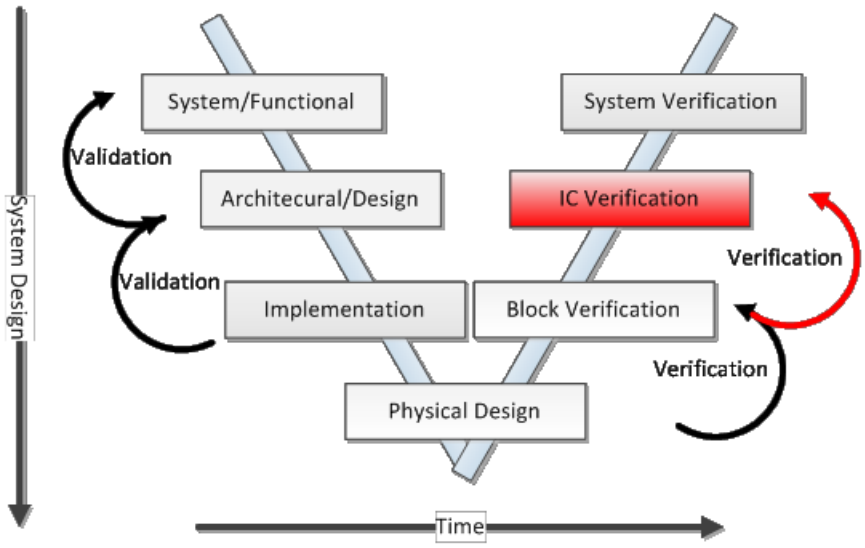


Fig. 6.4. V diagram with verification of IC highlighted.

Two rounds of testing were performed for the two different designs. As mentioned previously, Ridgetop Group constructed the physical design for the XFAB version. Only one die was delivered to the U of A for testing. The TSMC version has multiple versions of the DAC in segmented sections for better verification. Both will be presented in sequential order.

6.1 XFAB Testing

A printed circuit board was constructed to test this version of the DAC. This test board is designed to supply all the necessary voltage reference, as well as the digital code to the DAC. It has input pins for the clock signal and the reset signal. Testing of the XFAB DAC was performed on the bench in the MSCAD lab at the Cato Springs Research Center. Fig. 6.5 shows the test bench setup.

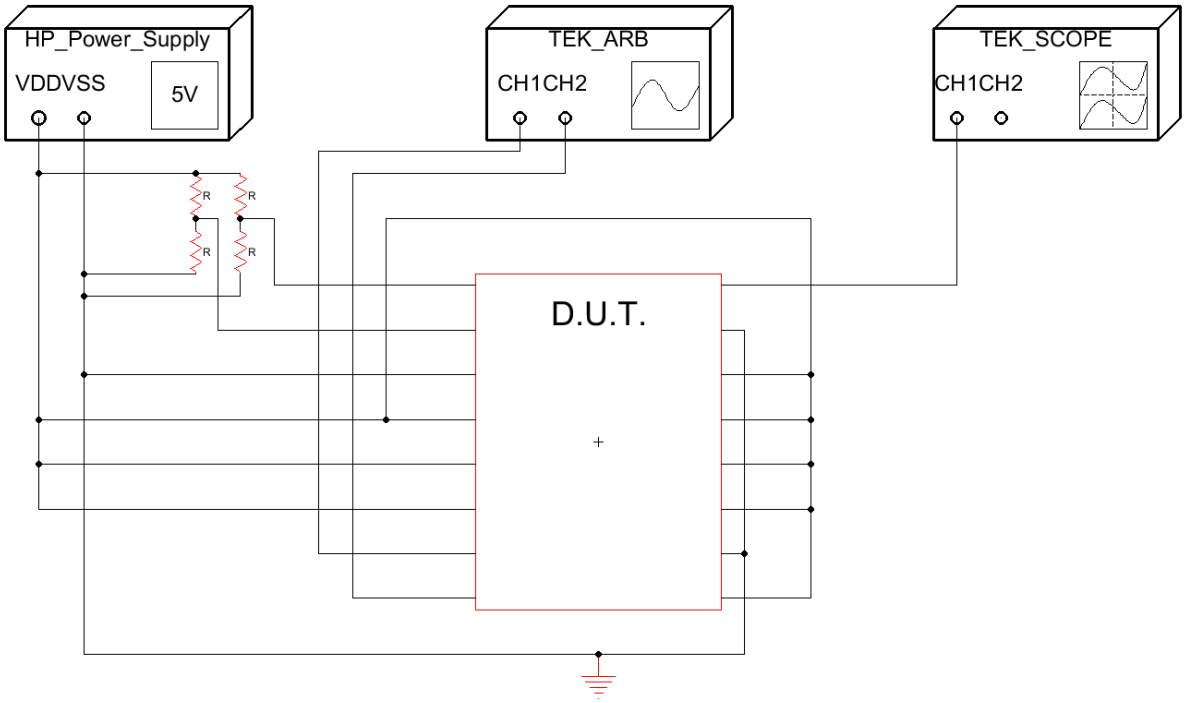


Fig. 6.5. Bench top test setup model for the device under test.

The device under test represents the PCB. The PCB was designed in EAGLE [16]. The schematic design of this PCB can be seen in Fig. 6.6. The layout was also executed in Eagle. The Gerber files were submitted to Advanced Circuits for fabrication.

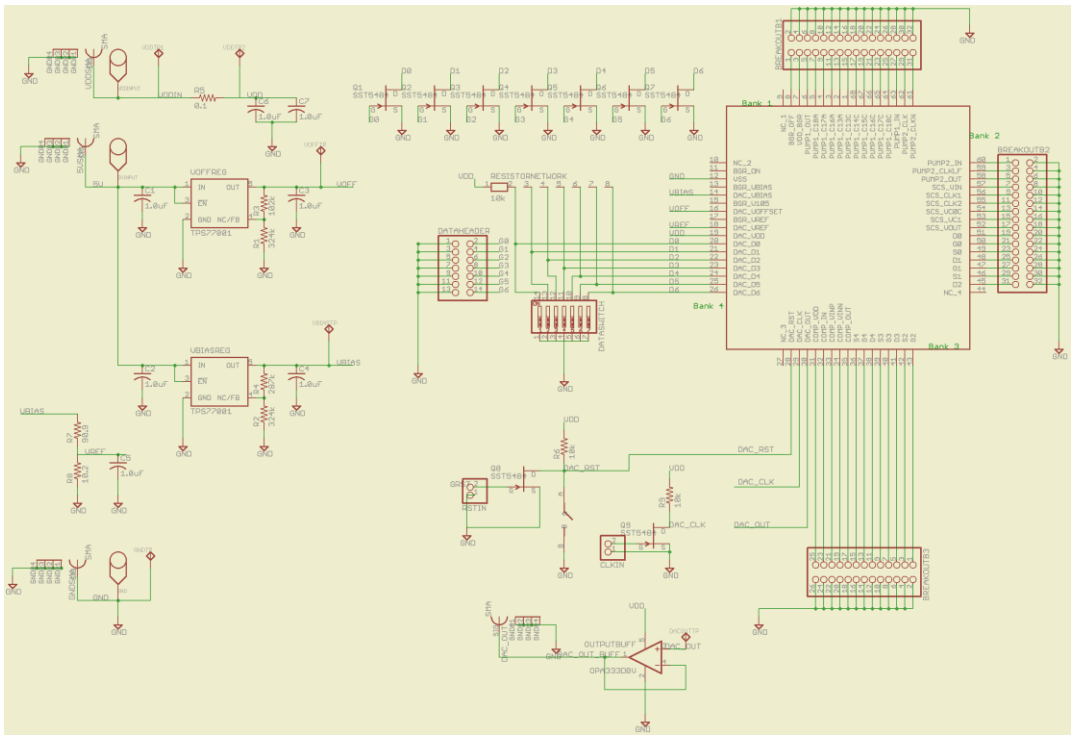
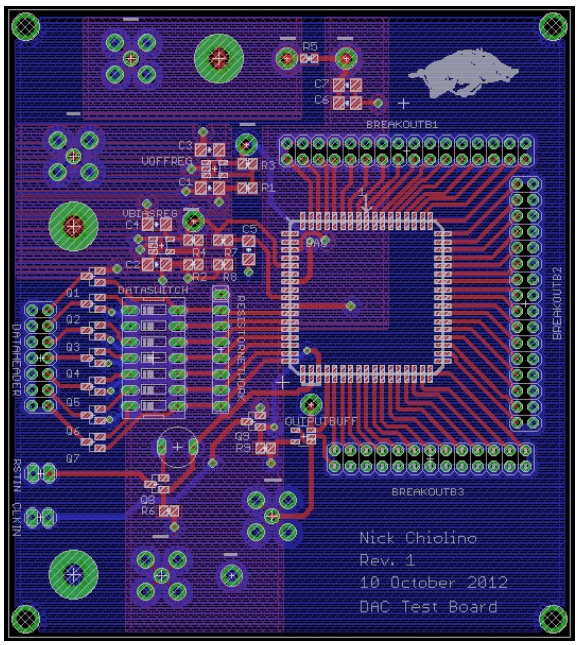
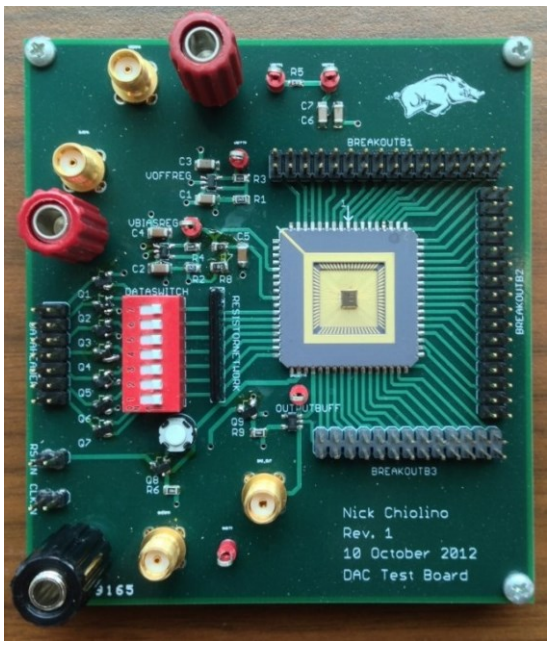


Fig. 6.6. XFAB PCB schematic from eagle.

The physical layout and the final board of this schematic can be seen in **(a)** **(b)** Fig. 6.7 (a) (b).





(a) **(b)**

Fig. 6.7. (a) XFAB PCB layout. (b) XFAB fabricated PCB.

As seen, this PCB is a four layer design. It utilizes proper power and ground plans with the added benefit of top and bottom routing. There are both surface mount and through hole elements. Power consumption is no higher than 100 mA and the majority of the signals needed are for DC biasing; larger than minimum traces were used due to this consideration. The maximum frequency will be no larger than 300 kHz so parasitics were of no concern. Anti-coupling capacitors where added on the output of each power source for removing power noise. Once the physical design of the board was completed, manufacturing was performed by Advanced Circuits. Assembly of the surface mount devices was performed at HiDEC in the assembly room at the engineering research park. The Sikama Falcon 5C was used to reflow the surface mount devices. The board was then powered up to confirm proper base line functionality.

6.1.1 Simulation Results

Simulations were run on the bench top for the XFAB version. The MSCAD lab has an automatic data capture system that uses a GPIB protocol with the aid of python code. Using this system the DAC was simulated over the full scale range. Fig. 6.8 shows the measured data from the DAC. As seen, the DAC ramps from 1.5 V to 15 V. The conversion time from simulation predicts that the DAC should output its FSR in 640 μs. The test results show the conversion time to be 50 ms. However, this simulation does verify functionality; demonstrating its ability to ramp from 1.5 V to 15 V.

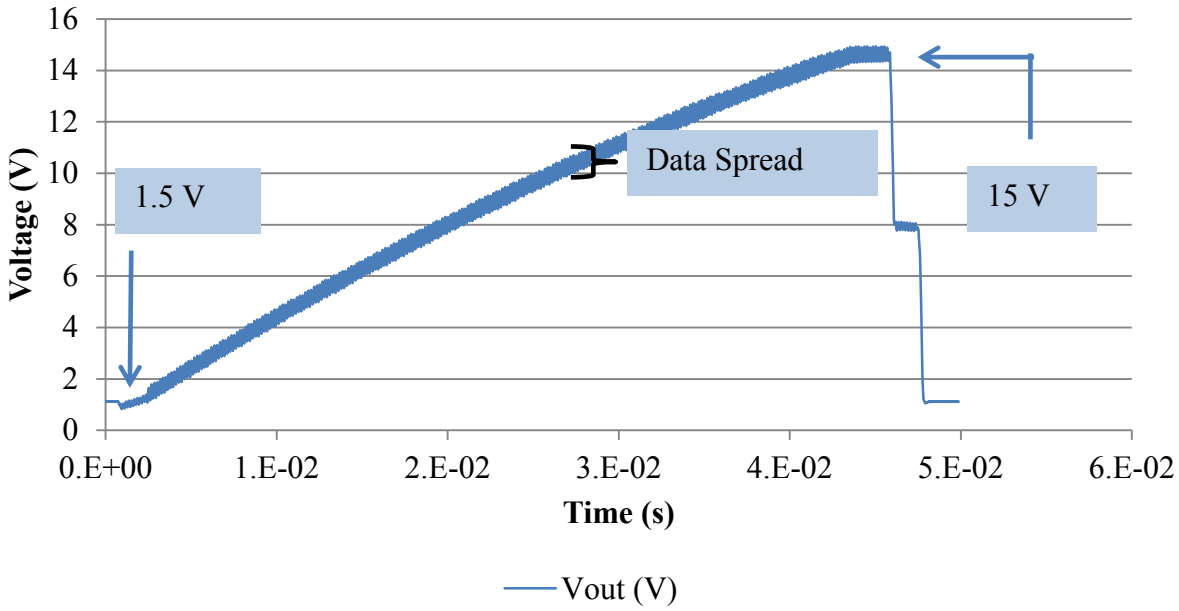


Fig. 6.8. Captured simulation of DAC's full scale ramp output from the XFAB process.

Zooming in on the graph in Fig. 6.8 generates the graph in Fig. 6.9. The output shows that the DAC is not holding a flat plateau increase from the previous 105 mV to the next 105 mV increment. The voltage is finding a path to either ground to a lower voltage. This could be attributed to one of two things; either the output is being tied to ground or the non-over lapping clocks are in fact overlapping therefore shorting each phase to ground temporarily. In fact, the D-type flip-flop cells, which generate the feedback for the non-overlapping clock, that were designed and validated for this architecture where not used for the physical design. The D-type flip-flop is NAND gate based and uses the S-R latch feedback to ensure non-overlapping behavior, if a minimum delay D-type flip flop was used, it could potentially switch logic before the next clock phase in the core.

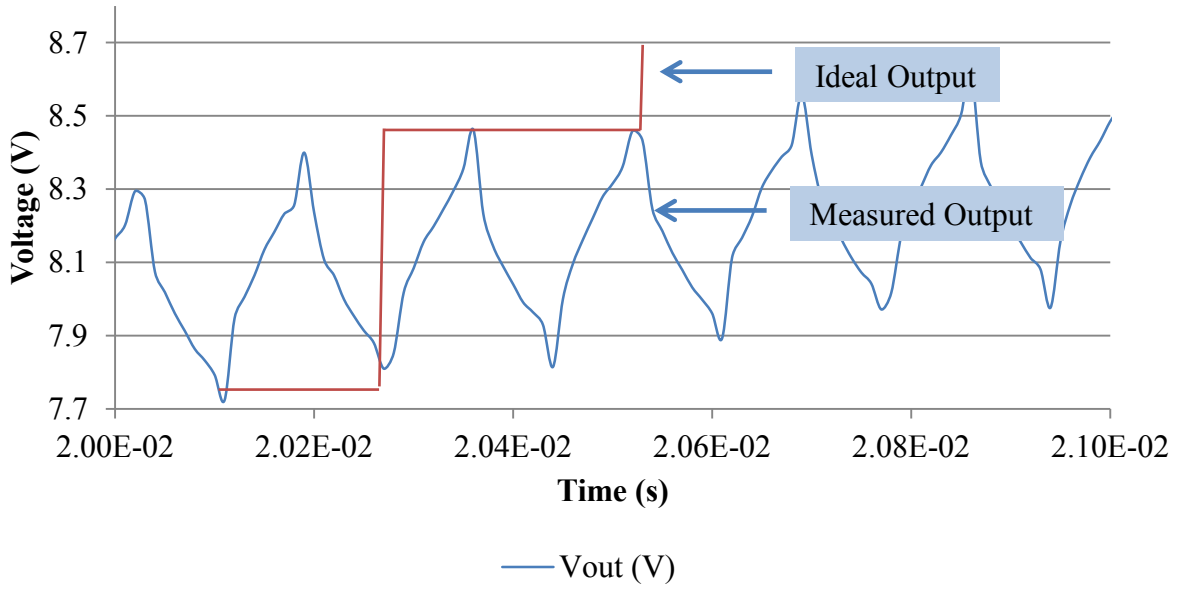


Fig. 6.9. Simulated results of DAC output with no dead-time.

Fig. 6.10 shows the ability of the DAC to ramp to a power supply that is lower than the requested digital input. The graph shows the output ramping linearly to a set power supply of 8.5 V.

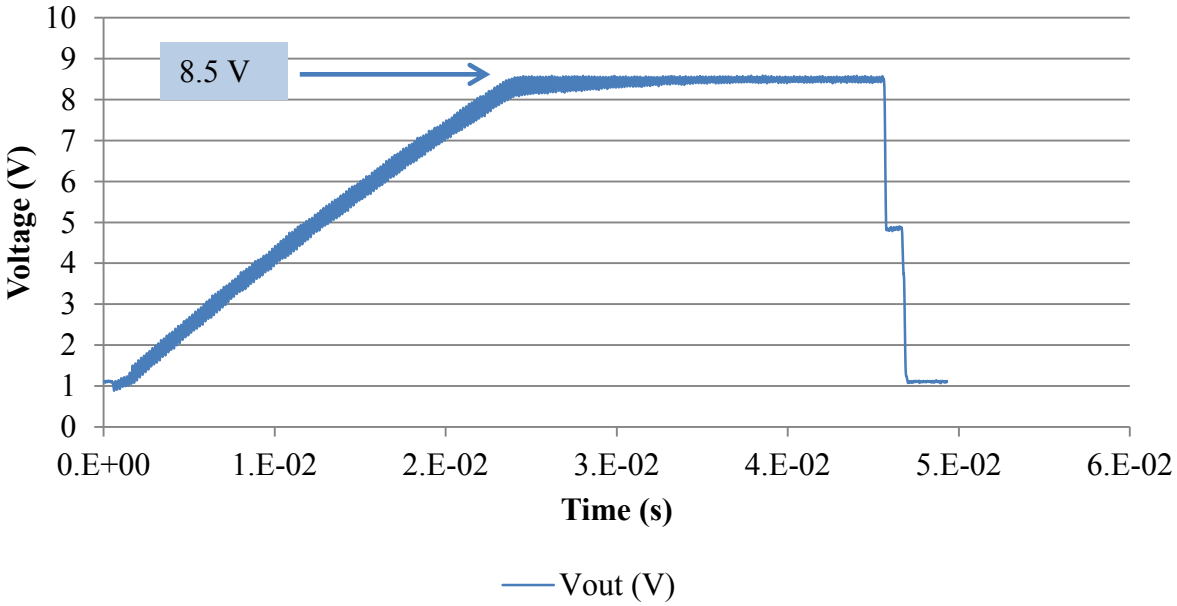


Fig. 6.10. Captured simulation of DAC's VDD cut-off output from the XFAB process.

6.2 TSMC Die Packaging

The physical design of the DAC was implemented on the same die as the electronics II project. The DAC was completed with its own pad ring. Upon arrival of the manufactured die, the DAC needed to be packaged for proper testing. The probe station could not be used due to probe tip limitations.

The DAC is a smaller component of the entire die that the U of A submitted to TSMC. Fig. 6.11 shows where the DAC is on the die. The die needed to be diced in order to package the part properly. The Kulicke & Soffa 982-10 dicing saw was used. The red lines show where the die was diced.

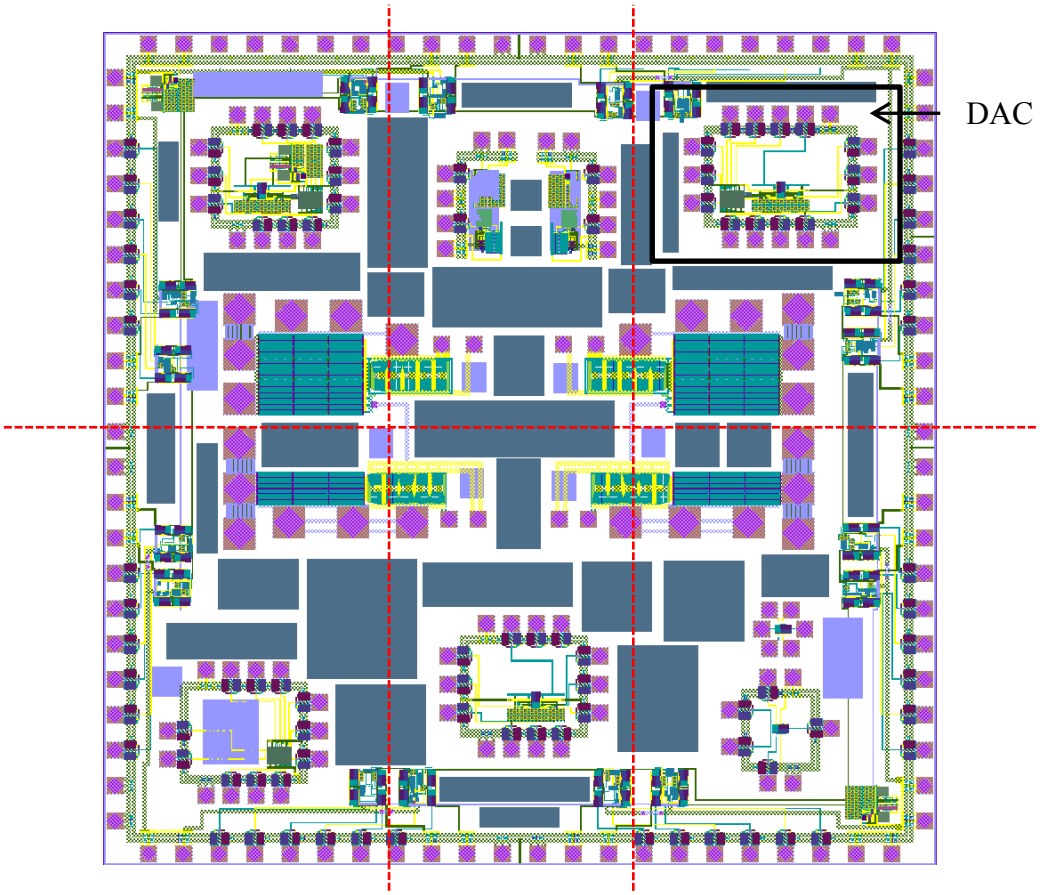


Fig. 6.11. Layout of entire TSMC die with the DAC highlighted.

Fig. 6.12 shows the die after dicing.

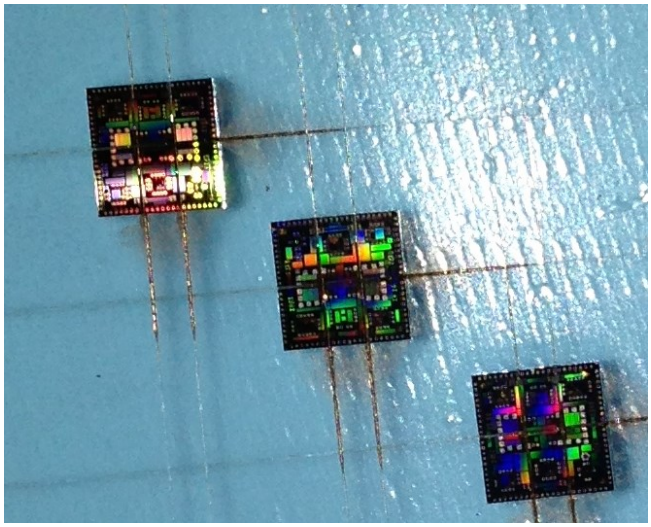


Fig. 6.12. TSMC die diced for DAC layouts.

After the die was diced it was attached to a 16 pin dual inline package. The die was attached to this package using the Fisher Isotemp Model 282 vacuum oven. The die, now in the package, needed to be bonded to the package pins. This was done using the Kulicke & Soffa 4700 wedge bonder. Fig. 6.13 shows the bonding diagram for the DAC.

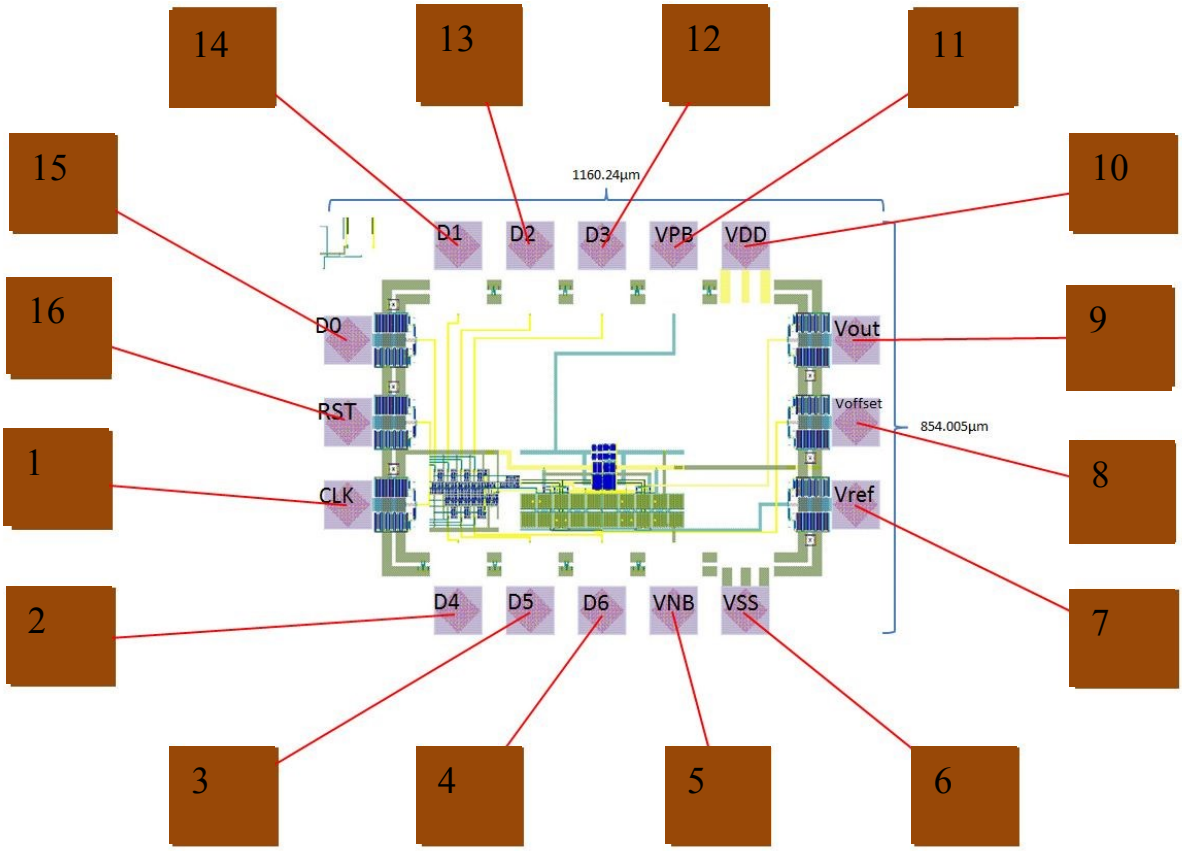


Fig. 6.13. DAC bonding diagram.

Fig. 6.14 shows the die after bonding.

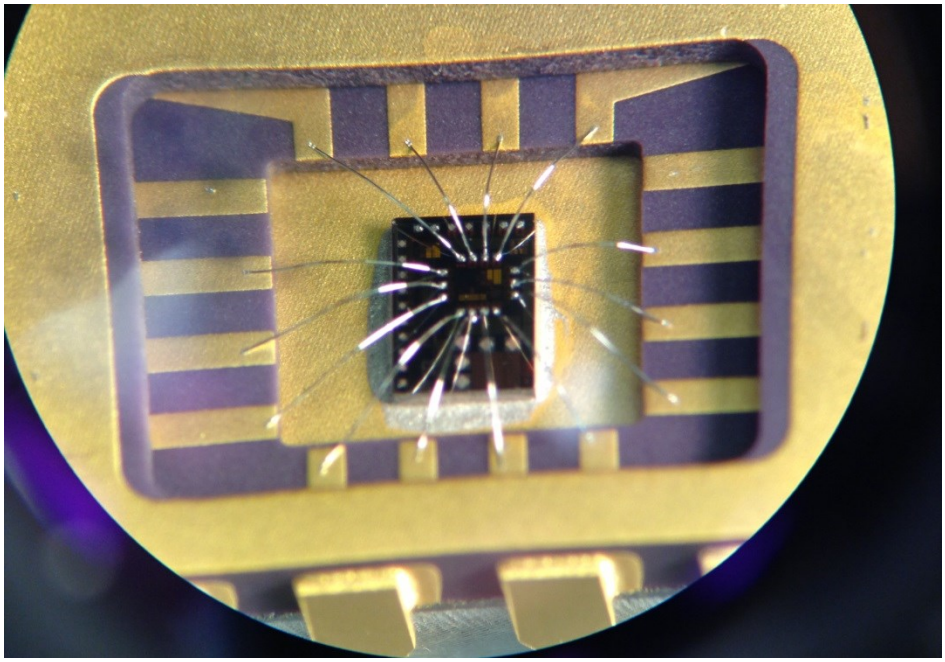


Fig. 6.14. Bonded TSMC die viewed through microscope.

The die is attached and bonded to the package and ready for testing.

6.3 TSMC Testing

As mentioned previously, the physical layout of the TSMC version was performed by the U of A. The DAC was designed and laid out for maximum flexibility for testing. All the voltage references needed for the internal op-amp and the DAC itself are generated off chip. This allows the user to observe its behavior if debugging is necessary. A PCB was designed for testing the DAC. The test setup for bench top testing can be seen in Fig. 6.15.

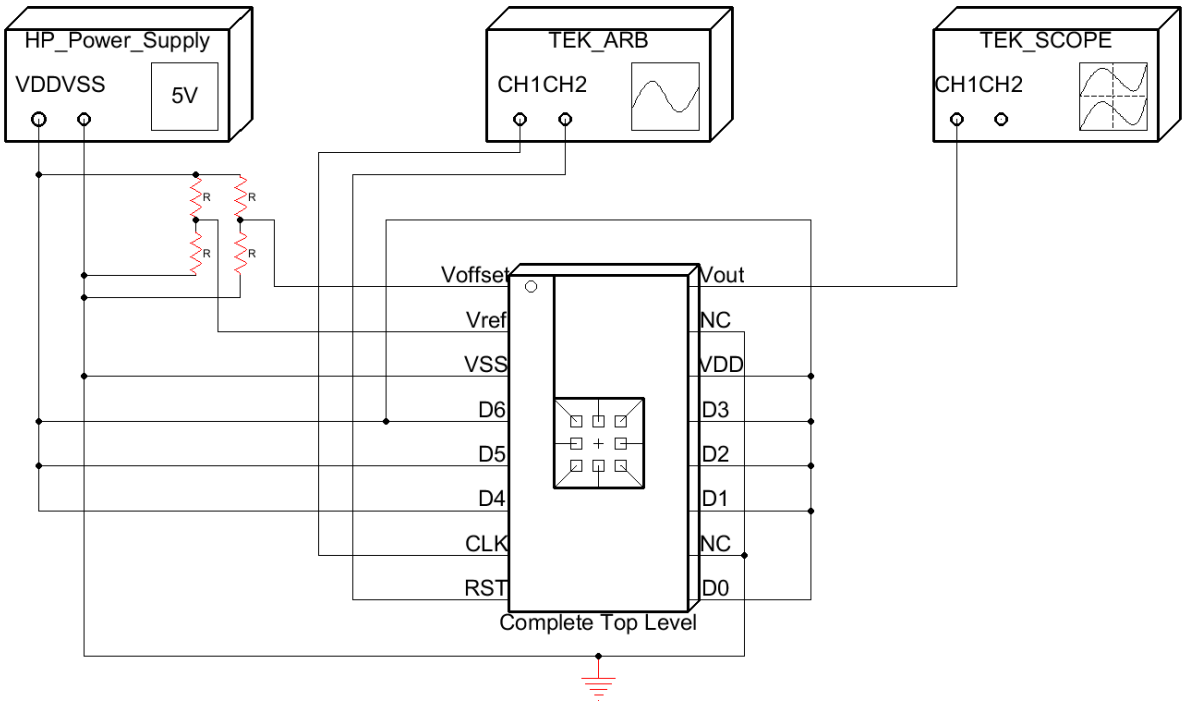


Fig. 6.15. TSMC bench top test setup model for the DAC.

The PCB was constructed and laid out in Eagle PCB editor. It was then submitted to Advanced Circuits for manufacturing. The schematic for the PCB can be seen in Fig. 6.16.

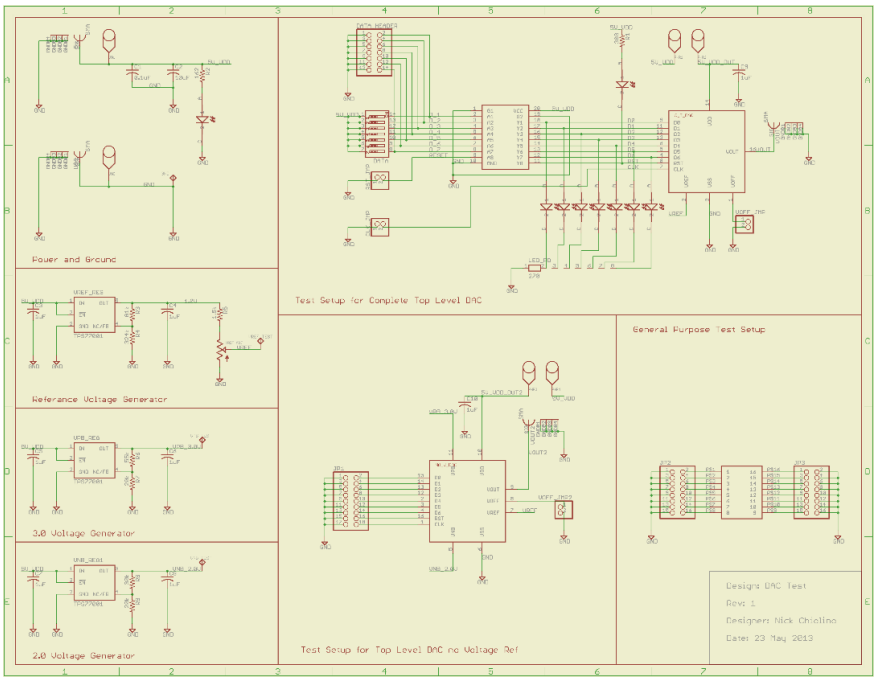
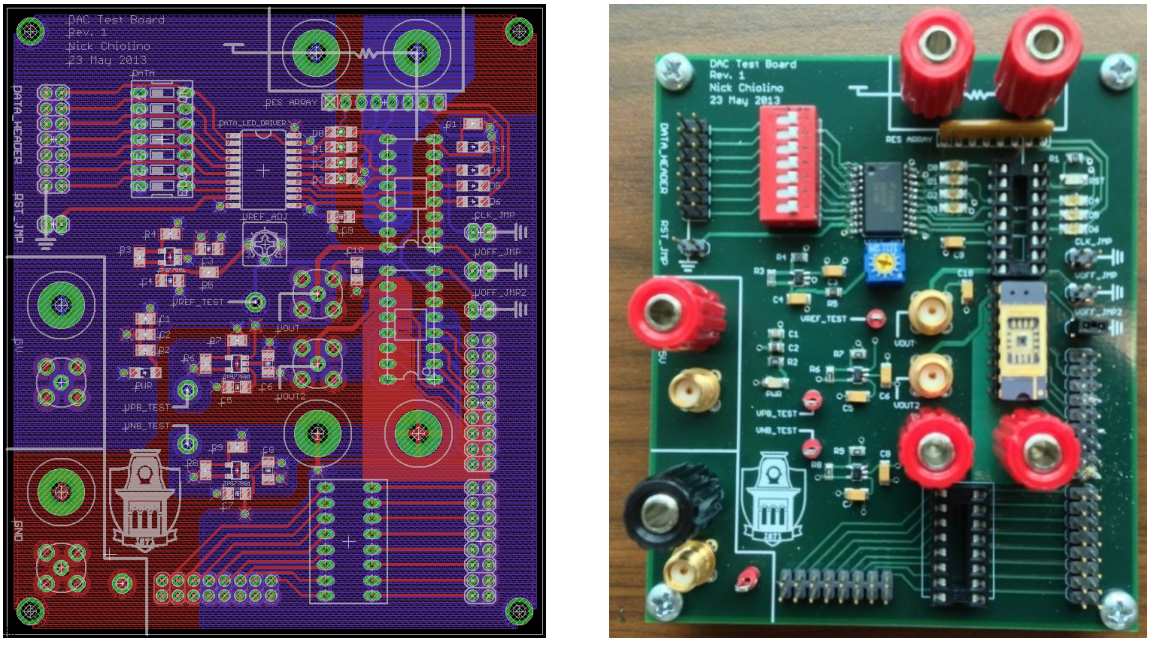


Fig. 6.16. PCB schematic for the TSMC test board.

The physical layout of the PCB can be seen in **(a)** **(b)** Fig. 6.17 (a) and (b).



(a) **(b)**

Fig. 6.17. (a) PCB layout. (b) Fabricated PCB.

This PCB is a four layer design utilizing best practices for proper ground and power plan, with the added benefit of top and bottom signal routing. It is equipped with evaluation feedback, such as power on LED's, and current monitoring capability. There are both surface mount and through hole devices. The surface mount parts where attached and re-flowed at HiDEC using the Sikama Falcon 5C. The through hole devices where completed at the MSCAD lab using a soldering iron. Once completed, the DAC was testing on the bench.

6.3.1 TSMC Simulation Results

The DAC was testing over the three main criteria to be verified in accordance to the original specifications. These three criteria are: full scale ramp, power supply saturation, and binary match. Fig. 6.18 shows the DAC results for the full scale ramp. Due to the output range of the op-amp, the DACs starting point, based on design and simulation, is around 0.7 V and up to 4.3 V. The bench top test confirms this behavior.

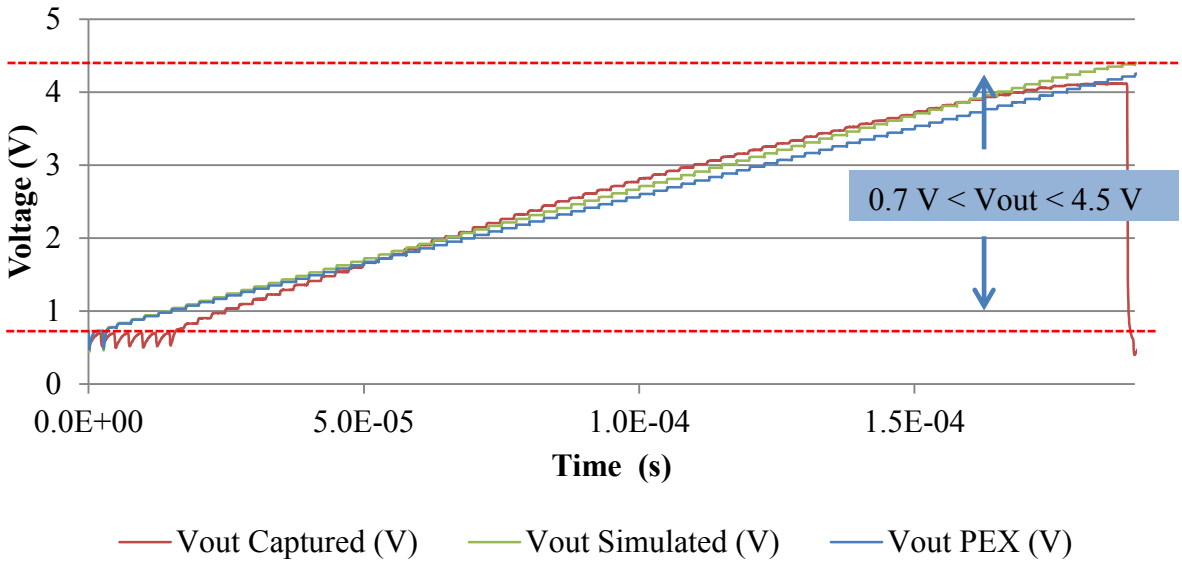


Fig. 6.18. Captured full scale ramp output of the TSMC DAC.

Fig. 6.19 shows the test results of the DACs ability to match a binary input. The parallel digital input was set to (0000111) = 7 * 0.23 V = 1.61 V.

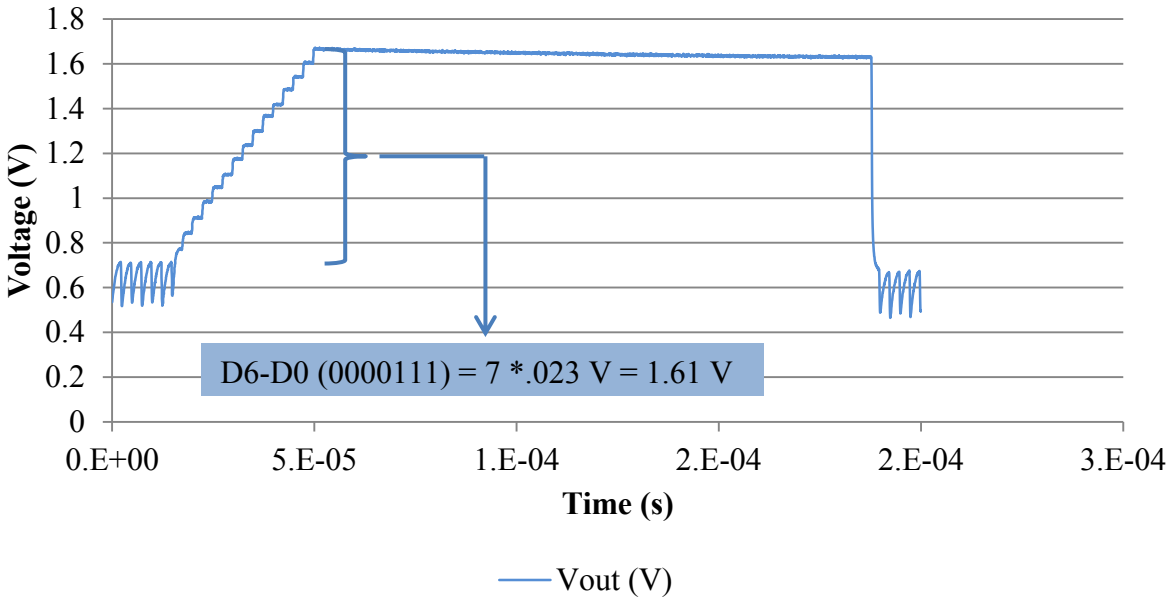


Fig. 6.19. Captured output of the DAC's binary match in the TSMC process.

Fig. 6.20 shows the test results of the DACs ability to ramp to the power supply when the binary input exceeds the power supply. One of the operations the DAC must perform is to ramp to an undetermined, lower, voltage in order to simulate the voltage of a battery dropping. In this simulation an arbitrary voltage of 2.3 is chosen in order to verify this operation. Simulations with the models provided by the foundry did not predict a monotonic transfer of data up to a lower voltage. This can be seen in Fig. 4.23. However, testing shows its ability to ramp to a 2.3 V power supply.

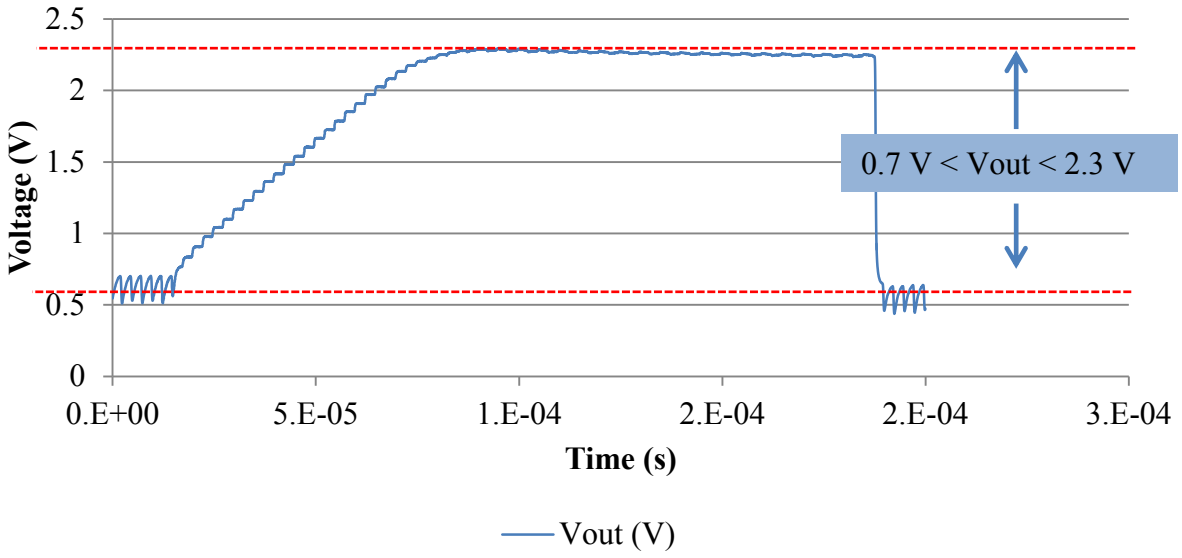


Fig. 6.20. Captured output of the DAC's VDD cut-off in the TSMC process.

6.4 Temperature Testing

6.4.1 TSMC Results

Bench top temperature testing was performed using a liquid nitrogen tank in combination with a Delta 9039 environmental chamber. The DAC was verified operational in the oven at room temperature before temperature testing began. Once, verified the change in temperature was the only independent variable throughout the entirety of the test. Fig. 6.21 shows the bench top test setup for temperature testing. The items labeled in the figure are (1) the liquid nitrogen tank and (2) the delta environmental oven and (3) the Tektronix scope probe and (4) the Tektronix function generator and (5) the Hameg quad power supply, and (6) the PC used for data capture.

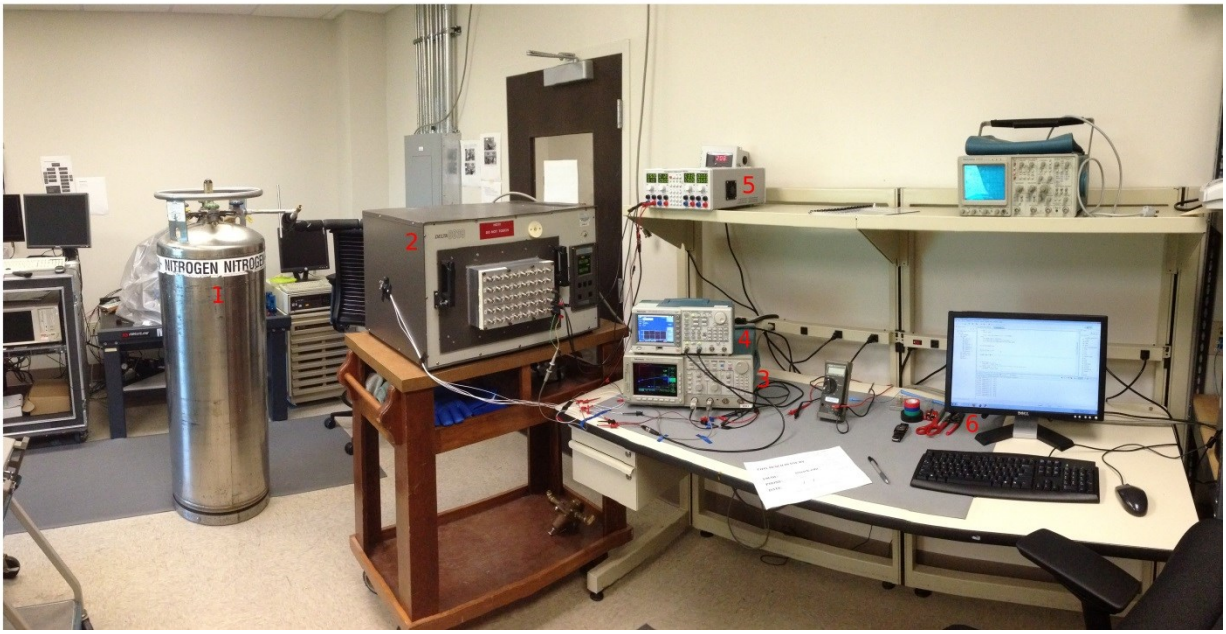


Fig. 6.21. Bench top test setup for temperature testing.

The TSMC version of the DAC was not designed to operate over the extended temperature range of the XFAB version. However, simulation results show that the TSMC version is fully functional for industrial grade. This operating condition is a result of the main analog component, the op-amp. Fig. 6.22 shows the minimum and maximum output range of the op-amp over temperature. This is directly related to the minimum and maximum output range of a full scale ramp for the DAC.

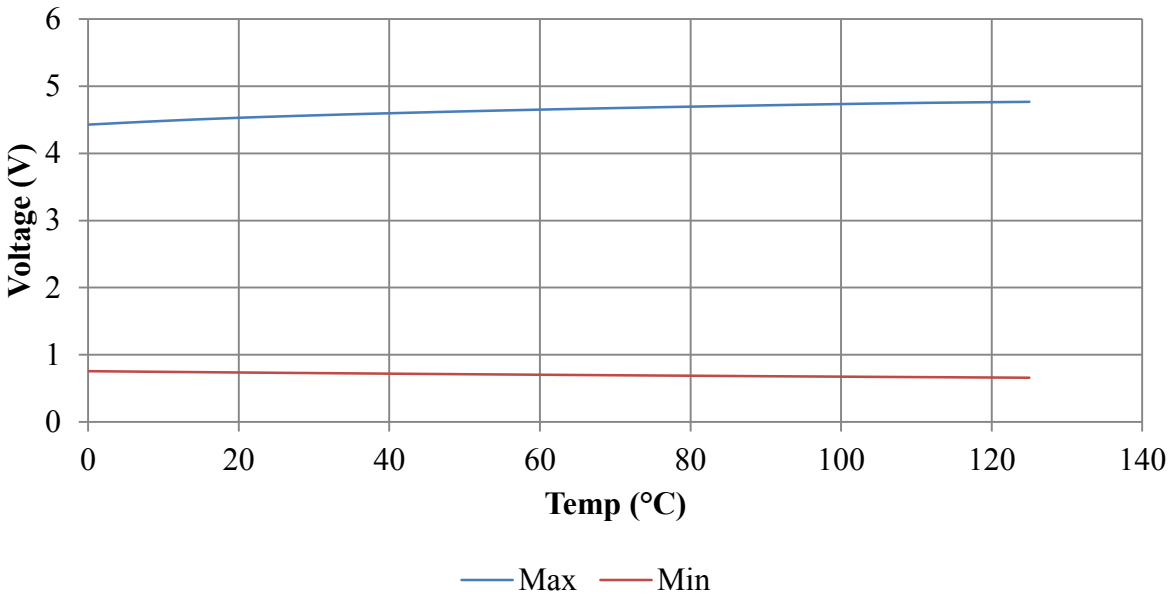


Fig. 6.22. Simulation of minimum and maximum output range of op-amp over temperature.

Bench top temperature testing was performed on the TSMC version. Functionality is verified with a full scale ramp, therefore, only this simulation is necessary to support operation. The DAC was swept over a temperature range of -125° C to 85° C. Fig. 6.23 shows the full scale output over all 128 steps.

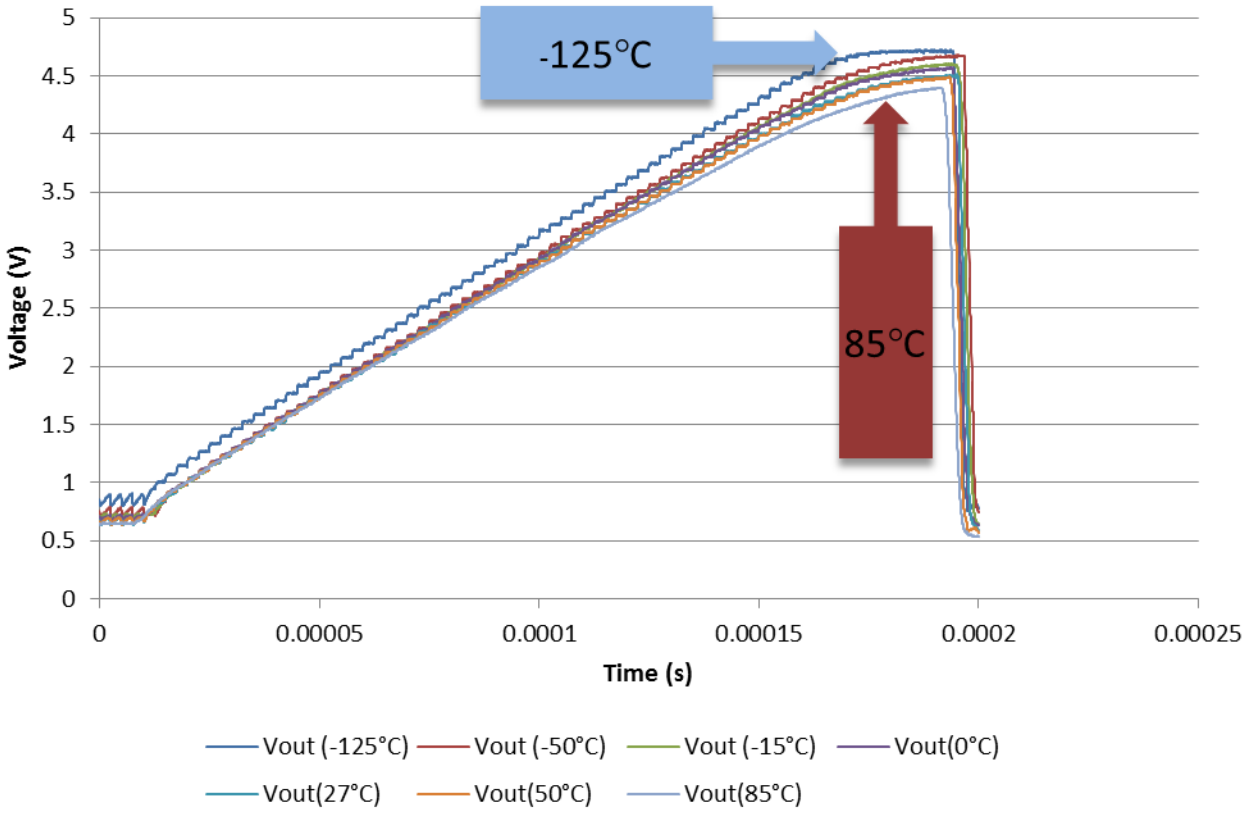


Fig. 6.23. Simulation of DAC over temperature (FSR).

The captured results show the DAC's output improving with lower temperatures. This is due to thresholds in the gates dropping therefore generating a better transfer of data from the previous "step." There is a major threshold shift at -125° C leading to an overall shift in that particular output capture. In order to interpret this data more clearly Fig. 6.24 illustrates the trend of the DAC output over temperature for is lowest, middle, and highest outputs. The shift in the minimum starting voltage is dominated by the thresholds of the op-amp. The decrease in maximum output is dominated by the maximum output voltage of the op-amp. Finally, the median demonstrates the trend in voltage over temperature at a point of ideal biasing for the op-amp.

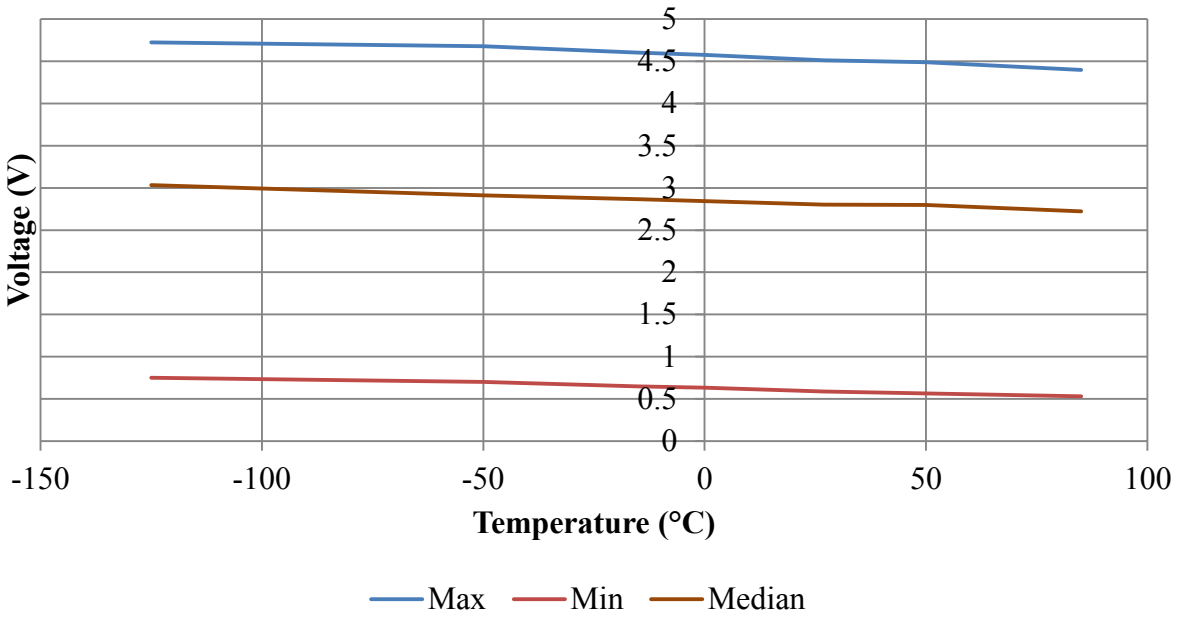


Fig. 6.24. Measured results of minimum, maximum, and median of the DAC output over temperature.

CHAPTER 7 – APPLICATIONS

The designed digital to analog system has extensive application areas, especially in low power. And these areas could be extended with different processes. The DAC is based on a charge pump system, therefore, any process with the capabilities to have capacitors can use these designs. The application that this design, in particular, was used in was for battery monitoring.

7.1 Full System Application

As mentioned in the introduction, the application of the full system is for low power battery monitoring for mobile backpack units. The goal is to monitor the battery voltage in order to make the user aware of how much power is left in his/her mobile unit. This will alert the user of how much time he/she has before running out of power. The battery monitoring system must be low power as to not draw significant power itself for monitoring the battery. The system diagram is shown in Fig. 7.2. It is important to note that the final step in the "V" diagram, system verification, would be implemented with this system. This step is highlighted in Fig. 7.1.

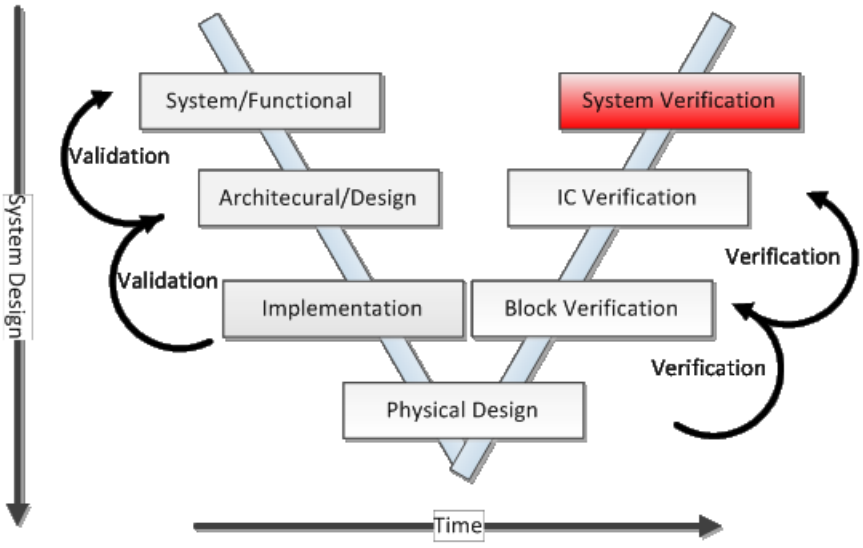


Fig. 7.1. V diagram with system verification highlighted.

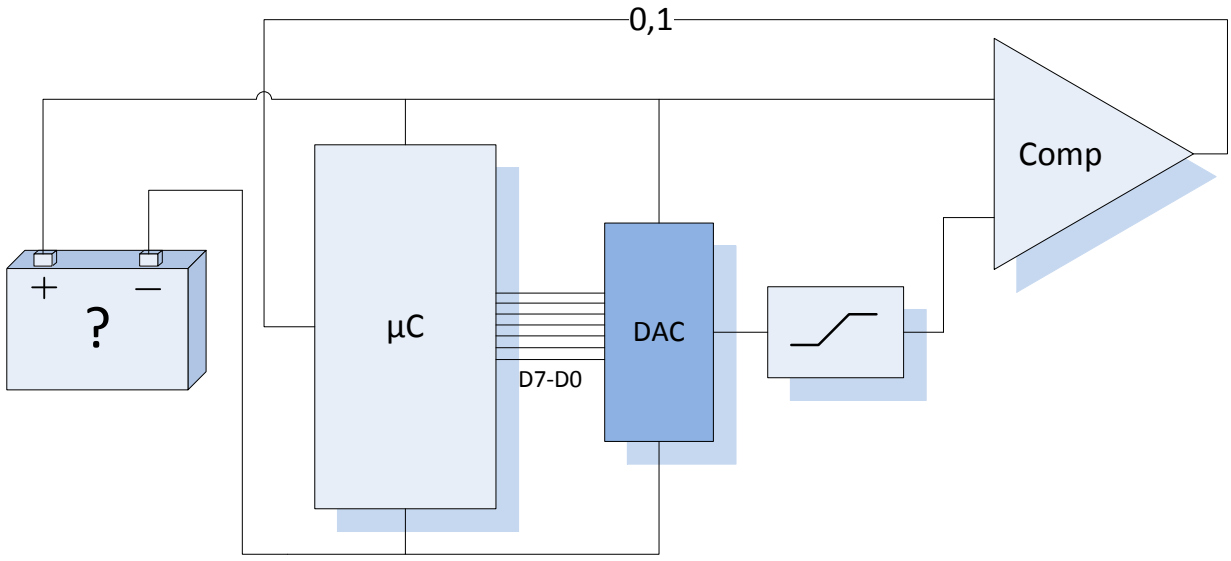


Fig. 7.2. Full system application schematic.

As seen, one input to the comparator is tied to the voltage of the battery and the other is tied to the DAC. The DAC simply acts as a ramp generator that continually cycles through its code until the comparator senses a match. Once this match occurs, the system now knows what the battery voltage is by looking at the step in the code when the match occurred. It is a cyclic system that runs at 200 kHz. Fig. 7.2 illustrates the entire system with the DAC highlighted in the center.

CHAPTER 8 – SUMMARY AND CONCLUSIONS

The UA was approached by Ridgetop Group in the fall of 2011 for consulting on a SBIR phase II. This phase II described a system that monitors battery voltage on mobile units. Ridgetop Group needed the University to design an element inside this system. This element was a 7-bit parallel digital to analog converter. Its unique set of specifications required an innovative design. These specifications can be seen in Table 1.1. One very important obstacle to this DAC is a changing power supply. The power supply that needs to be monitored, also powers the system. Without a reliable power supply, a new approach had to be adopted.

8.1 The Top Down Approach

Creating a working system that is novel from the device level is a difficult task. If a known design procedure has not been developed from the device level to aid the designer; it can seem nearly impossible. The top down approach is a method of design which progresses the designer down levels of abstraction to arrive at a working system at the device level. The designer starts with the most basic understanding, or more dominating variables of the system, to understand the inner working of the initial design. As the designer confirms the systems operation during this progression, he/she inherently creates higher fidelity models to be used in the system. Once the designer has increased the level of abstraction down to the physical design; each discrete element is integrated one level at a time and compared to the model to confirm its initial design. This approach was adopted for the design of the DAC.

8.2 Same Design; Two Processes

This design was implemented in two different processes. The XFAB process used wide voltage devices. The TSMC process used typical power supply range devices. The design and simulation of the two were both done by the UA. The XFAB version was laid out by Ridgetop

Group and the TSMC version was laid out by the UA. The two versions were delivered to the UA for testing. Testing was completed and confirmed that the design works across multiple processes, supporting the top down approach as a viable and beneficial tool for design. It is a testimony to the architecture of the DAC and confirmation that if higher level model confirmation is solid, device level variables can be interchangeable.

8.3 Packaging

The TSMC version of the DAC was delivered to the UA in wafer form from TSMC. The die that were received, however, needed to be sub-diced and packaged for testing. The die was successfully diced, attached to a package, bonded, and integrated into a PCB. Testing on the bench confirmed the operation of the DAC. The only element of the design that was not processed by the UA was the fabrication and processing of the wafer.

8.4 Future Work

Integration into the entire system would be the next step in the process. In accordance to the top down model approach, a model test bench of the entire system would be implemented in order to compare the ideal model with the results from the IC.

As it pertains to the DAC, an op-amp with self-biasing and more gain would be among the list of improvements along with smaller, faster digital logic to increase the operating frequency [17]. This DAC could be implemented in an exotic process, such as silicon carbide in order to gain attributes such as ultra-wide temperature ranges [18]. The features the DAC would gain depending on the process would target it towards different applications such as high speed digital or space applications. If low power was not a concern it could be made more robust with error amplifiers and resistor biasing. A bipolar CMOS process would open opportunities for greater drive strength and speed.

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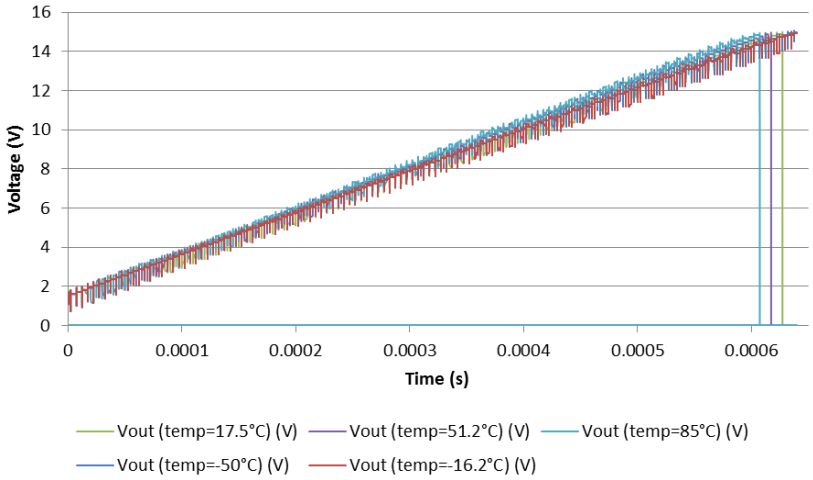
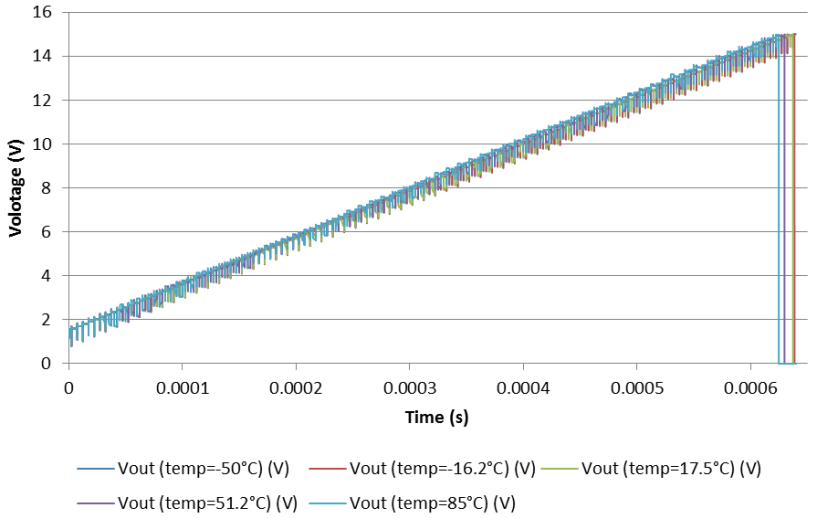
APPENDIX A

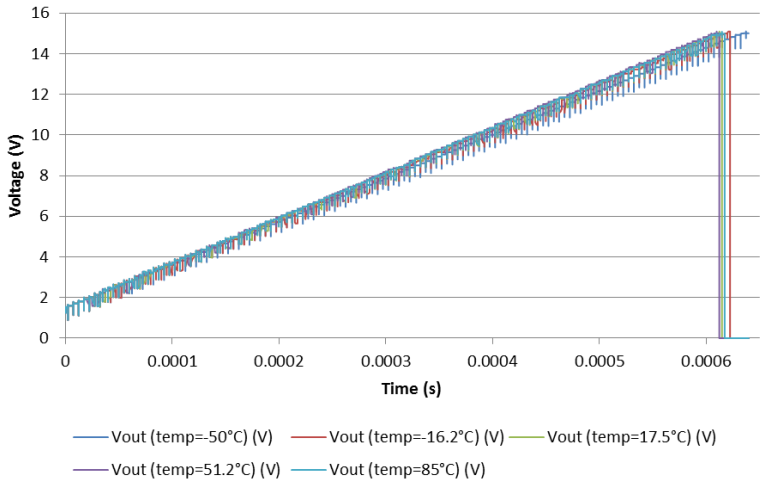
The process temperature range specified is -50° C to 85° C. The simulations are from the temperature models in the netlist. There are four corners that the DAC was simulated over. The simulations show ideal performance over the full scale ramp. The four corners wp, wz, ws, and wo and can be found in Fig. A.1.



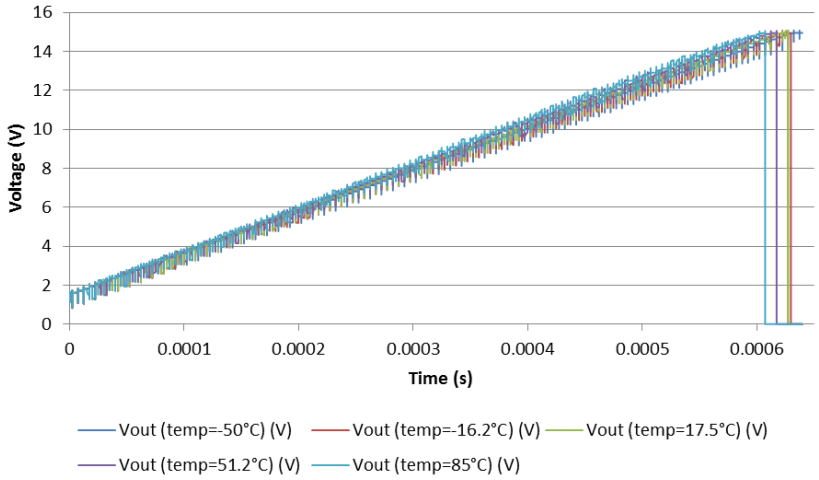
(a). Simulated results of the DAC's full scale ramp over temperature in the XFAB process with worst case power.



(b). Simulated results of the DAC's full scale ramp over temperature in the XFAB process with worst case zero.



(c). Simulated results of the DAC's full scale ramp over temperature in the XFAB process with worst case speed.



(d). Simulated results of the DAC's full scale ramp over temperature in the XFAB process with worst case one.

Fig. A.1. XFAB FSR All Corners WP(a), WZ(b), WS(c), WO(d)