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Modeling and Characterization of P-Type Silicon Carbide Gate Turn off Thyristors

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MODELING AND CHARACTERIZATION OF P-TYPE SILICON CARBIDE GATE TURN OF THYRISTORS

MODELING AND CHARACTERIZATION OF P-TYPE SILICON CARBIDE GATE TURN OF THYRISTORS

A dissertation submitted in partial fulfillment
of the requirements for the degree of
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ABSTRACT

Silicon carbide (SiC) power semiconductor devices have emerged in the past decade as the most promising technology for next generation power electronic applications ranging for electric vehicles to grid-connected power routing and conversion interfaces. Several devices have been developed, and even some have been released commercially, including diodes, MOSFETs, JFETs, thyristors, gate turn-off thyristors, and IGBTs. The model development, characterization and experimental validation of SiC p-type Gate Turn-off Thyristors (GTO) is presented in this work. The GTO device in this work is being used as part of a SiC-based solid-state fault current limiter under development at the University of Arkansas' National Center for Reliable Electric Power Transmission. The developed model is a level-3 physics-based model, that predicts on-state and switching behavior with high fidelity. The model also incorporates temperature effects of both a physical and empirical nature such that it will accurately predict device performances from 25 °C to +175 °C. Custom gate drivers and test configurations were designed to accurately characterize and test an 8 kV p-type SiC GTO provided by Cree. The measured data was used to validate the model's performance.

This dissertation is approved for recommendation
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Osama Shihadeh Saadeh

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Overview of Thyristors and GTOs

Thyristors are four-layer latching bipolar devices, which have the highest power handling capability of semiconductor devices available. They were first developed in the mid 1950s, but only commercially available in the mid 1960s [1, 2, 3]. This was primarily due to the lack of understanding of the device's behavior. Four layer devices latch up and a short trigger will cause the device to turn on, even if the trigger is removed. This type of behavior was not present in previous devices.

Fig. 1.1 below shows a simplified two dimensional structure of a thyristor.

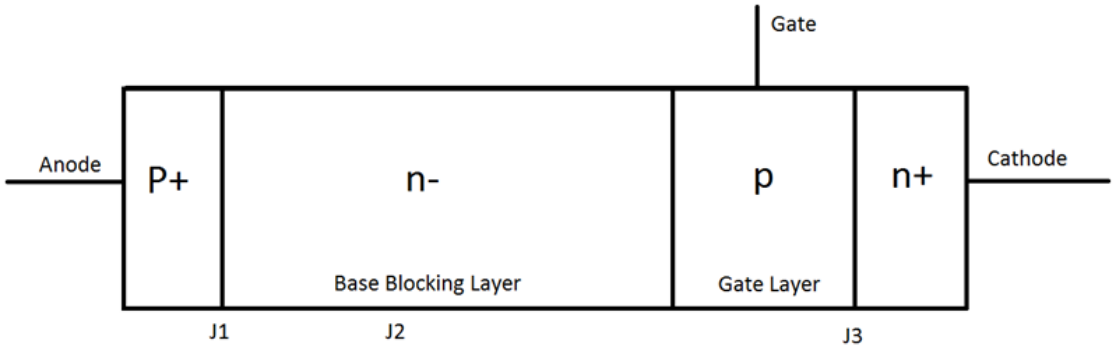

Fig. 1.1. A simplified two dimensional thyristor structure.

Thyristors are semi-controllable minority carrier devices that can turn on via a gating signal, but cannot be turned off directly via the gate signal. Auxiliary commutation circuits have been developed to add turn-off capability [3]. The problem with these circuits is that they are complex and bulky. Thyristors only block in the forward direction, requiring a series diode for reverse blocking. Due to the high rating and maturity of these devices, they have dominated applications that require high power and low switching speeds, such as motor drives and utility applications [1].

For lower current rating applications, thyristors are diced into small die that are individual packaged, usually in a stud package as shown in Fig. 1.2.

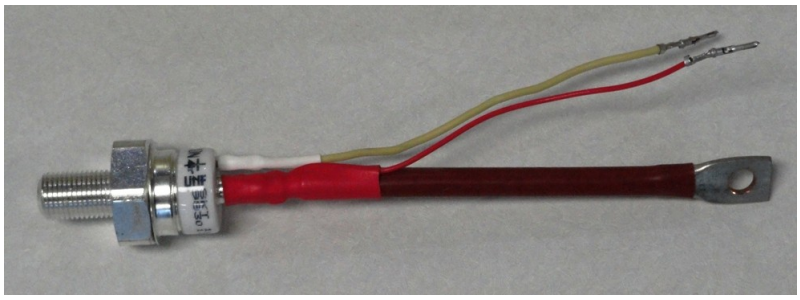

Fig. 1.2. Single stud GTO.

For higher current capabilities, thyristors can be fabricated on an entire wafer, and the wafer is packaged in a press pack as shown in Fig. 1.3.

Fig. 1.3. Press pack GTO

Since a thyristor is a four layer device, predicting its behavior in circuit applications can be non-trivial. Two bipolar junction transistors (BJT) connected in positive feedback configuration are used to clarify thyristor operation as shown in the sub-circuit in Fig. 1.4 [1, 2, 3].

The base of each of the transistors is connected to the collector of the other, so as long as the product $\beta 1 \cdot \beta 2 > 1$ (where β is the transistors current gain), once a small current is introduced to the gate the two transistors will drive each other into steady-state due to the positive feedback. Even if the original gate current is removed, the device will stay on. This operation of the thyristor demonstrates that it is a current controlled device [1, 2, 3].

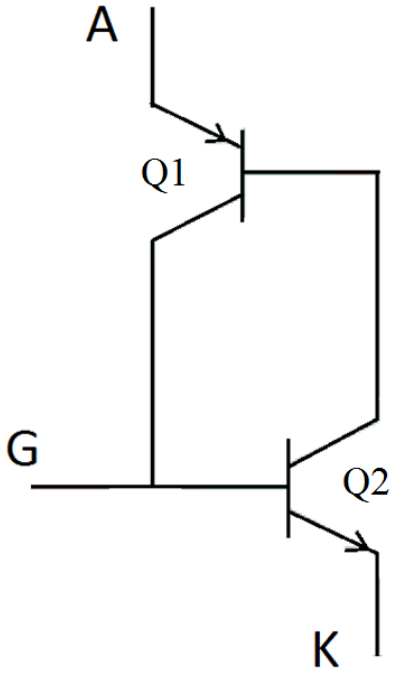

Fig. 1.4. Thyristor sub-circuit.

During on-state operation once the thyristor is triggered it acts as a diode, conducting in the positive direction, but with no blocking in the reverse direction. The on-state resistance is very low, which makes it attractive for normally on applications where low on-state losses are needed. When current in the main path of the thyristor is removed, the thyristor will turn off due to natural commutation. For AC circuit applications, this requires a gate pulse to be supplied for every positive half cycle in which the device is intended to operate.

When the thyristor is in the off-state, it will block voltage in both the positive and negative directions. Thyristors are typically asymmetrical devices, which means they are capable of blocking higher voltage levels in the forward direction than in the reverse direction.

As mentioned previously, external auxiliary circuits are used to turn off thyristors while current is still present in the main path. These circuits are called forced commutation circuits. Forced commutation may be achieved using voltage or current commutation schemes. In a voltage commutation scheme, a reverse biased voltage is applied across the thyristor, and this

forces the removal of stored charge in the thyristor's base layer. The applied reverse voltage is stored in a capacitor that is sized based on the operating voltage and the turn-off time of the thyristor. This requires complex capacitor charge circuitry and control. In current commutation, the commutating circuit brings the main current in the thyristor down to zero with a finite slope [2].

N-type silicon thyristor structures have the gate contact in the *p* region and the device requires a positive current into the gate to turn on the device. This is accomplished by applying a positive gate-cathode voltage. N-type silicon carbide (SiC) wafer technology has matured faster than that of the p-type wafers, due to p-type dopants (Al) memory effects [4, 5]. This has led to using n-type wafers predominantly to prototype SiC power devices. N-type wafers yield p-type thyristors. P-type thyristors have the gate in the *n*- region and require a negative current into the gate (where the convention is for positive gate current to flow into the gate) to turn on the device.

The control complexity of thyristors has lead researchers to modify the standard device structure to achieve better switching characteristics. This experimentation has led to a family of thyristor-like four layer structures. The most notable and highly used being the gate turn-off thyristor (GTO) [1, 2, 3], which was introduced into the market in the early 1970s. The major operating difference in comparison to a conventional thyristor is that a GTO may be turned off by applying a gate signal. For the gate signal to be reasonably small, a high turn-off gain is required [2]. This is done by increasing the gain of the top BJT and reducing the gain of the bottom BJT in the sub-circuit of Fig. 1.4. This is done by using a narrow *p* gate layer and a heavily doped cathode *n* layer [3]. This modification reduces the forward blocking capability. To increase efficiency, the gate-cathode structure is interdigitated. This reduces the distance between the gate and the cathode center, reducing any emitter focusing problems. Emitter

focusing is when the majority of the current travels in the middle of the device to the center of the anode contact. This leads to areas within the device with very high current densities, causing localized hot spots that can damage the material in that area, which will lead to device failure. Anode shorts are also introduced to reduce the carrier lifetime, which increases turn-off speed. These modifications to achieve a gate turn-off capability result in the device exhibiting a higher on-state loss and reduced reverse blocking capability compared to traditional thyristors [3]. A GTO structure is shown in Fig. 1.5.

Manufacturers provide GTOs with an attached gate driver because of the complexity of achieving effective turn-off. This gives the manufacturer control over the operating region of the device. Most gate drivers will come with specific *di/dt* and *dv/dt* requirement and protection, specifically designed for the attached GTO. The commercial GTO shown in Fig. 1.3, along with its attached gate driver in the aluminum enclosure, is called an insulated gate-commentated thyristor (IGCT) [4].

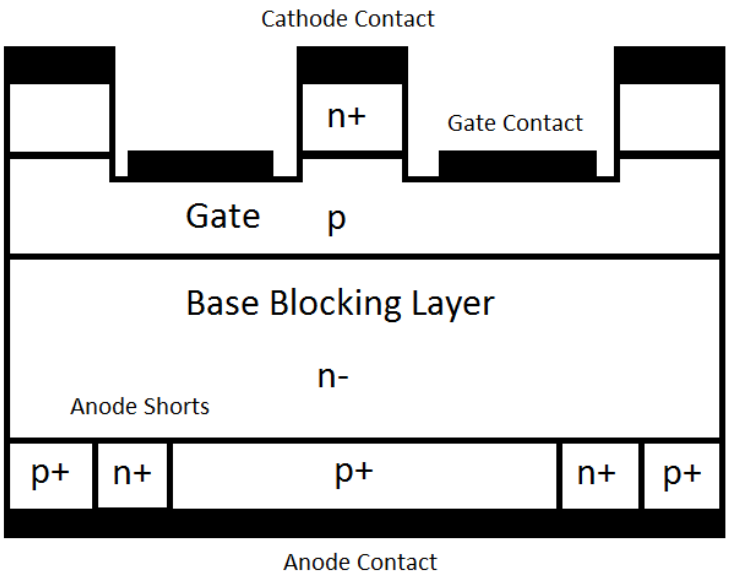

Fig. 1.5. GTO cross-sectional structure.

1.2 Silicon Carbide

Silicon carbide has revolutionized the power electronic industry [5, 6, 7, 8]. Several key developments in SiC technology over the last decade has made it an attractive choice for building power electronic devices. This includes factors such as increasing the wafer dimensions, defect free wafers, and improving minority lifetime in lightly doped regions [5]. Increasing wafer dimensions reduces the cost of SiC devices. The defect free wafers increase the device yield. And improving the mobility lifetime, can result in high voltage device that can switch at faster speeds.

SiC is a wide bandgap semiconductor material that has been known and used since the 19th century in industrial applications. It was first used in electronics in 1907 to produce light emitting diodes (LEDs). The first SiC wafer was produced in 1978, but it was not until 1989 when Cree started to sell blue SiC LEDs and SiC wafers that commercial electronic applications became possible [9].

Over the last decade manufacturers have experimented in using SiC to produce diodes, BJTs, JFETs, MOSFETs, thyristors, GTOs and IGBTs. Medium voltage and low current diodes, JFETs and MOSFETs are currently commercially available. GTOs will likely be the first high voltage device commercialized. This is primarily due to the structure not having an oxide layer, and potential voltage operating levels and applications.

At room temperature SiC is a very hard material. It reacts poorly with other materials and lacks a liquid phase, it sublimes at temperatures exceeding 1800 ^{o}C. These chemical properties prevent manufacturing wafers by traditional means, and they also complicate introducing dopants into the material. Dopants must be implanted at very high energies or grown into the material [8].

SiC is ideal for high temperature operation because of its direct wide bandgap properties and thermal conductivity. Negligible junction leakage currents at temperatures up to 600 ^{o}C are typical [5, 6]. The bandgap for SiC ranges form 2.39 - 3.33 eV depending on the crystal structure of the material [9, 10]. The thermal conductivity of SiC can be compared to that of metals. Temperature increases in semiconductors can change the physical properties of the material and damage the device. Also, increased temperature decreases carrier mobility because of lattice vibration. This causes silicon to reliably operate at temperatures up to or near 150 ^{o}C, whereas SiC can work at temperatures up to 600 ^{o}C [8]. This results in an order of magnitude improvement in the power density of power modules. If suitable heat removal strategies are implemented, heat sink size can be reduced and active cooling often eliminated [11]. Even though SiC devices can operate at higher temperatures than Si, operating current is usually de-rated at higher temperatures [12]. Applications that can take advantage of SiC temperature properties include: extreme environment applications (wide temperature, radiation), transportation, and infrastructure systems.

Extreme environment applications, such as space exploration and deep well mining, require that the electronics be shielded in special enclosures to prevent thermal damage. The electronics can also be at a remote location away from the harsh environment. This is not necessary when using SiC as the devices can be located at the application location, without any necessary special protection.

An important factor when designing transportation systems is weight and volume. This is true for aviation, vehicle or naval systems. Using SiC not only reduces the size of the electronics used, but also vastly reduces the cooling systems needed.

With the expansion of urban centers, electric power demand is increasing. This higher power

demand means that the power system will have to supply much more current to the load sites, resulting in very high power densities in large cities. Orders of magnitude higher fault currents occur due to the higher power density. This requires upgrading the electric grid and system infrastructure to handle the new load demands. Circuit breakers, transformers and fault interrupters that are rated for the higher magnitudes are larger in size. Real estate and expansion are very scarce and expensive in these types of scenarios. Installing larger system is not usually on option, as no room is available in the substations. When SiC is used in these systems, the power density can be increased, without increasing the volume currently used. This allows for an easier upgrade option, while meeting the new power demands.

A device's critical electric field is the largest electric field the device can withstand before the material destructively breaks down. SiC has an electric field breakdown that is an order of magnitude higher than that of Si when comparing devices with the same blocking voltage rating. The higher breakdown electric field of SiC allows the design of thinner, highly doped voltage blocking layers. For a majority carrier device, this results in two orders of magnitude improvement in the power density. Two orders of magnitude improvement in the switching speed for minority carrier devices is achieved as well. The faster switching speeds lead to a reduction in the size of passives elements required in accompanying circuitry and the power transformers [11].

Saturated velocity is the maximum velocity of a carrier in the semiconductor material. SiC has twice the saturated velocity of Si. This higher velocity increases the current density in power electronic devices to levels not possible in Si devices [5]. Si devices have a maximum current density of 100 A/cm^2, and with SiC this can theoretically be pushed up to 500 A/cm^2 of continuous operation if the appropriate heat removal strategies are developed [5].

Atoms in semiconductors are usually organized in a crystal structure. Silicon crystals form what is called a diamond structure. SiC has the same structure, but since it is a compound material composed of two different elements it is called a zinc blende structure. These two crystals have the exact same physical arrangements and alignment in space, but differ in the material composite.

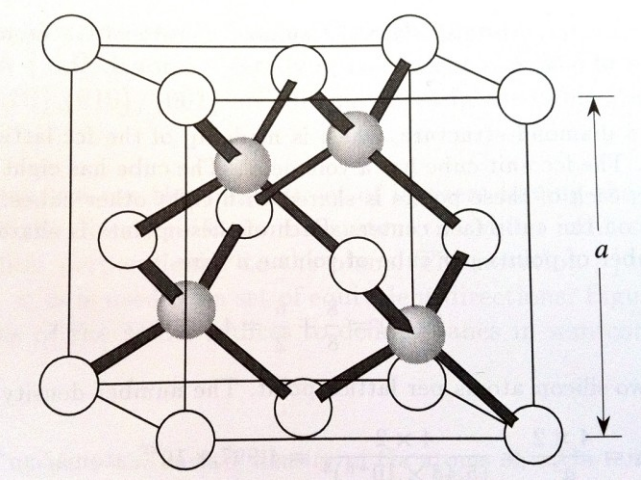

Fig. 1.6. SiC zinc blende structure

Each silicon atom has four nearest carbon neighbors, and each carbon atom has four nearest silicon neighbors. The unit cell, which is the smallest representation of the material consists of covalently bonded silicon and carbon atoms in a tetrahedral structure as shown in Fig. 1.6. Where the dark atoms are silicon and the white ones are carbon.

The silicon atoms in the above structure are located at (¾, ¼, ¼) , (¼,¾, ¼) , (¼, ¼, ¾) and (¾,¾,¾) using the conventional (x, y, z) coordinates. In such a structure the carbon atoms located at the corners are shared with adjacent cells. The different stacking sequence results in what is referred to as different polytypes.

There are over 200 known SiC polytypes. The table below [5, 6, 11] summarizes many of the key physical properties of Si and 4H-SiC, which is the most commonly used crystal structure for

power semiconductor devices. The gray rows indicate properties discussed above that lead to a compelling argument for the use of SiC in power electronic applications.

Table 1.1. Si and 4H-SiC Properties.

Parameter	Si	4H-SiC
Energy Bandgap (eV)	1.12	3.26
Electric Field Breakdown ($\times 10^6$ V/cm @ 1 kV operation)	0.25	2.2
Dielectric Constant	11.8	9.7
Intrinsic Carrier Concentration n_i (cm^{-3} @ room temperature)	10^{10}	$8.2x10^{-9}$
Electron Mobility, μ_e ($cm^2/V{\cdot}s$ @ room temperature)	1400	700-980
Hole Mobility, μ_h ($cm^2/V{\cdot}s$ @ room temperature)	450	120
Saturated Electron Drift ($\times 10^7$ cm/s @ E>$2x10^5$ V/cm)	1.0	2.0
CTE (ppm/K)	4.1	5.1
Young's Modulus (GPa)	156	400
Thermal Conductivity (W/m·K @ Room Temperature)	150	400
Density (g/cm^3)	2.3	3.2
High Breakdown Strength, (MV/cm·K)	1.5	4.9
Current Density (A/cm^2)	200	1000
	100 most commonly found	100 currently achieved, and up to 800 reported

Table 1.2 below summarizes the advantages of some of the key properties of SiC.

Table 1.2. Summary of Advantages of SiC.

Performance Metric	Causal Property Affecting Metric	Advantage
Blocking Voltage	Electric Field Breakdown	Higher blocking voltages 10×
Current Density	Saturated Electron Drift	Higher current density 5×
Volumetric Reduction	Electric Field Breakdown	Power density 100×
Switching Speed	Electric Field Breakdown	Faster speeds 100×
Operating Temperature	Energy Bandgap, Thermal Conductivity	Higher operating temperature 4×

All of these attributes allow SiC to compare favorably to Si in power electronic applications. The highest blocking voltage Si devices have reached is 6.5 kV [13]. SiC has the potential to yield 20 kV devices [14] and perhaps larger. This means that at higher voltage level utility application fewer devices will be needed in series voltage blocking stacks. A single SiC device will be able to replace three or four Si devices. So even though the wider bandgap of SiC will result in higher per device on-state voltage drop in some cases, the resulting application driven switching position will have comparable, if not better, on-state performance [11, 15].

Another key advantage is volumetric reduction of power electronic systems. This is achieved by using fewer devices in high voltage stack, simpler thermal management systems due to higher operating temperature capabilities, and smaller commutating passive components due to faster switching speeds [11, 15].

Traditionally, high speed, high power semiconductor switches were not readily available. This prevented most power system applications from adapting many of the modern advantages in circuit design, signal conditioning and smart electronics. Most power system applications still rely on legacy mechanical solutions, or low speed Si solutions. SiC GTOs make use of all of the key advantages of SiC: faster speed, higher temperature operation and volumetric reduction. This allows the development of intelligent power system applications such as solid-state transformers,

relays and fault current limiters (SSFCL). All of these applications will modernize power systems and the power grid [11].

The operating range of SiC has introduced a new challenge to packaging engineers. Current packaging technology can support either high temperature operation or high voltage operation, but not both. This is primarily due to the insulating and encapsulating material used within the package. Materials that can block high voltages at high temperatures simply have not been identified. To be able to take full advantage of SiC in system applications, high-voltage high-temperature packaging processes and materials must be developed.

1.3 Overview of GTO Models and Modeling Approaches

State-of-the-art computer-aided design (CAD) tools are extensively used by engineers and circuit designers to better predict and understand the operation of the circuit. This increases the overall productivity of the design process, and reduces the final product cost by detecting any faults or potential issues before time and money are invested [16]. Accurate, fast, and reliable physics-based models are required for this to happen. Unfortunately, most simulation tools lack such models for high power semiconductor devices. Until recently, most power electronic designs were simple enough that sub-circuit models were sufficient. With the development of these robust new semiconductor power devices and the desire to design far more intelligent solid-state solutions, accurate models are in need.

Several sub-circuit GTO models have been developed over the years: the three junction model (3-diode) [18, 19], the two transistor model [20, 21] and the two transistor-three resistor model [20].

Fig. 1.7 below shows the three different model topologies.

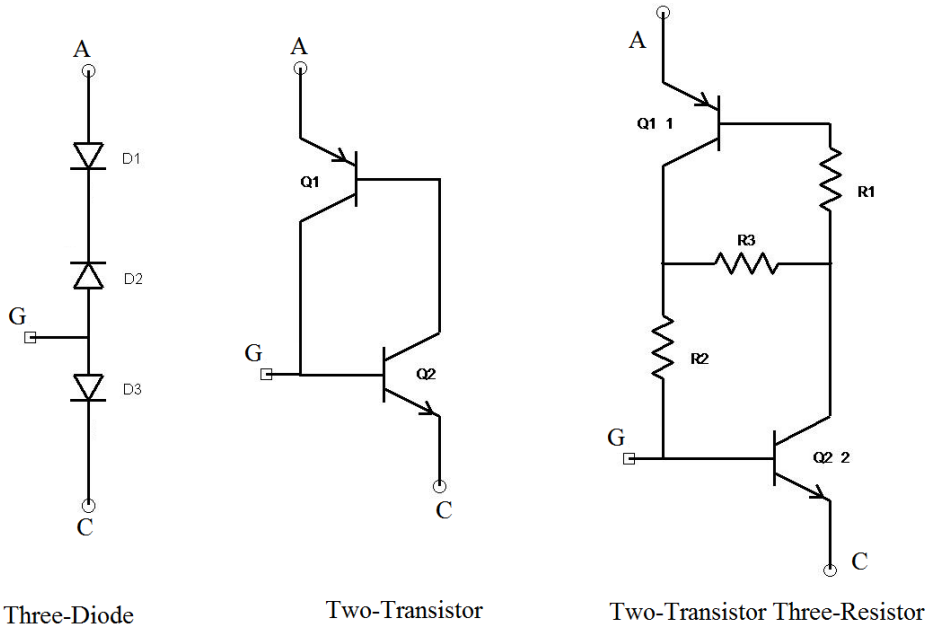

Fig. 1.7. Sub-circuit GTO model topologies.

For the three junction model to accurately fit device performance, the diode models used must be individually fit to mimic certain performance metrics of device operation. This is a tedious process and only captures first order static effects. The two transistor model fails to simulate the static on-state negative differential resistance, and it only has the capability to act like a conducting diode with no forward breakdown. The two transistor-three resistor model simulates the on-state negative differential resistance, but with no forward breakdown. Both transistor models only capture first order effects.

Ma's lumped charge model [22] is the only physics-based GTO model to take into account physical aspects of the device. This model has been commercialized in the Saber circuit simulator [23]. The model is Si *n*-type, does not incorporate thermal effects, or modern mobility models, and no parameter extraction procedure is provided.

Up to now there has been no need for SiC *p*-type GTO models, since the devices simply did

not exist. With the rapid development of these devices, circuit designers are showing an increased interest in using them in advanced designs and this model will be important in the near future.

1.4 GTO Characterization and Gate Drive Design

GTOs were developed in the mid 1960s [1], and commercialized in the early 1970s. They still have the highest power handling capabilities of modern controllable gated devices. The maturity of these devices has led to standardized techniques for device characterization and performance evaluation [23, 24]. A typical GTO data sheet will have all the standardized test results that a designer needs.

The available SiC device prototypes have no gate drive attached and perform at high speeds and elevated temperatures. Circuit designers are expecting the model to faithfully reproduce actual device behavior. It is for this reason that accurate characterization must be performed. This requires the design of appropriate gate drivers and specialized test configurations for device evaluation.

1.5 High Voltage SiC GTO Applications and Considerations

SiC is still a maturing technology that has the potential to change the way power systems are designed and operated. Current GTO technology is bulky, requires active cooling, and has slow response times. The highest rated Si devices can block 6 kV at 5 kA. Theoretically, SiC can deliver a 20 kV single wafer blocking device that can conduct several tens of kiloamps, at faster speeds and much higher temperature operation.

Once the technology is available and robust, power electronics circuits can be implemented at the distribution and transmission levels at a reasonable cost and with valuable benefits.

When designing devices in the medium to high voltage range, unidirectional asymmetrical

structures dominate the design spectrum. This forces the use of anti-parallel legs to conduct both the positive and negative half cycles. This is also requires the use of series diodes to protect the device in the reverse direction, as asymmetrical devices have very low reverse blocking capability. For this reason, high voltage PiN diodes are being developed hand-in-hand with the GTOs. This series configured anti-parallel configuration is called a switching position, which is the basic building block of all power electronic systems. The first two applications that are being heavily investigated are inverter circuits and protection equipment.

Inverter and converters are emerging as important building blocks of the modern power grid. They are used to store and retrieve energy from battery systems, to better manage peek demands, power quality and power factor correction. These circuits are also used in the interfaces between renewable energy resource, distributed generation and micro-grids with the power system.

Protection equipment has always been a cornerstone of a reliable, stable and robust power system. Most protection systems rely on an electronic monitoring and control unit that controls an electromechanical circuit breaker. So far this has worked with great efficiency, but with the continuing increase in power demand and growing power densities, new issues are arising that are complicating traditional operation and planning. One such issue is the increase in fault currents. The increase in power density, results in much higher fault currents. In some areas this increase can be magnitudes higher than what the system was designed for. The higher fault current can damage customer loads, the distribution system and protection equipment. The lead solution to this problem is the Solid State Fault Current Limiter (SSFCL).

Fault current limiters are designed to limit the fault current to a level that the traditional protection equipment can handle if used with an existing infrastructure, or as a standalone solution in new system designs. The flexibility of using a SiC-based solution allows the direct

deployment on the power system, and having fast response times to prevent any major damage from happening. Using SiC GTOs in SSFCL circuits better enables the technology in reaching its goals, by taking advantage of its material property discussed above.

CHAPTER 2

SILICON CARBIDE GTO MODELING

2.1 Introduction to Simulators and Modeling

Any circuit design process starts with simulation. This is important due to the complexity of most modern designs. It allows for a better understanding of how the circuit operates, how it interacts with other components in the system, and identifies any potential risks or problems before time and money are invested in the project. This reduces the final overall consumer cost.

In power electronics, where systems deal with tremendous amount of power and stored energy, proper simulation and analysis can save lives, cost, and property. An example of this is demonstrated by the National Institute of Science and Technology (NIST) IGBT model which is estimated to have saved approximately $16-17 million in prototyping costs alone [26]. Accurate, fast, reliable simulators and models make this possible.

Once the model equations have been derived, they may be implemented in several different hardware description languages (HDLs). HDLs are unique in that they were specifically designed to describe the operation of hardware devices [17]. These models can be used in an off the shelf, commercially available simulator such as SPICE or Saber [23].

Simulator tools were initially developed for the integrated circuit (IC) industry. IC designs tend to have a large number of components, so accuracy was an absolute necessity. A tremendous amount of work was put into developing accurate, fast, and efficient numerical solvers for these tools. When the demand for such tools increased in the power electronics industry, several different CAD designs companies were able to take advantage and leverage this previous work and tailor it to fit power electronics. The first and most popular of these commercial tools is the SPICE family of simulators. Models run in this simulator must be written

in the C language and compiled into the simulator executable. This makes model development a long tedious process. Several HDLs model based simulators are available, some of the more well-known ones are summarized in Table 2.1 below [8].

Table 2.1 Well Known HDLs and Associated Simulators.

Language	Simulator
MAST	Saber
Verilog-A	Spectre
VHDL-AMS	System Vision
C	SPICE3

The model developed in this dissertation was implemented in the MAST HDL [23] and simulated in the Saber simulation environment. The model equations may be implanted in any of the other HDLs as well.

Different model types and levels may be developed depending on the amount of accuracy required. Different levels of power semiconductor models reflect different levels of complexity with model level-0 being the simplest and model level-4 being the most complex [16, 17]. Fig. 2.1 shows the process flow for modeling a device.

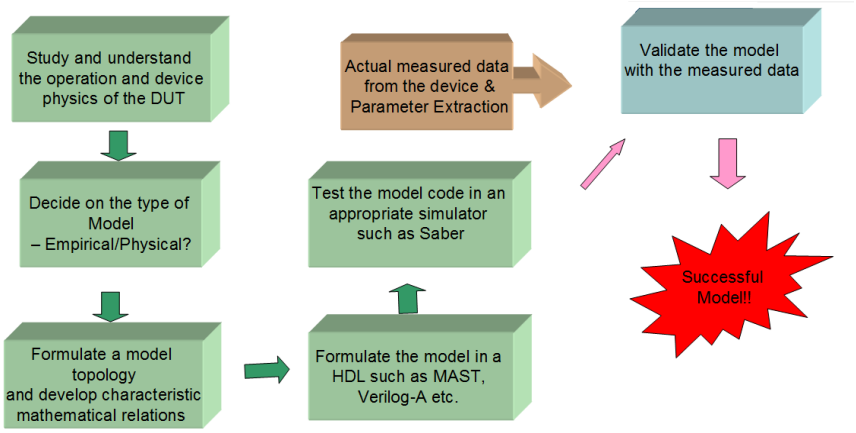

Fig. 2.1. Process flow of device modeling.

As can be seen in the above figure, device modeling is a complex procedure that requires deep understanding of device physics, device operation, programming and proper characterization techniques. This all requires a great deal of time and effort put into the model development process.

The model developer must study and fully understand the device at hand. This includes the electrical and physical behavior of the device, and the application space. This enables the identification of model level and the key performance aspect to be captured. When the model is completed it is validated against measured experimental data and tested in different circuits in the simulator.

2.2 Bipolar Semiconductor Equations

A GTO is a bipolar device, also known as a minority carrier device. This means that both electrons and holes are involved in the device operation. For the model to truly reflect the physical performance of the device, bipolar semiconductor equations are used to model the different physical phenomena. The following is a description of these equations:

Boltzmann Relation

The Boltzmann relation governs how the carrier concentration is related to electric field. The basic equations governing the concentration of carriers are:

$$n \approx \mathrm{N_c P}(\xi_C) \tag{2.1}$$

$$\mathrm{P}\ \xi_C\ = \frac{1}{1+e^{(\xi_C - \xi_F)/kT}} \tag{2.2}$$

$$v = \frac{\xi}{q} \tag{2.3}$$

$$\phi_t = \frac{kT}{q} \tag{2.4}$$

Using the Boltzmann approximation:

$$\mathrm{P}\ \xi_C\ \approx e^{-(\xi_C-\xi_F)/kT} \tag{2.5}$$

Substituting the above equations and approximation in Equation 2 .1 yields:

$$\mathrm{n} \approx n_0 \mathrm{e}^{(\mathrm{V}_1-\mathrm{V}_2)/\phi_\mathrm{t}} \tag{2.6}$$

$$p \approx p_o \mathrm{e}^{(\mathrm{V}_1-\mathrm{V}_2)/\phi_\mathrm{t}} \tag{2.7}$$

where:

n is electron concentration,

n_o is equilibrium background electron concentration,

p_o is equilibrium background hole concentration,

p is hole concentration,

N_C is the conduction band density,

q is electron charge,

ξ is energy,

$P(\xi_C)$is the Fermi-Dirac probability function at the edge of the conduction band,

ϕ_t is the thermal voltage.

Charge Neutrality and Conservation

For a physics based model, charge must be conserved. Charge is neither created nor destroyed, so injected excess carriers must be related with ionized background doping and the equations must be valid over all ranges of operation. This insures that the model fitting parameters will be within their physical limits.

Bipolar equation charge may be represented or modeled in two major different approaches: either by Fourier series charge control or by lumped charge [22, 27]. The Fourier series method is suitable for finite element solvers, such as MATLAB. When using an HDL based simulator for

bipolar device modeling, modeling charge in lumped discrete quantities is more suitable. Modeling charge in discrete quantities at discrete locations is not new, but Dr. Lauritzen's modeling group at the University of Washington developed the *Lumped Charge* modeling approach [22, 27] as a systematic way of choosing the charge nodes' locations, and developing the appropriate modeling equations.

Carrier Transport Equations

The movement of carriers, both electrons and holes, results in an electric current. This motion is referred to as carrier transport. The two mechanisms of carrier transport of interest are drift and diffusion.

Drift is carrier transport due to the electric field resulting from the applied voltage. It is described in the following equations:

$$J_p = q\mu_p pE \tag{2.8}$$

$$J_n = q\mu_n nE \tag{2.9}$$

where:

J_p is the hole current density,

J_n is the electron current density,

μ_p is the hole mobility, and

μ_n is the electron mobility.

Diffusion transport occurs due to a carrier concentration gradient. Carrier will tend to move from an area of larger concentration to an area of lower concentration. The transport is independent of the carrier density; it is dependent on the concentration gradient. Diffusion current is governed by the following equations:

$$J_p = -qD_p \frac{dp}{dx} \tag{2.10}$$

$$J_n = qD_n \frac{dn}{dx} \tag{2.11}$$

where:

D_p is the hole diffusion constant,

D_n is the electron diffusion constant.

In most cases drift and diffusion transport coexist. This is especially true when an electric field and a concentration gradient are present inside a device. The total current density is therefore the sum of both drift and diffusion current as shown below:

$$J_n = q\mu_n nE + qD_n \frac{dn}{dx} \tag{2.12}$$

$$J_p = q\mu_p pE - qD_p \frac{dp}{dx} \tag{2.13}$$

The Einstein Relation

Mobility is a measure of a carrier's readiness to move in response to an electric field gradient. Diffusivity is a measure of carrier's readiness to move in response to a concentration gradient. The two transport carrier measures are related by Einstein's relation:

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{D}{\mu} = \frac{kT}{q} = \phi_t \tag{2.14}$$

with a generic form:

$$D = \mu \times \phi_t \tag{2.15}$$

SiC Mobility Models

A great deal of theoretical and experimental work has been done to model 4H-SiC mobility [28, 29]. The most recent models are:

$$\mu_p\ 4H-SiC\ = \mu_{p(300,Np)}\left(\frac{T}{300}\right)^{-\beta_p} \tag{2.16}$$

$$\mu_n\ 4H-SiC\ = \mu_{n(300,NA)}\left(\frac{T}{300}\right)^{-\beta_n} \tag{2.17}$$

where B_p and B_n are fitting parameters that are a function of doping.

Room temperature mobility may be calculated by:

$$\mu\ 300, NA\ = \mu^{min} + \frac{\mu^{max}-\mu^{min}}{1+\left(\frac{NA}{N_{fitting}}\right)^{Y_{fitting}}} \tag{2.18}$$

where the fitting parameters are interpolated from measured and statistical data.

Transit Time

The time it takes a carrier to transit or move from one point in the semiconductor to another is defined as the transit time. It is important when designing bipolar devices to insure the geometries and material properties are fine-tuned so that the transient time is smaller than the carrier lifetime in that region. The transient time is governed by the following equation:

$$\tau_t = \frac{d_r \times d_t}{2D_p} \tag{2.19}$$

where:

τ_t is the transient time,

d_r is the region width,

d_t is the distance traveled.

Using the Einstein relation, transient time will be used in the current transport equation instead of mobility and diffusivity. To introduce temperature effects, the transient time may be scaled as follows:

$$\tau_t = \tau_o(\frac{T}{300})^{-B} \tag{2.20}$$

where:

τ_o is the transient time at room temperature,

T is operating temperature,

B is the temperature fitting parameter.

Current Continuity Equations

Current continuity is important as drift, diffusion, and recombination occur simultaneously in a semiconductor at any given time. The current continuity equation governs the overall effect of these physical phenomena as following:

$$\frac{dp_n}{dt} = D_p\frac{d^2p_n}{dx^2} - \mu_p E\frac{dp_n}{dx} - \frac{p_n - p_{no}}{\tau} \tag{2.21}$$

Accumulation Diffusion Drift Recombination

Poisson's Equation

Poisson's equation is used to covert a volumetric charge density profile into an electrical field profile. It can be used to solve the junction depletion width and vary the transient time accordingly. This will be shown in the following section.

Kirchhoff's Equations

Kirchhoff's equations are used to relate the internal voltage and current with the terminal equations tying the model with external circuitry. For this to be an accurate physics based model the, sum of all internal voltage drops in the device is equal to the voltage drop across the device terminals, and the sum of all the components of internal current is equal to the terminal currents.

2.3 Model Equation Formulation

The GTO device structure to be modeled is shown in Fig. 2.2 below.

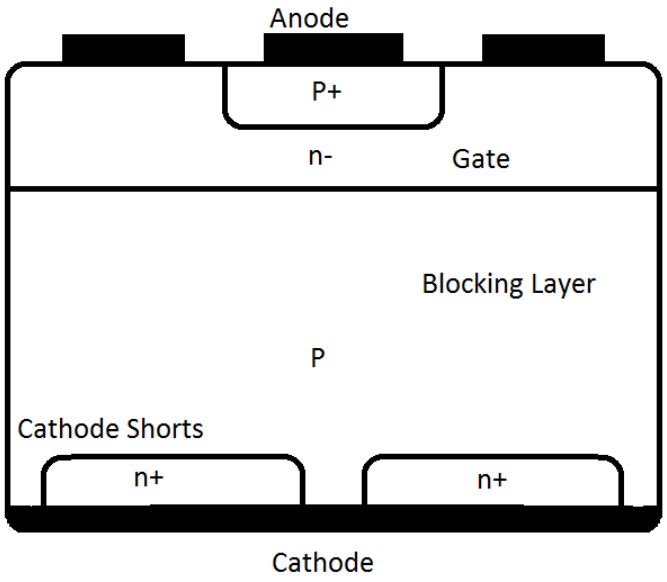

Fig. 2.2. GTO structure.

Fig. 2.3 shows a two dimensional view for illustration proposes, with the appropriate charge nodes.

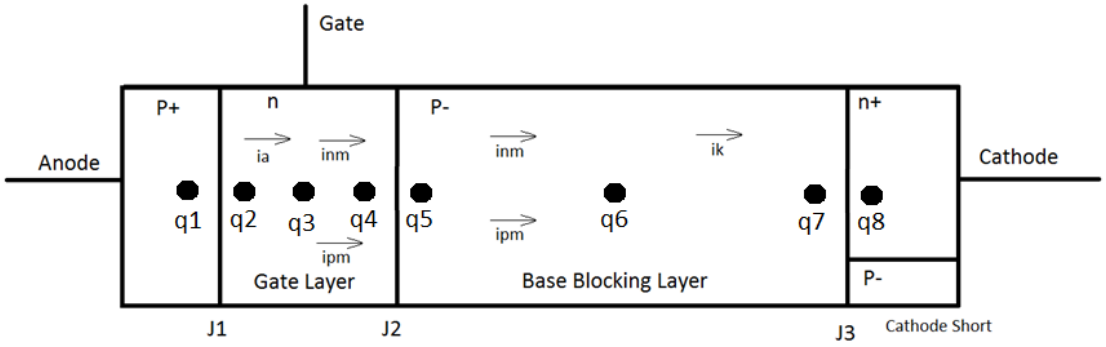

Fig. 2.3. Two dimensional GTO structure.

The next step in the modeling procedure is formulation of model equations. Using the above structure and the semiconductor equations described in the previous section the modeling equations are developed as shown below.

Current Transport Equations

Substituting equations (2.15) and (2.19) in equations (2.12) and (2.13), and using a linear diffusion term with the lumped charge convention yields the following current transport equations:

Gate Region:

From node 2 to node 3

Only hole current exists in this region. We can still formulate two current equations that describe current transport. Equation (2.22) is for hole current which is equal to the injected terminal current. The first term is the drift portion of the current, and the second term is the diffusion portion.

$$i_A = \frac{q_{p2} - q_{p3}}{2T_{p2}} + \frac{q_{p3}}{2T_{p2}} \frac{v_{23}}{\phi_t} \tag{2.22}$$

where:

i_A is the injected anode current,

q_{p2} is the hole charge of node 2,

q_{p3} is the hole charge of node 3,

T_{p2} is the hole transient time in the gate region,

v_{23} is the voltage potential between node 2 and node 3,

ϕ_t is the thermal voltage.

The sum of electron currents in this region is zero, and is described in Equation (2.23). Even though the net electron current is zero, this equation is used to help the simulator predict an appropriate solution for the equations.

$$0 = \frac{q_{p3} - q_{p2}}{2T_{n2}} + \frac{q_{p3} + Q_G}{2T_{n2}} \frac{v_{23}}{\phi_t} \tag{2.23}$$

where:

T_{n2} is the electron transient time in the gate region,

Q_G is the background charge of the gate region.

From node 3 to node 4

Equation (2.24) describes the hole current in this region.

$$i_{pM} = \frac{q_{p3} - q_{p4}}{2T_{p2}} + \frac{q_{p3}}{2T_{p2}} \frac{v_{34}}{\phi_t} \tag{2.24}$$

where:

i_{pM} is the total hole current in the region,

q_{p4} is the hole charge at node 4,

v_{34} is the voltage potential from node 3 to node 4.

Equation (2.25) governs the electron current in the same region.

$$i_{nM} = \frac{q_{p4} - q_{p3}}{2T_{n2}} + \frac{q_{p3} + Q_G}{2T_{n2}} \frac{v_{34}}{\phi_t} \tag{2.25}$$

where:

i_{nM} is the total electron current between node 3 and node 4,

In the Base Region

From node 5 to node 6

Equation (2.26) describes the hole current in this region.

$$i_{pM} = \frac{q_{n5} - q_{n6}}{2T_{p3}} + \frac{q_{n6} + Q_B}{2T_{p3}} \frac{v_{56}}{\phi_t} \tag{2.26}$$

where:

q_{n5} is the electron charge at node 5,

q_{n6} is the electron charge at node 6,

T_{p3} is the hole transient time in the base region,

Q_B is the background doping of the base region,

v_{56} is the voltage potential from node 5 to node 6.

Equation (2.27) governs the electron current in the same region.

$$i_{nM} = \frac{q_{n6} - q_{n5}}{2T_{n3}} + \frac{q_{n6}}{2T_{n3}} \frac{v_{56}}{\phi_t} \tag{2.27}$$

where:

i_{nM} is the total electron current between node 5 and node 6,

T_{n3} is the electron transient time in the base region.

From node 6 to node 7:

In this region only the electron current flows. We still formulate two current equations to govern current transport in this region. Equation (2.28) is for hole current.

$$0 = \frac{q_{n6} - q_{n7}}{2T_{p3}} + \frac{q_{p6} + Q_B}{2T_{p3}} \frac{v_{67}}{\phi_t} \tag{2.28}$$

where:

q_{n7} is the electron charge at node 7,

v_{67} is the voltage potential between node 6 and node 7.

Equation (2.29) governs the electron current, which is equal to the cathode terminal current i_{ki}.

$$i_{ki} = \frac{q_{n7} - q_{n6}}{2T_{n3}} + \frac{q_{n6}}{2T_{n3}} \frac{v_{67}}{\phi_t} \tag{2.29}$$

where:

i_{ki} is the cathode current.

Current Continuity Equations

For the Gate region:

Both the anode and the gate current are injected into this region. Equation (2.30) governs the charge carrier recombination in the region. Equation (2.31) relates the external current with the internal current.

$$i_{nM} + i_g = \frac{q_{p3} - Q_{Gp}}{\tau_G} \tag{2.30}$$

$$i_A = i_{nM} + i_{pM} + i_G \tag{2.31}$$

where:

Q_{Gp} is the hole background charge of the gate region,

τ_G is the carrier life time in the gate region.

For the Base region:

Only one terminal current is present in this region, it is related to internal currents by Equation (2.31). Charge carrier recombination and charge variation with time are governed by Equation (2.32).

$$i_K = i_{nM} + i_{pM} + i_{shunt} \tag{2.31}$$

$$i_{nM} - i_k = \frac{q_{n6} - Q_{Bn}}{\tau_B} + \frac{dq_{n6}}{dt} \tag{2.32}$$

where:

Q_{Bn} is the background charge of the base region due to electron concentration,

τ_B is the carrier life time in the base region.

i_{shunt} is the current through the shunt resistor connected from base to cathode region,

Junction Equations

The junction voltage is a function of background charge and the closest node charge. For the first junction it is governed by Equation (2.34).

$$q_{p2} = Q_{Gp} \exp\left(\frac{v_{J1}}{\phi_t}\right) \tag{2.34}$$

The equations for the second junction are a little more complex. This is due to the lightly

doped base region, and the large volume difference between the two adjacent regions. Equations (2.35) and (2.36) relate the junction voltage with the physical parameters.

$$q_{p4} = (q_{n5} + Q_B)\exp\left(\frac{-(v_{J2} + \phi_{45})}{\phi_t}\right) f_v \tag{2.35}$$

$$(q_{p4} + Q_G)q_{p4} = (q_{n5} + Q_B)q_{n5} f_v^2 \tag{2.36}$$

where:

fv is the gate to base volume ratio.

Equation (2.37) describes the third junction similarly to the first junction, since the same situation applies.

$$q_{n7} = Q_{Bn} \exp\left(\frac{v_{J3}}{\phi_t}\right) \tag{2.37}$$

Poisson's Equations

Poisson's equation is used to model the variation of depletion width with the variation of voltage in the base region. This is very important since the forward blocking voltage is sustained across this region. The transient time is varied using a voltage dependent variable l_2 as shown in the equations below.

$$T_{n3} = T_{n30}(1 - l_2)^2 \tag{2.38}$$

$$l_2 = \left(\frac{\phi_{45} + v_{J2}}{\phi_{B2}\left(1 + \frac{|i_{pM}|}{I_{B2}}\right)}\right)^{\frac{1}{2}} \tag{2.39}$$

Terminal Equations

Since this is a closed loop system, Kirchhoff's equations can be used to relate the internal voltages and current established above with the terminal values. This will tie the model with externally connected devices and circuitry.

$$v_{AK} = v_{J1} + v_{23} + v_{34} + v_{J2} + v_{56} + v_{67} + v_{J3} \tag{2.40}$$

$$v_{AG} = v_{J1} + v_{23} \tag{2.41}$$

$$v_{GK} = v_{34} + v_{J2} + v_{56} + v_{67} + v_{J3} \tag{2.42}$$

$$i_{shunt} = \frac{v_{67}}{R_{shunt}} \tag{2.43}$$

$$i_K = i_A - i_G \tag{2.45}$$

2.4 Model Implementation in MAST

Now that the equations have been formulated, they must be implemented in an HDL for use in a simulator. Saber was chosen for this work, for its flexibility and wide use by power electronic engineers, but any simulator may be used. To use Saber, the model is developed in the MAST language [23].

Implementing a robust model requires a thorough understanding of the device operation and equation dependencies to better structure the model equations for an optimal solution. The simulator will suggest a solution for a small subset of the unknown quantities, known as variables, and calculate the rest of the unknowns using the model equations.

The voltage between nodes 7 and 8 (v_{78}), the junction voltage between nodes 4 and 5 (v_{45}) and the electron charge at node 6 (q_{n6}) were chosen as our variables. This gives the simulator all the information it needs to solve the rest of the unknowns as following:

- Transit times are calculated using the variable v_{45} and equations 2.38 and 2.39.
- q_{n7} is calculated using the variable v_{78} and equation 2.37.
- q_{n5} is calculated using the variable v_{45} and the junction equation.
- v_{67} is calculated using q_{n7} and equation 2.28.
- i_k is calculated using q_{n7} and v_{67} and equation 2.29.
- q_{p3} is solved using the terminal voltage v_{ag} and the junction equation.
- The system of three variable equations 2.26, 2.27 and 2.31. are solved for i_{pm}, i_{nm} and v_{56}.
- i_g is calculated using i_{nm} and equation 2.30.
- v_{34} is calculated using i_{pm} and equation 2.24.
- Finally i_a is calculated using the terminal equation.

Since this is a physics based model, the equations relate mathematical theory to physical device constants. These parameters include dopant concentrations, device geometry, mobility and carrier lifetime [8].

The developed model has 18 physical parameters. If the device geometry doping profile and structure are known, most of these constants can be simply calculated; otherwise they are used as fitting parameters to fit the model to a specific device's performance.

CHAPTER 3

SiC GATE DRIVE DESIGN

3.1. Introduction and Background

Gate turn-off thyristors (GTOs) are optimized thyristor structures that can be turned on and off through a gate signal. Typical GTOs are rated for high current and voltage values. Commercial devices always come attached to a gate driver board that is specifically designed for that device [1, 2].

GTOs are designed for medium and high voltage applications, and therefore are typically packaged in a press pack. Si GTOs are an order of magnitude slower than Si thyristors and typically block less voltage [2, 3]. Since GTOs are controllable devices, this eliminates the use of forced commutation circuitry associated with thyristors. This makes their usage easier and more attractive.

SiC SGTO can block higher voltage levels at the same current density of Si counterparts. These devices also switch at much faster speeds, which results in less power consumption during the turn-off process. This also means that if a capacitor is used to provide the turn-off voltage, it will be much smaller since it has to provide the voltage for a much shorter period of time. The SiC GTOs currently available are still experimental research parts. The turn-off gain is high, typically having a value of about 70%. This means 70% of the main current through the device must be removed through the gate for proper turn-off. This is primarily due to defects in the original material or defects resulting from processing the devices.

3.2. GTO Gate Drive Concepts

A small current can be used to turn on the device, but for proper turn 70% off the main anode-cathode current must be extracted from the gate. This design is for SiC p-type GTOs.

For turn on a positive anode-gate voltage is applied. For turn-off a positive gate-anode voltage is applied. Even though a small current can be used for turn-on, a high *di/dt* initial current is typically used for faster turn-on. The *di/dt* is controlled, to minimize any overvoltage in the system and enable soft turn-on application. This fast rising current is only supplied for a short pulse, so the power consumption is minimal. A small current must be continuously supplied to the gate of the GTO when the device is on.

A positive gate-anode voltage is applied for turn-off. The turn off time depends on how fast the stored charge in the device is dissipated. Depending on the application, this may be controlled by current rise *di/dt*. For soft switching applications, to prevent voltage spikes, the turn-off speed must be slowed down. For fault and overcurrent applications, the engineers must design around the voltage spike issues.

Appropriate isolation of the power circuit and the control circuit is essential for proper operation. This is due to that fact that the reference on the power side is the anode of the GTO, which can experience rapid excursions relative to the gate control reference. This isolation can be accomplished in either of two ways: opto-couplers and isolation transformers [2, 30].

All these factors create a unique gate drive design that is more complex than typical device gate drives.

3.3.SiC GTO Gate Drive Design

Due to current technology and process limitations, available SiC GTOs are limited to modest current values in the order of 50-75 A. Most GTO applications require much more current, so devices must be paralleled. A typical application for such devices would require paralleling 16 devices to get a 1000 A of operating current. The important device parameters for the design process are nominal current, turn-on time, turn-off time and holding current.

The gate drive designed will be used with a SiC GTO. The device is rated for 64 A, but the final application requires 16 parallel devices in a switching position rated at 1000 A. So two gate drives were designed: one that is suitable for a single device and another that can drive up to 20 devices in parallel.

3.3.1. Single Device Gate Driver

Fig. 3.1 below shows the schematic for a single device gate drive circuit.

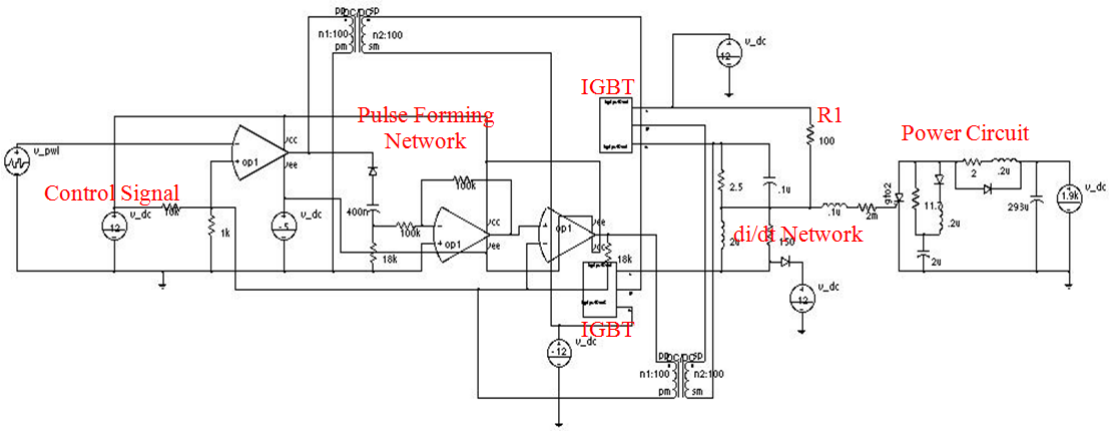

Fig. 3.1. GTO gate drive schematic.

The power circuit is a typical GTO test circuit [22] with a snubber to insure proper device operation. The operational amplifier power supplies are all low power supplies. The supplies connected to the IGBTs need to be able to handle the main GTO current for the turn-off duration. This can be accomplished with either high power rated supplies or filtering networks, depending on the GTO turn-off time and the GTO current ratings.

The input control signal is conditioned through a pulse forming network and voltage level shifting op-amps to create the appropriate IGBT control signals.

The top IGBT is triggered when the GTO is turned on; it is only on for a short period of time to enable the *di/dt* network for fast turn-on. The length of this period depends on the GTO [30], and is controlled using the capacitor in the pulse forming network. The *di/dt* value is controlled by the *di/dt* network elements. For the rest of the on period the IGBT is off, and holding current is provided through R1. The value of R1 determines the amount of holding current.

The bottom IGBT is triggered when the GTO is turned off. This creates a lower potential path through which the main GTO current is diverted. This IGBT must be on long enough to ensure the GTO turn-off. To be on the safe side, the path is held open for the duration of the off period.

The unity isolation transformers are used to isolate the control circuitry from the power circuit, which is necessary since the IGBT emitter is not connected to ground. These transformers should have enough isolation to prevent any spikes on the power side from damaging the control side. This will provide a truly floating gate driver. In reality isolation will also be provided through the IGBT gate driver [32] shown in Fig. 3.2.

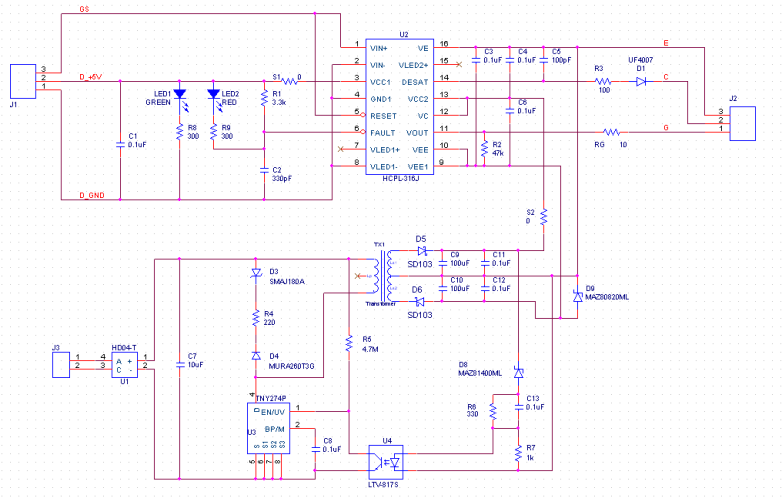

Fig. 3.2. IGBT gate drive with power supply circuit.

The saber simulation waveforms for this gate driver are shown in Fig. 3.3.

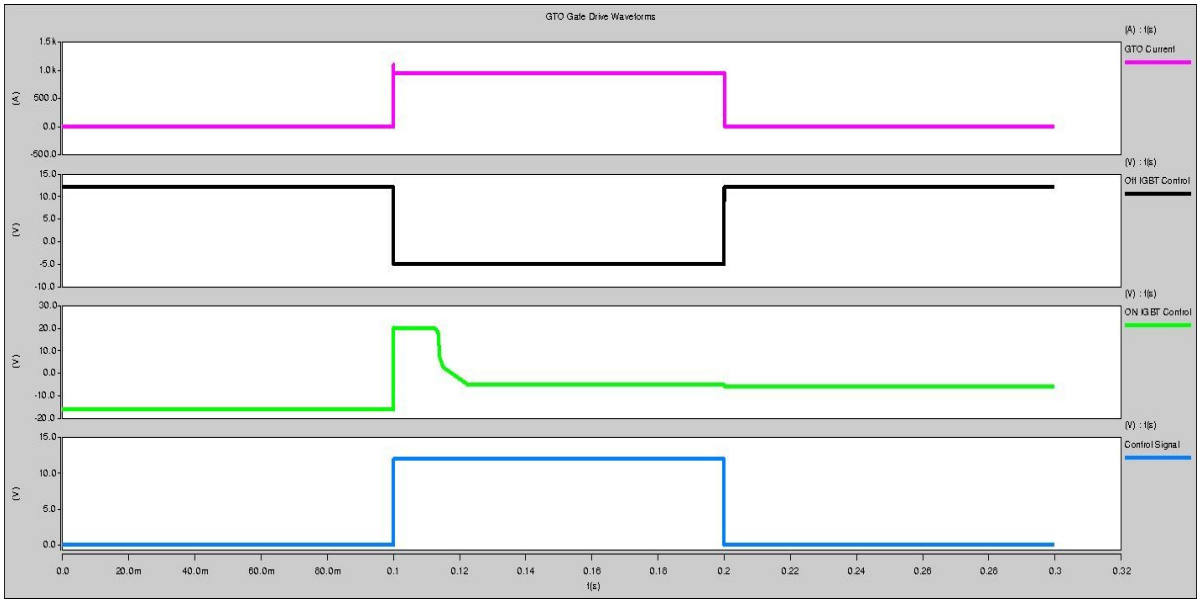

Fig. 3.3. Saber simulations.

The bottom waveform is for the user input control signal; any digital logic level will work. The green waveform is the control signal for the top IGBT that controls the high *di/dt* period. The black waveform is the control for the off IGBT. The top waveform is for the GTO main current, which is operating as intended.

The turn-on and turn-off current sink power supplies were not designed. The turn-on power supply can be a low current supply, but the turn off the supplies need to be able to handle the high current for the turn off duration. This design may be used for devices with turn-off currents up to 75 A.

This design was not prototyped due to application needs, where it was determined that a gate driver capable of 1000 A turn-off was necessary.

3.3.2. High Current Switching Position Gate Drive

The high turn off gain of SiC GTOs makes it extremely difficult to design a single gate driver for both turn-on and turn-off. For the device at hand the gate drive will need to supply 1 A of current for turn-on, but 45 A for turn-off per device in the switching position. The main problem is designing the current path and the voltage sources. This problem can be solved by designing two gate drivers that will be used simultaneously in the system. One for turn-on, and one for turn-off. The initial design is based on a typical thyristor turn-on circuit [33], but has been modified and redesigned to fit the application needs. The two gate drivers have the same schematic, but with some different components in the current path.

For the turn-on gate driver, the output is connected positive anode-gate, and a current limiting resistor is used to limit the current to a desired value. This will limit the turn-on speed, but will also allow soft turn on, with no voltage overshoots. For turn-off, the output is connected gate-anode, and no current limiting resistors are used. This will allow the GTO to sink as much

current as needed for proper turn-off. This will accomplish maximum turn-off, but will make the system prone to voltage overshoots. This is especially true in utility applications where large stray inductances are typical. The schematic is shown below in Fig. 3.4.

The transformer steps the 120 VAC input voltage down and also provides physical isolation

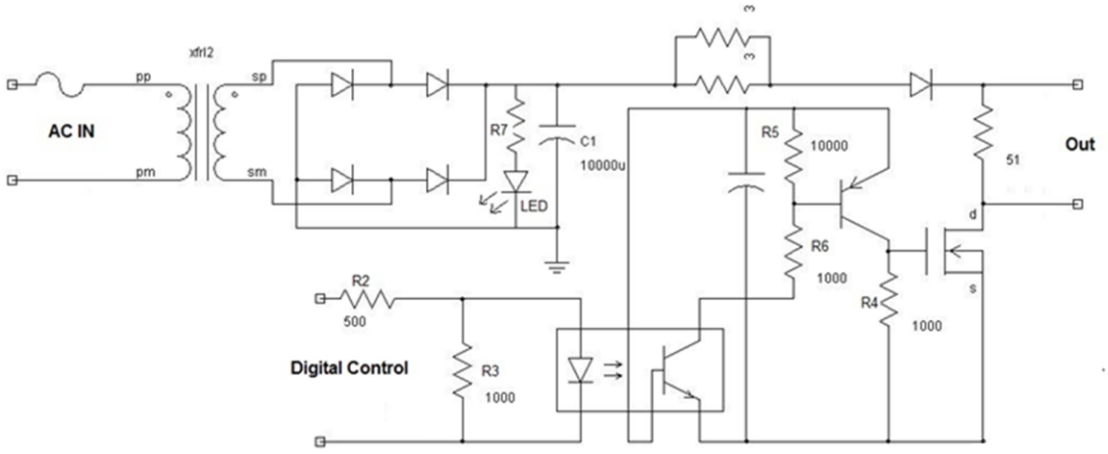

Fig. 3.4. GTO gate driver schematic.

from the power circuit. This is important since two gate drivers are going to be connected at the same time. A custom 10 kV input-to-output isolation transformer was ordered from *Signal Transformers, Inc*. The AC input voltage is then rectified by the Diode Bridge, and charges the 10 mF capacitor to 18 VDC. As explained previously, GTOs are current controlled device. The magnitude of the capacitor voltage is not important in this application, as long as the appropriate voltage is chosen to store the charge necessary for the turn off process. R7 and the LED are present for safety. The LED indicates the presence of charge on the capacitor.

The opto-coupler isolates the digital control from the circuit. The output of the opto-coupler is coupled with a PNP BJT that controls the power MOSFET.

The MOSFET completes the path for the capacitor to discharge through the current limiting resistor and the 51 ohm resistor. If the GTO is connected, the current will bypass the 51 ohm resistor and go through the device, since the devices on-state resistance is much smaller than the parallel resistor.

For the turn-on case, the current will flow from anode to gate turning the device on. The current is limited by the current limiting resistors to 10 A; this is sufficient for fast turn-on. Two 3 Ω 10W resistors are used parallel to get the appropriate power rating. If the gate drivers were used for DC or very slow frequency operation higher power resistors would have to used.

For turn-off, there is no current limiting resistor, and the GTO is connected gate anode, the device will pull 70% of main current for the duration of the turn off process.

Characterization of the GTO explained in detail in the next chapter show that the GTO will turn off in about 1μs. This is when the GTO is tested on its own with no circuit parasitics. In reality, since this is a current controlled device, circuit conditions could have an effect on how fast the device turns off. A system test using similar devices along with other circuitry showed a turn-off time of 6.7 μs.

For safety reason a maximum system turn-off time of 100 μs will be used,

$$Q = \int I\, dt \tag{3.1}$$

where:

Q is stored charge necessary for turn-off,

I is turn-off current.

If designed for worst case scenario (safe operation), with constant current discharged from the capacitor, then:

$$Q = I \times t = 700A \times 100us = 70mC \tag{3.2}$$

The minimum size for the capacitor to store the necessary charge is:

$$C = \frac{Q}{V} = \frac{70m}{18} = 3888\ \mu F \tag{3.3}$$

The PCB was laid out using *PCB Artist* [34]. The schematic below is a capture from that program.

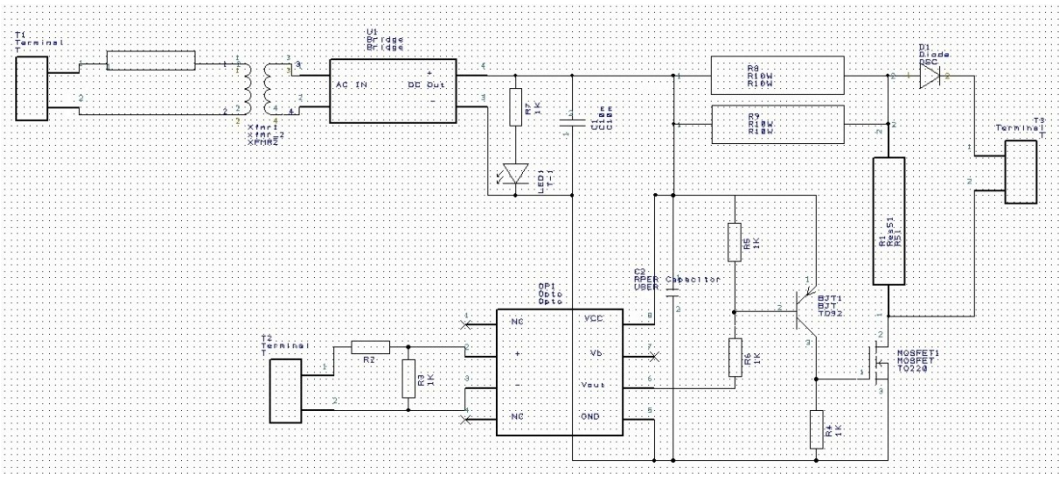

Fig. 3.5. PCB artist schematic.

Fig. 3.6 is the PCB layout using the same program.

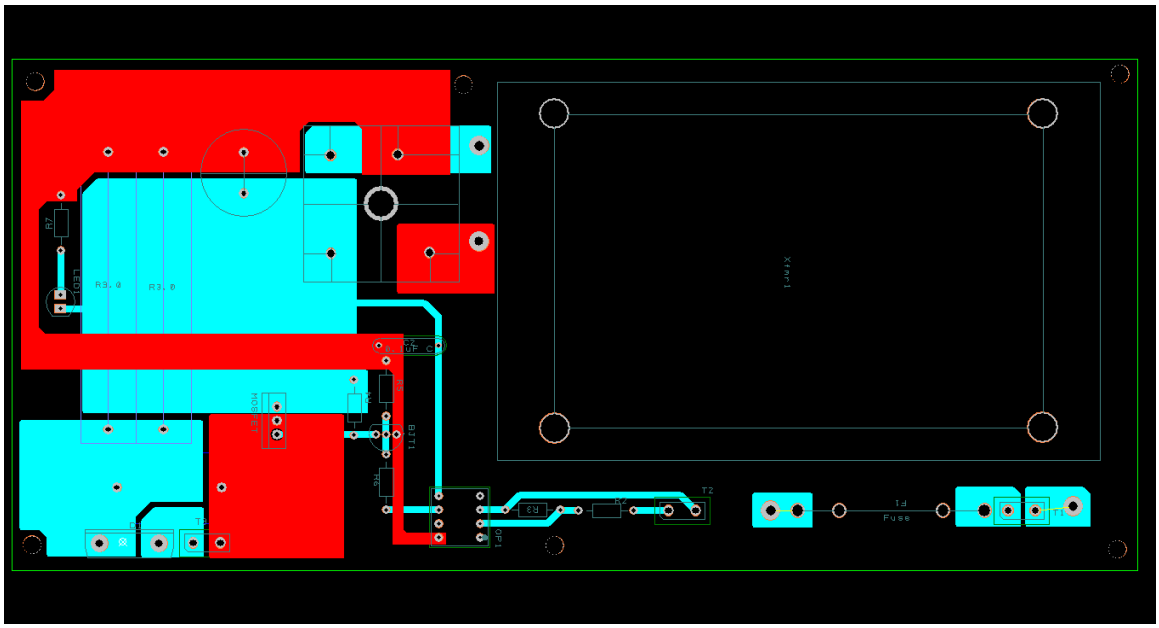

Fig. 3.6. PCB layout of the gate driver.

Thick PCB and 4 oz. copper were used to be able to handle the weight of the transformer and the current rating of the design.

The final design components are listed in Table 3.1.

Table 3.1 Component List for Gate Driver

Part Number	Description
R-10531	TRANSF 12.6VAC 3.41A 43 VA, 10 kV ISOLATION
565-1922-ND	CAP 10000UF 10V ELECT LXZ RAD
HCPL4503M-ND	OPTOCOUPLER TRANS 1CH HS 8DIP
F2652-ND	FUSE 250V SLO-BLO 3AB 20A CART
F3305-ND	FUSE CLIP 15A 250V EAR 13/32TIN
P51W-3BK-ND	RES 51 OHM 3W 5% METAL OXIDE
A98355-ND	TERM BLOCK 2POS SIDE ENTRY 5MM
641-1388-ND	RECT BRIDGE GPP 800V 50A GBPCW
IRF1404PBF-ND	MOSFET N-CH 40V 202A TO-220AB
HS365-ND	HEATSINK TO220 CLIPON W/TAB.75"
2N3906D26ZCT-ND	IC TRANS PNP SS GP 200MA TO-92
ALSR10-3.0-ND	RESISTOR SILICONE 3.0 OHM 10W

Fig. 3.7 is the final turn-on gate drive

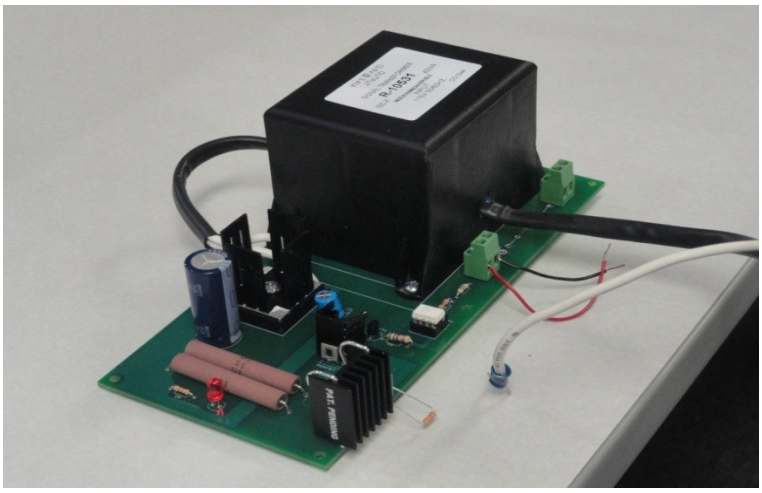

Fig. 3.7. GTO gate driver board.

Fig. 3.8 is the final turn-off gate driver, showing the copper strap used in place of the current limiting resistors, to carry the full rated current.

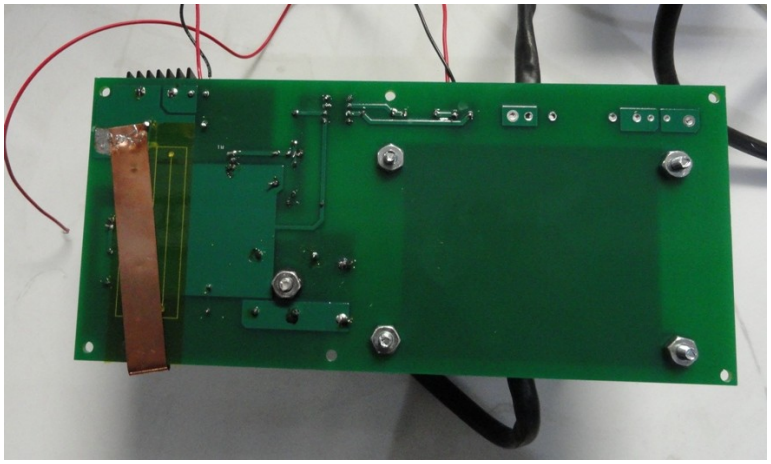

Fig. 3.8. Turn-off gate driver.

CHAPTER 4

SIC P-TYPE GTO CHARACTERIZATION

4.1. Introduction

Device characterization is an important part of device modeling, packaging and system design. After a model is developed it must be validated against experimental data. This requires the model parameters and constants be fitted to the specific device tested.

SiC is a maturing technology, and devices have just recently started to be commercialized. However, GTOs still have a way to go. Samples are still hard to obtain and expensive to purchase. SiC p-type GTOs from Cree were acquired [36, 37], for use in a solid-state fault current limiter (SSFCL) project. These devices were tested for functionality at Cree, but more data was needed for modeling, packaging and system design purposes.

4.2.Device Test Setup and Measurement Results

The team received 40 8mm×8mm devices, which was the yield of two complete wafers, which amounts to a 33% yield. A picture of a SiC GTO wafer before dicing is shown in Fig. 4.1.

Cree's criteria for a good device are as following:

- Anode-Cathode voltage higher than 8 kV at a leakage current of 1 μA.
- Gate-Anode voltage below 100 V at a leakage current of 100 μA.
- Anode-Cathode on state voltage under 5V at 40A of main current.

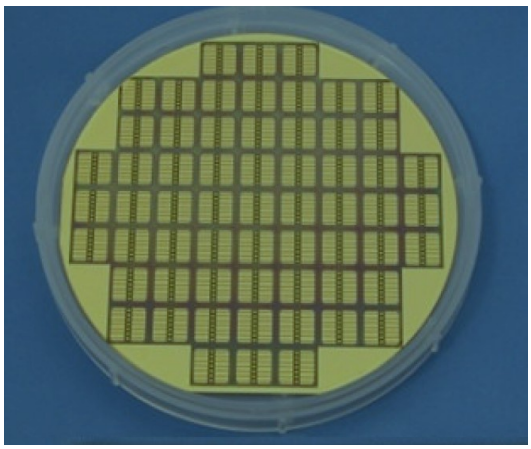

Fig. 4.1. 4 inch SiC wafer with p-type GTOs
(Courtesy of Cree).

A number of devices did not pass all the manufacturer's and the application's criteria, but

were still deemed useful for testing and packaging proposes.

Cree designed these devices in partnership with *Silicon Power Corporation* (SPCO). The contact metallization is optimal for SPCO's ThinPak packaging techniques [38]. This process is ideal for pulsed power applications, but must be altered for continuous operation. This technique involves using a ceramic lid with through hole vias to pull the current out of the top side. The figure below shows a SiC GTO, lid and lidded device.

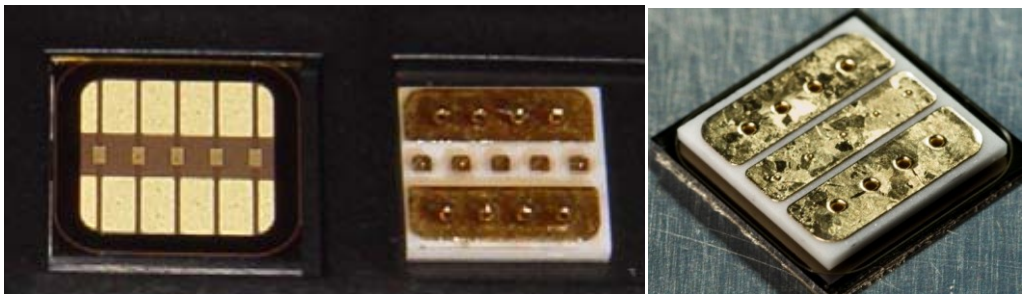

Fig. 4.2. 8mm SiC GTO, lid and a lidded GTO.

The backside of these devices is the cathode, the five small rectangles in the center are the gate contacts, and the larger rectangles on the sides are the anode. The devices are rated for 8 kV with a max leakage current of 1 μA. The safe operating current density for continuous operation is 100 A/cm^2 yielding 64 A devices. The ratings of these devices make it difficult to design the appropriate test setups.

Blocking Voltage Test Setup

These devices are very sensitive to leakage currents at high breakdown voltages and can be easily damaged. When testing high breakdown devices in the range of 10 kV, the surrounding air breaks down. Testing must be conducted in a high voltage isolation medium. Fluorinert [39] was chosen since it can isolate the high voltage levels needed, and the material can be easily cleaned off. This is extremely important to not introduce any contaminants into the packaging process. A

ceramic probe card designed with pogo probes to pull high currents out of the backside of the GTO is immersed in the Fluorinert bath as shown in Fig. 4.3.

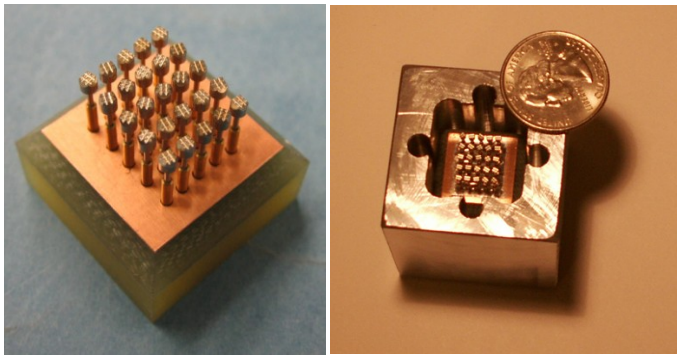

Fig. 4.3. High voltage probe card setup.

The top side is then probed using customized high voltage (20 kV) isolated probe holder designed by *Creative Devices, Inc* , shown Fig. 4.4.

Fig. 4.4. 20 kV isolated probe tip holders.
(Courtesy of Creative Devices, Inc)

The test schematic for the blocking voltage is shown in Fig. 4.5.

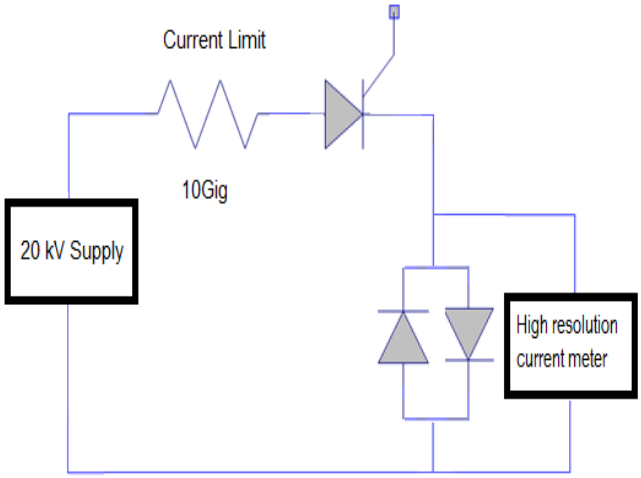

Fig.4.5. Blocking voltage test schematic

A 20 kV power supply from *Glassman High Voltage* is used. The power supply has a manual current limit up to 8 mA, and a voltage resolution of 100V. Two 15 kV, 1% accuracy, 5 GΩ resistors in series are used to limit the current through the devices to 1µA at the device's rated voltage. This will prevent any damage to the device if breakdown occurs. A high resolution 8.5 digit multimeter from *Agilent* is used to measure the leakage current. The multi-meter is placed on the low potential side of the circuit, since both the meter and power supply are grounded, this will guarantee that none of the instrumentation is floating, reducing any risk of damaging the devices or the equipment. Two anti-parallel clamping Schottky diodes are used to protect the multimeter from any voltage spikes. The diodes will clamp any voltage across the multimeter to less than 1V.

A voltage is applied, and a current is measured in the above setup. This allows for de-embedding the effect of the current limiting resistor according to:

$$V_{DUT} = V_{supply} - R_{limit} \times I_{measured} \tag{4.1}$$

Fig. 4.6 shows the test results for the blocking setup. The test was conducted with a bare die

GTO. The test was repeated with the same device after packaging. Due to the 100 V resolution of the supply, the test was stopped at 8 kV to prevent possible damage to the device.

On-State Measurement Test Setup:

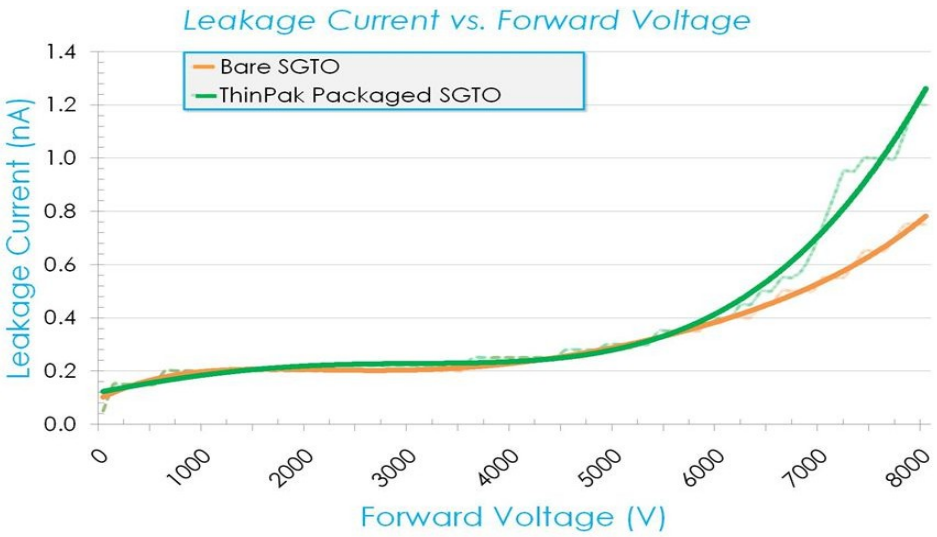

Fig.4.6. Forward voltage blocking test.

It is important to measure the device's performance under forward biased conditions. In this measurement the DUT is forward biased, a gate signal supplied and the current measured. The 371B power curve tracer from *Tektronix* is used for this test.

These devices have very low on-state resistance; therefore, any resistance in the path will have an effect on the measurement. This includes parasitic resistance such as wire, probe and probe holder resistance. This also includes the ohmic contact resistance between the probe tips and the device. This problem is eliminated by reducing these resistances, and using a four point Kelvin measurement.

To reduce the parasitic resistances, 35µm tip probes were used. The thicker probe tips have a larger contact area, reducing the contact resistance. To reduce the backside contact resistance, the

DUT was attached to a substrate that was then probed. This eliminates any resistance variation on the devices backside due to uneven surface, or uneven pressure. This will also reduce any high resistance due to work surface oxidation.

In a Kelvin measurement, shown in Fig. 4.7, there are two separate paths for the current: a path for the supply current and another for the measurement. The effect of parasitic resistance can be eliminated.

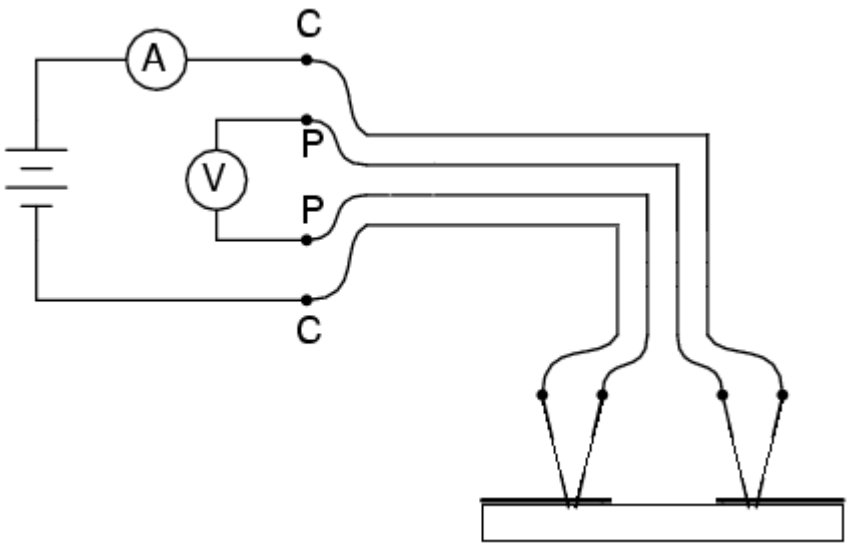

Fig. 4.7. Kelvin measurement test setup.

The 371B has a built in four point measurement option, that is utilized to conduct this type of measurement.

Fig. 4.8 shows the effect of conducting the on-state measurement using the probe card of Fig. 4.3 and with the DUT attached to a substrate.

The same GTO was also tested with different gate current, and after lidding and adding underfill to the device. Results are shown in the figure below.

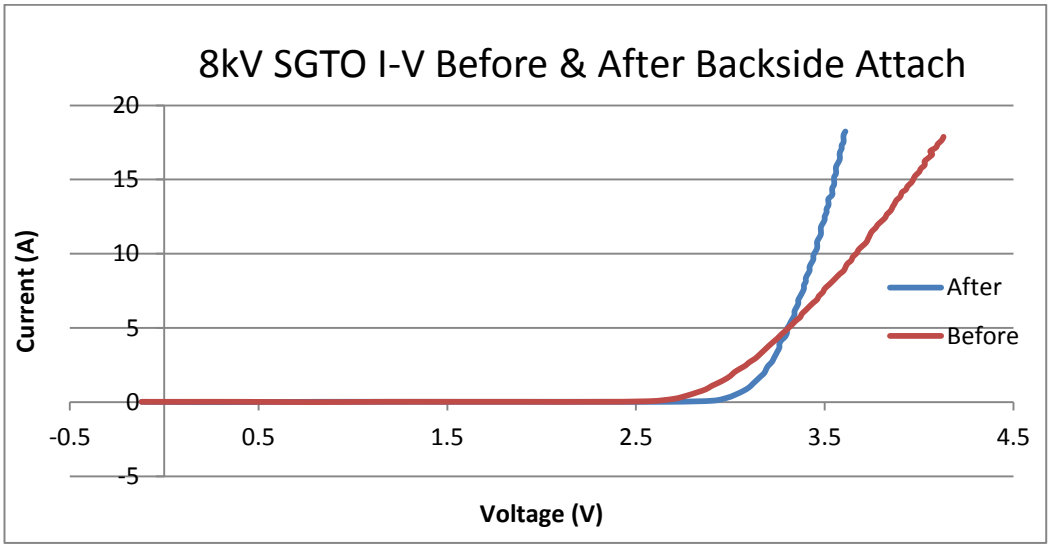

Fig.4.8. Effect of back side contact on on-state measurement.

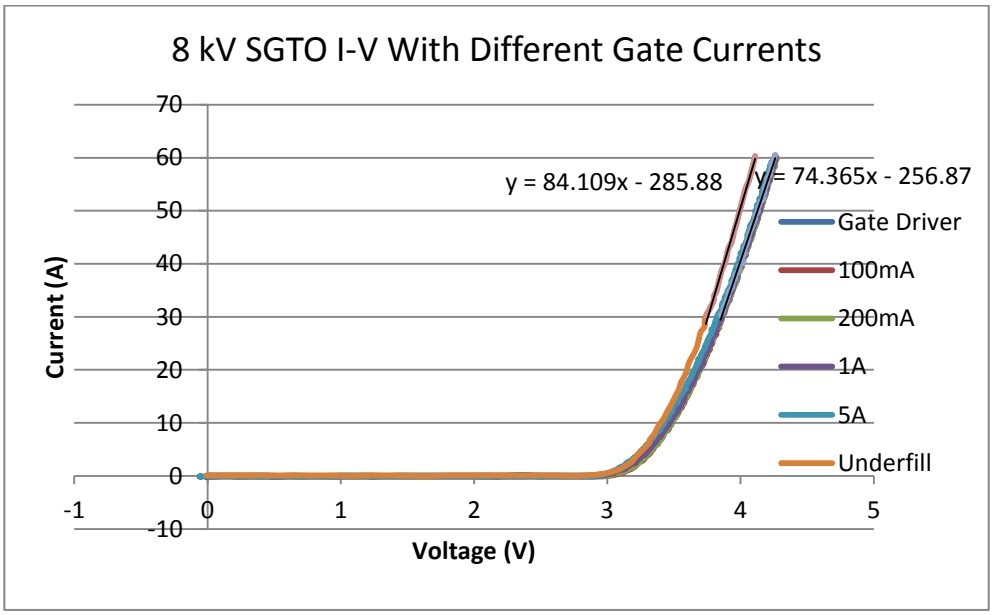

Fig. 4.9. Effect of gate current on on-state performance.

The above results show that the on-state resistance is not a function of the gate current. One of the tests was performed with an external gate driver providing 500 mA of gate current. In the

rest of the measurements, the current was provided by the curve tracer.

It can be noted that the on-state resistance dropped from 13.44 mΩ to 11.9 mΩ after the packaging processing step. The DUT has several anode and gate pads. Before the lidding process only one pad can be probed, and after this packaging step all the pad are shorted. This leads to a more uniform current distribution through the device, and any form of anode focusing is greatly reduced.

SiC semiconductor technology is still maturing. Material defects and processing difficulties still result in variation in devices output characteristics. Fourteen of the devices received in this project are from the same wafer. These devices should exhibit very similar performance. Fig. 4.10 below shows the output on state performance of all these devices.

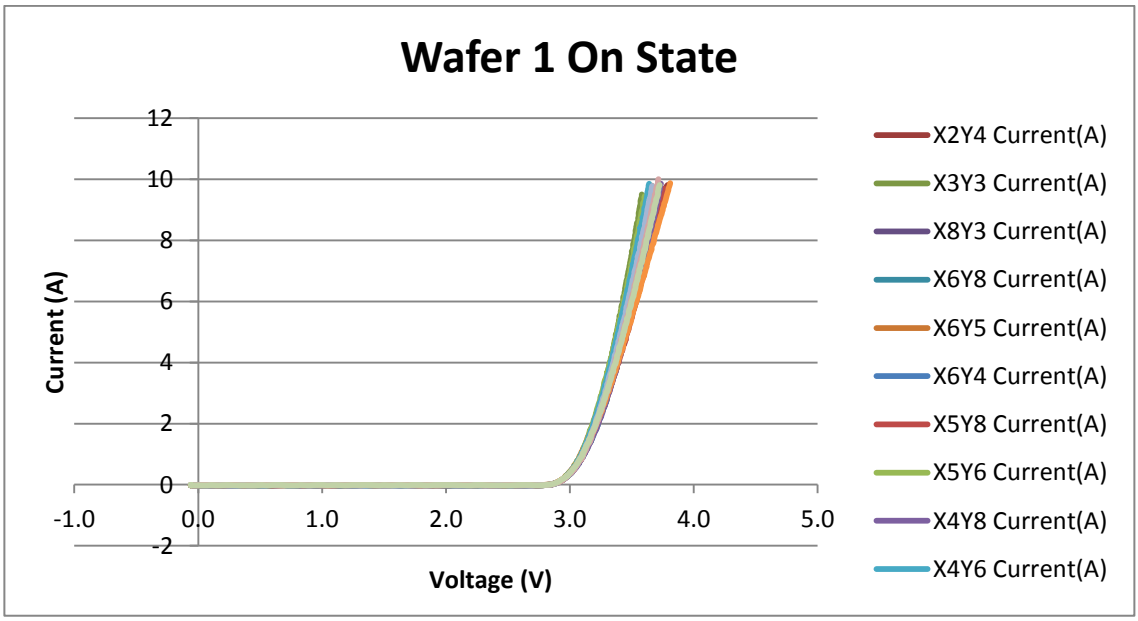

Fig. 4.10. Wafer 1 on state performance.

As can be seen in the above figure, the devices exhibit a noticeable variability in performance. This variability will be even wider at higher current and temperature operation.

Temperature Measurement:

These devices will be operated at a very high power density. The power losses will force the devices to operate at higher temperatures. SiC devices can operate at temperatures up to 600^{o}C, but the existing packaging techniques at the required operating voltages will limit the temperature to 125^{o}C. The device on-state performance will vary with temperature, so it must be characterized at several different temperature points.

A high temperature probe station from *Signatone* is used for this measurement, shown in Fig. 4.11.

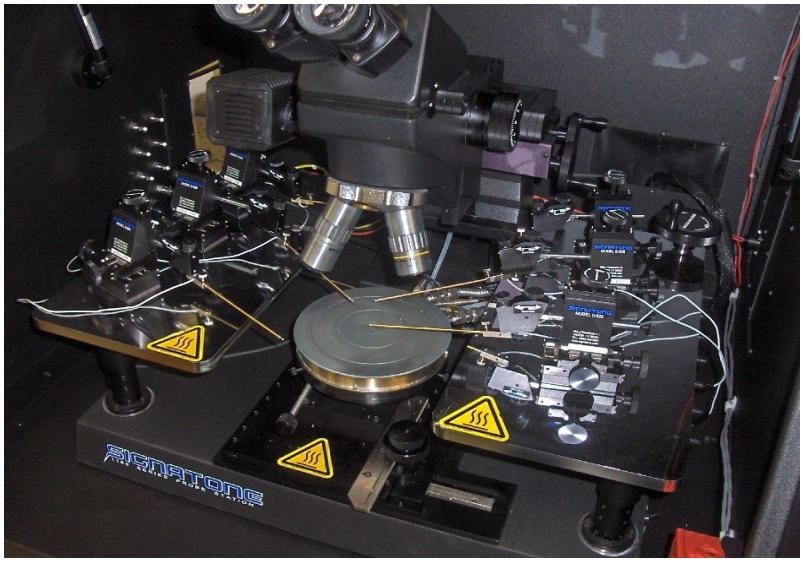

Fig. 4.11. Signatone high temperature probe station.

The probe station has a high temperature chuck that is rated for 500^{o}C operation. The temperature is varied using a sensitive high resolution PID controller. The controller monitors the temperature using two T-type thermocouples connected to the chuck.

Due to the thermal mass of the DUT and the substrate, the setup is soaked to reach the

desired temperature. The temperature is monitored through a T-type thermocouple that is attached to the substrate connected to the backside of the DUT, and an inferred thermal meter.

The above results show that the GTO has a negative temperature coefficient on-state resistance. This means that at a given voltage, the higher the current the higher the temperature

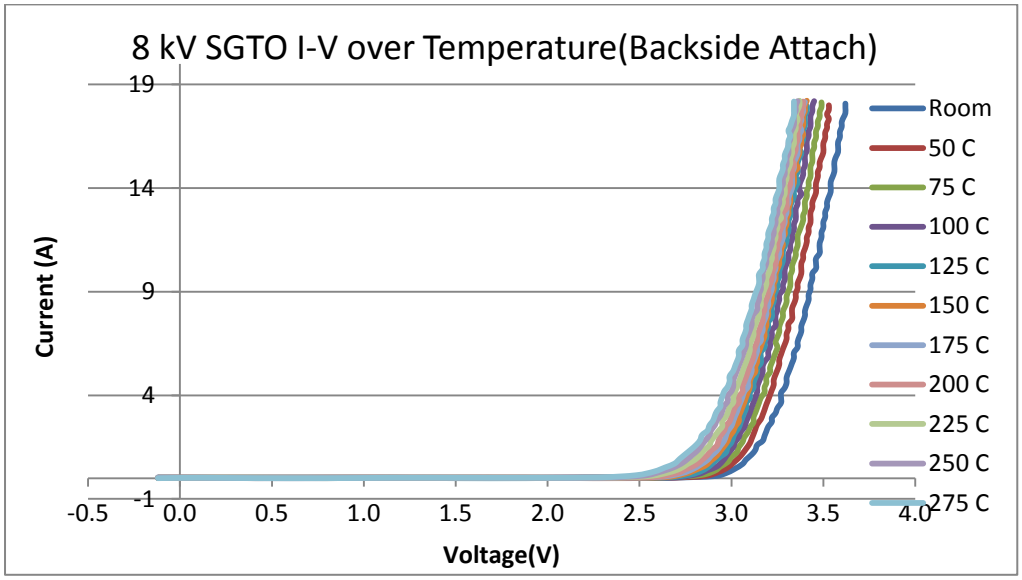

Fig. 4.12. Temperature effect on on-state performance.

rise. At high temperature this translates into lower on-state resistance leading to higher currents again. This is a positive feedback loop that can lead to thermal runaway [39]. This is especially dangerous when paralleling devices, which is necessary given the die size of the available devices. When paralleling devices, any small on-state resistance variation will lead the device with lowest on-state resistance to carry most of the current. This will cause that device to go into thermal runaway, and eventually fail. Then this will happen again to the next best device in a domino effect. Several solutions have been proposed to counter this problem [39], but as the technology matures and device size grows then there will be no need to parallel devices.

Switching Measurements:

Fig. 4.13 shows the schematic for the switching measurement test setup.

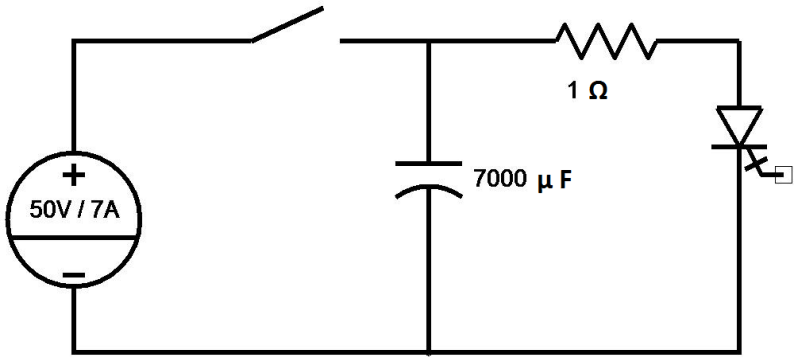

Fig. 4.13. Switching measurement test setup.

When measuring switching performance at very high speeds, it is important to reduce parasitics as much as possible. The goal of this circuit is to measure switching time at rated current and the gate drive performance.

In the above circuit the DC power supply charges the capacitor to 50 V before testing is initiated. The capacitor is charged very fast due to the 7 A capability of the supply, and no current limit. The capacitor value was chosen according to equation 3.3. It will store enough charge to supply 50 A for several cycles of testing.

A 1 Ω ceramic resistor is used as a load and as a current sensor. Ceramic resistors have very low parasitic inductance, and this will reduce any switching delays and voltage spikes. The 1 Ω value was chosen to get 1:1 current to voltage ratio as a current sensor.

Fig. 4.14 shows the turn-on performance of the GTO.

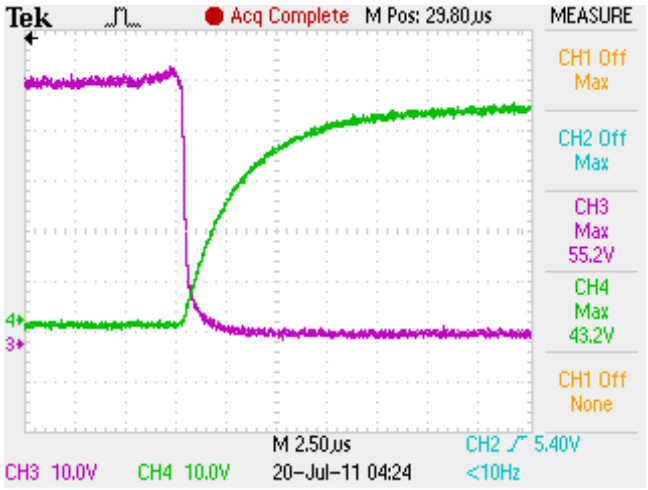

Fig. 4.14 Turn-on waveforms.

In the figure above channel 3 (CH3) is the voltage across the device, and channel 4 (CH4) is the voltage across the 1 Ω resistor, which has the same magnitude as the current through the DUT.

It can be noticed from the above figure that the turn-on time is about 7 µs. This is a speed of 6 A/µs. For current controlled devices, this is a function of the gate current *di/dt*. For GTO applications, anything faster will lead to very high voltage spikes that will prevent the device from soft switching turn on-applications.

Fig. 4.15 shows the turn-off waveforms.

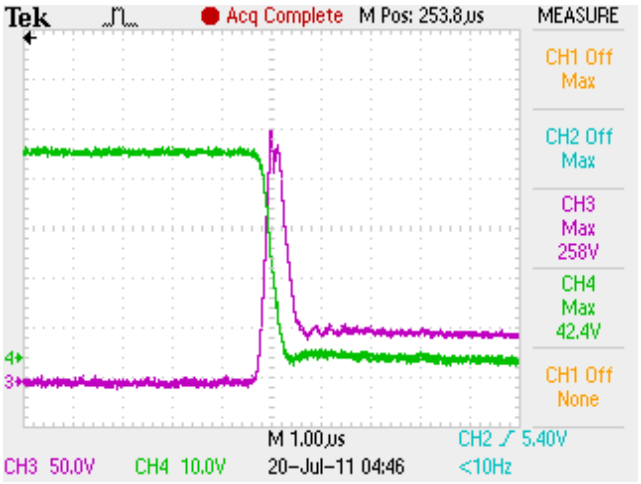

Fig. 4.15 Turn-off waveforms.

For turn-off, the gate driver has no limiting resistor to control the gate current or the gate current *di/dt*. The only thing that control the turn-off in this case is the device. For a GTO to turn off, the stored charge in the device must be discharge out of the gate contact. The speed of this discharge will determine the turn off speed. For maximum turn off, this will require a very low discharge impedance path from the gate. This leads to maximum turn-off speed of about 700 ns, but also results in very high voltage spike of 258 V for a 50 V system. The *di/dt* is 60 A/μs. De-embedding the path inductance for the voltage spike give an inductance of approximately 3.5 μH.

The voltage spike can be reduced by controlling the *di/dt* at turn-off. However, the application intended for these devices required maximum turn-off speed under fault conditions. Under normal operation the device will turn off by natural commutation.

CHAPTER 5

MODEL VALIDATION

5.1.Model Fitting and Results

The developed model has been successfully tested for electrical behavior (feature validation) and a SiC GTO was successfully characterized. It is important to validate the accuracy of the model. This is done by comparing simulated with measured results (accuracy validation).

Fitting parameters are used to fit the model to a specific device's performance. Fitting parameters are related to physical properties of the devices, such a doping, geometry and material properties. A list of model parameters and their default values is shown in Table 5.1 below.

Since this is a physics-based model, model parameters are related to the physical operation of the device. This means that specific electrical behavior is not controlled by only one parameter. For example the on state voltage drop is a function of Q_G, fv, Q_{Bn}, but Q_{Bn} also effect the blocking voltage. An individual parameter will usually affect several different device output waveforms, producing a coupling effect of parameters.

To make the model more useful and attractive to the end user, a parameter extraction guide that relates model parameters to device performance is developed. A sensitivity-based inspection regarding the effect of parameter changes on performance (output waveforms) is employed.

Table 5.1 Default Model Parameter Values.

Model Parameter	Parameter Description	Default Value
Q_{GP}	Thermal equilibrium hole charge in gate region	3×10^{-13}
Q_G	Thermal equilibrium electron charge in gate region	5×10^{-3}
Q_{Bn}	Thermal equilibrium electron charge in base region	3.5×10^{-17}
Q_B	Thermal equilibrium hole charge in base region	1.2×10^{-3}
T_{n20}	Equilibrium electron transient time from node 3 to 4	40µ
T_{n30}	Equilibrium electron transient time from node 5 to 6	5µ
R_{sh}	Base region short	10
fv	Gate to base volume ratio	0.08
V_{j2BK0}	Breakdown voltage of J2 junction	100
V_{j3BK0}	Breakdown voltage of J3 junction	8k
f_{j2g}	Gate side depletion region factor	.2
τ_B	Base lifetime	18µ
τ_G	Gate lifetime	5µ
mr_{low}	Mobility ratio in low doped region	2
mr_{high}	Mobility ratio in heavy doped region	3.5

Certify [41], a model optimization and analysis tool developed by the MSCAD group at the University of Arkansas, is used to aid the development of the parameter extraction guide. The goal of the parameter extraction guide is to identify to the user what parameters to optimize and used to fit an output waveform. This simplifies the fitting process to the user.

Certify requires the model, the measured device data to be fit, and the simulation circuit

netlist. It can then be used to analyze the sensitivity of the output waveform to a specific parameter, or to optimize parameters to the waveforms. This gives the user the ability to analyze the parameters without working knowledge of the model's internal physical equations.

The sensitivity analysis shows that output performance is typically dominated by a small subset of parameters. These are summarized in Table 5.2 below.

Table 5.2. Summary of Model Parameter Output Effects.

Output Effect	Controlling Model Parameters
On-State Voltage Drop	Q_G, *fv*, Q_{Bn}
On-State Resistance	Q_B,Q_{GP} T_{n20}, T_{n30}
Blocking Voltage	Q_{Gp}, Q_{Bn}, T_{n20}, T_{n30}, τ_B, *Vj3BK*, *fj2*,
Turn-On Time	*murlow*, *murhigh*, τ_B, τ_G, Q_{Bn}
Turn-Off Time	Q_{Bn}, Q_B,Q_{GP}, T_{n20}, τ_B,

On-Stave IV curve:

The two critical regions in the "On State IV curve" are: the on region, and the off-state to on-state transition region. The on region is fit by fitting the on state resistance using Q_B, Q_{GP} and T_{n30}. The on state voltage drop is controlled with Q_G and *fv*. The curvature of the transition region is controlled by T_{n20}.

Blocking Curve:

The forward blocking voltage maybe fitted using several of the model parameters. For simplicity, and to reserve some of the parameter for other fitting curves *Vj3BK* and *fj2,* are used.

Switching Measurements:

The turn on and turn off curves are controlled by many of the same parameters. For turn on *murlow, murhigh* and τ_G are used. For turn off Q_{Bn} and τ_B are used.

Below in Fig. 5.1 is the forward blocking fit.

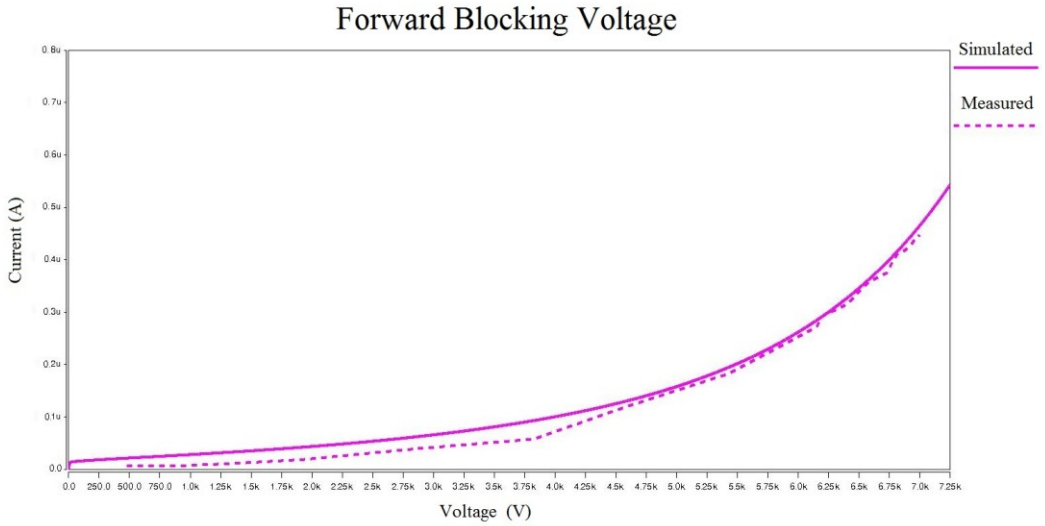

Fig. 5.1. Forward blocking waveforms of model and measured data.

It can be concluded from the above figure that the model fits the measured device's blocking performance very well.

Fig. 5.2.shows the model's forward on-state conduction I-V characteristic fitted to the I-V characteristic obtained using the experimental setup.

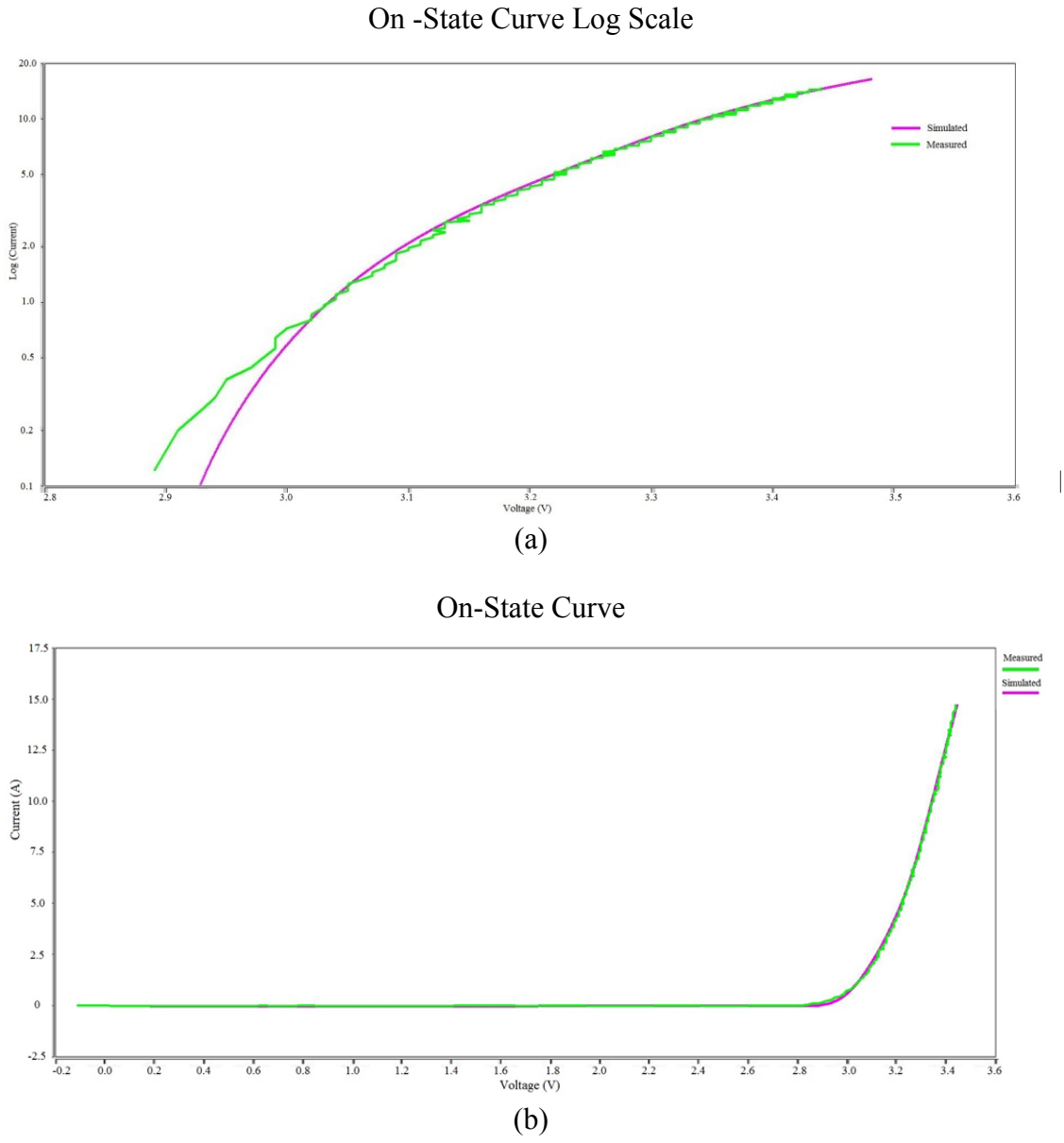

Fig. 5.2. Forward on-state curves of measured results and model. (a) Log Scale (b) Linear Scale.

Again, from the above figure, it can easily be concluded that the model accurately matches the measured device's performance.

Fig. 5.3. below shows the model's temperature prediction.

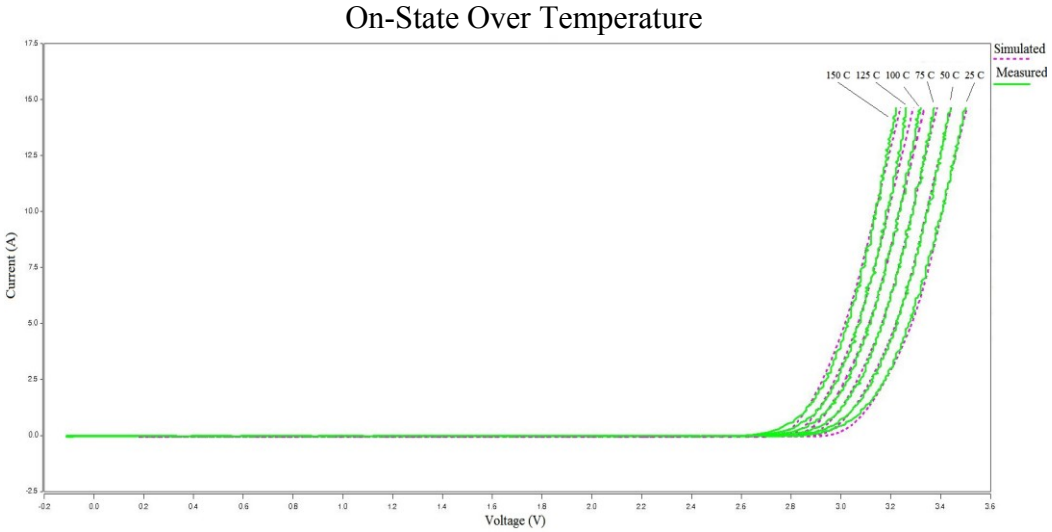

Fig. 5.3.Model and device performance over temperature.

In the figure above, on state waveforms for a device from room temperature up to 150 ^{o}C in 25 ^{o}C increments is shown. The wave form on the far right is room temperature, and the waveform to the far left is 150^{o} C. Again the model shows high fidelity in producing accurate output waveforms.

Figs. 5.4 and 5.5 shows the transient fits.

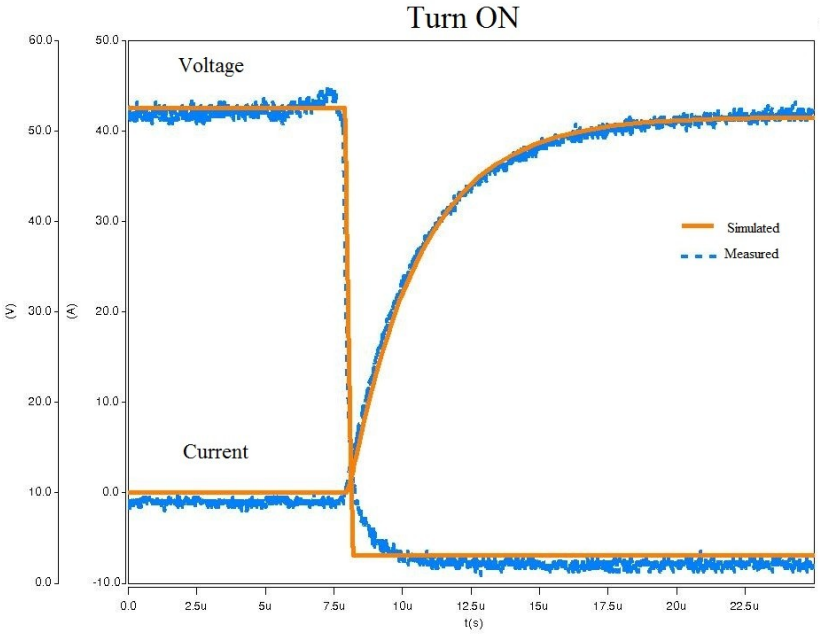

Fig. 5.4.Turn-on performance of device and model.

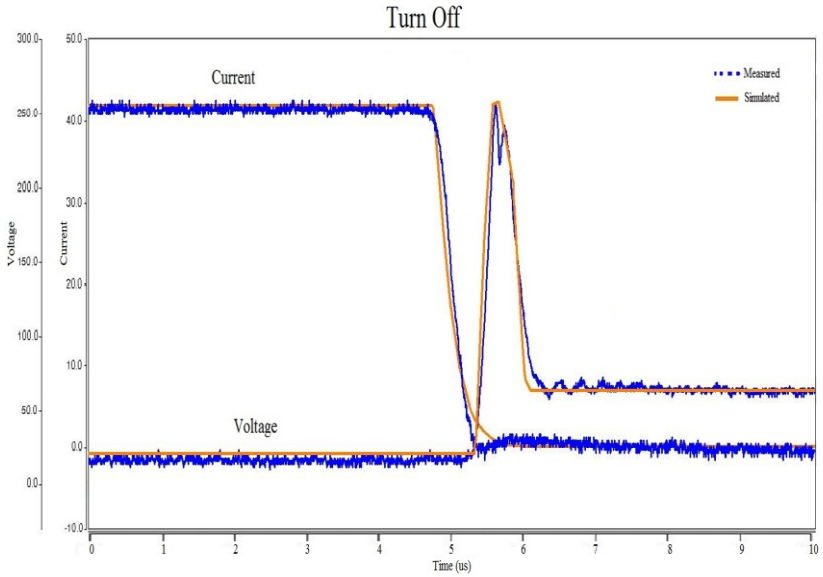

Fig. 5.5. Turn-off waveforms.

In Figs. 5.4 and 5.5 it can be noticed that the time and transient mechanism for the current and voltage to reach steady state accurately reflects that of the device. Again the model accurately reflects the measured device's performance.

Table 5.3 is a summary of the model's performance when compared with measured data.

Table 5.3.Summary of Model's Performance.

Parameter	Measured	Simulated
Blocking Voltage (kV)	7.25	7.25
On-Resistance (mΩ)	13	13
Turn-Off Time (μs)	1	1
Turn-On Time (μs)	7	7

Even though no circuit data is currently available, it is still of value to show the model's performance in an application. Fig. 5.6 below shows the schematic of a full bridge rectifier that was simulated using the developed model.

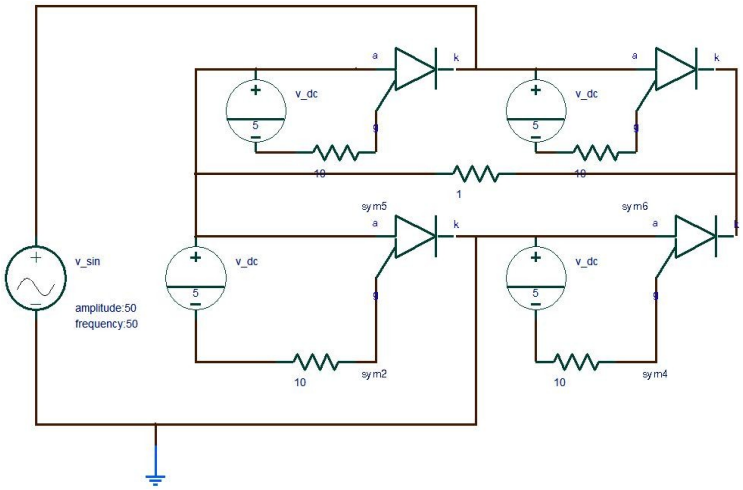

Fig. 5.6. Simulated full bridge rectifier circuit.

Fig. 5.7. Shows the output current waveforms of the full bridge, and a half bridge rectifier.

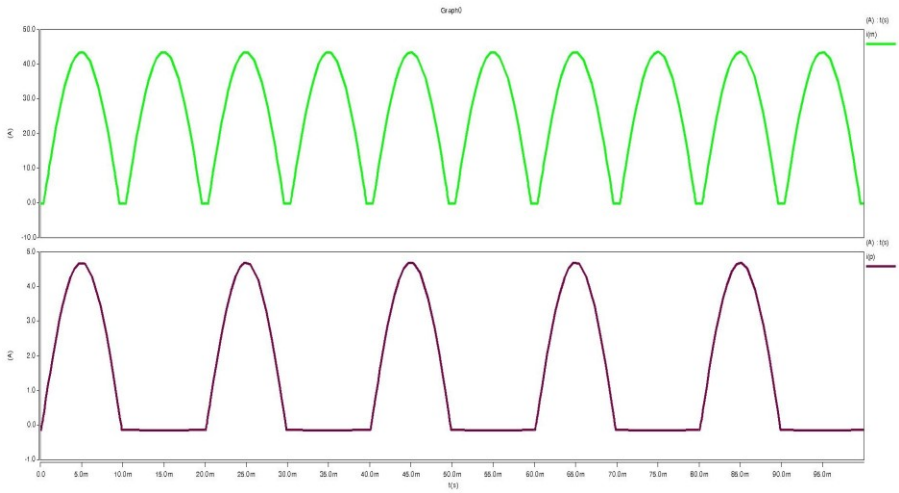

Fig. 5.7. Output current of simulated half bridge and full bridge rectifier.

The model accurately describes the performance of both the full bridge and half bridge rectifying circuits.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

A SiC p-type GTO model has been developed and implemented in the Saber circuit simulator. The model accurately describes GTO physical behavior, including temperature effects. This is the first physics based SiC GTO model. This model will help deploy cutting edge future smart power electronics systems in a wide variety of applications, including extreme environments, transportation, and the electrical grid.

For this research project to be complete, the model had to be compared to measured results. This required a full characterization of first generation SiC GTOs. Both static and transient measurements were successfully conducted, with customized non-destructive test setups.

To be able to accurately measure and operate these devices, a unique gate drive topology was designed, prototyped and used. The topology is flexible enough to be used with wide range of differently rated GTO devices.

Parameter extraction procedures and guides are important to enable the use of the model. This enables the circuit designer to fit the model's performance with any device, without any necessary working knowledge of the models internal physical equations or operation. With physics based models this can prove difficult as many of the parameters may be coupled. Using the Certify modeling optimization and analysis tool, a sensitivity study was conducted. This study enabled a much clearer understanding of the model parameters, resulting in simpler parameter fitting guide.

SiC high voltage device technology is still maturing. Only recently have 1.2 kV MOSFET and BJTS become commercially available. The higher voltage rated devices still have a way to

go before being commercialized. Challenges to these devices include yield, active area, and blocking layer.

Improving the yield will dramatically decrease the price. This will increase their usage in end user products, where price is a large factor. Increasing the active area will increase the current rating of the device, making it possible for high current applications without having to parallel a large number of devices. Paralleling high voltage devices is difficult due to the negative temperature coefficient of the devices. Traditionally, bipolar (GTOs and BJTs) devices have a negative temperature coefficient of on-state resistance, while unipolar (MOSFETs and IGBTs) devices have a positive temperature coefficient. This is not true of very high voltage (>10kV) devices with a thick lightly doped blocking epitaxial layer. The epitaxial layer's negative coefficient dominates for both types of devices. The GTO will be the first high voltage SiC device that resolves most of these issues due to the well understood simpler structure, and the lack of an oxide.

6.2 Recommendations for Future Work

For future work, more standardized automated test setups can be developed. This can include custom test boards that are fitted with appropriate test equipment connectors to reduce any circuit parasitics. This is especially important in order to have a good frame of reference among a large number of devices. Due to the nature of currently available SiC devices, there is a large variability in performance between the devices. Automated test setups will remove many external variables. Adding automation to these setups will increase measurement accuracy and reduce test time.

Improvement to the model computational speed is also recommended. This model will be used in complex systems, with many devices and other circuits in the simulation. Improvement on the simulation speed, while preserving accuracy, is always desired.

All modern power electronic systems are electromechanical in nature, with the electrical and mechanical aspects coupled. For example, the power loss in the electrical system relates to the temperature rise in the mechanical system. The building block of these systems is power modules. A single module may contain the power stage, control layer and feedback sensors. The module as a whole must be fully analyzed, characterized and studied for proper system design. This makes module models extremely important for proper system simulations. Developing module models entails combining the proper individual electrical and mechanical models into one coherent package. This will require coupling the electrical system to the thermal system, and having direct feedback in both directions.

The developed GTO model accounts for temperature effects. This can be especially valuable in a module model where thermal-electrical simulations are run. This will require developing accurate thermal models of the GTO cooling system interaction and interface. Other mechanical models that relate the GTO package to the module will also be necessary. This will include modeling stress, parasitics and thermal spreading. This will be crucial in a complete system design development, and in basic system studies such as thermal runaway.

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