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High Voltage Direct Current Energy Transmission Using Modular Multilevel Converters

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by

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ABSTRACT

This thesis focus on high voltage direct current (HVdc) energy transmission using modular multilevel converter (MMC) based terminals. It provides a brief comparison between different HVdc technologies, focusing on voltage source converters (HVdc-VSC) with the MMC-based terminal emerging as the topology of choice for ratings less than 1 GW. The controllers for a two-terminal HVdc-link are analyzed and Matlab/Simulink™ simulation models are presented. The simplified models and full Matlab/Simulink™ based model are used to select the gains for the MMC controllers. Simulation results carried out on the full model validated the proposed methodologies. A new control technique that eliminates the voltage sensors on the grid side normally used to synchronize the MMC-based terminal with the grid is proposed. The performance of proposed technique was evaluated through Matlab/Simulink™ simulations by considering inverter operation. The sensorless technique is able to synchronize a MMC-based inverter terminal to a grid under non-ideal conditions as well to accurately detect changes in the grid voltages. Finally, an analysis of the impact that a 15-kV SiC IGBT would have on HVdc MMC-based terminals is presented. The analysis evaluates parasitic inductances within the sub-module (SM) of an MMC, changes on the required SM capacitance, and impact on the voltage waveform THD. The evaluations showed that the 15-kV SiC IGBT would be only suitable if the module is rated 400 A or greater.

ACKNOWLEDGMENTS

DEDICATION

Esta tesis va dedicada a mis padres, Zuleika y Julio. Gracias por el amor incondicional, apoyo y consejos que me han brindado desde el día en que nací. Esta tesis no hubiera sido posible sin ustedes, los amo.

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CHAPTER ONE

INTRODUCTION

1.1   Brief History of HVdc Energy Transmission

The idea of using high voltage direct current (HVdc) systems for energy transmission is not new. The first energy distribution systems in the USA were direct current (dc) systems since lines were short. The dc systems in the USA were challenged by the alternate current (ac) systems at the end of the 1880's in what is known as the "War of the Currents" [1]. At that time, the dc power had to be generated close to where it was consumed, since the generated voltages were relatively low, so long distance transmission was not possible. Furthermore, increasing or decreasing the dc voltage was also not possible, so loads that required a different voltage needed separate generating sources. These were some of the technical reasons that led ac systems to become the most practical choice for energy transmission at that time.

In the early 1920's, the limitations of the ac systems over long distances and for submarine cables were recognized. It was not until 1954 that the first commercial HVdc project was built because of the maturity and commercial availability of mercury arc valves [2]. This first HVdc project was built to transport electric power between the Sweden mainland and the island of Gotland, and had a power rating of 20 MW. In 1970, the HVdc link of the island of Gotland was upgraded to handle 30 MW of power. To make this upgrade possible, the system was re-engineered using the first thyristors valves for a commercial HVdc project. In 1997, the first project using voltage source converters (VSC) based on IGBT's was commissioned to ABB [3].

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Since 1997 several HVdc terminals using VSC have been built around the world. In 2003 a new topology was proposed for terminals using VSC technology. This topology was called the modular multilevel converter (MMC) [4]. With the coming of the MMC and the technological advances in semiconductor devices, HVdc has become a feasible technology for integrating renewable energies with power grids all over the world [5]. Recently, Europe has been planning a dc grid, to interconnect different sources of energy and increase the stability of the regional grid [6].

1.2   History HVdc in the United States of America

The first HVdc project in the USA, built in 1932 by General Electric Company, was an experimental station located between Mechanicville and Schenectady, NY [7]. It was not until 1970, however, that the first commercial HVdc project was commissioned: the Pacific DC Intertie. The goal of this project was to connect the hydro-electric power in the state of Oregon with the load centers in Los Angeles, CA. The Pacific DC Intertie was the first of many other HVdc projects in the USA. Among these other projects is the Quebec – New England Transmission, which has two stages. The first stage has two stations located between Sherbrook, Quebec (Canada) and Monroe, New Hampshire (USA). Stage two included three additional terminals to the connection. This made the Quebec – New England Transmission the only multi-terminal HVdc project in the USA [8].

Soon after the Quebec – New England additional terminals were finished, the Trans-Bay Cable project was built, and started its operations in 2010 between San Francisco, CA, USA and Pittsburg, CA, USA, becoming the first project in the USA to use a modular multilevel converter (MMC), utilizing HVdc-VSC based terminals [9]. The location of the HVdc projects in the USA

as of February 2013 is shown in Fig. 1.1 [10]. More recently the "Tres Amigas" project has been awarded to Alstom to implement a 750 MW VSC-HVdc project [11].

1.3   Thesis Motivation

The increasing penetration of renewable energy sources in power grids is expected to play a significant role in the future. In some cases, renewable energy sources such as wind are located off shore, and bringing this power to the mainland can be a challenge.

One of the alternatives for solving these problems is using HVdc transmission whose use is not limited to integrating renewable energy sources into power grids; it can also interconnect two different grids between two countries.
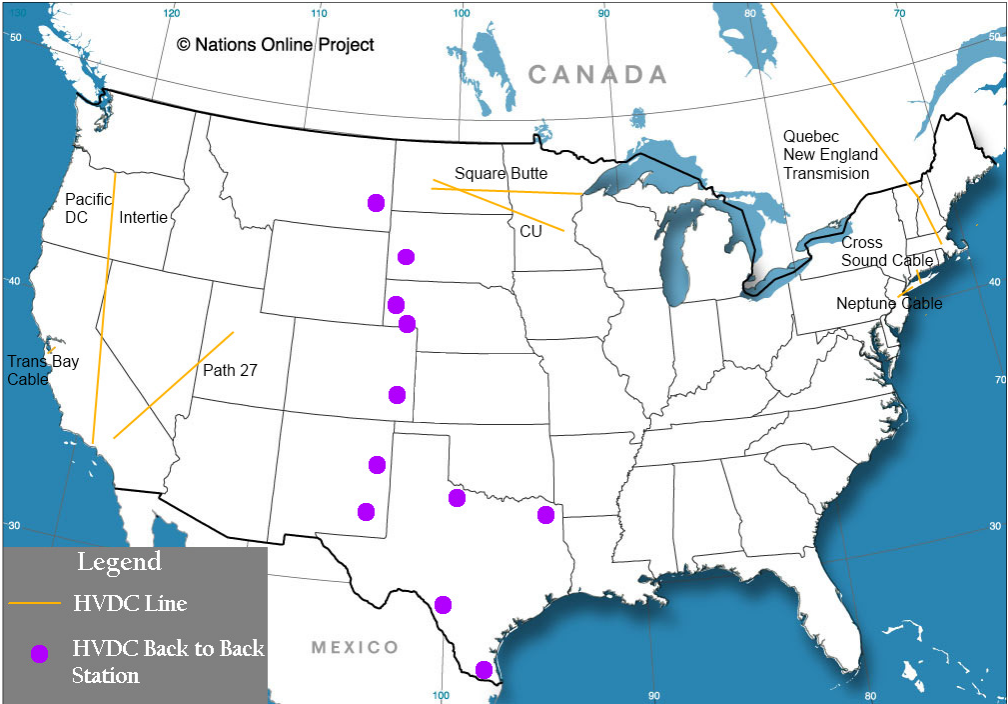
Fig. 1.1. HVDC Projects in the USA [12]

An example of a case where two countries' power grids can be connected by an HVdc system is the plan to interconnect the grids of Panama and Colombia [13]. The author of this thesis was born and raised in Panama. The interconnection of Panama and Colombia will be the first HVdc project made in Panama and it is of great interest of the author to contribute towards the realization of this project. To contribute with the realization of this project, the author needs a deeper understanding of how HVdc technology works. This knowledge can be acquired by doing research and learning the state of the art in HVdc. Therefore, simulations models are selected as a learning and research tool for gaining a deeper understanding in HVdc technologies.

1.4   Thesis Objectives

The main objective for this thesis is to analyze the different technologies used for transmitting power between two points, focusing on MMC-based HVdc systems. To accomplish the main objective, the enabling objectives are:

- To familiarize the reader with modular multilevel converters for HVdc applications.

- To build a simulation model of the interconnection of two ac-grids using an HVdc link. Both terminals will be MMC-based. The terminals will be placed in Panama and Colombia to represent the planned interconnection between these two countries [13].

- To implement a sensorless control technique for connecting the MMC-based inverter terminal with the grid. This technique eliminates the grid-side voltage and current sensors used to synchronize an MMC-based terminal with a grid.

- To analyze the impact of a high voltage device on MMC-based terminals for HVdc applications, with a focus on SiC IGBT's.

1.5   Thesis Organization

To achieve the main objective of this thesis the following chapters are proposed:

- Chapter Two presents the reasons for using HVdc transmission. Different HVdc technologies are compared and analyzed. The principles of operation of the MMC and the selection of the passive components are also detailed in this chapter.

- Using Chapter's Two background theory, Chapter Three shows a methodology to calculate the various for the controllers of an HVdc systems as wells as the controllers to control the capacitor voltages and circulating currents within the MMC-based terminal using simplified Matlab/Simulink™ models.

- Using the controllers presented in Chapter Three, Chapter Four presents a full Matlab/Simulink™ based simulation model of a two-terminal HVdc link and implements a sensorless control technique to connect the inverter terminal of an HVdc system with a grid. The performance of this sensorless control technique is evaluated under ideal and non-ideal grid conditions [14].

- Chapter Five explains the impact of a high voltage, fast switching device in the MMC realization. The study includes the impact on the number of sub-modules required, the capacitance of the sub-module, and the possible impacts in the THD of the system [15].

- Chapter Six summarizes the work done, presents the conclusions of the research and recommendations for future work are presented as well.

References

[1]   B. Finn, "Origin of Electrical Power", National Museum of American History, [Online]. Available: http://americanhistory.si.edu/powering/past/prehist.htm [Accessed: Feb. 1, 2013]

[2] O. Peake, "The History of High Voltage Direct Current Transmission," *presented at the Australasian Engineering Heritage Conference*, 2009.

[3] ABB "Tesla vs. Edison: the war of currents" [Online] Available: http://www.abb.com/cawp/seitp202/c646c16ae1512f8ec1257934004fa545.aspx [Accessed: Feb. 1, 2013]

[4] A. Lesnicar, R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *Proceedings of Power Tech Conference, 2003 IEEE Bologna* , vol.3,pp. 23-26, June 2003.

[5] N. Ahmed, A. Haider, D. Van Hertem, Lidong Zhang, and H.-P. Nee, "Prospects and challenges of future HVDC SuperGrids with modular multilevel converters," *Proceedings of the 2011-14th European Conference on Power Electronics and Applications*, 2011, pp. 1–10.

[6] P. Fairley, "Germany jump-starts the supergrid," *Spectrum, IEEE* , vol.50, no.5, May 2013

[7] J.A. Besha, "The Historic Mechanicville Hydroelectric Station. 1. The Early Days [History]," *Industry Applications Magazine*, IEEE, vol.13, no.1, pp.8-11, Jan.-Feb. 2007.

[8] ABB "History of ABB's HVDC expertise" [Online] Available: http://www.abb.us/cawp/seitp202/7cfd9a3a7416a383c1256e8600406f4f.aspx [Accessed: Jan. 31, 2013].

[9] H.-J. Knaak, "Modular multilevel converters and HVDC/FACTS: A success story," *Proceedings of the 2011-14th European Conference on Power Electronics and Applications*, vol., no., pp.1-6, Aug. 30 2011-Sept. 1 2011.

[10] University of Idaho "HVDC Projects Listing" [Online] Available: http://www.ece.uidaho.edu/hvdcfacts/Projects/HVDCProjectsListingMarch2012-existing.pdf [Accessed: Dec.3, 2012]

[11] Alstom "Alstom Grid will provide Tres Amigas LLC in the USA with first-of-its-kind Smart Grid "SuperStation"" [Online] Available: http://www.alstom.com/press-

centre/2011/4/Alstom-Grid-will-provide-Tres-Amigas-LLC-in-the-USA-with-first-of-its-kind-Smart-Grid-SuperStation/ [Accessed: Jun. 2, 2013]

[12] Nations Online [Online] Available:
      http://www.nationsonline.org/oneworld/usa__blank_map.htm [Accessed: Jun.26, 2012]

[13] Inter-American Development Bank "Colombia-Panama Interconnection" [Online]
      Available:
      http://www.iadb.org/en/projects/project-description-title,1303.html?id=rs%2Dt1241
      [Accessed: Jan.31, 2013].

[14] Escobar-Mejia, D. Guzman, J.C. Balda and C. Busada, "New Control Technique for
      Sensor-less Grid Synchronization of Modular Multilevel Converters for HVDC Systems,"
      Proceedings of the IEEE Energy Conversion Congress & Exposition, 2013.

[15] D. Guzman, J.C. Balda, "The Impact of High-Voltage and Fast-Switching Devices on
      Modular Multilevel Converters", *Proceedings of the Applied Power Electronics
      Conference and Exposition*, 2013.

CHAPTER TWO

HIGH VOLTAGE DIRECT CURRENT ENERGY TRANSMISSION

Abstract

This chapter explains the advantages of HVdc transmission over HVac transmission and provides a comparison between different HVdc technologies focusing on HVdc-VSC, more specifically in modular multilevel converters (MMC). Some of the advantages of the MMC over others HVdc-VSC topologies are presented and the fundamental principles of operation of the MMC are explained. With the information presented in this chapter the reader should be able to have a basic understanding of the different classifications within HVdc technologies and the fundamental operating principles of MMC.

2.1 Introduction

When compared with high voltage alternate current (HVac) energy transmission, HVdc has several advantages that can be summarized as follows [1]-[3] :

- No technical limit for underwater cable distances.

- More power capability per cable.

- Lower losses per line; 20% less losses when compared to a HVac line.

- Power transmission over long distances.

- Does not require synchronous operation; can connect to ac systems with any frequency.

- Does not increase the short-circuit current of the switchgear of the connecting ac systems.

- It is possible to use the ground as a return path; therefore, each conductor could be controlled as an independent circuit.

These advantages over HVac have made HVdc the technology of choice for transmitting power over long distances and for offshore transmission. After choosing HVdc, the next stage is to choose the converter technology for implementing the HVdc system. The specific technologies are line-commutated current-source converters (CSCs or HVdc-CSC), and voltage source converters (VSCs or HVdc-VSC) [1]. This Chapter provides a detailed explanation and comparison of the above two technologies and analyzes, in particular, the topology of the MMC.

2.2   Current-Source Converters

This is the oldest and most used technology in HVdc systems [4] and is currently the most cost-effective alternative for power ratings over 1.2 GW 0. This technology employs thyristors as switches to change from ac to dc, or vice versa. The thyristors are configured as a three-phase, full-wave bridge rectifier as shown, in its simplest form, in Fig. 2.1. This configuration is also known as a six-pulse bridge, named after the harmonic ripple it produces, which is six times the fundamental frequency on the ac voltage side. The inverter topology is similar. To mitigate the harmonics effects and reduce the size of the ac filters, a twelve-pulse configuration can be used. The twelve-pulse configuration consists of two six-pulse arrangements connected to Y–Y and Y–Δ transformers, as shown in Fig. 2.2. Filters are placed at both sides of the rectifier to mitigate the switching noise. The ac-side filters are also used to provide reactive power to the converter. Rectifier and inverter operation demand reactive power from the ac system due to the commutation process; this can be described as the current transfer between phases due to the thyristors switching [6]. Therefore, the ac current lags the voltage during the converters normal operation. The ac system connected to the CSC has to provide the reactive power to the CSC if the ac filters are unable. Thus, the CSC is required to be connected to a strong ac system to keep its stability.

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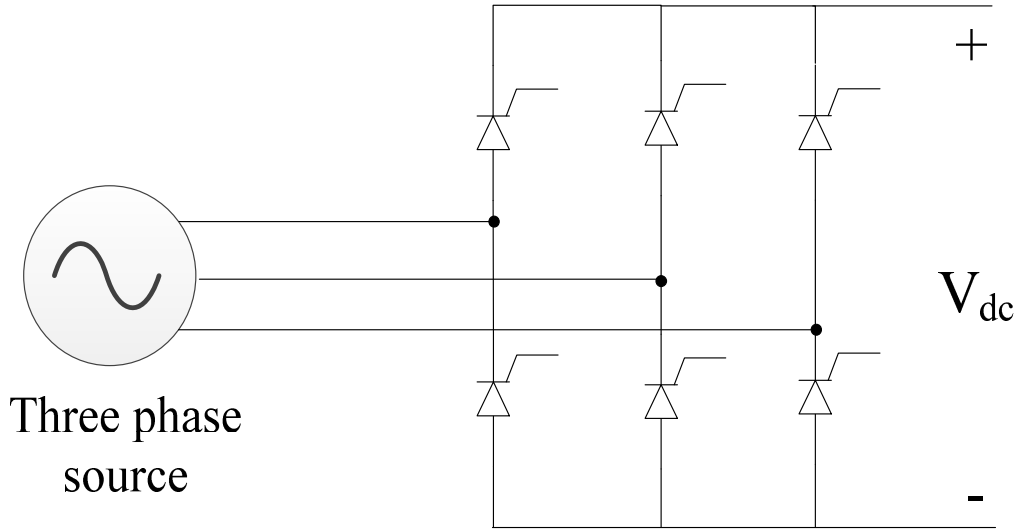
Fig. 2.1. Six-pulse rectifier
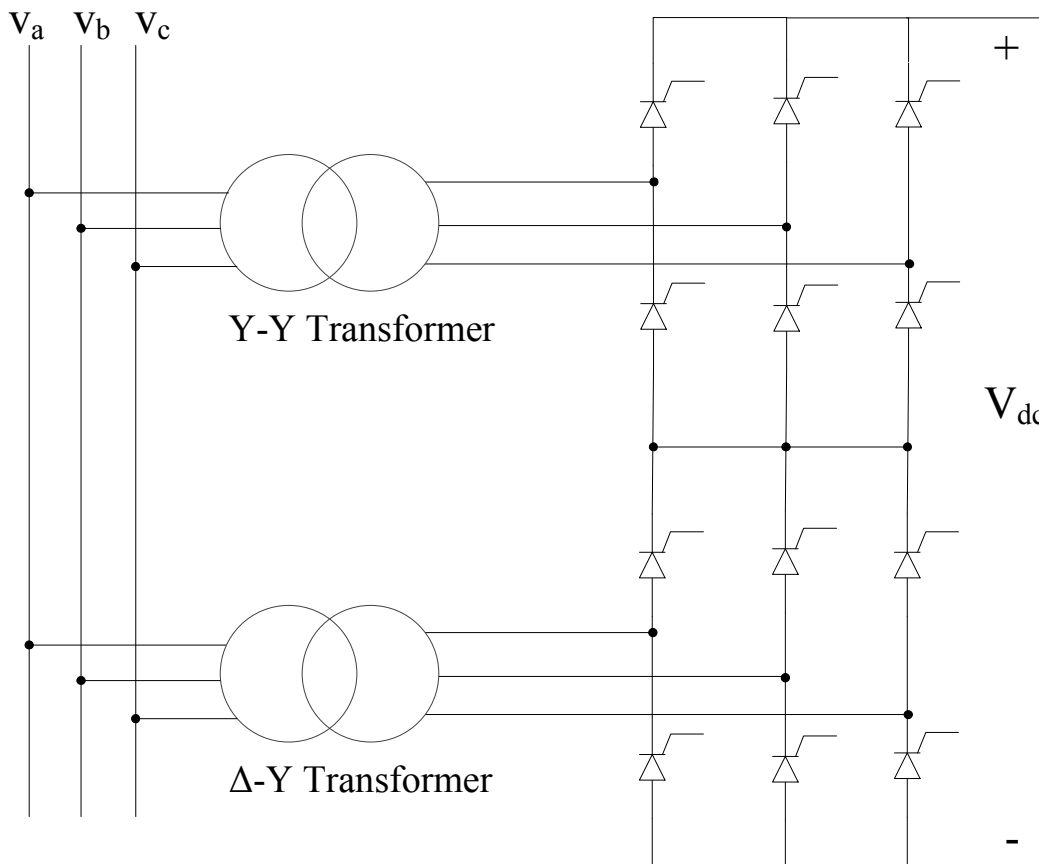
Fig. 2.2. Twelve-pulse rectifier

In order to connect to weaker ac systems, series capacitors are connected between the transformers and the valves to compensate for the reactive power; these are known as capacitor-commutated converters (CCCs).

The controllers of the CSCs or CCCs can only control the active power, and in order to change the power flow, the polarity of the terminals must be reversed. The filters required for an HVdc-CSC link to operate are very bulky and take up most of the space in the HVdc substation, up to 75%. These are some of the drawbacks of the HVdc-CSC links which, despite these drawbacks, are widely used in the USA and around the world to transmit high amounts of energy over long distances. The popularity of HVdc-CSC links is due to the maturity of the technology. This was the first engineering solution proposed by the manufactures, such as ABB 0. When HVdc-CSC was first proposed, mercury valves where used as switches [7]. Each switching position requires several series-connected switches to satisfy the voltage isolation requirements. Voltage isolation and current capability make thyristors the best switch for a high power HVdc-link.

2.3   Voltage-Source Converters

To overcome the limits in the controllability of the HVdc-CSC, it is necessary to be able to control the turn-on and turn-off of the switches. The VSC uses IGBTs to control the turn-on and turn-off of the switch, and the IGBTs are voltage controlled using pulse width modulation (PWM). The VSCs are able to control active and reactive powers independently, and can be controlled as a synchronous generator [6]. Fig. 2.3 presents a simplified three-phase, two-level VSC. It is called two-level because it produces two different ac voltage levels when it is working as an inverter: $+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$, using the midpoint of the dc bus as the reference.

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However, the two-level VSC still requires bulky filters at the output. To overcome this limitation, multilevel converters were proposed [8]. The main multilevel converter topologies are: diode-clamped multilevel converter, flying capacitor multilevel converter and modular multilevel converter [9]. The latter is preferred by manufacturers due to the advantages given in Section 2.4. HVdc-VSC terminals using MMC are compared to the HVdc-CSC terminals in Table 2.1 [2].

Currently it is not economically to make an HVdc-link over 1.5 GW using HVdc-VSC so, all of the projects that are over this power rating use HVdc-CSC technology. Likewise, a new project below 1.5 GW is expected to use the HVdc-VSC technology. Currently, the two technologies coexist together, and some HVdc links have been changed from HVdc-CSC to HVdc-VSC for increased controllability [11].
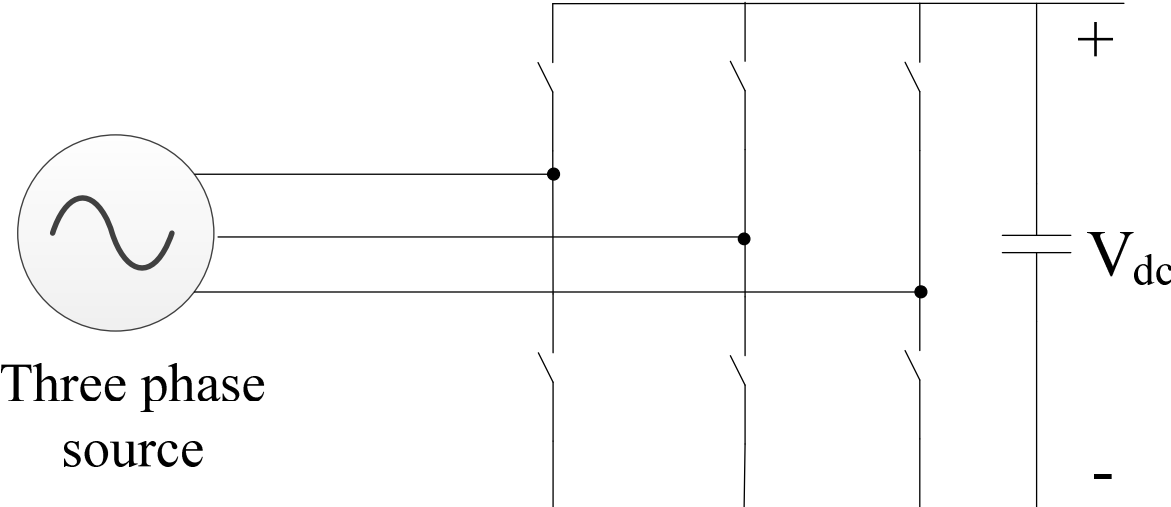
Fig. 2.3. Simplified voltage source converter topology

Table 2.1 . HVdc-CSC and HVdc-VSC Comparison [2], [10]

HVdc-CSC		HVdc-VSC	
Advantages	Disadvantages	Advantages	Disadvantages
Low cost	High harmonics content	Low harmonic content	Higher cost
High power rating	Filters require a large area	Control of active and reactive power	Limited power rating **due to power devices**
Reliable and robust	Requires polarity reversal to change power flow	No polarity reversal required to change power flow.	Low overload capability **due to power devices**
Low losses	Multi-terminal is challenging to achieve	Multi-terminal HVDC is accessible	High losses due to high electronic component count
Can suppress dc faults without a dc breaker	Needs a high short circuit ratio (strong ac system)	Smaller HVdc substations	Requires a dc circuit breaker (depending on the topology)
Well studied technology	Not able to do a "black start"	Able to do a "black start"	
	Requires a synchronous voltage source	Can work with weak AC systems	

2.4   Modular Multilevel Converter

Due to the advantages mentioned over the other topologies. The MMC is selected as the topology for this work in HVdc applications. The MMC topology is shown in Fig. 2.4, with the green dashed line showing one of the arms of the MMC and the blue dashed line showing one of the legs of the MMC. When compared to the HVdc-VSC topologies, mentioned in Section 2.3, the MMC has the following advantages [10]:

- Less expensive and faster fabrication process due to modular design.

- It is easy to scale up to high voltages without adding extra complexity.

- The rise time of dc-side fault currents is limited by the arm inductors.

There have been three proposed topologies for the SM of a MMC. These topologies are: half-bridge sub-module (HBSM), full-bridge sub-module (FBSM) and clamp-double sub-module (CDSM) [12]. The major limitation of the HBSM is that it is unable to block dc-side faults, but this can be overcome by the use of a dc-breaker like the one proposed in 0. The mayor advantages of the HBSM are the lower component count, when compared to the other SM topologies, and higher efficiency. For the reasons mentioned before, the HBSM is selected as the SM topology for the MMC. The HBSM has four possible current paths, as shown in Fig. 2.5.
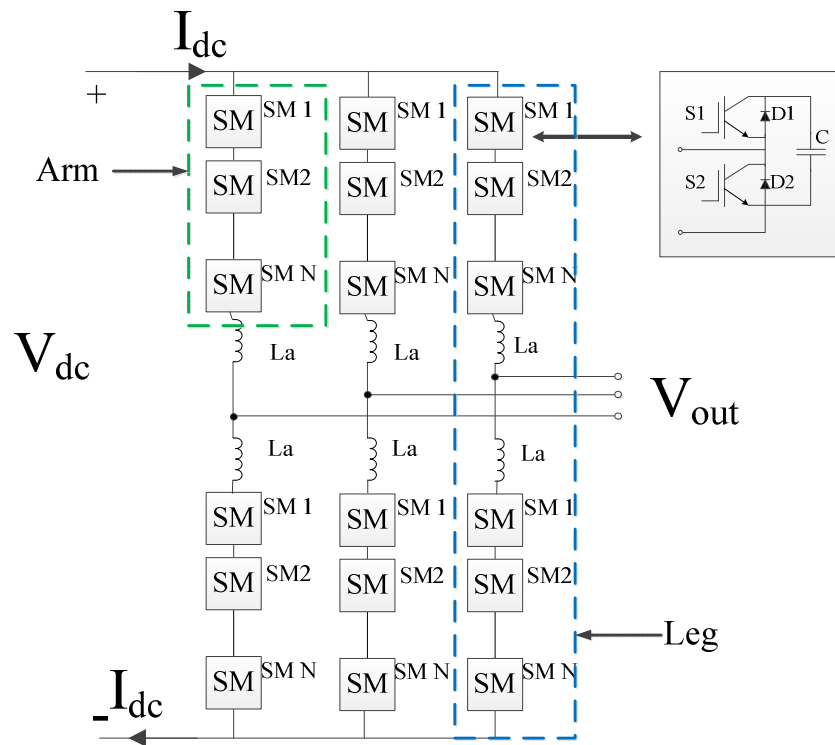
Fig. 2.4. Modular multilevel converter [12]
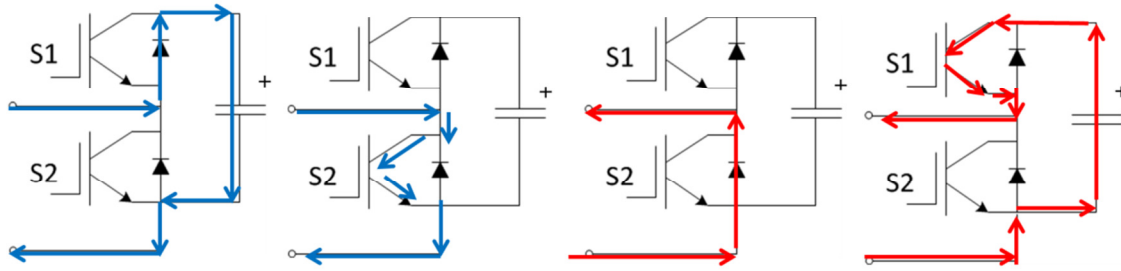
Fig. 2.5. SM Current Paths

The blue lines indicate current flowing into the SM and the red lines indicate current flowing out of the SM. Currents flowing into the SM charge the capacitor and currents flowing out discharge the capacitor.

2.4.1. Operation principles

The MMC operates by inserting or bypassing the SM capacitor to form, in staircase shape, the output voltage waveform [14]. The capacitor is inserted when S1 is on, and bypassed when S2 is turned on. When both switches in the SM (i.e., S1 and S2) are off, the current flows through the freewheeling diodes. The operation of the MMC is illustrated in Fig. 2.6, using dc sources instead of capacitors and a selector. The selector inserts or bypasses dc sources according to the control algorithm of the MMC. The inserted dc sources produce a voltage output with a staircase form, as shown in Fig. 2.7. The six levels voltage waveform in Fig. 2.7 is produced with five SMs per arm of the MMC.
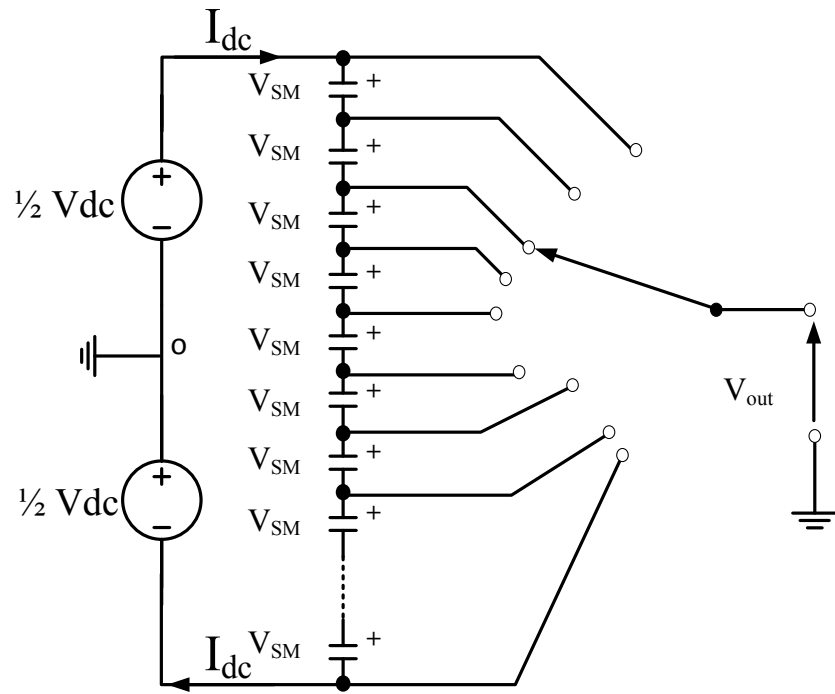
Fig. 2.6. MMC Representation [2]
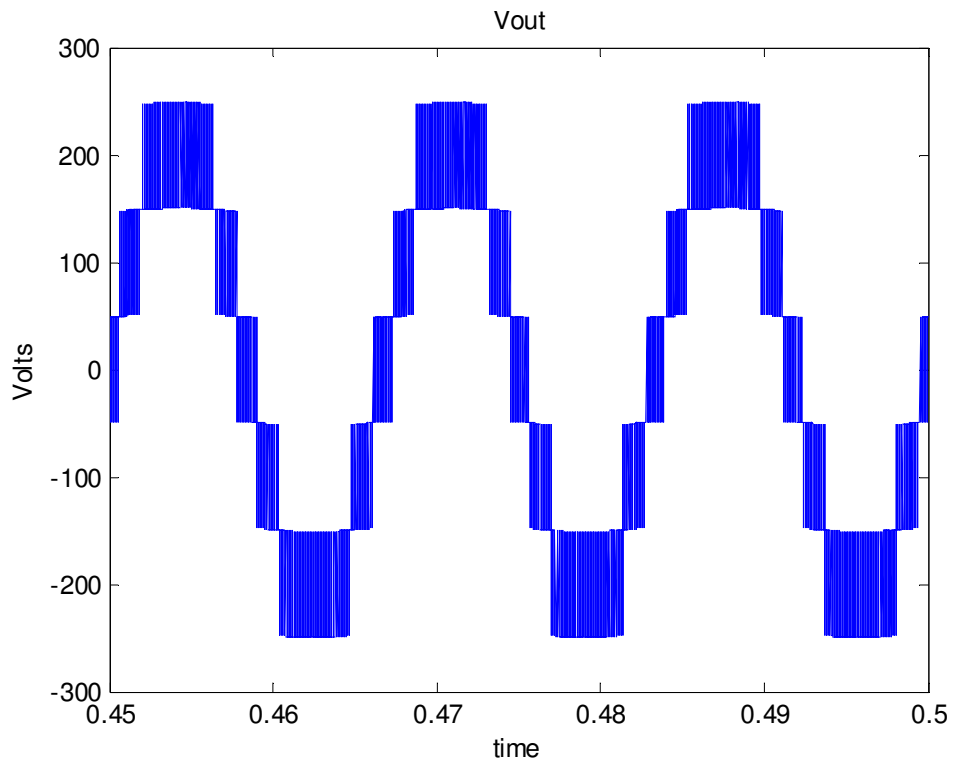
Fig. 2.7. Output Voltage of the MMC

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2.4.2. Passive components of the MMC

This section explains the process of selecting the values for the passive components, namely, the SM capacitor and the arm inductor, whose main functions are energy storage and limiting the circulating current, respectively. The selection of the SM capacitance and inductance values for the MMC has been discussed in [15]-[17], and this section is an explanation of what is presented in the literature.

Assuming that the MMC has an infinite amount of SM and neglecting inductor L_a, the arms of the MMC can be replaced by ideal ac voltage sources as shown in Fig. 2.8, and the dc link can be considered as an ideal dc source. By applying Kirchhoff's current law to Fig. 2.8, the arm current for one phase can be defined as [17]:

$$i_{a1}(t) = \frac{1}{3}I_{dc} + \frac{1}{2}i_a(t) = \frac{1}{3}I_{dc} + \frac{1}{2}\hat{I}_a\sin(\omega_0 t + \varphi) \tag{2.1}$$

where ω_0 is the fundamental frequency of the system in radians per second, φ is the phase shift between the voltage and the current, and $\hat{I}_a$ is the peak phase current.
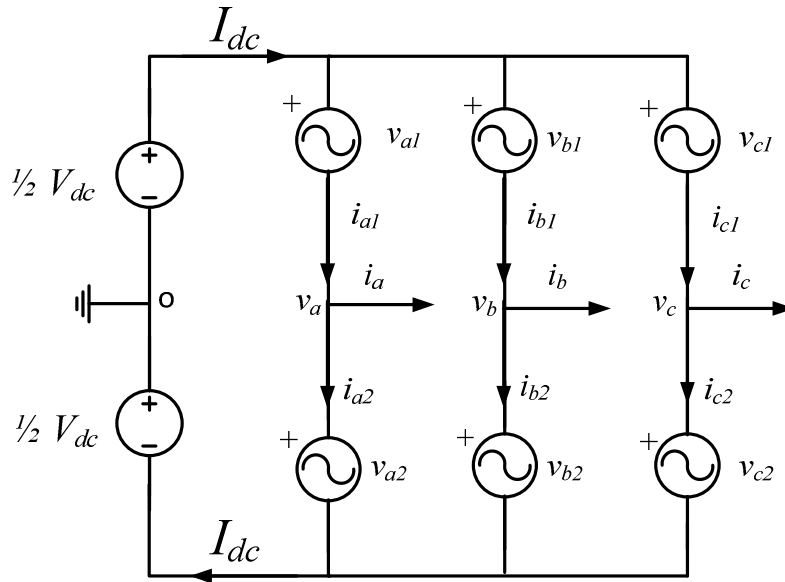
Fig. 2.8. Ideal model of MMC

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By applying Kirchhoff's voltage law to Fig. 2.8, the arm voltage source can be defined as:

$$v_{a1}(t) = \frac{1}{2}V_{dc} - v_a(t) = \frac{1}{2}V_{dc} - \hat{V}_a \sin(\omega_0 t) \tag{2.2}$$

For simplicity, (2.3) and (2.4) the relation between ac and dc variables as are defined as [16]:

$$m = \frac{3}{2}\frac{\hat{I}_a}{I_{dc}} \tag{2.3}$$

$$k = 2\frac{\hat{V}_a}{V_{dc}} \tag{2.4}$$

Introducing (2.3) and (2.4) into (2.1) and (2.2), respectively, gives:

$$i_{a1}(t) = \frac{1}{3}I_{dc}[1 + m\sin(\omega_0 t + \varphi)] \tag{2.5}$$

$$v_{a1}(t) = \frac{1}{2}V_{dc}[1 - k\sin(\omega_0 t)] \tag{2.6}$$

In order to calculate the power in the arm of the MMC, (2.5) and (2.6) are multiplied, yielding:

$$P_{a1}(t) = \frac{P_{dc}}{6}[1 + m\sin(\omega_0 t + \varphi)][1 - k\sin(\omega_0 t)] \tag{2.7}$$

where P_{dc} is defined by (2.8)

$$P_{dc} = V_{dc}I_{dc} \tag{2.8}$$

Integrating (2.7) over half a period yields the total energy change ΔW in the arm of the MMC as follows:

$$\Delta W = \frac{2\,P_{dc}}{3\,k\omega_0\cos\varphi}\left[1 - \left(\frac{k\cdot\cos\varphi}{2}\right)^2\right]^{3/2} \tag{2.9}$$

In order to obtain the energy change of the MMC SM, (2.9) is divided by the number of SMs per arm (N), yielding:

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$$\Delta W_{SM} = \frac{2 \, P_{dc}}{3 \, k\omega_0 N \cos \varphi} \left[1 - \left(\frac{k \cdot \cos \varphi}{2} \right)^2 \right]^{3/2} \tag{2.10}$$

The energy stored in a capacitor is defined as:

$$W = \frac{1}{2} C V^2 \tag{2.11}$$

By combining (2.10) and (2.11), the SM capacitance can be calculated as:

$$C_{SM} = \frac{\Delta W_{SM}}{2\varepsilon V_{SM}^2} \tag{2.12}$$

where ε is the capacitor voltage ripple factor in percentage and V_{SM} is the SM voltage. The capacitors of the SM are charging and discharging during the normal operation of the MMC. This will create a voltage difference across the arm inductances that can be defined by [18]:

$$v_{dif} = V_{dc} - (v_{a1} + v_{a2}) = 2R_a i_{z\_a} + 2L_a \frac{d}{dt} i_{z\_a} \tag{2.13}$$

$$i_{za} = \frac{i_{a1} + i_{a2}}{2} \tag{2.14}$$

where i_{z_a} represents the circulating current between phases and R_a the arm resistance of the MMC. Neglecting the arm resistance, the voltage difference (2.13) can be approximated by:

$$v_{dif} = 2L_a \frac{d}{dt} i_{z\_a} \tag{2.15}$$

Then (2.15) can be used to determine the value of the arm inductance. If the inductance arm inductance is too low, the circulating current can become difficult to control; if selected too great v_{dif} becomes too large and makes the voltages of the leg difficult to balance [15]. Using (2.14) and simulations, to fine tune the results, it was found that a value of 2% was a good compromise between the two tradeoffs.

2.4.3. *MMC modulation strategies*

Different PWM strategies can be implemented to modulate the MMC. Space vector modulation has been applied to three-level converters [19]. As the number of levels increases, the complexity of a space vector algorithm increases as well. For a high number of levels, the implementation of space vector modulation is very complex and requires high computational power. Another option is sinusoidal PWM (SPWM). For a multilevel SPWM, multiple triangular carriers are required. The number of triangular carriers is related to the number of levels of the converter. In the MMC, the number of carriers is equal to the number of SM per arm. The carriers can be arranged in a level shifted disposition (LS-SPWM) or in a phase shifted disposition (PS-SPWM). The LS-SPWM can be divided into three categories which are [20]:

- In phase disposition (IPD)

- Phase opposite disposition (POD)

- Alternative phase opposite disposition (APOD)

In a IPD LS-SPWM arrangement for a five-level control the carriers are spread in different levels between -1 and 1, as illustrated in Fig. 2.9. For the IPD, all the carriers are in phase, for the POD, the carriers are shifted 180° in their respective level, and for the APOD, the carriers above zero are in phase and 180° phase shift when compared to the carriers below zero. According to [15], PS-SPWM has a better performance in terms of harmonic distortion for MMC applications.
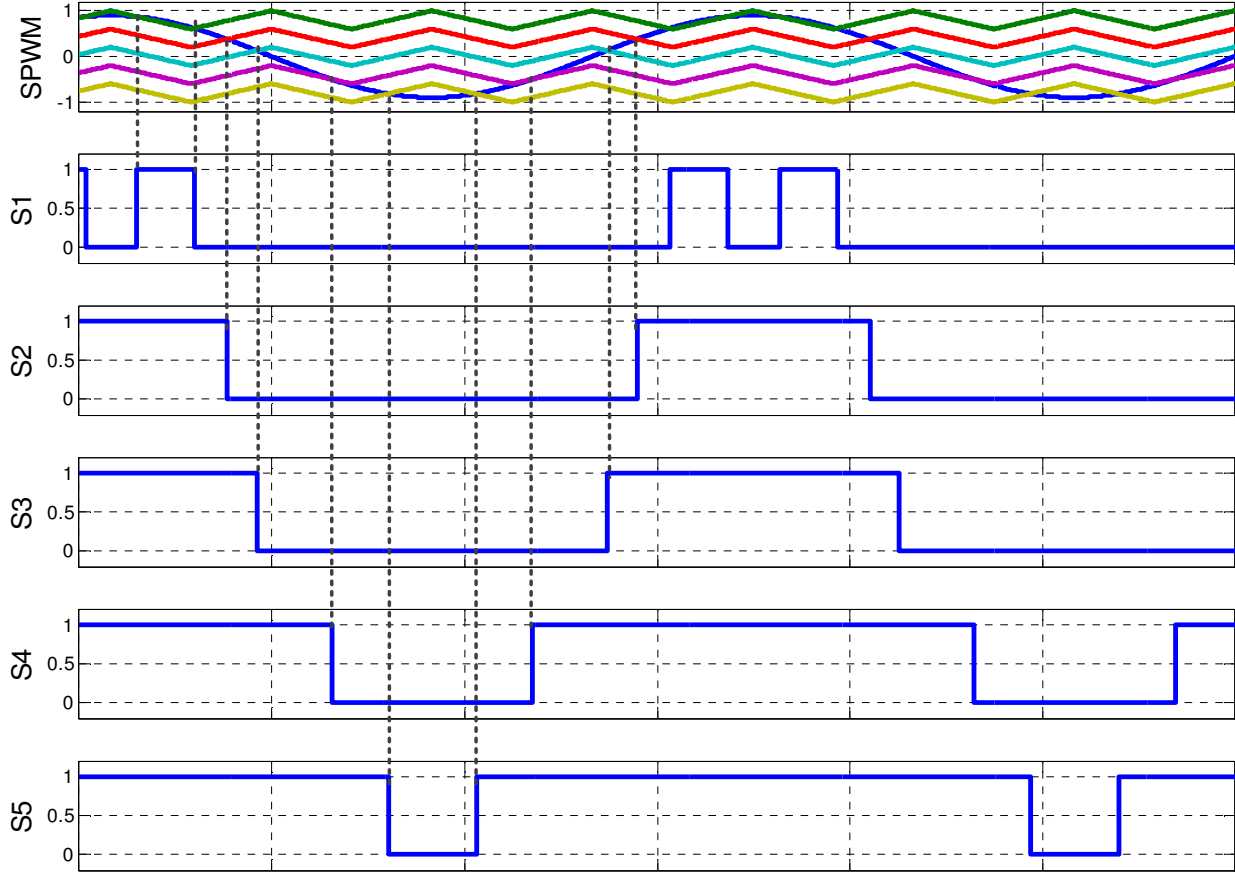
Fig. 2.9. Level Shifted PWM

Therefore, the PS-PWM is selected to be used for the simulations of this thesis. The operation of PS-SPWM for a five-level control, with each triangular carrier controlling one of the switches, is presented in Fig. 2.10. The phase shift between the carriers is determined by:

$$\Phi = \frac{360}{N_c} \tag{2.15}$$

where N_c is the number of carriers. Equation (2.15) in the time domain becomes:

$$T_d = \frac{1}{(N_c f_c)} \tag{2.16}$$

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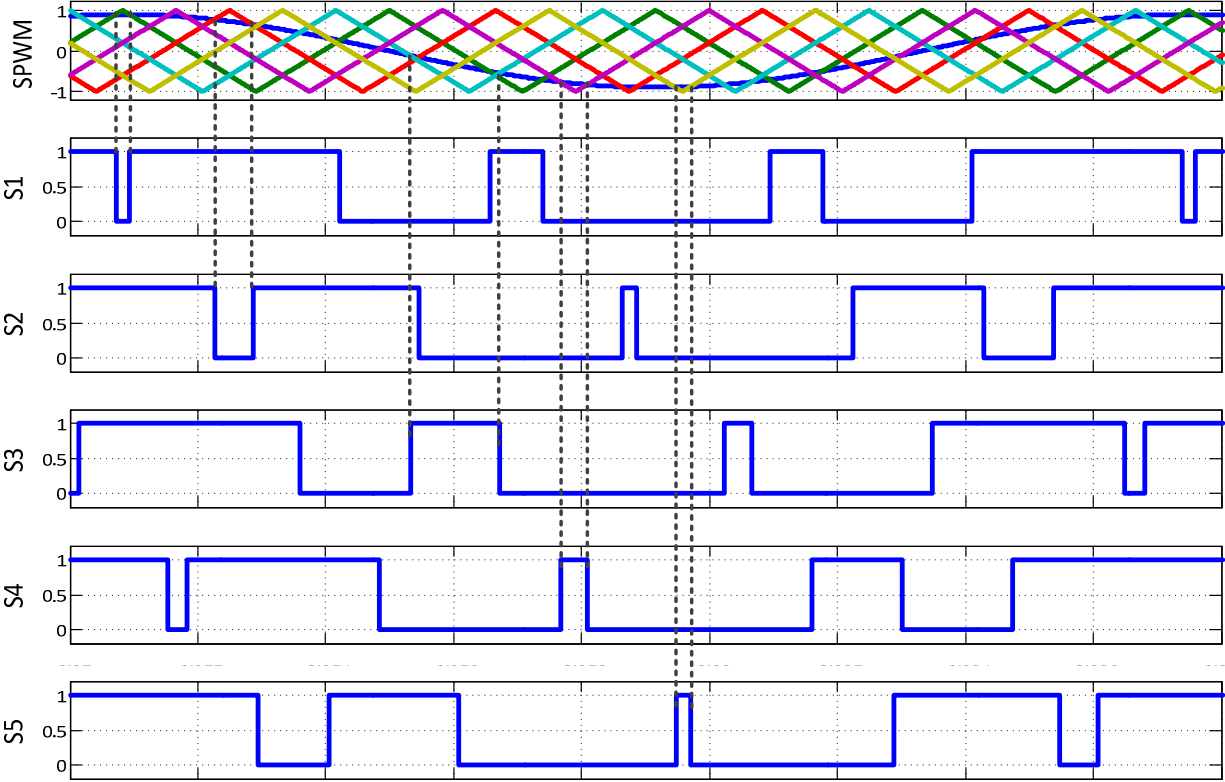
Fig. 2.10. Phase Shifted PWM

where f_c is the triangular carrier frequency. Since the switches of the SM are complementary to each other, only one carrier is needed to control both switches. The SM on the top and bottom arm of a leg of the MMC operates in complementary manner as well [21].

The complementary operation of the SM on a leg means that the maximum amount of SM that can be on at any given time is N. The complimentary operation can be represented by:

$$N = N_{on} = n_{up} + n_{low} \tag{2.17}$$

where N_{on} represents the number of SM that are inserted at any time in the MMC leg, n_{up} represents the number of SM that are inserted in the upper arm of the MMC, and n_{low} is the number of the SM that are inserted in the lower arm of the MMC.

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Using the modulation scheme and concepts presented in this chapter, it is possible to simulate the operation of the MMC using an adequate simulation software package such as Matlab/Simulink™ or PSCAD®, the former is used for this thesis.

2.5   Conclusions

HVdc transmission has more advantages over HVac transmission that make it more suitable when it comes to transmitting power over long distances or underwater cables. Once HVdc has been selected, a study of the right HVdc technology for the HVdc terminal must be performed. Each HVdc technology (HVdc-CSC or HVdc-VSC) has its advantages and disadvantages depending on the application, with both technologies coexisting.

Among the different HVdc-VSC topologies, the MMC has several advantages over the others making it an attractive solution for HVdc-VSC projects. Within the SM topologies for the MMC, the half-bridge it is the most efficient due to lower component count. The operation of the MMC produces a staircase shape output voltage that with a high number of levels reduces the THD of the output voltage is to the point of eliminating the necessity for ac-side filters.

Chapter Three will analyze the SM capacitor voltage controllers and the controllers used for HVdc transmission using the MMC fundamental operating principles provided in this chapter.

References

[1]   J. Arrillaga, Y.H. Liu, and N.R. Watson *Flexible Power Transmission, The HVDC Options*, West Sussex: John Wiley & Sons 2007.

[2]   R. Adapa, "High-Wire Act: HVdc Technology: The State of the Art," *Power and Energy Magazine, IEEE*, vol. 10, no. 6, pp. 18-29, Nov. 2012.

[3] K. Meah, S. Ula, "Comparative Evaluation of HVDC and HVAC Transmission Systems," *Power Engineering Society General Meeting, 2007. IEEE*, pp. 1-5, 2007.

[4] R. Rudervall, J. Charpentier, and R. Sharma, "High voltage direct current (HVDC) transmission systems technology review paper," *Energy week*, pp. 7-8, 2000.

[5] ABB. *Applications for HVDC Light®,* [Online]. Available: http://www.abb.us/industries/us/9AAF400197.aspx [Accessed: Jan. 15, 2013]

[6] M.P. Bahrman, B.K. Johnson, "The ABCs of HVDC transmission technologies," *Power and Energy Magazine, IEEE* , vol. 5, no. 2, pp. 32-44, 2007.

[7] O. Peake, "The History of High Voltage Direct Current Transmission," *presented at the Australasian Engineering Heritage Conference*, 2009.

[8] A. M. Abbas, P.W. Lehn, "PWM based VSC-HVDC systems — A review," *Power & Energy Society General Meeting, PES '09. IEEE*, pp. 1-9, 2009.

[9] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, Bin Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[10] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, M.A.M. Prats, , "The age of multilevel converters arrives," *Industrial Electronics Magazine, IEEE* , vol. 2, no. 2, pp. 28-39, June 2008.

[11] Alstom "Alstom Grid will provide Tres Amigas LLC in the USA with first-of-its-kind Smart Grid "SuperStation"" [Online] Available: http://www.alstom.com/press-centre/2011/4/Alstom-Grid-will-provide-Tres-Amigas-LLC-in-the-USA-with-first-of-its-kind-Smart-Grid-SuperStation/ [Accessed: Jun. 2, 2013]

[12] R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," *Proceedings of Power Electronics Conference (IPEC), 2010 International*, pp. 502-507, 2010.

[13]   ABB. *ABB solves 100-year-old electrical puzzle – new technology to enable future DC grid* [Online]. Available:
http://www.abb.com/cawp/seitp202/65df338284e41b3dc1257aae0045b7de.aspx
[Accessed: Nov. 30, 2012]

[14]   E. Abildgaard, "Exploring the Properties of a Modular Multilevel Converter Based HVDC Link. With Focus on Voltage Capability, Power System Relations, and Control System," M.S. Thesis, Dept. Electric Power Eng., Norwegian Univ. of Sci. and Tech., Norway. 2012.

[15]   M. Vasiladiotis, "Analysis, Implementation and Experimental Evaluation of Control Systems for a Modular Multilevel Converter," M.S. Thesis, Dept. Elect. Eng., Roy. Tech. Inst., Stockholm, Sweden 2009.

[16]   Y. Zhang, G. P. Adam, T. C. Lim, S. J. Finney, and B. W. Williams, "Analysis and experiment validation of a three-level modular multilevel converters," *Proceedings of IEEE 8th International Conference on Power Electronics and ECCE Asia* (ICPE & ECCE), pp. 983, 990. 2011.

[17]   Y. Zhang, G. P. Adam, T. C Lim, S. J. Finney, and B. W. Williams, "Mathematical Analysis and Experimet Validation of Modular Multilevel Converters," *Journal of Power Electronics*, vol. 12, no. 1, pp. 33, 39, 2012.

[18]   A. Antonopoulos, L. Angquist, H.P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter," *Proceedings of 13th European Conference on Power Electronics and Applications*, EPE '09. pp. 1-10 Sept. 2009

[19]   R.K. Behera, S.P. Das, "Space vector modulation for a three-level NPC ac-dc converter system: An experimental investigation," *Proceedings of International Conference on Power, Control and Embedded Systems (ICPCES),* pp. 1-5, Nov. - Dec. 1 2010.

[20]   C. Sandu, N. Carnu, and V. C. Costea, "Medium Voltage Modular Multi-Level Inverter," M.S. Thesis, Dept. of Energy Tech., Aalborg Univ., Aalborg, Denmark, 2008.

[21]   E. Solas, G. Abad, J. A. Barrena, A. Cárcar, and S. Aurtenetxea, "Modulation of Modular Multilevel Converter for HVDC application," *Proceedings of Power Electronics and Motion Control Conference (EPE/PEMC), 14th International* , pp. T2-84 - T2-89, 2010.

[22]   T. Modeer, H.P. Nee, S. Norrga, "Loss comparison of different sub-module implementations for modular multilevel converters in HVDC applications," *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011),* pp.1-7, 2011.

CHAPTER THREE

CONTROLLERS FOR A TWO-TERMINAL MMC-BASED HVDC TRANSMISSION SYSTEM

Abstract

The control of two terminal MMC-based HVdc system encompasses several controllers regulating the SM capacitor voltage, minimizing the circulating currents and transferring the desired active and reactive powers. This chapter analyzes the active and reactive power outer controllers, the dc-voltage outer controller, the current controller, and the SM capacitor voltage controllers and circulating current controller. The gains for the controllers are selected using simplified models, and Bode plots and step responses are used to evaluate the current and dc voltage controllers.

3.1   Introduction

Chapter Two provided the background to understand the MMC topology and the PS-SPWM algorithm controlling the switching devices. This chapter focuses on the controllers depicted in Fig. 3.1 for a two-terminal MMC-based HVdc transmission system. It is customary to control a two-terminal HVdc link by having the sending-end Terminal 1 controlling the dc-link voltage and reactive power, and the receiving-end Terminal 2 controlling the active and reactive powers injected into the receiving grid [1]. The associated controllers are indicated in Fig. 3.1 as "dc Voltage controller", "Power controller" and "Current controller" for Terminal 1 and "Power controller" and "Current controller" for Terminal 2. In addition, two other control functions are
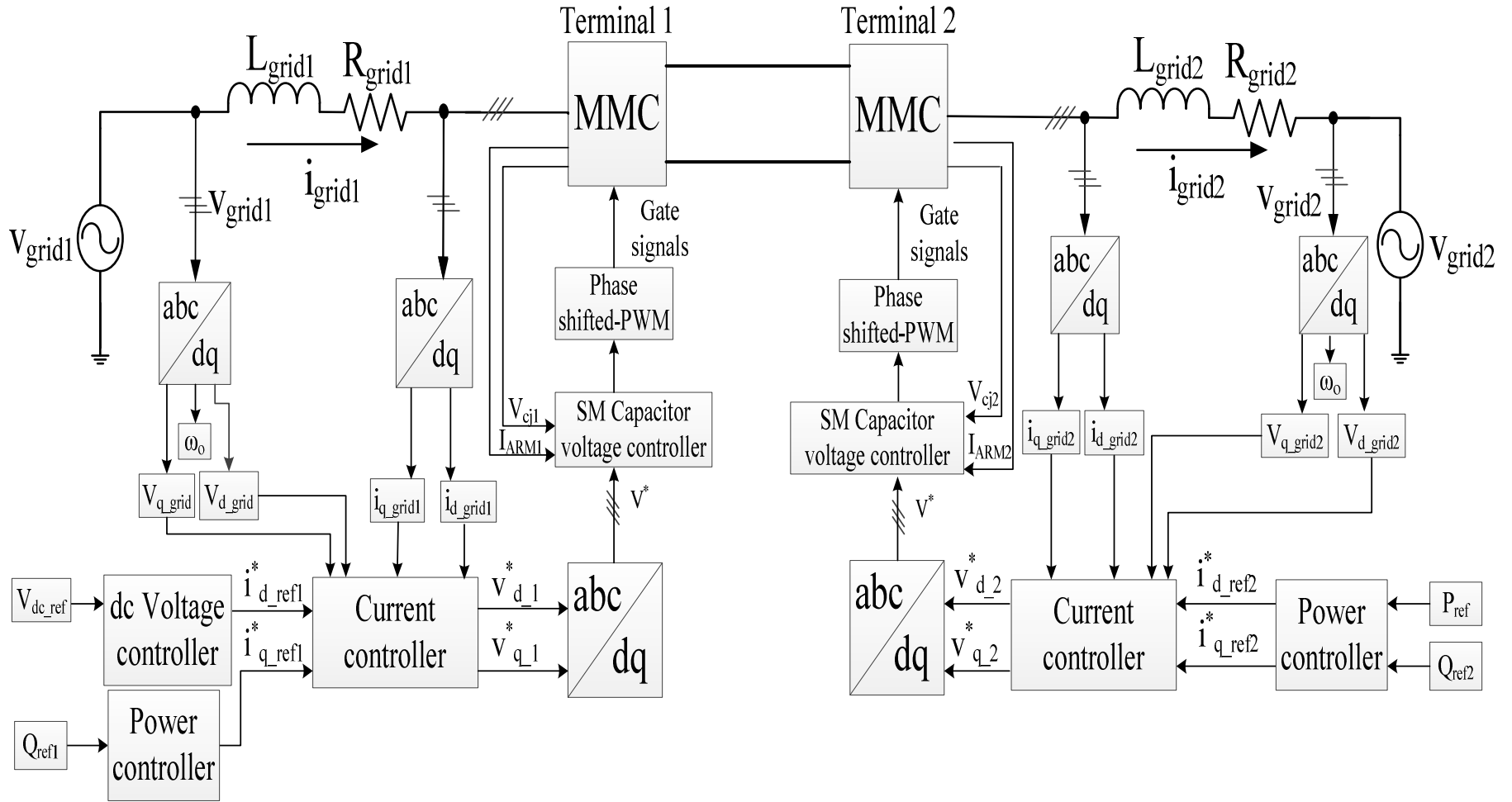
Fig. 3.1. Typical control scheme of a two terminal HVdc-link

important; namely, maintaining the SM capacitor voltages at their reference values, and controlling the circulating current to avoid system instabilities [2]. These two functions are accomplished by the "SM Capacitor voltage controller" block on each terminal. The "dc Voltage controller" and "Power controller" form the so-called outer controllers. The "Current controller" is the inner controller.

The "abc/dq" block makes use of the Park's Transformation [3] to transform from the abc stationary reference frame to a synchronously-rotating frame and its detailed Matlab/Simulink™ representation is given in Appendix A.1. The controllers are analyzed and their respective gains selected using the system whose parameters are given in Table 3.1 [4].

3.2   Outer Controllers

The outer controllers could be selected as: active power control, reactive power control, dc voltage control or ac voltage control. For this application, the following is selected [5]:

- Terminal 1 (rectifier): dc voltage control and reactive power control
- Terminal 2 (inverter): active power control and reactive power control

Selecting these controllers allows for independent control of reactive power at each terminal. Terminal 1 regulates the dc-link voltage and Terminal 2 controls the power flow.

Table 3.1. HVdc system parameters [4]

Parameter	V_{dc}	V_{grid1}, V_{grid2}	f_o	L_{grid1}, L_{grid2}	R_{grid1}, R_{grid2}	f_{sw}
Value	±200 kV	230 kV	60 Hz	28 mH	0.75 Ω	2 kHz

3.2.1 Active and reactive power controllers

The active and reactive power controllers used in this thesis are based on the ones proposed in [6]. For a three-phase grid, the real instantaneous power is given by:

$$P(t) = Re\{\overrightarrow{v_a}(t)\}Re\{\overrightarrow{i_a}(t)\} + Re\{\overrightarrow{v_b}(t)\}Re\{\overrightarrow{i_b}(t)\} + Re\{\overrightarrow{v_c}(t)\}Re\{\overrightarrow{i_c}(t)\} \tag{3.1}$$

by means of the identity $Re\{a\}Re\{b\} = \frac{Re\{ab\}+Re\{ab^*\}}{2}$ and space phasor notation for v_{abc}, and i_{abc}, (3.1) is rewritten as:

$$P(t) = \frac{Re\{\overrightarrow{v_a}(t)\ \vec{i}_a(t)\} + Re\{\overrightarrow{v_a}(t)\ \vec{i}_a(t)^*\}}{2} + \frac{Re\left\{\overrightarrow{v_b}(t)\ \vec{i}_b(t)e^{-j\frac{4\pi}{3}}\right\} + Re\{\overrightarrow{v_b}(t)\ \vec{i}_b(t)^*\}}{2}$$

$$+ \frac{Re\left\{\overrightarrow{v_c}(t)\ \vec{i}_c(t)e^{-j\frac{4\pi}{3}}\right\} + Re\{\overrightarrow{v_c}(t)\ \vec{i}_c(t)^*\}}{2} \tag{3.2}$$

For a three-phase balanced system $e^{j0} + e^{-j\frac{4\pi}{3}} + e^{-j\frac{8\pi}{3}} \equiv 0$, then (3.2) becomes:

$$P(t) = Re\left\{\frac{3}{2}\overrightarrow{v_a}(t)\ \overrightarrow{i_a}(t)^*\right\} \tag{3.3}$$

The same procedure can be applied to obtain the reactive power equation. The difference is that the imaginary part of $\{\vec{v}(t)\ \vec{i}(t)\}$ is used when deriving the reactive power equation:

$$Q(t) = Im\left\{\frac{3}{2}\overrightarrow{v_a}(t)\ \overrightarrow{i_a}(t)^*\right\} \tag{3.4}$$

Equations (3.3) and (3.4) are written in the d-q synchronously-rotating frame as follows:

$$P(t) = \frac{3}{2}\left(V_{d\_grid}(t)i_{d\_grid}(t) + V_{q\_grid}(t)i_{q\_grid}(t)\right) \tag{3.5}$$

$$Q(t) = \frac{3}{2}\left(-V_{d\_grid}(t)i_{q\_grid}(t) + V_{q\_grid}(t)i_{d\_grid}(t)\right) \tag{3.6}$$

where V_{d_grid}, V_{q_grid}, i_{d_grid} and i_{d_grid} are the voltages and the currents in the d-q axes, respectively. For steady-state conditions, with the d axis on Phase A, $V_{q\_grid} = 0$. Therefore, (3.5) and (3.6) under steady-state conditions, are rewritten as:

$$P(t) = \frac{3}{2} V_{d\_grid}(t) i_{d\_grid}(t) \tag{3.7}$$

$$Q(t) = -\frac{3}{2} V_{d\_grid}(t) i_{q\_grid}(t) \tag{3.8}$$

By inspection of (3.7) and (3.8), $P(t)$ and $Q(t)$ can be independently controlled by i_{d_grid} and i_{q_grid}, respectively, since the grid voltage is constant. Considering the fast reference tracking provided by the inner current controller explained in Section 3.3, $i_{d\_grid} \approx i_{d\_ref}$ and $i_{q\_grid} \approx i_{q\_ref}$; therefore, $P(t) \approx P_{ref}(t)$ and $Q(t) \approx Q_{ref}(t)$. Taking this assumption into account and knowing that under steady-state conditions V_{d_grid} is constant, the reference commands for i_{dq} can be written as:

$$i_{d\_ref} = \frac{2}{3V_d} P_{ref}(t) \tag{3.9}$$

$$i_{q\_ref} = -\frac{2}{3V_d} Q_{ref}(t) \tag{3.10}$$

The control block diagrams of (3.9) and (3.10) generating the reference commands for the inner current controllers in Fig. 3.1 are shown in Fig. 3.2. The controllers for i_{d_grid} and i_{q_grid} are the ones explained in Section 3.3.
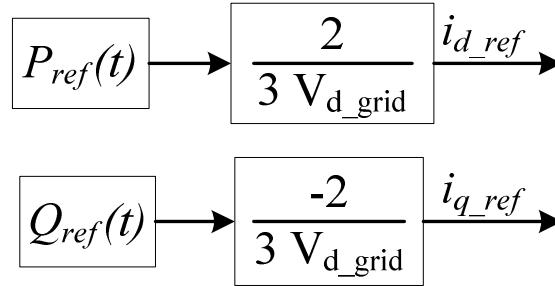
Fig. 3.2. Control block diagrams for the power controllers

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3.2.2 DC voltage controller at Terminal 1

The dc voltage controller for the MMC is based on the dc controller described in [7] that

provides a current reference on the d-axis for inner current controller in order to maintain the

voltage of the dc link constant, as shown in Fig. 3.1. Therefore, the dc-voltage controller forms

the outer loop, and the current controller forms the inner loop.

The controller was tuned first for a two-level rectifier and then implemented in the MMC-

based terminal. For a two-level rectifier, the transfer function that is used to control the dc

voltage across the dc-link capacitor is given by [7], [8]:

$$G_{dc}(s) = \frac{1}{sC_{dc}} \tag{3.11}$$

where C_{dc} is the capacitance of the dc-link capacitor. The capacitance for a two-level rectifier is

calculated taking into the account the tradeoffs between ripple attenuation, provided by a high

capacitance, and system dynamics, given by a lower capacitance [8]. The capacitance was

calculated to be 30 mF by using (3-7) of [8] for a starting point, and then fine tuning its value via

simulations using the model presented in Appendix A.2. A PI controller is implemented to

control the plant in (3.11), as illustrated by Fig. 3.3(a).
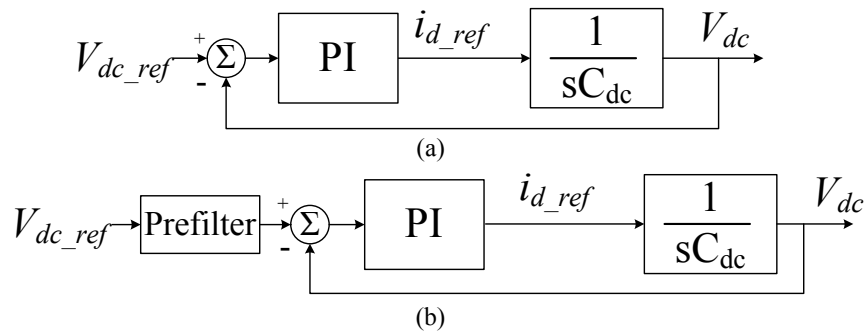
Fig. 3.3. dc voltage controller block diagram with: (a) no prefilter added (b) a prefilter

added

The design objectives for the voltage PI controller were selected as a damping factor of $\xi = 0.707$ and a bandwidth of 219 rad/s (35 Hz). Using the Matlab™ code presented in Appendix A.3 the calculated values for the gains of the PI controller are $k_{p\_dc} = 9.3\ \Omega^{-1}$ and $k_{i\_dc} = 1451\ \Omega\text{s}^{-1}$ and its associated closed-loop Bode plot is shown in Fig. 3.4. The system represented by the solid line of Fig. 3.4 has no prefilter as in Fig. 3.3(a) and the crossover frequency is more than twice the desired design objective. The faster bandwidth can cause instability issues when the output of the dc voltage controller is connected to the inner current controller. Therefore, a prefilter is added to compensate for the dynamics of the system as shown in Fig. 3.3(b) and is calculated by [7]:

$$T_{\text{filter}}(s) = \frac{1}{1 + s\left(\dfrac{k_p}{k_i}\right)}$$

(3.12)

where k_p and k_i are the proportional and integral gains of the controller, respectively. The system performance with the prefilter, is shown by the dashed line in Fig. 3.4. The crossover frequency is as desired once the prefilter is added.

The prefilter improves the overshoot in the step response plot shown in Fig. 3.5. The response of the system in Fig 3.3(a) is plotted in a solid line, which has an overshoot of 20.8%. By adding the prefilter, the overshoot is reduced to 4.32%, as illustrated by the dashed line in Fig. 3.5. The addition of the prefilter increases the settling time from 0.022 s to 0.027 s (23%). This increase should not affect the performance of the controllers.

3.3 Inner Current Control

This section describes the current control equations described in [5], [7]-[10] and the tuning of the controller. For MMC-based terminals, this control technique assumes an infinite number of levels which leads to sinusoidal currents and voltages at the MMC ac output. Hence, the MMC

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Bode Diagram
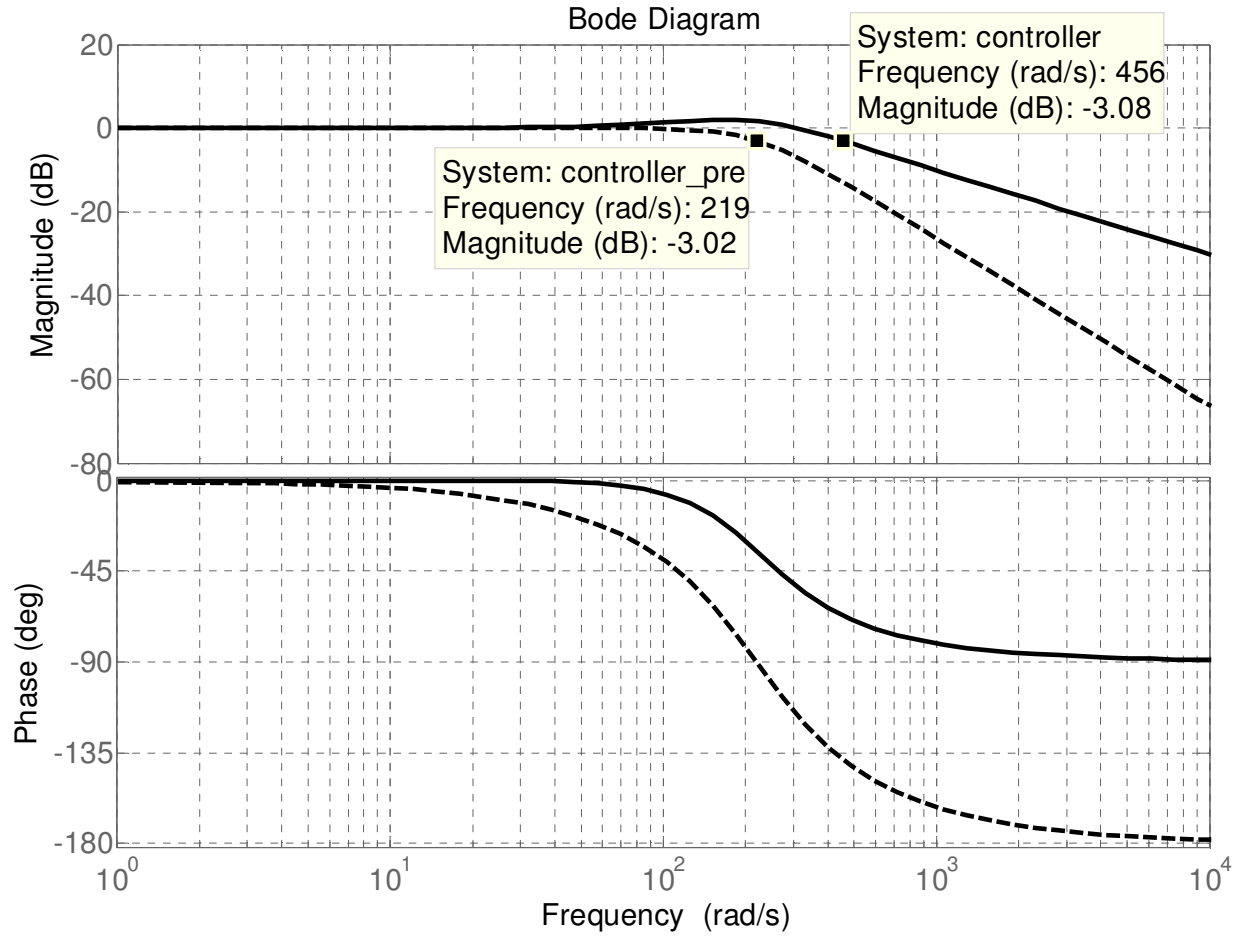
Fig. 3.4. Bode plot of the dc-voltage controller without prefilter (solid) and with prefilter

(dashed)

connection with the grid can be represented as in Fig. 3.6 and using Kirchhoff's voltage law yields:

$$v_{inv} = L_{grid} \frac{di_{grid}}{dt} + R_{grid}i_{grid} + v_{grid} \tag{3.13}$$
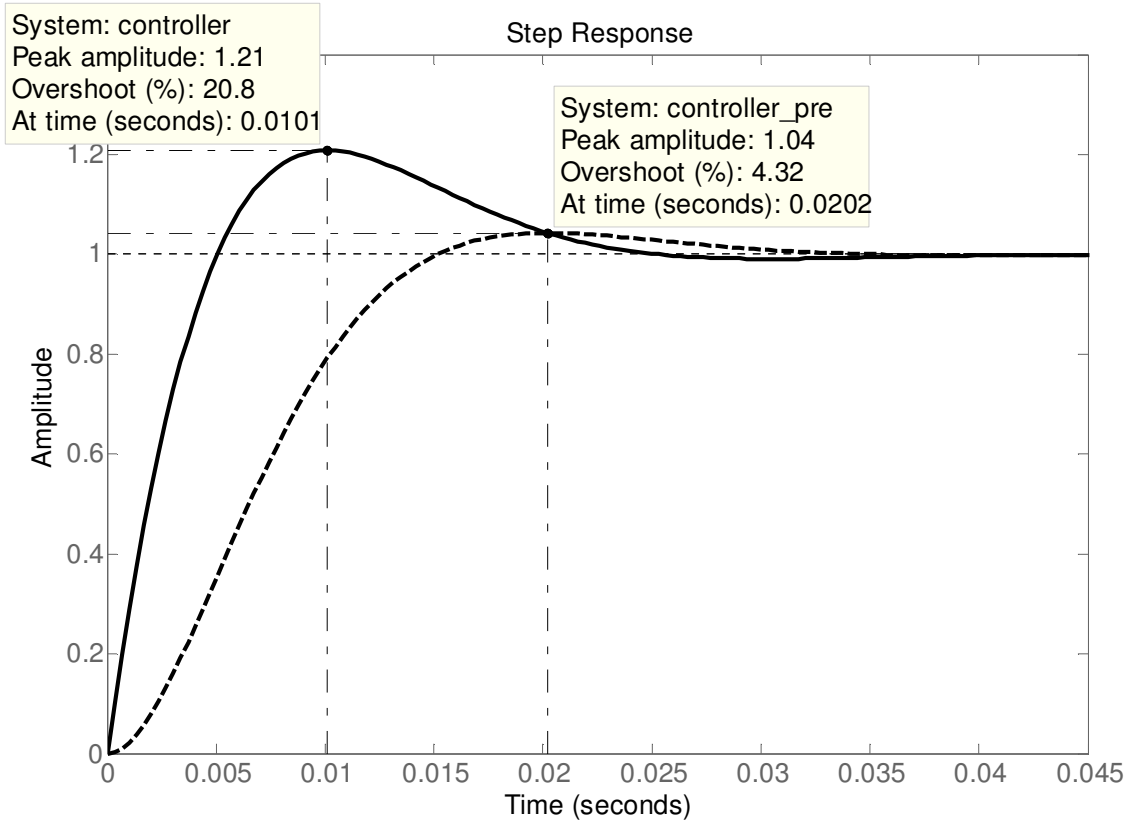
Fig. 3.5. Step response of the dc-voltage controller without prefilter (solid) and with prefilter (dashed)
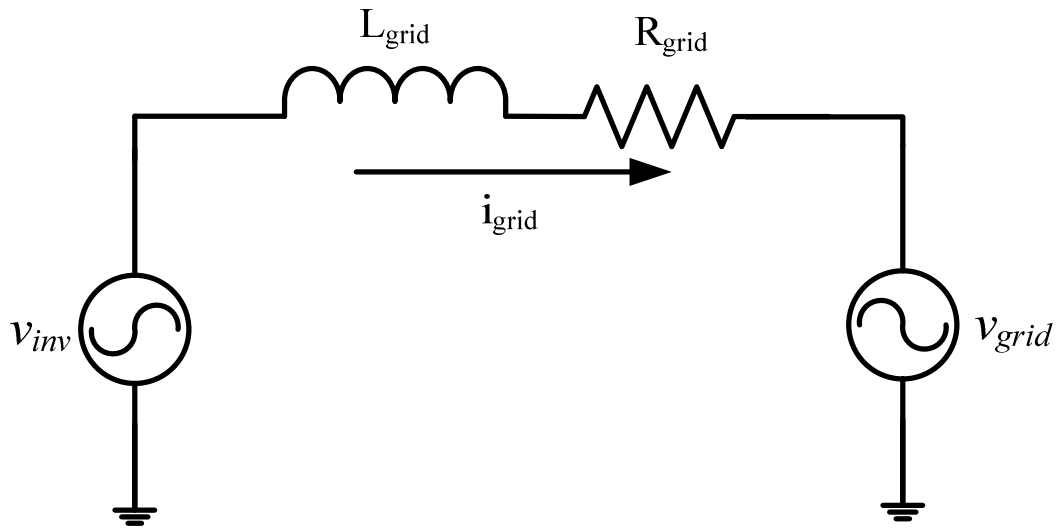
Fig. 3.6. Single-phase schematic of an ideal MMC connected to a grid in inverter mode

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By means of the Park's Transformation [3], (3.13) can be written in a synchronously-rotating reference frame as:

$$L_{grid}\frac{d}{dt}\left(i_{d\_grid}\right) = v_{d\_inv} - v_{d\_grid} - R_{grid}i_{d\_grid} + L_{grid}\omega_o i_{q\_grid} \tag{3.14}$$

$$L_{grid}\frac{d}{dt}\left(i_{q\_grid}\right) = v_{q\_inv} - v_{q\_grid} - R_{grid}i_{q\_grid} - L_{grid}\omega_o i_{d\_grid} \tag{3.15}$$

where ω_o is the angular frequency of the grid, L_{grid} is the grid inductance, v_{d_inv} and v_{q_inv} are the output voltages of the inverter in the d-q axes, and v_{d_grid} and v_{q_grid} are the grid voltages in the d-q axes.

The last terms in (3.14) and (3.15) show the typical cross-coupling term between the two axes; it must be eliminated in order to improve the system stability. This is accomplished by selecting inverter voltages as [7]:

$$v_{d\_inv} = v_d' + v_{d\_grid} - L_{grid}\omega_o i_{q\_grid} \tag{3.16}$$

$$v_{q\_inv} = v_q' + v_{q\_grid} + L_{grid}\omega_o i_{d\_grid} \tag{3.17}$$

where v_d' and v_q' are the outputs of PI controllers.

By inserting (3.16) and (3.17) into (3.14) and (3.15), respectively, and working into the Laplace domain, the following transfer function is obtained for the d-axis:

$$\frac{i_{d\_grid}}{v_d'} = \frac{1}{sL_{grid} + R_{grid}} \tag{3.18}$$

A similar equation may be obtained for the q-axis. Fig. 3.7 (a) shows the block diagram of the inner current controller for the d axis; the q axis can be represented similarly. The PI controller needs to be tuned to meet design requirements in terms of bandwidth and settling time for the system parameters in Table 3.1. The design requirements of the controller are set as follows [5]:

- Damping factor of: $\xi = 0.707$

(a)

(b)
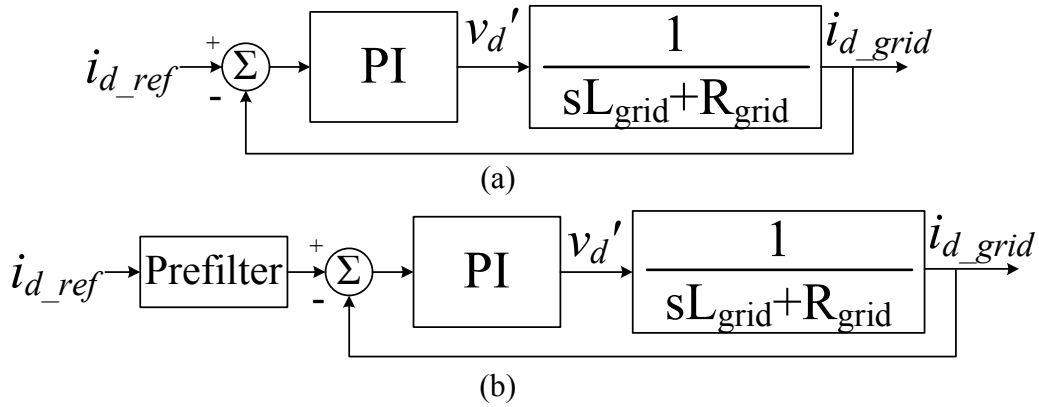
Fig. 3.7. Inner controller block diagram with: (a) no prefilter added (b) a prefilter added

- Bandwidth of: 10 times the dc-voltage controller and smaller than 5 times the angular switching frequency

The selected bandwidth for the controller is 2513 rads/s (400 Hz). This controller must be faster than the controller of Section 3.2 to decouple the dynamics of the state variables of both controllers. If the current controller is at least 10 times faster than the dc-voltage controller of the outer loop, then the current controller can be considered as an infinite bandwidth loop since it would be much faster than the outer loop [7]. Therefore, the current reference into the inner loop would change slowly enough so that the controller can track it without errors. With the given values for the damping and bandwidth and using the Matlab™ code presented in Appendix A.3 the calculated values for the PI controller gains are: $k_{p\_i} = 99 \ \Omega$ and $k_{i\_i} = 1.77 \times 10^5 \ \Omega/\text{s}$.

The closed-loop Bode plot of the system, shown in Fig. 3.8, is obtained using the calculated gains for the system of Fig. 3.7(a). The solid line in Fig. 3.8 corresponds to the system shown in Fig. 3.7(a); the dashed line corresponds to the system of Fig. 3.7(b). The crossover frequency of the system without the prefilter is 5.12 krad/s, wich is more than double the design target. Once

the filter is added, the bandwidth of the system is 2510 rad/s, which is the desired design target. Similar to Section 3.2.2, the prefilter also improves the step response of the system.

In Fig. 3.9, the solid line shows the step response of the system of Fig 3.7(a), and the dashed line shows the response of the system with the prefilter added, see Fig. 3.7(b). The overshoot is reduced from 20.5% without a prefilter to 4.32% with the prefilter. The tradeoff of the prefilter is that the settling time increases by 21% with the prefilter. The system still responds fast enough to react for load changes. In Fig. 3.8 and Fig. 3.9 the system is stable in a closed loop using
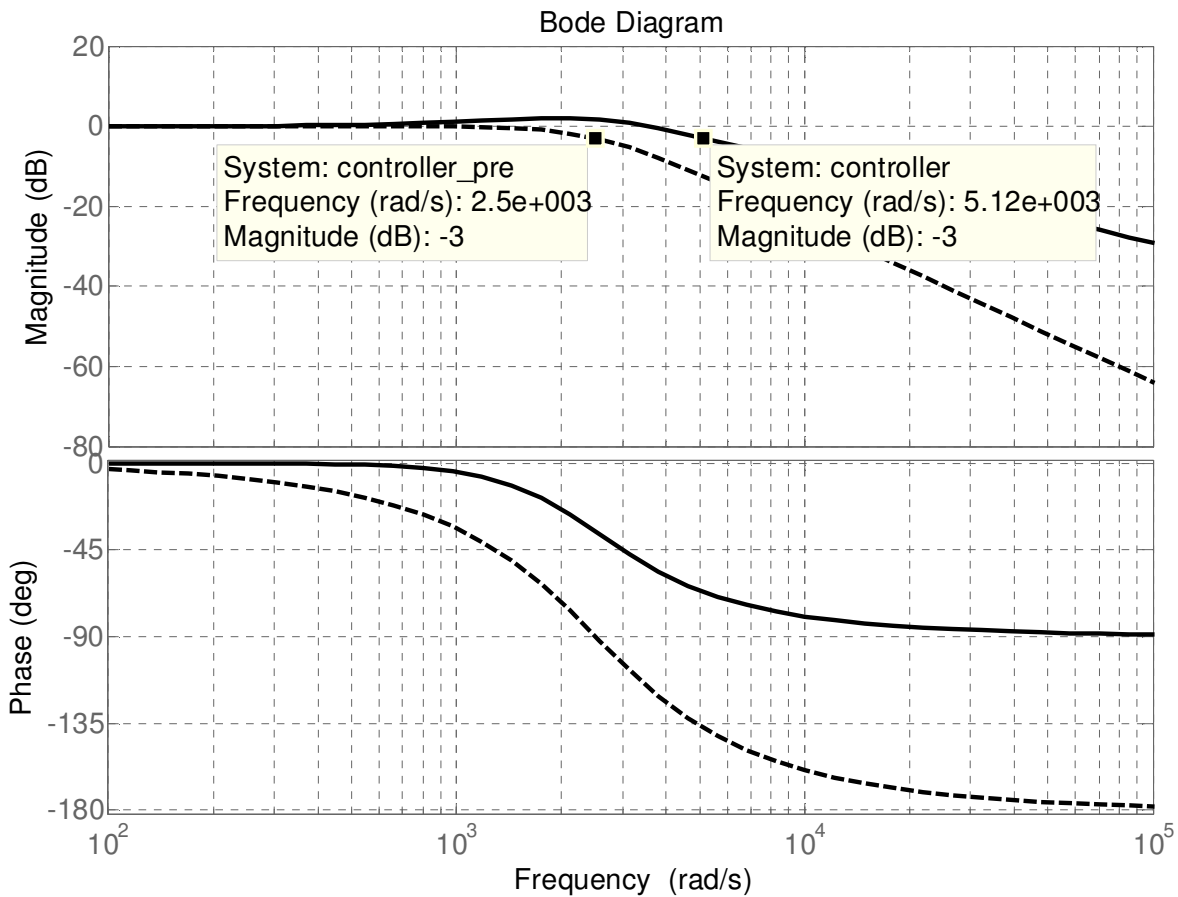
Fig. 3.8. Bode plot of the inner current controller without prefilter (solid) and with prefilter (dashed)
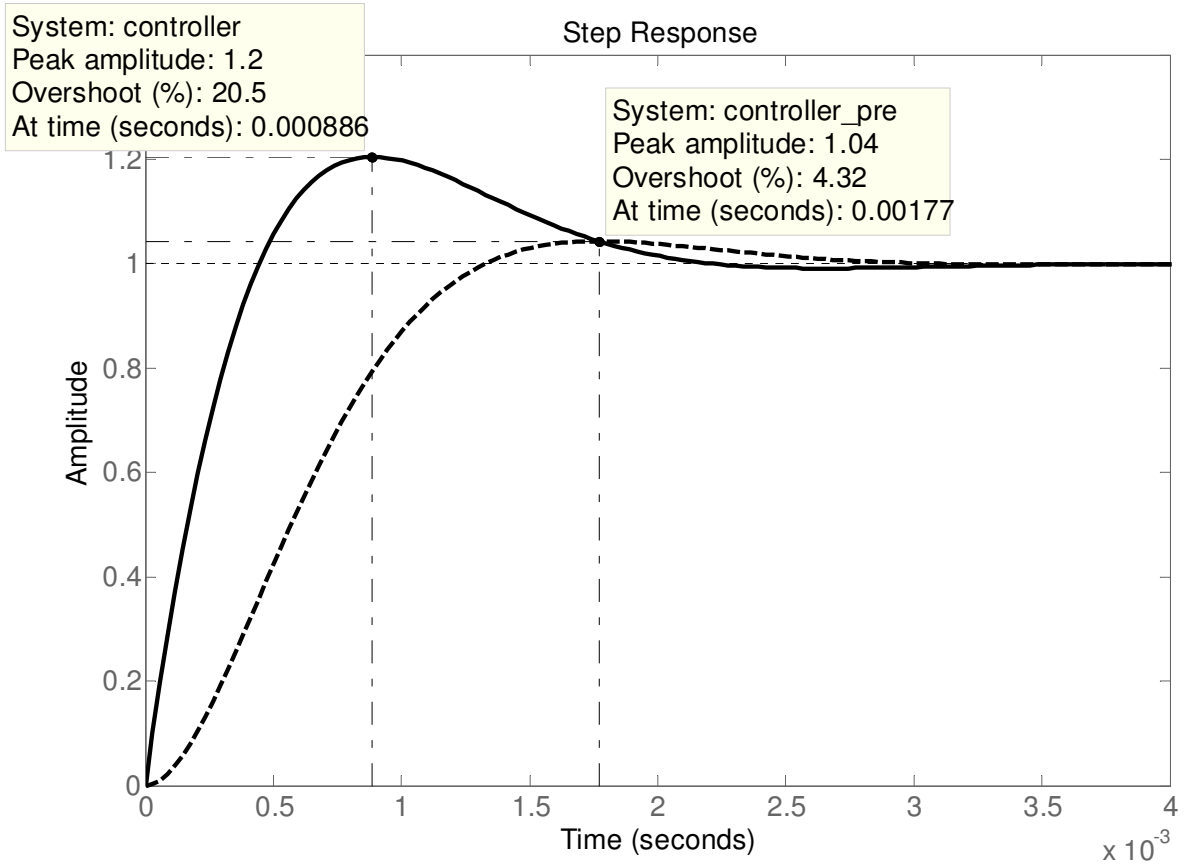
Fig. 3.9. Step response of the inner current controller without prefilter (solid) and with prefilter (dashed)

gains calculated for the controller. Therefore, these are the gains that will be used for the inner current controllers of the HVdc system illustrated in Fig. 3.10. The reference currents come from the controllers explained in Section 3.2. The two variables v_{d_inv} and v_{d_inv} are transformed into the abc frame by means of the inverse Park's Transformation to generate v_u^* for the PS-PWM algortihm controlling the switching devices.
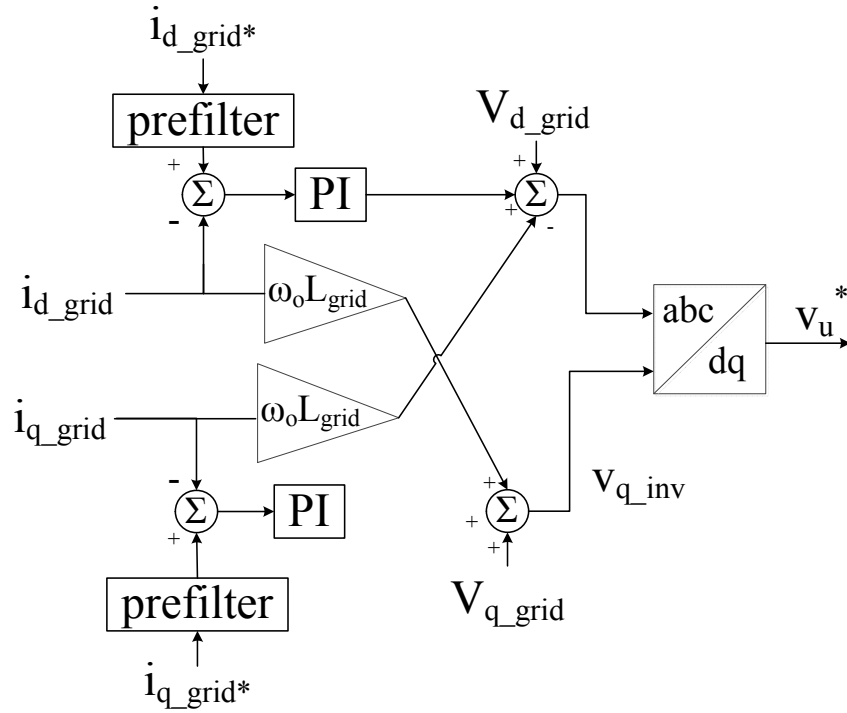
Fig. 3.10. Inner current controller for the MMC

3.4 SM Capacitor Voltage and Circulating Current Control

As previously mentioned control of the SM capacitor voltage control and the circulating current are important to keep the system stable. This section is dedicated to analyze the controllers that make this possible. There are several techniques described in the MMC literature [2], [9]-[12] for controlling the SM capacitor voltages. After an evaluation, the technique presented in [2] and [10] is selected for this work, because of its capabilities of controlling the circulating current.

The main objectives of this section are to analyze the chosen technique and to explain the purpose of each of the three controllers which are:

- Capacitor average voltage control through circulating current control
- Balancing control of the instantaneous capacitor voltages

- Arm average voltage balancing control

The MMC Matlab/Simulink™ model used for selecting the gains of these three controllers is provided in Appendix A.4, as well as the blocks used for each controller implementation.

3.4.1 Capacitor average voltage control

It has been demonstrated that during normal operation, the charging and discharging of the capacitors in the MMC produces a voltage difference between the dc link and the phase legs [12]. This voltage difference is associated with a phase circulating current i_{zu} that is illustrated in Fig. 3.11, which shows a single leg of an MMC. The phase circulating current is given by [2]:

$$i_{zu}(t) = \frac{i_{p\,u}(t) + i_{n\,u}(t)}{2} \tag{3.19}$$

where $i_{p\,u}(t)$ and $i_{n\,u}(t)$ are the top and the bottom currents of phase "u", which is the phase that the leg belongs to.

If it is not controlled i_{zu} raises the RMS value of the arms currents, thus, increasing the losses of the active and passive leg components, and creating disturbances during transients [12]. Reference [2] proposes to control the average capacitor voltage to generate a reference control i_{zu}, as illustrated in Fig 3.12. The capacitor average voltage is represented by $\bar{V}_{c\,u}$, where "u" is phase that the leg belongs to. For simplicity, the voltage balancing technique is explained for just one phase, but the same technique is applied to the other two phases.

The average capacitor voltage is calculated by:

$$\bar{V}_{c\,u} = \frac{1}{2N} \sum_{j=1}^{2N} v_{cju} \tag{3.20}$$

Fig. 3.11. Single-phase MMC leg
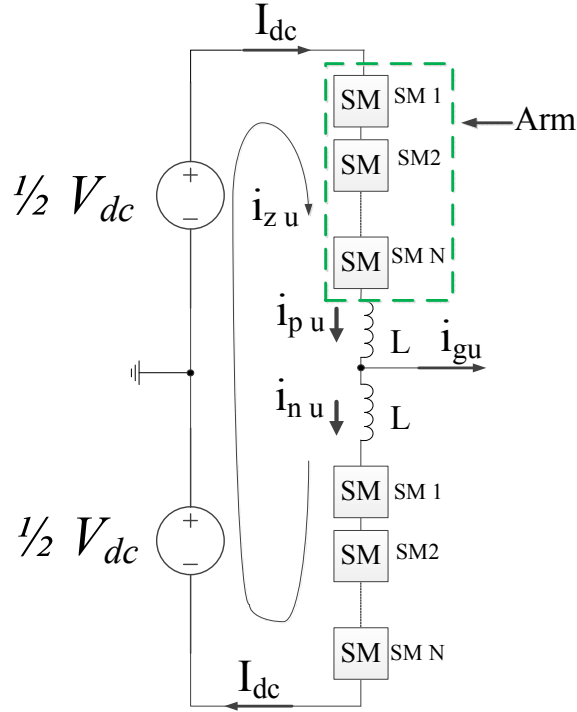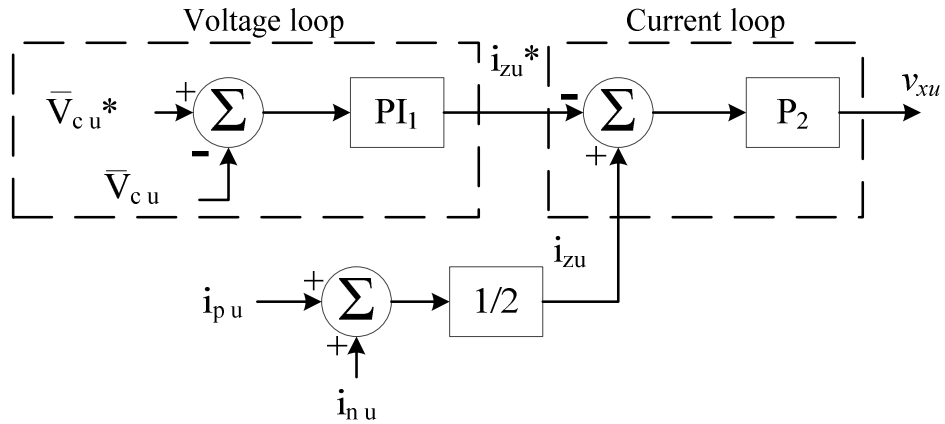

Fig. 3.12. Block diagram of the capacitor average voltage control approach

If the voltage drop across the arm inductors is neglected, the average capacitor voltage should

be $\frac{V_{dc}}{2N}$. Taking this into account, [1] proposes the following control approach:

$$i_{zu}{}^*(t) = k_1(\bar{V}_{cu}^* + \bar{V}_{cu}) + k_2 \int (\bar{V}_{cu}^* + \bar{V}_{cu})\, dt \qquad (3.21)$$

$$v_{xu}(t) = k_3(-i^*_{zu} + i_{zu})$$ (3.22)

where k_1 and k_2 are the proportional and integral gains of PI_1, respectively, shown in Fig. 3.12 and k_3 is the proportional gain of P_2 . A trial and error approach using the Matlab/Simulink™ model in Appendix A.4 was applied to select the gains starting with the values proposed in [10] (k_1 = 0.3 A/V, k_2 = 3 A/(Vs) and k_3 = 1 V/A). After several tests, with different gains, the best results were obtained with the values proposed in [10]. There are two loops in this controller, as presented in Fig. 3.12.

The output of the voltage loop produces the current reference $i_{zu}{}^*$ necessary to force the average capacitor voltage to follow the reference the commanded voltage $\bar{V}^*_{cu}$. The current loop forces the circulating current i_{zu} to follow the reference command $i_{zu}{}^*$ generated by the voltage loop. These two loops generate a voltage reference named v_{xu}. This strategy controls the average capacitor voltage and the circulating current without affecting the control of the phase current [2], [10], [12].

3.4.2 *Balancing control of the instantaneous capacitor voltage*

This controller forces the instantaneous voltage of the SM v_{cju} to follow the voltage reference $v^*_{cj\,u}$, and thus, makes sure that the SM voltages are balanced. This controller uses the polarity of the currents $i_{p\,u}$ and $i_{n\,u}$ to select the sign of the controller output. For the upper arm, the SM capacitors are charging and power is transferred into the SM capacitors when $i_{p\,u}$ is positive, while the SM capacitors are discharging and power transferred out of the SM capacitors when $i_{p\,u}$ is negative. The same is true for the lower arm. The control block diagram of this controller is presented in Fig. 3.13 and its equations are [2]:
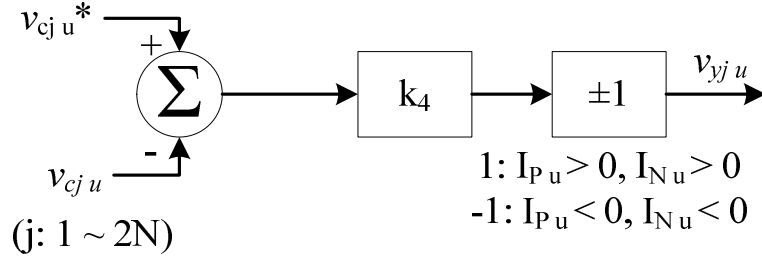
Fig. 3.13. Individual capacitor voltage balancing control block diagram

$$v_{yj\,u} = \pm 1\, k_4 \left(v^*_{cju} + v_{cju} \right); \ 1: i_{p\,u} > 0, -1: i_{p\,u} < 0 \tag{3.23}$$

where v^*_{cju} given by $\frac{V_{dc}}{N}$, since the arm SMs operate in a complementary way, k_4 is the proportional constant that is shown in Fig. 3.14. The value of the gain is selected with the same procedure as in Section 3.2.1. The conclusion of this process is that a gain $k_4 = 0.5$, proposed in [10], works well for this controller. The model used for testing for this gain is provided in Appendix A.4.

3.4.3 *Arm average voltage balancing control*

Applying Routh-Hurwitz stability criterion to the previous two controllers provides that the system is unstable if the MMC operates as a rectifier [10]. To make the system stable for all operating modes, the controller shown in Fig. 3.14 is proposed in [10]. The control purpose is to minimize the difference between the average voltages of the upper $\bar{V}_{cp\,u}$ and lower arm $\bar{V}_{cn\,u}$. The control law for this controller is as follows:

$$v_{zu} = \pm 1\, k_5 \left(\bar{V}_{cp\,u} - \bar{V}_{cn\,u} \right) i_{g\,u}(t); \quad 1: inverter\ mode,\ -1: rectifier\ mode \tag{3.25}$$

where $i_{g\,u}(t)$ is the grid phase current corresponding to the arms being controlled and k_5 is the proportional gain of the controller, selected to be 0.5 A^{-1} [10], by using the same process as in
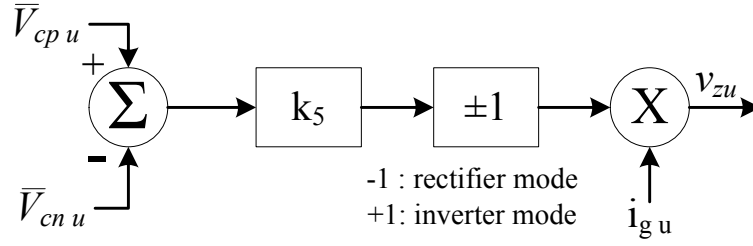
Fig. 3.14. Arm average voltage balancing control block diagram

Section 3.2.1. When the MMC is operating as an inverter, k_5 is positive, and when is operating

as a rectifier, k_5 is negative [10].

3.5 Voltage Reference Generation

Once all the capacitor voltage controllers have been implemented, and the control voltages are

produced by the current controllers, the reference voltage for switching the switches in a SM is

formed as shown in Fig. 3.15. This reference voltage is the control voltage for the PS-PWM

algorithm. Since the MMC arm operations are complementary, the references for the upper arm

and the lower arm are also complementary. In Fig. 3.15 $v_{rpj\,u}$ is the control voltage for a SM

capacitor in the upper arm and $v_{rnj\,u}$ is the control voltage for a SM capacitor in the lower arm;

these variables are given by:

$$v_{rpj\,u} = v_{xu} + v_{yju} + v_{zu} + \frac{v_u^*}{N} + \frac{V_{dc}}{2N} \tag{3.24}$$

$$v_{rnj\,u} = v_{xu} + v_{yju} + v_{zu} - \frac{v_u^*}{N} + \frac{V_{dc}}{2N} \tag{3.25}$$

where v_{xu}, v_{yju} and v_{zu} are given by the controllers explained in previous sections. The variable

v_u^* is generated by the controller explained in Sections 3.3. The term $\frac{V_{dc}}{2N}$ in (3.24) and (3.25) is a

voltage feedforward term which corresponds to half of the nominal SM voltage; the nominal SM

voltage could be used as well. Making use of simulations it was determined that using $\frac{V_{dc}}{2N}$

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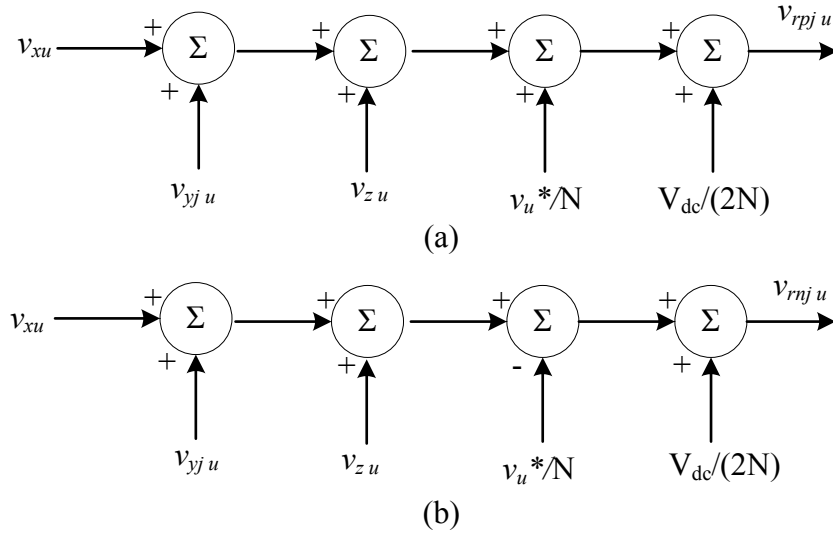
Fig. 3.15. Reference voltage generation: (a) top arm, (b) bottom arm

reduces the settling time of the overall capacitor voltage controller. The terms $v_{rpj\,u}$ and $v_{rnj\,u}$ are normalized by the instantaneous individual capacitor voltage, and then used as the control voltage for the PS-PWM to control the switching of the SMs.

The Matlab/Simulink™ implementation of Fig. 3.15 together with the PS-PWM algorithm to control the switches is depicted in Appendix A.4.

3.6   Conclusions

Each of the controllers of the MMC-based HVdc terminal performs a different function and by the combination of all of them it is possible to control the active and reactive powers injected into a grid.

For the capacitor voltage controllers, it is important to control the circulating current between the legs and the dc-link, to reduce losses and ensure system stability. The arm-balancing voltage control is required to make the capacitor voltage controllers stable under all operating modes of the terminal.

For the current and dc voltage controllers, the use of prefilters improves the system bandwidth and step response. Both controllers have been designed for a transfer function modeling the functioning of an MMC and need to be validated by simulations.

These controllers will be validated through system simulations in Chapter Four. The controllers will be also compared with a sensorless control technique for the inverter terminal that is described in Chapter Four.

References

[1]   J. Arrillaga, Y.H. Liu, and N.R. Watson "VSC Transmission," in *Flexible Power Transmission, The HVDC Options*, West Sussex: John Wiley & Sons 2007. pp. 299-309.

[2]   M. Hagiwara and H. Akagi, "PWM control and experiment of modular multilevel converters," *Proceedings of IEEE Power Electronics Specialists Conference. PESC 2008*, pp. 154-161.

[3]   P.C. Krause, "Reference-Frame Theory," in *Analysis of Electric Machinery*, 1st ed. McGraw Hill, 1986. pp 133-157.

[4]   Inter-American Development Bank. *Colombia-Panama Interconnection* [Online] Available:
http://www.iadb.org/en/projects/project-description-title,1303.html?id=rs%2Dt1241 [Accessed: Jan.31, 2013].

[5]   S. M., Rodrigues F., "Dynamic Modeling and Control of VSC-based Multi-terminal DC Networks," M.S. Thesis, Dept. Elect. Eng. and Comp. Sci. Lisboa Tech. Univ. Portugal, 2011.

[6]   A. Yazdani and R. Iravani, "Space Phasors and Two-Dimensional Frames" in *Voltage-Sourced Converters in Power Systems - Modeling, Control and Applications*, 1st ed. Hoboken, NJ John Wiley pp. 105.

[7]   M. S. Huertas, "The Use of Power Electronics for Emulating Electric Power Distribution Feeders," M.S. Thesis, Dept. of Elect. Eng., Univ. of Arkansas, Fayetteville, USA, 2008.

[8]   T. Rybarski and B. Sfurtoc, "Optimization of Multilink DC Transmission for Supergrid Future Concepts," M.S. Thesis, Dept. of Energy Tech., Aalborg Univ., Aalborg, Denmark, 2012.

[9]   M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2903, 2912, Oct. 2010.

[10] M. Hagiwara, R. Maeda, and H. Akagi, "Control and Analysis of the Modular Multilevel Cascade Converter Based on Double-Star Chopper-Cells (MMCC-DSCC)," *IEEE Transactions on Power Electronics*, vol. 26, no. 6, pp. 1649, 1658, June 2011.

[11] E. Solas, G. Abad, J. A. Barrena, A. Cárcar, and S. Aurtenetxea, "Modulation of Modular Multilevel Converter for HVDC application," *Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International*, 2010, pp. T2–84-T2–89.

[12] A. Antonopoulos, L. Angquist, H-P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter," *Proceedings of 13th European Conference on Power Electronics and Applications*, EPE '09. pp. 1-10 Sept. 2009

APPENDIX A.1

PARK'S TRANSFORMATION

The Park's Transformation is implemented in Matlab/Simulink™ using the blocks developed by Andres Escobar Mejia who is a PhD. candidate in the Electrical Engineering Department at the University of Arkansas. The Park's Transformation is divided into two steps first it, the abc variables are transformed into the $\alpha\beta$ axes and then to the dq axes as follows:

$$x_{\alpha\beta} = T_{\alpha\beta}x_{abc} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{1}$$

$$x_{dq} = T_{dq}x_{\alpha\beta} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{2}$$

where x is any variable in the abc frame; for the case illustrated in Fig. A.1 x can be either the grid currents or voltages. The grid angle θ and is calculated with a phase locked loop (PLL) as shown in Fig. A.2.

The gains used in the PLL PI controller are k_p = 2 and k_i = 0.1 and w is the grid ideal angular frequency, 377 rad/s.

The inverse Park's Transformation is also done in two steps as follows:

$$x_{\alpha\beta} = T_{dq}^{-1}x_{dq} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix}\begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{3}$$

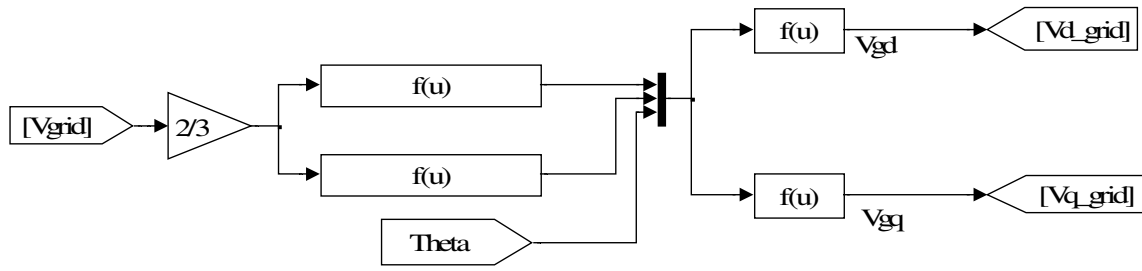$$x_{abc} = T_{\alpha\beta}^{-1}x_{\alpha\beta} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{4}$$

Park's Transformation for the grid voltages
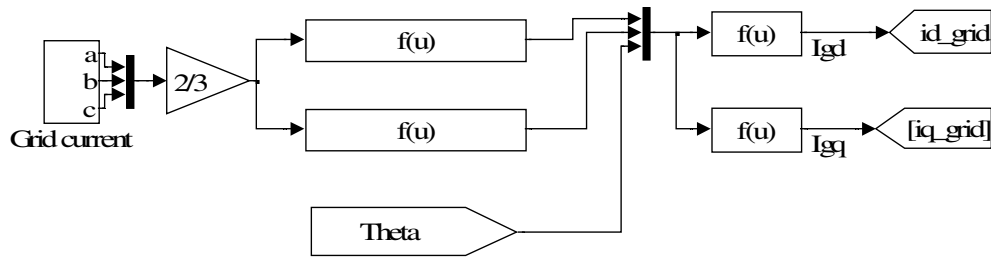
Park's Transformation for the grid currents

Fig. A.1. Park's Transformation implemented in Matlab/Simulink™

PLL
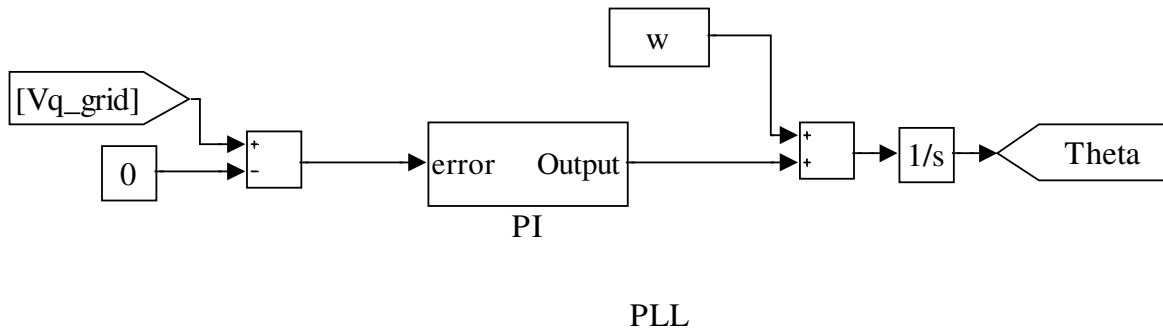
Fig. A.2. PLL to calculate α implemented in Matlab/Simulink™

The Matlab/Simulink™ of the inverse Park's Transformation is done as depicted in Fig. A.3.

Fig. A.3. Reverse Park's Transformation implemented in Matlab/Simulink™

APPENDIX A.2

TWO-LEVEL RECTIFIER MODEL
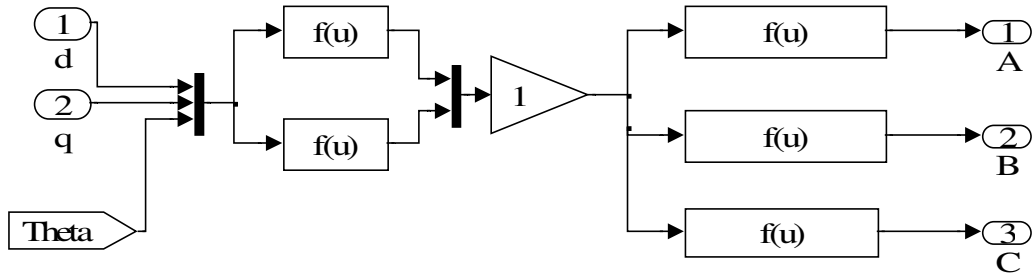
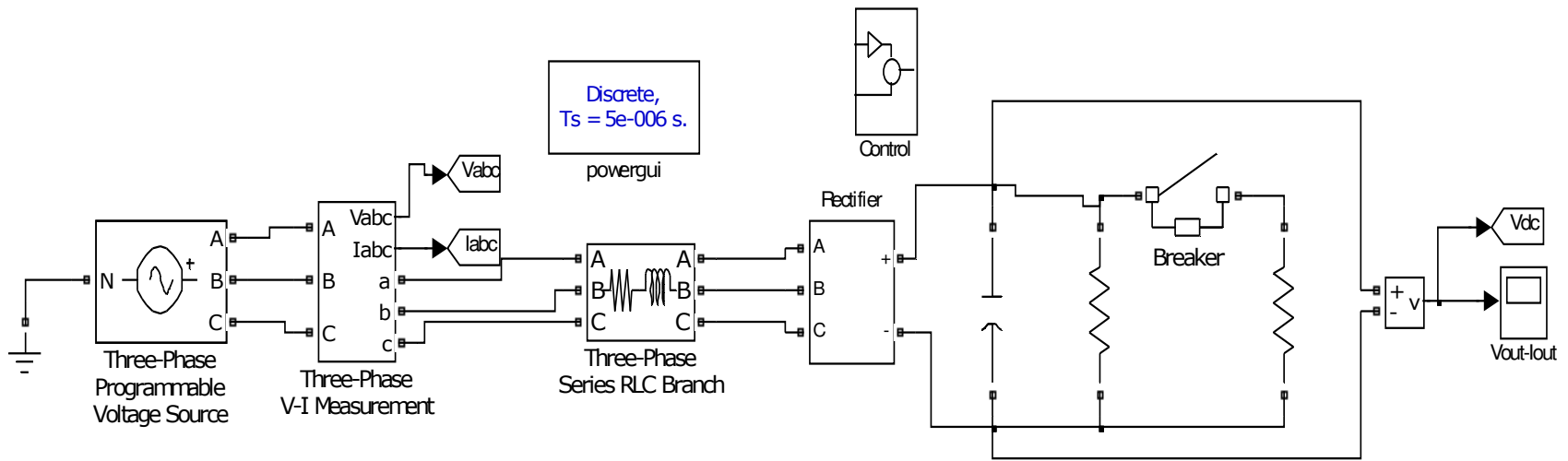The Matlab/Simulink™ model used for tuning the capacitor value for a two-level rectifier is exemplified in Fig. A.3.

Fig. A.3. Two level rectifier as modeled in Matlab/Simulink™

APPENDIX A.3

MATLAB™ CODE FOR CALCULATING THE CONTROLLER GAINS

This appendix presents the Matlab™ code written to calculate the gains of the dc-voltage and current controllers explained in Chapter Three. For the dc-voltage controller the following code was used:

```
%% Vdc ontrol %
C = 30e-3; %dc capacitance
Gdc = tf(1,[C 0]); %dc cap transfer function

% To calculate the gains of the Vdc controller %
damp=sqrt(2)/2; %damping
fcdc=40; %controller natural frequency in Hz, must be at least wn/10
wndc=2*pi*fcdc; %controller natural frequency in rad/s
kidc=C*wndc^2; %integral gain of current controller
kpdc=2*damp*wndc*C; %proportional gain of current controller
Cdc=tf([kpdc kidc],[1 0]); %Vdc controller tf

% Pre-filter %
Fdc=tf(1,[kpdc/kidc 1]); %pre-filter tf to minimize overshoot
controller = feedback(Gdc*Cdc,1);
controller_pre = Fdc*feedback(Gdc*Cdc,1);

% Stability plots %
figure(3)
step(controller,controller_pre)
figure(4)
bode(controller,controller_pre)
```

For the current controller the following code was used:

```
%% current control %
L=28e-3;
R=0.79;
Ginv = tf(1,[L R]); %Inverter transfer function

% To calculate the gains of the current controller %
damp=sqrt(2)/2; %damping
fci=400; %controller natural frequency in Hz
wn=2*pi*fci; %controller natural frequency in rad/s
kic=L*wn^2; %integral gain of current controller
kpc=2*damp*wn*L-R; %proportional gain of current controller
Cc=tf([kpc kic],[1 0]); %current controller tf

% Pre-filter %
Fi=tf(1,[kpc/kic 1]); %pre-filter tf to minimize overshoot
```

```
controller=feedback(Ginv*Cc,1);
controller_pre=Fi*feedback(Ginv*Cc,1);



% Stability plots %
figure(1)
step(controller,controller_pre)
figure(2)
bode(controller,controller_pre)
```

MATLAB/SIMULINK™ MODELS USED FOR THE CAPACITOR

VOLTAGE CONTROLLERS

The Matlab/Simulink ™ model used for evaluating the capacitor voltage controller gains is depicted in Fig. A.4
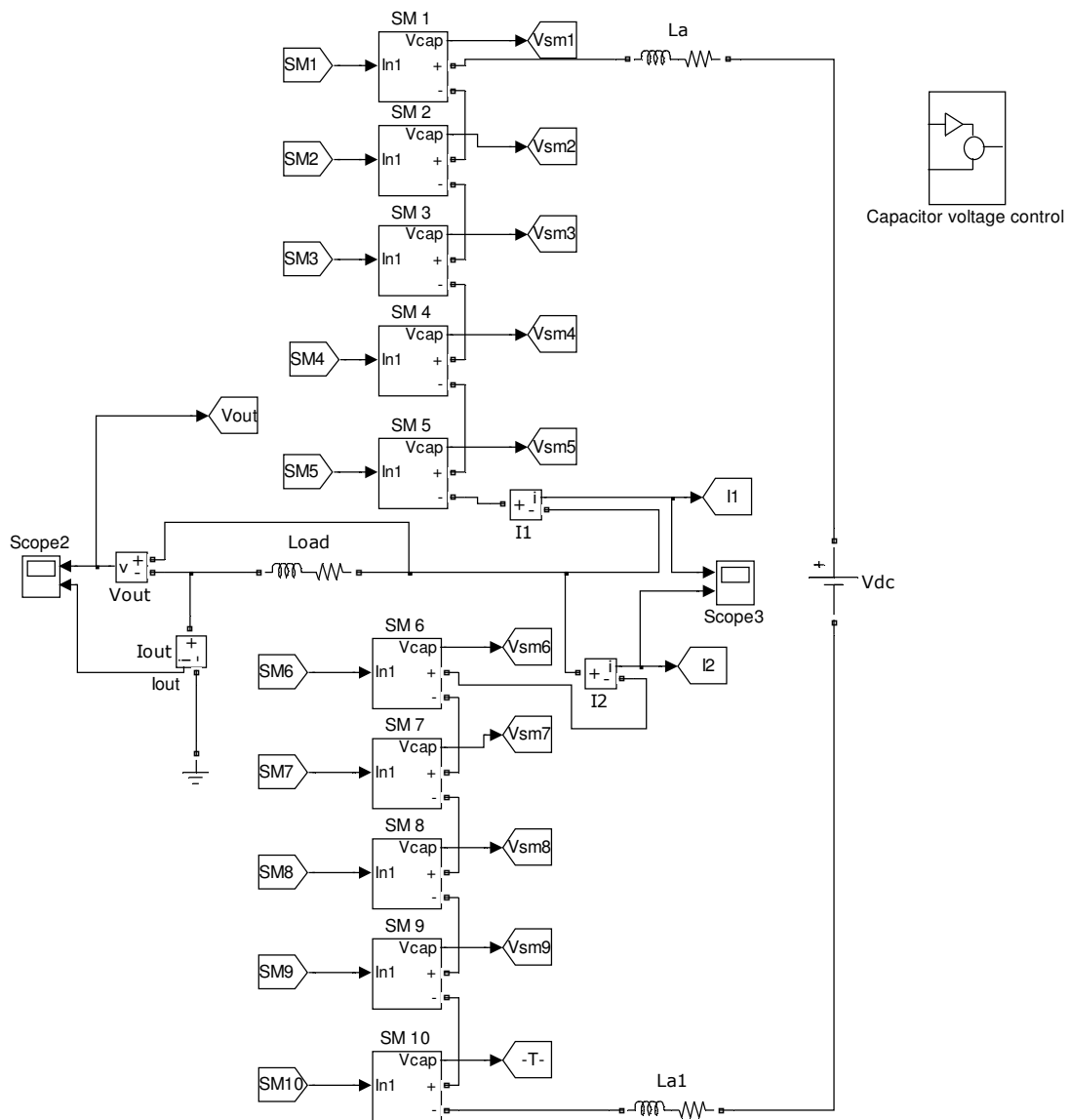
Fig. A.4. MMC terminal used for evaluating the gains of the controllers in Section 3.4
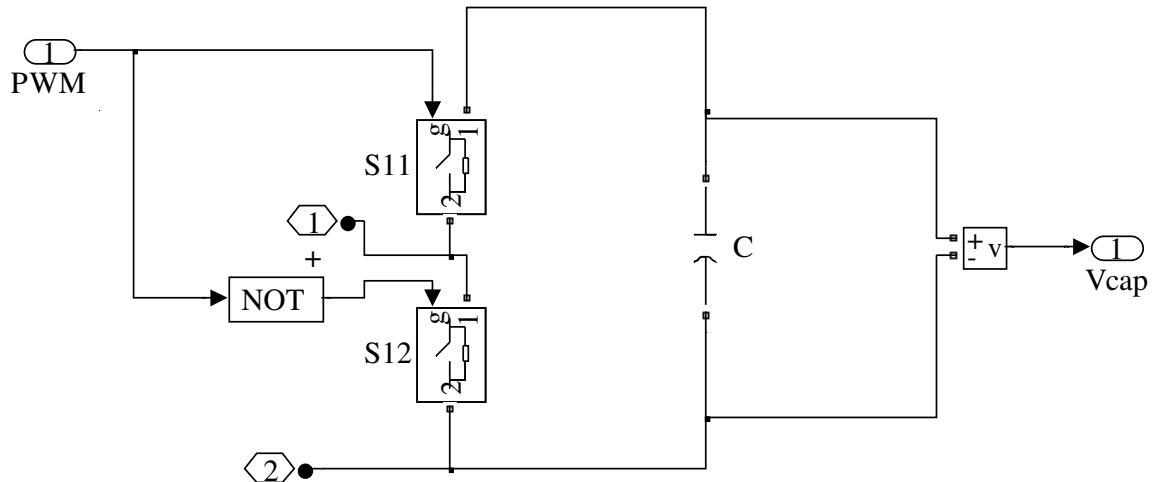
Fig. A.5. SM representation in Matlab/Simulink™
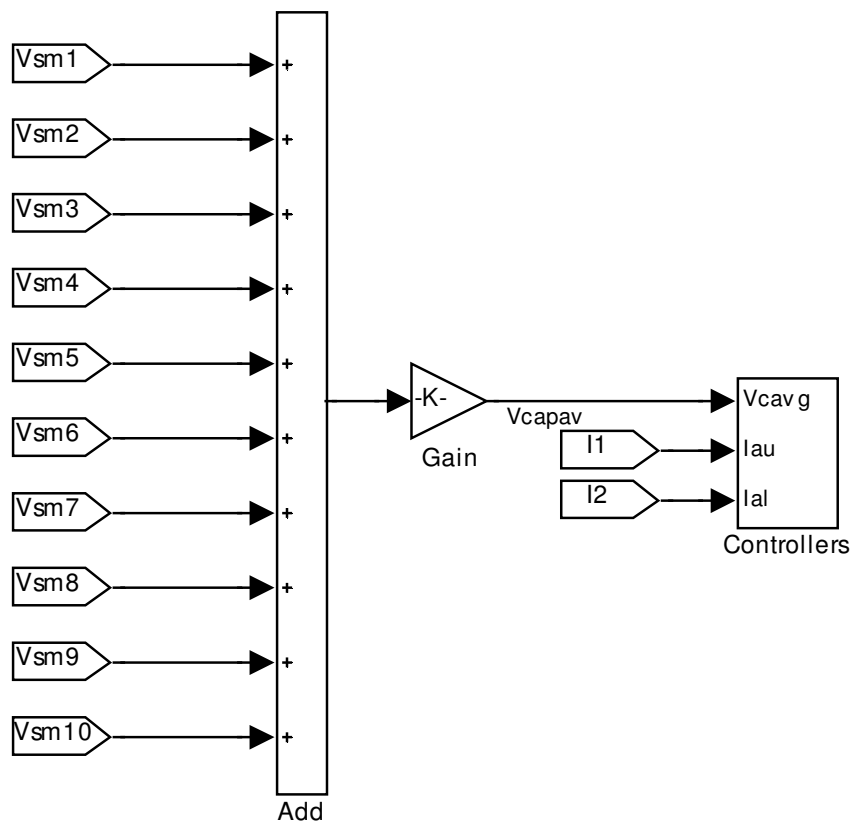
Fig. A.6. Calculation of the capacitor average voltage in Matlab/Simulink™
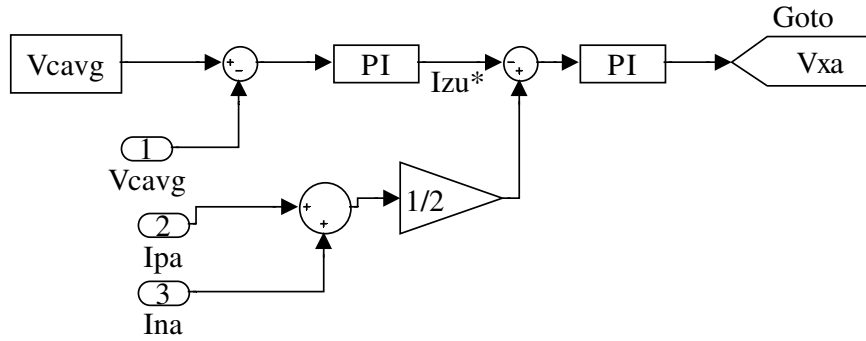
Fig. A.7. Capacitor average voltage control in Matlab/Simulink™
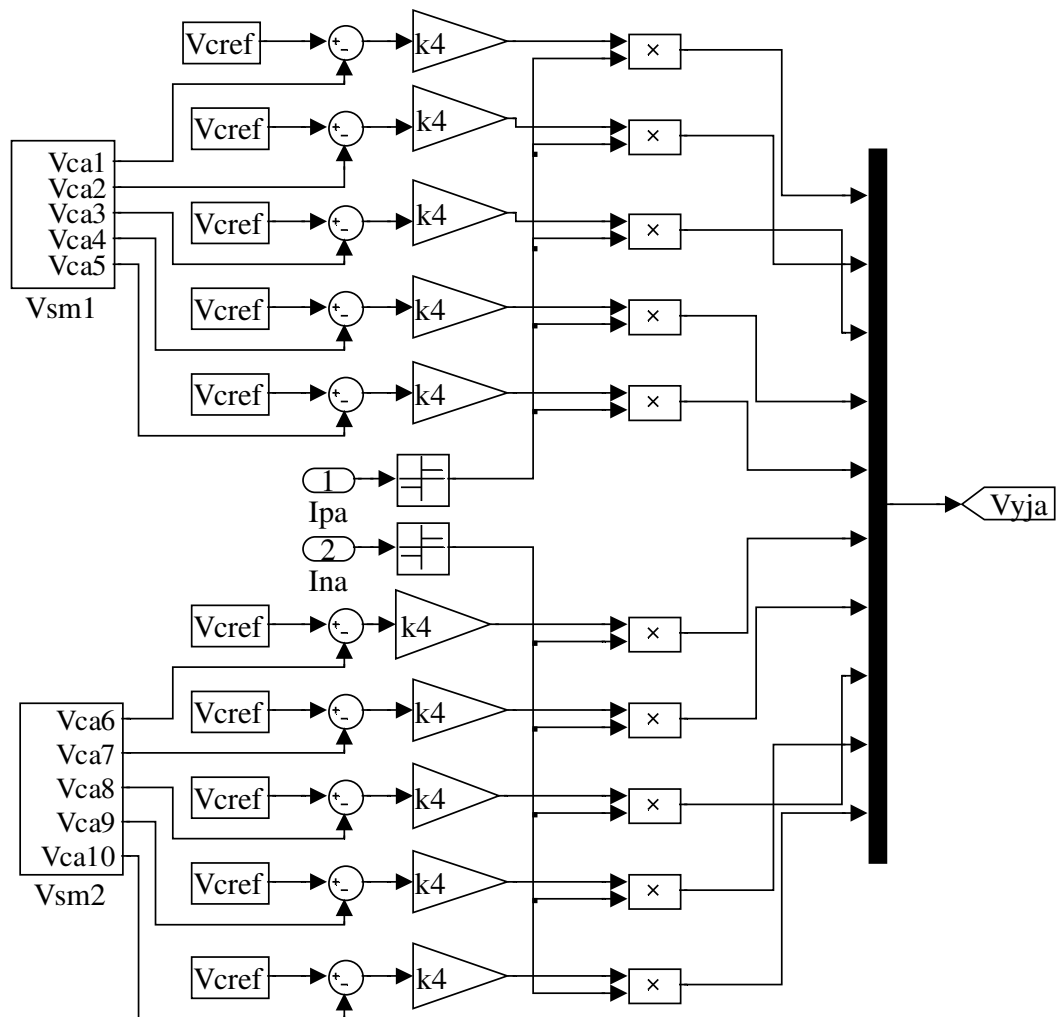
Fig. A.8. Balancing control of instantaneous capacitor voltages in Matlab/Simulink™

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Fig. A.9. Arm-balancing voltage control in Matlab/Simulink™
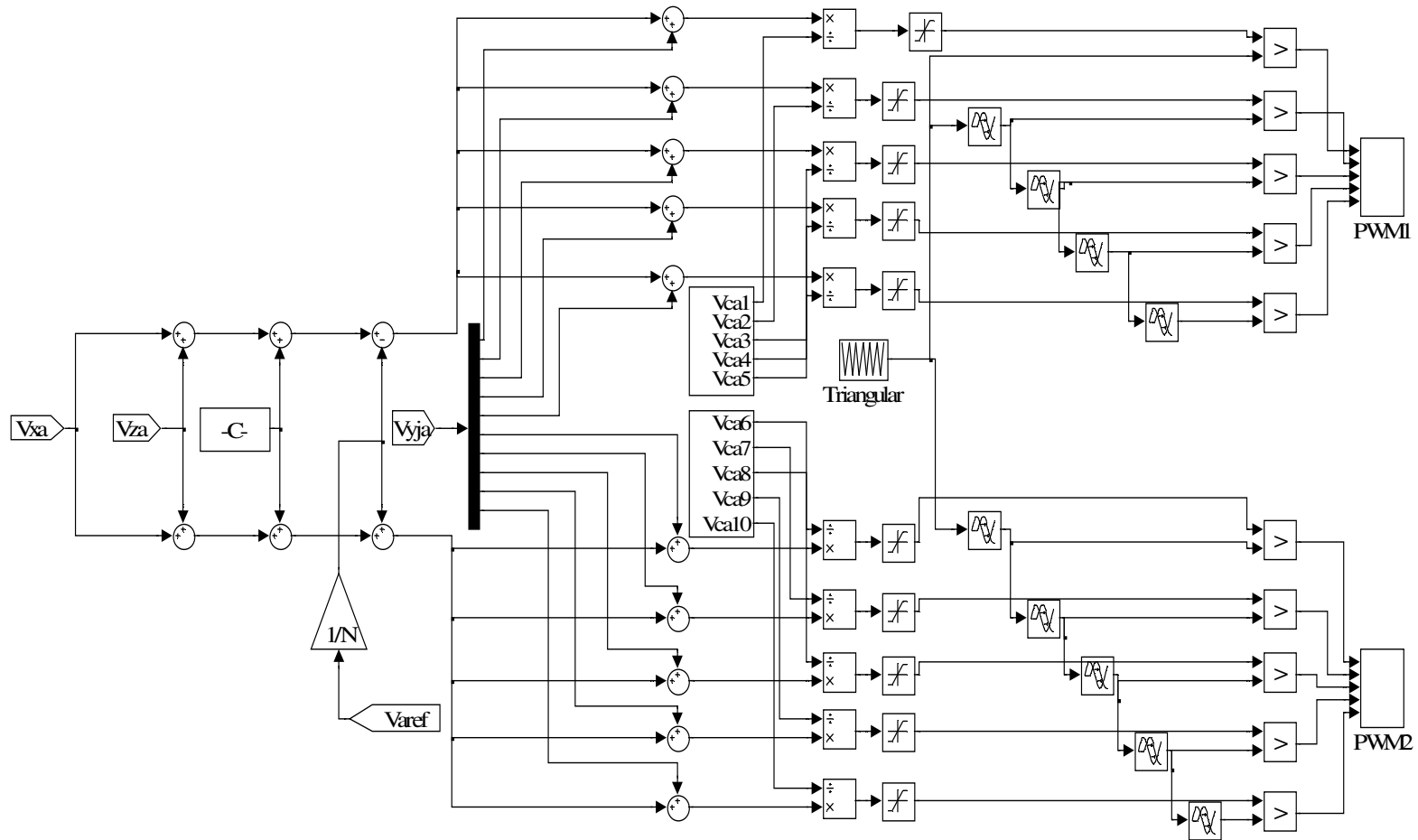
Fig. A.10. Switching signal generation in Matlab/Simulink™

CHAPTER FOUR

SIMULATION RESUTLS AND SENSORLESS CONTROL OF THE SELECTED TWO-TERMINAL HVDC SYSTEM

Abstract

The various gains for the controllers designed in Chapter Three to be proved to be suitable for this case study when using simplified models. A full simulation model of the two-terminal HVdc system is built using the developed controllers to validate the design approaches and effectiveness. The procedure for implement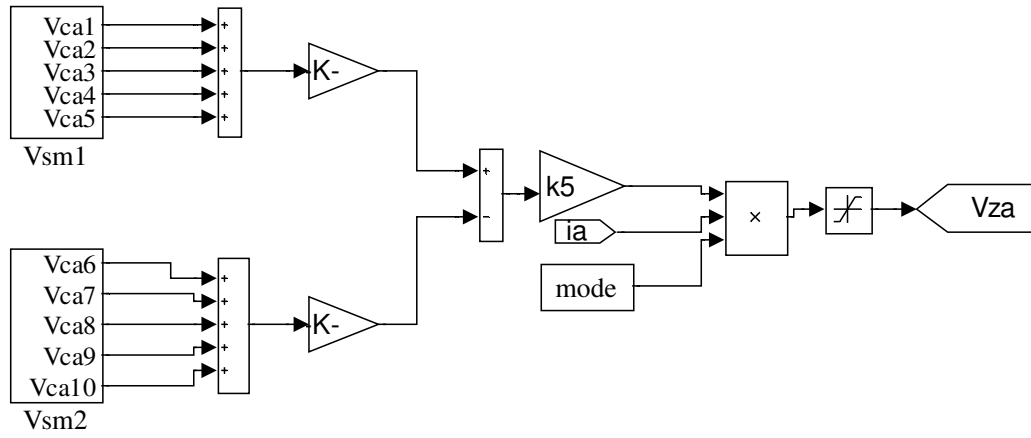ing a sensorless control technique on an MMC inverter terminal is also presented and validated using simulations. The sensorless control technique is robust and able to sense the grid voltages under ideal and non-ideal grid conditions with satisfactory results.

4.1   Introduction

The controllers designed in Chapter Three are implemented in a full simulation model of the selected two-terminal HVdc system. This model is used to analyze the controller responses to different operating conditions. This chapter also implements a sensorless technique to synchronize the inverter terminal with the grid based on the technique proposed in [1]. The sensorless technique is compared with the controllers proposed in Chapter Three and evaluated under frequency changes and harmonic pollution on the grid-side voltage.

4.2   Matlab/Simulink™ Setup of Two-Terminal HVdc System

A simulation model of an MMC-based two-terminal HVdc system was built using Matlab/Simulink™ to validate the design methodology for controllers in Chapter Three. The

characteristics of the system corresponding to the interconnection between Panama and Colombia [2] are presented Table 4.1 and the overall Matlab/Simulink™ setup is given in Fig. 4.1. The Terminal 1 and Terminal 2 blocks have inside the MMC Matlab/Simulink™ model presented in Appendix B.1. Inside the Grid 2 block are the Grid impedance, the Three-Phase Breaker, and the Grid blocks connected in the same way as presented in Fig. 4.1 for Grid 1. The content of the outer controllers is given in Appendix B.1. The contents of the Capacitor voltage control blocks are illustrated in Appendix B.1. The gains for the controllers were calculated as shown in Chapter Three, and then tuned to work with the two-terminal model depicted in Fig. 4.1. The gains values used are given in Table 4.2.
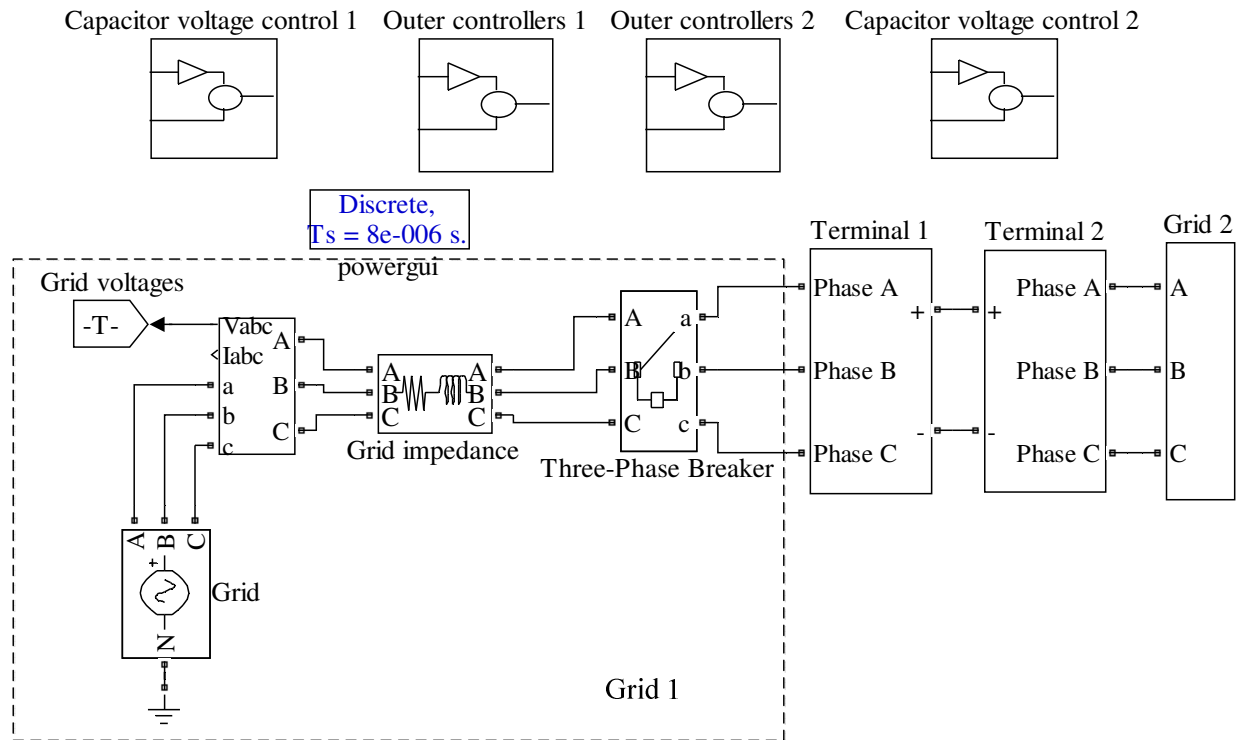

Fig. 4.1. Matlab/Simulink™ simulation setup

Table 4.1. System parameters for the Case Study

Parameter	V_{dc}	$V_{grid1,2}$	C_{SM}	L_a	f_{sw}	f_o	L_{grid}	R_{grid}	P
Value	±200 kV	230 kV	1 mF	7 mH	2 kHz	60 Hz	28 mH	0.8 Ω	500 MW

Table 4.2. Controllers gains for the system whose parameters are in Table 4.1

	dc-voltage controller		Inner current controllers		Capacitor voltage controllers				
Parameter	k_{p_dc}	k_{i_dc}	k_{p_i}	k_{i_i}	k_1	k_2	k_3	k_4	k_5
Value	5.33	1050	78.7	1.77×10^5	0.3	3	1	0.35	0.35

4.3 Simulation Results of the Case Study

This section evaluates the results of the simulations done with emphasis on the outer controllers and the SM capacitor voltage controller. The operating conditions are V_{dc_ref} = 400kV, Q_{ref1} = 0MW, P_{ref} =500 MW, and Q_{ref2} = -100MW, a reactive power flow reversal is commanded at t = 0.23 s (Q_{ref2} = 100MW) and an active power flow reversal is commanded at t = 0.25 s (P_{ref} = -500 MW).

4.3.1 Outer controller results

The line-to-line voltages at Terminal 1 are shown at the top of Fig. 4.2. From t = 0 s until t = 0.25 s, Terminal 1 operates as a rectifier. At t = 0.25 s, the power flow reverses so Terminal 1 operates as an inverter. The THD measured of the voltage waveform is 2.9%. There are no filters added to the system and the THD is expected to decrease as the number of levels of the MMC-based terminal is much higher in a real-world application [3].
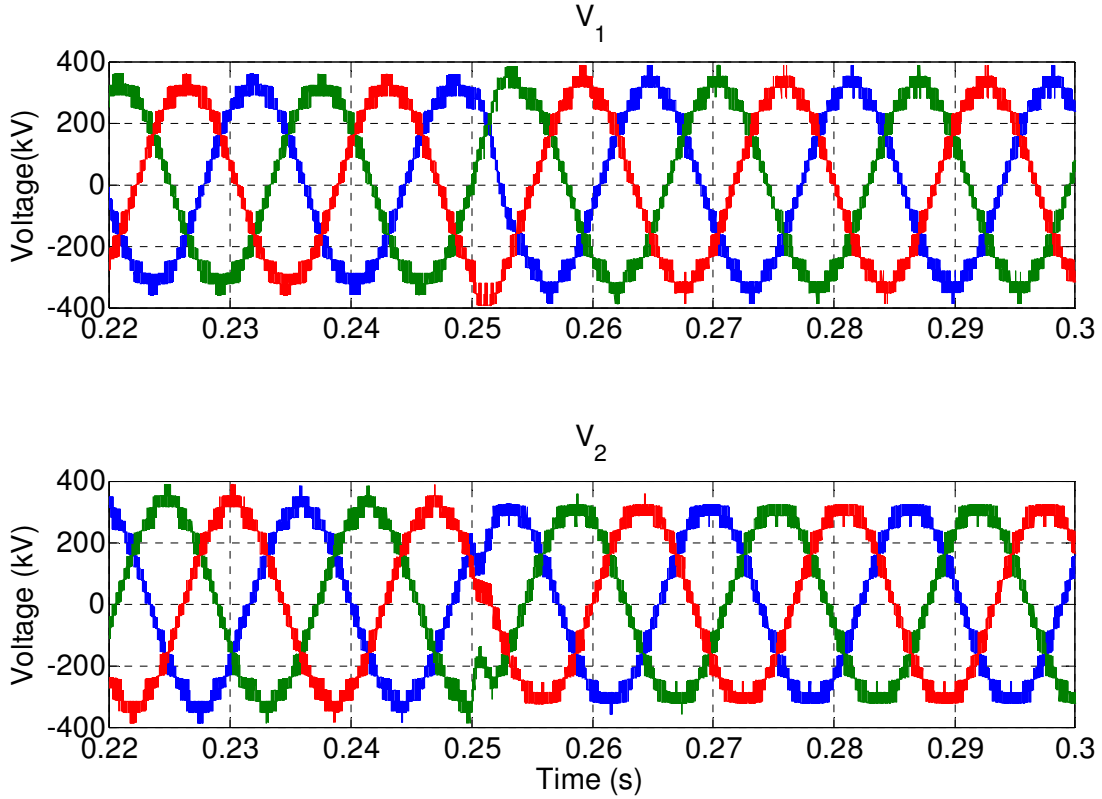
Fig. 4.2. MMC terminals voltages: Terminal 1 (top) and Terminal 2 (bottom)

The bottom waveforms in Fig. 4.2 are the ac voltages of Terminal 2 which is operating as an inverter until t = 0.25 s when the power flow reverses and starts operating as a rectifier. The voltage THD of Terminal 2 is 3.2%; there is a 0.3% increase in the THD when compared to Terminal 1. Fig. 4.2 shows that the controllers are able to keep the system stable when the power flow is reversed using a step.

The current injected into the grid for both terminals is presented in Fig. 4.3; the ac currents injected by Terminal 1 into the grid are the top waveforms. At t = 0.25 s, the power flow reversal occurs, then the controller starts reacting at t = 0.26 s, and stabilizes back at t = 0.27 s. The settling time of this controller is faster by 7 ms than the calculated in Section 3.4.2; which was
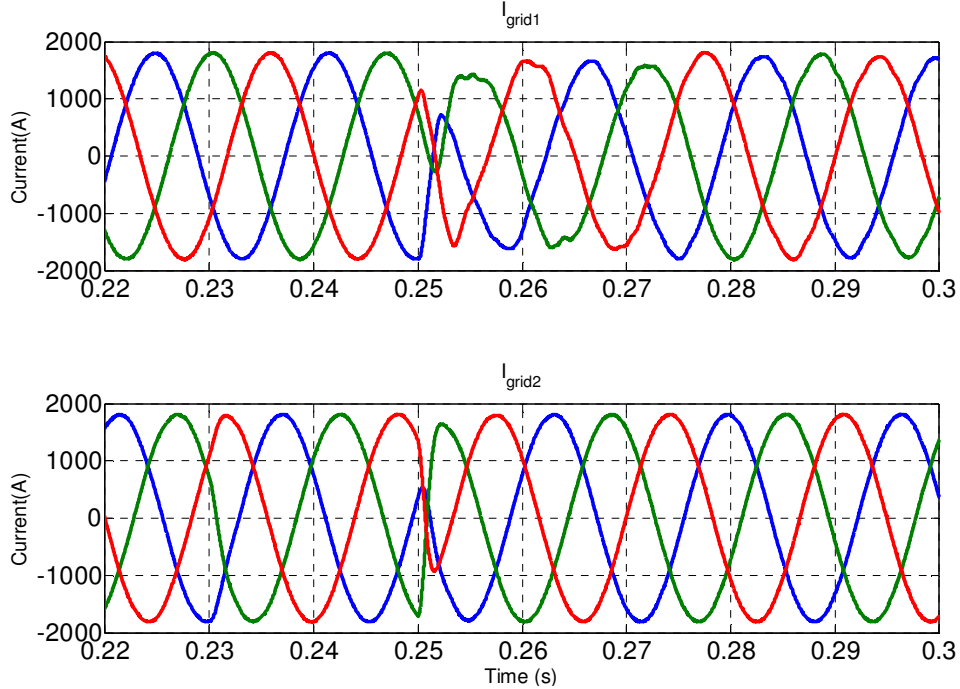
Fig. 4.3. Grid currents: Terminal 1 (top) and Terminal 2 (bottom)

calculated using a transfer function model. There is no current overshoot on any phase for currents injected by Terminal 1 into the grid.

The currents injected by Terminal 2 into the grid correspond to the bottom waveforms, and there is a no overshoot in the Phase B current at the moment of the power flow reversal. The THD of the current injected into Grid 1 is 1.08%, and the THD for the current injected into grid 2 is 1.23%. Both currents have a good THD performance without any filters.

The active power injected into Grid 2 is shown by the green line in Fig. 4.4, and the active power reference given to the controller is depicted by the blue line. The reactive power is shown by the black line, with its reactive power reference indicated in red. The active power is injected

65
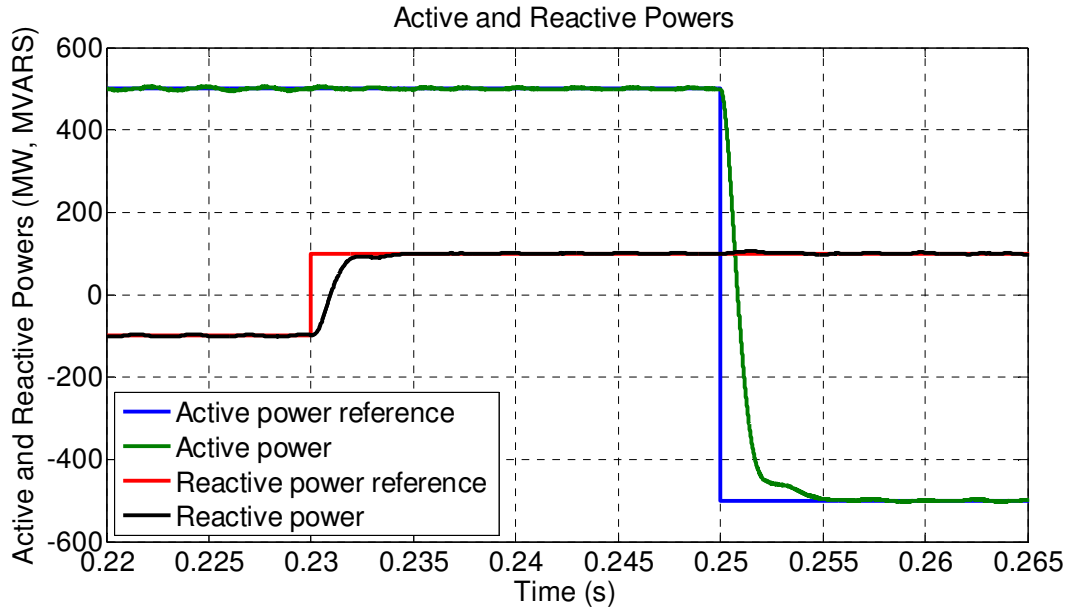
Fig. 4.4. Active power reference (blue) and actual (green) and reactive power reference

(red) and actual (black) on Terminal 2

into Grid 2 when the reference is positive and injected into Grid 1 when it is negative. The controllers are able to track the power reference even under power flow reversal.

Nor the active or reactive powers have an overshoot when the power flow is reversed. At t = 0.23 s, the reactive power reference changes from a 0.98 lagging to a 0.98 leading, validating the capability of the controller to control independently active and reactive powers.

4.3.2. *Capacitor voltage controller results*

The phase (blue) and the circulating (green) currents of Phase A in Terminal 2 are depicted at the top graph of Fig. 4.5. The maximum value of the circulating current is 804 A, with a dc-offset of 431 A. An FFT analysis to the circulating current reveals a 2nd harmonic fundamental

Fig. 4.5. Phase and circulating currents (top), and phase and arms currents (bottom) when circulating current is controlled

frequency [4]. The phase (blue), upper arm (green) and lower arm (red) currents of Phase A are shown in the bottom graph of Fig. 4.5. This graph shows the contribution of each arm current to the phase current, and that the harmonic pollution caused by circulating current only affects the arm currents. Both upper and lower arm currents present a 30% 2nd harmonic and a dc-offset of 431 A caused by the circulating current. If the dc-current of the three legs is multiplied by the dc voltage it yields 517 MW, which coincides with the active power reference of 500 MW [4], the difference between the two might be caused by inaccuracies of the FFT analysis done in Matlab/Simulink™.

The Phase A current is given by the difference between the two arm currents in a leg per the convention selected. This difference cancels out the dc-offset and the 2nd harmonic present in both of the arm currents. The capacitor average voltage control is turned off at t = 0.3s. One

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cycle after the capacitor average voltage control is turned off, the peak circulating current increases beyond the peak phase current, as illustrated in Fig. 4.6. In this case, the circulating current increases to the point where it cannot be controlled and the system collapses. This test shows the importance of controlling the circulating current on the MMC [4].

To illustrate the complementary operation of the MMC arms two SM that have the same position in the upper and lower arm are selected; therefore, the SM 1 (blue) and SM 6 (green) capacitor voltages of Phase A leg for Terminal 2 are illustrated in Fig. 4.7. The ripple in the capacitor voltage is ±1.3% of the rated SM voltage (80 kV) the calculated ripple using (2.12) is

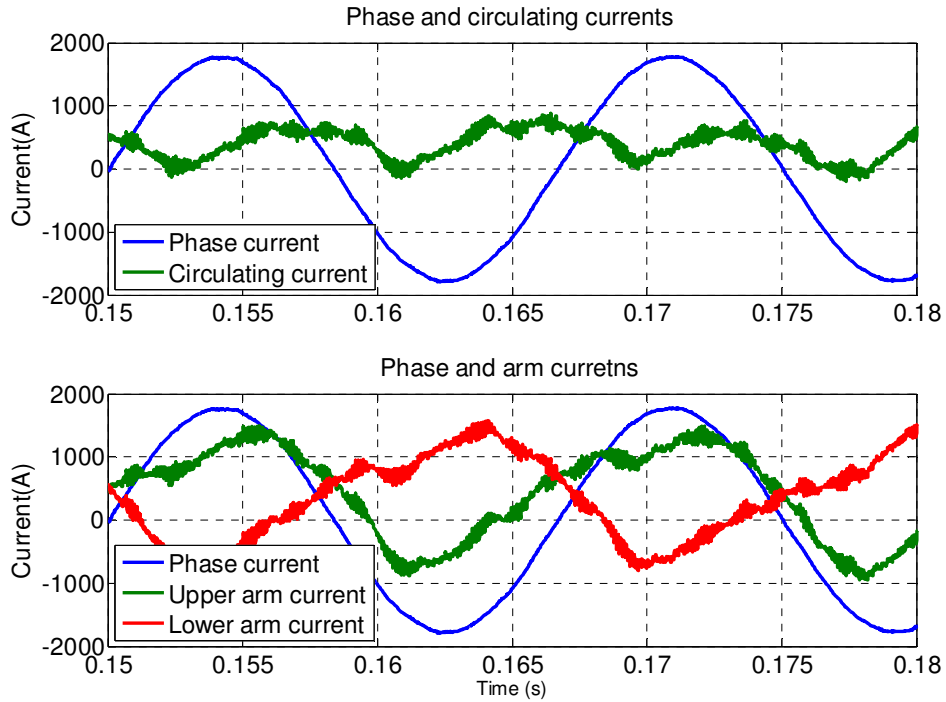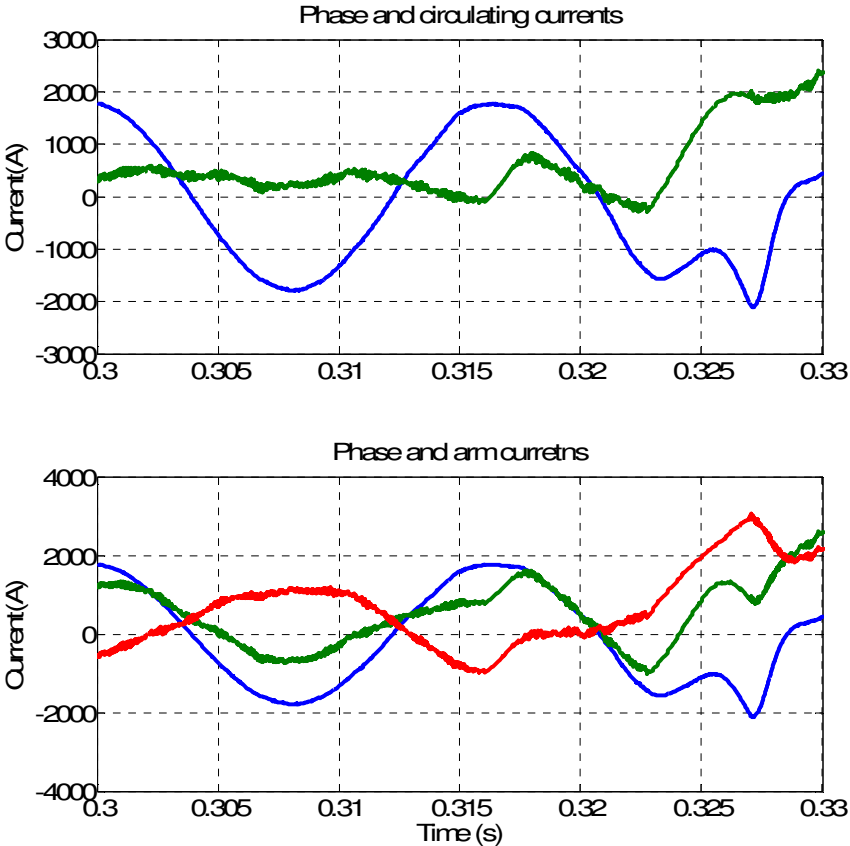**Fig. 4.6. Phase and circulating currents (top), and phase and arms currents (bottom) when the circulating current is not controlled**

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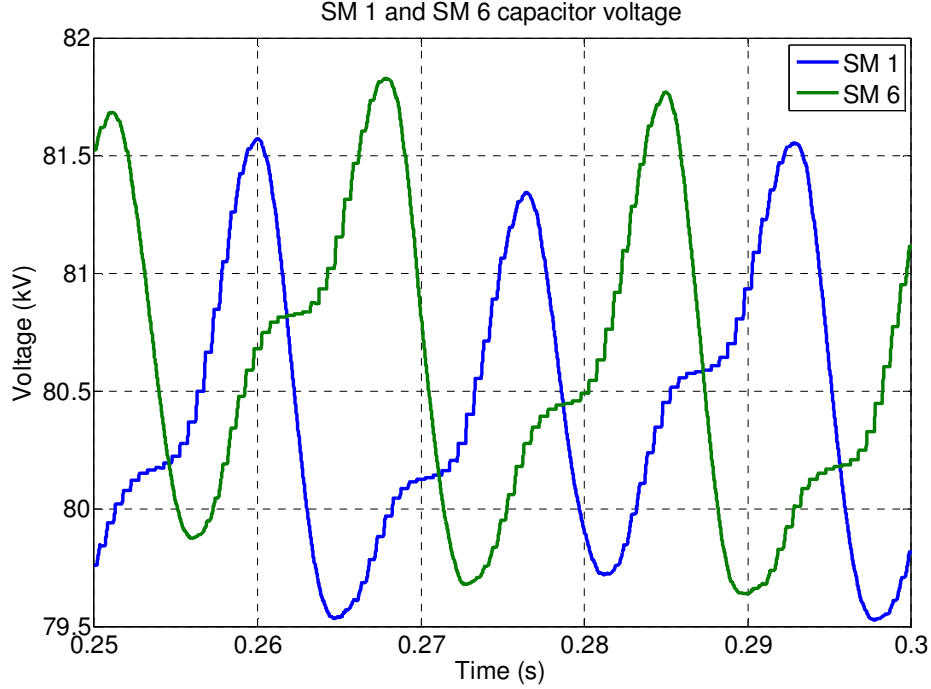
Fig. 4.7. SM1 (blue) and SM6 (green) capacitor voltages

±1.2%. The waveform of the capacitor voltage has a 60-Hz fundamental-frequency component with 56.7% 2nd harmonic component caused by the circulating current.

4.4   Sensorless Control Technique

This controller assumes that the MMC terminal has an infinite number of levels so the ideal operation can be analyzed using the circuit diagram of Fig. 4.8. Using Kirchhoff's voltage and working on the synchronously-rotating frame yields:

$$L_{grid}\frac{d}{dt}\left(i_{d\_grid}\right) = v_{d\_inv} - v_{d\_grid} - R_{grid}i_{d\_grid} + L_{grid}\omega_o i_{q\_grid} \qquad (4.1)$$

$$L_{grid}\frac{d}{dt}\left(i_{q\_grid}\right) = v_{q\_inv} - v_{q\_grid} - R_{grid}i_{q\_grid} - L_{grid}\omega_o i_{d\_grid} \qquad (4.2)$$

where ω_o is the angular frequency of the grid, L_{grid} is the grid inductance, v_{d_inv} and v_{q_inv} are the outputs voltage of the inverter in the dq axes, and v_{d_grid} and v_{q_grid} are the grid voltages in the d-q

Fig. 4.8 Ideal MMC connected to a grid – inverter operation

frame. To decouple the axes using a sensorless controller, the following control law is used [1] in the Laplace domain:

$$v_{d\_inv} = -\frac{(As + 1)(i_{d\_grid} - g_q v_{q\_grid})}{Bs + g_d} - \omega_o L_{grid} i_{q\_grid} \qquad (4.3)$$
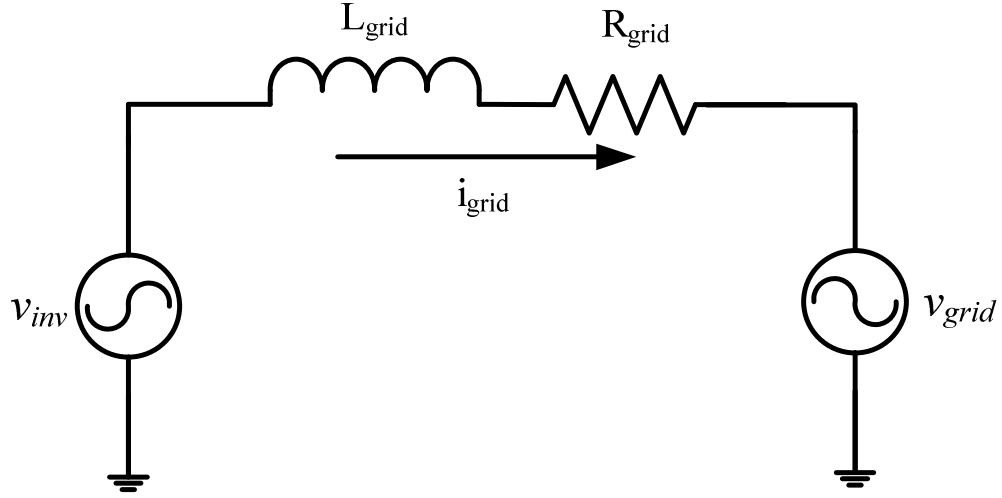
$$v_{q\_inv} = -\frac{(As + 1)(i_{q\_grid} + g_q v_{d\_grid})}{Bs + g_d} + \omega_o L_{grid} i_{d\_grid} \qquad (4.4)$$

where A is a forward direct gain, B is a forward indirect gain, g_d and g_q are the conductance gains in the d-q frame. The controller is able to estimate the grid voltages $\hat{v}_{d\_grid}$ and $\hat{v}_{q\_grid}$ at the output of its integrator as shown in Fig. 4.9. The grid currents are obtained by the difference of the arm currents, since the capacitor voltage controller requires measuring the arm currents; so no additional current sensors are required. The inverter voltages are then transformed back to the abc frame using the inverse Park's Transformation [5]. The angle used for the Park's and inverse Park's Transformation is an arbitrary angle given by:

$$\theta = \int \omega_0 t \, dt + \theta_0 \qquad (4.3)$$

where θ is changing at the same speed as the grid angle ω_0 and the initial conditions are zero.

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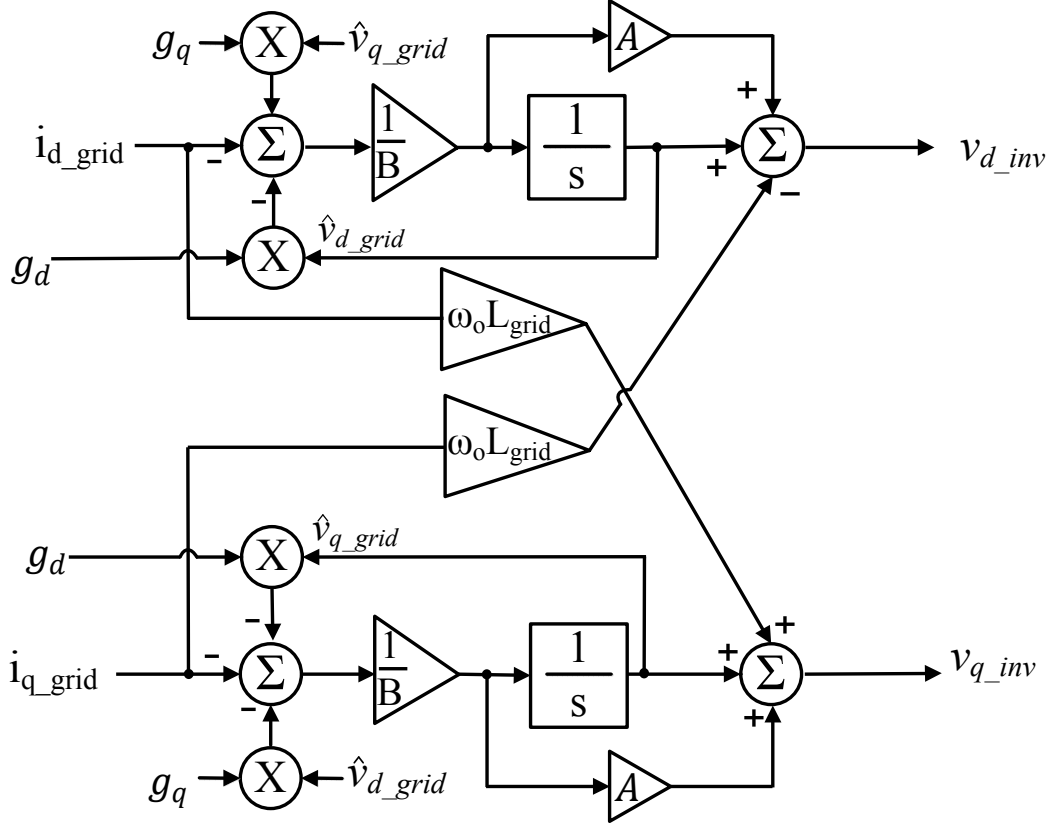
Fig. 4.9. Proposed control technique

Replacing (4.3) and (4.4) into (4.1) and (4.2), respectively, yields the transfer functions of the system as:

$$i_{d\_grid} = -\frac{Bs + g_d}{LBs^2 + (Lg_d + A)s + 1} v_{d\_qrid} + g_q v_{q\_grid}(As + 1) \tag{4.6}$$

$$i_{q\_grid} = -\frac{Bs + g_q}{LBs^2 + (Lg_d + A)s + 1} v_{q\_grid} + g_q(Av_{q\_grid}s - v_{d\_grid}) \tag{4.7}$$

Under steady-state conditions ($s\rightarrow0$) the grid currents are given by:

$$i_{d\_grid} = -g_d v_{d\_grid} + g_q v_{q\_grid} \tag{4.8}$$

$$i_{q\_grid} = -(g_d v_{q\_grid} + g_q v_{d\_grid}) \tag{4.9}$$

where the grid currents can be controlled by controlling g_d and g_q.

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4.4.1. *Transfer function parameter selection*

Transfer functions (4.6) and (4.7) must be stable for the all operational modes of the terminal. There are four parameters that need to be selected to achieve this: A, B, g_d and g_q. The parameters g_d and g_q will change depending on the selected power flow. Hence, A and B need to be selected so that the transfer function is stable for any given value of g_d and g_q. Transfer functions (4.6) and (4.7) have the same characteristic equation, thus the parameters A and B are selected using the characteristic equation of (4.6):

$$L_{grid}Bs^2 + (L_{grid}g_d + A)s + 1 = 0 \qquad (4.10)$$

Assuming $g_q = 0$ the value of g_d is given by (4.8) with its maximum and minimum values being 6.6 mΩ^{-1} and -6.6 mΩ^{-1}, respectively. These two values are obtained using the maximum and minimum current in the dq axes given by the system power flow. The following stability criterion is applied to (4.10): if the terms $a_1 > 0$ and $a_0 > 0$ for the polynomial $a(s) = s^2 + a_1 s + a_0$, then the transfer function is stable [6]. Consequently, the value of A is determined as follows:

$$\frac{L_{grid}g_d + A}{L_{grid}B} > 0 \qquad (4.11)$$

for (4.11) to be positive the following must be true: $B > 0$ and $A > -L_{grid}g_d$, using $g_d = -6.6$ mΩ^{-1}, A is selected to be 0.45 mHΩ^{-1}. To ensure that all of the poles of the transfer function are on the left side of the origin the discriminant of the quadratic equation for (4.10) has to be negative, which yields:

$$B > \frac{(L_{grid}g_d + A)^2}{4L_{grid}} \qquad (4.12)$$

With (4.12), the value of B is selected to be 4.5 $\mu H\Omega^{-2}$. Using the selected values for A and B, and the grid inductance of 28 mH, the root locus of the transfer function (4.6) is plotted in Fig. 4.10. The root locus plot shows that the poles are in the left hand side of the origin and the system is stable for the selected values.

Since g_d changes with the power flow, the root locus is also plotted in Fig. 4.11 for when g_d= 6.6 $m\Omega^{-1}$. This figure shows that the poles are closer to minus infinity when g_d is positive than when g_d is negative. By examining Fig. 4.10 and Fig. 4.11, it is concluded that the selected values of A and B make the transfer function stable for any of the given values of g_d.
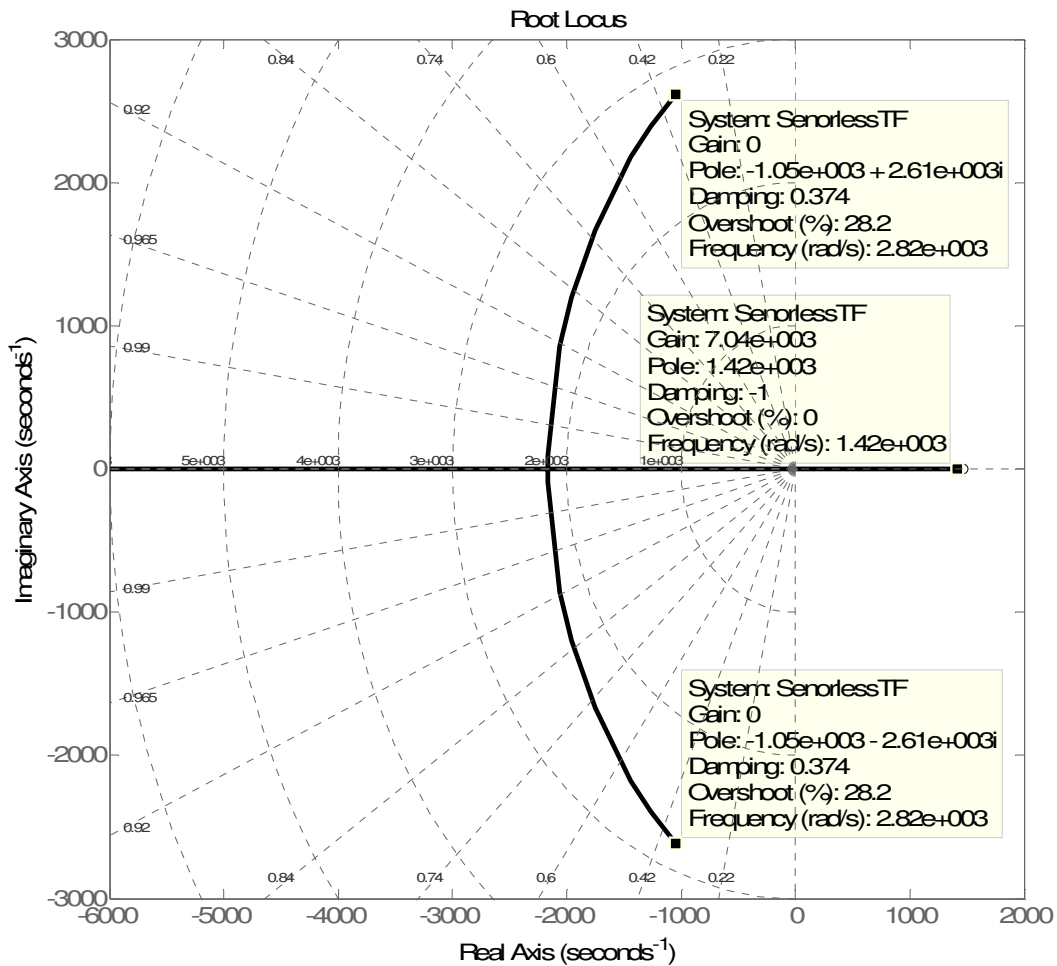
Fig. 4.10. Root Locus of transfer function (4.6) with g_d = -6.6 $m\Omega^{-1}$
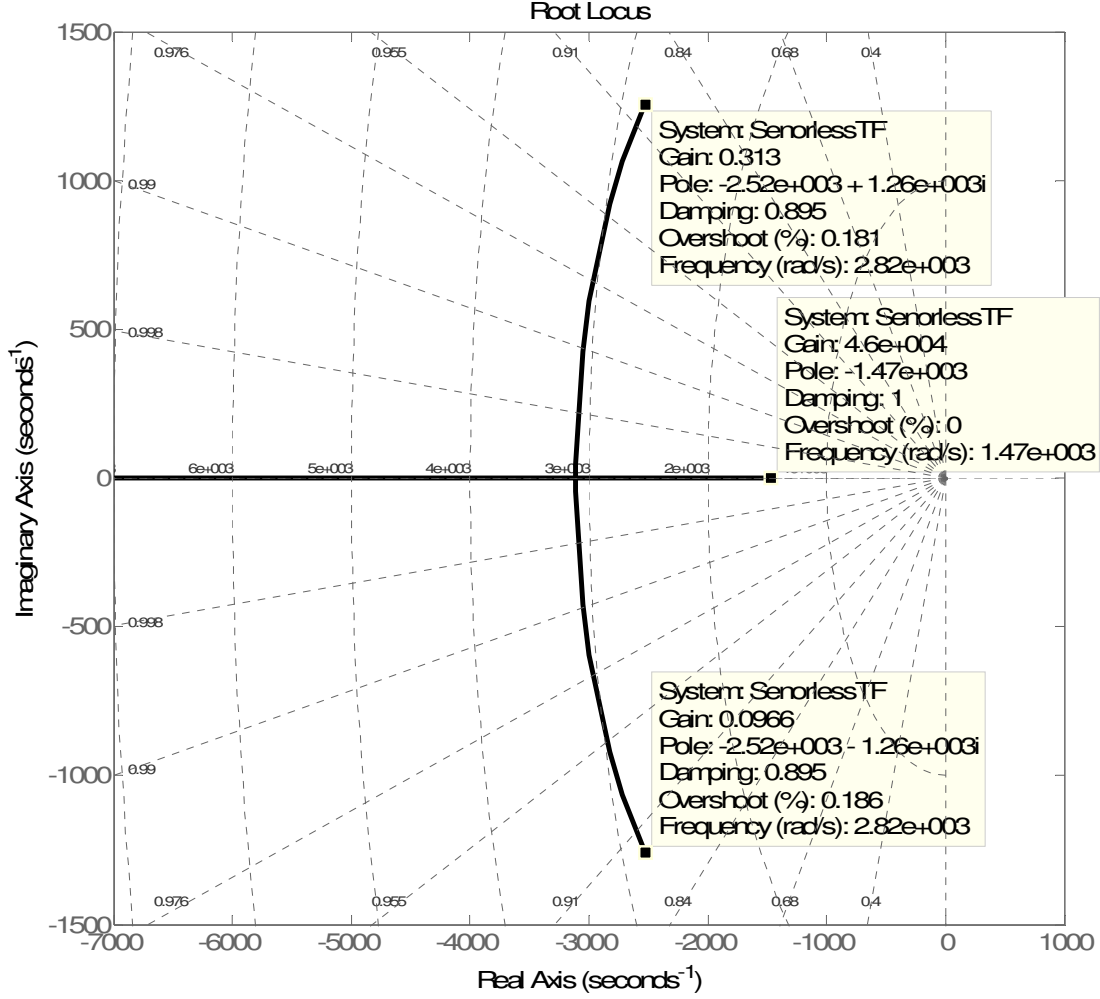
Fig. 4.11. Root Locus of transfer function (4.6) with $g_d = 6.6$ mΩ^{-1}

4.4.2. PI controller design

Equations (4.8) and (4.9) demonstrate that the grid currents can be controlled by controlling the conductance gains g_d and g_q; therefore, these conductances are selected to be the outputs of the PI controllers that control the active and reactive power flows.

In the case of the sensorless controller, the estimated active and reactive powers are given by [7]:

$$\hat{P} = \frac{3}{2}\left(\hat{v}_{d\_grid}\, i_{d\_grid} + \hat{v}_{q\_grid}\, i_{q\_grid}\right) \tag{4.13}$$

$$\hat{Q} = \frac{3}{2}\left(-\hat{v}_{d\_grid}\, i_{q\_grid} + \hat{v}_{q\_grid}\, i_{d\_grid}\right) \tag{4.14}$$

When selecting the values of the PI controllers, it is assumed that the values of $\hat{v}_{d\_grid}$ and $\hat{v}_{q\_grid}$ are constant, and equal to the grid voltages and the d axis is placed on Phase A. With this assumption, the system is linearized to the operating point $g_d= 6.6$ mΩ^{-1} using the Matlab/Simulink™ PID tuner tool. The gains obtained with this procedure are given in Table 4.3. Both controllers use the same gains, which will be used for the simulations to evaluate the performance of the sensorless control technique.

4.5   Performance Evaluation of the Sensorless Technique

The sensorless technique is evaluated considering a MMC-based inverter terminal with an ideal dc-source in the dc-link and the parameters given in Table 4.1. The Matlab/Simulink™ setup and models used for the simulations are given in Appendix B.2. The performance of the sensorless control technique is evaluated for the following cases:

- Comparison with the traditional control technique used in Chapter Three
- Ideal grid conditions
- Harmonic pollution of the grid voltages
- Grid-frequency changes
- Variations of the grid-voltage magnitudes

Table 4.3. Controller gains for the sensorless technique

	Active and reactive power controllers	
Parameter	k_p	k_i
Value	5.1×10^{-12} 1/(ΩVA)	1.5×10^{-8} 1/(ΩVAs)

The capabilities of keeping the stability of the system under non-ideal conditions and accurately estimating the grid voltages are evaluated with these five cases.

4.5.1. Comparison with the traditional control technique

The PS-SPWM waveforms of the voltage reference commands obtained using the traditional control technique shown in Chapter Three and those obtained with the sensorless technique are compared. These waveforms represent the ideal inverter voltage calculated by both control techniques. The voltage reference commands of the traditional control technique are at the top of Fig. 4.12, whereas the voltage reference commands of the sensorless technique are at the bottom. The THD of the voltage reference commands using sensors is 0.5%, with the sensorless technique is 0.74%. If the THD analysis is done at the output voltage of the inverter, both waveforms have the same THD of 2.68%. From these results, it is concluded that both techniques have a similar performance under ideal grid conditions; thus, further evaluation focuses only on the sensorless technique.

4.5.2. System performance under ideal grid conditions

In this evaluation, the grid is represented by ideal voltage sources and the initial angle of the grid is selected so that the d axis is on Phase A when θ is used. The phase to phase inverter voltages are illustrated at the top of Fig. 4.13, and the grid currents are at the bottom. At $t = 0.25$ s, the active power reference was changed from 400 MW (injecting) to -400 MW (absorbing), and at $t = 0.27$ s, the reactive power reference was changed from a 0.97 (lagging) to 0.97 (leading), verifying that the controller can control independently the active and reactive powers.
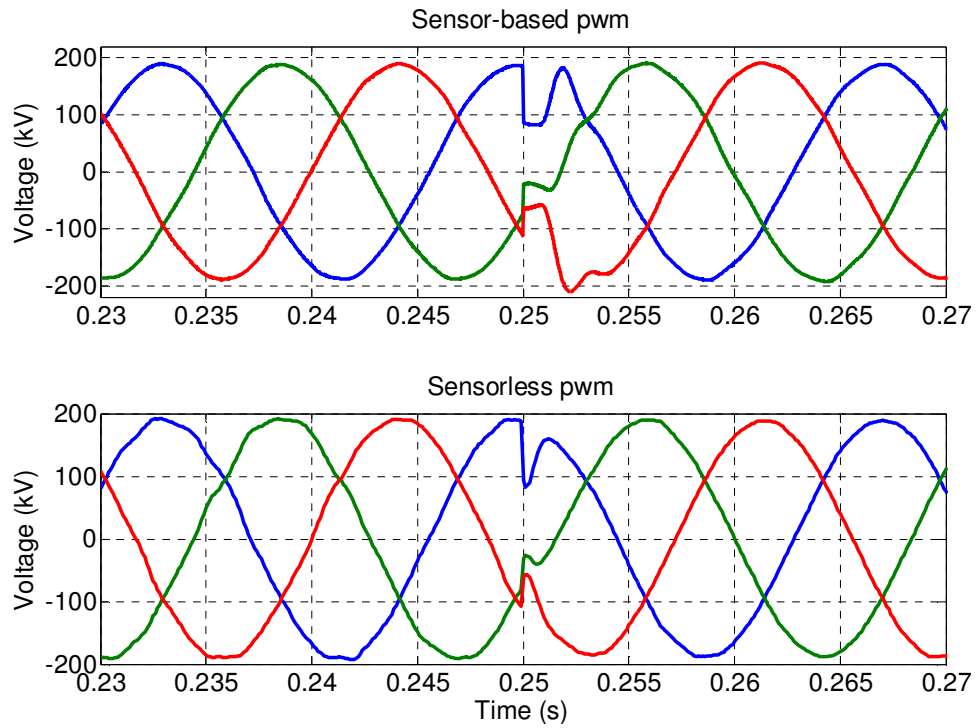
Fig. 4.12. Sensor-based voltage reference (top), and sensorless-based voltage reference
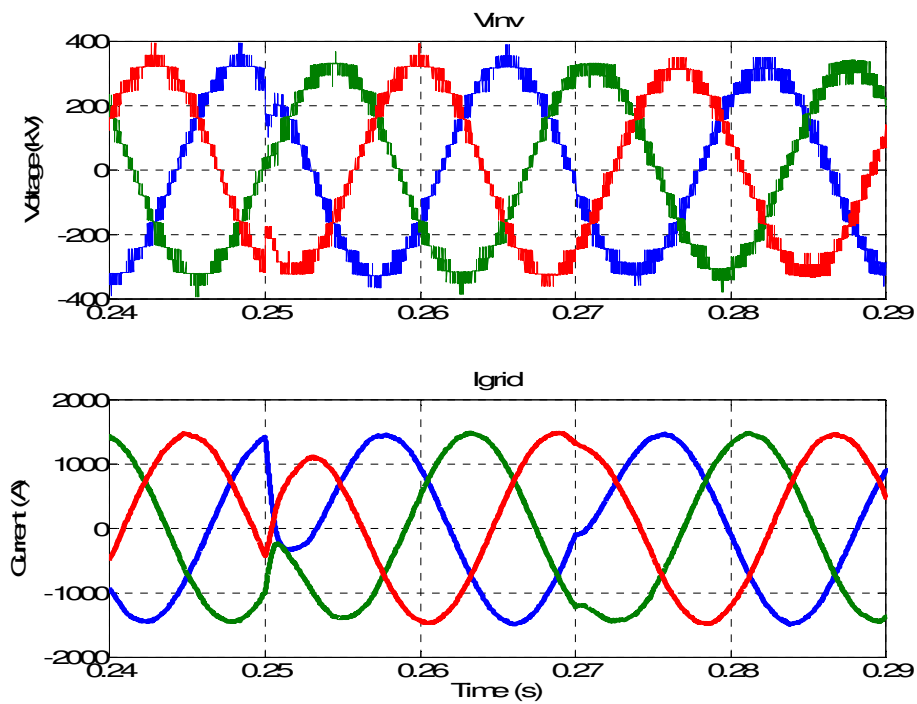
(bottom)

Fig. 4.13. Inverter output voltages (top) and currents (bottom)

There are no current or voltage overshoots for any of the reference changes. The estimated active and reactive powers of the controller are compared with the actual active and reactive powers as depicted in Fig. 4.14, with satisfactory results. In a real system the active and reactive powers will be measured, therefore, the term "measured" will be used thought the rest of the chapter to refer to the actual values. There are no overshoots for any of the powers, and the settling times for the active and reactive powers are both 7 ms. This test has verified the capability of the controller to control both active and reactive powers independently; thus, for the subsequent cases, only the active power will be changed and the reactive power will be fixed at -50 MVAR.
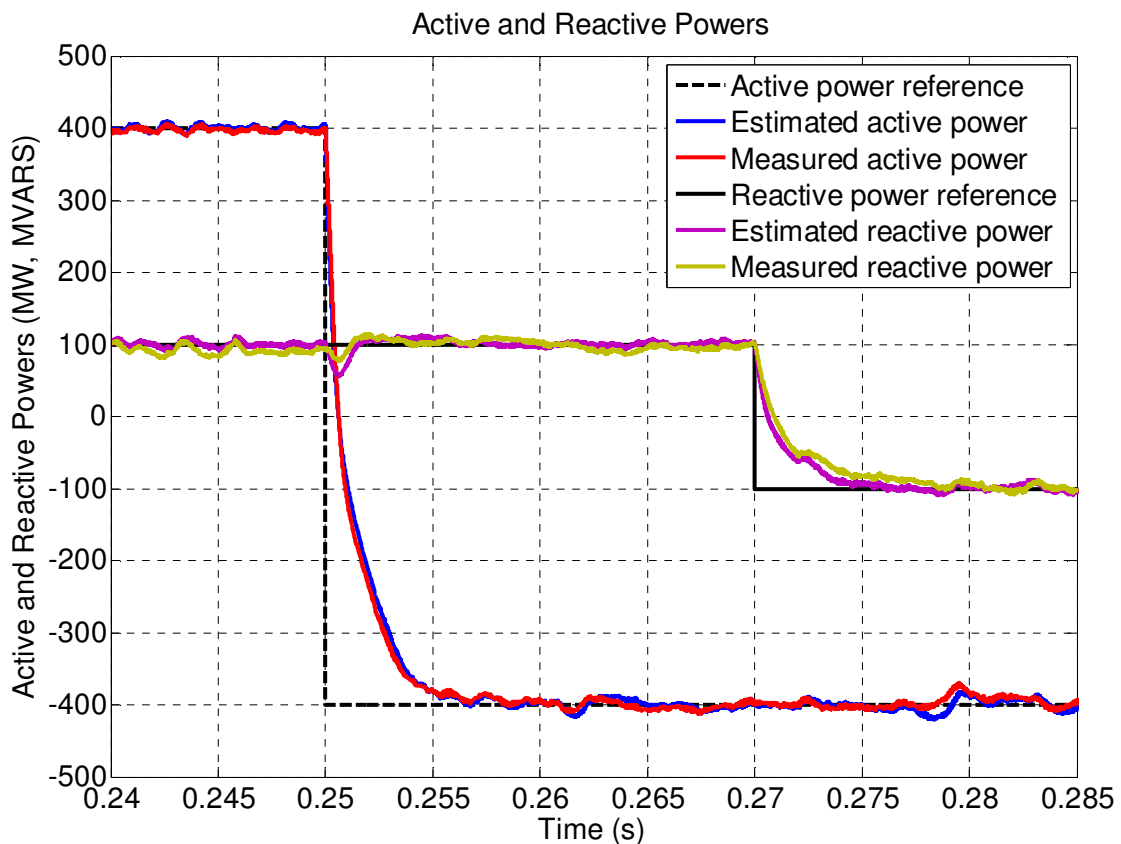

Fig. 4.14. Active and reactive powers injected into the grid under ideal grid conditions

4.5.3. *System perormance under harmonic pollution of the grid voltages*

The total THD limit for a grid with $V_n > 161$ kV is 1.5 % according to the IEEE Standard 519-1992. The grid voltages are polluted beyond the limits of the IEEE Standard 519-1992 from t = 0.22 s until the end of the simulation, resulting in a total THD of 3.2% with a 5th harmonic of 2.5%, and a 7th harmonic of 2%.

The current THD before harmonic voltage pollutions is 0.88%, which increases to 2.73% after applying the disturbances. The total current THD after the grid voltages are polluted is still within the IEEE Standard 519-1992 limit for a grid with a short-circuit ratio greater than or equal to 50. The grid (top) and inverter (middle) voltages, and grid currents (bottom) are presented in Fig. 4.15. At t = 0.25 s, the active power reference changes from 250 MW to 500 MW, as illustrated in Fig. 4.16. The grid harmonic pollution of the voltages are polluted in the abc frame translates on the d-q frame as 6th harmonic pollution, as illustrated in Fig. 4.16. This harmonic pollution causes an overshoot of 17.2% on the estimated active power, but no overshoot on the measured active power.

The ripple on the measured active power is ±6% and on the estimated active power is ±10%. Even with the estimated voltage ripple produced by the harmonic pollution of the grid voltages, the controller is able to keep the system stable. Nevertheless, a higher harmonic pollution on the grid voltages might cause instability issues for the system. Harmonic rejection techniques such as adding a second-order generalized integrator should be explored [8]-[9].
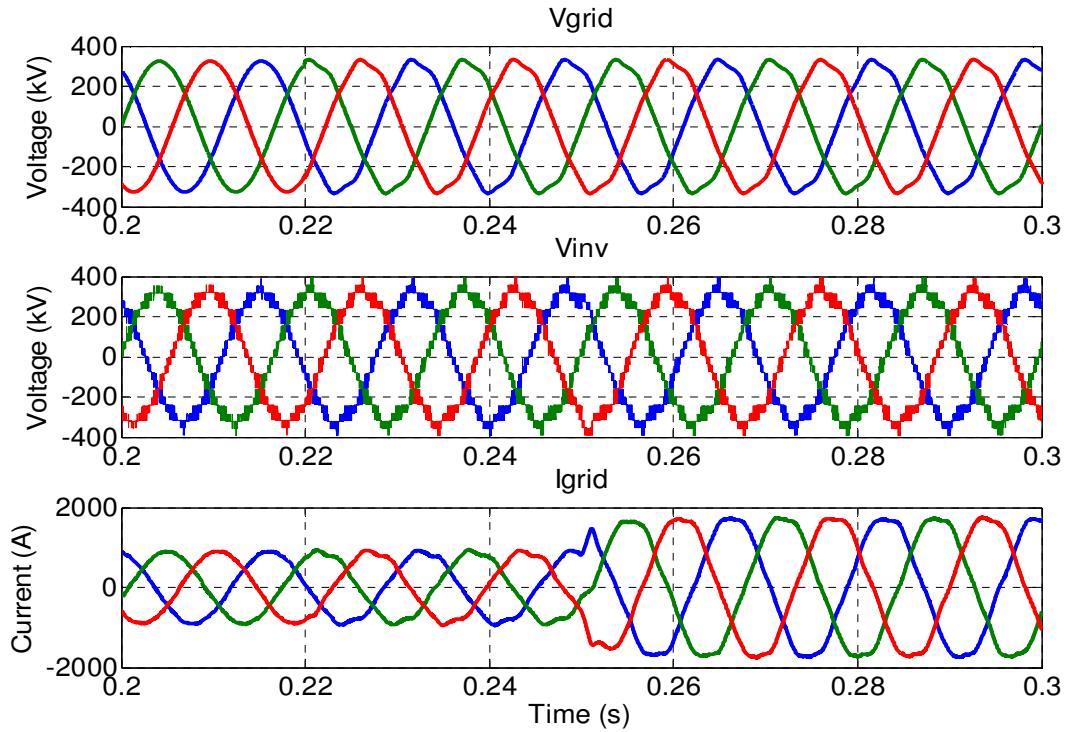
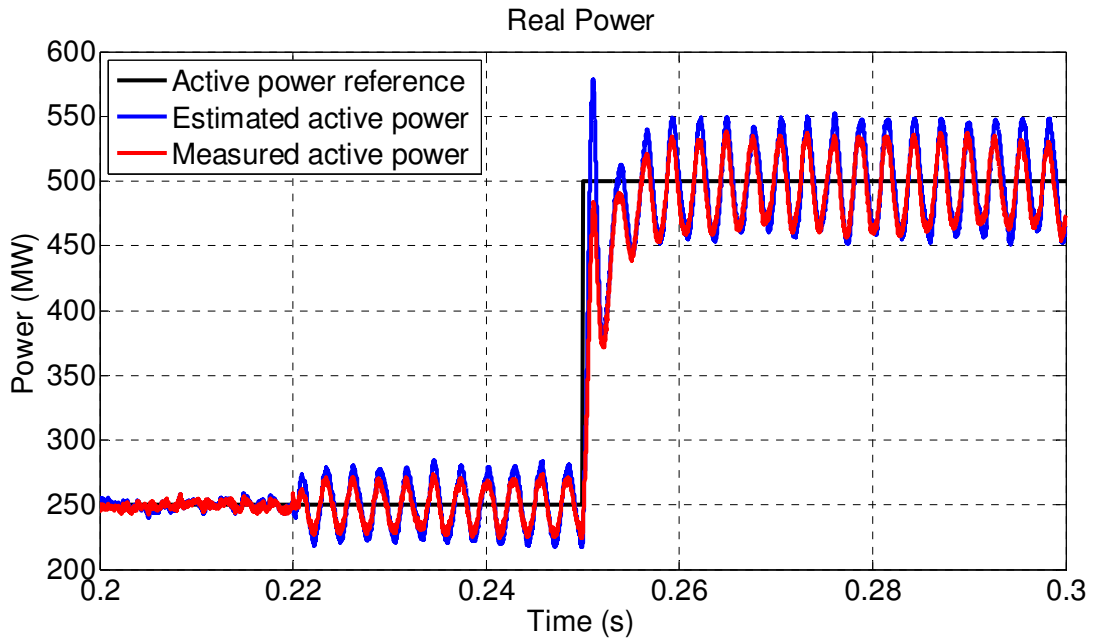**Fig. 4.15. Grid (top) and inverter (middle) voltages and grid currents (bottom) under grid-voltage harmonic pollution**

Fig. 4.16. Reference (black), estimated (blue) and measured (red) active powers under grid-voltage harmonic pollution

4.5.4. *System performance under grid frequency changes*

Initially the grid frequency was reduced by 1 Hz from t = 0.22 s to t = 0.28 s, and the active power reference was increased from 250 MW to 500 MW at t = 0.25 s. The inverter voltages and grid currents are at the top and bottom of Fig. 4.17, respectively. There are no current or voltage overshoots when the active power reference is changed, nor for any of the grid-voltage frequency changes. There is an overshoot of 1.4% on the estimated power for the reference change, nevertheless; this overshoot is not present in the measured active power, as illustrated by the top graph of Fig. 4.18.

The estimated and measured grid voltage magnitudes are presented at the bottom of Fig. 4.18. As expected, the measured grid voltages remain constant despite frequency changes, and estimated grid voltages change. This variation on the estimated grid voltages is produced due to grid-frequency dropping; this causes the estimated angle θ to rotate faster than the grid angle. The difference in the angular velocity of both angles causes the d-axis to start leading Phase A, which causes $\hat{v}_{q\_grid}$ to start decreasing.

For the second part of the evaluation, the grid frequency is increased by 1 Hz from t = 0.22 s to t = 0.28 s, and the active power reference is increased from 250 MW to 500 MW at t = 0.25 s. The inverter voltages and grid currents are at the top and bottom of Fig. 4.19, respectively. Once more, the controller is able to keep the system stability without any voltage or current overshoots for neither when the grid frequency nor the active power reference are changed. There is no overshoot on the estimated active power nor on the measured active power for the reference change, as illustrated by the top graph of Fig. 4.20.
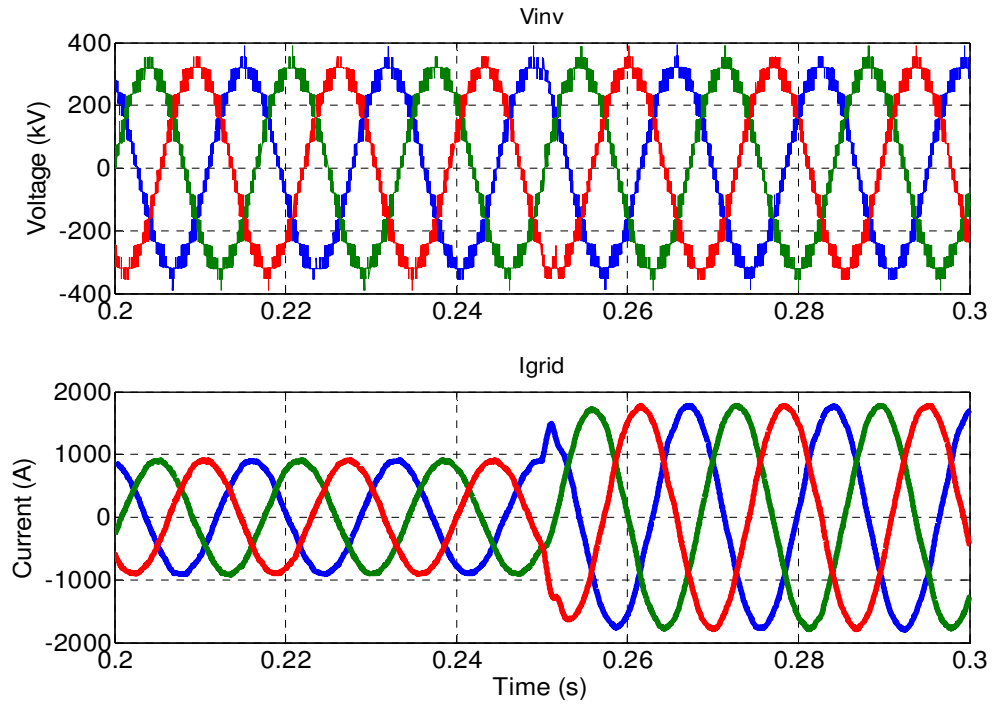
Fig. 4.17. Inverter voltages (top) and grid currents (bottom) with a grid frequency step
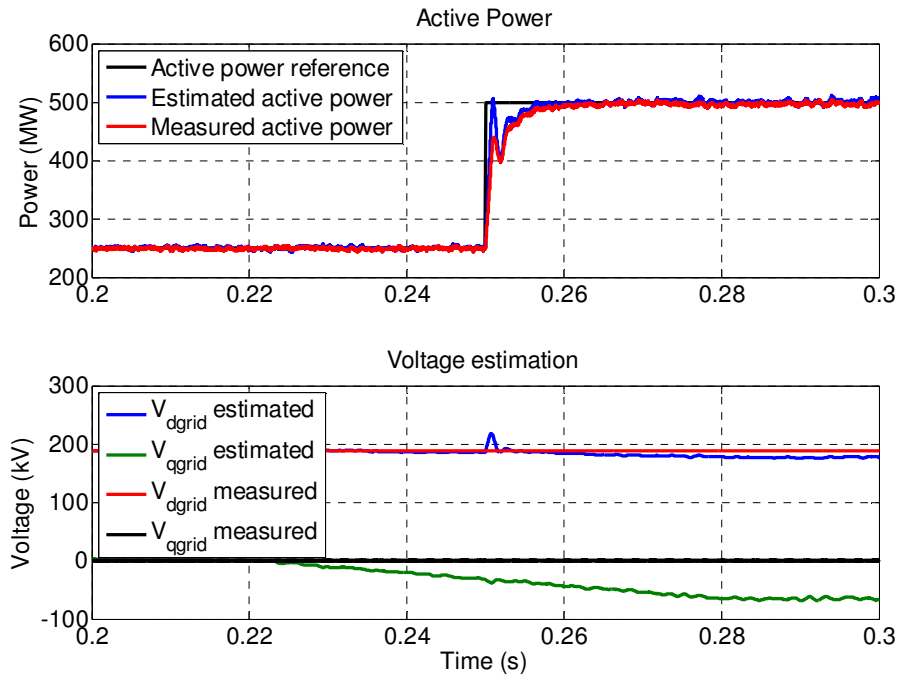
of -1.0 Hz

Fig. 4.18. Active power (top) and grid estimated voltages (bottom) with a grid frequency
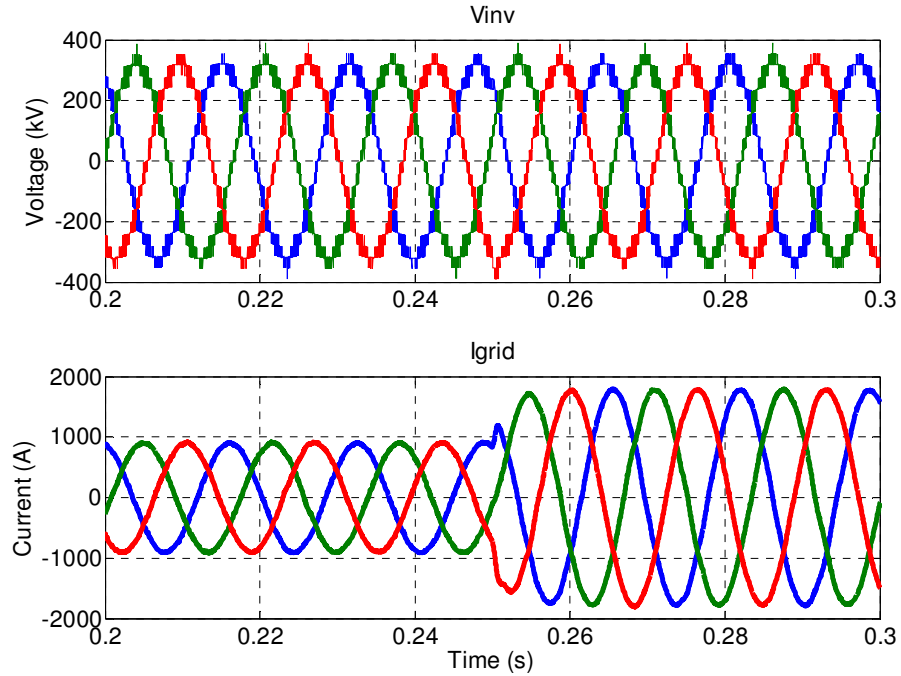
step of -1.0 Hz

Fig. 4.19. Inverter voltages (top) and grid currents (bottom) with a grid frequency step
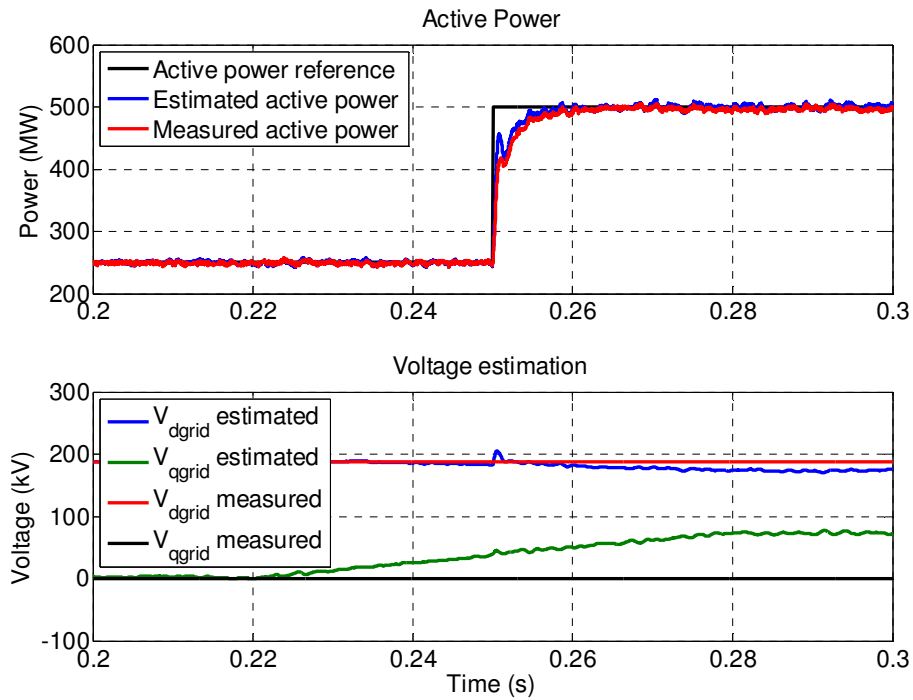
of 1.0 Hz

Fig. 4.20. Active power (top) and grid estimated voltages (bottom) with a grid frequency

step of 1.0 Hz

Similar to when the grid frequency is reduced, the estimated grid voltages differ from the measured grid voltages when the frequency is increased; this is illustrated at the bottom of Fig. 4.20. When the grid frequency increases, the difference between the grid angle and the estimated angle θ will cause the d axis to start lagging Phase A; this causes $\hat{v}_{q\_grid}$ to start increasing.

4.5.5. *System performance under variations of the grid voltage magnitudes*

The grid voltages are increased by 6% at t = 0.22 s, and then stepped back up to their nominal value at t = 0.28 s for the first part of this test. The inverter voltages and grid currents are illustrated at the top and bottom of Fig. 4.21, respectively. There is no significant change on the inverter voltages once the grid voltages are increased. In contrast, the controller reduces the current injected into the grid to keep the active power at its commanded reference. There is no current overshoot when the active power reference is increased from 250 MW to 500 MW at t = 0.25 s. At t = 0.28 s, the controller senses the grid voltage stepping down to its nominal value, and it increases the injected current in order to keep the active power constant.

The estimated active power (blue) and the measured active power (red) are presented at the top of Fig. 4.22. The controller keeps accurate track of the active power when the grid-voltage is increased and when the grid voltage changes back to its nominal value. The overshoot seen in the estimated active power is not present in the measured active power. The estimated grid voltage (blue) and the measured grid voltage (red) on the d axis are shown at the bottom of Fig. 4.22. The overshoot on the estimated grid voltage is caused by the active power reference change. This overshoot causes the estimated active power overshoot; however, this overshoot is not present in the estimated or measured active powers, and the grid injected currents. The sensorless technique keeps precise track of the grid-voltage changes while keeping track of the active power reference command.
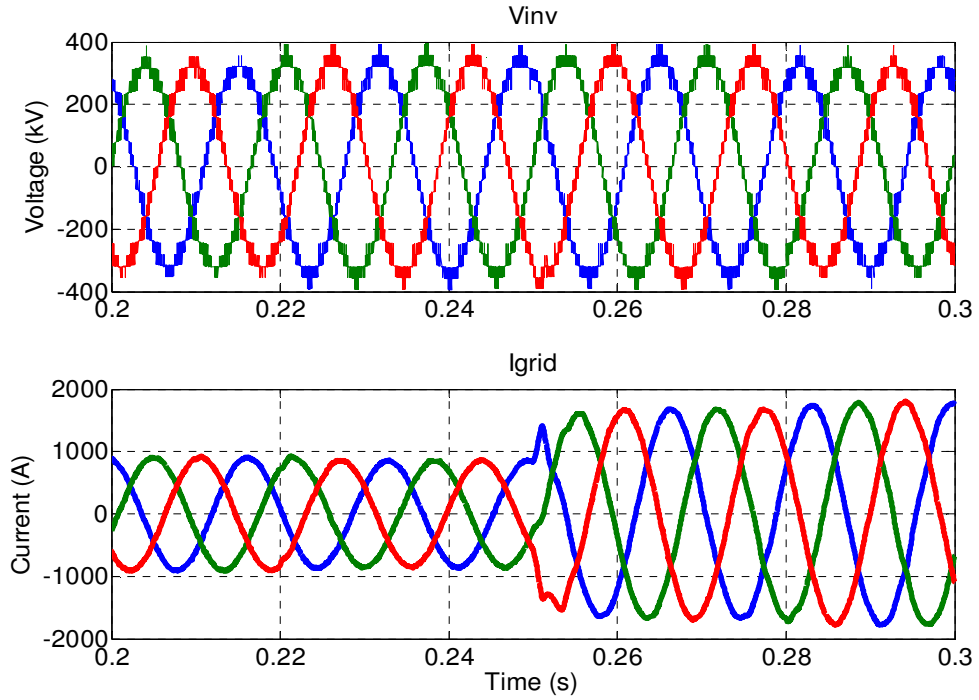
Fig. 4.21. Inverter voltages (top) and grid currents (bottom) with a grid-voltage increase

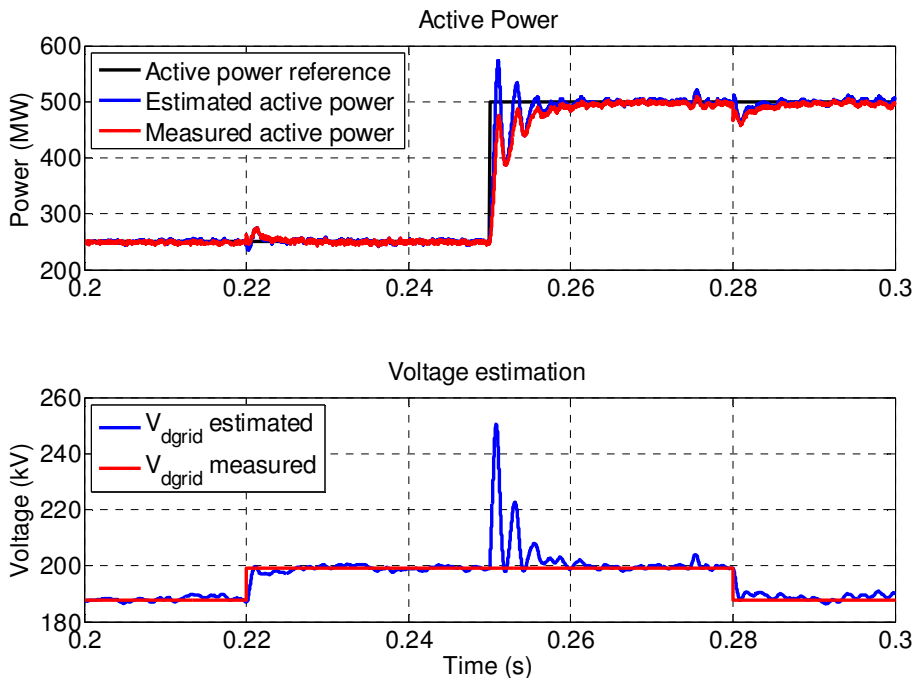**of 6%**

Fig. 4.22. Active power (top) and grid estimated voltages (bottom) with a grid-voltage

increase of 6%

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The grid voltages are decreased by 6% at t = 0.22 s, and then stepped back up to their nominal value at t= 0.28 s for the second part of this case. The inverter voltages and grid currents are illustrated at the top and bottom of Fig. 4.23, respectively. There is no significant change on the inverter voltages once the grid voltages are decreased. In contrast, the controller increases the current inject into the grid to keep the active power at its commanded reference. There is no current overshoot when the active power reference is increased from 250 MW to 500 MW at t = 0.25 s. At t = 0.28 s, the controller senses the grid voltage stepping up to its nominal value, and it decreases the injected current in order to keep the active power constant.

The estimated active power (blue) and the measured active power (red) are presented at the top of Fig. 4.24. The controller keeps accurate track of the active power when the grid voltage is decreased and when the grid voltage changes back to its nominal value. There is no overshoot in
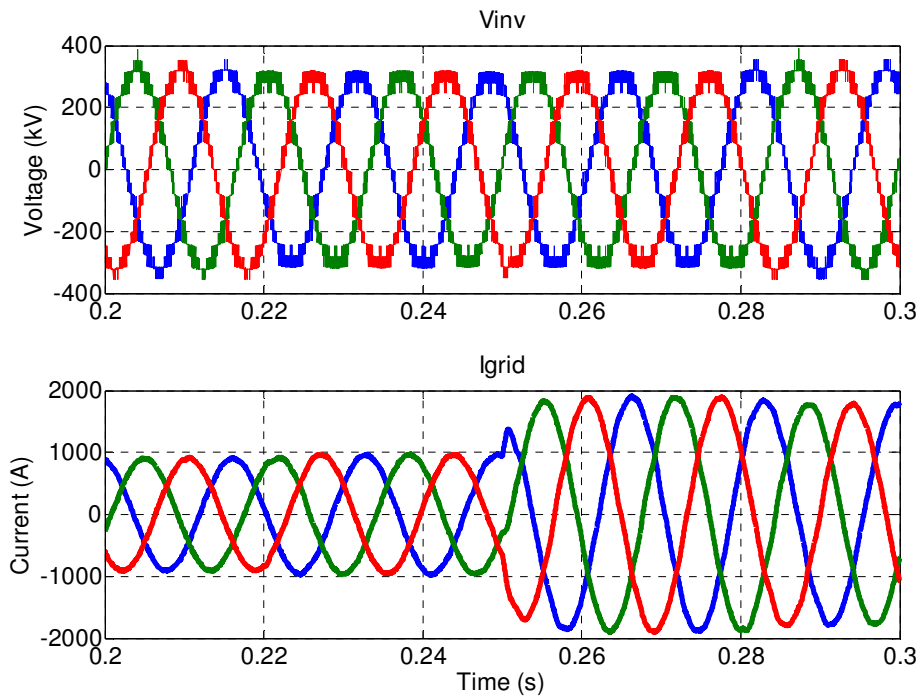

Fig. 4.23. Inverter voltages (top) and grid currents (bottom) with a grid-voltage decrease of 6%
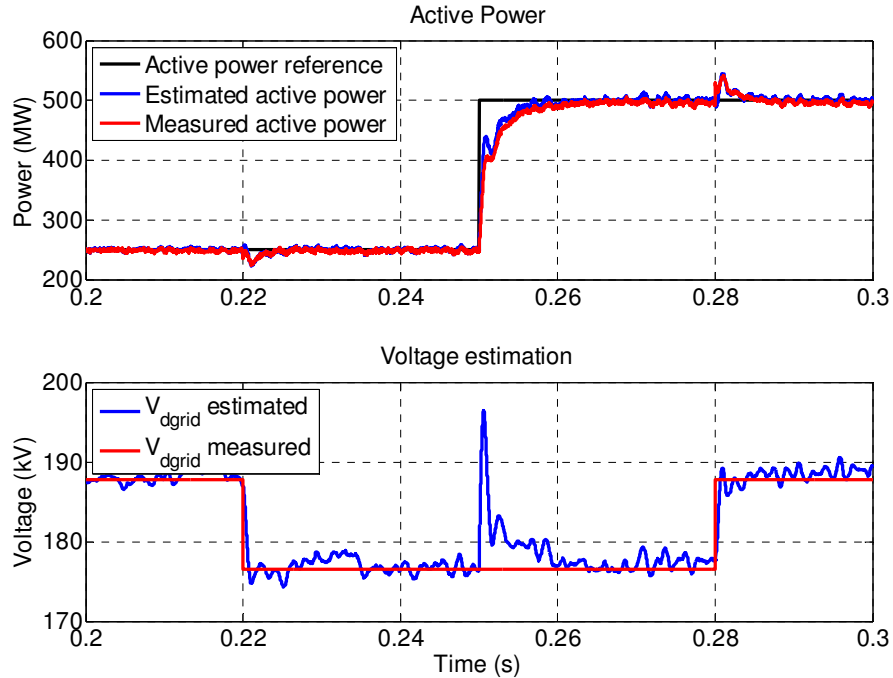
Fig. 4.24. Active power (top) and grid estimated voltages (bottom) with a grid-voltage decrease of 6%

the estimated or measured active powers. The estimated grid voltage (blue) and the measured grid voltage (red) on the d axis are shown at the bottom of Fig. 4.24. The overshoot on the estimated grid voltage is caused by the active power reference change; however, this overshoot is not present in the estimated or measured active powers, and the grid injected currents. The sensorless technique keeps precise track of the grid-voltage changes while keeping track of the active power reference command. An overshoot of 9% on the measured and estimated active powers is caused by the grid voltage stepping back to its nominal value.

4.6   Conclusions

The procedure to calculate the outer controller's gains has been validated with Matlab/Simulink™ simulations. The active and reactive power flows were controlled successfully with the various selected controller gains. A bandwidth of 400 Hz for the current

controller and 40 Hz for the dc-voltage controller proved to be suitable for the selected case study. The simulations demonstrated that not controlling the circulating current of the MMC leads to instability issues, potentially damaging the SM switching devices, and increasing losses in the system. The controllers designed in Chapter Three provided a suitable method to control the circulating current on the MMC.

The procedure to select the parameters of the transfer function of the sensorless technique was also validated with simulations. The selected values for A and B plus the selected PI controller gains kept the system stable for all the considered cases. There were no overshoots with the selected gains for ideal grid conditions; however, there was a 9% overshoot on the estimated active power when the grid voltage was suddenly increased in magnitude.

The sensorless control technique implemented in the MMC inverter terminal also proved to be robust for non-ideal grid conditions, and for detecting precisely changes on the grid voltage and frequency; however, when the grid-voltages were polluted with harmonics, the sensorless technique showed a ±10% ripple on the estimated active power.

The reliability of an HVdc terminal could be increased if the sensorless technique is used as a backup for the traditional control techniques using sensors.

Chapter Five will analyze the impacts that a 15 kV-Silicon-Carbide IGBT may have on an MMC-based HVdc terminal.

References

[1]   A. Escobar-Mejia, D. Guzman, J.C. Balda and C. Busada, "New Control Technique for Sensor-less Grid Synchronization of Modular Multilevel Converters for HVDC Systems," *Proceedings of the IEEE Energy Conversion Congress & Exposition*, 2013.

[2]   Inter-American Development Bank. *Colombia-Panama Interconnection* [Online]
        Available:
        http://www.iadb.org/en/projects/project-description-title,1303.html?id=rs%2Dt1241
        [Accessed: Jan.31, 2013].

[3]   B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC
        technologies for power transmission," in *Transmission and Distribution Conference and
        Exposition*, 2008, IEEE/PES, 2008, pp. 1–16.

[4]   A. Antonopoulos, L. Angquist, H-P. Nee, "On dynamics and voltage control of the
        Modular Multilevel Converter," *Proceedings of 13th European Conference on Power
        Electronics and Applications*, EPE '09. pp. 1-10 Sept. 2009

[5]   P.C. Krause, "Reference-Frame Theory," in *Analysis of Electric Machinery*, 1st ed.
        McGraw Hill, 1986, pp. 133-157.

[6]   L. Qiu, K. Zhou, "Stability and Stabilization," in *Introduction to Feedback Control*, 1st ed.
        Upper Saddle River, NJ: Prentice-Hall, pp. 81.

[7]   A. Yazdani and R. Iravani, "Space Phasors and Two-Dimensional Frames" in *Voltage-
        Sourced Converters in Power Systems - Modeling, Control and Applications*, 1st ed.
        Hoboken, NJ, John Wiley, pp. 105.

[8]   P. Rodriguez, A. Luna, I. Candela, R. Teodorescu, F. Blaabjerg, "Grid synchronization of
        power converters using multiple second order generalized integrators," *Proceedings of
        Industrial Electronics Conference.*, pp. 755-760, 10-13 Nov. 2008.

[9]   M. Liserre, R. Teodorescu, F. Blaabjerg, "Multiple harmonics control for three-phase grid
        converter systems with the use of PI-RES current controller in a rotating frame," in IEEE
        Transactions on Power Electronics, vol. 21, no. 3, pp. 836–841, May, 2006.

MATLAB/SIMULINK™ SIMULATION SETUP FOR SENSOR-BASED CONTROL

The Matlab/Simulink ™ models used for the simulations in Chapter Four are presented in this appendix.
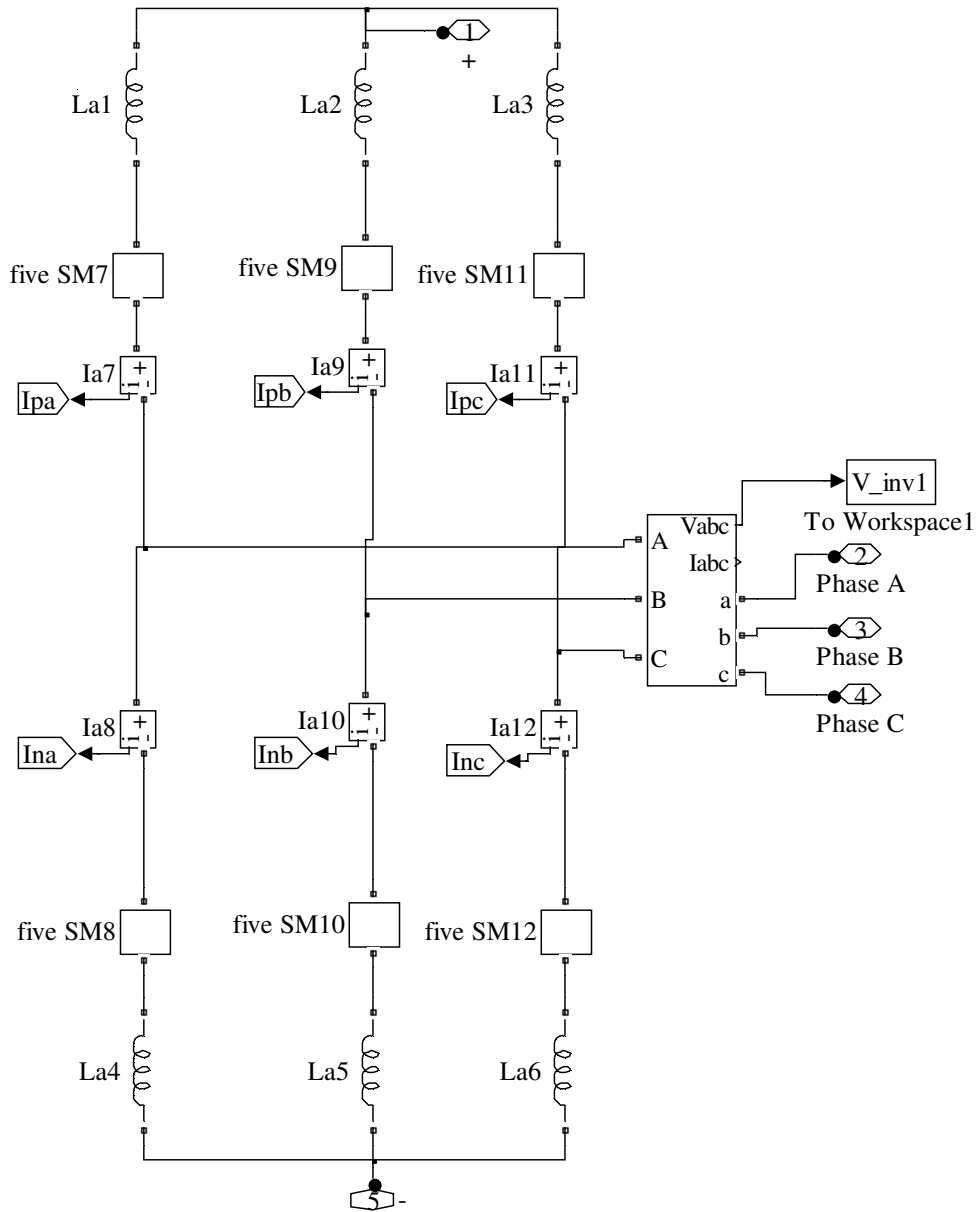

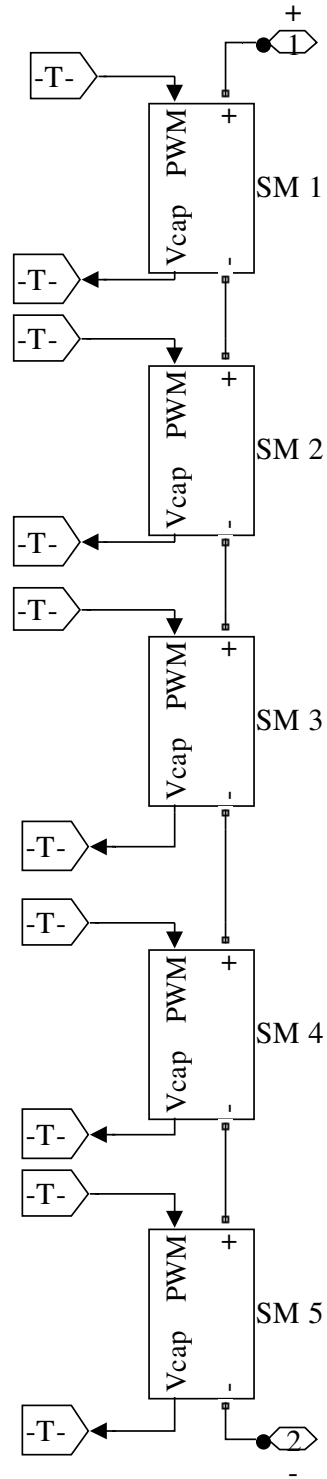**Fig. B.1. Three-phase MMC model used for Terminal 1 and Terminal 2**
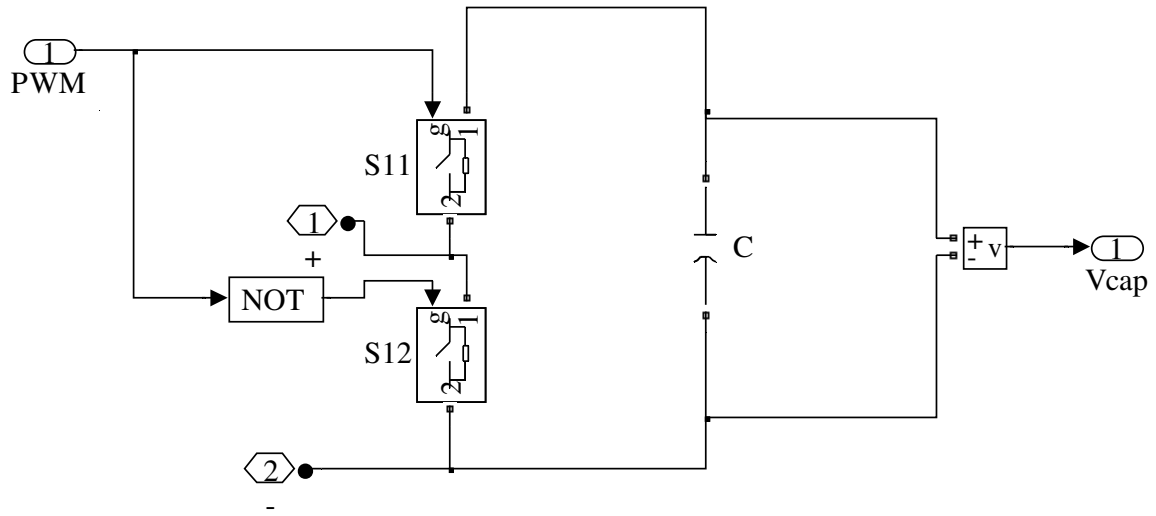
Fig. B.2. Connection of the five SM within the MMC arm
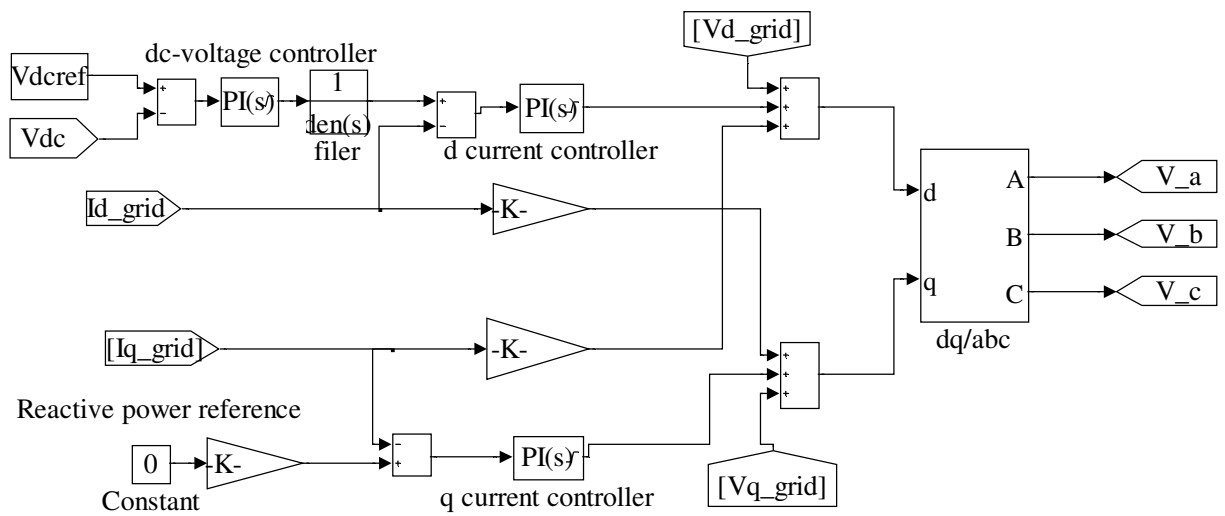
Fig. B.3. SM representation in Matlab/Simulink™
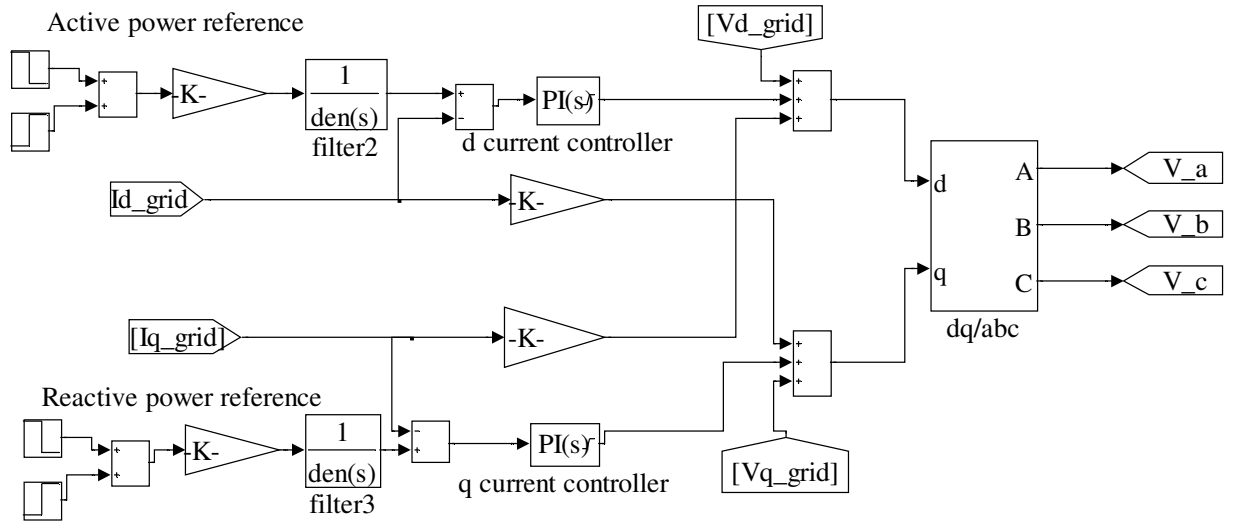

Fig. B.4. Controller for Terminal 1
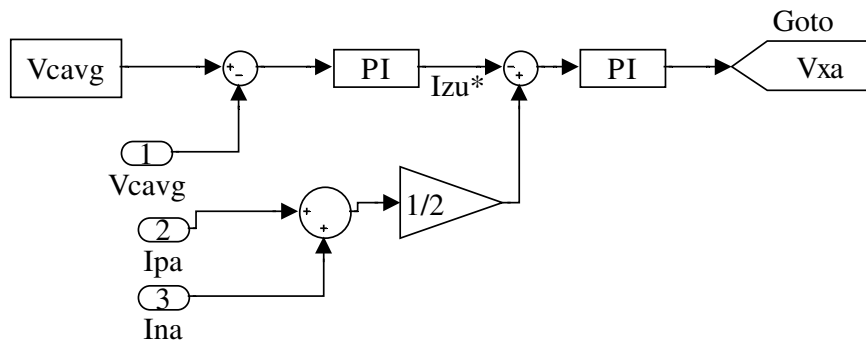
Fig. B.5. Controller for Terminal 2

Fig. B.6. Capacitor average voltage control in Matlab/Simulink™

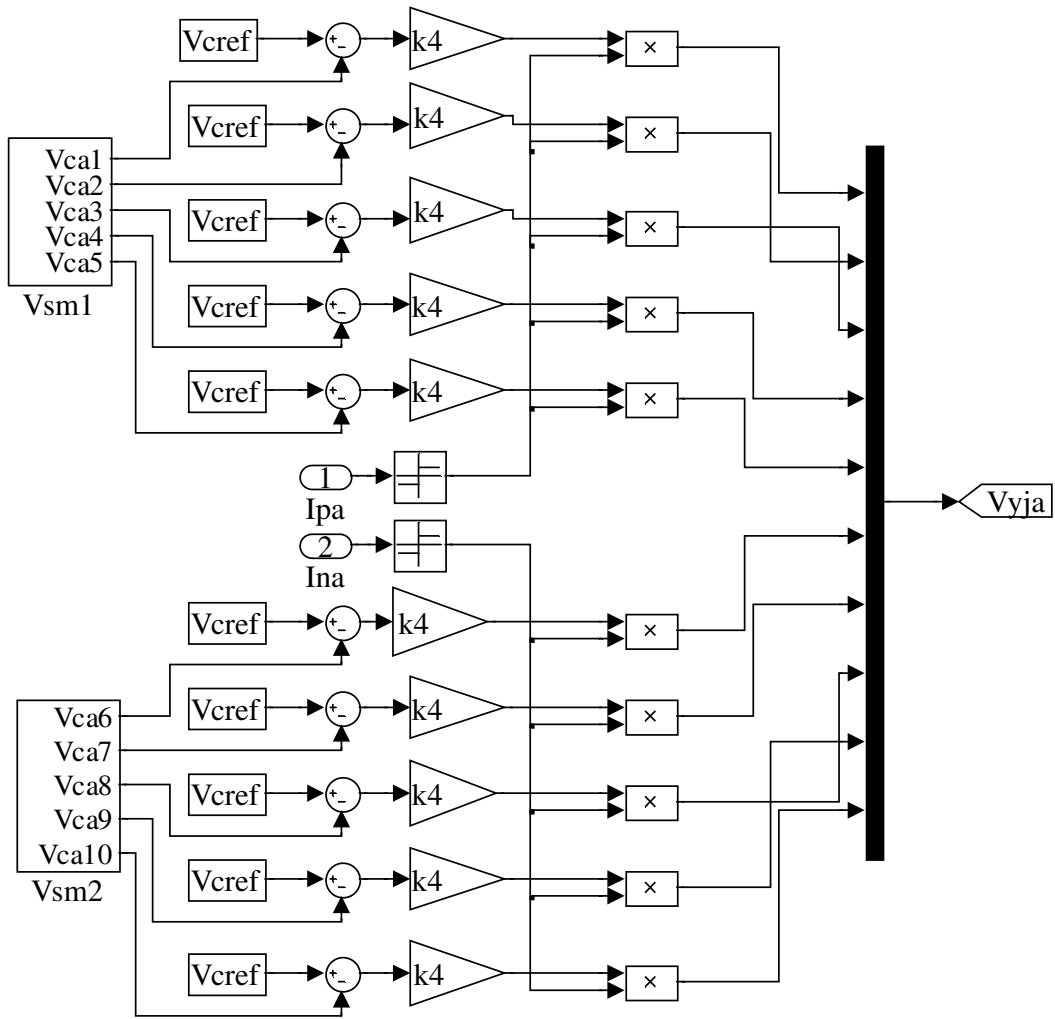**Fig. B.7. Balancing control of instantaneous capacitor voltages in Matlab/Simulink™**
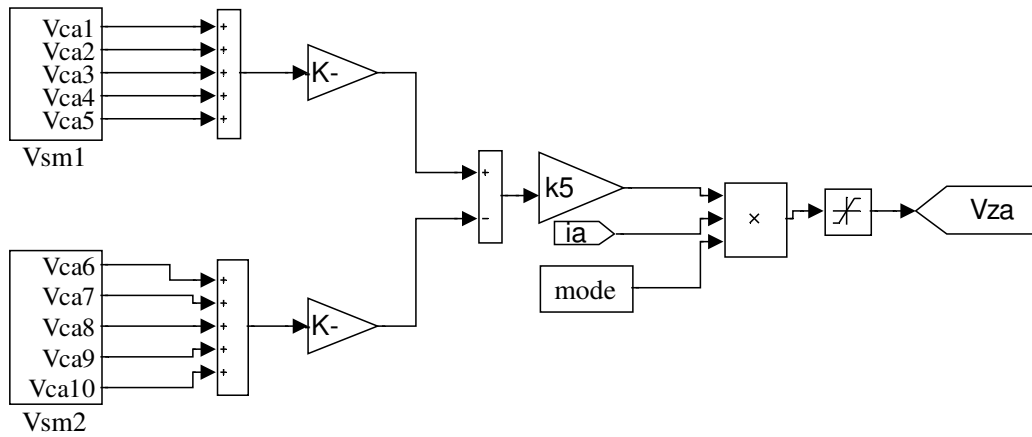
Fig. B.8. Arm-balancing voltage control in Matlab/Simulink™

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Fig. B.9. Switching signal generation in Matlab/Simulink™

MATLAB/SIMULINK™ SIMULATION SETUP FOR SENSROLESS CONTROL

The Matlab/Simulink models used for evaluating the sensorless control technique are depicted in this appendix.

Fig. B.10. MMC terminal model used for evaluating the sensorless control technique

Fig. B.11. Matlab/Simulink™ implementation of the sensorless control technique

CHAPTER FIVE

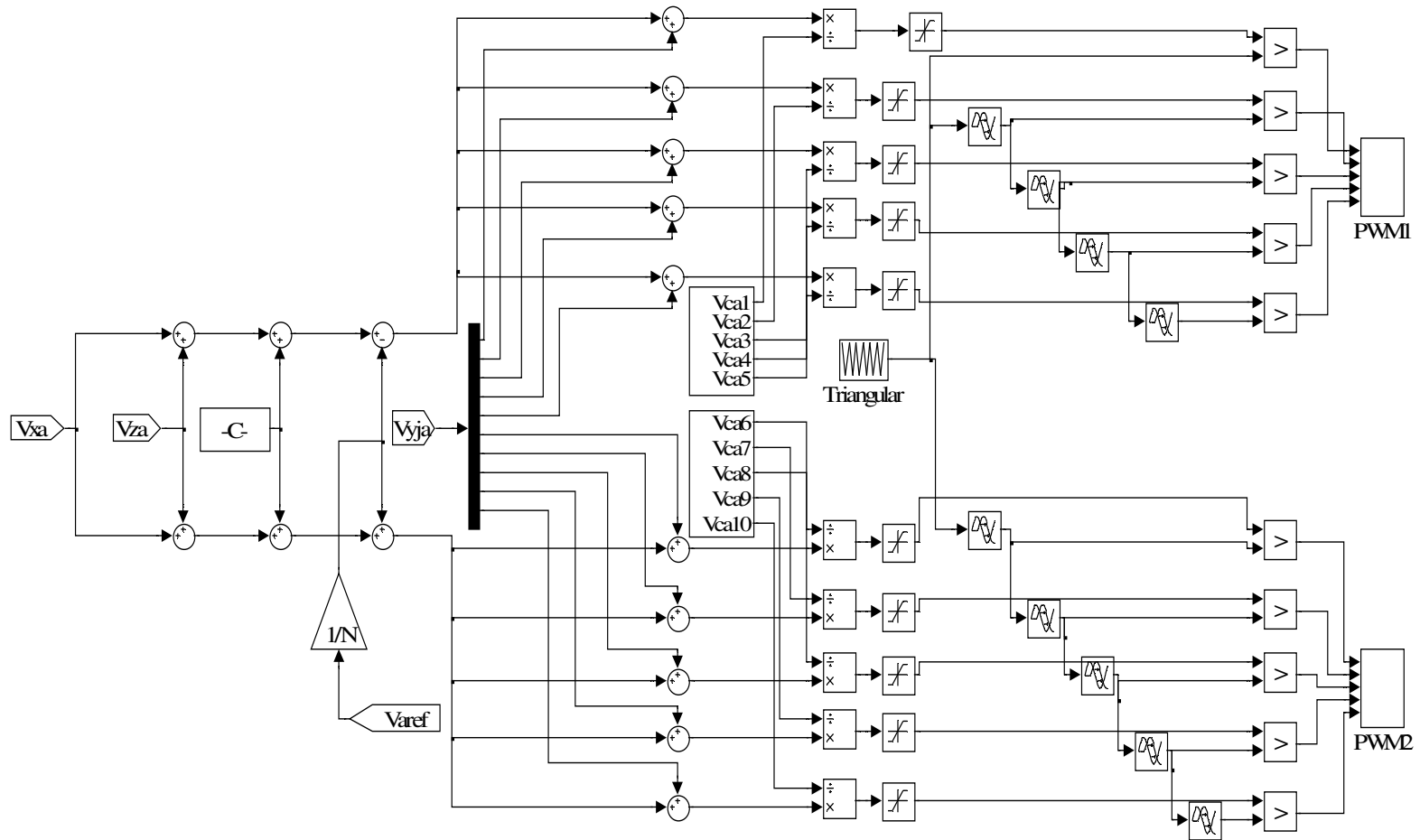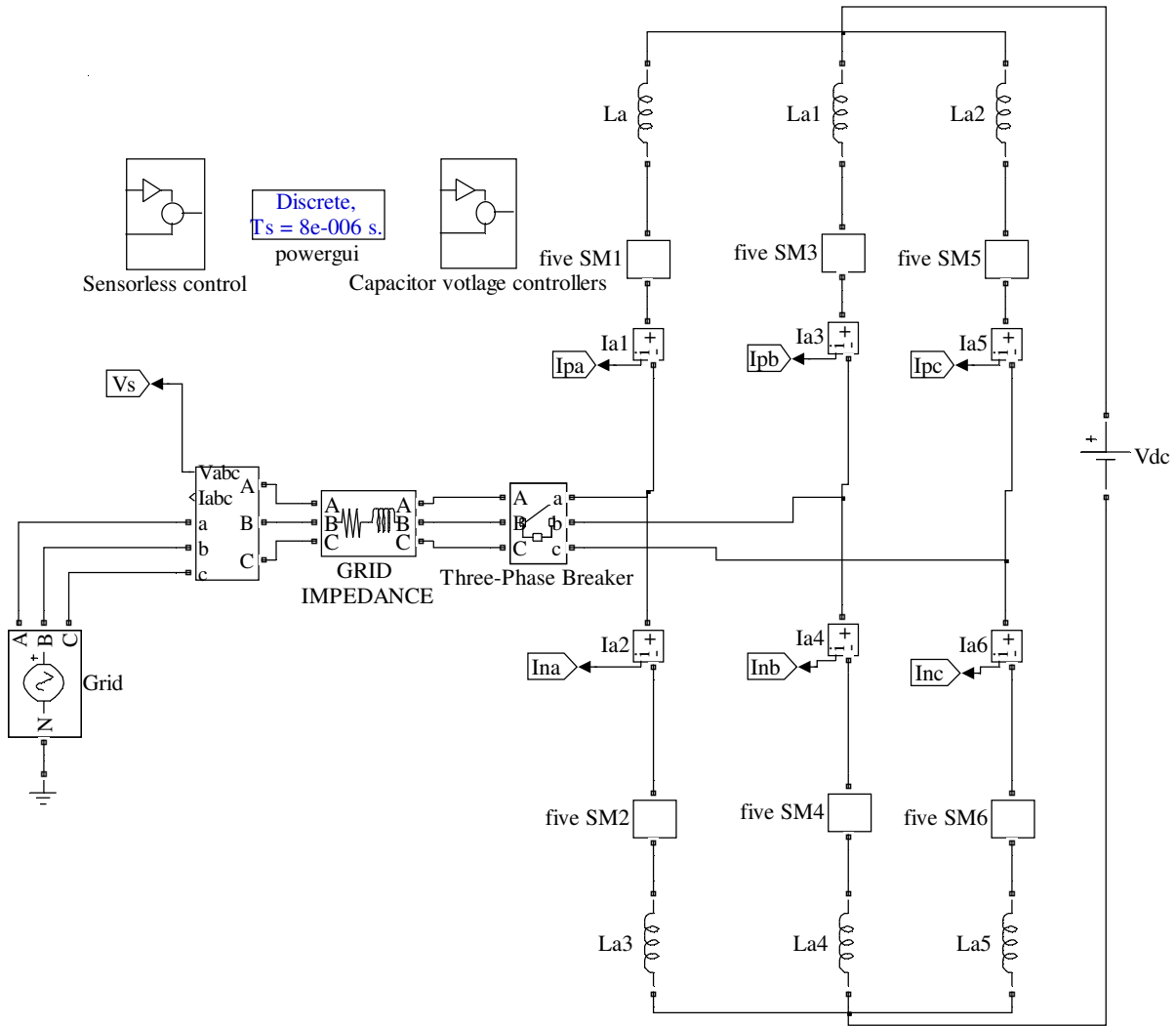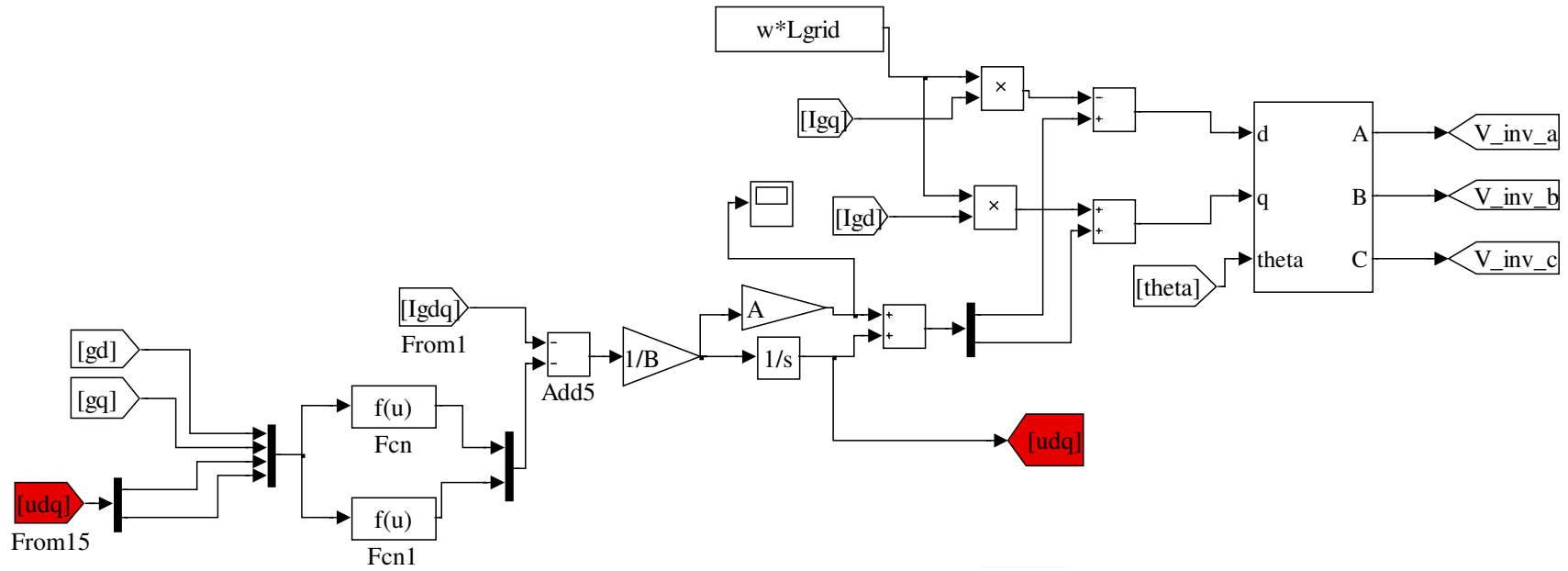# THE IMPACT OF HIGH-VOLTAGE AND FAST-SWITCHING DEVICES ON MODULAR MULTILEVEL CONVERTERS

Abstract

US government is funding the development of high-voltage and fast-switching power semiconductor devices based on silicon carbide (SiC) for applications in medium- and high-voltage power systems. The availability of these devices should reduce the complexities of grid-connected advanced power electronic systems like medium-voltage voltage-source converters (VSC) for HVDC terminals, power electronic interfaces for distributed generation, or high-power motor drives. However, fast-switching devices may augment the adverse effects of parasitic inductances that are inherent in any power converter layout. Hence, this paper presents a theoretical analysis of the impacts that the developing 15-kV SiC insulated gate bipolar transistors (IGBTs) have on modular multilevel converters (MMCs) in terms of the sub-module (SM) numbers, the SM capacitance, the effects of parasitic inductances on overvoltages, capacitor and IGBT module volumes, and THD. An 800 MW ±320 kV VSC-HVDC terminal is selected as a case study to illustrate the potential advantages of such a high-voltage and fast-switching semiconductor device.

5.1   Introduction

The MMC proposed in [1] and illustrated in Fig. 5.1 is currently used in VSC-HVDC projects around the world [2], since it presents several advantages over the LCC topologies, in particular:

- Higher efficiencies due to fundamental-frequency switching: efficiencies over 99.3% and 99.8% are claimed in [3] and [4], respectively.

- No dc-link capacitor, since the dc-link voltage can be controlled using the MMC SMs.

- The internal arm currents have a continuous flow and can be controlled by the MMC control algorithm eliminating voltage overshoots caused by parasitic inductances in the arm.
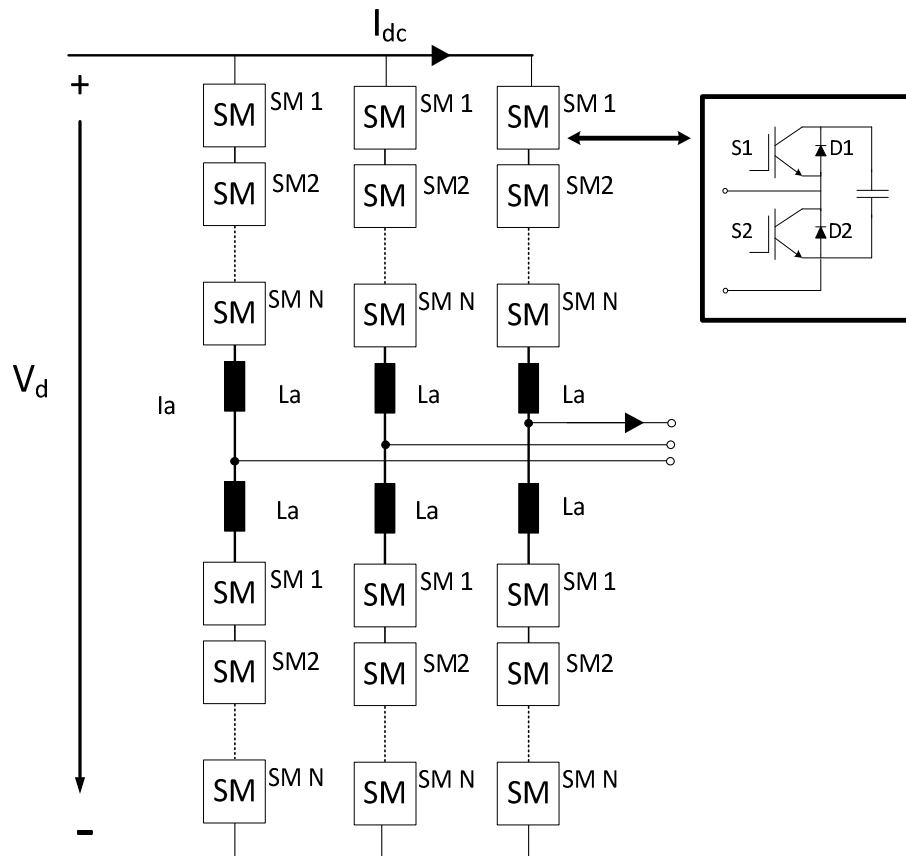

Fig. 5.1. Modular multilevel converter topology

As shown in Fig. 5.1, the MMC consists of several SMs connected in series to realize the desired output voltage waveform [1]. The number of SMs connected in series (N) depends on the dc-link voltage and the voltage rating of the devices used in the SM. Devices with high-voltage ratings should reduce system complexities by decreasing the required number of SMs and, thus, enabling potentially more compact designs due to fewer devices needed for an HVDC link. Reference [4] used a normally-on SiC JFET for the MMC, whose performance was compared with a SiC MOSFET in terms of efficiency, but parasitic inductances within the SM were not addressed.

Considering a 15kV SiC IGBT under development [5], this paper presents the effects of the high-speed switching, as well as calculations and analyses of the number of levels N, the number of devices for a HVDC terminal, the change in the SM volume with N, and the relation between N and the output voltage total harmonic distortion (THD).

This paper is organized as follows: Section 5.2 reviews, for completeness, basic concepts of VSC-HVDC and MMC. Section 5.3 describes the VSC-HVDC system used, the model of the SM, and analyzes the SM number and capacitance required for a MMC as a function of the device voltage. Section 5.4 presents the proposed PSpice-based simplified model of a generic 15-kV SiC IGBT. Section 5.5 analyzes the effects of the parasitic inductances within the SM architecture. Section 5.6 gives a comparison of the volume of the capacitors, the volume of the IGBT modules and the output voltage THD in the MMC. Finally, Section 5.7 presents the conclusions of this work.

5.2   MMC Sub-Modules

5.2.1   *Power modules and capacitors*

Knowing the VSC-HVdc system parameters (e.g., those shown in Table 5.1), it is possible to calculate the number of SMs needed for each HVdc terminal, and, therefore, the required number of IGBT modules. The topology selected for the SM is the half bridge topology; the advantages of using this topology are given in [10]. The use of an IGBT module for the MMC is shown in [2].

The calculations for the number of SMs per terminal are made taking into account a 25% safety margin on the breakdown voltage for the IGBTs and adding an extra SMs for reliability in the event of a SM failure. The maximum current per IGBT module is obtained from the datasheet of 3.3-kV and 6.5-kV modules, respectively [6].

For the 15-kV IGBT, the current is obtained from the information given in [7], and a 400-A module is selected as a possible future development. A 20% safety margin is used for the maximum current through the modules.

The SM capacitance can be calculated as follows [8]:

$$C_{SM} = \frac{\Delta W_{SM}}{2\varepsilon V_C^2}$$
(5.1)

Table 5.1. System Parameters [9]

Parameter	Power	ac Voltage	dc Voltage	Frequency
Value	800 MW	155 kV	±320 kV	60 Hz

where ΔW_{SM} is the energy pulsation per SM, V_C is the average value of the capacitor or SM voltage (see Table 5.2), and ε is the desired voltage ripple factor. The SM energy pulsation is defined by [16]:

$$\Delta W_{SM} = \frac{2\,P_{dc}}{3\,k\omega_0\,\cos\varphi}\left[1 - \left(\frac{k\cos\varphi}{2}\right)^2\right]^{3/2} \tag{5.2}$$

where P_{dc} is the real dc power of the system, φ is the angle between the voltage and the line current, ω_0 is the angular frequency of the system, and k is the relation between the ac and dc voltages given by [11]:

$$k = 2\frac{V_{a1}}{V_d} \tag{5.3}$$

where V_{a1} corresponds to the arm fundamental ac voltage in Fig. 5.1 and V_d to the dc link voltage.

Table 5.2 shows the minimum number of modules required in a MMC for the selected system. A 15-kV SiC IGBT module (i.e., several dies in parallel) with a maximum current capability of 150 A is not a viable alternative for the SM, since it would require more than double the amount of modules than a silicon 6.5-kV IGBT. However, a 15-kV SiC IGBT module with a current capability of 400 A or higher would be a viable solution. The reduction in the SM capacitor size is significant; a reduction of 6.1 times is observed when the IGBT rated voltage is changed from 3.3 kV to 15 kV. Another important advantage of using a 15-kV SiC IGBT is the capability of operating at higher temperatures [12]. A higher temperature rating of the module would reduce the size of the heatsink required for the module, and could potentially reduce further the size of the overall cooling system of an MMC terminal.

Table 5.2. Number of modules required per MMC terminal

Voltage rating of the IGBT (kV)	3.3	6.5	15	15
Number of SMs per arm	286	146	64	64
Sub-module voltage (kV)	2.24	4.38	10	10
Capacitance per SM (mF)	6.7	2.4	1.1	1.1
Peak current per arm (A)	2524	2524	2524	2524
Maximum current per module (A)	1500	750	150	400
Modules required in parallel	3	5	22	8
Minimum required modules per MMC	10296	8760	16896	6144

5.2.2 Sub-module model

References [8], [16] and [13] analyze the MMC arms as voltage sources with a dc bias $\pm V_d$ and an ac component as shown in Fig. 5.2 (a). Since the main focus is on the behavior of the SM, the arm of the MMC is modeled as shown in Fig. 5.2 (b). The model shown in Fig. 5.2 (b) is used in the simulations addressed in Section 5.5 because the output voltage waveform of the MMC is formed by adding up all the voltages of the "on-state" SMs, and the voltage seen by each SM is ideally not more than its capacitor voltage.

5.3   IGBT PSpice Model

This paper uses PSpice to model a 15-kV SiC IGBT based on the simulated results presented in [7] and [14]. The IGBT model in [7] is done using a physics-based approach, different from the circuit-based approach of PSpice; thus, some of the PSpice parameters were obtained here by curve fitting the turn-on and turn-off characteristics in these references.
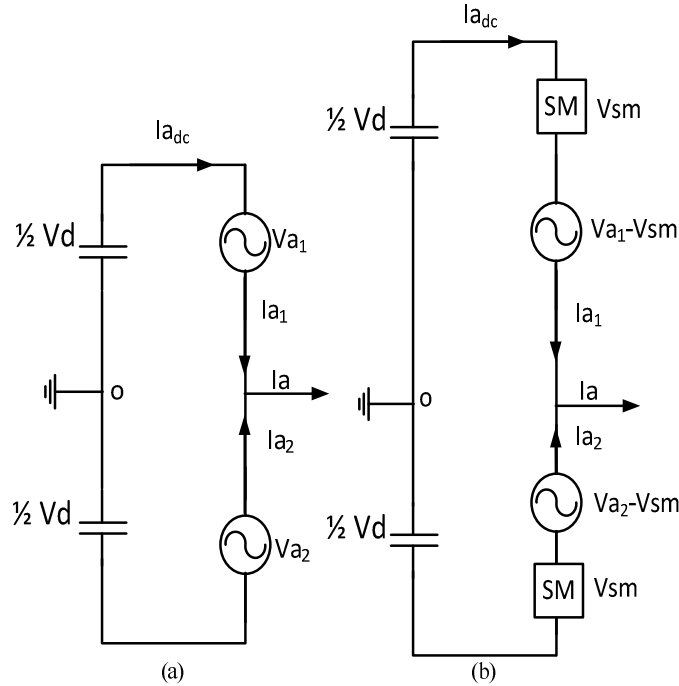
Fig. 5.2. (a) Phase A of a MMC model [8], (b) Used model of Phase A of an MMC

Table 5.3 illustrates the PSpice parameters used in this paper to model the 15-kV IGBT from [5]. Reference [14] provides an explanation of the PSpice IGBT parameters. The fall time can be calibrated by adjusting the lifetime of the minority carriers, TAU [15]. When calibrating the turn-off delay, the PSpice parameters COXD and CGS need to be adjusted until the desired waveform is obtained. For modeling the breakdown voltage of the device, the area of the device (Area), the avalanche multiplication exponent (BVN), and the avalanche uniformity factor (BVF) are adjusted. The turn-off transient of the IGBT is shown in Fig. 5.3, with the total turn-off time being approximately 390 ns, compared to 360 ns in [7]; the model is considered in good agreement taken into account the scope of this paper. The green line represents the collector current, the red line is the collector to emitter voltage, and the purple line is the gate to emitter voltage (±15 V) applied to to the IGBT.

Table 5.3. IGBT PSpice parameters

| Name	Description	Value	Units	Source
Area	Area of the device	1.0	cm^2	[7]
MUN	Electron mobility	950	$cm^2\,V^{-1}\,S^{-1}$	[7]
MUP	Hole mobility	124	$cm^2\,V^{-1}\,S^{-1}$	[7]
NB	Base doping	4.5×10^{14}	cm^3	[7]
WB	Metallurgical base width	117	µm	[14]
VTD	Gate-drain overlap depletion threshold	-5	V	[14]
VT	Threshold voltage	8.0678	V	[14]
BVN	Avalanche multiplication exponent	25	--	[14]
JSNE	Emitter saturation current density	6.5×10^{-13}	A/cm^2	[14]
THETA	Transverse field factor	0.02	V^{-1}	[14]
TAU	Ambipolar recombination lifetime	20×10^{-9}	s	Curve fitting
BVF	Avalanche uniformity factor	5.5×10^4	--	Curve fitting
AGD	Gate-drain overlap area	0.55	cm^2	Curve fitting
KP	MOS transconductance	5.5219	A/V^2	Curve fitting
KF	Triode region factor	0.18368	--	Curve fitting
CGS	Gate-source capacitance	1×10^{-15}	F/cm^2	Curve fitting
COXD	Gate-drain oxide capacitance	1.3×10^{-12}	F/cm^2	Curve fitting
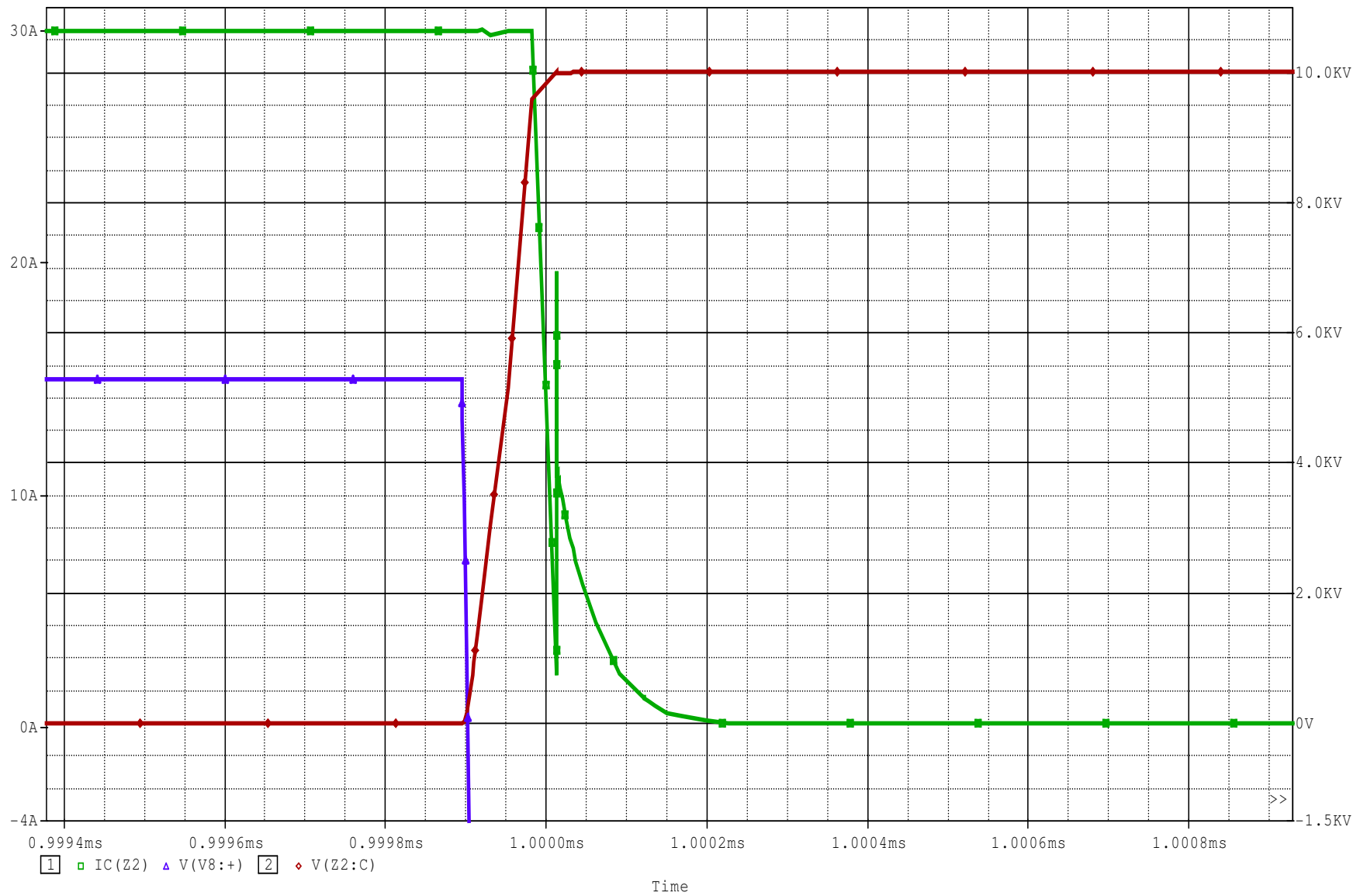
Fig. 5.3. Turn-off of the 15-kV SiC IGBT PSpice model

Reference [6] has three IGBTs placed in parallel within the IGBT module to obtain the rated current of the module. To represent a 15-kV SiC IGBT module, three and eight IGBT's are placed in parallel within the module. This will result in current ratings of 150 A and 400 A, respectively, for the IGBT module.

5.4   Effects of Parasitic Inductances

Table 5.2 showed that several IGBT modules need to be placed in parallel within the SM due to the current limitations of the IGBT modules commercially available for the selected voltage ratings. A busbar arrangement is used to parallel IGBT modules; this busbar arrangement will have inherent parasitic inductances, particularly between the emitter of S1 and the collector of S2 as shown in Fig. 5.4. Different values for the parasitic inductances are calculated using (5.4) [16].

$$L_{bar} = 0.002l \left(2.303 \log_{10} \left[\frac{2l}{b+c} \right] + 0.5 + 0.2235 \left[\frac{b+c}{l} \right] \right) \tag{5.4}$$

where l represents the bus bar length, b, the bus bar width, and c, the bus bar thickness. The value of L_{bar} is given in µH. The cross section of the bus bar is calculated using [17] and the current ratings using the parameters in Table 5.1.

Different configurations for paralleling the IGBT modules within the SM will result in different parasitic inductance values. A symmetrical configuration is used to parallel the IGBT modules; this means L_1 is equal to L_2. A sensitivity analysis is performed for different busbar lengths with the results given in Table 5.4. The model developed in section 5.4 is used for the simulations of the effects of the parasitic inductances with a load current of 120 A representing only 4.8% of the total load current for the system in Table 5.1.
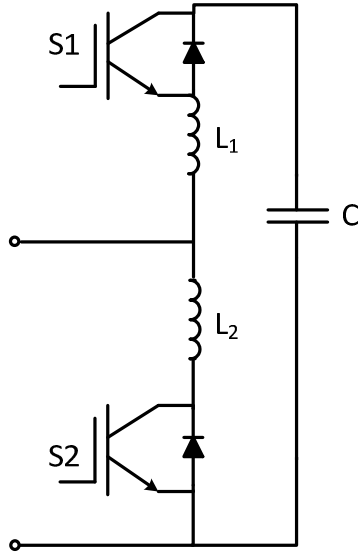
Fig. 5.4. SM parasitic inductances

Table 5.4 Sensitivity analysis results

Inductance (nH)	Overshoot (V)	Busbar length (cm)
43	132	12.7
95	331	25.4
154	546	38.1
219	1102	50.8
287	1880	76.2

The largest voltage overshoot of 1.88 kV or 18.8 % is produced for a parasitic inductance value of 287 nH. The ringing frequency of this turn-off transient is around 71 MHz. Fig. 5.5 displays the simulation results for these conditions; the current is in green and the voltage in red. Table 5.4 also shows, as it is well known, the importance of keeping the length of the bus bar as short as possible in order to minimize the parasitic inductances.
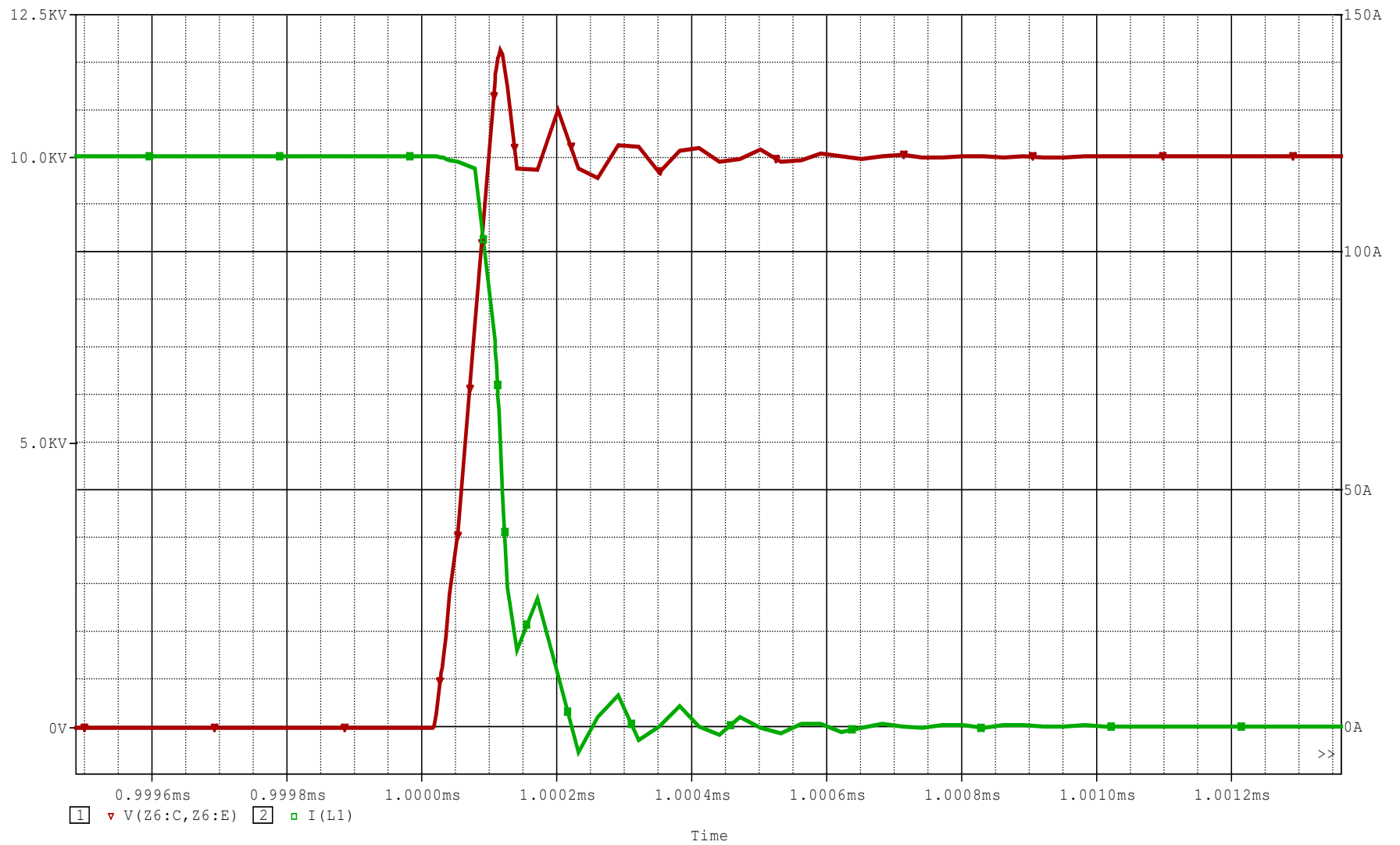
Fig. 5.5. Turn off transient of the IGBT PSpice model

Table 5.5 IGBT module volume

IGBT Module	Voltage Rating (kV)	Individual Module Volume (L)	Total Module Volume (kL)
5SNA 1500E330305	3.3	1.01	10.4
5SNA 0750G650300	6.5	1.28	11.2

5.5   MMC Terminal Volume and THD

5.5.1   IGBT module volume

The total volume occupied by the IGBT modules can be evaluated as well to calculate the total space needed for the HVDC terminal. To calculate the total volume of the IGBT modules, the commercially available modules from ABB; "5SNA 1500E330305" was selected as a 3.3 kV IGBT module and the "5SNA 0750G650300" was selected as a 6.5 kV IGBT module [6].

Using the dimensions of these modules given in the datasheet the volume of an individual module was calculated, and then the total volume of all the modules on a terminal was calculated. These results are presented in Table 5.5. No volume calculation was done for a 15-kV 400-A SiC IGBT module, as this module is not available yet. The calculation is just for the volume of the IGBT module itself and does include the volume of the thermal management system.

Table 5.5 shows that the 6.5-kV IGBT design requires about 7.8% more space in an HVDC substation than one with the 3.3-kV IGBT module.

5.5.2   Capacitance volume

The SM capacitance is another important parameter that changes with the number of SM. From Table 5.2 and comparing to the 3.3-kV device, the SM capacitance is reduced by 80% when

using 15-kV devices. The number of components is another important reduction; a 15-kV device reduces the number of components by 40% compared to the 3.3-kV device, and by 30% compared to the 6.5-kV device.

Even with a reduction in the overall number of modules required, as shown in Table 5.2, the overall volume occupied by a 6.5-kV IGBT module is increased due the difference in the volume of the individual module.

The physical volume of the capacitors in the MMC can be compared by selecting a commercially available capacitor line; for example, EPCOS MKK-DC capacitor line [18]. First, the SM capacitance was calculated using (1) and then the capacitors are selected. The criterion for choosing the combination of capacitors was the following:

- The nominal voltage of the capacitor combination should be the SM voltage at a minimum.

- The maximum voltage of the capacitor combination should be the IGBT voltage rating as a minimum.

- The total capacitance of the capacitor combination should be at least the calculated capacitance using (1).

- Capacitors with the same voltage rating should be used.

Once the capacitor combination was selected, the total volume of the equivalent capacitance was calculated using the dimensions provided in the datasheet. The volumes for the SM capacitors are given in Fig. 5.6(a) using the values from Table 5.2 and [18].

Fig. 5.6 (a) presents a decrease of 77.8% in the SM capacitor volume using the 3.3-kV device when compared to the 15-kV device due to the voltage rating limitations of the selected capacitor.

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The total volume of the capacitors for an MMC arm is calculated and shown in Fig. 5.6(b). The overall volume of the capacitors decreases by 1.3% when comparing the 3.3-kV device with the 15-kV device. Even though there is a noticeable difference in the SM capacitance volumes, the overall MMC capacitor volumes are much closer due to the reduction in the component count when using 15-kV devices. Once again, this volume difference is created by the lack of a capacitor with the required capacitance range and a voltage rating high enough for a 15-kV device.

(a)   (b)
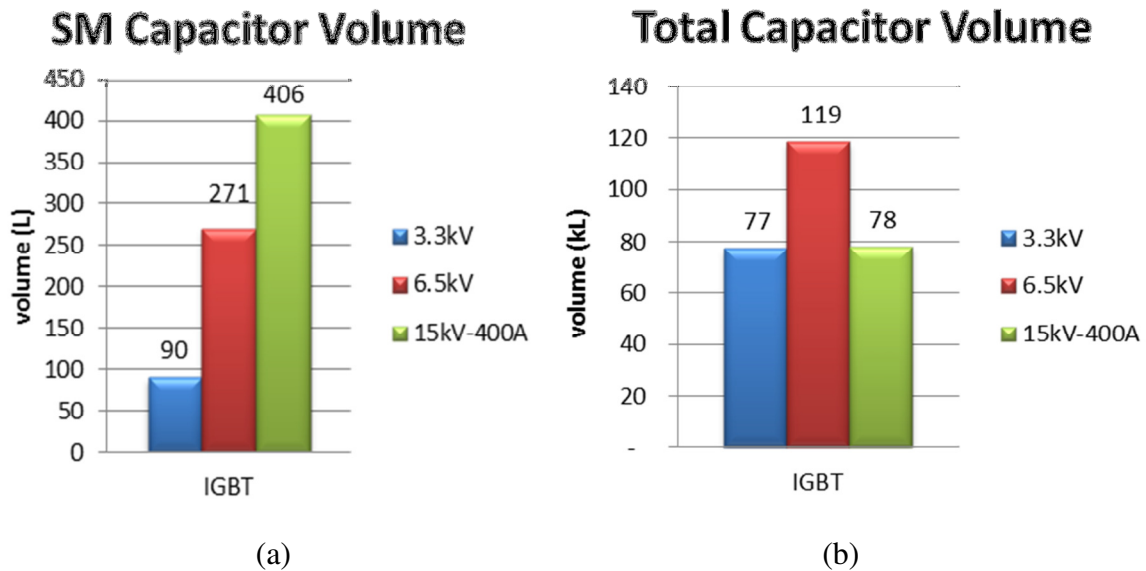
Fig. 5.6. (a) SM capacitor volume. (b) Total volume of capacitors in the MMC

Table 5.6. Total volume occupied by the MMC sub-modules

IGBT Module	Capacitance Volume (kL)	Total Module Volume (kL)	Total SM Volume (kL)
5SNA 1500E330305	77	10.4	87.4
5SNA 0750G650300	119	11.2	130.2

After comparing the volume of the capacitors and the IGBT modules, the overall volume of the components of the SM is calculated and shown in Table 5.6. Table 5.6 shows that a reduction in the amount of SMs needed for the MMC terminal does not directly translate into a reduction in the volume required for the SM. This is due to the volume of the IGBT modules itself. Using a 6.5 kV IGBT module reduces the amount of devices by 15%, compared with the 3.3 kV IGBT, but increases the overall volume by 8.5% as a tradeoff.

5.5.3   *Total harmonic distortion*

Not requiring an output filter because of the large number of steps forming the ac waveform is an important advantage for the MMC, since the output filters are bulky and take a considerable amount of space in the HVDC substation.

The number of steps is related to the number of SMs per arm. The number of steps will decrease with the use of a 15-kV SiC IGBT module, and, therefore, affect the THD of the ac voltage waveform. Reference [19] demonstrated that the output voltage waveform does not require any filters after 23 levels per arm. As shown in Table 5.2, a 15-kV SiC IGBT module would require at least 32 levels for the considered HVDC system. Therefore, the output voltage waveform would not require any additional filtering to fulfill the IEEE 519 requirement for transmission levels of 1.5% THD.

Using Microsoft Excel, it is possible to tabulate the data points for the THD provided in [19], and use a power trend line to obtain an approximate equation relating the number of SMs and the output voltage THD. This equation is:

$$THD(\%) = 147.53(N)^{-1.44} \qquad\qquad (5.4)$$

where N represents the number of SMs per arm in the MMC HVDC terminal. Fig. 5.7 depicts, in graphical form, the relationship between the number of levels N, the output voltage THD, and the SM capacitance volume; the blue line shows the volume that the capacitors will occupy within the SM, the green line, the required capacitance per SM, and the black line, the trend line for the THD as N increases. Fig. 5.7 also shows that the capacitance volume per SM decreases when N increases.

5.6   Conclusions

The use of 15-kV SiC IGBT modules is a viable option for the MMC if these modules are rated 400 A or higher. A 150-A module would definitely not be a suitable option for HVDC systems. A 15-kV IGBT greatly reduces the amount of SMs and lowers the capacitance of each SM. The tradeoff is that using 15-kV SiC IGBT modules reduce the number of steps for forming the ac voltage waveform.

However, the reduction in the number of steps does not result in the THD being above 1.5%, so no output filters are required. A high voltage capacitor is required in order to have a significant reduction in the overall volume of the MMC terminal.

The influence of the parasitic inductances must be taken into account when the SM is being designed, since large overvoltages may lead to lower SM voltages, and, thus, a larger amount of SMs, which has an impact on the cost of the VSC-HVDC terminal. Keeping the parasitic inductances minimized enables the design engineer to increase the operating voltage of the SM.
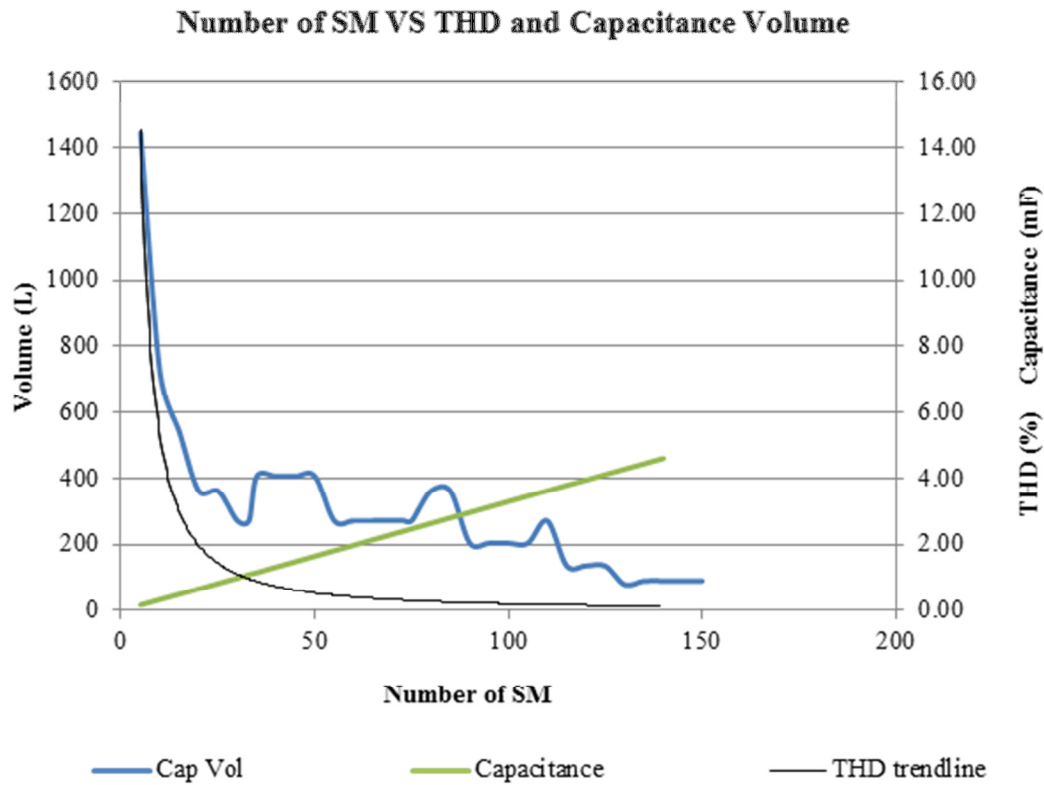
Fig. 5.7 THD, SM capacitance volume, capacitance and N relation

Lastly, a 15-kV SiC IGBT module capable of conducting more than 400 A can also increase the overall power that an MMC terminal is able to handle, therefore increasing the power limit for the VSC-HVDC technology.

Acknowledgment

References

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings*, 2003 IEEE Bologna, 2003, vol. 3, p. 6 pp. Vol.3.

[2]   B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *Transmission and Distribution Conference and Exposition*, 2008, IEEE/PES, 2008, pp. 1–16.

[3]   S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *IEEE Power Electronics Specialists Conference*, Rhodes, Greece, June 2008, pp. 174–179.

[4]   D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J.-K. Lim, M. Bakowski, L. Ängquist, and H. Nee, "High-Power Modular Multilevel Converters With SiC JFETs," *Power Electronics, IEEE Transactions* on, vol. 27, no. 1, pp. 28 –36, January 2012.

[5]   J. Wang, A. Huang, W. Sung, Y. Liu, and B. J. Baliga, "Development of 15-kV SiC IGBTs and their Impact on Utility Applications," *IEEE Industrial Electronics Magazine*, vol. 3, no. 2, pp. 16 –23, June 2009.

[6]   ABB "ABB HiPak - IGBT and Diode Modules (Semiconductors)." [Online]. Available: http://www.abb.com/product/db0003db004291/c12573e7003304adc1256f01003e367f.aspx ?productLanguage=us&country=US. [Accessed: 16-Jul-2012].

[7]   W. Sung, "Design and Fabrication of 4H-SiC High Voltage Devices," North Carolina State University, Raleigh, North Carolina, USA, Doctoral dissertation, 2012.

[8]   M. Vasiladiotis, "Analysis, Implementation and Experimental Evaluation of Control Systems for a Modular Multilevel Converter," M.S. Thesis, Dept. Elect. Eng., Roy. Tech. Inst., Stockholm, Sweden 2009.

[9]   "ABB DolWin1 - ABB HVDC Reference Projects in Europe (HVDC References)." [Online]. Available: http://www.abb.com/industries/ap/db0003db004333/8b74a5fe4cc03e44c125777c003f3203. aspx. [Accessed: 02-Jul-2012].

[10]   N. Ahmed, A. Haider, D. Van Hertem, Lidong Zhang, and H.-P. Nee, "Prospects and challenges of future HVDC SuperGrids with modular multilevel converters," in Proceedings *of the 2011-14th European Conference on Power Electronics and Applications* (EPE 2011), 2011, pp. 1–10.

[11] Y. Zhang, G. P. Adam, T. C. Lim, S. J. Finney, and B. W. Williams, "Analysis and experiment validation of a three-level modular multilevel converters," in *2011 IEEE 8th International Conference on Power Electronics and ECCE Asia* (ICPE & ECCE), 2011, pp. 983–990.

[12] R. Singh, S.-H. Ryu, D. C. Capell, and J. W. Palmour, "High temperature SiC trench gate p-IGBTs," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 774 – 784, Mar. 2003.

[13] Q.i Tu, Z. Xu, H. Huang, and J. Zhang, "Parameter design principle of the arm inductor in modular multilevel converter based HVDC," in *2010 International Conference on Power System Technology* (POWERCON), 2010, pp. 1–6.

[14] J. A. VanGordon, "Hefner model parameters for power IGBTS under pulsed power conditions," University of Missouri, Columbia, Missouri, USA, Master's Thesis, 2010.

[15] A. Haddi, A. Maouad, O. Elmazria, A. Hoffmann, and J. P. Charles, "A Simplified Spice Model for IGBT," *Active and Passive Electronic Components*, vol. 21, no. 4, pp. 279-292, 1998.

[16] G. L. Skibinski and D. M. Divan, "Design methodology and modeling of low inductance planar bus structures," in *Power Electronics and Applications*, 1993., Fifth European Conference on, 1993, pp. 98, 105 vol.3

[17] Copper Development Association Inc. "Ampacities and Mechanical Properties of Rectangular Copper Busbars." [Online]. Available: http://www.copper.org/applications/busbar/ampacity/bus_table3.html. [Accessed: 13-Nov-2012].

[18] EPCOS AG, "Power capacitors" MKK-DC / MKK-DCI(-H) / MKKCD-R, Product Brief, 2011.

[19] C. C. Bonilla, S. M. Tigga, "Design and performance comparison of Two-level and Multilevel Converters for HVDC Applications," Chalmers University of Technology, Sweden, Master's Thesis, 2011.

APPENDIX C.1

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July 1, 2013

To whom it may concern,

This letter is to verify that Mr. David Alejandro Guzman, ID number: 010591001, is the first author and did at least 51% of the work for the paper titled "The Impact of High-Voltage and Fast-Switching Devices on Modular Multilevel Converters".

Kind Regards,

Dr. Juan Carlos Balda

University Professor and Major Advisor to Mr. Guzman

Interim Department Head

CHAPTER SIX

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1   Conclusions

The main objective of this thesis was to analyze the current technologies used for transmitting power, focusing on HVdc systems. The enabling objectives were to build a simulation model of an HVdc system between to power grids, to implement a sensorless controller for grid synchronization of an MMC-based HVdc terminal, and to analyze the impact of a high-voltage, fast-switching SiC IGBT's on an MMC-based terminal. This thesis has accomplished the following:

- A theoretical background was given of HVdc technologies, focusing on MMCs. From this background it was concluded that the MMC has several advantages over other HVdc-VSC topologies so it is a viable alternative for HVdc-VSC links, especially when trying to connect to weak ac grids.

- A technique for balancing the SM capacitor voltage in the MMC was presented and analyzed. The technique presented also controls the circulating current within the phases of the MMC.

- A first order transfer function to model the MMC plant was presented. Once a PI controller is added to control the plant, it becomes a second order transfer function that facilitates the design the current controller of the MMC. The process was shown and validated with simulations. The calculation of the various gains for the inner current of the MMC followed a similar process to the one followed for a two-level inverter. This

facilitates the process of building a simulation model for individuals already familiar with a three-phase two-level inverter control. A prefilter was added to reference command of the controller to ensure the selected bandwidth was achieved. Without a prefilter, the system bandwidth is more than twice the selected design target.

- The outer controllers of an HVdc link, power control and dc-voltage control, were explained and a method was presented to calculate the various gains for the controllers. The tuning of the outer controllers must be done with care to ensure that the correct bandwidth of the controller is selected in order to avoid instability issues of the system. A bandwidth of 40 Hz for the outer controller proved to be suitable for the Matlab/Simulink™ simulations.

- A working model of an MMC-based two-terminal HVdc link was presented and the design steps of the model were given. The model was built using the theoretical background given in the thesis and it can be expanded and improved for different simulation purposes.

- A new sensorless control technique was proposed to synchronize a MMC-based HVdc terminal to a grid. The proposed technique was analyzed to test its performance under grid-frequency changes, harmonic-voltage pollution and voltage sags. The technique performed well under the different tests. It was able to detect voltage sags, keep its stability under grid-frequency changes and was able to inject currents with low THD, even when the grid had harmonic-voltage pollutions. It was shown to be a viable sensorless control technique that could be implemented to reduce complexity in an HVdc substation by eliminating sensors or in conjunction with a traditional technique,

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to add a safety layer in case of sensor failure. The various PI gains were selected so no overshoots were present for a commanded reference change.

- A simplified PSpice-based model of a 15-kV SiC IGBT was proposed. The model was used for an study on the impact that a 15-kV SiC IGBT would have on a MMC for HVdc applications. The study covered the effect of parasitic inductances within the SM of the MMC, impact on the output voltage THD due to the reduction of number of levels and how the SM capacitance would change in nominal value and volume with the new device. The study concluded that a 15-kV SiC IGBT would be a viable option for MMC terminals if the current capability of the IGBT is increased, a module of 400A was proposed as a development target. Another conclusion of the study was that the currently commercially available capacitors do not have the voltage capability that a 15-kV SiC IGBT-based SM would require. Therefore, in order to implement the 15-kV SiC IGBT in an MMC for and HVdc application, the voltage capability of the capacitors should be increased.

6.2   Recommendations for Future Work

Some suggested improvements include the following:

- A comparative study between different SM capacitor voltage balancing techniques: this study should include the voltage balancing techniques proposed in the MMC literature and evaluate the tradeoffs between different techniques. This study should provide the readers with a reference for choosing the right voltage balancing technique.

- Analyze the behavior of the MMC under fault conditions: a controller for unbalanced conditions can be applied to the MMC terminals to improve the system response under faults and unbalanced conditions.

- The simulation model of a two-terminal HVdc link can be expanded to a multi-terminal simulation model: a third terminal, for example a wind farm, can be added to the system to analyze its behavior.

- Include a model for the dc-transmission lines for a more accurate simulation of an HVdc transmission system.

- The multi-terminal simulation model can be used to study the response of the system under faults and unbalanced conditions.

- A small-scale prototype of an MMC: this prototype could be used to test different voltage balancing algorithms as well as the different control algorithms presented in this thesis.

- Negative- and zero-sequence controllers can be added to the proposed sensorless controller to improve its performance under unbalanced conditions.

- Reduce the time step of the simulations to further verify the results obtained.

- A second order generalized integrator can be implemented to the sensorless technique to further improve its robustness against harmonic pollution on the grid voltages.

- The simplified model of the 15-kV SiC IGBT can be improved and exported to Matlab/Simulink™ to realize more tests regarding the efficiency of the system when compared with a 3.3-kV Si IGBT.

- An average model of the MMC can be used to speed up the simulation times when evaluating new control algorithms at the system level.