8-2013

Electrical Design Considerations and Packaging of Power Electronic Modules

Shijie Wang
University of Arkansas, Fayetteville

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A thesis submitted in partial fulfillment
of the requirements of the degree of
Master of Science in Electrical Engineering

By

Shijie Wang
University of Arkansas
Bachelor of Science in Electrical Engineering, 2011

August 2013
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

_____
Dr. Simon S. Ang
Thesis Director

_____
Dr. Juan C. Balda
Committee Member

_____
Dr. Randy L. Brown
Committee Member

ABSTRACT

A modern power electronic module can save significant energy usage in the power electronic systems by improving their switching efficiencies. One way to improve the efficiency of the power electronic module is to reduce its parasitic circuit elements. The purpose of this thesis is to investigate the mitigation of parasitic circuit elements in power electronic modules. General methods of mitigating parasitic inductances were analyzed by the Q3D Extractor and verified by the time-domain reflectometry (TDR) measurements. In most cases, the TDR measurement results closely matched those predicted by the Q3D Extractor. These methods were applied to design and analyze a 50KVA 650V silicon carbide (SiC) half-bridge power electronic power module consisting of three separate power substrates interconnected in parallel. The layout of this power module was constrained by the existing module housing. The parasitic inductances of the power module substrates were measured by TDR, and compared to those simulated values by the Q3D Extractor. Due to the differences in the lengths of current paths, the parasitic circuit elements for the three paralleled SiC power substrates, each consisting of 10 SiC power MOSFETs and 9 SiC diodes, were different.

ACKNOWLEDGMENTS

First of all, Thank God for giving me the opportunity to be a student at the University of Arkansas and the chance to be a research assistant while working for a master degree in electrical engineering which gives me the drive to accomplish one of my most important lifetime goals.

There are many people I would like to thank for, my family, my friend, my teachers, my colleagues, and so on. The person I would like to thank the most is my advisor, Dr. Simon Ang. I cannot complete my graduate coursework and research without his encouragement. I really appreciate his support and encouragement. Also, I would like to thank him for all the things he has done for me from the first day of being his graduate student. He is not only a professor to me, but he also helped me like a friend. I would like to thank my classmates who helped me during the last two years. Jingchang Zhou and Hao Zhang trained me how to use the laboratory equipment. Atanu Dutta discussed and shared many of his research experiences. Shilpa Prabhudeva helped me on data acquisition. Xingeng Yang gave me the most encouragement as a best friend of mine. I am blessed that I can study together with such a nice group of classmates. Lastly, I must thank my family who unconditionally supports me throughout my studies.

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Chapter 1. Introduction

Power electronic modules which incorporate multiple power semiconductor devices together with their control circuitries into a single compact package are becoming essential components in many power electronic systems. Besides cost reduction, these power electronic modules can reduce parasitic circuit components, reduce weight and size, and improve electrical performance. These modules not only can lower the cost but they also can increase the reliability of the power electronic systems. Power electronic modules are currently in widespread use in electric vehicles, uninterrupted power supplies, motor control, robot welding machine, washing machines, air conditioners, refrigerators, and many others. This thesis focuses on the design and packaging of power electronic modules for electric or hybrid electric vehicles. An H-bridge power electronic module was designed and fabricated. The electrical design considerations and fabrication processes will be discussed.

The purpose of this thesis is to design and package an H-bridge module for hybrid electric (HEVs) or electric vehicles (EVs). In general, the technology investigated in this thesis is also applicable for the development of power electronic modules for other applications. By incorporating multiple power semiconductor devices together with their control circuitries into a single compact module, the parasitic circuit elements (inductance and resistances) in the power electronic circuits have been shown to reduce considerably compared to the discrete power semiconductor device solutions where the interconnections are the main sources of the parasitic circuit elements. Besides this main merit, the power modules also reduce the cost of the system since individual packages are not needed for each power semiconductor devices. Packages for power semiconductor devices are a substantial cost component. However, besides the parasitic circuit elements, thermal management becomes an important consideration in these power electronic modules due to the close proximity of the power semiconductor devices. The electrical design parameters are addressed in this thesis.

Once the circuit topology has been decided, the power electronic module design starts with the layout of the power semiconductor devices along with peripheral circuit elements such as current sensing resistors, gate-source resistors, and others. The main goal for the module layout is to reduce the parasitic circuit elements by reducing the interconnection paths among the power semiconductor devices. Simulation tools are usually used to help in this layout task. Besides electrical optimization, thermal design needs to be performed concurrently. Once the electrical and thermal designs of the power module are done, the material selections for the module are to be decided based on the electrical, thermal, and mechanical properties desired for the module. Compromises are needed to integrate these materials into a reliable power module.

This thesis is organized into four chapters. Chapter 1 introduces the objectives of this thesis and the rationales behind the research work. Chapter 2 presents the parasitic mitigation as a part of the design process for the power electronic modules. Chapter 3 discusses the design and packaging of a silicon carbide half-bridge power module. Chapter 4 concludes the thesis work.

Chapter 2. Electrical Design Considerations

2.1 Introduction

Parasitic circuit elements in power electronic modules are unavoidable and cannot be totally eliminated. These parasitic circuit elements include parasitic capacitances, parasitic resistances, and parasitic inductances. P-cell and N-cell based IGBT power module design has been used to mitigate parasitic circuit elements in power electronic modules [1] This design technique has been verified by the Q3D parasitic extraction software, double pulse test, and impedance analyzer [1] on a simple full-bridge switch topology by comparing the parasitic circuit elements from two different layouts of the full-bridge switch. The power semiconductor devices for the optimized layout have shorter current communication loop, as such, parasitic circuit elements are mitigated [1].

In [2], the authors identified the critical layout path and described the mechanisms on how this path influenced the switching performance. It was shown that current sharing and common impedances affect the switching performance of the power electronic switch. Four effects were identified: stray inductance of the different power commutation loops, the inductances along the common emitters, direct coupling, and different positive and negative couplings [2]. The main influence on the current distribution is the different positive and negative couplings, and one of the semiconductor devices is accelerating during turn-on due to the wire bond packaging [2]. In [3], it was demonstrated that a 5nH parasitic inductance can be achieved using a double-layer ceramic substrate. In [4], the current paths are separated into a screw contact and a PCB-based connection to reduce the parasitic elements. From the above literature review, it is clear that the most effective way to mitigate parasitic circuit elements is to shorten the length of the current path or to decrease the area of current loop.

In this thesis work, only the parasitic resistances and parasitic inductances of the power modules are considered. The extraction of parasitic circuit elements is accomplished using the

ANASYS Q3D software simulation. A time-domain reflectometry (TDR) measurement will be used to verify some of these parasitic circuit elements. In this Chapter, some of the most common parasitic circuit elements in power modules will be simulated. The parasitic circuit elements contributed by the copper traces on the direct bonded copper (DBC) substrate, wire bonds, and power terminal connections are considered. Methods to reduce these parasitic circuit elements are proposed and verified by TDR using test structures.

2.2. Parasitic Extractions of Simple Copper Conductors by Q3D Simulator

A simple copper conductor structure on DBC to investigate its parasitic circuit elements is shown in Figure 2.1. As shown, the green conductor is the copper trace on the DBC substrate. The green conductor is 20 mm long, 5 mm wide and 0.3 mm thick, which represent the thickness of the copper trace. The blue pads on both sides of the copper trace are the terminal connectors which may represent the power connectors or inputs and outputs (I/Os). In Q3D simulation, these are known as the source and sink. Both the source and sink terminals are 5 mm $\times$ 5 mm $\times$ 1 mm (width, length and height). As such, the length between the source and drain terminals is 10 mm. In this Q3D simulation, only a DC analysis is performed.

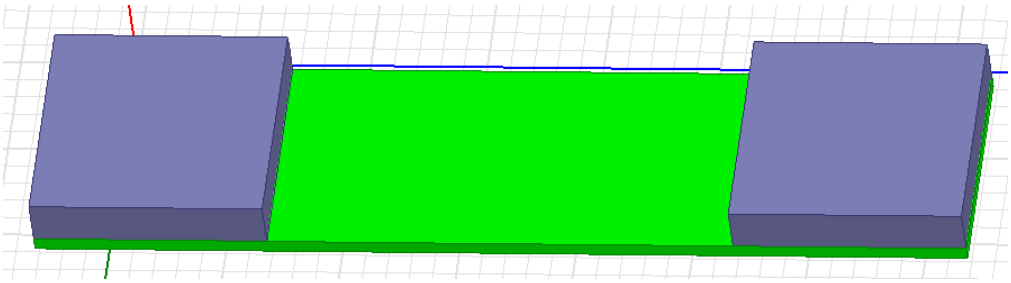


Figure 2.1: A simple conductor for parasitic extraction

Various lengths of the conductor length were simulated and the simulated results for the parasitic inductances and resistances are summarized in Table 2.1. As can be seen, the parasitic inductance increases with increasing conductor length. The increase is almost a linear relationship since the self-inductance of the conductor is directly proportional to the length of the conductor as shown in

Fig. 2.2. As such, the long DBC copper trace can contribute a significant amount of the parasitic inductance.

Length (mm)	**1**	**2**	**4**	**6**	**8**	**10**	**12**	**14**
Inductance (nH)	0.6	1.0	1.9	2.9	4.0	**5.2**	6.4	7.7
Resistance(mΩ)	0.02	0.03	0.06	0.08	0.1	**0.125**	0.15	0.17

Table 2.1: Q3D simulated parasitic circuit element results.

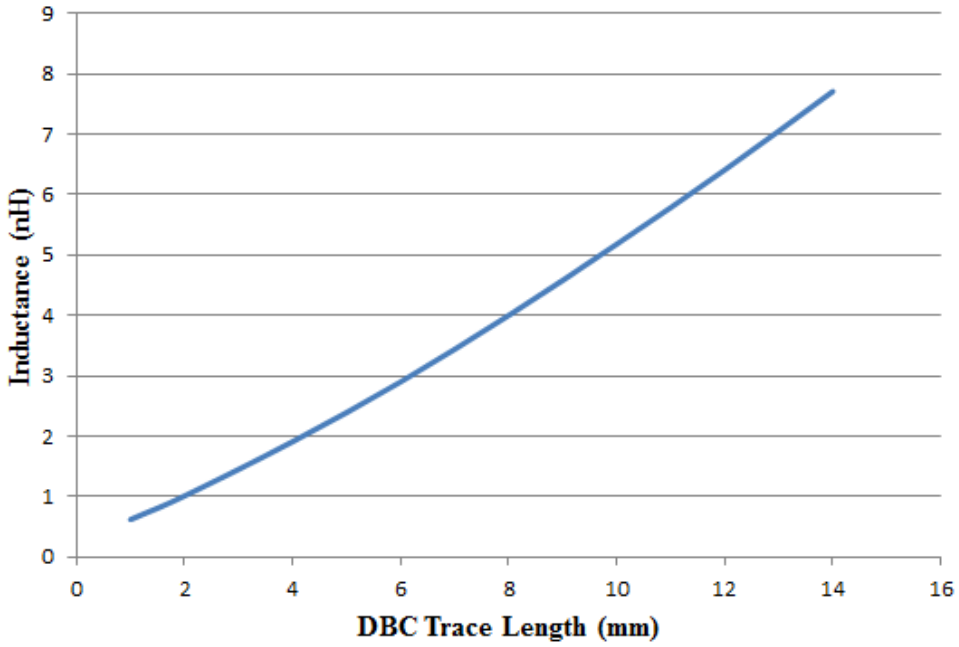


Figure 2.2: Parasitic inductance versus DBC conductor length

It is obvious that the parasitic inductance and resistance also depend on the width of the copper conductor. Table 2.2 shows the parasitic inductances and resistances for different DBC copper widths from 1mm to 8 mm at a fixed length of 5 mm. The parasitic resistance is directly proportional to the aspect ratio, $\frac{l}{w}$, where l is the length of the copper trace and w is the width of the copper trace. As such, the parasitic resistance decreases as the width of the copper conductor on DBC increases. Figure 2.3 shows the non-linear relationship of the parasitic inductance as a function of the copper conductor width on DBC for a fixed length of 5mm. It shows that as the

width of the copper conductor becomes larger, the decrease of the parasitic resistance also decreases. However, a smaller decrease in parasitic inductance is obtained as the conductor width increases.

Width (mm)	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Inductance (nH)	8.2	6.9	6.2	5.6	5.2	4.9	4.8	4.6
Resistance (mΩ)	0.6	0.3	0.21	0.16	0.125	0.1	0.09	0.08

Table 2.2: DBC substrate width simulation results

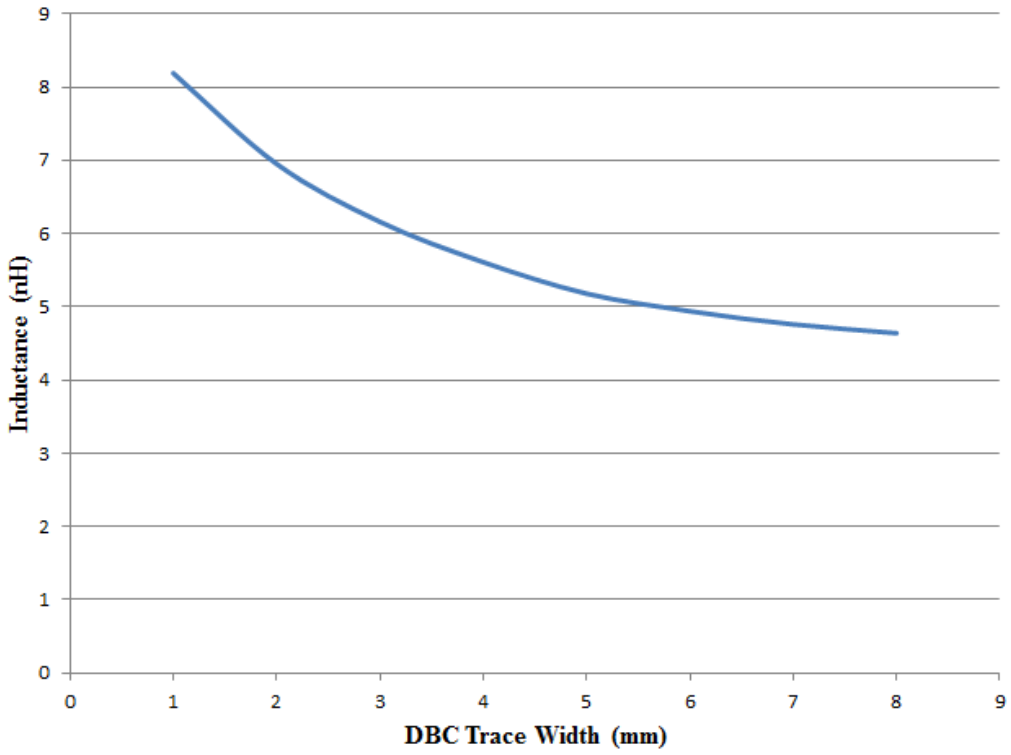


Figure 2.3: Parasitic inductance versus width of copper conductor.

2.3. Parasitic Extraction of Meander and Straight Conductors by Q3D

The electrical conductors in power electronic module are seldom straight, they usually have bends and sometimes, meander in geometry. This is because of the layout constraints due to size of the power substrate or parasitic mitigation. Meander conductors are quite common to increase the desired trace resistance for certain applications such as current sensing resistors for the power semiconductor devices. As such, it is necessary to determine the parasitic circuit elements in these

meander conductors. Figure 2.4 shows a meander conductor and its equivalent straight conductor. Both conductors have a similar length of 30 mm and a width of 3 mm. The spacing between the two conductors in the meander conductor is 1 mm.

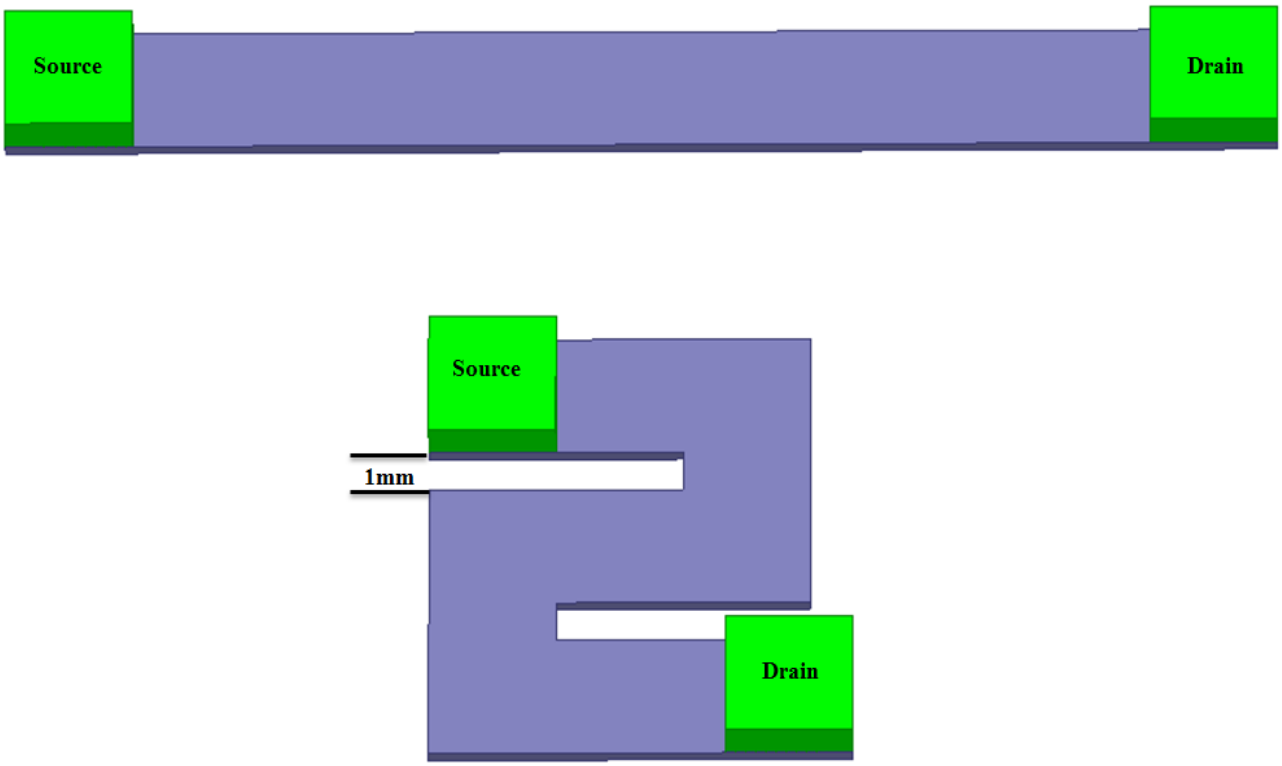


Figure 2.4: Straight and meander conductors used for parasitic extraction.

	Straight Conductor	**Meander Conductor**
Inductance	13.5nH	**4.4nH**
Resistance	0.062Ω	**0.059Ω**

Table 2.3: Parasitic circuit elements of the straight and meander conductors.

As can be seen in Table 2.3, the parasitic inductance for the meander conductor is about 3 times smaller than that of the straight conductor while its parasitic resistance is almost the same for the two structures. The decrease in parasitic inductance is due to the self-inductance cancelling

effects of the current flows in opposite directions in the meander conductor. The parasitic resistance is similar, but, slightly smaller for the meander conductor, due to the current crowding at the two corner conductors.

2.4. Parasitic Extraction for Different Terminal Connections

It has been found that different terminal connections affect the parasitic circuit elements in power electronic module layout. Increasing the height and width of the output terminal affects the parasitic circuit elements. The effects of different terminal connections on the parasitic circuit elements are investigated in this section.

2.4.1 Height of Terminal Connections

Different terminal heights were simulated for the conductor trace shown in Figure 2.1. Table 2.4 lists the parasitic inductance and resistance as a function of the terminal connection heights from 1mm to 8mm. As can be seen, the parasitic inductance and resistance are increasing with terminal height, similar to the increasing in length of the conductor. This is because as the terminal height increases, the effective length of the conductor increases. Figure 2.5 shows the parasitic inductance increases with terminal height.

Height (mm)	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Inductance (nH)	5.18	6.15	6.89	7.5	8.13	8.81	9.39	9.87
Resistance (mΩ)	0.0125	0.127	0.129	0.130	0.131	0.132	0.133	0.136

Table 2.4: Terminal height simulation results

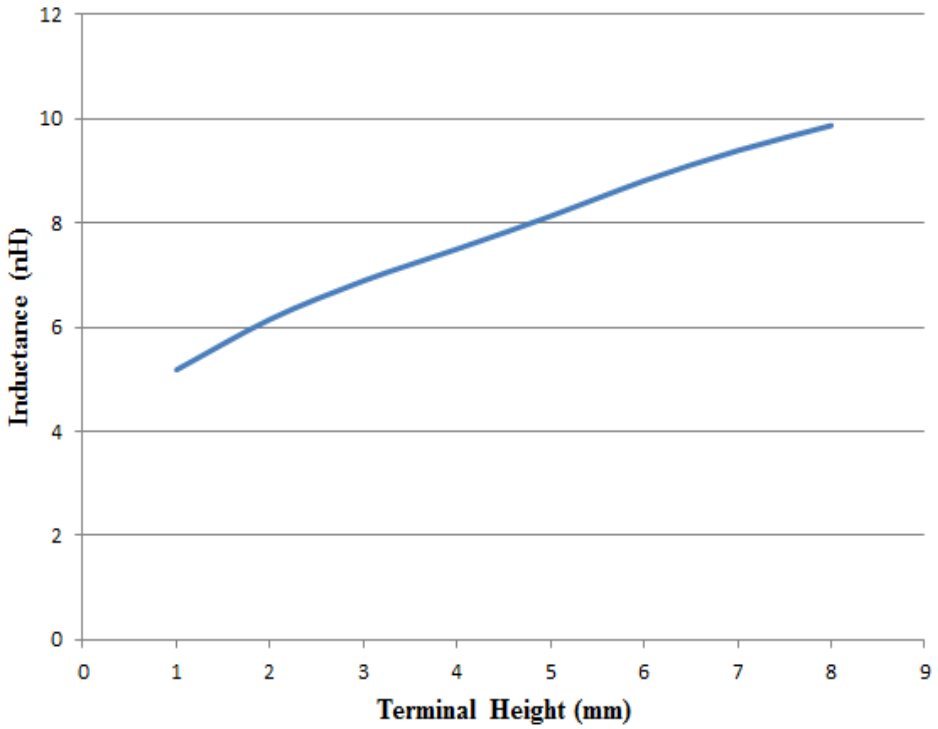


Figure 2.5: Parasitic inductance versus terminal height.

2.4.2. Area of Terminal Connection

It was shown in Figure 2.3 that the parasitic inductance for conductor decreases with the increasing width of the conductor. Thus, it is reasonable to predict that the parasitic inductance also decreases with increasing width of the terminal connection. The area of the terminal connection is changed from 1mm x 1mm to 8mm x 8mm and the parasitic inductance and resistance are extracted using Q3D and summarized in Table 2.5. As the area of terminal connection increases, the parasitic inductance and resistance decrease.

Width and Length (mm)	**1×1**	**2×2**	**3×3**	**4×4**	**5×5**	**6×6**	**7×7**	**8×8**
Inductance (nH)	9.9	8.9	7.7	6.4	5.2	4.0	3.0	2.0
Resistance (mΩ)	0.22	0.2	0.17	0.15	0.125	0.1	0.08	0.06

Table 2.5: Parasitic simulation result as a function of the area of the terminal connection.

2.5. Parasitic Extraction for Bond Wires

Wire bonds are used in connecting the power semiconductor devices to the packaging substrates as well as to provide interconnections. Wire bond introduces parasitic circuit elements in power electronic modules. As such, it is desired to know the parasitic circuit element contributions of these wire bonds. Usually, bond wires of different diameters are used to provide the required current carrying capability. Multiple bond wires are also used to increase the current carrying capability. As such, the parasitic contributions from these wire bonds are important electrical design considerations.

2.5.1. Parasitic Extraction for Multiple Bond Wires

Figure 2.6 shows a power module interconnection structure with multiple bond wires to provide the electrical interconnection. The conductor trace is separated into two equal parts of 10mm with a 2mm gap between the two conductors. Bond wires of 0.15mm diameter are used to connect the two conductors. The length of the bond wires is 0.25mm. One to twelve bond wires are used to connect the two conductor paths. The parasitic extractions using Q3D simulator are shown in Table 2.7. Figure 2.7 shows the parasitic inductance versus the number of bond wires.

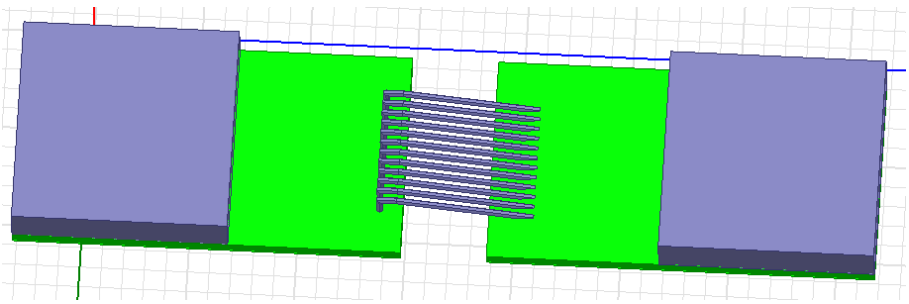


Figure 2.6: Wire bond parasitic simulation

Number of Wires	1	2	3	4	5	6	7	8
Parasitic Inductance (nH)	4.9	4.6	4.3	4.0	3.9	3.8	3.7	3.6

Number of Wires (continued)	9	10	11	12
Parasitic Inductance (nH)	3.54	3.48	3.43	3.39

Table 2.6: Wire bond simulation results

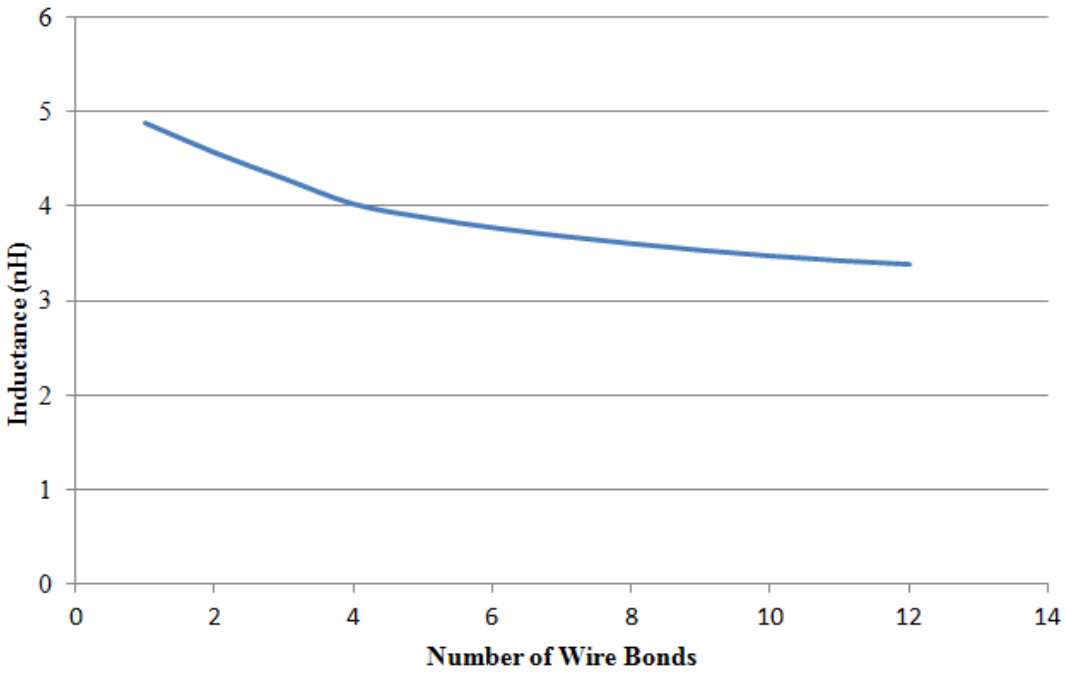


Figure 2.7: Parasitic inductance versus the number of bond wires.

As can be seen from Figure 2.7 the parasitic inductance decreases as the number of bond wire increases. The parasitic inductance decreases more rapidly as the number of bond wires increases from one to four. Thereafter, the decrease in parasitic inductance is more gradual after reaching this critical number of bond wires. For a large number of bond wires such as 10, the decrease in parasitic inductance is very small. The parasitic resistance is decreasing as the number of bond wires increases because the effective width of the conductor path is wider. However, the number of bond wires should be as many as possible to decrease its parasitic resistance.

2.5.2. Parasitic Extraction of Different Length of Bond Wires

Next, the length of the bond wire is varied and Q3D is used to extract the parasitic circuit elements. The same conductor parameters similar to Section 2.5.1 are used. Table 2.8 shows the

results of the Q3D extractions. As can be seen both the parasitic inductance and resistance increase as the length of the bond wire increases.

Length of wires (mm)	2.46	2.8	3.35	4	5
Inductance (nH)	4.7	4.8	5.0	5.2	5.3
Resistance (mΩ)	0.76	0.96	1.02	2.15	3.38

Table 2.7: Wire bond length simulation results

2.5.3. Parasitic Extraction for Different Diameter of Bond Wires

The effects of the diameter of the bond wire on the parasitic circuit elements are investigated. Increasing the diameter of the bond wire increases the current carrying capability of the wire bond. Table 2.9 shows the Q3D extracted results for different diameters of the bond wires. Both the parasitic resistance and inductance are expected to be reduced using larger diameter bond wires. Figure 2.8 shows the parasitic inductance of the bond wire versus its diameter. A larger decrease in parasitic inductance (about 20%) occurs as the diameter of the bond wire increases from 1mil to 3 mil, thereafter, the decrease in parasitic inductance becomes gradual. The reason for the erratic result of the 2 mil diameter is not known.

Diameter of Wires (mil)	1	2	3	4	5	6	7
Inductance (nH)	5.8	6.0	5.2	5.2	4.97	4.8	4.7
Resistance (mΩ)	7.1	7.4	2.3	2.7	4.25	8.3	8.8

Diameter of Wires (mil) (Continued)	8	9	10	11	12	13	15
Inductance (nH)	4.6	4.59	4.46	4.45	4.37	4.3	4.3
Resistance (mΩ)	0.69	0.69	0.47	0.47	0.42	0.38	0.44

Table 2.8: Wire bond diameter simulation results

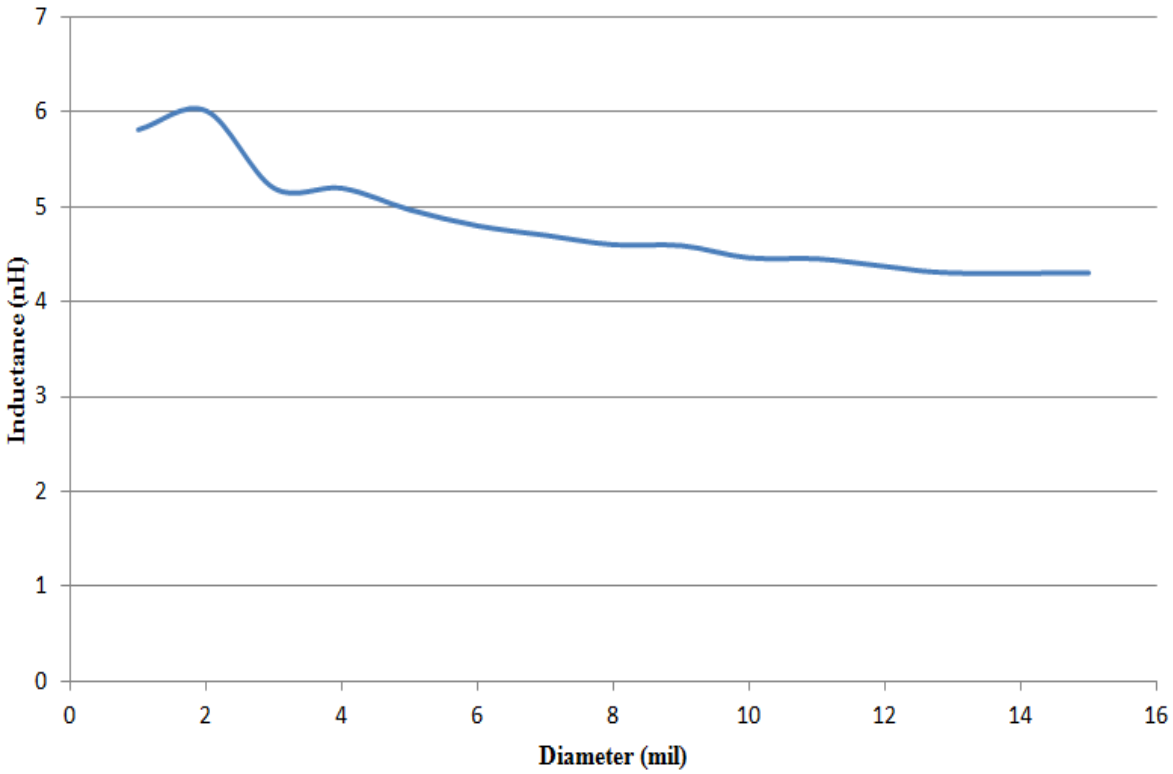


Figure 2.8: Parasitic inductance versus diameter of bond wire

2.5.4. Parasitic Extraction for Wire Bond with Different Spacing

In some power modules more than ten bond wires are used for interconnections. As shown earlier, paralleling of multiple bond wires decreases the parasitic inductance as well as the parasitic resistance. Table 2.10 shows the Q3D extraction results of multiple bond wires with 0.125mm and 0.325mm spacing between each bond wire. As can be seen the decrease in parasitic inductance with a larger spacing is very little for increased spacing. As such, there is not much gain in parasitic inductance mitigation by increasing the spacing between the bond wires.

Wire bond numbers	0.125mm separation between each wire bonds	Separated each 9 wires with 0.325mm
18 wires	16.1nH	15.85nH
27 wires	15.64nH	15.26nH
36 wires	15.1nH	14.93nH

Wire bond numbers	0.125mm separation between each wire bonds	Separate half wire bonds with 0.325mm
2 wires	17.92nH	17.70nH
4 wires	17.43nH	17.10nH
6 wires	17.07nH	16.92nH

Table 2.9: Parasitic inductance versus distance between bond wires.

2.5.5. Wire Bond versus Conductor Trace Comparison

One reason for using wire bond technology in power module is because of its flexibility. However, from the perspective of parasitic inductance, does wire bond have the perceived benefit of parasitic mitigation? Since both wire bonds and copper conductors contribute to parasitic inductance, it is important to compare their contributions to parasitic inductance. Figure 2.9 shows the two structures used for Q3D comparison of parasitic contributions. The width of the conductor trace, 5 mm, is the same for both simulated structures. For the wire bonded structure, 20 bond wires are used. However, different number of bond wires are also simulated and summarized in Table 2.10.

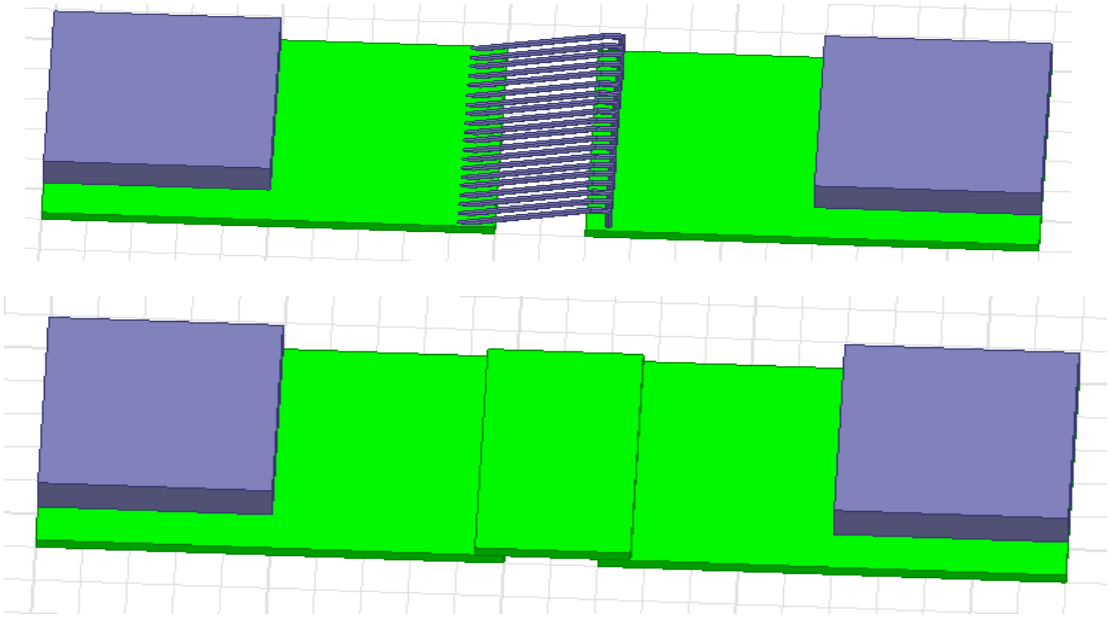


Figure 2.9: Structures used to compare copper trace and wire-bonded copper trace.

	Copper Trace	Copper trace with solid copper Interconnect	1 wires	5 wires	10 wires	15 wires	20 wires
Inductance	6.1nH	6.15nH	8.6nH	7.2nH	6.7nH	6.4nH	6.4nH

Table 2.10: Parasitic inductance for structures shown in Figure 2.9.

As can be seen from Table 2.10 the solid copper interconnect between the copper trace increases the parasitic inductance slightly, from 6.1nH to 6.15nH. Even though the parasitic inductance decreases with the increase in the number of bond wires, the parasitic inductance is still higher than that of the copper trace with solid copper interconnect.

2.6. Summary of Parasitic Extraction

The above parasitic extractions illustrate the principles of how to mitigate the parasitic circuit elements for power electronic module design. First, wire bond is not the best method to provide interconnection because of its parasitic inductance contribution. It is best to use the copper traces on direct bond copper substrate for interconnections. Second, the interconnection copper traces should be as short as possible. Third, if wire bonds are needed, use as many bond wires as possible. Fourth,

use a large diameter bond wire. Fifth, spacing between bond wires should be large. These are summarized in Table 2. 11.

Classification	Method to Use
Wire Bond	1. Increase number of bond wires 2. Shorten the length of bond wires 3. Increase the diameter of bond wires 4. Increase spaces between bond wires 5. Replace bond wires with DBC trace 6. Use new connection technology
DBC Substrate	1. Shorten the Length 2. Widen the width 3. Use meander structure
Power Connector	1. Reduce the height 2. Reduce the area

Table 2.11: Parasitic mitigation design guidelines.

2.7. Test Structure Verification

Time-Domain Reflectometry (TDR) can be used to verify the parasitic inductance in power electronic module. TDR sends a pulse voltage signal to the test structure and measured the reflected waveform to extract the impedance of the structure. Figure 2.10 shows a TDR measurement instrument and the test fixture which simply consists of two wires used to measure the interconnect structures in power electronic module substrate. These two wires are soldered to the copper traces. It should be noted that even though the test fixture looks very primitive, the impedance measurement is quite accurate due to the background impedance subtraction. A Tektronix 6160 TDR is used for the measurement.

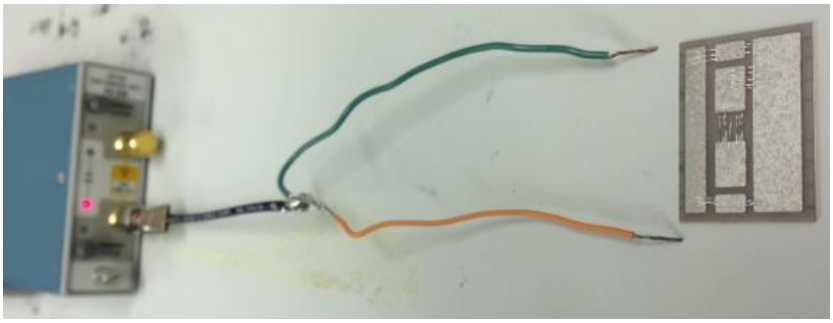


Figure 2.10: A TDR measurement set up.

Figure 2.11 shows the two test structures for TDR measurements. A to G represent the wire bonds along with their copper traces to be measured. Copper traces 1 and 2 are used to extract the copper trace parasitic inductance. Some experimental errors are the different sizes of the source and drain terminal connections. Due to the rise time of the TDR test signal, the TDR measurement cannot be performed for copper traces less than 8mm long. Even though the result may not match the simulation result, but the behaviors of each test is successfully verified by the testing result. Figure 2.12 shows a typical TDR plot for the copper trace with a parasitic inductance of 62nH. As shown the x-axis is the time in nano second and the y-axis is the inductance in nH. The TDR measurement starts with the initialization of the software parameters and then performs a connectivity check. Then, the two connecting wires are soldered onto the test structure. The black TDR waveform represents the parasitic inductance for the measured test structure. The pink TDR waveform is the parasitic inductance of the two connecting wires which is measured by shorting the two connecting wires on the test substrate. The red TDR waveform displays the parasitic inductance of the test structure after subtracting the black TDR waveform from the pink TDR waveform.

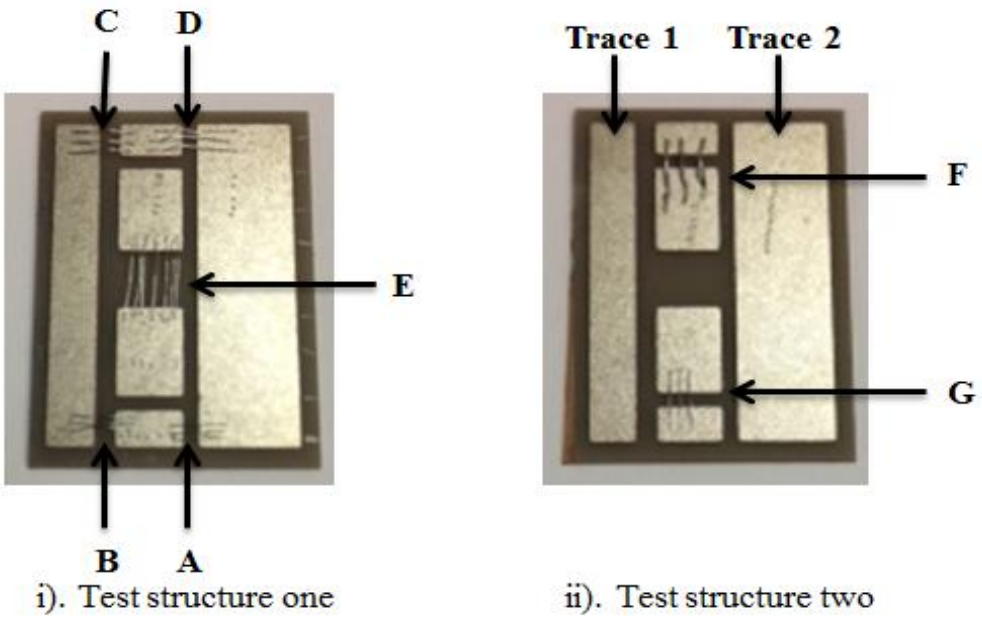


Figure 2.11: TDR test structures.

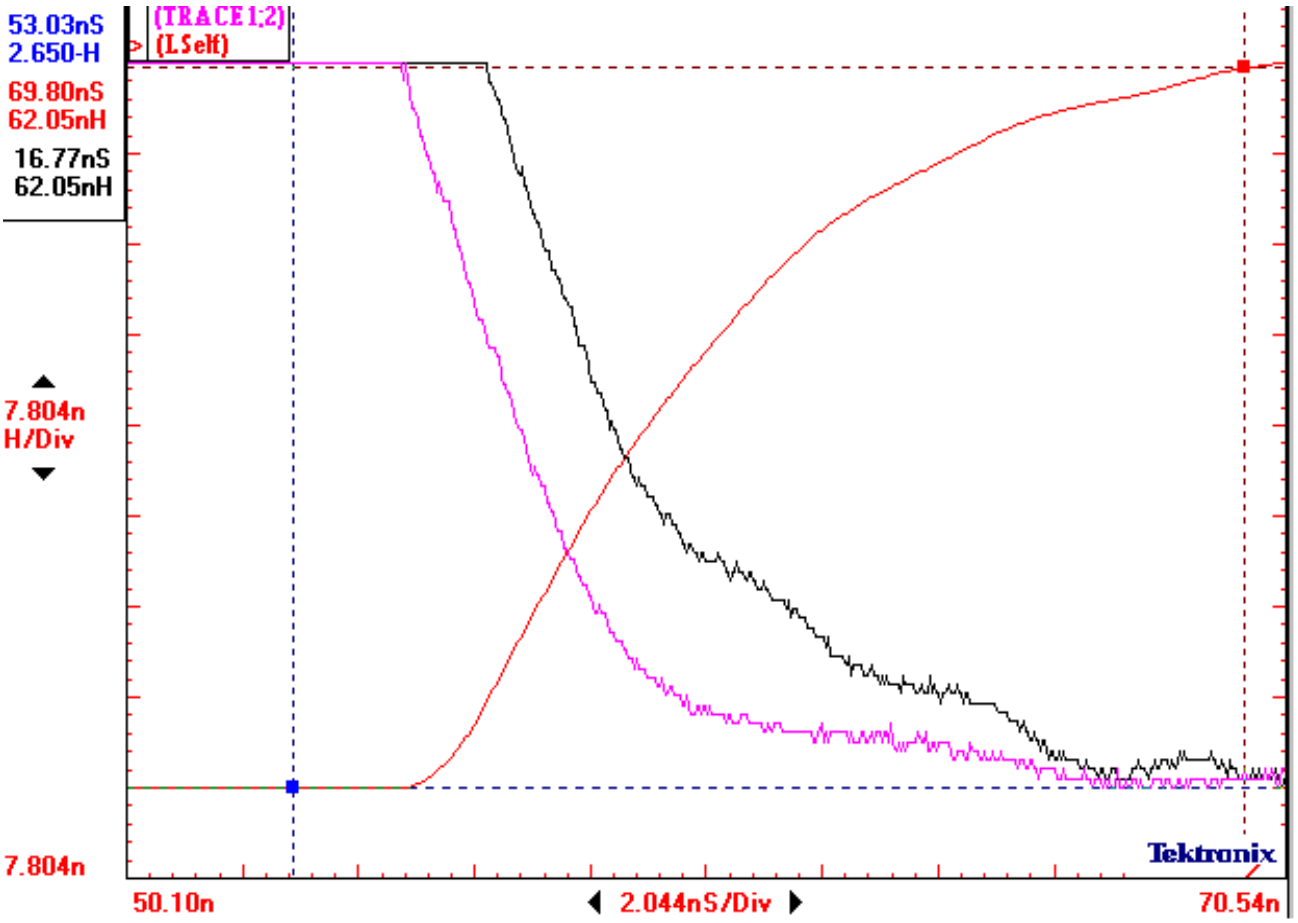
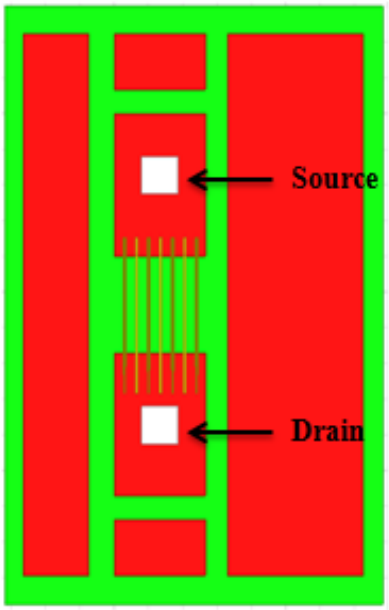


Figure 2.12: TDR waveform for the copper trace.

2.7.1. TDR Measurement of Wire Bonds

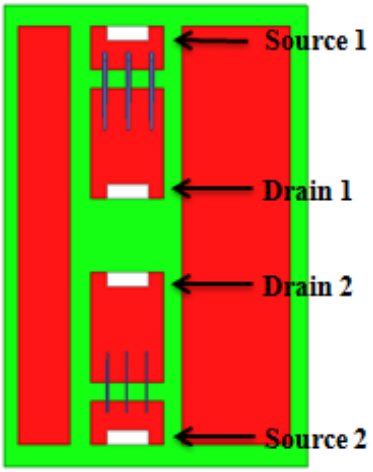
Wire bond E is verified by both the Q3D extraction and TDR measurement. The TDR measurement is taken after one to seven wire bonds are made. Figure 2.13 shows the parasitic inductance extracted from the Q3D and TDR measurement. The discrepancy between the Q3D and TDR results is most likely due to the length of the bond wires. From these results, it shows that the parasitic inductance decreases from four bond wires to one bond wire. The decrease of the parasitic inductance from four bond wires to seven bond wires is very gradual. There is a slight error in measuring the parasitic inductance for the 5 bond wires from the TDR measurement. Hence, the Q3D extraction and TDR measurement yielded similar parasitic inductances.



Number of Wire Bonds	Simulation	Testing result
1	11.6nH	11.7nH
2	9.8nH	11.0nH
3	8.9nH	10.3nH
4	8.4nH	9.8nH
5	8.0nH	8.9nH
6	7.7nH	9.6nH
7	7.5nH	9.36nH

Figure 2.13: Parasitic inductance for one to seven bond wires from Q3D and TDR.

The test structures F and G are both simulated by Q3D and verified by TDR measurements. Figure 2.14 shows the simulated and TDR measured parasitic inductances for bond wire diameters of 5 mils and 12 mil. Each wire bond has three bond wires. A significant parasitic inductance reduction using a larger diameter bond wire can be seen from the results. The large discrepancy of the Q3D extraction and TDR measurement results may be due to short distance between the source and drain contacts. Due to the rise time constraint of the TDR test signal, the measurement can only be performed on a path longer than 8mm.



	5 mils wire bonds	12 mils wire bonds
Testing result	17.8nH	12nH
Simulation	6.2nH	5.9nH

Figure 2.14: Wire bond diameter verification**.**

Test structures A, B, C, D in Figure 2.11 represent wire bonds of different lengths. Test structure A has the shortest wire bonds while test structure D has the longest wire bonds. Table 2.12 shows the TDR measured parasitic inductances. As can be seen the longer the bond wire the larger the parasitic inductance.

	TDR Test Results	Distance of Wires
A	4.8nH	3.9
B	7.5nH	4.5
C	8.0nH	5.6
D	11.6nH	6.75

Table 2.12: Parasitic inductance of bond wires of different lengths.

Copper traces 1 and 2 are used to measure the parasitic inductance and the results are summarized in Table 2.13. As can be seen trace 2 has a smaller parasitic inductance compared to trace 1 because it has a larger width. For both traces 1 and 2, a longer length yields a larger parasitic inductance. These results are verified by Q3D extractions.

	8mm	**14mm**	**20mm**	**28mm**
Trace 1 Test Result	6.35nH	10.2nH	14nH	25nH
Trace 2 Test Result	4.6nH	7nH	10nH	16nH

Table 2.13: Parasitic inductance of DBC substrate of different lengths and widths

Hence, TDR measurements verified the Q3D extracted parasitic inductances for copper interconnect and wire bond structures commonly used in power electronic modules.

Chapter 3. Design and Packaging of a Power Electronic Module

3.1. Design Parameters of a Power Electronic Module

Power electronic modules have many applications. In this thesis, a 1200V 450A silicon carbide (SiC) half-bridge module for electric vehicle application was designed and fabricated. The module is layout with the constraint to fit into an existing silicon insulated-gate bipolar transistor (IGBT) half-bridge module package for a direct footprint replacement in an electric vehicle inverter drive. The ratings for both the SiC power MOSFETs and diodes are 1200V at 50A. As such, many of these devices must be paralleled to provide the required current handling capability. Figure 3.1 is the circuit topology of the power module. It consists of an upper (or high-side) switching position and a lower (or low-side) switching position. Each switching position consists of 15 SiC power MOSFETs in parallel with three SiC diodes in anti-parallel position. The SiC anti-parallel diodes are to provide reverse current conduction when the anti-paralleled power MOSFETs are switched off. The module was designed to operate at a junction temperature of 200^{o}C. According to the date sheet provided by the manufacturer [7-8], the current carrying capability of the SiC power MOSFETs is de-rated to 30A at 200^{o}C. This is the reason that 15 SiC power MOSFETs are chosen. Since the SiC diode is capable of carrying a 50A current at the junction temperature of 200^{o}C, only nine of them are required. Thus, the switching position is rated at 450A at 200^{o}C.

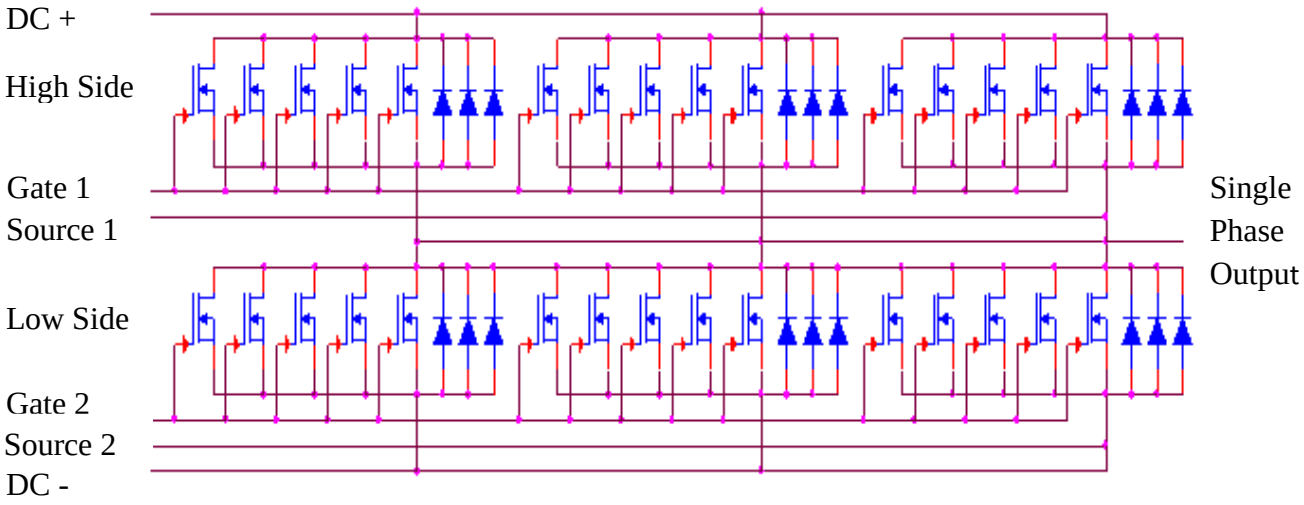


Figure 3.1: 600V/450A SiC MOSFET circuit schematic for 50KVA electric vehicle.

The power substrate for the module is chosen to be a direct bonded copper (DBC) substrate. The power substrate area is 96mm × 32mm to fit into the existing module package. In order to minimize the thermal and mechanical stresses, the power substrate is separated into three identical pieces to be electrically connected by wire bonding. Each of these power substrates, 38mm x 32mm, has 5 SiC MOSFETs and 3 SiC diodes attached for both the high-side and low-side switching positions. The dimensions for the SiC power MOSFET are 4.08mm × 4.08mm while the dimensions for the SiC diode are 8.23mm × 4.08mm. Table 3.1 summarizes the parameters of the power devices.

	Manufacture number	Die size	Source pad size	Gate pad size	Thickness	Anode pad opening
MOSFET	CREE CPMF-1200-S080B	4.08mm × 4.08mm	0.98mm ×2.09mm (×2)	0.84mm ×0.6mm	365μm	N/A
Diode	CREE CPW2-1200S050	4.02mm × 8.23mm	N/A	N/A	387μm	3.22mm ×7.41mm

Table 3.1: Dimensions of the SiC MOSFET and diode [7-8].

The module package has an outside dimension of 152mm × 62mm as shown in Figure 3.2. The inside cavity is 96mm x 38mm. The housing provides electrical terminal connections and gate control pins for the module. The positive and negative power supply terminals are placed at the right side of the housing, and the two load connections are placed at the left side of the module. There are

seven pins located on the both sides of the housing for the control signals. In this design, the module package size is the limiting factor. The layout needs to be as symmetric as possible to reduce the power losses. The other issue is the thermal performance. Due to the size and form factor of the power substrate, the base plate may bend due to mismatch in thermal coefficient of thermal expansion of different interface layers of the module.

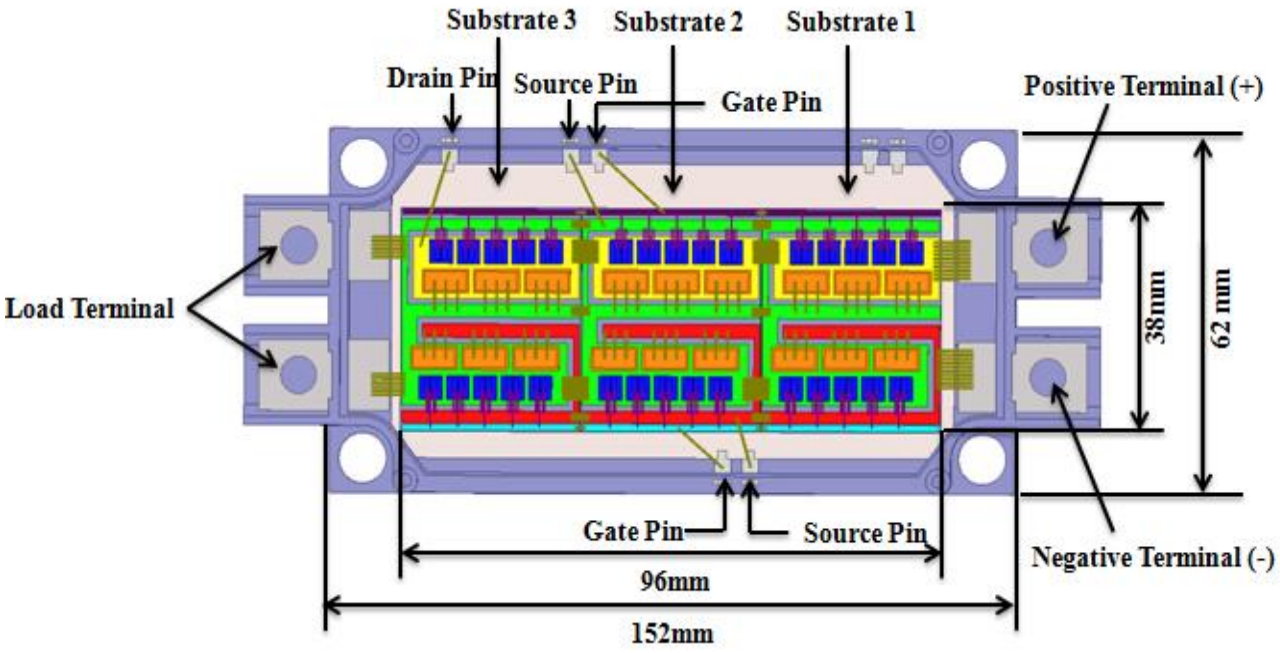


Figure 3.2: Package and power substrate of the module.

3.2. Design Considerations - Current Sharing

Unbalanced current sharing of power semiconductor devices can occur with improper layout. This happens when some of the powers MOSFETs are conducting a larger share of the total current. This can happen because of the differences in the intrinsic parameters (such as $r_{ds\ (on)}$) of the power MOSFETs or external parameters such as differences in parasitic circuit elements due to layout. Unbalanced current sharing can lead to having different power losses on the paralleled power devices which may lead to undesired module performance. The current sharing of the paralleled power semiconductor devices will be considered.

For a half-bridge switching position, there are two states of operation. When the top side switching position is switched on, a current of 450A is flowing from the right positive terminal to the left load terminal connections. Figure 3.3 shows the current flow through different impedances on the common source for each of the power substrate. When the upper switching position is switched off and the bottom switching position is switched on, the 450A current is flowing from the left load terminals to the right negative terminal. Figure 3.4(A) and 3.4(B) show the current flow directions for the high-side switching position and low-side switching position, respectively.

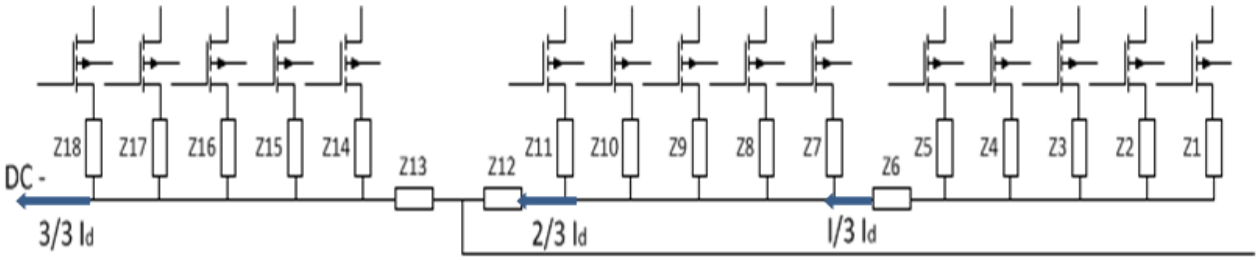


Figure 3.3: Current flow on the common source conductor.

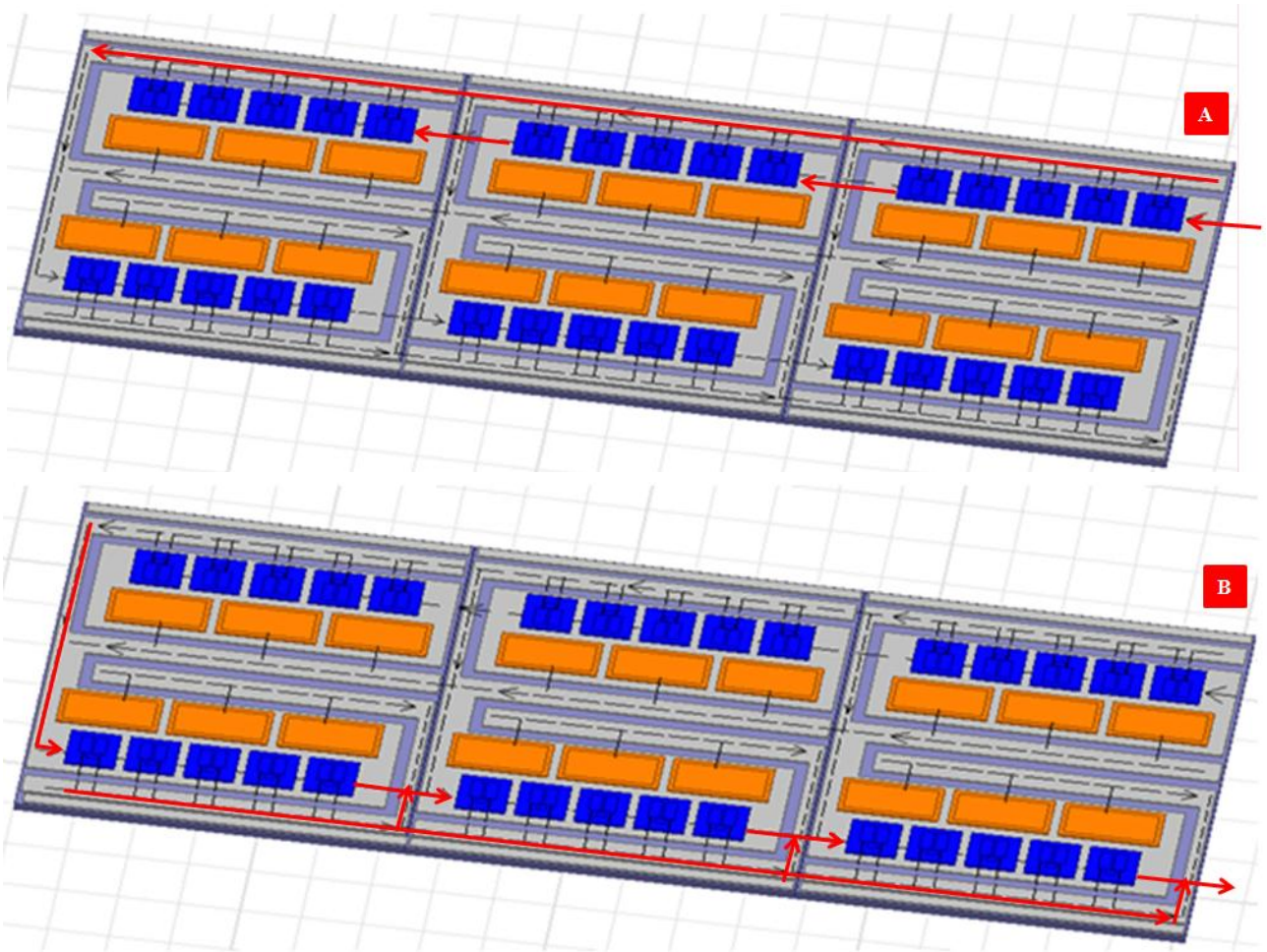


Figure 3.4: Current flow for the (A) high-side and (B) low-side switching positions.

3.3. Simulation of Current Vector

The current sharing simulation is performed using the ANSYS Q3D simulator. The source and sink are the inlet and outlet for the current flow in Q3D simulation. For these simulations, a current of 450A is injected into the source terminal and this current exists from the sink terminal. From these current flow vector simulations, the current distribution for the upper and lower switching positions are almost similar. This means that the current is equally shared by the fifteen power MOSFETs in both the upper and lower switching positions because of the symmetrical layout of these power MOSFETs. In general, the current density is low, about 1.43×10^5 A/m. The current density is higher for the copper traces where the wire bonds connect to the sink and source areas for

both the high-side and low-side switching positions. Since the current accumulates from the source to the drain, the drain side has the highest current density, as can be seen in the low-side switching position.

3.4. Resistor Network Analysis

According to Ohm's law, the current is the ratio of the voltage divided by the resistance. Hence, the voltage across the parallel string of power semiconductor devices is the same. So, the current in each string depends on its equivalent resistance. Since the conduction path will include copper traces and wire bonds, their equivalent resistance may not be similar. In order to keep the same impedance in each parallel path, it must contribute an equal amount of parasitic circuit elements. Thus, the copper traces and number of bond wires and their lengths must be the same.

The path lengths for the two side and middle power substrates to the supply terminals are different because of the placement of the power connectors. Thus, each of these three power substrates would have different parasitic resistances. Figure 3.5 shows a resistive network for the power substrates. A voltage source represents the voltage for each paralleled path. From the left side of resistor network shown in Figure 3.5(A), the equivalent resistances of the fifteen paralleled MOSFETs are represented by Rm while Rp represents the path resistance connecting these power MOSFETs. The currents that flow into each MOSFET are represented by I1 to I15 sequentially. In Q3D simulation, Rm is equal to $45\,\mu\Omega$ and Rp is equal to $40\,\mu\Omega$.

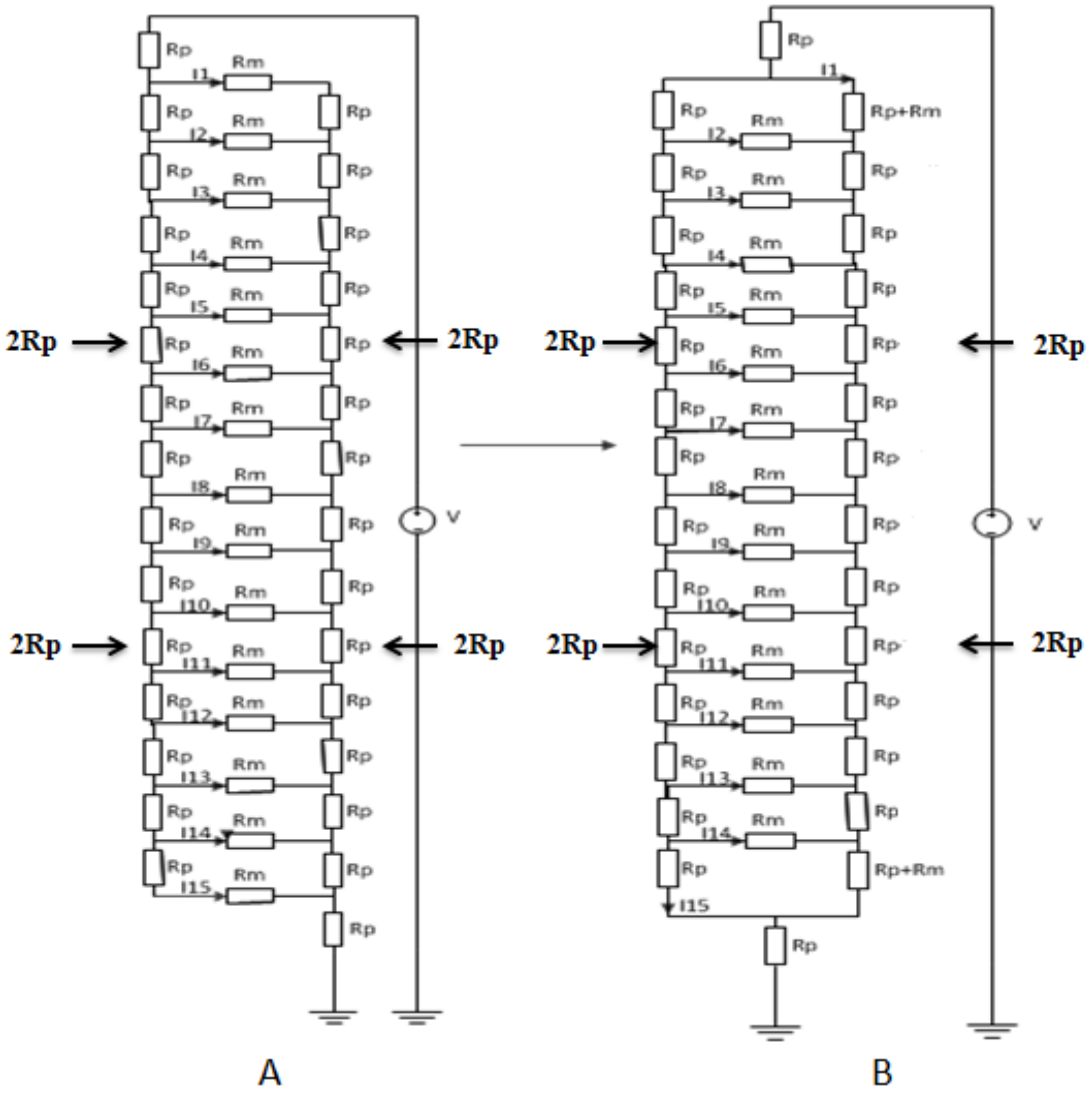


Figure 3.5: Resistive network representation of the paralleled MOSFETs.

As can be seen from Figure 3.5(A) the equivalent resistances for each paralleled path are not the same. The main reason is that Rp is not the same for each of these 15 SiC MOSFETs. As mentioned earlier the power substrate is separated into three identical power substrates, each with 5 SiC MOSFETs, in order to mitigate thermal and mechanical stresses. These three identical power substrates are connected by wire bonds which give rise to a higher parasitic resistance. It was found that the Rp between the three power substrates is 80μΩ while the Rp within each power substrate is

40μΩ. By a simple re-drawing of the resistive network, the resistive network of Figure 3.5(B) shows different turn-on resistances for the SiC power MOSFETs.

A different layout scheme, the star-connection, will be discussed later. This layout can mitigate current imbalance but it is not usually realizable due to the size limitation and special packaging requirements.

3.5. Conduction Loss

Power losses in power modules consist of conduction losses and switching losses. Only conduction losses will be discussed since switching losses depend on the power electronic topology. Conduction loss is given by $P = I^2R$ where I is the drain current of the MOSFET and R is the equivalent resistance during conduction. From Q3D simulations of the high-side and low-side switching positions shown in Figure 3.6, the high-side switching position has an equivalent resistance of 0.92mΩ while the low-side switching position has an equivalent resistance of 0.88mΩ. With a conduction current of 450A, the conduction losses for the high-side and low-side switching positions are 186W and 178W, respectively. In order to minimize the conduction losses the diameter of bond wires should be considered. Table 3.2 shows the conduction losses using different wire bond diameters for the connection between the power devices as well as the power substrates. The result shows the conduction loss is significantly reduced if a larger bond wire diameter is used. The conduction loss is 270W if a bond wire diameter of 0.38mm is used while the conduction is reduced to 180W if a bond wire diameter of 0.15mm is used.

Wire Bond Diameter (devices to the pads)	0.15mm	0.38mm
Conduction loss (High Side)	270W	184W
Conduction Loss (Low side)	274W	178W

Table 3.2: Conduction loss simulation results.

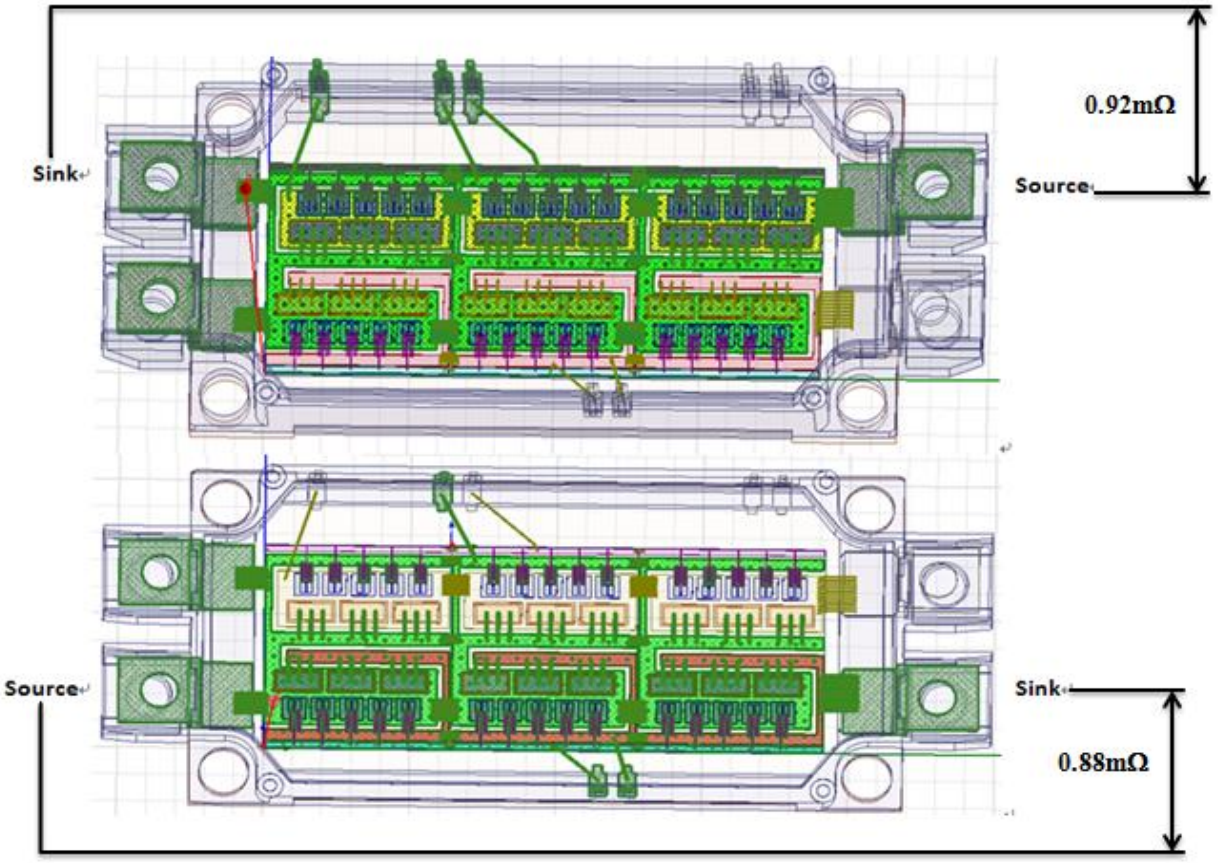


Figure 3.6: Conduction and parasitic Q3D simulation for high-side (top) and low-side (bottom).

3.6. Parasitic Extraction

Parasitic circuit elements affect the performance of switching positions in power electronic systems. The main parasitic inductances are gate loop inductance, switch loop inductance, and the common source inductance. The mitigation methods described in the previous Chapter will be used to minimize the parasitic inductances. The objective is to minimize the parasitic inductance of the power module. TDR measurements will be used to verify the parasitic inductance in the power module.

3.6.1. Parasitic Extraction of a Single Switching Position

According to Figure 3.2, there are three identical power substrates each consists of 5 power MOSFETs and 3 SiC diodes for the upper and lower switching positions in the power module. Parasitic extraction is first performed for one of these three identical power substrates. There are

five parts contributing to the parasitic inductances and resistances. These are the DC+ bus path inductances (DC+ terminal connection and high-side auxiliary drain), MOSFET and diode wire bonds inductances, gate loop inductances, common source inductances, and DC- bus path inductance (Low-side common source and DC- terminal connection). Table 3.3 summarizes these parasitic inductances and resistances for one of these power substrates as shown in Figure 3.2.

Parasitic Path	**Parasitic Inductance**	**Parasitic Resistance**
DC+ terminal path (+ to yellow)	8.8nH	0.28mΩ
High-Side MOSFET wire bonds	2.3nH	0.45mΩ
Low-Side MOSFET wire bonds	2.5nH	0.46 mΩ
Diode wire bonds	2.6nH	0.46mΩ
Gate wire bonds	5.8nH	11.2mΩ
High side common drain path (yellow)	12.4nH	0.13mΩ
Gate1 loop (purple)	27.2nH	5.3mΩ
Gate 2 loop (light blue)	22.2nH	4.1mΩ
High-Side common source (middle green)	11nH	0.8mΩ
Low-side common source (middle red)	12nH	0.9mΩ
DC- terminal path (- to red)	8.1nH	0.28mΩ

Parasitic Extraction	Phase to Phase wire bonds connection				
	High-side Drain	Common Source	Low-side Source	Gate 1	Gate 2
Stray inductances	2.3nH	6.5nH	1.8nH	1.7nH	1.9nH
Resistance	0.2mΩ	0.71mΩ	0.22mΩ	0.8mΩ	0.85mΩ

Table 3.3: Q3D parasitic extraction for a single switching position.

As can be seen the low-side and high-side siwtching positions have slightly different parasitic circuit elements. Figure 3.7 shows the parasitic inductance model for the high-side and low-side switching positions.

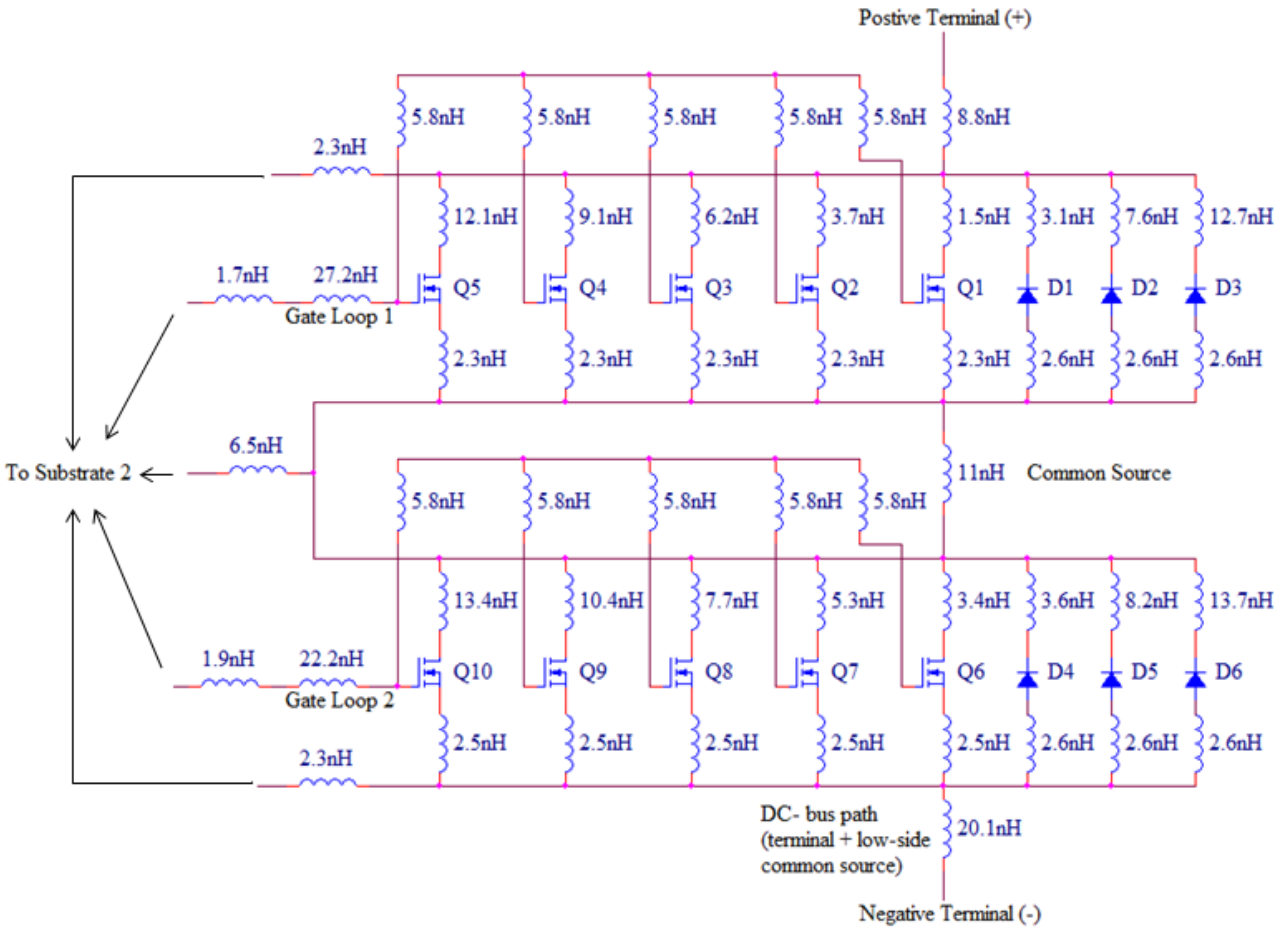


Figure 3.7: Parasitic model for the high-side and low-side switching positions.

As can be seen the gate loop parasitic inductance is larger than other parasitic inductances. The main reason is due to its longest current path. The other is due to the use of only one bond wire for the gate connection. This is because the size of the gate pad is 0.84mm×0.6mm which can only accommodate one bond wire. The length of the gate bond wire is also determined by the gate pins on the module package.

The length of the current path contributes to the most parasitic circuit elements for the module. Since the interconnection distance is different for each MOSFET and diode, their parasitic circuit elements are different. These differences in parasitic inductances affect current sharing for these power MOSFETs. A similar situation occurs at the wire bond connections for the power MOSFETs and diodes. Due to the different sizes for the power semiconductor devices, different number of bond wires can be used to make the interconnections, as such, the parasitic circuit elements are different. These bond wires can contribute a parasitic inductance from 1.5nH to 5.8nH. The common source pad contributes a parasitic inductance of 13nH. The total contributions for the wire bonds and DBC copper traces are about the same. Therefore it is necessary to extract the parasitic circuit elements for the whole module.

3.6.2. Parasitic Extraction of the Switching Positions for the Whole Module

Since the three power substrates are identical, it is only necessary to to consider one of the three identical power substrates. Because of the consideration of the whole module, the simulated current path is different from the previous section as shown in Figure 3.8. When the high-side switching position is switched on, current is flowing from the positive terminal at the upper right-hand side of the module package to the drain terminals of the upper switching position. The parasitic inductances for each of the power substrate is different because of the different lengths of the copper trace from the source terminals to the load terminal at the left hand side of the module package.

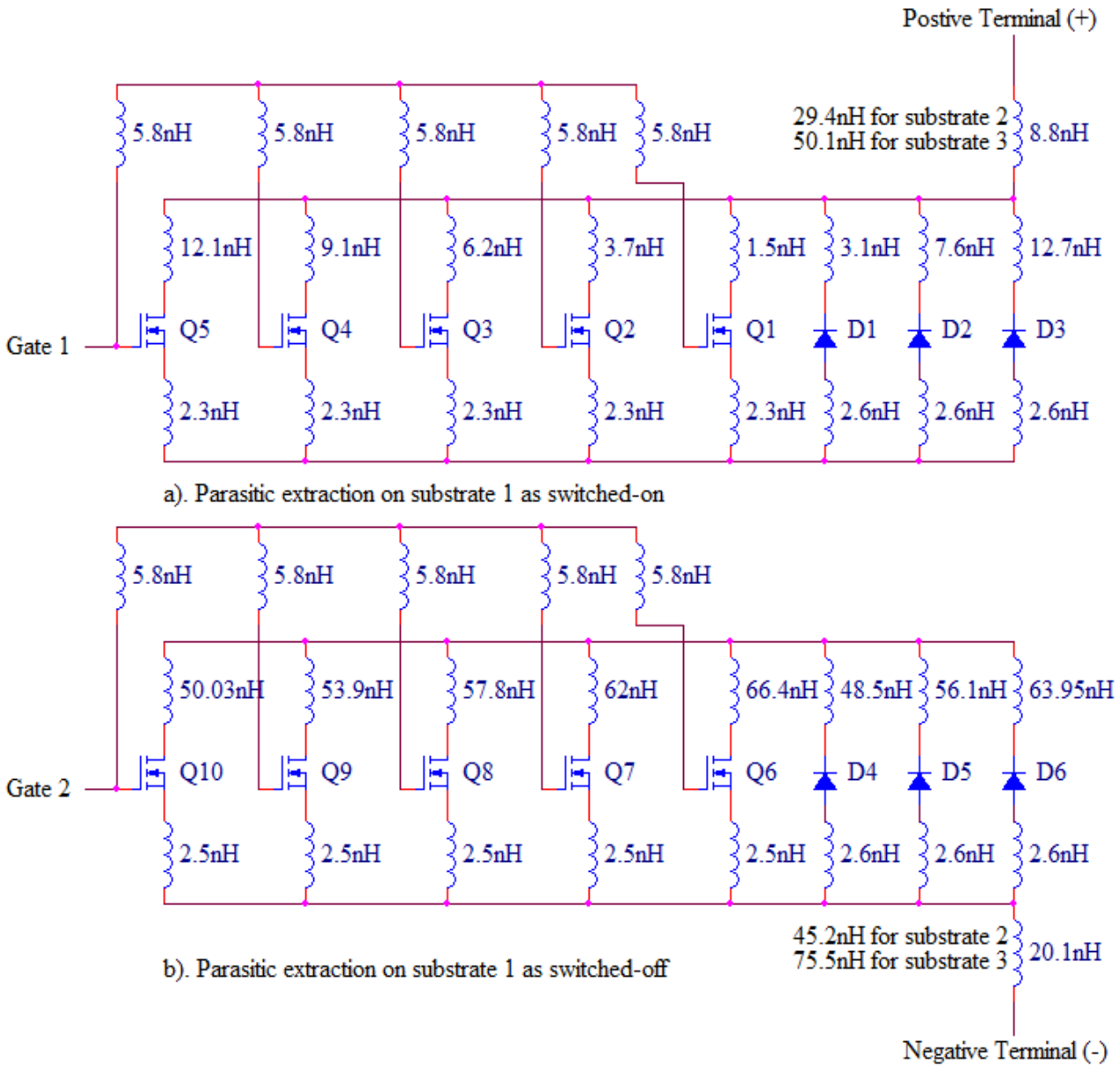


Figure 3.8: Parasitic extraction of substrate 1 in the entire module.

When the upper switching position is switched on, the current is flowing from the positive terminal on the upper right hand side of the module package to the load terminal located on the right side of the module package. Because of the differences in length of the current paths from each of the power substrates to the load terminal, their parasitic inductances will be different. For power substrate 1 as shown in Fig. 3.2, the parasitic inductance from the positive terminal to the drain terminal is 8.8nH. Similarly, the parasitic inductances for power substrates 2 and 3 are 29.4nH and

50.1nH, respectively. When the lower switching position is switched off, the current is flowing from the load terminal to the negative terminal on the lower right side of the module package. As such, the parasitic inductances from the load terminal to the drain terminals of each of the power substrates will be different. For power substrate 1, the parasitic inductance from the negative terminal to the drain terminal is 20nH. Similarly, the parasitic inductances from the negative terminal to the drain terminal for power substrates 2 and 3 are 45nH and 75.5nH, respectively.

3.7. TDR Verification of Parasitic Inductances

TDR is used to measure the parasitic inductances of the power substrate in order to verify the parasitic inductances from the Q3D simulations. Figure 3.9 shows the single power substrate for the 5 power SiC MOSFETs and 3 SiC diodes. The common drain pad for the high-side switching position is shown as yellow while the common drain pad for the low-side switching position is shown as green on the bottom part of the power substrate. Table 3.4 shows the parasitic inductances from the Q3D simulation and TDR measurement.

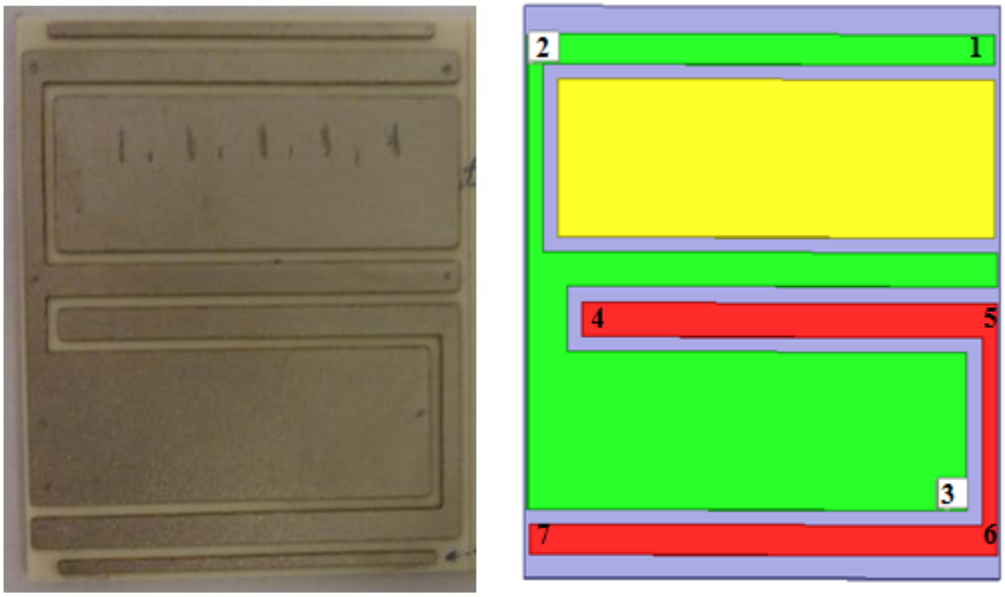


Figure 3.9: Single power substrate for 5 MOSFETs and 3 diodes.

Cases	Source to Drain	TDR	Simulation
Case 1	1 to 2	26nH	23nH
	2 to 3	32nH	31.8nH
	Top Gate Path	20nH	22nH
	Bottom Gate Path	27nH	27nH
Case 2	4 to 5	22nH	19nH
	5 to 6	12.7nH	11.3H
	6 to 7	26nH	22.8nH
	4 to 7	39.5nH	43.6nH

Table 3.4: Parasitic inductance for the single power substrate.

As can be seen from Table 3.4 the measured TDR parasitic inductances match those from Q3D simulations. For example, the parasitic inductances for the common source copper trace for the upper switching position which is shown as point 2 to point 3 in Figure 3.9 are 32nH and 31.75nH from TDR measurement and Q3D extraction, respectively. The parasitic inductance for the current path for the lower switching position's common source is low due to its unique current flow pattern shown in red color on Figure 3.9. Obviously parasitic inductance cancellation occurs for this common source current path as it wraps around the return drain current path in the middle. When the current flows through point 5 to point 6 its parasitic inductance is reduced by approximately 25%. As the current passes through points 4 to 7, the parasitic inductance reduces from 60.7nH to 39.5nH. The 60.7nH parasitic inductance is calculated by adding the total parasitic inductances from points 4 to 5, 5 to 6, and 6 to 7. As such, it is possible to mitigate the parasitic inductances by carefully considering the current return paths in power electronic modules.

3.8. Interconnected Power Substrates

The three power substrates are interconnected on a copper base plate. The function of the base plate is to hold these three power substrates to enable them to be interconnected as well as to aid in heat spreading. Two cases are considered. First, four 5-mil bond wires are used to perform interconnection between all the interconnection sites on the power substrates. Second, 12 5-mil bond wires are used to interconnect the common drain pad between the power substrates in addition to the interconnections made in the previous case. In both cases the structure is first simulated by Q3D to extract the parasitic inductances. Then, TDR is used to verify the simulated results.

Figure 3.10 shows the three power substrates interconnected by bond wires in six locations. Figure 3.11 shows the colored current paths for the high-side and low-side switching positions. The simulated and test points are labeled as points 1 through 6. Table 3.5 lists the Q3D extracted and TDR measured parasitic inductances. As the length of the current paths increases, the measured parasitic inductance increases as shown by the increase in parasitic inductance from 32nH from point 1 to 2 to 56nH from points 1 to 6.

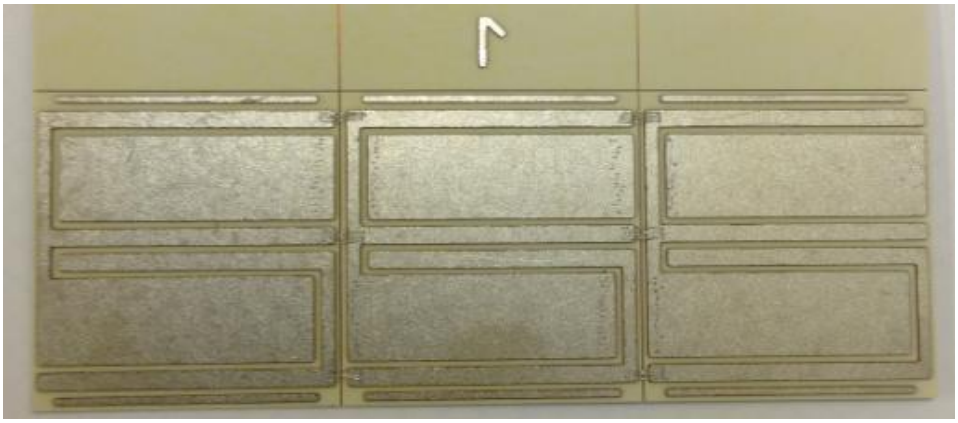


Figure 3.10: Interconnected power substrates on a base plate.

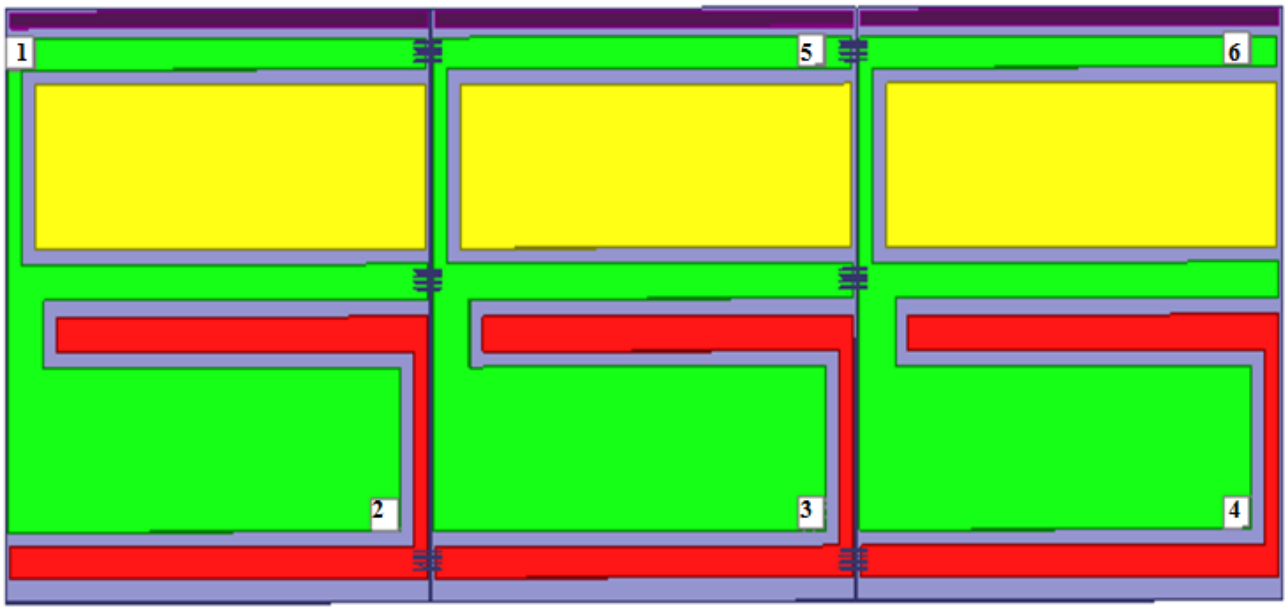


Figure 3.11: Simulated and test points for interconnected power substrates.

Parasitic Inductance	Test Structure	Simulation
1 to 2	32nH	29nH
1 to 3	45nH	46nH
1 to 4	62nH	72nH
1 to 5	42nH	40nH
1 to 6	56nH	73nH

Table 3.5: Parasitic inductances of the interconnected power substrates.

In the second case, 12 5-mil bond wires are used to interconnect the common drain pads between the power substrates in addition to the previous wire bond connections as shown in Figure 3.12. Table 3.6 lists the parasitic inductances extracted by Q3D and measured by TDR measurements. As can be seen, the parasitic inductance reduces 7.4% to 24% from Q3D extraction compared to the decrease of 4% to 19% from TDR measurements.

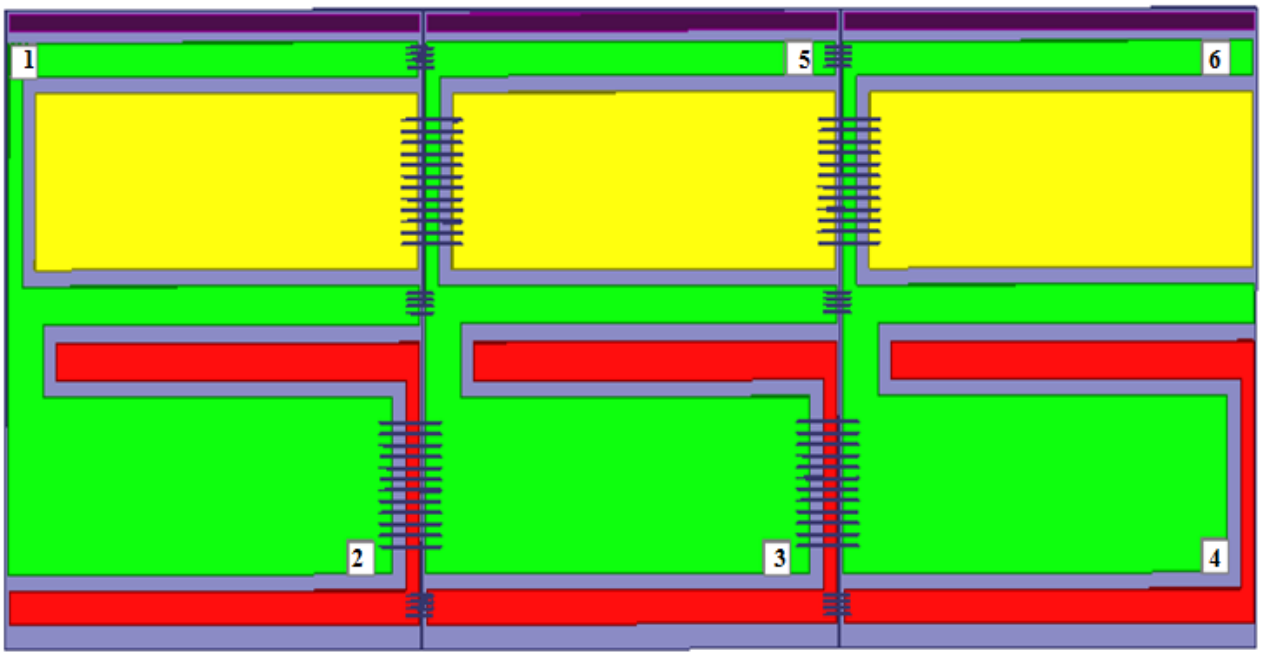


Figure 3.12: Interconnected power substrates with interconnected common drain pads.

Parasitic Inductance	Test Structure	Simulation
1 to 2	30nH	22nH
1 to 3	39nH	37nH
1 to 4	55nH	61nH
1 to 5	42nH	36nH
1 to 6	59nH	68nH

Table 3.6: Parasitic inductances of interconnected power substrate shown in Figure 3.13.

In the layout for the high-side common source and low-side common drain pads, a reduction in parasitic inductance is observed. As can be seen from Table 3.6 the parasitic inductances for the common drain paths are 30nH (points 1-2), 40nH (points 1-3), and 60nH (points 1-4). So, when the high-side switching position is switched off, the current flows from the load terminals to the negative terminal through the low-side switching position. The large differences of parasitic inductances as

the current flows through each power substrate may make the current sharing for the three power substrates a bit challenging.

3.9. Star Layout Design

Conventional 3-phase inverter power module for electrical vehicles uses 6 Si IGBTs and 6 diodes as the switching devices. The Si IGBT has a dimension of 13.5mm×13.5mm while the Si diode has a dimension of 10mm × 10.0mm. The power rating for the module is 450A at 600V. Figure 3.13 shows the circuit topology of the 3-phase inverter. Most design layouts are for square or rectangular power substrates. A star layout is proposed and is shown in Figure 3.14.

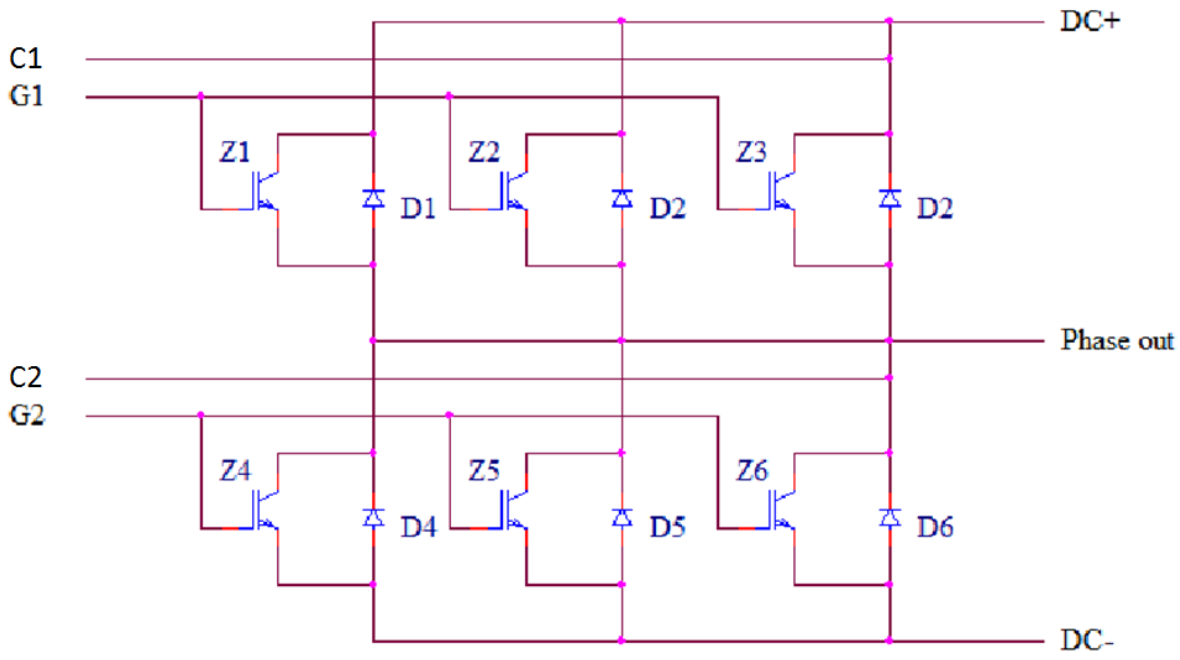


Figure 3.13: Conventional IGBT switching position.

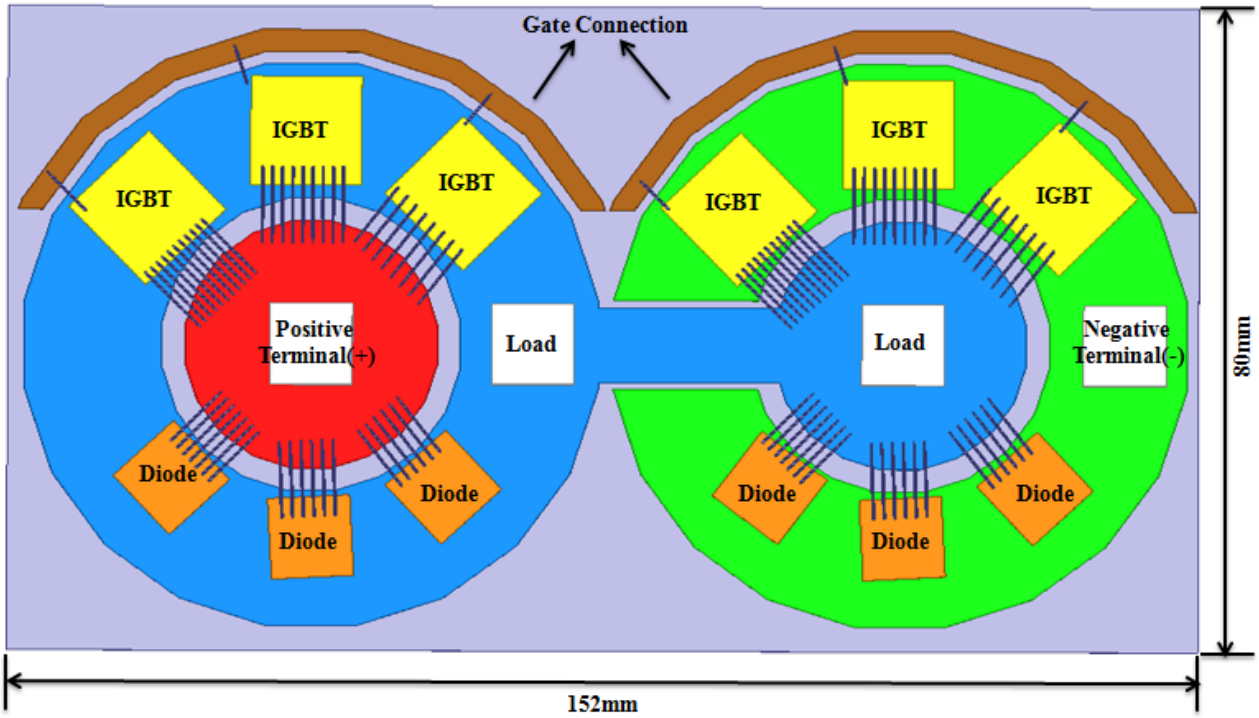


Figure 3.14: Star layout configuration for the module.

The advantage of this star layout is the equal distance from the power terminals to the emitter pad of each device. The layout is symmetrical. The circle on the left is the high-side switching position while the right circle is the low-side switching position. The major disadvantage is the large area needed for the module. There are plenty of waste spaces on the power substrate as well. The star layout yields an area of 152mm × 86mm compared to an area of 152 mm × 62mm for the conventional rectangular layout. The disadvantage is the wasted area due to the round structure of the star layout configuration. The gate wire bond from each device has to be over the common emitter electrode. The difference in the areas of the positive and negative supply terminals may cause some electromagnetic interference (EMI) concerns.

The star layout module was simulated using Q3D. Similar simulation parameters were used. Table 3.7 lists the Q3D simulated results.

	Switched-on	Switched-off
Parasitic inductance	12.7nH	14.8nH
Resistance	0.11mΩ	0.11mΩ
Calculated Conduction Loss	22.3W	22.3W

Table 3.7: Simulation results of star layout design.

The main goal of the star layout design is to achieve the same parasitic influence for both the high-side and low-side switching positions. To achieve this, the positive and load terminals must be located in the center of the module. However, in order to create a perfect symmetrical layout, the load terminal is moved from position X to the middle of the power module to achieve a similar current path from the high-side and low-side switching positions. In this way, the current is shared equally. Table 3.7 lists the parasitic circuit elements and conduction losses for the star module. As can be seen the parasitic inductances for the low-side and high-side switching positions are 14.8nH and 12.7nH, respectively. The difference in parasitic inductance is only 3.1nH. Table 3.8 lists the parasitic inductances for the conducting paths. The parasitic inductance from the collector terminal to the IGBT 1, 2, 3 and diode 1, 2, 3 for the high-side switching position is 7nH. However, the parasitic inductances from the load terminal to IGBT 4 and diode 4, IGBT5 and diode 5, or IGBT 6 to diode 6 are all larger than 7nH. However, these parasitic inductances are much smaller than the parasitic inductance for the rectangular layout module.

	Parasitic Inductance
High-side: collector terminal to IGBT 1,2,3 and diode 1,2,3	7.1nH
Low-side: Load terminal to IGBT 4 and diode 4	7.7nH
Low-side: Load terminal to IGBT 5 and diode 5	10.6nH
Low-side: Load terminal to IGBT 6 and diode 6	13.8nH

Table 3.8: Simulation result for the niche of star layout design

3.10. Fabrication of the power module

The fabrication of the power substrate starts with the cleaning step. This is a very critical first step to ensure the quality and reliability of the power module. Copper is selected as the material for the base plate due to its high thermal conductivity. Direct bonded copper is selected as the power substrate. The DBC power substrates and copper base plate are first cleaned in an ultrasonic bath using a 10% hydrochloric acid in water. After clean and dry, the power substrates and base plate are nickel plated immediately. The thickness of nickel must be in the range of 2-5μm. The plated nickel is to prevent the copper from oxidation during further processing as nickel oxidizes easily after exposure in the air environment. Nickel also increases the corrosion resistance of the DBC. The copper trace on the DBC power substrate is then patterned using a dry film process. The nickel and copper are etched using a ferric chloride solution. Thus, current conducting paths are formed on the DBC substrate. Next, the power substrates are diced into individual pieces. Power semiconductor devices are attached onto the DBC power substrates using a fluxless and void-free soldering process. A vacuum furnace with an inert ambient is used to anneal the tin-silver-copper (SAC 405) solder alloy preforms. Figures 3.16 and 3.17 show the temperature profile and pressure profile for the solder attach process. As shown a peak temperature of 275℃ is needed to achieve a successful attachment. The pressure is needed to yield void-free solder attach. Graphite fixture is used to hold the power semiconductor devices to prevent them from moving during the vacuum annealing process. Figure

3.18 shows the fixture design. Next, the copper base plate is attached using a solder alloy that has a lower melting point than the die attach. After this, wire bonds are used to connect the power semiconductor devices to the copper traces. A 5mil bond wire is used to connect the gate electrodes while multiple 15 mil bond wires are used to connect the source electrodes of the power MOSFETs to the copper traces as shown in Figure 3.15. Last but not least the assembly is placed inside a plastic module housing. Encapsulation is then dispensed and cured to protect the power module from environmental factors and handling. Figure 3.19 shows the module after completion of the process. As can be seen, the module consists of 30 SiC MOSFETs and 18 SiC diodes.

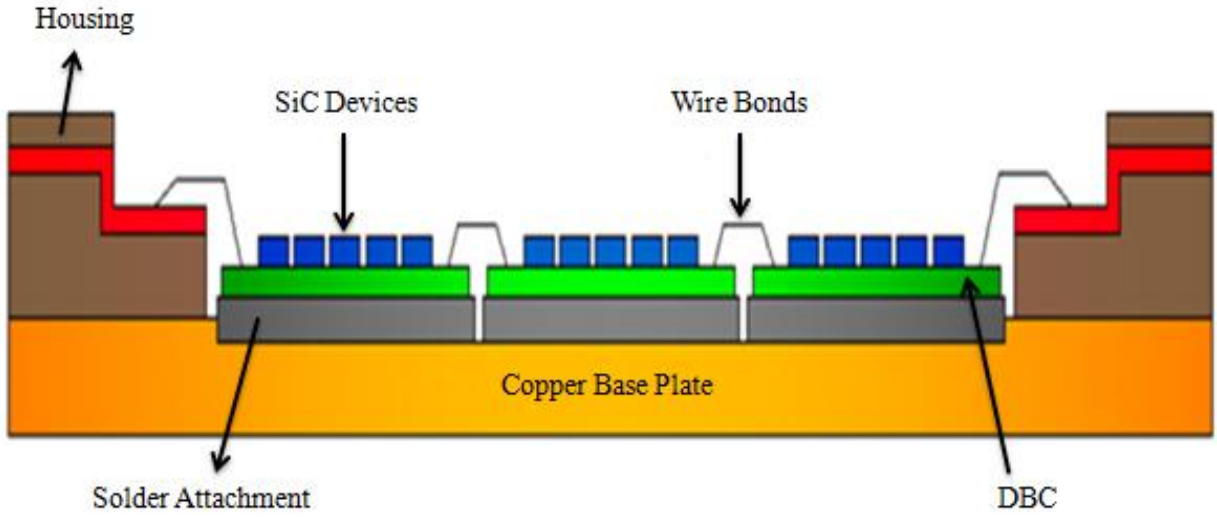


Figure 3.15: A cross section view of the power module.

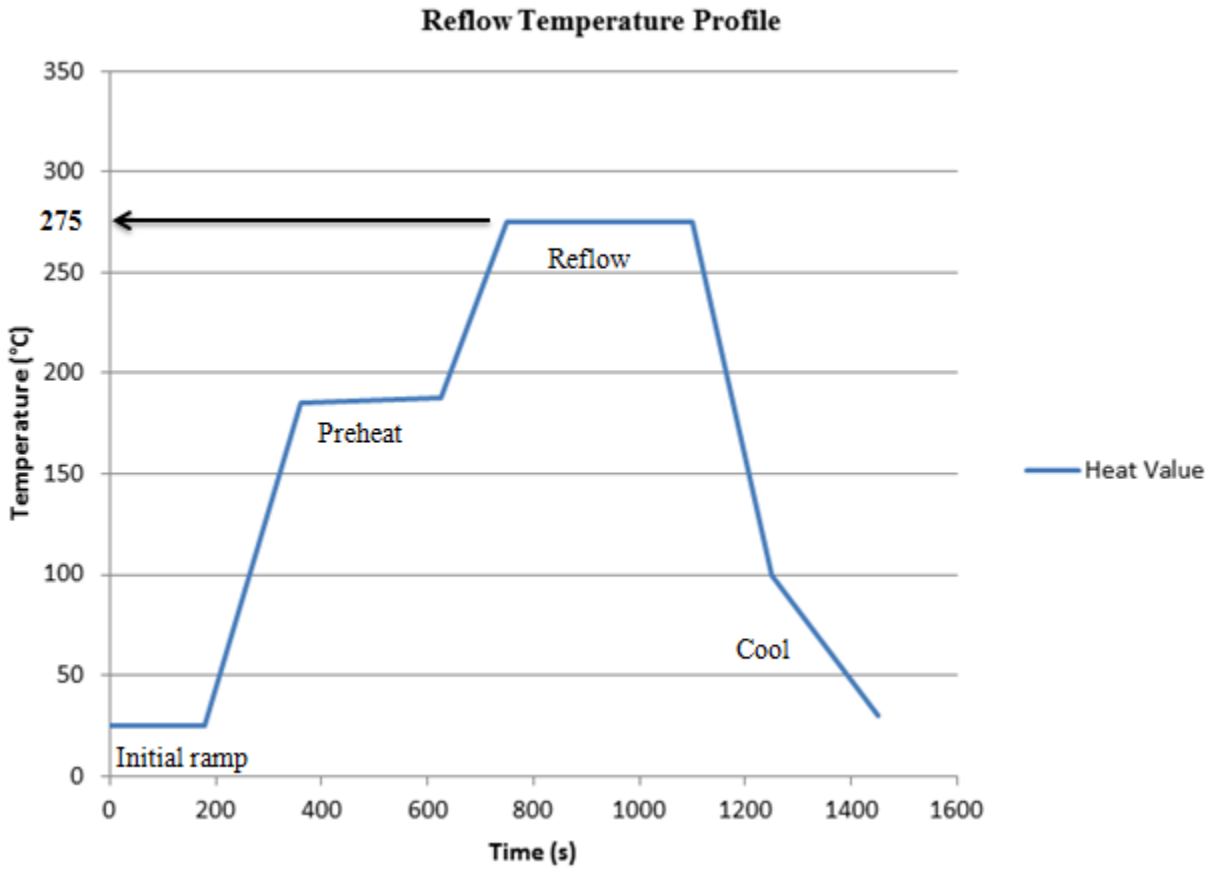


Figure 3.17: Temperature profile for die attachment of the power module.

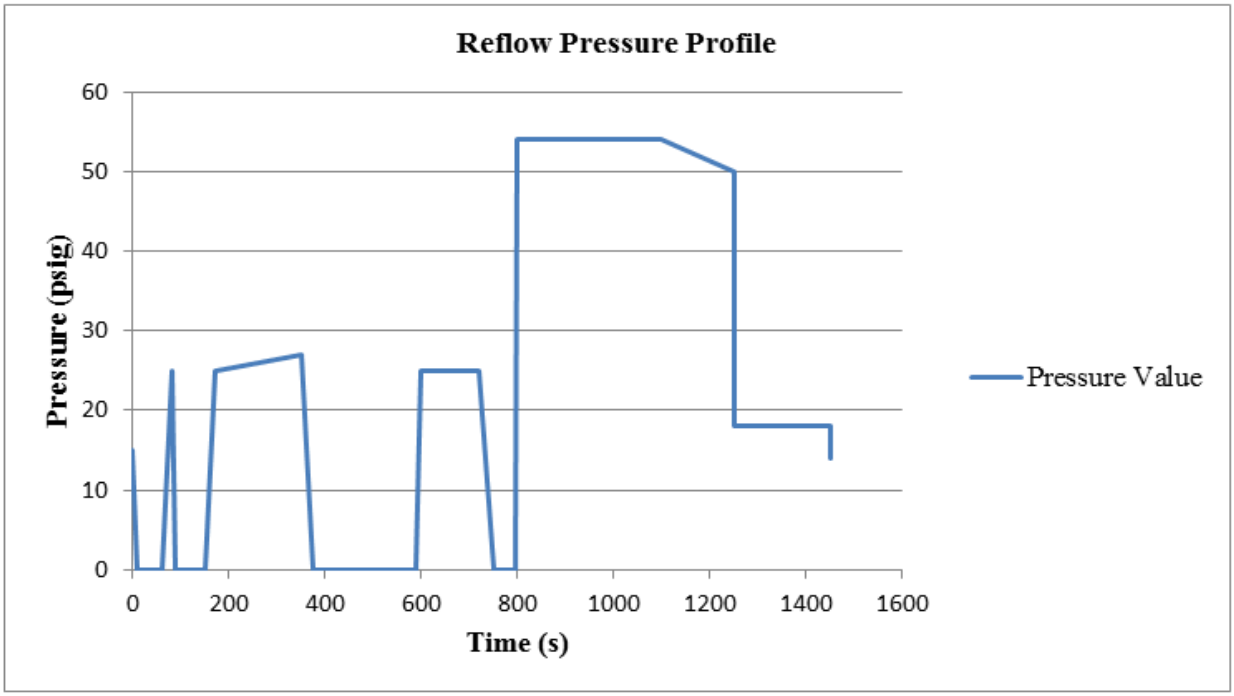


Figure 3.18: Pressure profile for die attachment of the power module.

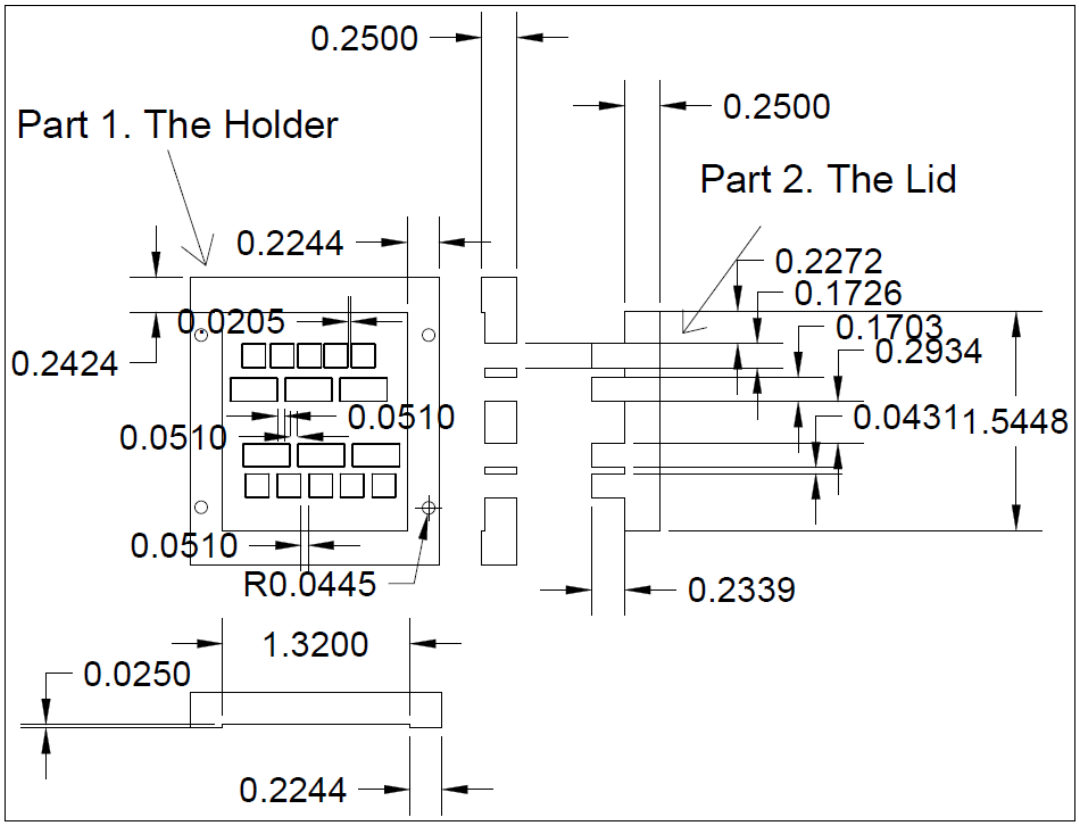


Figure 3.19: AutoCAD fixture design of the power module.

Figure 3.20: Fabricated power module.

Chapter 4. Conclusion

Parasitic circuit elements are unavoidable in power electronic modules. These parasitic circuit elements produce unwanted power losses and degrade the switching performance. The design and parasitic mitigation of power electronic module is investigated in this thesis research. Both Q3D extraction software and TDR measurements were used to determine the parasitic inductance contributions of the current conduction paths and wire bonds. The parasitic inductances from both the Q3D extractions and TDR measurements were very similar. A half-bridge 1200V, 450A switching position using SiC devices was designed and fabricated. The layout of this power module was constrained by the module housing. The parasitic inductances of the power module substrates were measured by TDR, and compared to those simulated values by Q3D Extractor. Due to the differences in the lengths of current paths for the power module substrates, the parasitic circuit elements for the three paralleled SiC power modules, each consisting of 10 SiC power MOSFETs and 9 SiC diodes, were different.

In future work, the current sharing of individual power device in a power module should be investigated and their electrical characteristics due to the differences in the parasitic circuit elements should be investigated. The star layout scheme, with further refinement, should be further investigated.

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