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THE DEVELOPMENT AND PACKAGING OF A HIGH-DENSITY, THREE-PHASE, SILICON CARBIDE (SIC) MOTOR DRIVE

THE DEVELOPMENT AND PACKAGING OF A HIGH-DENSITY, THREE-PHASE, SILICON CARBIDE (SIC) MOTOR DRIVE

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering

By

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University of Arkansas
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ABSTRACT

Technology advances within the power electronics field are resulting in systems characterized by higher operating efficiencies, reduced footprint, minimal form factor, and decreasing mass. In particular, these attributes and characteristics are being inserted into numerous consumer applications, such as light-emitting diode lighting, compact fluorescent lighting, smart phones, and tablet PCs, to industrial applications that include hybrid, electric, and plug-in electric vehicles and more electric aircraft. To achieve the increase in energy efficiency and significant reduction in size and mass of these systems, power semiconductor device manufacturers are developing silicon carbide (SiC) semiconductor technology.

In this dissertation, the author discusses the design, development, packaging, and fabrication of the world's first multichip power module (MCPM) that integrates SiC power transistors with silicon-on-insulator (SOI) integrated circuits. The fabricated MCPM prototype is a 4 kW, three-phase inverter that operates at temperatures in excess of 250 °C. The integration of high-temperature metal-oxide semiconductor (HTMOS) SOI bare die control components with SiC power JFET bare die into a single compact module are presented in this work. The high-temperature operation of SiC switches allows for increased power density over silicon electronics by an order of magnitude, leading to highly miniaturized power converters.

This dissertation is organized into a compilation of publications written by the author over the course of his Ph.D. work. The work presented throughout these publications covers the challenges associated with power electronics miniaturization and packaging including high-power density, high-temperature, and high-efficiency operation of the power electronic system under study.

This dissertation is approved for recommendation
to the Graduate Council.

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 ACKNOWLEDGMENTS

Thanks first to my family for helping me through the last several years to achieve my goal of obtaining a doctoral degree. Thanks to my wife Anne and daughters Hannah, Ella, & Lydia for standing by me and supporting me. Thanks to my parents for teaching me the value of hard work and education and for always being there for me in whatever endeavor I take on.

I would like to thank my good friend Alex Lostetter for being an inspiration, a great leader, and great mentor. Without your help and support this goal of achieving a doctoral degree would not have happened. Thanks to my friends and co-authors; Sharmila Mounce, Brice McPherson, and Edgar Cilio, you have helped and have been an instrumental part in my research. Thanks to all at Arkansas Power Electronics International, Inc. for your help and encouragement.

Thanks to my advisor, Dr. Alan Mantooth, for your leadership and for supporting my research goals. Thanks to my other committee members, Dr. Alex Lostetter, Dr. Rick Couvillion, Dr. Simon Ang, and Dr. William Brown, for being there for me when I needed assistance. Additionally thanks to Dr. Kraig Olejniczak for your mentorship, for getting me started in graduate school, and for helping read through and edit this dissertation.

Finally, I give my appreciation to God and country for giving me the opportunities that have so greatly blessed my life and the life of my family. I'm humbled by the grace of God and his presence in my life. I'm grateful for the opportunity to live in the Unites States of America and for the freedoms that I have and enjoy from being a citizen of this great land.

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[1] J. Hornberger, A. B. Lostetter, K. J. Olejniczak, T. McNutt, S. M. Lal, and A. Mantooth, "Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments," in the Proc. of the IEEE Aerospace Conference, vol. 4, pp. 2538 – 2555, March 2004.

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Drive Module," in the Proc. of the 38th IEEE Power Electronics Specialists Conference (PESC 2007), vol. 1, pp. 1048 – 1053, June 2007.

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CHAPTER 1

INTRODUCTION

Since the first silicon carbide (SiC) Schottky diode was introduced to the commercial market in 2001 [1], there have been many research facilities and commercial entities that have put forth much effort to bring to life SiC power electronic devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs), junction field-effect transistors (JFETs), bipolar junction transistors (BJTs), and gate-turn-off (GTOs) thyristors. As a wide bandgap material, SiC has many enhanced capabilities over state of the art silicon (Si) power devices. For example, when compared to Si, SiC can operate at higher temperatures (up to 600 °C), higher switching frequencies (10-100 times), has decreased energy losses (1/10th), has a higher breakdown voltage (10 times that of Si), and is capable of higher current densities (3-4 times higher than Si) [2]. Together with the advantages of SiC and the advancements made to fabricate SiC power devices, the power electronics industry is undergoing a technology revolution where power electronic systems and applications can see an order of magnitude decrease in size and weight with a simultaneous increase in performance.

Applications that can benefit from SiC are widespread and all-encompassing in the area of power electronics. Some of these applications include, but are not limited to, electric motor drives for hybrid electric and electric vehicles; motor drives and power converters for aircraft, spacecraft, and space exploration vehicles; power converters for solar power, wind power, and geological exploration; and solid-state circuit breakers and current limiters for industrial electric transmission, distribution, and smart grid systems. Ultimately, any system that would see improvement from high-density, high-efficiency, or high-temperature power electronics would benefit from SiC.

While significant effort has been dedicated to bringing these new SiC power electronic devices to life, resources to develop systems with SiC as well as the power electronic packaging that fully enable the benefits of SiC have been lacking. The work presented here by the researcher represents efforts to advance state of the art power electronic systems through the development of circuits, applications, and power electronic packaging.

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CHAPTER 2

RESEARCH DIRECTION

The goal of this research is to advance the field of power electronics by utilizing SiC power devices; to reach this goal there have been many steps and milestones achieved along the way. This dissertation is portrayed in the format where research goals, milestones, and results are discussed throughout several publications. Figure 2.1 depicts the path of the author to reach the ultimate goal of developing the world's first SiC multichip power module (MCPM) motor drive with integrated control capable of high-temperature operation above 250 °C.

The first goal was to develop a controller capable of three-phase operation and transition the design to high-temperature components. This work was conducted in the author's master's work [3].

The second goal was to transition the control circuitry to high-temperature components and to demonstrate controller operation at high temperature. The description of research relating to this second goal is described in [4-6].

After implementation of the controller at high temperature, the third goal was to implement the MCPM concept with a single-phase, low-power demonstrator transitioning from packaged board-level components to an integrated bare die form. This single-phase MCPM, research milestone three, is discussed in [6-8].

The fourth research milestone was to transition from a single-phase MCPM demonstrator to a three-phase, low-power MCPM demonstrator. Results for fabrication and testing of this demonstrator are discussed in [8, 9].

The fifth goal was to develop the fully-integrated final design of the high-temperature MCPM, and to test it for high-power operation in a single-phase implementation of the module. The results of this fifth research milestone are discussed in [9-11].

Finally, the fully-integrated, high-temperature, three-phase MCPM prototype was implemented at high-power and shown operational to > 250 °C. The results of research milestone six are discussed in [11-13].

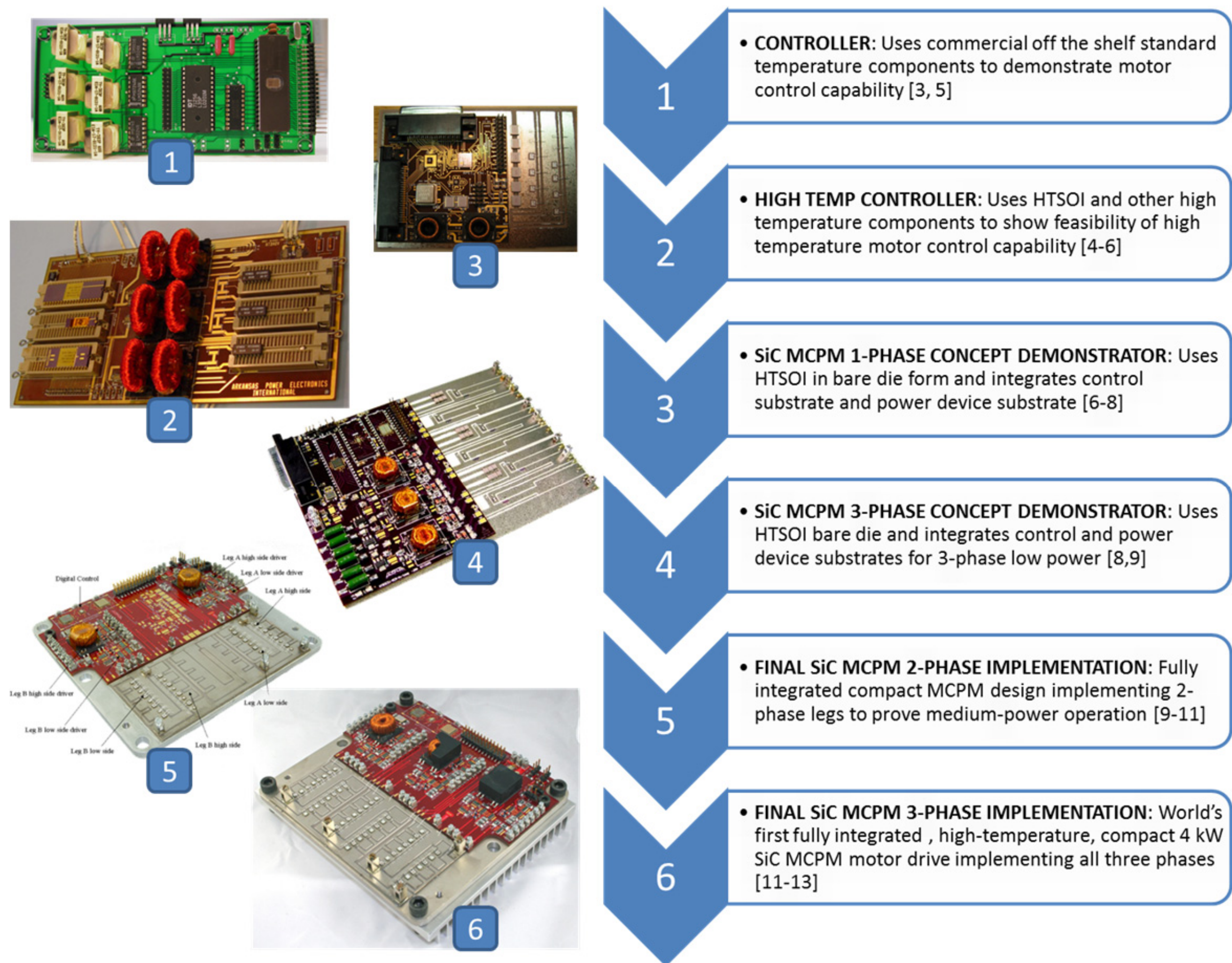

Figure 2.1: Research milestones achieved through the course of developing a high-temperature three-phase motor drive from concept to tested prototype.

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CHAPTER 3

SILICON-CARBIDE (SIC) SEMICONDUCTOR POWER ELECTRONICS FOR EXTREME HIGH-TEMPERATURE ENVIRONMENTS

J. Hornberger, A. B. Lostetter, K. J. Olejniczak T. McNutt, S. Magan Lal, and A. Mantooth

© 2004 IEEE. Reprinted, with permission, from Hornberger et al, Silicon-Carbide (SiC) Semiconductor Power Electronics for Extreme High-Temperature Environments, IEEE Aerospace Conference, March 2004.

ABSTRACT

This paper will discuss the current state of SiC electronics research at Arkansas Power Electronics International, Inc. (APEI) with regard to high-temperature environments and applications. The University of Arkansas (UA) researchers' modeling and characterization of SiC power devices for these high-temperature environments will also be discussed. Devices to be covered include SiC Schottky diodes, SiC power MOSFETs, and SiC static-induction-transistors (SITs). The paper will review the current application of these devices to the specific harsh environments of deep Earth drilling and combat electric vehicles, as well as outline APEI's research work into developing operational SiC motor drives for these systems. It is proposed that this technology development be transferred to NASA space exploration applications. Two areas within the NASA program that would find this technology highly beneficial are (1) probes and landers that must operate in high-temperature environments and (2) ultra-lightweight power electronics for satellite and spacecraft power converter systems.

1. INTRODUCTION

The past decade has seen an intense and steady increase into the research of the viability of SiC–based device technology. This technology has the potential to improve upon many of the

current limitations associated with silicon electronics, in particular, the limitations of silicon device switching speeds, junction temperatures, and power density.

The team of researchers from APEI and the University of Arkansas specialize in the development of silicon and silicon-carbide power electronics for harsh environment applications, including silicon Systems on a Chip (SoC) DC-DC converters for NASA-JPL, silicon-carbide motor drives for deep Earth geological exploration, and silicon-carbide motor drives for the U.S. Army Future Combat Systems (FCS) hybrid-electric combat vehicle program. The researchers are proposing to map over the developing silicon-carbide power electronics technology to the arena of space electronics and/or solar system exploration. There are two areas within the NASA program that would find this technology highly beneficial.

The first NASA area that would benefit from SiC technology is very specific. It is envisioned that SiC electronics would be of great benefit to probes and landers that must operate in high-temperature environments, such as the Venusian atmosphere. Venus' upper atmosphere is composed of a high concentration of sulfuric acid, and the surface environment exceeds temperatures of 460 °C at 92 bars of pressure. Silicon-carbide electronics could be used to drive small actuators and DC motors required to move robotic arms, spin soil drills, or drive the wheels of a Venus rover. Normal silicon electronics, even in a heavily shielded environment, would fail in a matter of hours under such conditions. This paper will present the idea that it is conceivable that SiC electronics could operate in the surface environment for an extended period of time with *little to no shielding or protection at all*. A lander's electronics composed exclusively of SiC would function days or weeks before failure, instead of hours, thus greatly increasing the scientific data acquisition capability of the overall system.

The second NASA area that could benefit from this technology, required on almost every piece of space hardware ranging from high–power solar array and fuel cell supplies to low-voltage (3.3 V or 2.5 V) digital electronics, are DC-DC power electronics energy converters. Silicon-carbide power electronics have the potential to bring about enormous cost savings. SiC power switches, with reduced switching losses, would improve the overall electrical efficiency of onboard systems. The ability to operate at high junction temperatures would greatly reduce the size and weight of heatsinking strategies (by as much as an order of magnitude or more). The ability to switch at higher frequencies would result in large reductions in the size of capacitor, inductor, and magnetic components (again, perhaps by as much as an order of magnitude). Implementing these changes in conjunction with a modular (or building block) strategy similar to the U.S. Navy's power electronic building block (PEBB) program, with built in "intelligence," would result in easy-to-build, easily cascadable, power electronics systems with improved reliability and 1/10th the size and weight of today's design solutions. Reduction in size and weight means immediate savings in cost to launch, and improving modularity translates to a reduction in complexity, which again results in cost savings.

It is evident from these two applications alone that silicon-carbide electronics not only could map over to NASA functions, but due to NASA's specific and unique requirements, would become an excellent driver for cost savings and improved scientific exploration.

2. Silicon-Carbide

The utilization of discrete high-power SiC devices is set to revolutionize the power electronics industry and bring the benefit of improved efficiency, improved reliability, and reduced costs to the commercial markets. The 2001 European Power Electronics Conference in

Graz, Austria, was an unveiling: the world's first commercial SiC power diodes were made available to the private sector [1].

SiC is a wide bandgap semiconductor material capable of high temperature operation (theoretically up to ~600°C) [2]. When compared to silicon-based devices, SiC devices (e.g., Schottky diodes, *pn* diodes, static-induction-transistors, and power MOSFETs) possess a higher breakdown voltage (10 times that of Si), possess lower switching losses, are capable of higher current densities (approximately 3 to 4 times higher than Si or GaAs), and can operate at higher temperatures (approximately 5 times higher than Si) [4]. In short, SiC transistors have the potential to revolutionize the industry of power electronics.

The interests in SiC technology can be traced down to the comparison of the fundamental physics between it and silicon. First, as illustrated in Table I, SiC technology offers an order of magnitude higher breakdown electric field than Si. Higher breakdown electric field allows for thinner and more highly doped devices. Since a SiC device can be made thinner and doped higher, the diffusion length L, and lifetime τ are reduced, and faster switching speeds (up to 10s of GHz) can be achieved With a higher electric breakdown field, SiC can surpass the voltage limits reached by Si power electronic devices by an order of magnitude. SiC power devices also have increased switching speeds because saturated electron drift is twice that of Si. Another contributing factor to switching speeds is electron mobility which in SiC is actually less than in Si and is a disadvantage at low voltages. However, the effect of saturated electron drift is dominant over electron mobility in high voltage devices and the overall effect is an increase in switching speeds. Additionally, SiC transistors with faster switching speeds, smaller drive currents, and smaller on resistances will have reduced power losses and increased electrical efficiency over silicon devices.

Table I. Fundamental properties of various semiconductors [3].

Property	6H SiC	4H SiC	GaN	GaAs	Si
Energy Bandgap (eV)	2.9	3.26	3.39	1.43	1.12
Electric Field Breakdown (x106 V/cm @ 1kV operation)	2.5	**2.2**	3.0	0.30	**0.25**
Dielectric Constant	9.6	9.7	9.0	12.8	11.8
Intrinsic Carrier Concentration,ni (cm-3 @ Room Temp)	10-6	8.2x10-9	1.9x10-10	2.1x106	1010
Electron Mobility, μe (cm2/V·s @ Room Temp)	330-400	**700-980**	1,000 2,000 2DEG	8,500	**1,400**
Hole Mobility, μh (cm2/V·s @ Room Temp)	75	120	200	400	450
Saturated Electron Drift (x107 cm/s @ E >2x105 V/cm)	2.0	**2.0**	3.0	1.0	**1.0**
CTE (ppm/K)	4.5	5.1	4	5.73	4.1
Young's Modulus GPa	400	400	181	70	156
Thermal Conductivity (W/m K @ Room Temp)	490	**370**	130	55	**150**
Density (g /cm3)	3.2	3.2	6.15	5.3	2.3

The second major advantage of SiC electronics is their potential to operate in extremely harsh environments, and in particular high-temperature environments, due to the large bandgap. This ability to operate at high temperatures, coupled with the excellent electrical efficiencies, gives SiC the potential to operate at very high power densities not achievable with Si electronics. This ability leads one to the immediate recognition that power electronics would benefit greatly from the implementation of SiC devices. The current commercially available SiC devices are Schottky diodes, and recently SiC MESFETs. SiC PiN diodes, power MOSFETs, gate-turn-on-thyristors (GTOs), and static-induction-transistors (SITs) are all currently under development by research and manufacturing organizations (such as Northrop-Grumman, Infineon, Cree, Army research lab, and Rockwell Scientific), although none of these devices have yet been released into the commercial marketplace. The increasing development of SiC opens up a world of possibilities in electronics design and applications that hitherto have been unthinkable.

Improving SiC Technology

The first real interest in the use of silicon-carbide as an electronic substrate material dates back to the late 1950s, but it wasn't until the late 1980s and early 1990s that the research area truly began to gain momentum. This was when Nishino and Powell developed the heteroepitaxial growth of SiC crystals on Si substrates. The early and mid 1990s found the introduction of commercial grade SiC wafers of 4H-SiC and 6H-SiC polytypes [5].

The industry, however, is still plagued with unreliable and defective wafers, slowing much of the desired research in SiC device development. The two major reasons for crystal growth difficulties are: (1) conventional melt techniques (such as those used in silicon) cannot be utilized since SiC does not melt under reasonably attainable pressures and temperatures (SiC sublimes at temperatures above 1800 °C), and (2) different polytypes with different electrical characteristics can grow under identical conditions [6]. Current SiC wafers contain high defect densities, the most significant of which are tubular voids referred to as micropipes, which in turn limit the defect-free semiconductor surface area and thus the size of devices.

The current major areas of SiC development can be identified as follows:

1. *SiC wafer and substrate fabrication*—The key dominating issues here are in reducing the physical flaws and defect densities in the wafers (such as tubular voids and micropipes), and increasing wafer sizes for more cost effective fabrication.

2. *SiC physics and device development*—This means developing not only the theoretical design of SiC devices, but also the practical issues associated with layout and manufacturing processes and the building of the devices or ICs. Such issues that need improvement are ohmic contacts and strong dielectric oxide layers. One of the key steps in making discrete devices capable of withstanding high temperature is proper devices passivations.

3. *SiC device modeling*—The ability to develop and validate accurate device models is key in today's world of computer simulations. End users need to be able to simulate their circuit and system designs using device models or they are unlikely to apply the devices themselves.

4. *SiC packaging*—The key here is again high temperature. If the maximum high-temperature solder liquefies at 300 °C, then of what use is a 600 °C electronic device? The package not only has to operate at high temperatures but must be reliable as well if it is to be of any use. Currently, all areas of electronic packaging are highly deficient with regard to high-temperature operation and reliability.

5. *SiC applications*—Currently, the most promising applications are power-electronics systems and drives, RF modules, and simple sensors. The key here is the lack of availability of SiC devices. Without transistors on the commercial market, it is difficult to build and prove the application.

<u>SiC Semiconductor Devices</u>

SiC Diodes—Recently, silicon-carbide (SiC) power devices have begun to emerge with performance that is superior to that of silicon (Si) power devices. For a given blocking voltage, SiC minority carrier conductivity-modulated devices, such as a PiN diode, show an improvement in switching speed by a factor of 100 as compared to Si, while majority carrier SiC devices show a factor of 100 times less in resistance compared to Si [7]. Prototype devices have already demonstrated improvements over Si technology for devices of various current and voltage ratings. Because power rectifiers are more easily produced than three terminal power devices, they have become the first commercially available SiC power devices. Figure 1 shows the cross section of a SiC Schottky diode.

Generally speaking, there are three classes of SiC power rectifiers: (a) Schottky diodes, which offer extremely high switching speeds but suffer from high leakage current; (b) PiN diodes, which offer low leakage current but show reverse recovery charge during switching and have a large junction forward voltage drop due to the wide bandgap of 4H-SiC; and (c) Merged PiN Schottky (MPS) diodes, which offer Schottky-like on-state and switching characteristics, and PiN-like off-state characteristics [8]. It has been shown that a 1500 V SiC MPS diode provides superior performance over Si diodes with voltage ratings of 600 V to 1500 V [9], and that a SiC PiN diode has superior performance compared to Si diodes with voltage ratings from 1200 V to 5000 V [10].

SiC DiMOSFET— Until recently, there have been no SiC transistors on the commercial market. These devices however, are under research and development by several manufacturers, including Northrop Grumman, Cree, Infineon, and Rockwell Scientific.

SiC power MOSFETs are expected to have advantages over existing Si technology similar to that of the above-mentioned SiC diodes, and are attractive for implementation as high-voltage, high-speed power devices. Figure 2 shows the simplified cross section of the unit cell structure of a recently introduced experimental 2 kV, 5A SiC DiMOSFET that has fast switching performance [11]. The structure of the DiMOSFET is similar to that of the VDMOSFET used for Si power MOSFETs, in that the p-well and n^+ source regions typical of the VDMOSFET structure still exist in the DiMOSFET structure. The main difference between the two structures is that the DiMOSFET p-well and n^+ source regions are much shallower than those of a Si VDMOSFET due to the lower impurity diffusion coefficients inherent in SiC.

In the on-state region of operation, electrons flow laterally from the n^+ source through the MOSFET channel formed in the implanted p-well and then vertically between adjacent cells and

through the lightly doped drift layer to the drain contact. For a 2 kV Si MOSFET, the drift layer resistance dominates the on-resistance of the device, whereas the specific on-resistance is dominated by the channel resistance for the SiC DiMOSFET structure [11].

SiC Static-Induction-Transistor (SIT)—Power MOSFETs and Insulated Gate Bipolar Transistors (IGBTs) are normally-off devices and require positive voltage signals applied to the gate in order to turn the devices on into their forward conduction modes. On the other hand, SITs are normally-on devices and therefore require the application of a negative voltage signal to the gate in order to turn the device off. Figure 3 illustrates the structure of the SIT.

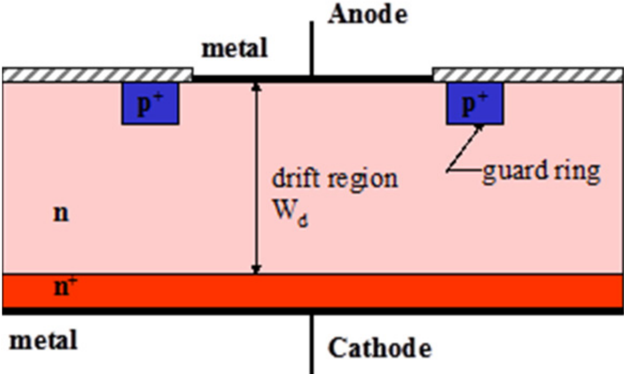


Figure 1. Cross section of SiC Schottky diode.

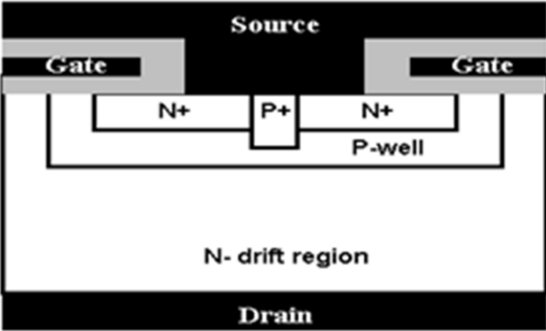


Figure 2. Cell structure for a 5 A, 2 kV SiC DiMOSFET

The SIT uses a recessed gate structure, where a large number of the source and gate regions are built up in parallel, thus allowing increased current flow through the device. The uniqueness of the SIT is that it can operate in both unipolar and bipolar modes, giving the user and applications engineer the choice between higher frequencies of operation or higher current sinking capabilities.

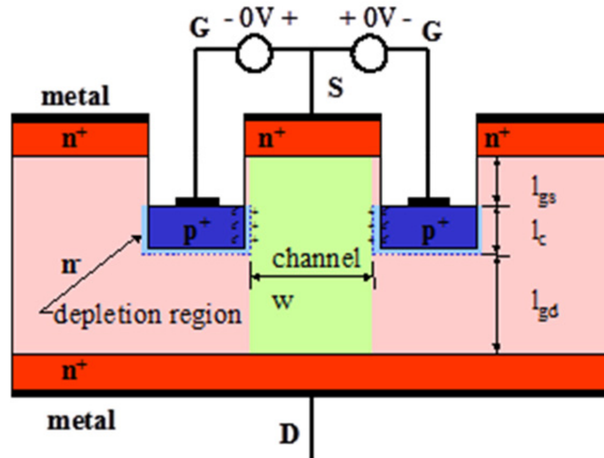


Figure 3. Cross- section of SIT structure

When 0 V is applied to V_{gs} of the device, the device is operating in its normally-on mode. In this mode, the drain and source are shorted through the n-type region. A small depletion region forms between the p^+/n^- interface, and the channel that forms has a width of the distance between the two depletion regions. When a voltage is applied between the drain and source, electrons flow from source to drain. The electrons are the majority carriers, and in this case, the only mechanism of current flow, and so the SIT is operating in a unipolar mode. The design of the SIT is optimized by minimizing the length of the channel l_c and the drain-drift region l_{gd}, while maximizing width and thus minimizing the on-resistance of the device.

As a negative voltage is applied to the gate with respect to the source, the depletion region of the pn-junction begins to grow. As the depletion region grows, the channel width is

reduced and the channel length is increased, thus restricting the flow of current while increasing the on-resistance. When a large enough reverse voltage is applied, the depletion regions grow to such an extent that they meet beneath the source, thus cutting off completely the flow of current.

Operating the SIT in the unipolar mode utilizes a similar control scheme as that developed for power MOSFET devices, since it is a voltage controlled device. The gate signal applied is 0 to V_t where V_t is positive for power MOSFETs and negative for SITs.

If more current handling capability is required however, the SIT can be operated in the bipolar mode, which increases power at the cost of complicating the gate drive and reducing switching frequency. This mode of operation can be achieved by applying a positive voltage signal to the gate with respect to the source. In this mode, the gate to source region is forward biased, thus essentially turning on the pn-junction (a diode) into conduction mode between the p^+ and the n^- regions. This effect injects holes into the main body of the semiconductor and the channel, thus reducing the on-resistance of the device. It is obvious that in order to inject holes from the gate, a significant current capability must be available from the gate source— thus it is no longer simply a voltage control, but also a current control. This greatly complicates possible gate drive schemes.

3. Current Work

Researchers at APEI, Inc. and the University of Arkansas have performed extensive research in the area of SiC device applications, packaging, and modeling for power electronic systems. Work reviewed in this section includes device control for SiC SITs, half-bridge SiC SIT power stages, and a 3-phase control board for operation up to 250°C for use with geological exploration and the Army's FCS vehicles. Packaging techniques of high temperature electronics and SiC is overviewed, as well as the modeling of SiC diodes, MOSFETs, and SITs.

Applications

The potential applications of SiC are widespread and all-encompassing in the area of power electronics. Military and space exploration vehicles are the first major applications that could significantly benefit from this technology. Control electronics and sensors of a jet or rocket engine that could be placed directly on or into the engine would be of great use. Also, a Venus probe could significantly benefit from SiC by being able to reliably perform experiments and collect data without failure soon after landing on the planet's surface. Additionally, the Army is looking for high power density motor drives for their hybrid-electric combat vehicles. Other high-performance applications to benefit would be nuclear power reactors, where sensors could endure the high-temperature and high-radiation environments; or petroleum and geological exploration, where electronics could be sent deep beneath the Earth in high-temperature bore-wells. Finally, any system that would see improvement from high-density motor drives would benefit from SiC.

Energy Exploration SiC Application—Energy companies are interested in SiC power electronics. Deep Earth exploration encounters hostile environments and extreme temperatures in which it is difficult to place silicon electronics. With SiC, it is possible to send electronics down-hole, thereby improving motor drive control and efficiency, increasing exploration and sensors' capabilities, and ultimately aiding in the discovery of previously hidden energy sources (such as large and wide, but shallow petroleum reservoirs).

APEI, Inc. is currently working in conjunction with Cole Enterprises on a Down Hole Orbital Vibrator (DHOV) that will integrate a high-temperature motor drive and a 3-phase induction machine for use in geological exploration. The DHOV is currently used in industry but has a few drawbacks. Current technology relegates the control and motor drive electronics to

operation on the surface. Developing the high-temperature technology would allow the integration of the electronics with the motor sources for use down-hole. Such a strategy would increase total power delivery capability and would enhance fine motor control (since the control electronics would not be located two miles away on the surface). These improvements would allow for higher accuracy and very fine mapping of the geological layers, thus greatly improving the chances of petroleum discovery. Figure 4 illustrates a 4 hp motor drive design developed by Cole Engineering, Inc. that is currently in production for petroleum industry clients.

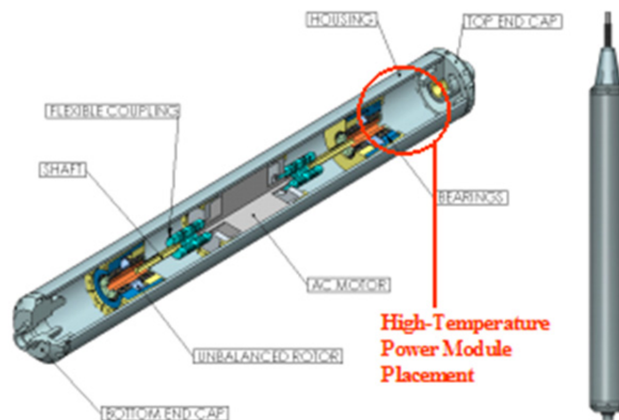


Figure 4. Down hole orbital vibrator for use with 3-phase 4 hp induction machine.

Current work under development by APEI, Inc. consists of miniaturizing the high-temperature control circuitry and combining it with SiC power switches (as shown in Figure 5) for placement inside the cylinder casing of the DHOV. The conceptualized drive would be a 2×2 inch square**.** Control components in bare die form would be mounted on a multi-layer substrate, such as polyimide or Rogers 4000, bonded on DBC with the power components. This multi-chip power module (MCPM) would miniaturize the 3-phase motor drive required by the DHOV and therefore will enable it to be placed inside the DHOV cylinder.

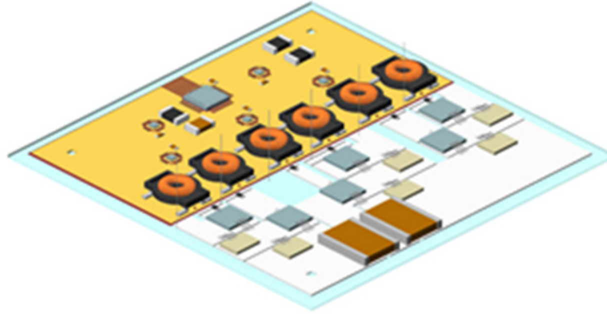


Figure 5. Miniaturized high-temperature control circuitry for DHOV.

SiC for military applications—The U.S. military is interested in SiC power electronics for use in their hybrid-electric combat vehicles, such as the Bradley Fighting Vehicle in Figure 6. These combat vehicles must utilize high-power converters and motor drives that are capable of operating within harsh environmental parameters. Due to their increased thermal abilities and increased power densities, high-temperature motor drives can be integrated onto the motors and bulky heatsinks can be eliminated. This saves both weight and space in the combat vehicle.

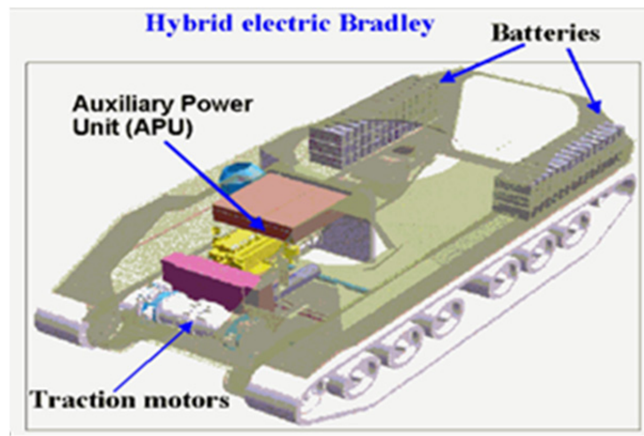


Figure 6. Hybrid-electric Bradley combat vehicle.

The researchers have designed, built, and tested control circuitry for use with SiC power switching devices for the specific application to the Army's Future Combat Systems (FCS). The circuitry consists of Honeywell's line of HTMOS high temperature microelectronics with the core of the control circuitry provided by the HT83C51 microcontroller. Honeywell's silicon-on-

insulator (SOI) HTMOS parts are guaranteed to operate at 225 °C for a period of five years and at 300 °C guaranteed for one year. Honeywell's tests have shown that after five years, there is a 99.6% reliability rate on components that have been operating at 225 °C.

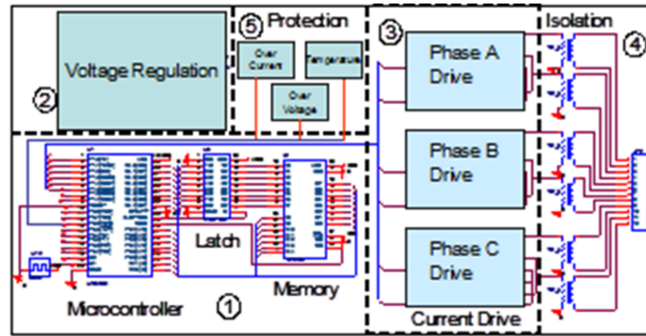


Figure 7. Block diagram of 3-phase controller.

The 3-phase controller consists of five main parts as shown in Figure 7.

(1) The core control consists of Honeywell's HT83C51 8-bit microcontroller. The microcontroller uses external RAM that is loaded with program memory before startup, thus increasing the versatility of the control algorithm.

(2) Next is the voltage supply regulation. Again, the HTMOS line supplies voltage regulators for 5, 10, or 15 V applications with an output current of 300 mA.

(3) Since the microcontroller is not capable of sourcing enough current to drive power devices, a current amplification circuit is implemented through the use of HT1104 operational amplifiers. Depending on what type of power switching device is used, this circuit will vary. A detailed circuit for driving SITs will be outlined later in this section.

(4) The isolation circuit serves three purposes; first to isolate the drive circuitry from noisy distortion caused by power switching, second to provide an increased gate drive capability

by doubling the voltage at its inputs, and third and most importantly, it allows for a floating voltage to be applied to the high-side power switch gates.

(5) Included with the control is protection from potential catastrophic failures such as over voltage, over current, and over temperature.

In order to complete the high-temperature prototype version of the control circuitry shown in Figure 8, passive components, such as capacitors, resistors, IC sockets, printed circuit boards (PCBs), and various other devices proper temperature ratings were utilized. Magnetic wire and high-temperature Magnesil toroidal core materials were utilized in the hand wound isolation transformers. High temperature burn-in zero insertion force (ZIF) sockets were used for all ICs in order to facilitate prototype testing and changes. High-temperature solders were obtained through Indalloy, and the high-temperature ICs were purchased from Honeywell.

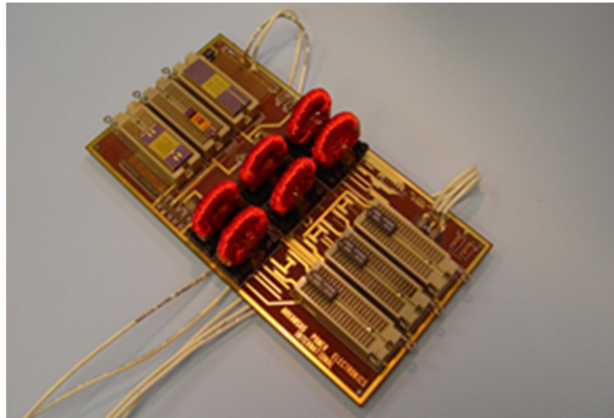


Figure 8 . 250 °C 3-phase motor control prototype.

High-temperature testing of the control circuitry was completed and proven to drive a 3-phase 4 hp induction machine under load. Figure 9 shows the control output of a single phase from the HT83C51 operating at 250 °C (Ch1 high side Ch2 low side).

Additionally, Figure 10 is the gate drive signal output from the isolation transformers operating at 250 °C with Ch1 as the microcontroller output, and Ch2 and Ch3 as the high and low side respectively.

The authors are also working with Northrop-Grumman to verify certain device electrical switching characteristics, to develop high-temperature technology for SIT packaging, and most importantly, to verify full SIT operation in an industry (as opposed to military) viable application. The authors built a SiC SIT power stage on an aluminum-nitride direct bond copper substrate (nickel plated) [12]. The devices were mounted with a high-temperature Indalloy solder. Figure 11 illustrates a photograph of the SIT half-bridge 200 watt power stage.

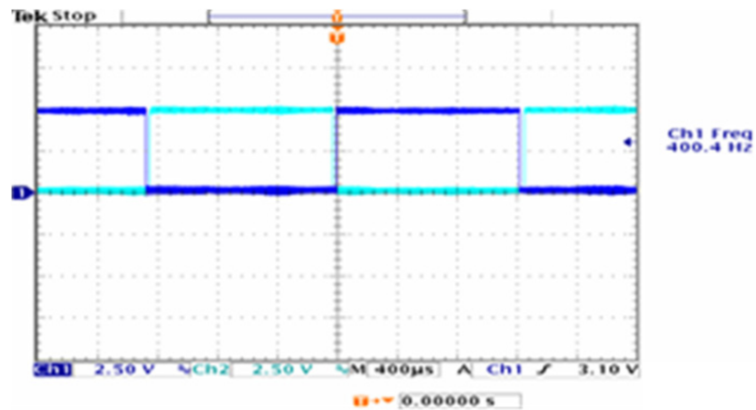


Figure 9. Output of HT83C51 operating at 250 °C

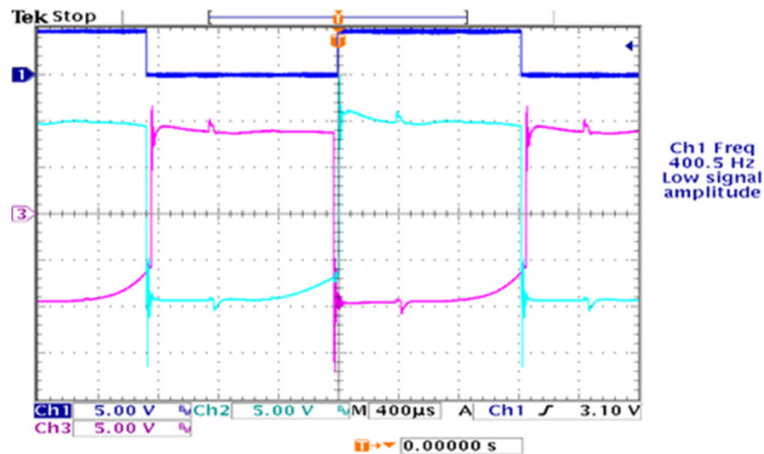


Figure 10. Output of transformers operating at 250 °C.

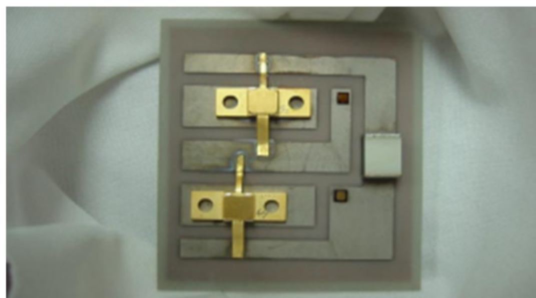


Figure 11. SiC SIT half-bridge.

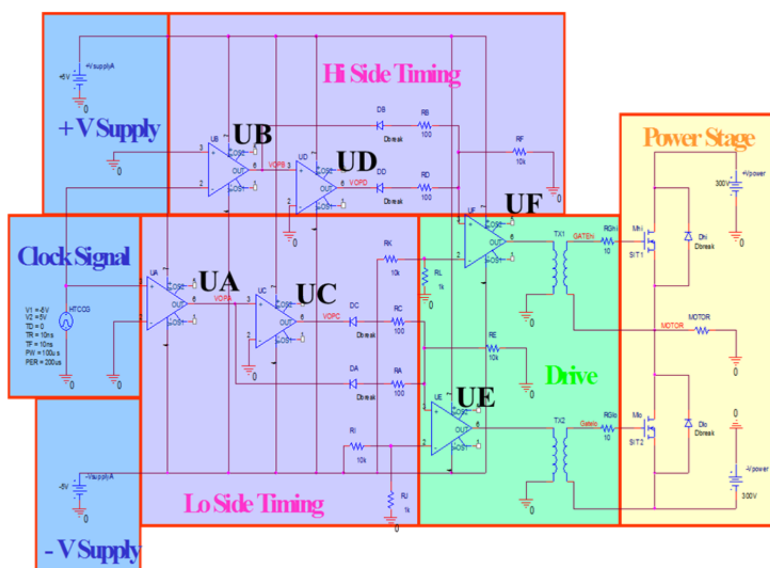


Figure 12. SiC SIT half-bridge control circuitry.

The drive circuit for the SiC SIT half-bridge was designed using Honeywell's HT1104 op-amps, and Cree SiC PiN diodes. The power half-bridge is composed of a high side and low side transistor, the gates of which are driven by respectively inverting control signals. In addition to the inversion, deadtime is required so both half-bridge power switches are off simultaneously for a short period of time.

Referring to Figure 12, the generated clock signal controls the ultimate timing of the pulse drive signal delivered to the high and low side transistor gates. The positive and negative voltage supplies are generated by high-temperature voltage regulators (Honeywell HTNREG and HTPREG).

Initially, the clock signal is fed in parallel to op-amps UA and UB (low side and high side timing, respectively). Op-amp UB is set up as a rail-to-rail inverter thus inverting the clock signal, while Op-amp UA is simply a delay to keep the two signals timed together. These signals are illustrated in Figure 13. It is important to note that even though the signals are inverted, there is no deadtime present in the control.

The next step is then to insert the appropriate deadtime. For this purpose, the output of op-amp UA is fed into op-amp UC, and the output of op-amp UB is fed into op-amp UD (where UC and UD simply act as delays). The key to creating deadtime is in determining a method to AND the two signals (UA and UC for low-side) together. Ideally, this is shown in Figure 14. It is apparent that the off-time exceeds the on-time, and so when this function is carried out for the high-side signal as well as the low-side signal, there is a time period when both signals are off.

Figure 15 illustrates the circuit design developed by the researchers to achieve a mathematical AND. The resistors Ra, Rc (where Ra=Rc) and Rb (Rb=100·Ra) form a voltage divider and control the flow of current. The diodes utilized are Cree SiC bare die PiN diodes. Three cases for this circuit can arise.

(1) UA and UC outputs are both –5 V signals. In this case, current flows from ground to the op-amp output nodes of –5 V. Since Rb>>Ra, Rc, the majority of the voltage drop occurs across the Rb resistor, thus making the circuit output “signal” ≈ –5 V (off).

(2) UA and UC outputs are both +5 V signals. In this case, the two diodes block the flow of current from the +5 V nodes to ground. Since no current is flowing, the output “signal” is essentially grounded and is thus set to 0 V. It is important to remember that since the SITs are normally on devices; 0 V is an on-signal.

(3) One op-amp output is +5 V while the other is –5 V. In this case, the op-amp outputting the +5 V signal can be ignored, since the diode is blocking its current drive. The op-amp with the –5 V output is the controlling element, and current flows from ground to the –5 V node. Since Rb>>Ra or Rc, the majority of the voltage drop occurs across the Rb resistor, thus making the circuit output "signal" ≈ –5 V (off).

Due to the nature of the function of the timing circuit illustrated in Figure 15, the output "signal" is essentially a voltage signal with almost no current drive capability. Even though the SITs are operating as voltage-controlled devices, they still require some current drive to overcome the gate capacitance and switch them on. Due to this requirement, the low-side and high-side signals from op-amps UC and UD are fed into another set of op-amps, UE and UF respectively, of Figure 11's "drive" block. This inserts a current drive capability into the control signals (and returns the control to a +5 V to –5 V signal).

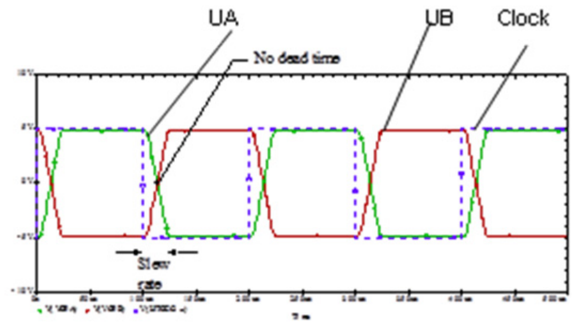


Figure 13. UA (green), UB (red), and clock (dashed) signals.

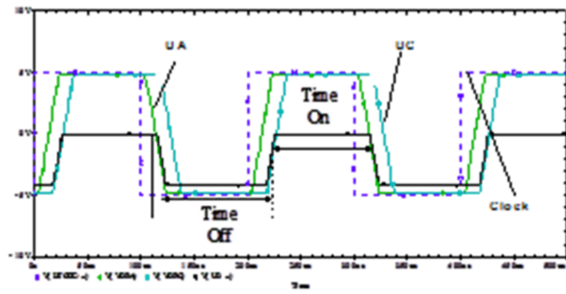


Figure 14. UA (green), UC (cyan), and clock (dashed) signals.

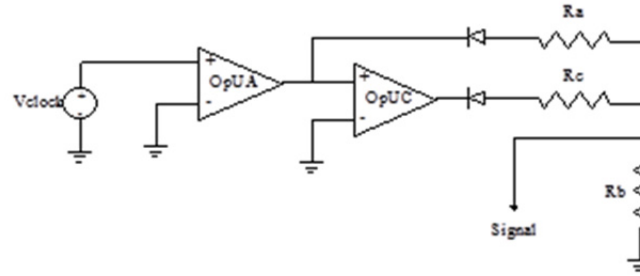


Figure 15. Mathematical AND circuit.

The signals are then fed to drive the isolation pulse transformers. Figure 16 illustrates the captured waveforms of the half-bridge gate drive signals generated by the control circuit, low (Ch2) and high (Ch3).

Figure 17 illustrates the captured waveforms of the SIT half-bridge operating at 200 watts. The Ch2 waveform is the high-side 100 V signal, and the Ch3 waveform is the hi-side 2 A signal (×10 current probe).

The results of the high temperature control circuit along with those of the SiC SIT based half-bridge prove that SiC devices can be driven at elevated temperatures and could therefore be integrated into industrial, military, and space applications. The next vital step to making these applications possible are to reduce size through specialized packaging techniques such as MCPMs.

Packaging

As SiC power devices are introduced into the commercial market, there are a number of factors that will limit their full potential use, the most prominent of which is the issue of high-temperature packaging. The full utilization of the advantages of SiC power devices would mean operating them at their *peak power densities*, i.e., operating at power levels that would bring the

semiconductor junction temperature to 600 °C. A high-temperature power package is vitally needed that will be capable of achieving this.

Silicon-carbide power Schottky diodes have just recently entered the commercial market. Currently they are offered only in discrete packages with the identical environmental operational capability as those used to house silicon devices. SiC technology is a new medium, and so the current focus is upon utilizing the 10× improved electrical efficiencies associated with SiC over silicon (thus standard packages are currently being used). Little research has yet been devoted towards the development of high-temperature packages that will be capable of taking advantage of the 10× power density capabilities of the devices. This technology development will be vital for power electronics miniaturization and volume/weight reduction.

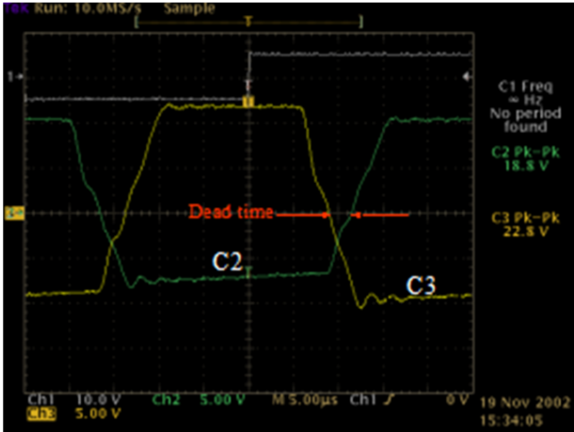


Figure 16. Gate drive control signals at 20 kHz.

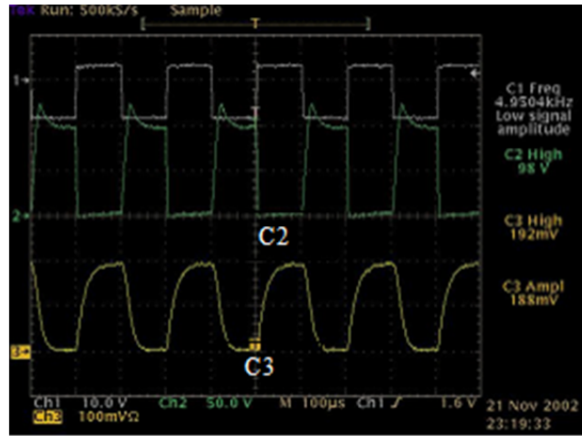


Figure 17. High-side voltage and current signals.

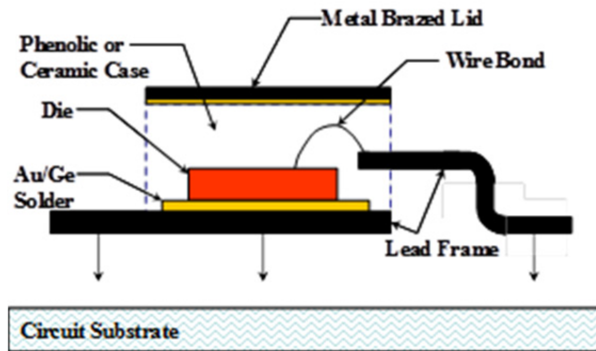


Figure 18. Schottky package cross-section

Figure 18 illustrates the cross section of a package design strategy under investigation by APEI, Inc. In this strategy, the case and baseplate lead frame are integrated and molded in a high-temperature Phenolic plastic (Phenolic is rated to over 400 °C and is used for transformer header electrical mounts) or ceramic. The bare-die SiC power device is mounted to a metal lead-frame via a very high-temperature solder such as 88Au-12Ge. The device is wire bonded to the lead post and a metal lid is brazed to the case. Packaging for SiC devices includes the investigation of high-temperature wire bonding, high-temperature die attach methods, and thermal stress analysis of the entire package. Additionally, advancements in the miniaturization of power electronic systems are seen through the use of multichip power modules (MCPM).

Since SiC devices are capable of operating into the GHz range, they offer a great reduction in the size of passive components such as capacitors, inductors, and other magnetic components. Integrating control and power layers into a single module would significantly reduce size, weight, and parasitic effects. This approach is a multichip power module in which multiple layers would be utilized to separate the power and control circuitry, as illustrated in Figure 19. The power module is built upon a metal-matrix-composite heatspreader, for which the material content has been specifically engineered to reduce the stresses of thermal expansion within the MCPM. A high-power substrate layer, such as direct-bond-copper (DBC), is utilized for its high current-carrying capability and significant thermal dissipation properties [14, 15]. The high-power SiC devices are mounted on this layer. High-temperature polyimide materials or LTCCs are utilized as the control layers, which are laminated upon the power layer. The control circuitry is gold plated in order to reduce oxidation and improve reliability, the control devices are then mounted on the top surface of the control layer, and electrical connections made between layers by vias.

It is clear that the use of SiC can reduce the size and weight of many circuits through the advantage of higher switching frequencies and through the use of advanced packaging techniques. Once a device has a suitable package, they can be characterized and models can be created for use in simulator tools.

Modeling

In order for circuit designers to fully utilize the advantages of the new SiC power device technologies, compact models are needed in circuit and system simulation tools. SiC power device models with extracted parameter sets will be provided in circuit simulator libraries and will be used to provide insight into the performance advantages of SiC power diodes.

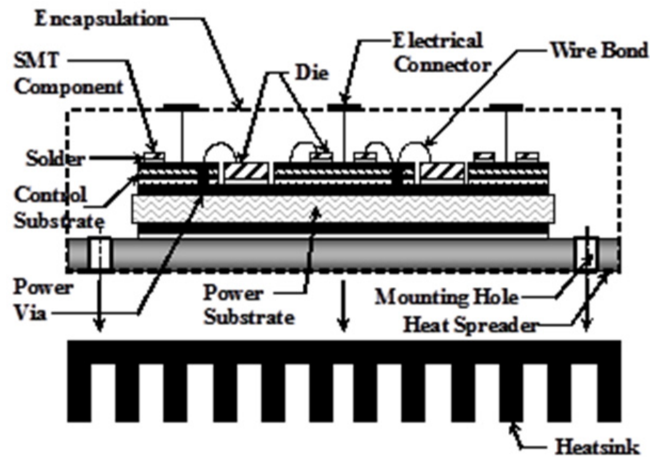


Figure 19. High-temp. SiC DC-DC converter design.

SiC diode model—The UA and the National Institute of Standards and Technology (NIST) researchers worked in collaboration to develop a SiC Schottky diode model. A novel high-speed reverse recovery test system developed at NIST was utilized for device characterization, and later for model validation. This test circuit is shown in Figure 20(a) and its equivalent circuit simulator model is shown in Figure 20(b). Figure 20(a) shows the test circuit used for characterizing the diodes for reverse recovery, and Figure 20(b) shows the behavioral representation including parasitic elements used for diode model validation. It is important to note that the test circuit in Figure 20(a) is well characterized, meaning that the values of all circuit components and parasitic elements are known. In order to operate the test circuit in Figure 20(a), first the vacuum tube is turned on to establish the test current i_L in the inductor L. Once the test current is reached, the tube is ramped off and the inductor current is commutated to the Device Under Test (DUT). To initiate the reverse recovery test, the tube is ramped on with a well controlled di_Q/dt at the tube anode. This results in a negative di_D/dt being applied to the DUT. As

the diode begins to recover, the diode voltage v_D rises toward the power supply voltage V_{drive} completing the recovery test.

The reverse recovery tests are performed for various values of forward diode current i_D, diode reverse bias power supply voltage V_{drive}, di_D/dt, and dv_D/dt, where dv_D/dt is controlled by

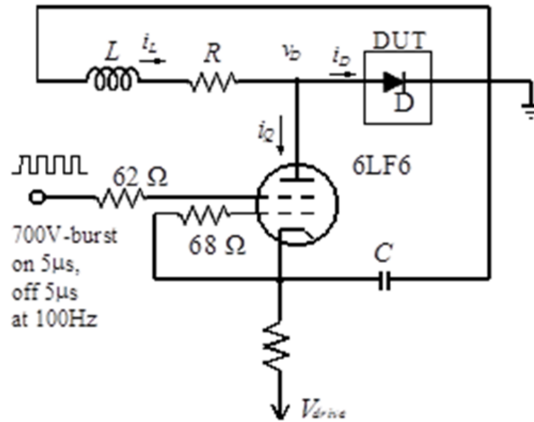


Figure 20(a). High-speed diode reverse recovery test setup.

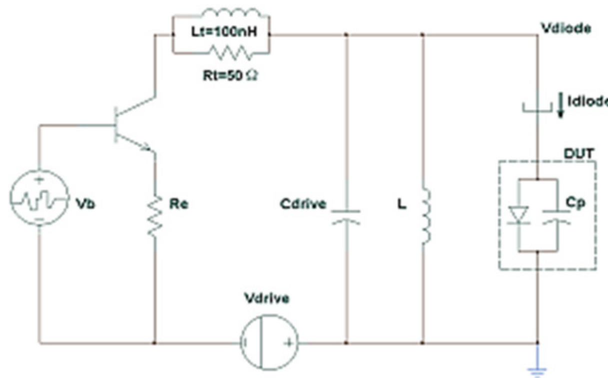


Figure 20(b). Equivalent behavioral circuit emulating test setup.

placing various driver capacitors across the DUT. By independently controlling V_{drive}, di_D/dt, dv_D/dt, and the forward diode current at turnoff, the new test circuit enables testing of the new SiC technology for the full range of conditions that occur for various application conditions. Varying the value of V_{drive} emulates the application conditions for circuits with different DC bus voltages, varying the value of di_D/dt emulates the application conditions of different speed anti-

parallel switching devices, and varying the value of dv_D/dt emulates the application conditions of using anti-parallel switching devices of different output capacitance. Also, varying the value of *dv/dt* aids in the determination of the portion of the diode recovery due to charge storage and the portion due to device capacitance. Varying the value of the forward diode current at turnoff aids in the determination of the portion of current that is due to emitter recombination and the portion that contributes to charge storage.

Results from this research were used to accurately model a new class of power devices, (PiN, Schottky, and MPS diodes with voltage ratings from 600 V to 10 kV and current ratings from 0.25 A to 20 A) and develop a parameter extraction sequence to enable the characterization of any SiC power diode. Parameters extracted from an MPS SiC diode are shown in Table II.

The SiC MPS diodes studied were designed such that the PiN diode does not turn on in normal forward bias operation. This type of operation is typically referred to as the junction-barrier-controlled-Schottky (JBS) diode mode. The PN junctions serve only to shield the Schottky barrier from high electric fields, thus preventing Schottky barrier lowering and reducing leakage current.

Figure 21 shows the simulated (dashed) and measured (solid) on-state characteristics for the 1500 V, 0.5 A (0.0045 cm^2) SiC MPS diode for different temperatures in the range of 25 °C to 225 °C. In these curves, the built-in potential decreases with increasing temperature because the increasing thermal energy of electrons in the metal voltage. The decrease in slope of the on-state voltage curves with increasing temperature is indicative of the reduction of mobility with temperature for a majority carrier device.

Figure 22 shows the measured (solid) and simulated (dashed) reverse recovery waveforms of the MPS diode for three different di/dt values and no external driver capacitance.

In these figures, the initial measured forward current is 0.6 A and the diode is switched by applying a constant negative di/dt with the tube.

Table II. SiC MPS diode model parameters [16].

Parameter	Parameter Name	0.5 A MPS
EG	Bandgap / Barrier Height	1.6
VJ	Built-in junction potential	1.2
CJ0	Zero-bias junction capacitance	30p
M	P-N grading coefficient	0.5
FC	Forward-bias depletion capacitance coefficient	0.5
RS	Forward series contact resistance	2.85
ISR	Low-level recombination saturation current	$4.26 \cdot 10^{-13}$
NR	Low-level recombination emission coefficient	1
XTIR	*ISR* temperature exponent	11.1
NTR	*ISR* thermal multiplication factor	2.1
TRS1	Linear *RS* temperature coefficient	1.45m
TRS2	Quadratic *RS* temperature coefficient	46.7μ
GAMMA	*RS* temperature exponent	2.93

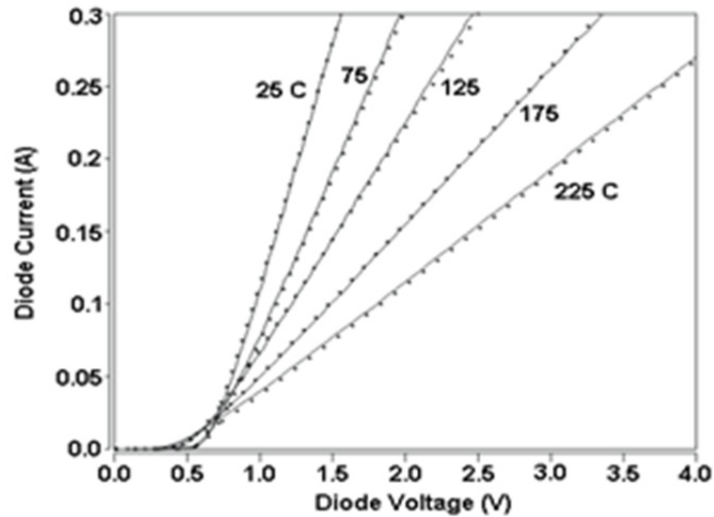


Figure 21. Simulated (dashed) and measured (solid) on-state characteristics for the 1500 V, 0.5A SiC MPS diode [16].

SiC MOSFET Model—The model used for the SiC MOSFET is based upon the latest version of the power MOSFET formulation utilized in the Hefner IGBT model [17]. The model has been enhanced by adding the temperature-dependent material properties of 3C-, 4H-, and 6H-SiC, which can be selected using the material-type parameter switch. The model contains features that have been shown to be important to describe the dynamic performance of vertical power MOSFETs including the two-phase nonlinear gate-drain overlap capacitance, negative gate voltage inversion of the gate-drain overlap, and nonlinear body-drain depletion capacitance. The MOSFET channel current expressions used in the model are unique in that they include (1) the channel regions at the corners of the square or hexagonal cells that turn on at lower gate voltages and (2) the enhanced linear region transconductance due to diffusion in the nonuniformly doped channel.

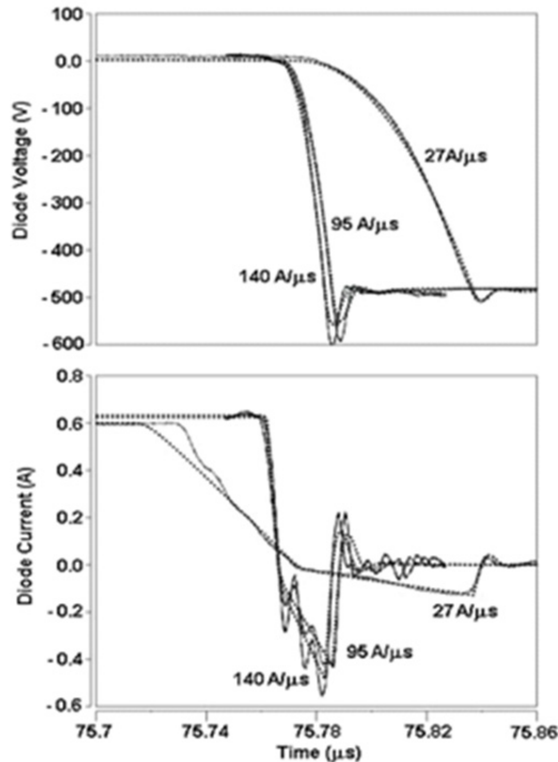


Figure 22. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 1500 V SiC MPS diode for three different di/dt values and no external driver capacitance [16].

Recently, a software package called IGBT Model Parameter ExtrACtion Tools (IMPACT) was introduced to automate laboratory instrument control and parameter determination for IGBTs [18]. To extend IMPACT to be applicable to SiC power MOSFETs, a material-type switch was added to select and calculate the temperature-dependent properties of the material. for power MOSFETs, the IMPACT package reduces to three programs that extract the power MOSFET model parameters. These programs are SATMSR, which measures the saturation current versus gate voltage; LINMSR, which measures the linear region on-state voltage versus gate voltage for a constant drain current; and CAPMSR, which measures gate and gate-drain charge characteristics. The extraction sequence is performed over an applicable temperature range to extract the temperature coefficients of the model parameters.

The MOSFET model is used to describe the performance of a 2 kV, 5 A 4H-SiC Double implanted MOSFET (DiMOSFET) and to perform a detailed comparison with the performance of a widely used 400 V, 5 A Si Vertical Double-Diffused MOSFET (VDMOSFET). To do this, the model parameters are extracted for each device at several temperatures using the extraction sequence, Table III show the model parameters extracted at 25 °C. Figures 23 and 24 show the simulated and measured output characteristics for the 2 kV SiC and 400 V Si MOSFETs at 25 ºC and 100 ºC. The on-state resistance at 25 ºC is similar between the Si and SiC MOSFETs, although the SiC device requires twice the gate drive voltage. Comparing the SiC and Si on-state curves, the Si curves are linear in the on-state region and have a pronounced change in curvature as the saturation or pinch-off region is approached.

The SiC curves, on the other hand, gradually transition from the linear region to the saturation region. In SiC MOSFETs, the epitaxial layer resistance is much smaller and the channel resistance is higher, thus making the MOSFET channel a more significant contributor to

the on-state voltage. This is due to the low channel surface mobility of SiC compared to Si. Because the SiC curves have less resistance in series with the MOSFET channel, the enhanced linear region transconductance model of [17] is essential for these devices. Furthermore, because the transconductance is much smaller for SiC, the on-state voltage is closer to the pinch-off voltage, and the model for the transition region is more important. At 100 ºC, the Si device has a severe reduction in conduction capability, whereas the SiC on-resistance is only minimally affected. This occurs because the drift region resistance is a smaller portion of the on-state resistance in the SiC device and because the channel mobility does not decrease with temperature for the SiC device. In the SiC MOSFET, the channel mobility increases with temperature as more interface traps become occupied with the larger concentration of electrons available for conduction, whereas the bulk mobility decreases with temperature as carrier scattering dominates [19]. The resulting effect is an increase in channel conductance and an increase in the drift layer series resistance.

The results for the widely used 400 V, 5 A Si power VDMOSFET and a new 2 kV, 5 A SiC power DiMOSFET demonstrate good agreement between the model and experiment [7]. The IMPACT parameter extraction tools were extended to be applicable to the power MOSFET model parameter extraction sequence and the SiC material parameters. The new model provides insights into the SiC MOSFET performance and provides the capability to simulate the performance of the new technology in different circuit applications.

TABLE III. Model parameters at 25 °C [7]

Parameter	Si	SiC
A	$0.1\ cm^2$	$0.06\ cm^2$
W_b	$50\ \mu m$	$20\ \mu m$
Nb	$3.1 \odot 10^{14}\ cm^{-3}$	$3 \odot 10^{15}\ cm^{-3}$
V_T		$5.77\ V$
K_p	$3.4\ V$	$0.33\ A/V^2$
θ	$3.3\ A/V^2$	$0.03\ V^{-1}$
K_f	0	2
R_s	1.7	$0.03\ \Omega$
Kfl	$0.02\ \Omega$	0.07
dV_{tl}	0	$2.5\ V$
P_{vf}	$0\ V$	0.95
V_{Td}	0.7	$0\ V$
A_{gd}	$3.4\ V$	$0.03\ cm^2$
C_{gs}	$0.075\ cm^2$	$2.68\ nF$
C_{oxd}	$1.114\ nF$	$2.18\ nF$
V_{bigd}	$2.066\ nF$	$2.8\ V$
F_{xjbe}	$0.6\ V$	0.5
F_{xjbm}	0.5	0.75

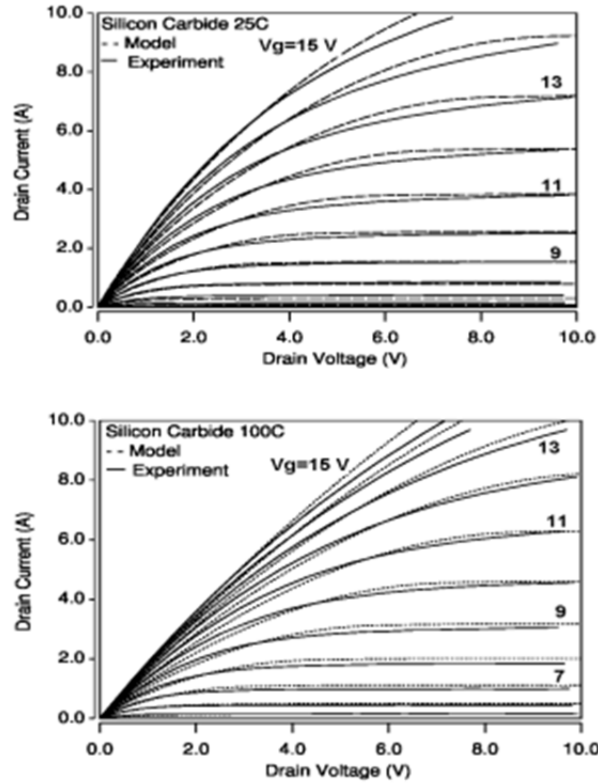


Figure 23. Silicon-carbide MOSFET simulated (dashed) and measured (solid) output characteristics as a function of gate voltage for (a) 25 ºC and (b) 100 ºC [7].

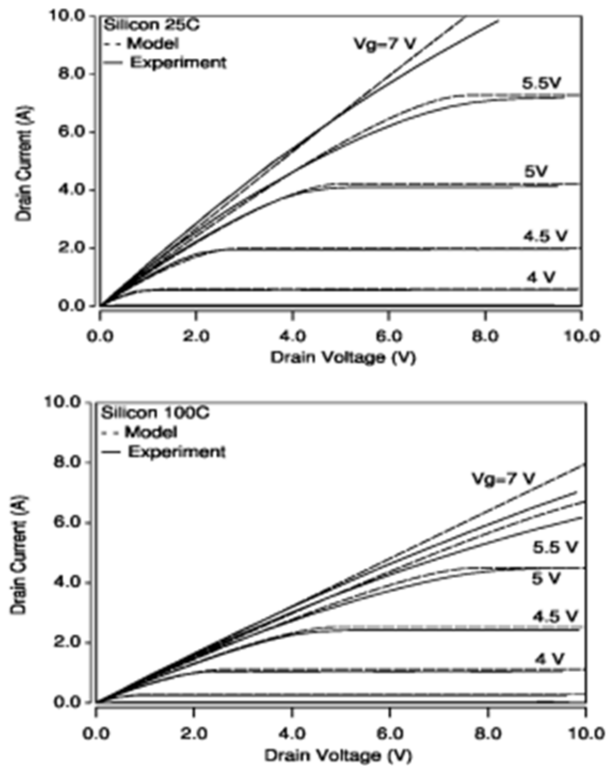


Figure 24. Silicon MOSFET simulated (dashed) and measured (solid) output characteristics as a function of gate voltage for (a) 25 ºC and (b) 100 ºC [7].

4. MAPPING TO NASA APPLICATIONS

NASA is potentially interested in SiC power converters for in-situ probes and landers for harsh environments, or satellite and spacecraft applications to drive low-voltage digital and analog electronics from high-voltage power sources (such as the DC solar arrays). The advantage to NASA of an increased operational temperature range for spacecraft applications is the reduction of required heatsinks and heat exchangers, which are bulky, heavy components within the overall systems. Additionally, the increase in switching frequencies reduces the size of passive components and therefore the size of any DC-DC converter. This reduction would result directly in the saving of critical weight (along with its accompanying exorbitant launch costs).

SiC for Harsh Environment Applications

The atmosphere of Venus is one of the most extreme environments one could possibly hope to penetrate, survive, and explore. The atmosphere is corrosive with high concentrations of sulfuric acid cloud formations, and at the surface altitude, the average surface temperature is 464 °C at a pressure of 92 atmospheres. The chemical composition of the near-surface atmosphere is composed of 96.5% carbon dioxide, 3.5% nitrogen, and trace amounts of sulfur dioxide (150 ppm), argon (70 ppm), water (20 ppm), carbon monoxide (17 ppm), helium (12 ppm), and neon (7 ppm) [20]. Thus the main survivability and operational reliability factors for in-situ probes and landers are (1) electronics operation at ambient temperatures in excess of 464 °C, (2) hermetic electronic packages capable of withstanding 92 atmospheres of pressure in an environment at 464 °C, (3) hermetic packages capable of maintaining reliable integrity within the chemical composition environments described above, and (4) mechanical-electrical systems such as DC motors and actuators that are able to reliably operate in the above conditions.

The overall concept investigated by the researchers is to develop the motor drive electronics and to integrate those electronics within the DC machine. Each DC motor (with its driving electronics) is thus modularized. The motors are then utilized throughout the application's system however required. This concept is illustrated in Figure 25, in which the researchers have envisioned a basic robotic arm such as might be used on a Venus lander. In this conceptual application the SiC motor drive module is mounted on the base of the DC motor and then hermetically sealed with a lid. The motors are then placed at the joints, mounted with gearing, to provide for arm movement.

It is easy to see how the clamp on the arm could be replaced with a soil drill, requiring little variation in the modular DC motor scheme. All of the motors and drive electronics are

identical. DC power would be brought up along the length of the arm through an internal structural track (not shown in this illustration), along with the command signals for the SiC motor control and drive modules. Tracked or wheeled vehicles could utilize the same or similar DC motors, the drive electronics of which would be identical to those used in the arms. Even if the control algorithms were different, the actual hardwired drive circuitry of the SiC control module would be the same. Every motor throughout the entire explorer would use that same drive and control module design.

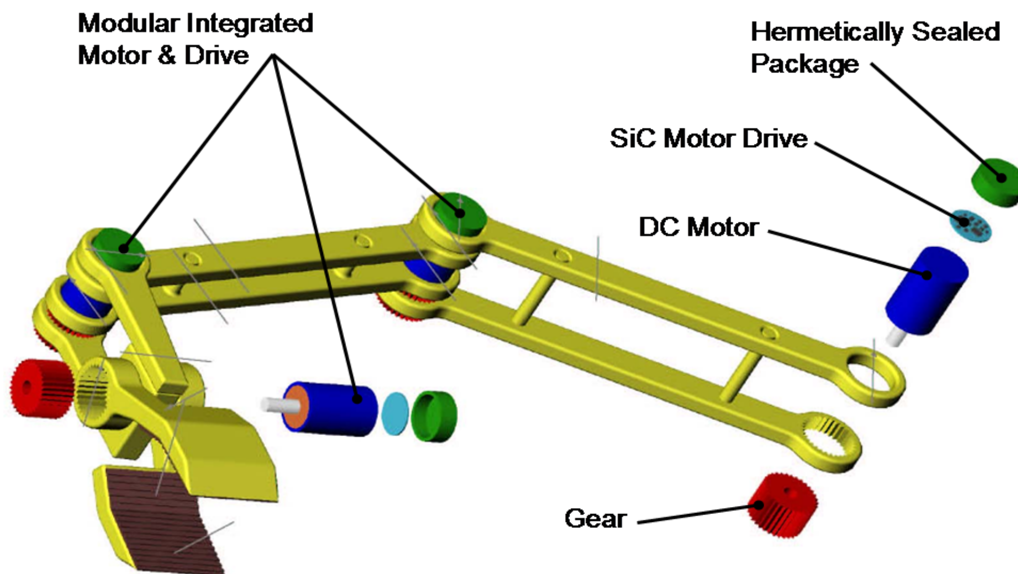


Figure 25. APEI, Inc.'s conceptualized systems application of modularizing SiC motor drives, such as might be found on a Venus lander robotic arm.

A closer look at the integrated DC motor, which is illustrated in Figure 26, shows the SiC drive electronics integrated into the DC motor by mounting at the base of the motor case. The power electronics package is hermetically sealed with a lid enclosure. The substrate will be a high-performance aluminum-nitride (AlN) ceramic-based DBC. Either bare-die SiC or high-temperature packaged components could be mounted to the substrate. The DC motor drive would consist of a SiC pulse width modulation (PWM) control chip, a drive chip, and power devices. Supporting high-temperature passives and magnetics would also have to be integrated.

A series of electrical pins and connectors would plug the module into the motor and provide connection to the DC voltage power bus.

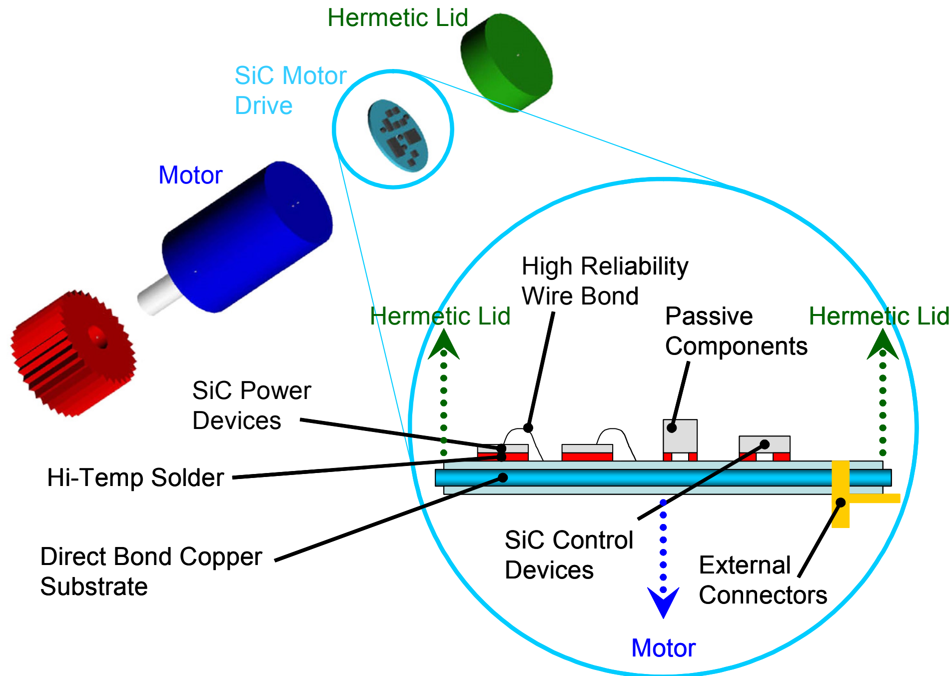


Figure 26. Conceptual illustration of an integrated SiC motor drive and DC machine.

One of the keys required for making the integration of the power electronics with the DC machine exciting, novel, and highly advantageous would be the integration of the entire power electronics drive circuit into the module. This necessitates the requirement of the control chips and supporting passive components to operate at high temperatures, along with the power devices. Therefore, the control ASICs must also be SiC devices. Figure 27 illustrates the circuit schematic of a minimum part count DC half-bridge motor drive that utilizes a control chip to create the power device gate drive timing waveforms, and a driver chip to deliver the timed waveforms with enough energy to switch the power devices [21]. These are the two chip functions that will have to be implemented in SiC. The control chips would have the necessary functionality for a specific NASA applications.

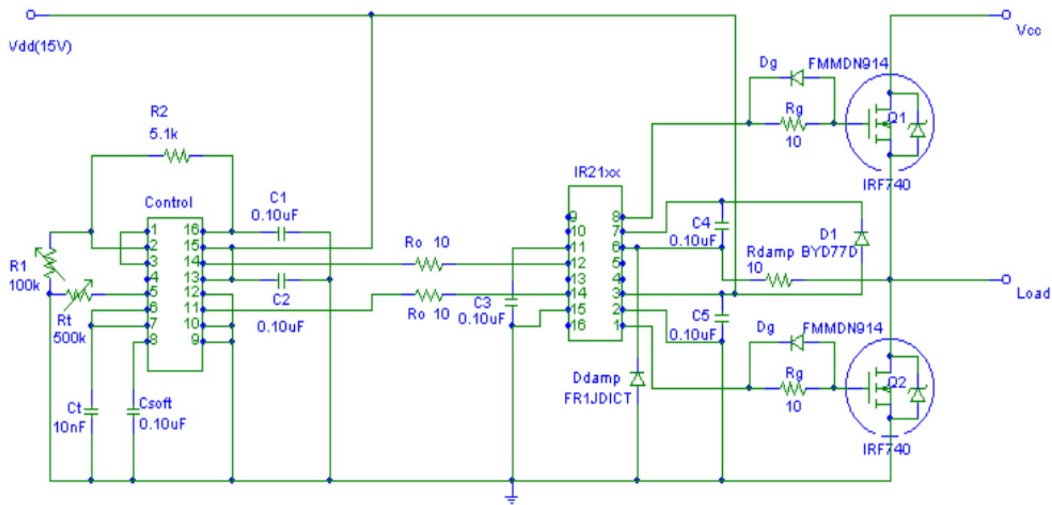


Figure 27. DC half-bridge minimum part count motor drive.

Many different applications will benefit from a versatile type of system such as described here. This design can extend in to other areas, including lightweight DC-DC converters.

SiC Ultra Light-weight DC-DC Converters

SiC not only offers great benefits to electrical systems in harsh environments but also offers the opportunity to create highly efficient ultra-lightweight DC-DC power converter modules for spacecraft and satellites. Increasing power density and efficiency, reducing size and weight, and improving modularity of electronics are all goals of the NASA program.

The development of lightweight DC-DC power converters is essential in almost all NASA electric power management applications. These converters would offer volume, weight, and performance benefits for energy conversion power systems, including solar arrays, fuel cell or battery banks, nuclear-powered cores, or other power sources. The energy from these sources must be converted to DC bus voltages for use by the onboard computer, telemetry, sensors, communication, and navigation systems. The same technology could be transferred to all types of power electronics systems, including DC motor drives, AC motor drives, or audio power conversion.

APEI, Inc. has performed several analyses on the weight reduction that can be obtained through the high power densities of SiC. To compare the power densities of Si to SiC, a half bridge model was developed and simulated in Flotherm. After creating an accurate model, the maximum operational characteristics of a Si package were determined by using the maximum operating temperature (150 °C) of most Si devices. Simulations in Figure 28 show that a maximum of 386 watts thermal (roughly 5 kW electrical) could be dissipated from the half-bridge with a heatsink weighing 3 kg and measuring 180mm × 125mm × 135 mm.

A similar simulation was run for a SiC half-bridge module with the same geometry and heatsink but with the theoretical limit of 600 °C. Figure 29 shows the results of the SiC module dissipating 1,856 W thermal or approximately 13 kW electrical. The thermal dissipation in the SiC module is an improvement of almost 5 times that of Si. Next a simulation of the SiC half-bridge with a 0.30kg (50mm × 50mm × 10mm) heatsink was performed. **This is a weight reduction of 90% and a volume reduction of 100×.** Figure 30 illustrates this package operating at 340 W thermal or approximately 7.5 kW. In order to make lightweight electronics, reducing or removing the heatsink is absolutely critical. With the ability of SiC to operate at high-temperatures and high-power densities, this possibility becomes real.

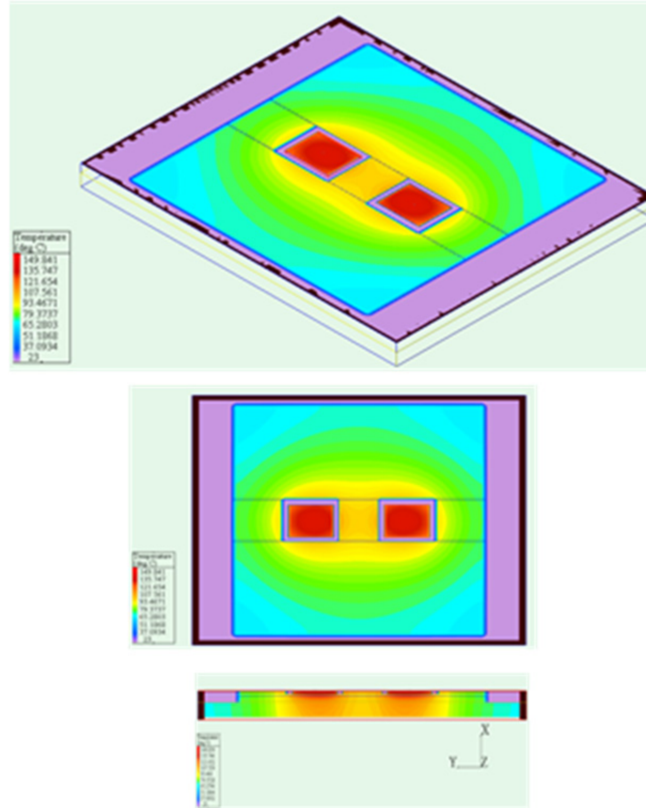
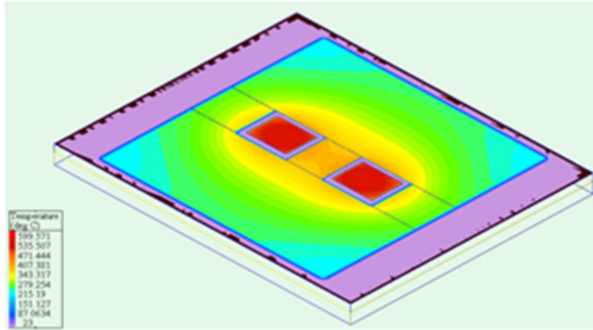


Figure 28. Flotherm thermal simulation of the Si model @ 386 W thermal.

The possibility of ultra-lightweight power electronics hinges on the need to develop high-temperature packaging technologies that can withstand the theoretical SiC junction temperature limits. With high temperature operation of the power electronics components, heatsinking and active cooling thermal management strategies can be significantly downgraded, thus reducing the size, volume, and weight of the overall power electronic systems by as much as two orders of magnitude. This will produce significant savings across the board in almost all areas of NASA applications.



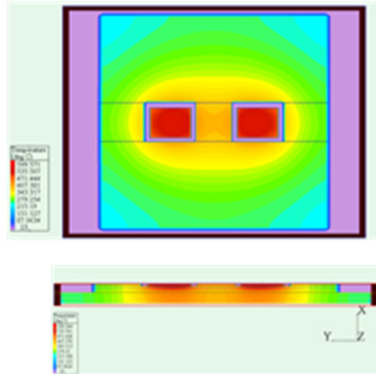
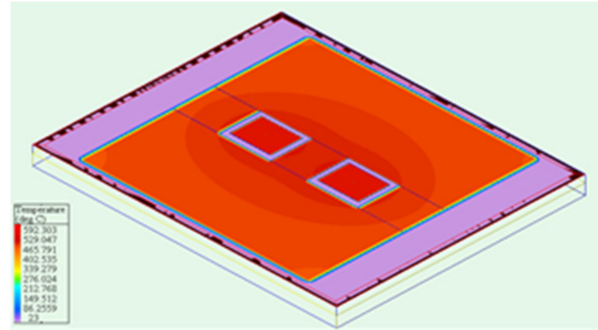


Figure 29. Flotherm thermal simulation Of the SiC model @ 1,856 W thermal.



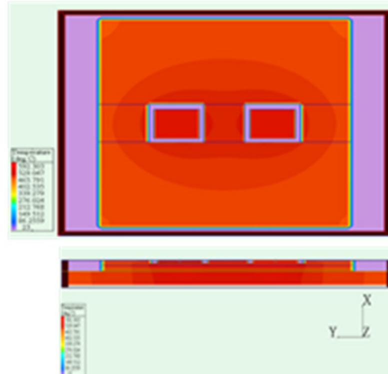


Figure 30. Flotherm thermal simulation Of the model @ 340 W thermal with a 1/100th sized heatsink.

5. Conclusion

This paper has introduced the reader to the emerging field of SiC electronics and the important role SiC will play in many systems requiring high-power devices. Other systems that require special operating conditions such as ultra-high temperatures will also benefit from the advancement of SiC electronics. Many of the benefits SiC electronics have over Si, such as switching capabilities, junction temperatures, power densities, and electric field breakdown have been outlined and explained. Additionally, specific devices such as SiC Schottky diodes, SiC SITs, and SiC MOSFETS have been introduced along with the results from extensive research, modeling, and characterization of these devices by the authors.

A selected few of the many applications for SiC have been discussed, including those that the researchers are currently involved in. Applications include control for SiC power devices,

integrated motor drives, lightweight DC-DC converters, extreme environments such as those found on Venus, and geological exploration.

Current packaging techniques do not allow for SiC devices to operate at their highest potential. An MCPM method for packaging SiC was introduced and a look at the problems and solutions with such a technique were discussed.

Many applications that were discussed can be directly mapped over to NASA applications. Examples of a SiC integrated motor drive for a robotic arm and ultra lightweight DC-DC converters for space craft and satellites are just two of the applications discussed that would be highly beneficial to NASA for both cost and reliability.

ACKNOWLEDGMENTS

We appreciate Northrop Grumman, Cree, Curamic, NIST, and NSF for their support of the research presented here.

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CHAPTER 4

A NOVEL THREE-PHASE MOTOR DRIVE UTILIZING SILICON ON INSULATOR (SOI) AND SILICON-CARBIDE (SIC) ELECTRONICS FOR EXTREME ENVIRONMENT OPERATION IN THE ARMY FUTURE COMBAT SYSTEMS (FCS)

J. Hornberger, A. B. Lostetter, K. J. Olejniczak, S. Magan Lal, and A. Mantooth

© 2004 IMAPS. Reprinted, with permission, from Hornberger et al, A Novel Three-Phase Motor Drive Utilizing Silicon on Insulator (SOI) and Silicon-Carbide (SiC) Electronics for Extreme Environment Operation in the Army Future Combat Systems (FCS), International Symposium on Microelectronics, November 2004.

Abstract

This paper will discuss the research, development, fabrication, and test results of a board level three-phase high-temperature motor drive demonstrating the feasibility for operation in the Army FCS vehicles. The motor drive has operation capabilities up to 250 °C using silicon on insulator (SOI) control electronics on a multi-layer control board. Extensive analysis has been performed on the high-temperature operation of components including; substrate material, resistor and capacitor function, SOI microcontroller and memory operation, and active op-amp electronics. Particular detail will be given to the design and building of high-temperature magnetics for on-board use. Data will be presented on the high-temperature operation of these components individually, and combined in the final prototype. The 3-phase motor drive prototype was tested under full load conditions up to 4 hp and at temperatures up to 250 °C. Operational and test data under simultaneous full load and high-temperature conditions will be presented, including microcontroller timing functions, gate drive signals, 3-phase power half-bridge operation, and motor operation.

Key Words

Silicon-carbide, static-induction-transistor (SIT), power electronics packaging, high-temperature electronics, three-phase motor drive, and HTMOS Silicon-on-Insulator (SOI) electronics.

Introduction

The key to advancing power electronic systems for use in advanced applications lies in the ability to make systems lighter, smaller, and more efficient. With higher operation temperature (up to 600°C), higher breakdown voltage (10 times that of Si), lower switching losses, and higher current densities (3 to 4 times higher than Si), SiC is a technology that has the potential to offer significant improvements over current Si based power electronic systems [1]. Many factors, however, are still limiting the use of SiC power transistors. First, only a few SiC devices are available on the commercial market, including Schottky diodes and SiC MESFETs (not a power device). SiC PiN diodes, power MOSFETs, gate-turn-on-thyristors (GTOs), bipolar junction transistors (BJTs), junction field effect transistors (JFETs), and static-induction-transistors (SITs) are all currently under development by research and manufacturing organizations (such as Northrop-Grumman, Infineon, Cree, Army Research Labs, Semi South Laboratories, and Rockwell Scientific), although none of these devices have yet been released into the commercial marketplace.

As SiC transistors are introduced into the commercial market over the next few years, there are other factors that will limit their full potential to operate at temperatures up to 600 °C. The lack of high-temperature packages and packaging technologies including die attach, wire bonding, and substrates will limit the operating temperature of SiC devices. Also, the lack of high-temperature control electronics, magnetics, capacitors, and resistors will limit the full

potential of SiC in various applications. Additionally, the lack of long term testing and reliability studies at elevated temperatures, and the lack of modularized power electronics will limit the full utilization of SiC.

Applications for SiC and high-temperature power electronics are widespread and all encompassing. The first functions that could significantly benefit from SiC are high technology applications such as military and space exploration vehicles. The Army is aiming for high power density motor drives to reduce size and weight for their hybrid-electric combat vehicles. Space exploration vehicles such as satellites would benefit greatly from high-density power modules by reducing weight which reduces the cost to launch. Space vehicles such as a Venus probe could significantly benefit from SiC by being able to reliably perform experiments and collect data without failure soon after landing on the planet's surface [2]. Control electronics and sensors of a jet or rocket engine that could be placed directly on or into the engine would improve system performance. Other high-performance applications to benefit would be nuclear power reactors, where sensors could endure the high-temperature and high-radiation environments; or petroleum and geological exploration, where electronics could be sent deep beneath the Earth in high-temperature bore-wells. Finally, any system that would see improvement from high-density, high-power, and/or high-efficiency electronics would benefit from SiC.

Army Future Combat Systems (FCS)

In late 1999, the Army's Chief of Staff launched an initiative to make combat forces lighter and more easily deployable. The Abrams Main Battle Tanks and Bradley Fighting Vehicles are heavy and can take weeks to fully deploy in force. A request to develop next generation air and ground vehicles that are lighter weight, more intelligent, and easy to maneuver led to the inception of the Army's Future Combat Systems (FCS) program [3].

In order to make combat vehicles lighter and more maneuverable, the FCS has its goals set to make a combat force that is purely electric by the year 2020. These vehicles will use electric drive trains, electric weapon systems, and active defenses and armor. These vehicles must use high-power converters and motor drives that are capable of operating in harsh environments. By utilizing SiC power devices, the size and weight of the converters can be reduced significantly thereby reducing the over all size and weight of the combat vehicle. The goal is to reduce the weight of these combat vehicles by one third to as much as one half of today's systems. The FCS goals are aimed at simultaneously improving lethality and survivability.

In order to develop advanced technological applications that are usable on the battlefield for the Army FCS (such as high power motor drives for hybrid-electric combat vehicles, or pulsed power modules for electromagnetic guns), light weight, high efficiency, and high reliability all become critical factors towards realization. The key technologies for these systems are high temperature power electronics modules that operate at high power densities with little to no heatsinking requirements. Because of its advantages (faster switching speeds, smaller switching losses, and higher junction temperatures) over today's technology, SiC offers significant size and weight reduction by as much as an order of magnitude for the Army's FCS. One example of an FCS vehicle in progress is the hybrid-electric Bradley Fighting Vehicle shown in Figure 1. High-temperature motor drives can be integrated onto the motors and bulky heatsinks can be eliminated with the use of SiC.

High-Temperature Three-phase Motor Drive

Researchers at Arkansas Power Electronics International, Inc. (APEI) have performed extensive research in the area of SiC device applications, power electronics packaging, and

modeling for power electronic systems [4-9]. The researchers have built and tested control circuitry for use with SiC power switching devices for the specific application to the Army's FCS motor drive system. The circuitry consists of Honeywell's line of HTMOS high temperature microelectronics with the core of the control circuitry provided by the HT83C51 microcontroller. Honeywell's silicon-on-insulator (SOI) HTMOS parts are guaranteed to operate at 225 °C for a period of five years and at 300 °C guaranteed for one year. Honeywell's tests have shown that after five years, there is a 99.6% reliability rate on components that have been operating at 225 °C.

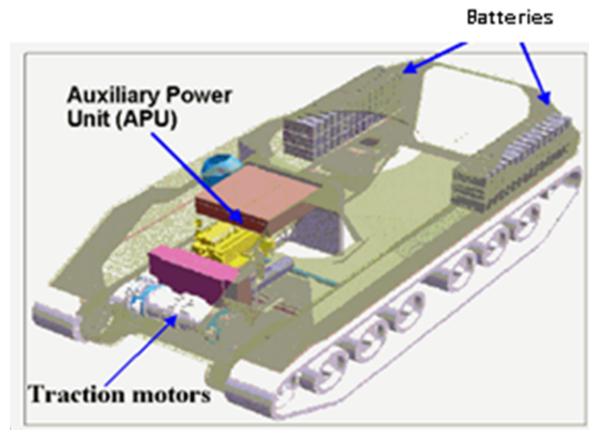

Figure 1. Hybrid-electric Bradley combat vehicle. (Army FCS graphic)

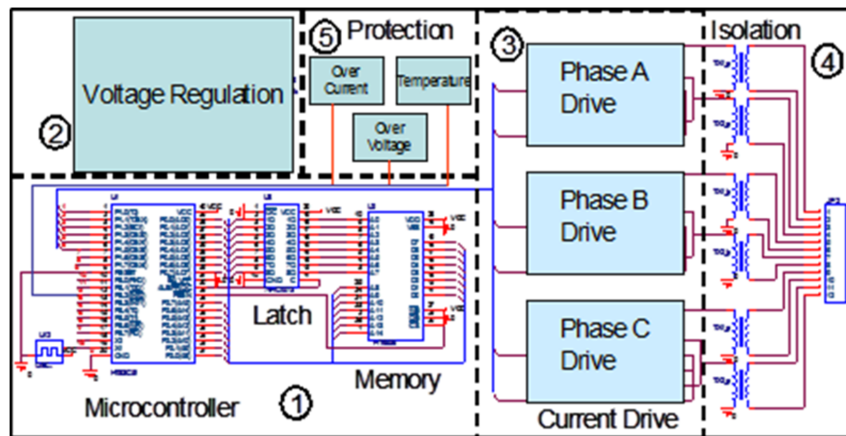

Figure 2. Block diagram of 3-phase controller.

The three-phase motor controller consists of five main blocks as shown in Figure 2.

(1) The core control consists of Honeywell's HTMOS 83C51 8-bit microcontroller. The microcontroller is pin for pin compatible with Intel's 8051 series microcontrollers and uses the same MCS-51 instruction set. The microcontroller uses external RAM that is loaded with program memory before startup, thus increasing the versatility of the control algorithm.

(2) The HTMOS line supplies voltage regulators for 5, 10, or 15 V applications with an output current of 300 mA.

(3) Since the microcontroller can only source a minimal amount of current in the range of micro-amps, a current amplification circuit is implemented through the use of HT1104 operational amplifiers. This circuit must be able to supply current in the range of miliamps for small FETs to 5 amps for large BJTs. Depending on the type of power switching device used, this circuit will vary. A simplified circuit for driving the gate of small MOSFETs is shown in Figure 3. Two operational amplifiers are paralleled and set up in a comparator type configuration with the control signal connected to the non-inverting terminal and a constant 2.5 V signal connected to the inverting terminal. These op-amps provide approximately 100 mA of current drive. Additionally, a circuit for driving SITs and JFETs has been developed and is detailed in [10].

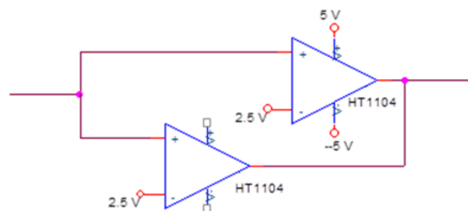

Figure 3. Current amplification circuit.

(4) The isolation circuit serves three purposes; first to isolate the drive circuitry from noise caused by power switching, second to provide an increased gate drive capability by doubling the voltage at its inputs, and third and most importantly, it allows for a floating voltage to be applied to the gate of high-side power switches.

(5) Included with the control is protection from potential catastrophic failures such as over voltage, over current, and over temperature.

The control circuitry was first tested with standard Si parts equivalent to the high-temperature design, on an FR4 board. This initial prototype is pictured in Figure 4. After successful testing of the initial prototype, a high-temperature prototype was built. In order to complete the high-temperature prototype version of the control circuitry shown in Figure 5, components, such as capacitors, resistors, transformers, IC sockets, printed circuit boards (PCBs), and various other devices with proper temperature ratings were employed. Magnetic wire and high-temperature magnetic core materials were utilized in the hand wound isolation transformers. High temperature burn-in zero insertion force (ZIF) sockets were used for all ICs in order to facilitate prototype testing and changes. High-temperature solders were obtained through Indalloy, and the high-temperature ICs were provided by Honeywell. A high T_g board was built from polyimide material (T_g=260 °C).

Passive components including resistors and capacitors for high-temperature operation present issues. Resistors tend to increase in resistance as temperature rises and therefore timing circuits are difficult to implement over varying temperatures. Caddock Micronox® (Type-MS) film resistors are capable of high-temperature operation to 275 °C with de-rated voltage and power. The resistance films are bonded to high strength ceramic cores and capped with gold-plated nickel leads. The components are encapsulated with a high-temperature silicon coating.

The component temperature coefficients are rated to +/- 50 ppm/°C [11]. This temperature coefficient relates to less than 1.5% change in resistance from 25 °C to 300 °C.

Capacitors also offer significant challenges. Currently only a few manufacturers sell capacitors rated up to 200 °C. Among the various types of capacitor dielectrics, NPO offers excellent capacitance stability over temperature. The main disadvantage of the NPO is its relatively low energy density. Novacap capacitors are guaranteed to operate at temperatures from -55 to +200 °C with maximum values of 0.47 μF and a temperature coefficient of +/- 30 ppm/°C. Other types of capacitors are able to operate at high-temperatures but have large variances over temperature [12].

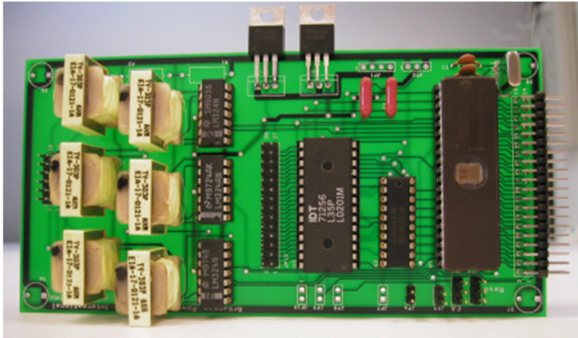

Figure 4. High-temperature design implemented on a low-temperature PCB. The board is populated with low-temperature equivalent components.

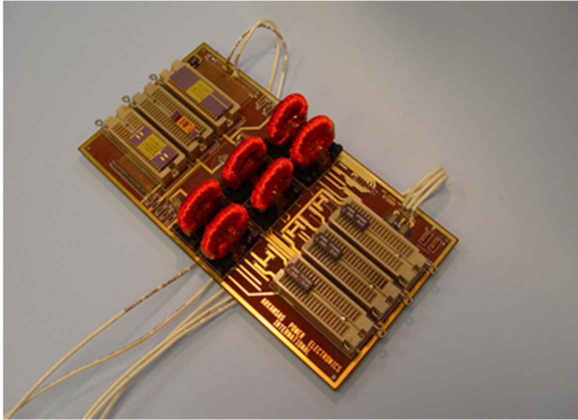

Figure 5. 250 °C 3-phase motor control prototype.

Another area that suffers greatly at high-temperature is magnetics. In order to have an operable transformer at high-temperatures, APEI, Inc. custom designed and built isolation transformers for both low frequency and high frequency applications. The design utilizes Magnesil toroidal cores rated to a maximum operational temperature of 500 °C, Ceramawire 28-gauge ceramic coated magnetic wire rated to 600 °C, and Lodestone Pacific phenolic toroidal core headers. Figure 6 shows a transformer developed to operate from 5 kHz to 1 MHz at high-temperatures. Testing of these transformers verified operation up to 400 °C. Figure 7 shows the waveforms of the transformer operating at 15kHz and 400 °C.

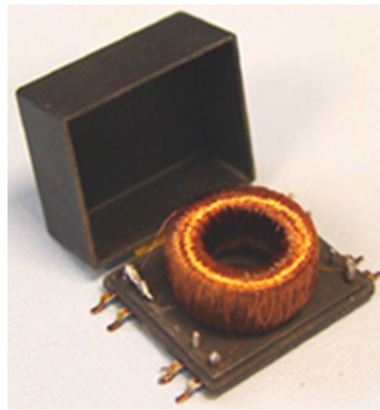

Figure 6. High-frequency high-temperature isolation transformer developed by APEI, Inc.

High-temperature testing of the control circuitry was completed and proven to drive a three-phase 4 hp induction machine under load. Figure 8 shows the control output of a single phase from the HT83C51 operating at 250 °C (Ch1 high side Ch2 low side). Figure 9 shows the output of the op-amps for the high (Ch2) and low (Ch3) side of a single phase of the circuit with the high output of the microcontroller (Ch1). Figure 10 illustrates the gate drive signal output from the isolation transformers operating at 250 °C with Ch1 as the microcontroller output, and Ch2 and Ch3 as the high and low side respectively.

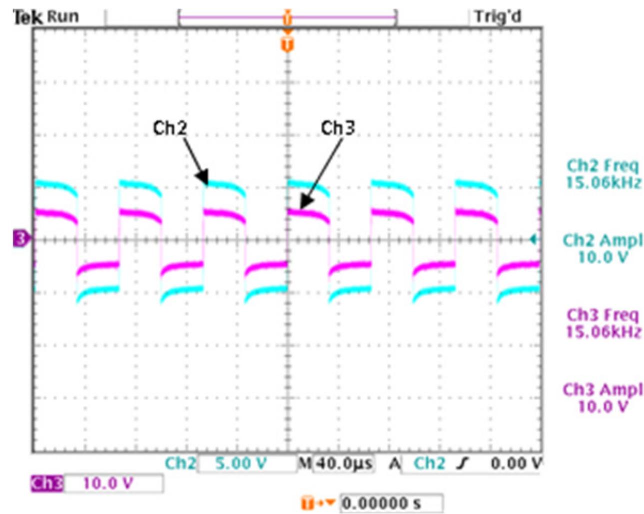

Figure 7. Transformer test at 400 °C and 15 kHz.

A full hardware test was performed with a 4 hp induction motor. Figure 11 shows the waveforms of the 3-phase 4 hp induction machine operating at startup. Ch1 is a signal from the microcontroller operating in the oven at 250 °C, Ch2 is the line-to-line voltage of the motor, Ch4 is the line-to-line current of the motor, and ChM is the instantaneous power. In this example, the motor is operating at peaks of approximately 3.5 hp.

Conclusions

This paper has introduced the reader to the emerging use of high-temperature electronics including SiC and SOI and their role in the Army Future Combat Systems. The potential of SiC to greatly improve the power electronics industry has been discussed along with the issues that currently limit that full potential. A prototype three-phase motor drive design has been introduced along with a few available high-temperature components. Testing of the control circuitry proves that the motor drive will operate up to 250 °C and is a basic “proof of concept” for a SiC based motor drive.

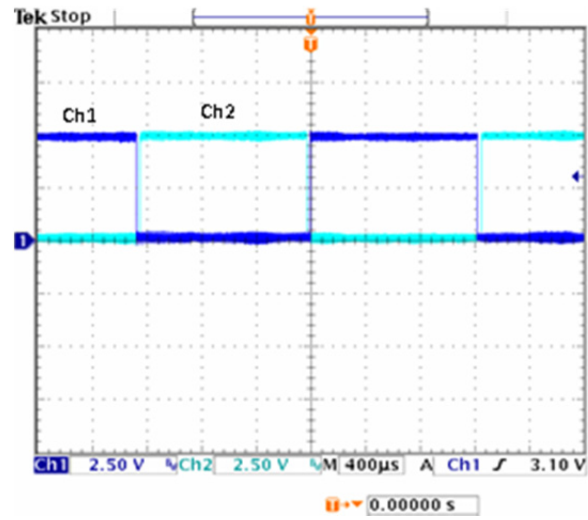

Figure 8. Output of HT83C51 operating at 250 °C.

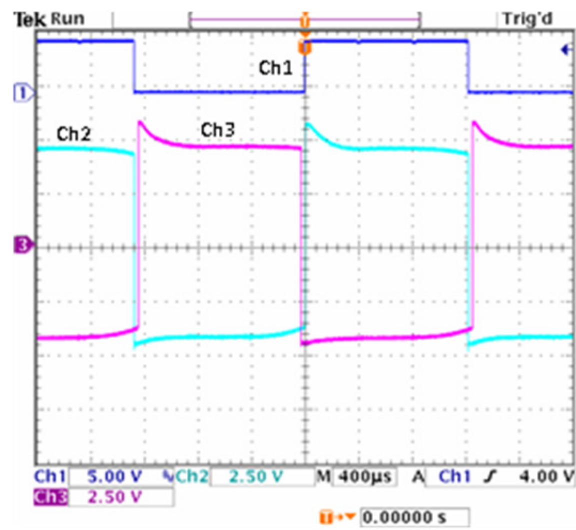

Figure 9. Output of HT1104 operating at 250 °C.

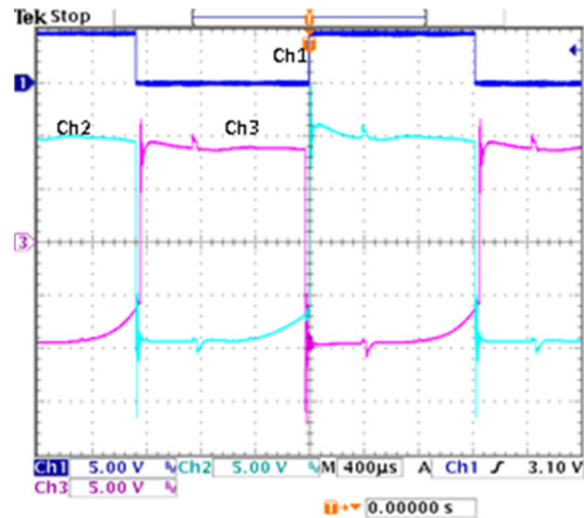

Figure 10. Output of transformers operating at 250 °C.

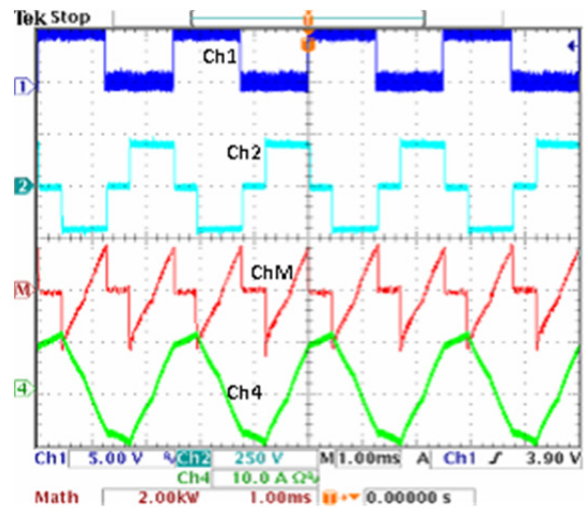

Figure 11. Waveforms of induction motor at start-up.

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APPENDIX

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Brian Schieman – Director, Program Development and Technology

CHAPTER 5

HIGH-TEMPERATURE SILICON CARBIDE (SIC) POWER SWITCHES IN MULTICHIP POWER MODULE (MCPM) APPLICATIONS

J. M. Hornberger, S.D. Mounce, R.M. Schupbach, and A.B. Lostetter, H. Alan Mantooth

© 2005 IEEE. Reprinted, with permission, from Hornberger et al, High-Temperature Silicon Carbide (SiC) Power Switches in Multichip Power Module (MCPM) Applications, IEEE Industry Applications Society Annual Meeting, October 2005.

Abstract

Arkansas Power Electronics International, Inc, (APEI, Inc.) and University of Arkansas researchers have developed a novel, highly miniaturized motor drive capable of operation in excess of 250 °C. The high-temperature multichip power module (MCPM) integrates silicon carbide (SiC) JFET power transistors with high-temperature MOS silicon-on-insulaor (SOI) control electronics into a single, highly miniaturized and compact power package. This paper will outline the design philosophy behind the high-temperature MCPM, illustrate thermal modeling results of the package, and present the results of prototype testing (demonstrating functionality).

Keywords

Silicon carbide (SiC); Silicon on Insulator (SOI); High-temperature electronics; High-temperature packaging; Multichip power modules (MCPMs)

Introduction

The future of power electronics will be greatly influenced by the commercialization of SiC semiconductor devices due to the promise of lighter, smaller, and more efficient systems. Since the first SiC power device was released to the commercial market (SiC Schottky diode in 2001), there has been an extensive effort to transfer other SiC power devices from the R&D labs. [1]. These devices include the metal-oxide-semiconductor field effect transistor (MOSFET), junction

field effect transistor (JFET), static induction transistor (SIT), gate-turn-off (GTO) thyristor, and bipolar junction transistor (BJT). With these SiC power devices the potential is present to develop highly miniaturized electronics modules and packages that will revolutionize the power electronics industry.

The desire to use SiC power electronics to miniaturize power converters also leads to the necessity of high-temperature control and gate drive circuits. The ultimate desire would be to use SiC control/digital ICs with SiC power switches and/or integrate SiC control with the SiC power switches. Since SiC control is not expected in the near future, SOI control electronics is the next best option for higher temperature operation.

Silicon Carbide (SiC)

SiC is a wide bandgap semiconductor material capable of high temperature operation theoretically up to ~600 °C. When compared to silicon based devices, SiC can operate at higher temperatures (approximately 5 times higher than Si), possess a higher breakdown voltage (10 times that of Si), possess lower switching losses, and are capable of higher current densities (approximately 3-4 times higher than Si). The potential applications of SiC are widespread and all encompassing in the area of power electronics. Some applications include military and space exploration vehicles, more electric aircraft, electric and hybrid-electric vehicles, nuclear power reactors, and petroleum and geological exploration instrumentation. Ultimately, any system that would see improvement from high-density or high efficiency power electronics would benefit from SiC.

Silicon on Insulator (SOI)

Typical bulk Si integrated circuits (ICs) and power devices are designed to operate at temperatures not exceeding 75 °C while military grade ICs and devices typically operate up to

125 °C. Beyond these temperatures, the device will cease to function according to specification or completely fail. Effects such as current leakage and decreased threshold voltages occur at elevated temperatures, resulting in MOSFETs that fail to turn off or experience thermal runaway. To reduce these effects associated with high-temperatures in Si devices, an insulating oxide layer can be utilized to create Silicon-on-Insulator (SOI).

A basic SOI building block consists of three layers; a silicon substrate, a buried oxide such as silicon dioxide as an insulator, and a thin layer of silicon on the surface where the transistors are formed. SOI completely isolates the transistor from its neighboring transistors and other circuit components with a layer of insulator material. This reduces the junction capacitance, which in turn reduces the amount of current required to switch a device [2]. In general, SOI devices are 25%-30% faster, have lower supply voltages, are more densely packed, are more immune to latch-up, and have leakage currents that are reduced by 100-1000 times at high- temperatures over bulk Si devices [3]. Additionally, some SOI devices have been characterized up to 500 °C [4].

II. HIGH-TEMPERATURE THREE-PHASE MCPM MOTOR DRIVE

Researchers at APEI, Inc. and the University of Arkansas have performed extensive research in the area of SiC device applications, packaging, and modeling for power electronic systems. Two high-temperature applications the researchers are currently working on are: (1) three-phase motor drives for use in geological exploration and (2) three-phase motor drives for use in the US Army's Future Combat Systems (FCS) vehicles.

Energy companies are interested in SiC power electronics for deep earth petroleum exploration where hostile environments with high ambient temperatures are encountered. The down hole orbital vibrator (DHOV) from Cole Egineering requires the integration of a high-

temperature motor drive with a three-phase induction machine in order to perform deep earth geological mapping. It is difficult to place Si electronics down hole because of the extreme environment found within the oil wells. With SiC and SOI electronics, it is possible to send the electronics down hole with the motor, thus greatly improving motor drive control and efficiency.

The goal of the U.S. Army's FCS hybrid-electric combat vehicles is to decrease vehicle weight (by as much as one-half), increase maneuverability, and increase survivability over today's state of the art systems. Another goal of the FCS program is to have ready by the year 2020 a fully electric combat force [5]. In order to accomplish these goals, the vehicles must use high-power converters and motor drives that are capable of operating in harsh environments. By utilizing SiC power devices, high power densities can be achieved with little or no heatsinking, thus reducing the size and weight of the converters, thereby reducing the overall size and weight of the combat vehicle.

A. MCPM Electrical Design

The electrical design of the MCPM stems from a demonstration three-phase motor control developed by APEI, Inc. for high temperature operation. The high-temperature motor controller shown in Figure 1 operated in an ambient environment of 250 °C and is detailed in [6]. Figure 2 illustrates the circuit block diagram of the current MCPM design. The core control block (block 1) contains an SOI microcontroller, latch, SRAM, and in-house developed software to generate the control signals required for a three-phase motor drive. The MCPM design contains start up circuitry to deliver power from the DC bus to the low voltage control logic (block 2). Another feature of the MCPM design is the feedback of critical conditions such as over voltage, current, and temperature (block 3). Block 4 takes the low voltage digital signals from the microcontroller and amplifies the voltage and current to drive the isolation transformers

in block 5. Block 6 can be customized to drive different types of power switches. In this case the design drives the gate of a JFET from -15 V (fully off) to +5 V (fully on). The JFET gate drive circuitry also ensures that there is adequate dead-time between the high and low side switches.

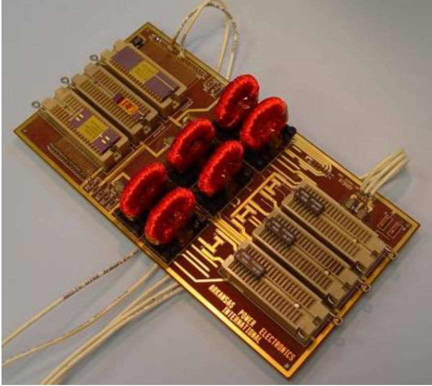

Figure 1. 250 °C 3-phase motor control prototype.

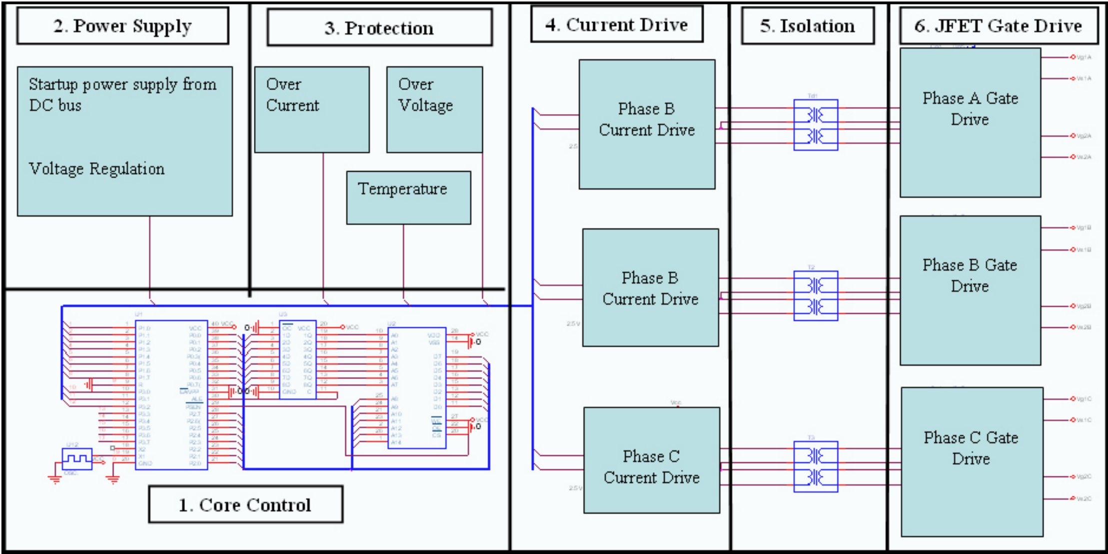

Figure 2. MCPM motor drive electrical design.

B. MCPM Mechanical Design

Since SiC devices are capable of operating into the GHz frequency range, a great reduction in the size of passive components such as capacitors, inductors, and other magnetic

components is expected. Integrating control and power layers into a single module significantly reduces size, weight, and parasitic effects. This approach is known as a multichip power module where multiple layers would be utilized to separate the power and control circuitry [7-10]. Figure 3 illustrates a cross-section of the MCPM design while Figure 4 illustrates an isometric view. The MCPM is built in two major stages. The first stage consists of the direct-bond-copper (DBC) power substrate, where gold plated copper plates are directly bonded to either side of an AlN ceramic substrate. The metallization traces on this power substrate are designed specifically for the capability to transmit large amounts of current at high voltages.

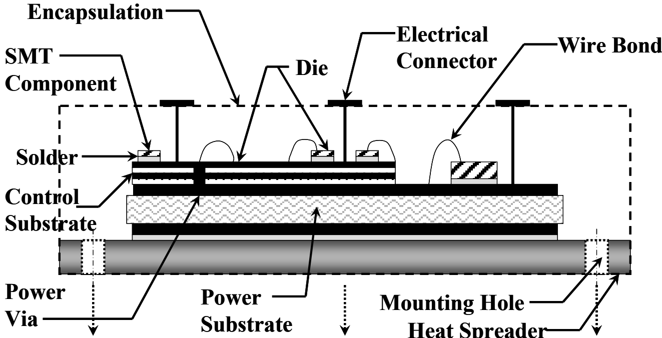

Figure 3. Cross-section of a possible SiC MCPM design.

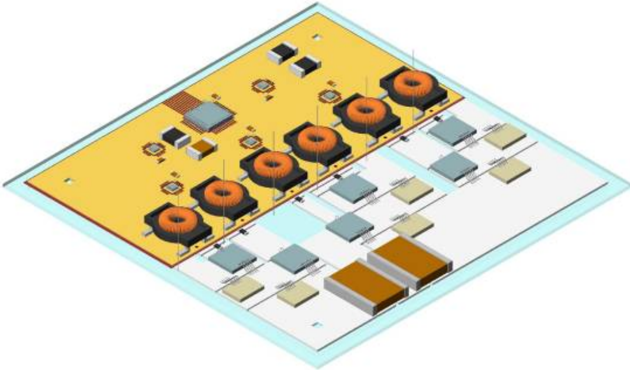

Figure 4. Isometric of high-temperature MCPM.

The high power bare-die SiC devices are mounted with a 300 °C 92.5Pb-5In-2.5Ag solder directly to the AlN DBC substrate, where a good thermal path can be traced to the heatspreader. Because of the demanding power and thermal requirements, the power substrate metallization traces can not be tightly patterned for high density control electronics. Instead, the control board is fabricated from a high temperature multilayer polyimide substrate. The metallization traces on these layers are flash gold plated for improved reliability. The control components are bare-die devices (wirebonded with high reliability gold wire), surface mount passives, and magnetic components. The control board is mounted to the high power substrate by a high temperature adhesive laminate. The heatspreader of the MCPM is a metal-matrix-composite material (such as AlSiC), which is a ceramic matrix injected with a metal. These heatspreader materials offer excellent thermal conduction capabilities while simultaneously providing a close CTE match to the DBC ceramic substrate (thus reducing stresses and the chances of thermal cycle / thermal shock failures).

III. THERMAL MODELING

To verify the MCPM design for high-temperature operation, Flotherm software was used to thermally model the MCPM with the SiC power JFETs and the SOI control devices. Figure 5 shows the model containing the DBC and polyimide boards, the SiC and SOI devices, and the heatsink and heat spreader. Figure 6 shows the SiC JFETS operating at a junction temperature of 307 °C and the SOI devices at a junction temperature of 240 °C. This simulation was designed to illustrate the limits of the power density. The die attach used for the SiC JFETs can not exceed 310 °C and therefore the max power this MCPM can deliver while keeping the JFETs to approximately 300 °C is 3.6 kW.

To clearly illustrate the advantages of this SiC/SOI MCPM, another simulation using the same heatsink and geometrical/mechanical design, but with Si control electronics and Si power switches, is shown in Figure 7. The junction temperature of the Si power switches is kept to approximately 150 °C (154 °C in the simulation) which is the max junction temperature of Si power devices. With the Si power devices operating at their max temperature the maximum power delivered by the converter is approximately 1.3 kW. This clearly illustrates a power density increase of approximately 3× through the use of high-temperature SiC and SOI technology.

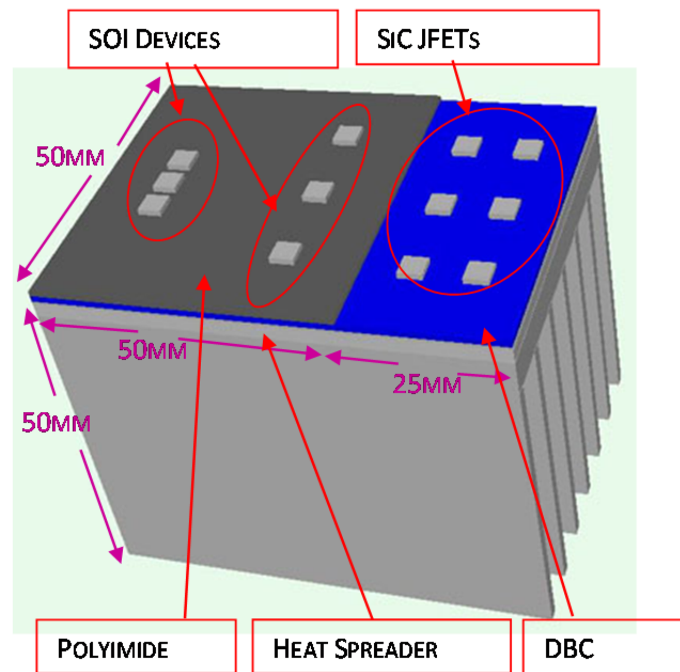

Figure 5. Flotherm model of the MCPM.

Testing Results

In order to demonstrate proof of concept and feasibility, a simple high-temperature MCPM prototype shown in Figure 8 was built and tested. The prototype is a half-bridge topology with the integrated SOI control electronics. Four SiC power JFETs are placed in parallel on the

high and low sides of the half-bridge, respectively, while two SiC Schottky's are placed in parallel on each side to act as free-wheeling diodes. These power devices are mounted to an AlN DBC substrate that is mounted to a low CTE AlSiC heatspreader. The control circuitry including the SOI devices and passive components are mounted to a multilayer polyimide PCB that is attached to the DBC substrate.

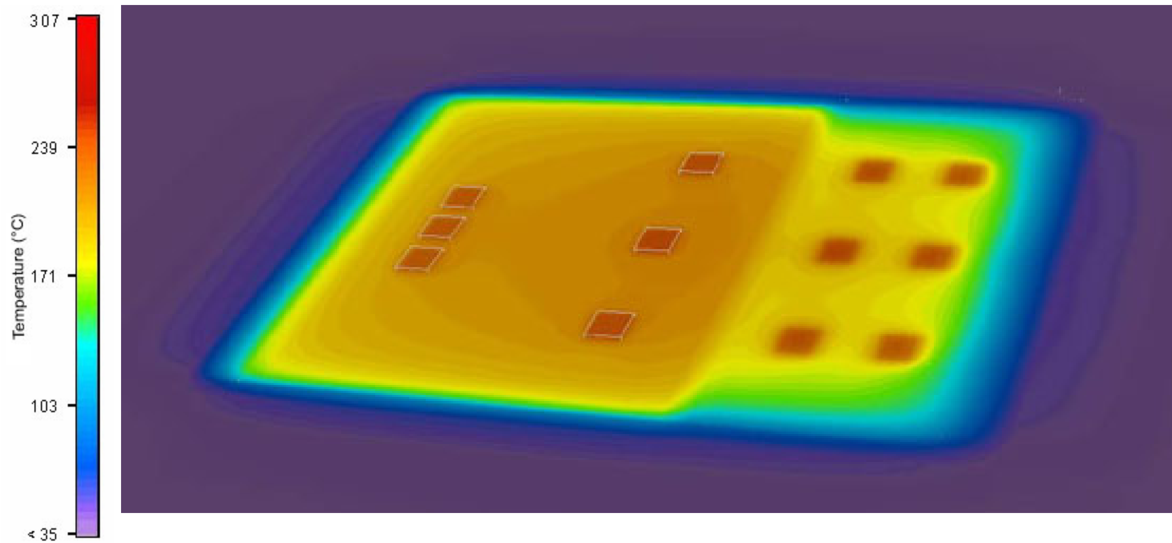

Figure 6. Flotherm simulation of 3-phase MCPM, SiC power device temperature 307 °C, SOI device temperature = 240 °C, power = 3.6 kW.

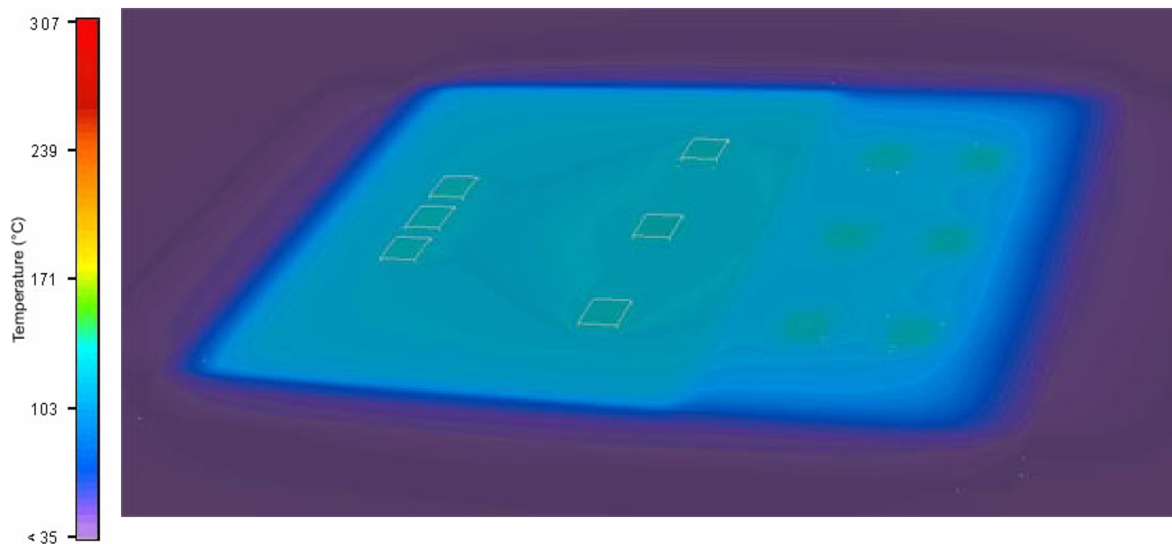

Figure 7. Flotherm simulation of 3-phase MCPM. Si power device temperature = 154 °C, Si IC device temperature = 132 °C, power = 1.3 kW.

Figure 9 illustrates an oscilloscope capture of the prototype operating under 250 °C environmental conditions. Ch2 (blue) is the input to the high-side isolation transformer, Ch3 (magenta) is the high side power switch gate to source voltage, and Ch4 (green) is the low-side power switch gate to source voltage. The JFET is a normally on device (usually on at Vgs = 0 V) and requires a negative voltage to turn it off. The gate drive circuitry in the MCPM switches between approximately -13 V to +7 V. Figures 10 & 11 are oscilloscope captures illustrating dead-time of 80ns and 108 ns between both the turn on and turn off of the half-bridge switches.

The full 3-phase MCPM motor drive with integrated SOI control electronics and SiC JFETs is currently being fabricated by the researchers. The MCPM will be capable of driving a 3-phase induction machine up to 3kW at temperatures in excess of 250 °C. Complete results for the high-temperature 3-phase MCPM motor drive will be given in the presentation at the conference.

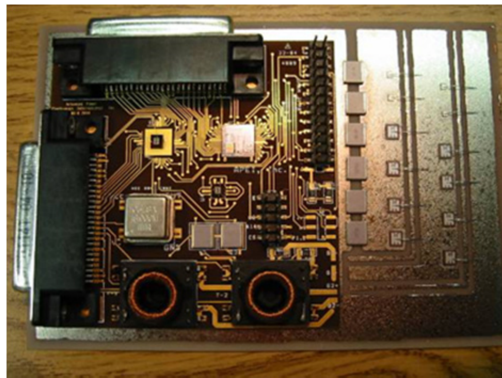

Figure 8. Single-phase MCPM SOI/SiC prototype.

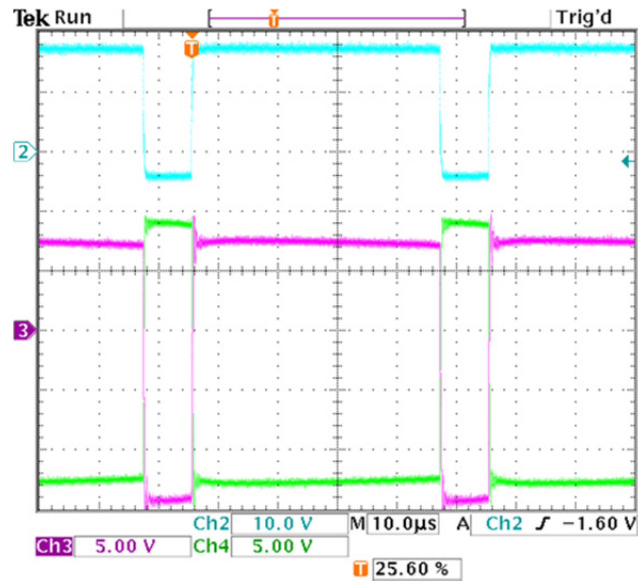

Figure 9. Vgs of JFET drive half-bridge signals.

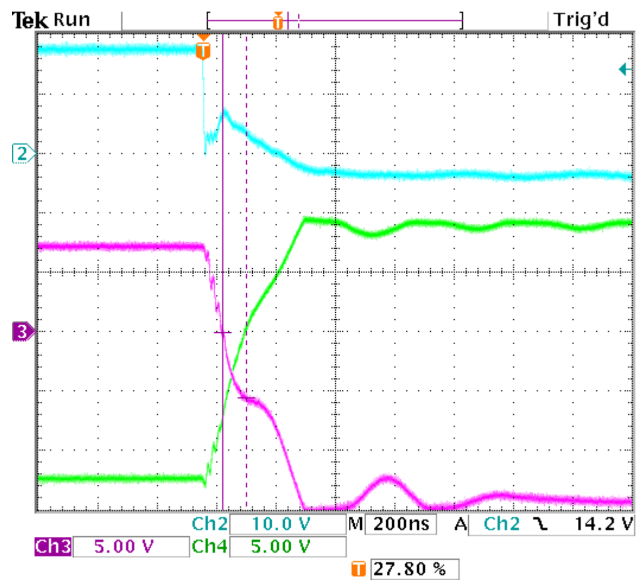

Figure 10. Deadtime = 80 ns.

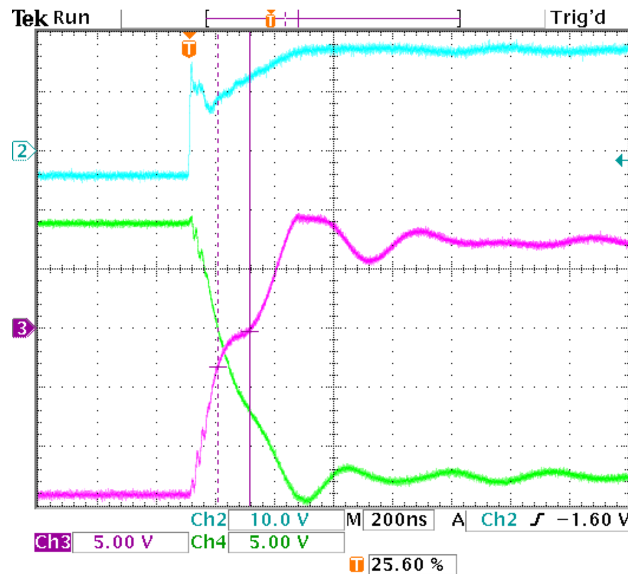

Figure 11. Deadtime = 108 ns.

ACKNOWLEDGMENT

The work presented in this paper was funded in part by the U.S. Army Research Laboratories and the U.S. National Science Foundation.

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CHAPTER 6

HIGH-TEMPERATURE INTEGRATION OF SILICON CARBIDE (SIC) AND SILICON-ON-INSULATOR (SOI) ELECTRONICS IN MULTICHIP POWER MODULES (MCPMS)

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W. Brown, and A.B. Lostetter

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Acknowledgments

The work presented in this paper was funded in part by the U.S. Army Research Laboratories and the U.S. National Science Foundation.

Keywords

Silicon carbide (SiC), Silicon on Insulator (SOI), High-temperature electronics, High-temperature packaging

Abstract

Arkansas Power Electronics International, Inc, (APEI, Inc.) and University of Arkansas researchers have developed a novel, highly miniaturized motor drive capable of operation in excess of 250 °C. The high-temperature multichip power module (MCPM) integrates silicon carbide (SiC) JFET power transistors with high-temperature MOS silicon-on-insulaor (SOI) control electronics into a single, highly miniaturized and compact power package. This paper will outline the design philosophy behind the high-temperature MCPM, discuss the high-temperature packaging technologies (including substrate selection, wirebonding, and die attach) developed and employed for module fabrication, illustrate thermal modeling results of the package, and present the results of prototype testing (demonstrating functionality).

Introduction

The future of power electronics will be greatly influenced by the commercialization of SiC semiconductor devices due to the promise of lighter, smaller, and more efficient systems. Since the first SiC power device was released to the commercial market (SiC Schottky diode in 2001), there has been an extensive effort to transfer other SiC power devices from the R&D labs. [1]. These devices include the metal-oxide-semiconductor field effect transistor (MOSFET), junction field effect transistor (JFET), static induction transistor (SIT), gate-turn-off (GTO) thyristor, and bipolar junction transistor (BJT). With these SiC power devices the potential is present to develop highly miniaturized electronics modules and packages that will revolutionize the power electronics industry.

The desire to use SiC power electronics to miniaturize power converters also leads to the necessity of high-temperature control and gate drive circuits. The ultimate desire would be to use SiC control/digital ICs with SiC power switches and/or integrate SiC control with the SiC power switches. Since SiC control is not expected in the near future, SOI control electronics is the next best option for higher temperature operation.

Silicon Carbide (SiC)

SiC is a wide bandgap semiconductor material capable of high temperature operation theoretically up to ~600 °C. When compared to silicon based devices, SiC can operate at higher temperatures (approximately 5 times higher than Si), possess a higher breakdown voltage (10 times that of Si), possess lower switching losses, and are capable of higher current densities (approximately 3-4 times higher than Si). The potential applications of SiC are widespread and all-encompassing in the area of power electronics. Some applications include military and space exploration vehicles, more electric aircraft, electric and hybrid-electric vehicles, nuclear power

reactors, and petroleum and geological exploration instrumentation. Ultimately, any system that would see improvement from high-density or high efficiency power electronics would benefit from SiC.

Silicon on Insulator (SOI)

Typical bulk Si integrated circuits (ICs) and power devices are designed to operate at temperatures not exceeding 75 °C while military grade ICs and devices typically operate up to 125 °C. Beyond these temperatures, the device will cease to function according to specification or completely fail. Effects such as current leakage and decreased threshold voltages occur at elevated temperatures, resulting in MOSFETs that fail to turn off or experience thermal runaway. To reduce these effects associated with high-temperatures in Si devices, an insulating oxide layer can be utilized to create Silicon-on-Insulator (SOI).

A basic SOI building block consists of three layers; a silicon substrate, a buried oxide such as silicon dioxide as an insulator, and a thin layer of silicon on the surface where the transistors are formed. SOI completely isolates the transistor from its neighboring transistors and other circuit components with a layer of insulator material. This reduces the junction capacitance, which in turn reduces the amount of current required to switch a device [2]. In general, SOI devices are 25%-30% faster, have lower supply voltages, are more densely packed, are more immune to latch-up, and have leakage currents that are reduced by 100-1000 times at high-temperatures over bulk Si devices [3]. Additionally, some SOI devices have been characterized up to 500 °C [4].

High-Temperature Three-Phase MCPM Motor Drive

Researchers at APEI, Inc. and the University of Arkansas have performed extensive research in the area of SiC device applications, packaging, and modeling for power electronic

systems. Two high-temperature applications the researchers are currently working on are: (1) three-phase motor drives for use in geological exploration and (2) three-phase motor drives for use in the US Army's Future Combat Systems (FCS) vehicles.

Energy companies are interested in SiC power electronics for deep earth petroleum exploration where hostile environments with high ambient temperatures are encountered. The down hole orbital vibrator (DHOV) from Cole Egineering requires the integration of a high-temperature motor drive with a three-phase induction machine in order to perform deep earth geological mapping. It is difficult to place Si electronics down hole because of the extreme environment found within the oil wells. With SiC and SOI electronics, it is possible to send the electronics down hole with the motor, thus greatly improving motor drive control and efficiency.

The goal of the U.S. Army's FCS hybrid-electric combat vehicles is to decrease vehicle weight (by as much as one-half), increase maneuverability, and increase survivability over today's state of the art systems. Another goal of the FCS program is to have ready by the year 2020 a fully electric combat force [5]. In order to accomplish these goals, the vehicles must use high-power converters and motor drives that are capable of operating in harsh environments. By utilizing SiC power devices, high power densities can be achieved with little or no heatsinking, thus reducing the size and weight of the converters, thereby reducing the overall size and weight of the combat vehicle.

MCPM Electrical Design

The electrical design of the MCPM stems from a demonstration three-phase motor control developed by APEI, Inc. for high temperature operation. The high-temperature motor controller shown in Figure 1 operated in an ambient environment of 250 °C and is detailed in [6]. Figure 2 illustrates the circuit block diagram of the current MCPM design. The core control

block (block 1) contains an SOI microcontroller, latch, SRAM, and in-house developed software to generate the control signals required for a three-phase motor drive. The MCPM design contains start up circuitry to deliver power from the DC bus to the low voltage control logic (block 2). Another feature of the MCPM design is the feedback of critical conditions such as over voltage, current, and temperature (block 3). Block 4 takes the low voltage digital signals from the microcontroller and amplifies the voltage and current to drive the isolation transformers in block 5. Block 6 can be customized to drive different types of power switches. In this case the design drives the gate of a JFET from -15 V (fully off) to +5 V (fully on). The JFET gate drive circuitry also ensures that there is adequate dead-time between the high and low side switches.

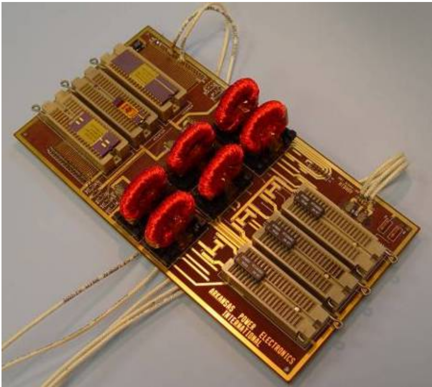


Figure 1. 250 °C 3-phase motor control prototype.

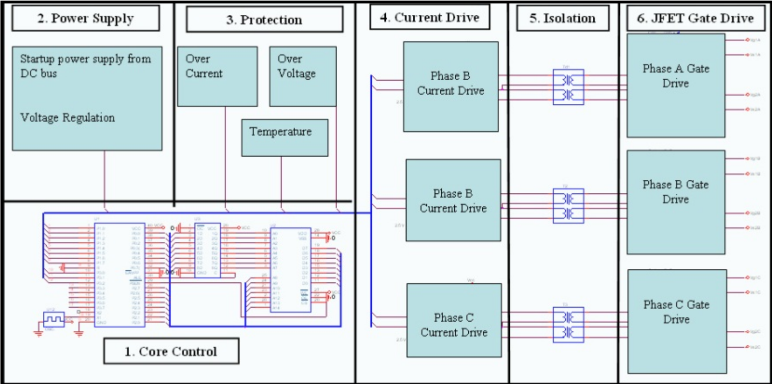


Figure 2. MCPM motor drive electrical design.

MCPM Mechanical Design

Since SiC devices are capable of operating into the GHz frequency range, a great reduction in the size of passive components such as capacitors, inductors, and other magnetic components is expected. Integrating control and power layers into a single module significantly reduces size, weight, and parasitic effects. This approach is known as a multichip power module where multiple layers would be utilized to separate the power and control circuitry [7-9]. Figure 3 illustrates a cross-section of the MCPM design while Figure 4 illustrates an isometric view. The MCPM is built in two major stages. The first stage consists of the direct-bond-copper (DBC) power substrate, where gold plated copper plates are directly bonded to either side of an AlN ceramic substrate. The metallization traces on this power substrate are designed specifically for the capability to transmit large amounts of current at high voltages.

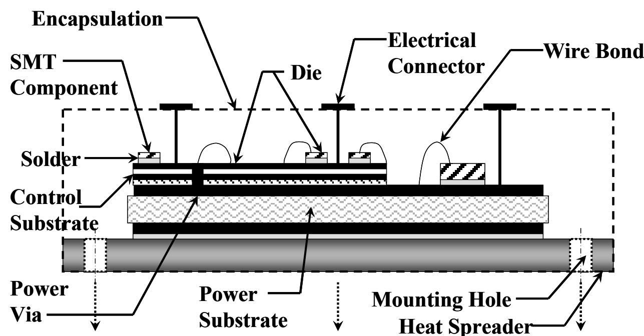


Figure 3. Cross-section of a possible SiC MCPM design.

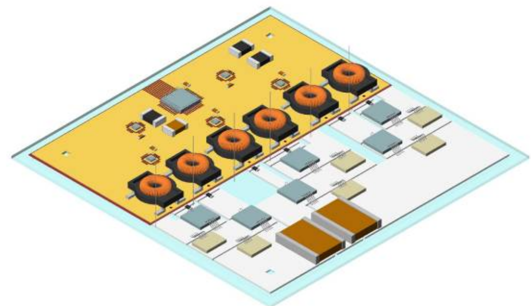


Figure 4. Isometric of high-temperature MCPM.

The high power bare-die SiC devices are mounted with a 300 °C 92.5Pb-5In-2.5Ag solder directly to the AlN DBC substrate, where a good thermal path can be traced to the heatspreader. Because of the demanding power and thermal requirements, the power substrate metallization traces can not be tightly patterned for high density control electronics. Instead, the control board is fabricated from a high temperature multilayer polyimide substrate. The

metallization traces on these layers are flash gold plated for improved reliability. The control components are bare-die devices (wirebonded with high reliability gold wire), surface mount passives, and magnetic components. The control board is mounted to the high power substrate by a high temperature adhesive laminate. The heatspreader of the MCPM is a metal-matrix-composite material (such as AlSiC), which is a ceramic matrix injected with a metal. These heatspreader materials offer excellent thermal conduction capabilities while simultaneously providing a close CTE match to the DBC ceramic substrate (thus reducing stresses and the chances of thermal cycle / thermal shock failures).

High Temperature Packaging

Substrates

Aluminum Nitride (AlN) is an ideal high power substrate and is a possible candidate for packaging silicon carbide devices due to its excellent electrical properties and chemical stability. It possesses a high thermal conductivity with a low CTE that matches SiC, minimizing the thermal stresses experienced under power operation. Typically, the copper on AlN DBC power substrates is plated with gold and/or nickel in order to reduce oxidization. The Ni is often used as a diffusion barrier, blocking the migration of copper into the surface gold layer, and thus helping to prevent oxidation. The nickel layer itself experiences accelerated diffusion at temperatures in excess of 300 º C, thus limiting its capability to block copper diffusion at high temperatures [10]. The AlN DBCs in this experiment were Ni plated with an electroless nickel phosphide solution containing 6-8% phosphorus. At temperatures above 350 ºC, the nickel phosphide-plated layer separates into nickel and phosphorous. The phosphorous then appears on the surface, contaminating component interconnects and significantly reducing long term reliability. Energy Dispersive X-ray (EDX) analysis was performed on the surface of a nickel-plated AlN substrate

before and after 400 °C annealing. The EDX graphs in Figures 5 & 6 show the phosphorous peak before and after thermal cycling of the nickel-plated AlN substrate. The EDX determines the elemental composition of the object under test; the x-axis on the graph produced by EDX represents the acceleration voltage in kV, elements that are farther in depth on the substrate are represented at higher voltages. The y-axis illustrates the weight or atomic percent composition of the elements and is determined by the intensity of the x-ray peak. Figure 5 shows the majority of the substrate surface to be Ni with a small percent (between 6-8%) of phosphorus as expected. Figure 6 after 400 °C annealing shows the phosphorus to be at a much higher percentage (between 15 & 20%) because of the break up of the nickel phosphide. Figure 7 shows the substrate before (left) and after (right) 400 °C annealing.

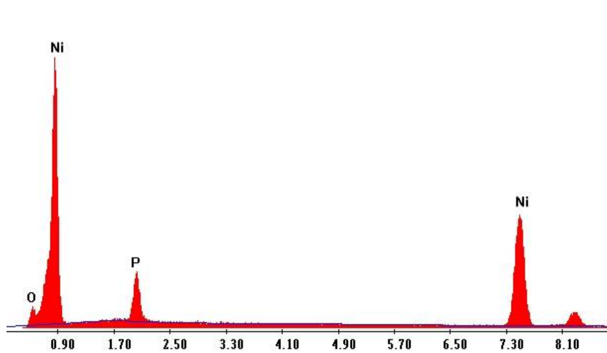


Figure 5. EDX analysis of AlN substrate before thermal cycling.

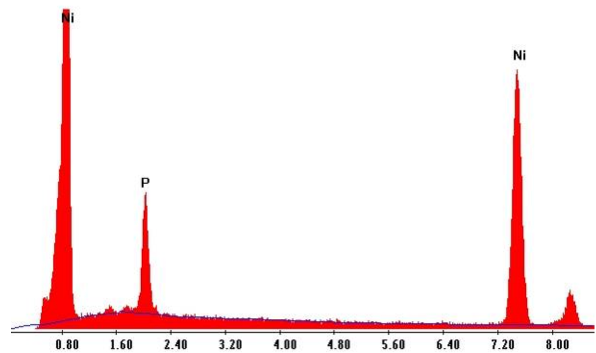


Figure 6. EDX of AlN substrate after 400 º C thermal cycling.

The breakdown of nickel phosphide in high-temperature environments has led the researchers to investigate other materials for use as a diffusion barrier for extreme temperature environments. Materials that show promise for use as a diffusion barrier on AlN are refractory metals such as Ti, Mo, and their alloys. Titanium tungsten (TiW) and tungsten carbide (WC) are favorable candidates because of their low contact resistance and thermo-dynamical stability. The

researchers are currently investigating two complete metallization schemes that include these alloys on AlN for high temperature applications.

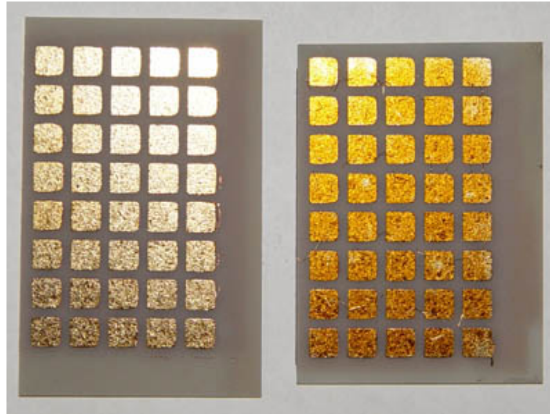


Figure 7. AlN substrate before (left) and after (right) 400 °C annealing.

Titanium – tungsten Diffusion Barrier

To study the diffusion barrier characteristics of titanium-tungsten, 3000 Å thick film of TiW was deposited on a 1000 Å thick Ti layer on copper metallized AlN substrates by sputtering at room temperature using a W-Ti (10 %) target. A subsequent Au layer of 1500 Å was sputtered on the film. The multilayer film was then subjected to thermal cycling at temperatures up to 400 ºC in both air and nitrogen environments. An EDX was performed before and after thermal annealing to determine the elemental composition of the multilayer. Figure 8 is the EDX of the substrate before annealing, Figure 9 is the EDX of the substrate after annealing in a nitrogen environment, and Figure 10 is the EDX of the substrate after annealing in air. These figures show only slight changes in the surface elemental content before and after annealing. Additionally, there is no change between a nitrogen environment and air, thus presenting the possibility of avoiding hermetic sealing.

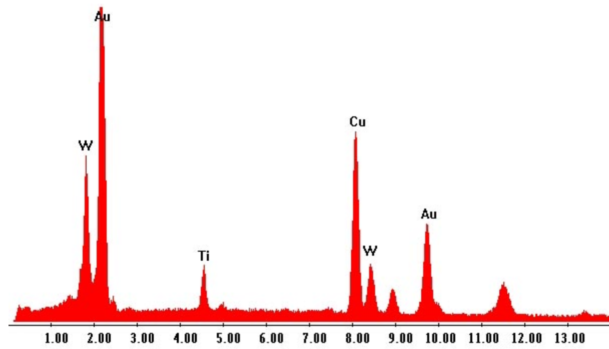


Figure 8. EDX of TiW diffusion barrier before cycling.

Tungsten Carbide (WC) Diffusion Barrier

Currently under investigation is WC as a high-temperature diffusion barrier. Preliminary tests show WC as a good high-temperature diffusion barrier. Complete results on WC will be presented at the conference.

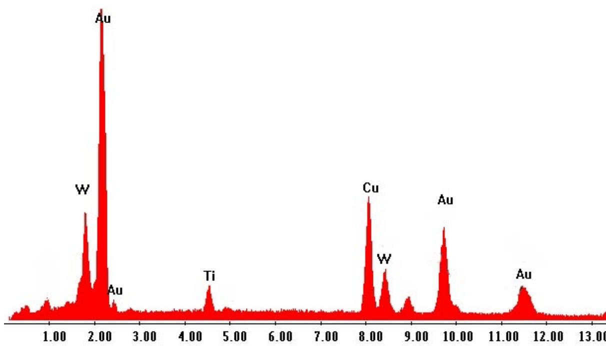


Figure 9. EDX of TiW diffusion barrier after 400 °C cycling in nitrogen.

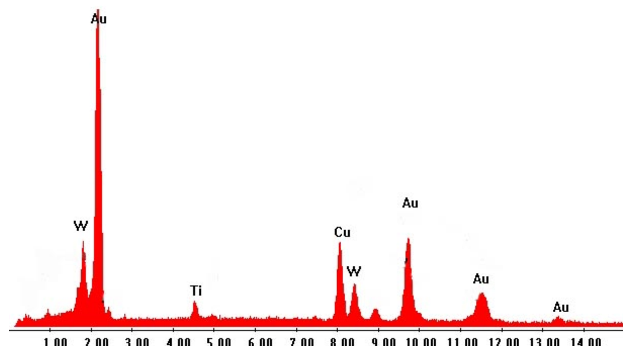


Figure 10. EDX of TiW diffusion barrier after 400 °C cycling in air.

Wirebonding

After attaching the SiC and SOI bare die components to their substrates, the devices must be electrically connected to the board. UA has performed several experiments with the reliability of wirebonding for use in high-temperatures. Among other past results [11], current experiments include the investigation of three mil gold wire-bonding for high temperature electronics.

The test sample consisted of 3 electroless deposited Au/Ni on copper metallized AlN substrates. Each substrate contained a large number of three mil Au wirebonds to give a large sample for testing. Substrate 1 acted as a control substrate and was not thermally cycled. Substrate 2 was cycled between -55 C and 300 C ten times at ten minutes per cycle. Substrate 3 was cycled similarly to that of substrate 2 with the exception of the temperature ranging from -55 C to 400 C. Substrates 2 & 3 were placed in a furnace in a N2 environment for the high temperature and then transferred to a liquid N2 environmental cold chamber for the low temperature. The transfer time from hot to cold did not exceed one minute. Each test was conducted according to U.S. MIL-STD-883E, method 1010.7 [12].

Figure 11 shows a scanning electron microscope (SEM) picture of a wirebond on substrate 2 before thermal cycling and Figure 12 shows the same wirebond unaffected after thermal cycling (however, notice the presence of cracks in the metallized substrate due to thermal cycling).

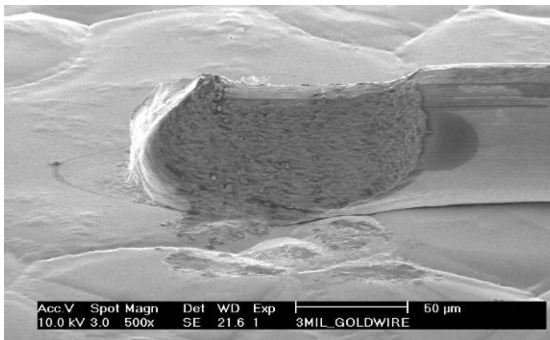


Figure 11. 3-mil gold wire wedge bond before thermal cycling.

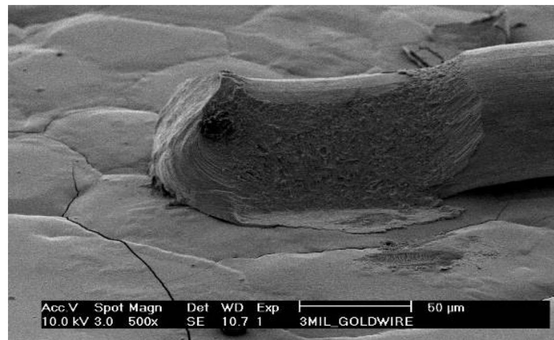


Figure 12. 3 mil gold wire wedge bond after thermal cycling.

After thermal cycling, a series of samples were prepared for destructive pull tests. Each wire bond was tested in accordance with MIL-STD-883C, method 2011.6. The average loop distance was held constant at 2.5 mm. The wire length from pad to pad was approximately 5

mm. A pull force was applied in the center of the wire loop to break the wire bond in a direction normal to the bond pad. A 0 to 2000 gram force gauge was used to measure the force required to break each bond. The average pull strengths are shown in Figure 13 for each temperature cycle. U.S. Mil-STD-883C method 2011.6 requires a minimum bond strength of 15 grams force (gf) in order for the bond to pass testing. Thermal cycling tends to weaken the bond strength due to the expanding and contracting of the wires. This can be seen from the room temperature bond strength of 85 gf to the bond strength of 75 gf after 300 °C cycling. For 3-mil gold wire, the average bond strength after 400 °C cycling was approximately 65 gf, which is acceptable and well above the military standard.

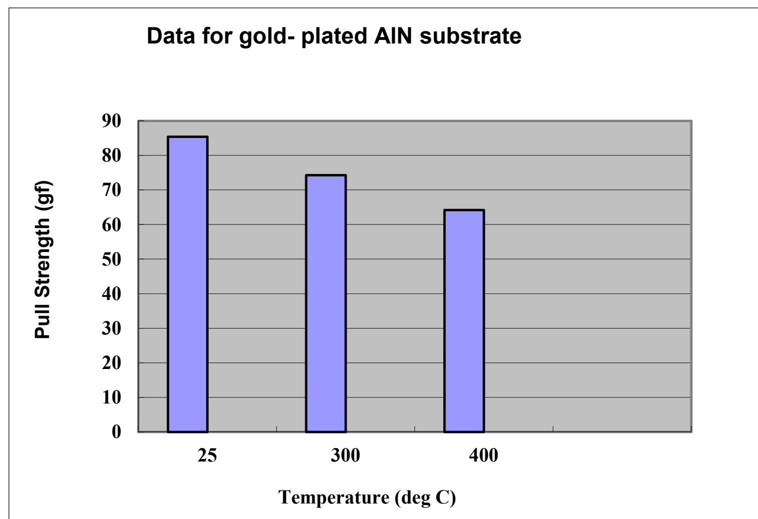


Figure 13. Pull strengths of 3-mil Au wirebonds.

Thermal Modeling

To verify the MCPM design for high-temperature operation, Flotherm software was used to thermally model the MCPM with the SiC power JFETs and the SOI control devices. Figure 14 shows the model containing the DBC and polyimide boards, the SiC and SOI devices, and the heatsink and heat spreader. Figure 15 shows the SiC JFETS operating at a junction temperature of 307 °C and the SOI devices at a junction temperature of 240 °C. This simulation was designed

to illustrate the limits of the power density. The die attach used for the SiC JFETs can not exceed 310 °C and therefore the max power this MCPM can deliver while keeping the JFETs to approximately 300 °C is 3.6 kW.

To clearly illustrate the advantages of this SiC/SOI MCPM, another simulation using the same heatsink and geometrical/mechanical design, but with Si control electronics and Si power switches, is shown in Figure 16. The junction temperature of the Si power switches is kept to approximately 150 °C (154 °C in the simulation) which is the max junction temperature of Si power devices. With the Si power devices operating at their max temperature the maximum power delivered by the converter is approximately 1.3 kW. This clearly illustrates a power density increase of approximately 3× through the use of high-temperature SiC and SOI technology.

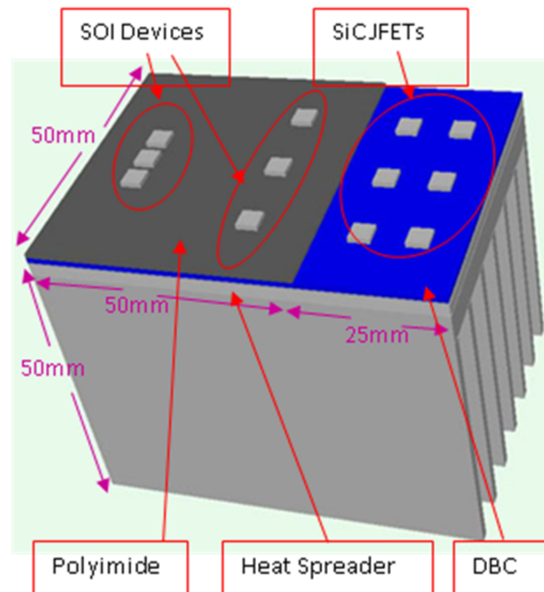
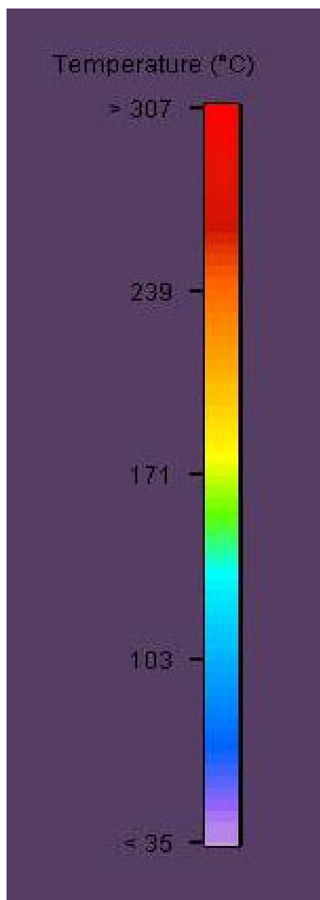


Figure 14. Flotherm model of the MCPM.

Testing Results

In order to demonstrate proof of concept and feasibility, a simple high-temperature MCPM prototype shown in Figure 17 was built and tested. The prototype is a half-bridge

topology with the integrated SOI control electronics. Four SiC power JFETs are placed in parallel on the high and low sides of the half-bridge, respectively, while two SiC Schottky's are placed in parallel on each side to act as free-wheeling diodes. These power devices are mounted to an AlN DBC substrate that is mounted to a low CTE AlSiC heatspreader. The control circuitry including the SOI devices and passive components are mounted to a multilayer polyimide PCB that is attached to the DBC substrate.



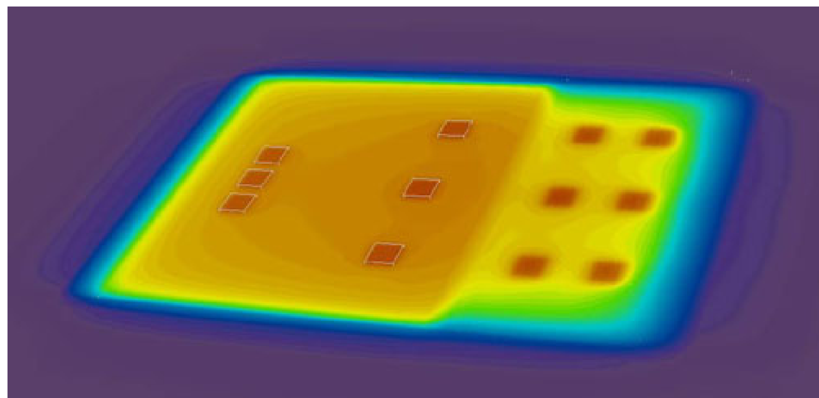


Figure 15. Flotherm simulation of 3-phase MCPM, SiC power device temperature 307 °C, SOI device temperature = 240 °C, power = 3.6 kW.

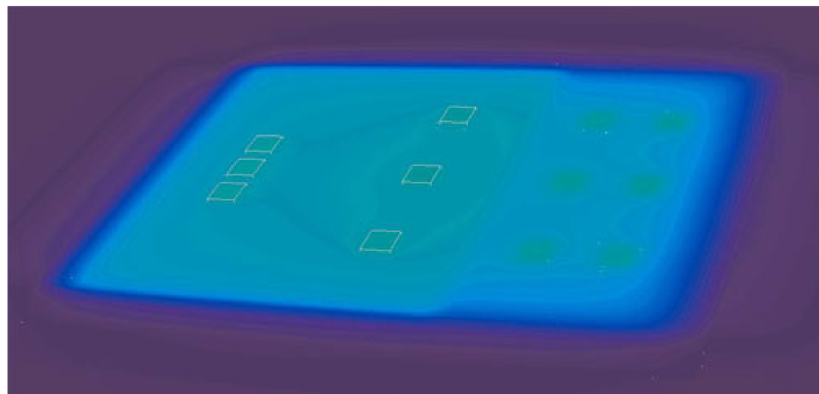


Figure 16. Flotherm simulation of 3-phase MCPM. Si power device temperature = 154 °C, Si IC device temperature = 132 °C, power = 1.3 kW.

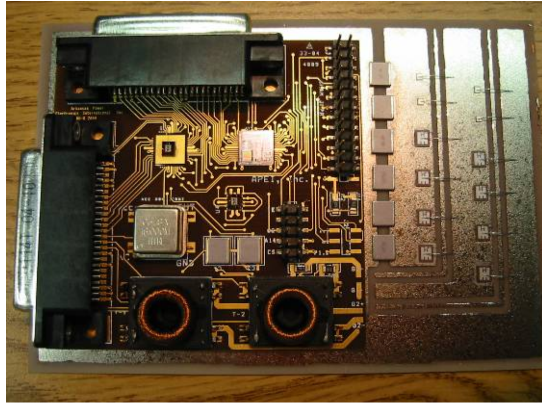


Figure 17. Single-phase MCPM SOI/SiC prototype.

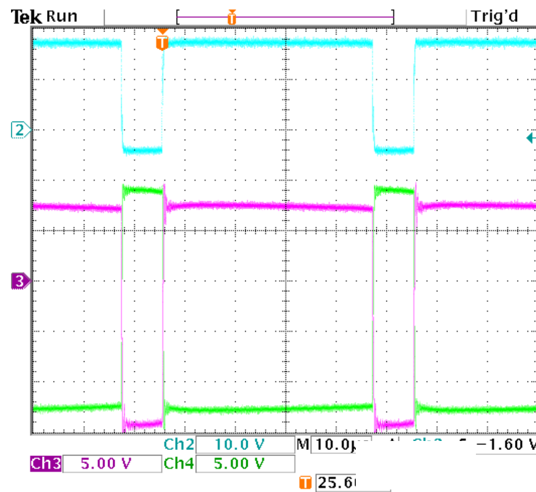


Figure 18. Vgs of JFET drive half-bridge signals.

Figure 18 illustrates an oscilloscope capture of the prototype operating under 250 °C environmental conditions. Ch2 (blue) is the input to the high-side isolation transformer, Ch3 (magenta) is the high side power switch gate to source voltage, and Ch4 (green) is the low-side power switch gate to source voltage. The JFET is a normally on device (usually on at Vgs = 0 V) and requires a negative voltage to turn it off. The gate drive circuitry in the MCPM switches between approximately -13 V to +7 V. Figures 19 & 20 are oscilloscope captures illustrating dead-time of 80ns and 108 ns between both the turn on and turn off of the half-bridge switches.

The full 3-phase MCPM motor drive with integrated SOI control electronics and SiC JFETs is currently being fabricated by the researchers. The MCPM will be capable of driving a 3-phase induction machine up to 3kW at temperatures in excess of 250 °C. Complete results for the high-temperature 3-phase MCPM motor drive will be given in the presentation at the conference.

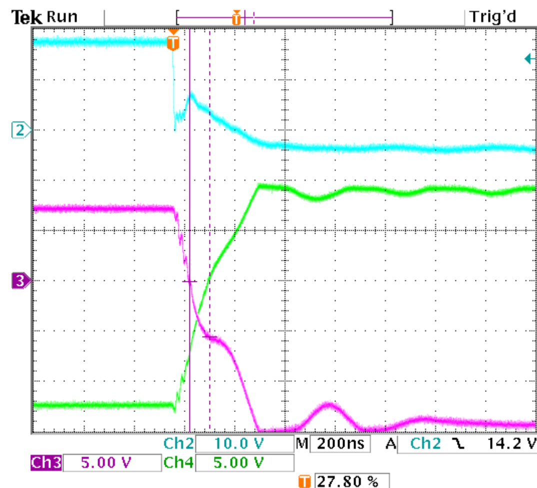


Figure 19. Deadtime = 80 ns.

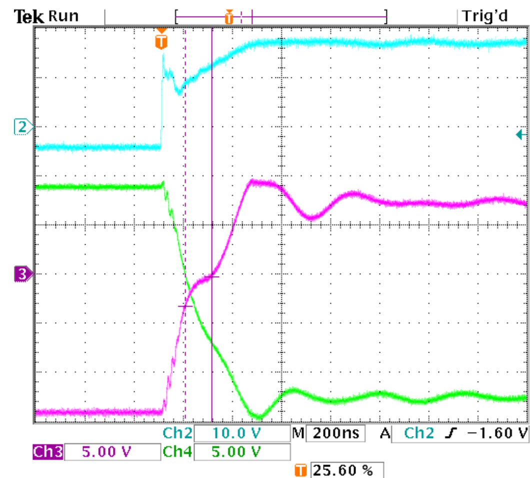


Figure 20. Deadtime = 108 ns.

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CHAPTER 7

PACKAGING OF A HIGH-TEMPERATURE SILICON CARBIDE (SIC) MULITCHIP POWER MODULE (MCPM)

J. M. Hornberger, B. McPherson, S.D. Mounce, R.M. Schupbach,

A.B. Lostetter, and H. Alan Mantooth

© 2005 IMAPS. Reprinted, with permission, from Hornberger et al, Packaging of a High-Temperature Silicon Carbide (SiC) Mulitchip Power Module (MCPM), International Symposium on Microelectronics, September 2005.

Abstract

Arkansas Power Electronics International, Inc, (APEI, Inc.) researchers have designed, developed, packaged, and manufactured the first complete multichip power module (MCPM) integrating SiC power transistors with silicon on insulator (SOI) control electronics. The MCPM is a 3 kW three-phase inverter that operates at temperatures in excess of 250 °C. Bare die HTMOS SOI control components have been integrated with bare die SiC power JFETs into a single compact module. The high-temperature operation of SiC switches allows for increased power density over silicon electronics by an order of magnitude, leading to highly miniaturized power converters. In this paper, the researchers will discuss the challenges associated with high-temperature operation of power electronics; present the electrical, mechanical, and thermal design of a high-temperature MCPM; discuss the multitude of packaging issues that were solved to reach high-temperature operation; illustrate the high power density and miniaturization achieved by the SiC MCPM; and present the experimental test results of the fully operational 3kW SiC MCPM.

Key words:

Silicon carbide (SiC), Silicon on Insulator (SOI), High-temperature electronics, High-temperature packaging, and Multichip power modules (MCPMs)

1.0 Introduction

The future of power electronics will be greatly influenced by the commercialization of SiC semiconductor devices due to the promise of lighter, smaller, and more efficient systems. Since the first SiC power device was released to the commercial market (SiC Schottky diode in 2001), there has been an extensive effort to transfer other SiC power devices from the R&D labs [1]. These devices include the metal-oxide-semiconductor field effect transistor (MOSFET), junction field effect transistor (JFET), static induction transistor (SIT), gate-turn-off (GTO) thyristor, and bipolar junction transistor (BJT). With these SiC power devices the potential is present to develop highly miniaturized electronics modules and packages that will revolutionize the power electronics industry.

The desire to use SiC power electronics to miniaturize power converters also leads to the necessity of high-temperature control, gate drive circuits, and passive components. The ultimate desire would be to use SiC control/digital ICs with SiC power switches and/or integrate SiC control with the SiC power switches. Since SiC control is not expected in the near future, SOI control electronics is the next best option for higher temperature operation.

1.1 Silicon Carbide

SiC is a wide bandgap semiconductor material capable of high temperature operation theoretically up to ~600 °C. When compared to silicon based devices, SiC can be utilized at much higher temperatures (approximately 5 times higher than Si), possess a higher breakdown voltage (10 times that of Si), possess lower switching losses, and are capable of higher current densities (approximately 3-4 times higher than Si). The potential applications of SiC are widespread and all encompassing in the area of power electronics. Some applications include military and space exploration vehicles, more electric aircraft, electric and hybrid-electric

vehicles, nuclear power reactors, and petroleum and geological exploration instrumentation. Ultimately, any system that would see improvement from high-density or high efficiency power electronics would benefit from SiC.

1.2 Silicon on Insulator

Typical bulk Si integrated circuits (ICs) and power devices are designed to operate at temperatures not exceeding 75 °C while military grade ICs and devices typically operate up to 125 °C. Beyond these temperatures, the device will cease to function according to specification or completely fail. Effects such as current leakage and decreased threshold voltages occur at elevated temperatures, resulting in MOSFETs that fail to turn off or experience thermal runaway. To reduce these effects associated with high-temperatures in Si devices, an insulating oxide layer can be utilized to create Silicon-on-Insulator.

A basic SOI building block consists of three layers; a silicon substrate, a buried oxide such as silicon dioxide as an insulator, and a thin layer of silicon on the surface where the transistors are formed. SOI completely isolates the transistor from its neighboring transistors and other circuit components with a layer of insulator material. This reduces the junction capacitance, which in turn reduces the amount of current required to switch a device [2]. In general, SOI devices are 25%-30% faster, have lower supply voltages, are more densely packed, are more immune to latch-up, and have leakage currents that are reduced by 100-1000 times at high-temperatures over bulk Si devices [3]. Additionally, some SOI devices have been characterized up to 500 °C [4].

2.0 High-Temperature Three-Phase MCPM Motor Drive

Researchers at APEI, Inc. and the University of Arkansas have performed extensive research in the area of SiC device applications, packaging, and modeling for power electronic

systems. Two high-temperature applications the researchers are currently working on are: (1) three-phase motor drives for use in geological exploration and (2) three-phase motor drives for use in the US Army's Future Combat Systems (FCS) vehicles.

Energy companies are interested in SiC power electronics for deep earth petroleum exploration where hostile environments with high ambient temperatures are encountered. The down hole orbital vibrator (DHOV) from Cole Engineering requires the integration of a high-temperature motor drive with a three-phase induction machine in order to perform deep earth geological mapping. It is difficult to place Si electronics down hole because of the extreme environment found within the oil wells. With SiC and SOI electronics, it is possible to send the electronics down hole with the motor, thus greatly improving motor drive control and efficiency.

The goal of the U.S. Army's FCS hybrid-electric combat vehicles is to decrease vehicle weight (by as much as one-half), increase maneuverability, and increase survivability over today's state of the art systems. Another goal of the FCS program is to have ready by the year 2020 a fully electric combat force [5]. In order to accomplish these goals, the vehicles must use high-power converters and motor drives that are capable of operating in harsh environments. By utilizing SiC power devices, high power densities can be achieved with little or no heatsinking, resulting in a reduction of the size and weight of the converters, thereby reducing the overall size and weight of the combat vehicle.

2.1 MCPM Electrical Design

The electrical design of the MCPM stems from a demonstration three-phase motor control developed by APEI, Inc. for high temperature operation. The high-temperature motor controller shown in Figure 1 operated in an ambient environment of 250 °C and is detailed in [6]. Figure 2 illustrates the circuit block diagram of the current MCPM design.

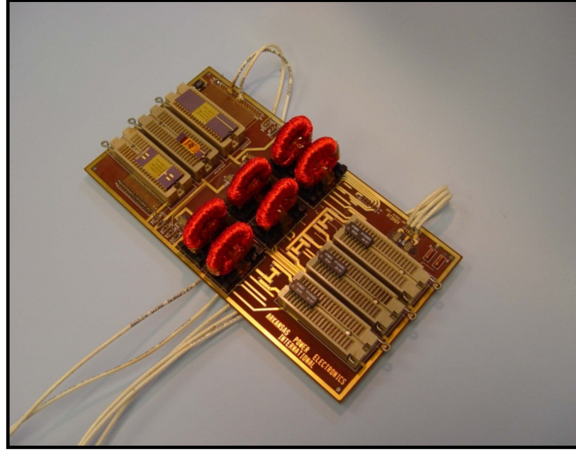

Figure 1: 250 °C 3-phase motor control prototype.

The core control block (block 1) contains an SOI microcontroller, latch, SRAM, and in-house developed software to generate the control signals required for a three-phase motor drive. The MCPM design contains start up circuitry to deliver power from the DC bus to the low voltage control logic (block 2). Another feature of the MCPM design is the feedback of critical conditions such as over voltage, current, and temperature (block 3). Block 4 takes the low voltage digital signals from the microcontroller and amplifies the voltage and current to drive the isolation transformers in block 5. Block 6 can be customized to drive different types of power switches. In this case the design drives the gate of a JFET from -15 V (fully off) to +5 V (fully on). The JFET gate drive circuitry also ensures that there is adequate dead-time between the high and low side switches.

2.2 MCPM Mechanical Design

SiC devices are capable of operating into the GHz frequency range; a great reduction in the size of passive components such as capacitors, inductors, and other magnetic components is expected. Integrating control and power layers into a single module significantly reduces size, weight, and parasitic effects. This approach is known as a multichip power module where multiple layers would be utilized to separate the power and control circuitry [7-10]. Figure 3

illustrates a cross-section of the MCPM design while Figure 4 illustrates an isometric view. The MCPM is built in two major stages. The first stage consists of the direct-bond-copper (DBC) power substrate, where gold plated copper plates are directly bonded to either side of an AlN ceramic substrate. The metallization traces on this power substrate are designed specifically for the capability to transmit large amounts of current at high voltages.

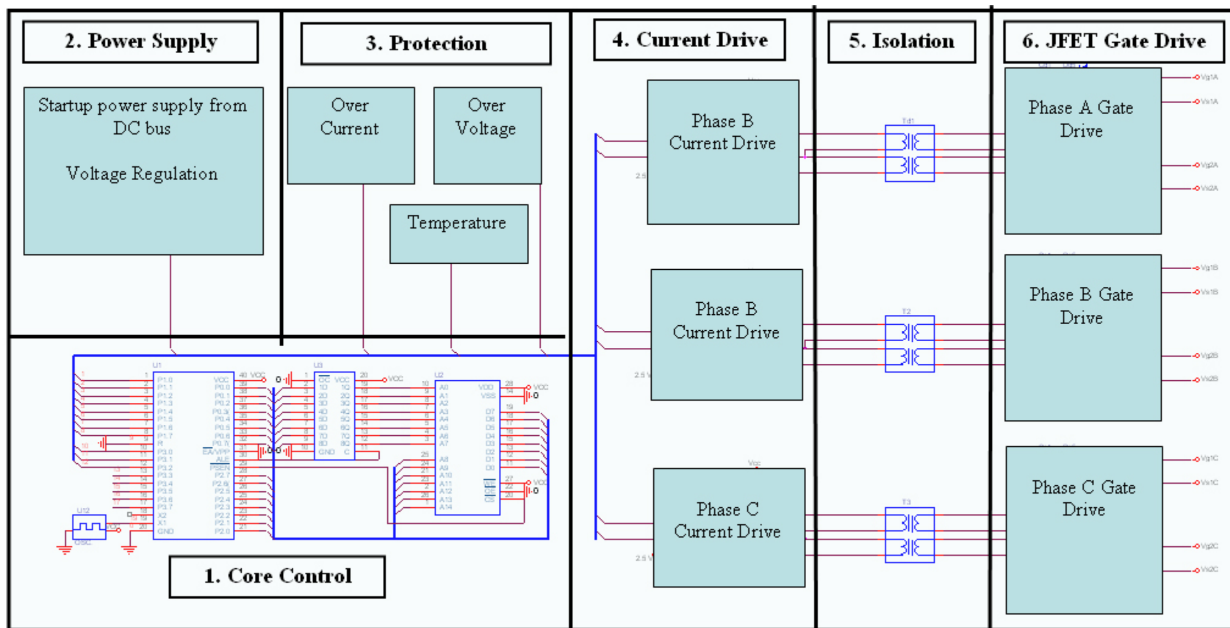

Figure 2: Schematic diagram of the three-phase MCPM.

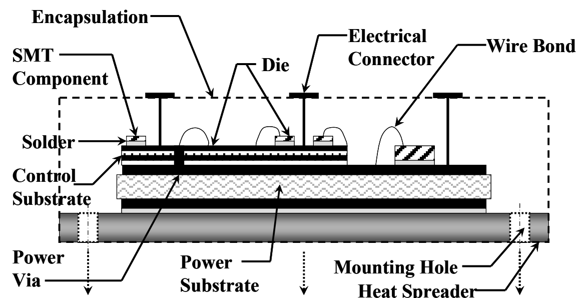

Figure 3: Cross-section of a possible MCPM design.

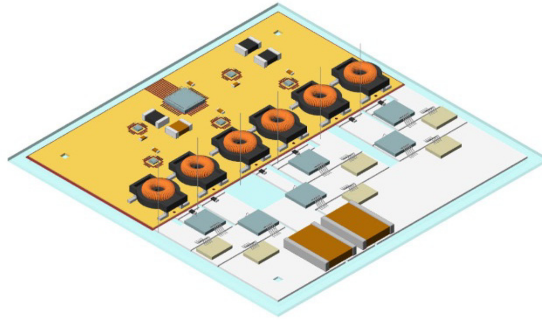

Figure 4: Isometric of High-Temperature MCPM.

The high power bare-die SiC devices are mounted with a 300 °C 92.5Pb-5In-2.5Ag solder directly to the AlN DBC substrate, where a good thermal path can be traced to the heatspreader. Because of the demanding power and thermal requirements, the power substrate metallization traces can not be tightly patterned for high density control electronics. Instead, the control board is fabricated from a high temperature multilayer polyimide substrate. The metallization traces on these layers are flash gold plated for improved reliability. The control components are bare-die devices (wirebonded with high reliability gold wire), surface mount passives, and magnetic components. The control board is mounted to the high power substrate by a high temperature adhesive laminate. The heatspreader of the MCPM is a metal-matrix-composite material (such as AlSiC), which is a ceramic matrix injected with a metal. These heatspreader materials offer excellent thermal conduction capabilities while simultaneously providing a close CTE match to the DBC ceramic substrate (thus reducing stresses and the chances of thermal cycle / thermal shock failures).

3.0 Thermal Modeling

To verify the MCPM design for high-temperature operation, Flotherm software was used to thermally model the MCPM with the SiC power JFETs and the SOI control devices. Figure 5 shows the model containing the DBC and polyimide boards, the SiC and SOI devices, and the

heatsink and heat spreader. Figure 6 shows the SiC JFETS operating at a junction temperature of 307 °C and the SOI devices at a junction temperature of 240 °C. This simulation was designed to illustrate the limits of the power density. The die attach used for the SiC JFETs can not exceed 310 °C and therefore the max power this MCPM can deliver while keeping the JFETs to approximately 300 °C is 3.6 kW.

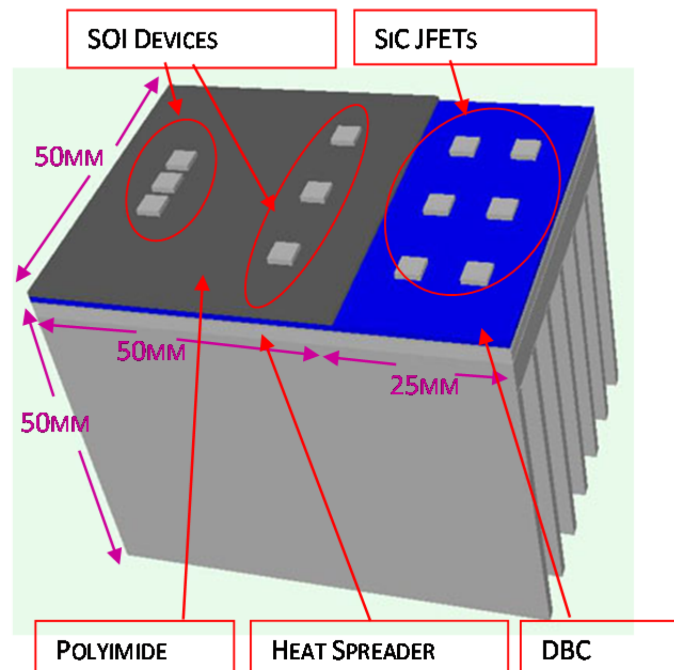

Figure 5. Flotherm model of the MCPM.

To clearly illustrate the advantages of this SiC/SOI MCPM, another simulation using the same heatsink and geometrical/mechanical design, but with Si control electronics and Si power switches, is shown in Figure 7. The junction temperature of the Si power switches is kept to approximately 150 °C (154 °C in the simulation) which is the max junction temperature of Si power devices. With the Si power devices operating at their max temperature the maximum power delivered by the converter is approximately 1.3 kW. This clearly illustrates a power

density increase of approximately 3× through the use of high-temperature SiC and SOI technology.

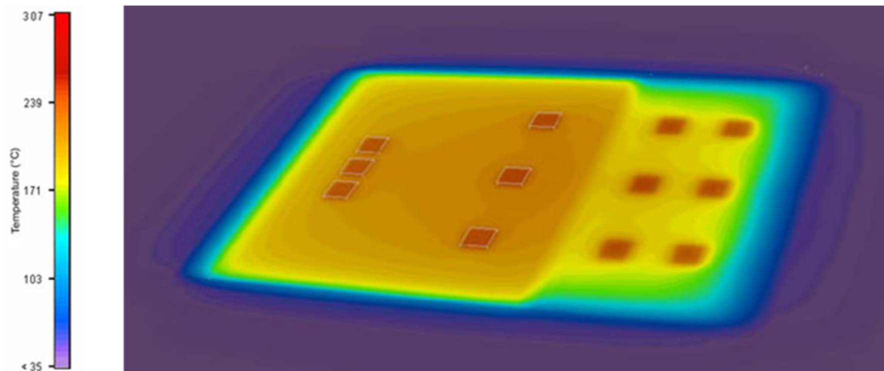

Figure 6: Flotherm simulation of 3-phase MCPM, SiC power device temperature 307 °C, SOI device temperature = 240 °C, power = 3.6 kW.

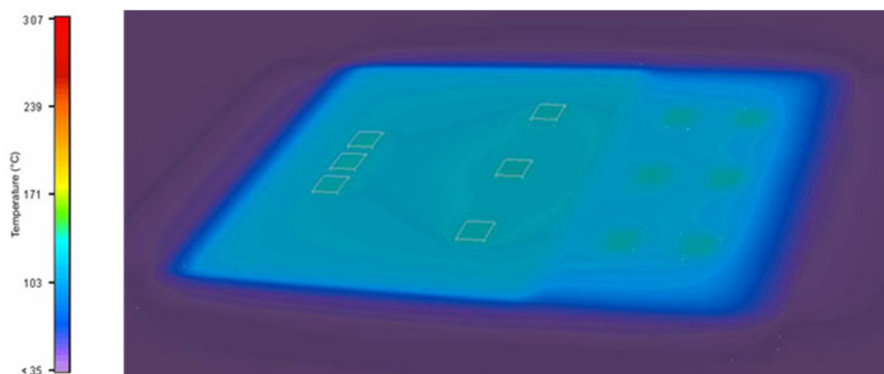

Figure 7: Flotherm simulation of 3-phase MCPM. Si power device temperature = 154 °C, Si IC device temperature = 132 °C, power = 1.3 kW.

4.0 Testing Results

4.1 High-Temperature Capacitor Test

Of all the passive devices required for a high-temperature application, none are as problematic as capacitors. Capacitance will often change significantly with increasing temperature (due to temperature dependent values of the dielectric constant), as will the equivalent series resistance, and dissipation factor. In addition, the volumetric efficiency of

capacitors fabricated with dielectric systems more compatible with high temperature operation is generally quite low.

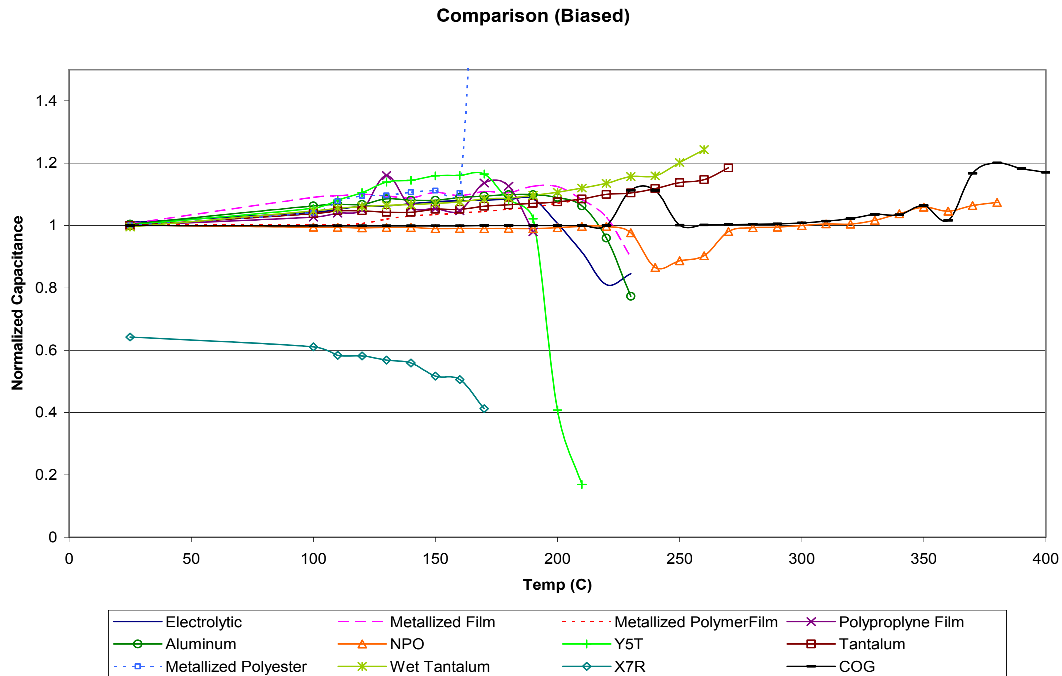

Figure 8: High-temperature capacitor test results.

Many power electronics applications require large filter and decoupling capacitor capabilities. Fast response and large energy reserves are expected in order to provide a stable, low ripple output. Improvements in current dielectrics and identification of new materials capable of operating reliably at high temperatures play a crucial role in the requirements realized for a highly miniaturized motor drive.

Twelve candidate materials were evaluated for high temperature operations. The test consisted of applying a DC voltage bias across each component equal to half its rated value (up to a 25V maximum). The components were each tested at room temperature, and then subjected to a 100 ºC environment. The temperature was raised with increments of 10 ºC with a dwell time

of ten minutes. The test results are presented in Figure 8. The chart plots the normalized capacitance (normalized to 0 voltage bias at room temperature) vs. temperature for each material. The best performing capacitor material was NPO/COG, which functioned with relative stability up to approximately 400 °C. The major disadvantage of this material is its relatively low energy density capabilities. Tantalum capacitor materials showed relatively good stability beyond 250 °C, and will be excellent choices for low voltage power electronics circuits due to their high energy densities (100μF+).

4.2 Single Phase MCPM

In order to demonstrate proof of concept and feasibility, a high-temperature MCPM prototype shown in Figure 9 was built and tested. The prototype was a half-bridge topology with the integrated SOI control electronics. Four SiC power JFETs were placed in parallel on the high and low sides of the half-bridge, respectively, while two SiC Schottky's are placed in parallel on each side to act as free-wheeling diodes. These power devices are mounted to an AlN DBC substrate that is mounted to a low CTE AlSiC heatspreader. The control circuitry including the SOI devices and passive components are mounted to a multilayer polyimide PCB that is attached to the DBC substrate.

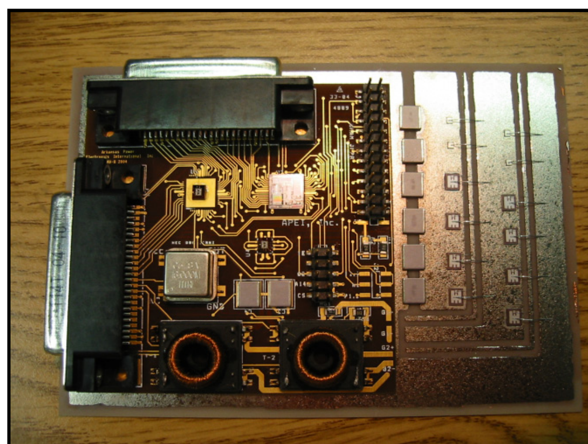

Figure 9: Single phase MCPM SOI/SiC prototype.

Figure 10 illustrates an oscilloscope capture of the prototype operating under 250 °C environmental conditions. Ch2 (blue) is the input to the high-side isolation transformer, Ch3 (magenta) is the high side power switch gate to source voltage, and Ch4 (green) is the low-side power switch gate to source voltage. The JFET is a normally on device (usually on at Vgs = 0 V) and requires a negative voltage to turn it off. The gate drive circuitry in the MCPM switches between approximately -13 V to +7 V. Figures 11 & 12 are oscilloscope captures illustrating dead-time of 80ns and 108 ns between both the turn on and turn off of the half-bridge switches.

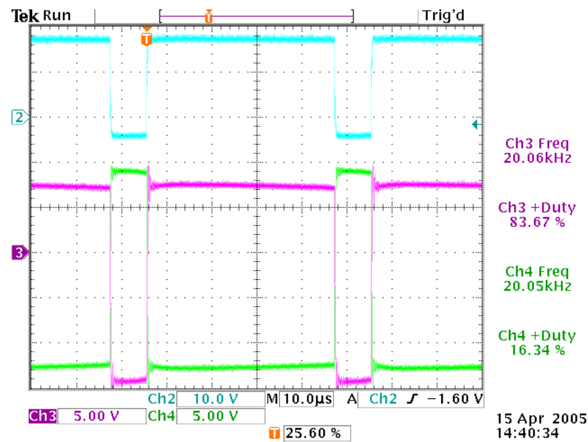

Figure 10: Vgs of JFET drive half-bridge signals.

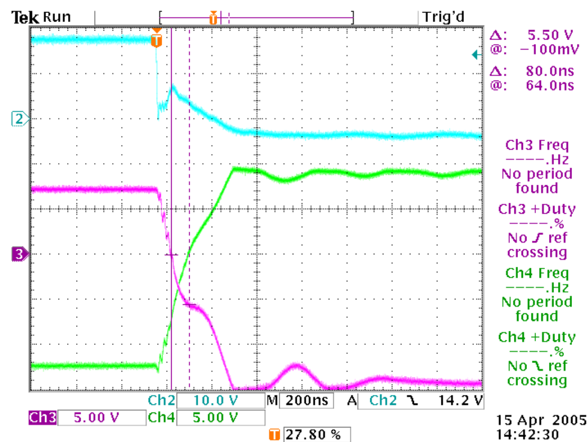

Figure 11: Deadtime = 80 ns.

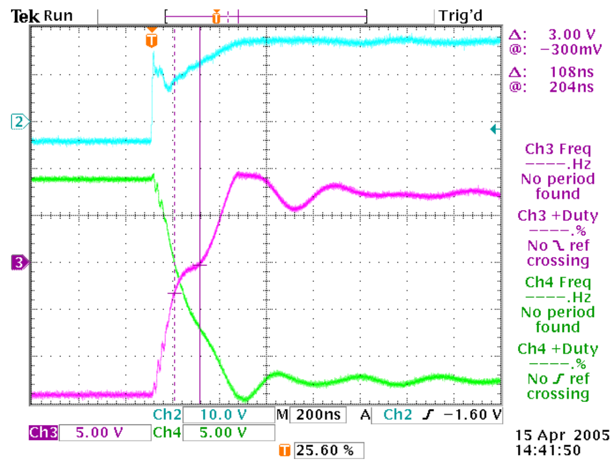

Figure 12: Deadtime = 108 ns.

4.2 Three-Phase MCPM

The full three-phase MCPM motor drive with integrated SOI control electronics and SiC JFETs is shown in Figure 13. The MCPM is capable of driving a three-phase induction machine up to 3 kW at temperatures in excess of 250 °C. The control electronics are mounted to a high T_g polyimide PWB that is attached to the DBC power substrate.

The high-temperature MCPM motor drive is currently being tested, and complete results, including switching waveforms, will be given in the presentation at the conference.

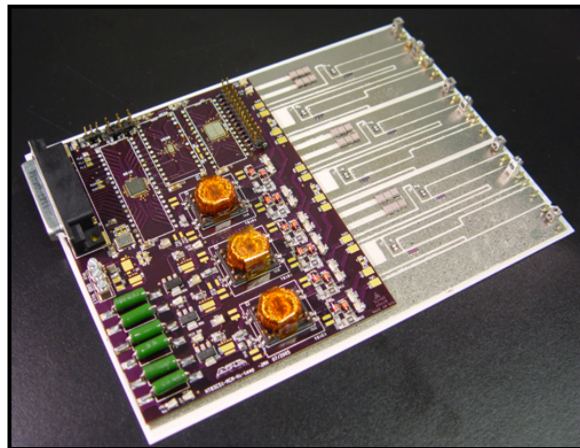

Figure 13: Completed MCPM 3-phase motor drive.

Acknowledgment

The work presented in this paper was funded in part by the U.S. Army Research Laboratories and the U.S. National Science Foundation.

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CHAPTER 8

A HIGH-TEMPERATURE MULTICHIP POWER MODULE (MCPM) INVERTER UTILIZING SILICON CARBIDE (SiC) AND SILICON ON INSULATOR (SOI) ELECTRONICS

Jared M. Hornberger, Edgar Cilio, Roberto M. Schupbach

Alexander B. Lostetter and H. Alan Mantooth

© 2006 IEEE. Reprinted, with permission, from Hornberger et al, A High-Temperature Multichip Power Module (MCPM) Inverter utilizing Silicon Carbide (SiC) and Silicon on Insulator (SOI) Electronics, IEEE Power Electronics Specialists Conference, June 2006.

Abstract

The researchers at Arkansas Power Electronics International, Inc. have designed, developed, packaged, and manufactured the first complete multichip power module (MCPM) integrating SiC power transistors with silicon on insulator (SOI) control electronics. The MCPM is a 4 kW three-phase inverter that operates at temperatures in excess of 250 °C. Bare die HTMOS SOI control components have been integrated with bare die SiC power JFETs into a single compact module. The high-temperature operation of SiC switches allows for increased power density over silicon electronics by an order of magnitude, leading to highly miniaturized power converters. In this paper, the researchers will discuss the challenges associated with high-temperature operation of power electronics; present the electrical, mechanical, and thermal design of a high-temperature MCPM; discuss the multitude of packaging issues that were solved to reach high-temperature operation; illustrate the high power density and miniaturization achieved by the SiC MCPM; and present the experimental test results of the fully operational 4 kW SiC MCPM.

I. INTRODUCTION

The past decade has seen an intense and steady increase into the research of the viability of silicon carbide (SiC) device technology. This technology has the potential to solve many of

the current limitations associated with silicon (Si) electronics; in particular, limitations with respect to switching speeds, junction temperatures, and power density. The utilization of high-power SiC devices is set to revolutionize the power electronics industry and bring the benefit of improved efficiency and improved reliability to the commercial markets while simultaneously benefiting society through improving energy savings on a global scale.

A. Silicon Carbide versus Silicon

SiC is a wide bandgap semiconductor material capable of high temperature operation, theoretically up to ~600 °C. When compared to Si devices, SiC devices can be utilized at much higher temperatures (~ 5 times higher), possess a higher breakdown voltage (~10 times higher), possess lower switching losses, and are capable of higher current densities (~ 3-4 times higher).

B. High-Temperature, High-Power Density Power Electronics

A powerful argument for using SiC power electronics is the size and weight reductions that can be achieved. To clearly illustrate these advantages, the researchers developed and analyzed Si and SiC half-bridge models in Flotherm thermal analysis software [1]. The simulations showed that a Si module with a 3 kg heatsink can achieve a maximum power of 5 kW assuming a junction temperature of 150 °C while a SiC module with a 0.3 kg heatsink can achieve a maximum power of 7.5 kW assuming a junction temperature of 600 °C. This implies that the use of a SiC module allows for a 50 % increase in power and a 90 % decrease in weight and volume.

To take full advantage of the high power density capabilities offered by SiC electronics, the development of high-temperature electronics as well as high-temperature packaging technologies and design methodologies are required. In particular, the integration of high temperature power devices and high temperature control electronics into a single module greatly

minimizes parasitics, allowing very high frequencies of operation. The researchers are pursuing these areas of development. Specifically, the authors have developed high-temperature multichip power modules (MCPMs) utilizing SiC power JFET devices integrated with silicon-on-insulator (SOI) control electronics.

II. Multichip Power Modules

SiC devices are capable of operating into the GHz frequency range; a great reduction in the size of passive components such as capacitors, inductors, and other magnetic components is expected. Integrating control and power layers into a single module significantly reduces size, weight, and parasitic effects. This approach is known as a multichip power module where multiple layers are utilized to separate the power and control circuitry [2-7].

A. MCPM Electrical Design

The electrical design of the MCPM stems from a demonstration three-phase motor control developed for high temperature operation. The high-temperature motor controller operated in an environment of 250 °C and is detailed in [8]. Figure 1 illustrates the circuit block diagram of the current MCPM design.

The core control block (block 1) contains an SOI microcontroller, latch, SRAM, and in-house developed software to generate the control signals required for a three-phase motor drive. The MCPM design contains start-up circuitry to deliver power from the DC bus to the low voltage control logic (block 2). Another feature of the MCPM design is the feedback of critical conditions such as over voltage, current, and temperature (block 3). Block 4 takes the low voltage digital signals from the microcontroller and amplifies the voltage and current to drive the isolation transformers in block 5. Block 6 can be customized to drive different types of power switches. In this case the design drives the gate of a JFET from -40 V (fully off) to 0 V (fully

on). The JFET gate drive circuitry also ensures that there is adequate dead-time between the high and low side switches.

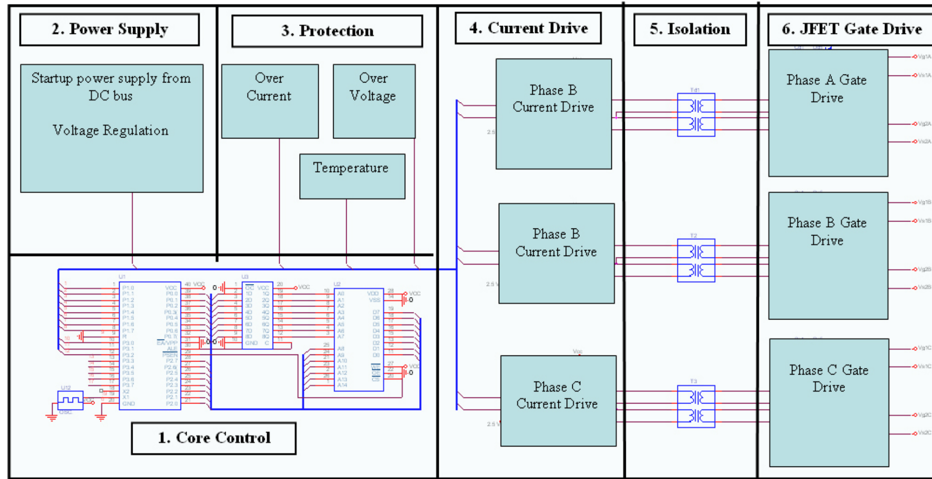

Fig. 1: Schematic diagram of the three-phase MCPM.

B. MCPM Mechanical Design

The MCPM has two main stages, the mechanical design and power electronic packaging aspect of the MCPM focuses on combining 1) a high-power, high-temperature dual layer ceramic substrate and 2) a high-density, high-temperature multi-layer PCB. The cross-section of this design methodology is illustrated in Figure 2, while Figure 3 illustrates an isometric view.

The first stage consists of high thermal conductivity direct-bond-copper (DBC) power substrate, where Ni plated copper plates are directly bonded to either side of an AlN ceramic substrate. The metallization traces on this power substrate are designed specifically for the capability to transmit large amounts of current at high voltages.

The high-power bare-die SiC devices are mounted with a high-temperature solder directly to the AlN DBC substrate allowing an excellent thermal path to the heatspreader. The SiC power devices are wirebonded with large diameter Al bonding wire to carry the power from the top-side contacts to the Ni plated DBC traces.

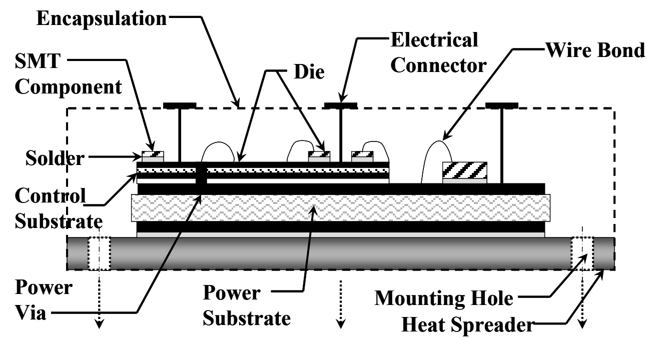

Fig. 2: Cross-section of the MCPM design.

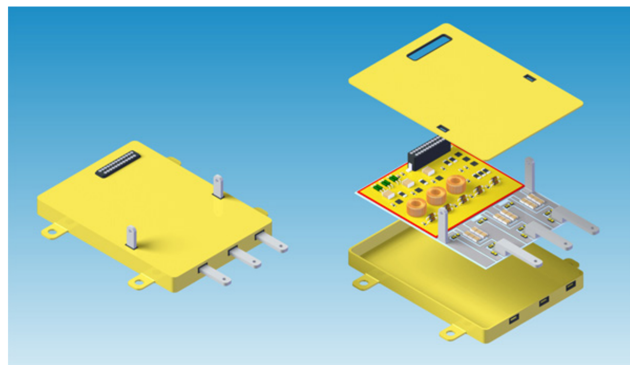

Fig. 3: Conceptualized High-Temperature MCPM.

Because of the demanding power and thermal requirements, the power substrate metallization traces cannot be tightly patterned for high density control electronics. Instead, the control board is fabricated from a high temperature multilayer polyimide substrate. The metallization traces on these layers are selective Au/Ni plated for improved reliability.

The control components are high-temperature SOI bare-die devices (wirebonded with 1 mil wire), surface mount passives, and magnetic components. The control board is mounted to the high power substrate by a high temperature adhesive laminate.

Finally, the module is attached to a heatspreader with engineered low coefficient of thermal expansion (CTE). The heatspreader of the MCPM is a metal-matrix-composite material; in this case AlSiC is used. The heatspreader offers excellent thermal conduction capabilities while simultaneously providing a close CTE match to the DBC ceramic substrate, thus reducing stresses and the chances of thermal fatigue or shock failures.

A low-power high-temperature three-phase prototype module shown in Figure 4 was fabricated and tested.

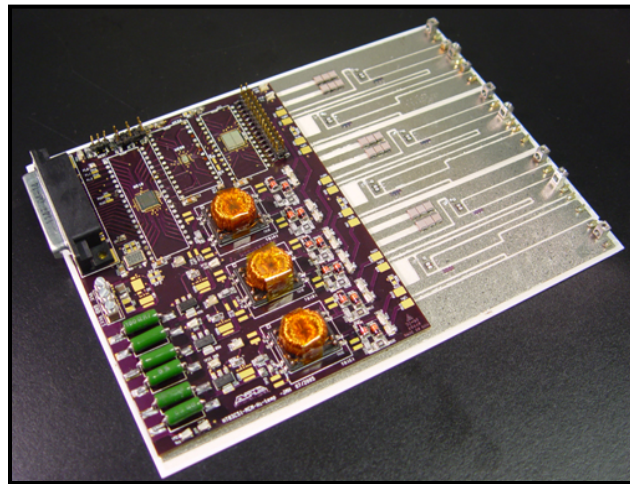

Fig. 4: Completed MCPM three-phase motor drive.

III. Thermal Model

To verify the MCPM design for high-temperature operation, a thermal model was generated in FLOTHERM for detailed 3D thermal analysis. The goal of the thermal simulations was to closely estimate and simulate the actual conditions experienced in the test setup of the MCPM. One-dimensional calculations were used to determine the proper heatsink required for a temperature rise at the power switches of 100 °C in a 150 °C ambient, resulting in a maximum junction operating temperature of 250 °C. Neglecting the die attach layer, the thermal resistance

per SiC device was calculated as in Eq. 1 where t is the thickness of the material (m), k is the thermal conductivity (in Watts/m·K) and A is the cross-sectional area (m^2).

$$R_{\theta Total} = \left(\frac{t_{Copper1}}{k_{Copper1} \cdot A}\right) + \left(\frac{t_{AlN}}{k_{AlN} \cdot A}\right) + \left(\frac{t_{Copper2}}{k_{Copper2} \cdot A}\right) + \left(\frac{t_{Baseplate}}{k_{Baseplate} \cdot A}\right) + R_{\theta SA} \qquad \text{Eq. 1}$$

The total thermal resistance represents the path through the top copper layer, the AlN ceramic, the bottom copper layer, and the AlSiC heatspreader. The cross-sectional area used in the thermal resistance calculation can be assumed to start at the base of the SiC power die generating the heat (due to electrical losses). The thermal contact area increases as the path moves through the varying layers. The angle of this spreading is a function of the thermal conductivities of the two materials in contact, and is determined quantitatively by Eq. 2, and the change in thermal contact area is governed by Eq. 3, where α is the angle of thermal spreading and L is the length of the thermal interface [9]. This increase in contact area results in an effective decrease in the thermal resistance of the material.

$$\alpha_a = \tan^{-1}\left(\frac{k_a}{k_b}\right) \qquad \text{Eq. 2}$$

$$L_2 = 2 \cdot t_a \cdot \tan(\alpha_a) + L_1 \qquad \text{Eq. 3}$$

Layer thicknesses, calculated thermal contact areas, and their thermal resistance are presented in Table I.

The theoretical worst-case efficiency is assumed to be 83% at 250 °C, where the increased on-resistance of the power devices results in an increase in losses. The assumed thermal loss of the entire module at full power (i.e., 4kW) is estimated to be approximately 650 W (27 W per SiC JFET). This loss is evenly distributed among the twenty four different SiC

JFETs used in the power stage. The devices are far enough apart from each other that they will not interfere with the thermal spreading of the neighboring die. A total junction to sink thermal resistance can be determined by adding the twenty four thermal resistances in parallel, resulting in an $R_{\theta JS}$ value of 0.017 °C/W. The maximum thermal resistance allowable for the heatsink for a 100 °C rise is calculated to be 0.183 °C/W.

Table I. Thermal resistances of each layer.

			Thermal	
Material	Thickness (m)	Area (m^2)	Conductivity (W/mK)	Resistance (°C/W)
Copper 1	3.048×10^{-4}	1.54×10^{-5}	385	0.051
Aluminum Nitride	6.35×10^{-4}	2.01×10^{-5}	170	0.186
Copper2	3.048×10^{-4}	3.19×10^{-5}	385	0.025
AlSiC Baseplate	5.08×10^{-3}	1.66×10^{-4}	200	0.153
TOTAL				0.415

High fin density profiles were examined, and the most effective profile (i.e., lowest thermal resistance vs. weight) was selected. To minimize the heatsink length to the dimensions of the module (5.4 inches), a forced convection airflow of 2.4 m/s was necessary. A three-dimensional conceptual model, displayed in Figure 5, was also developed for the three-phase SiC-based MCPM.

In order to verify the one-dimensional calculations, the air speed required to obtain a 100 °C junction temperature rise was determined through a number of simulations. Thermal results of this simulation are displayed in Figures 6 (the plane going across the heatsink), 7 (the plane at the base of the bare die power devices), and 8 (the plane passing through the heatsink).

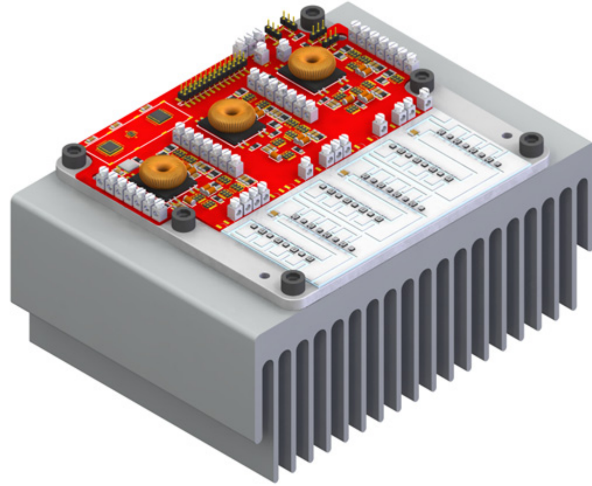

Fig. 5: Conceptual design of the module.

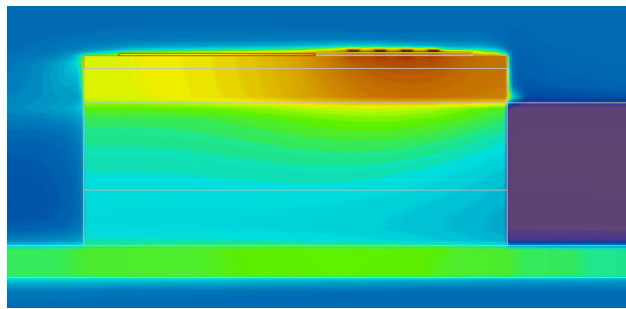

Fig. 6: *Z*-Axis temperature plot.

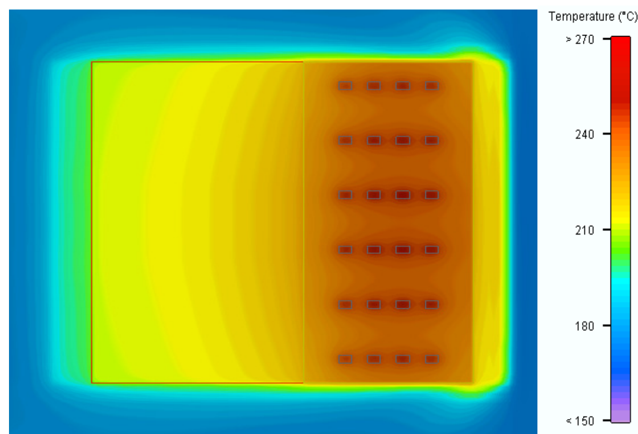

Fig. 7: *Y*-Axis temperature plot.

The results in Figure 6-8 display excellent thermal spreading, and an effective removal of generated heat through the heatsink. Figure 7 shows that a maximum die junction temperature of 258 °C occurs under maximum power and with an airflow of 50 CFM implying a 108 °C rise in junction temperature over the ambient of 150 °C.

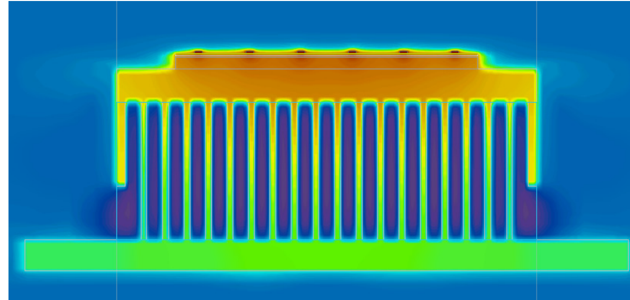

Fig. 8: *X*-Axis temperature plot.

IV. Test Results

In order to demonstrate proof of concept and feasibility at high-temperature, a low-power three-phase MCPM prototype inverter was fabricated and tested. After successful testing of the low power prototype, a 4 kW prototype module was built but with only two of the phases populated for single-phase full-bridge operation, Figure 9 shows the fabricated 4 kW module. Four SiC power JFETs along with four SiC Schottky anti- parallel diodes are placed in parallel on the high and low sides of each switching pair. These power devices are mounted to an AlN DBC substrate that is mounted to a low CTE AlSiC heatspreader. The control circuitry including the SOI devices and passive components are mounted to a multilayer polyimide PCB.

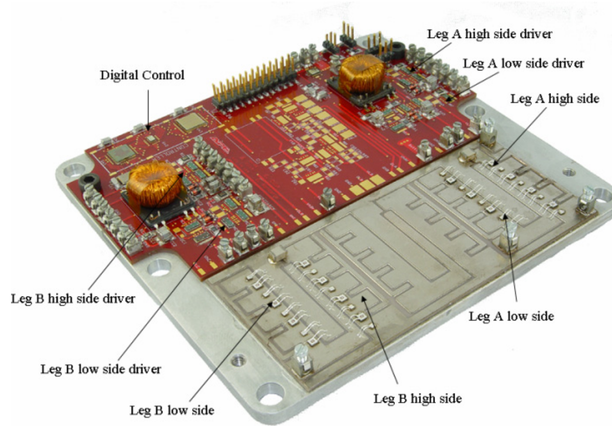

Fig. 9: Single-phase MCPM inverter module.

B. High-Temperature Testing

The high-temperature three-phase prototype module was tested for operation up to 250 °C ambient. The module was connected to a three-phase resistive load and a DC-bus of about 50 VDC.

Figure 10 shows waveforms from the module operating at room temperature and low power. Channel 1 represents the phase A PWM signal from the SOI microcontroller, Channel 2, Channel3, and Channel 4 are filtered (R = 200 kΩ, C = 2.2 nF) microcontroller signals phase A, B, and C respectively. The PWMs are switching at approximately 20 kHz and the filtered sinusoids show three-phase 60 Hz operation at 120 degrees phase shift. The same waveforms at high-temperature (250 °C) are shown in Figure 11. These figures show that the PWM signals generated by the microcontroller are not noticeably affected over temperature.

Figure 12 shows phase B high and low side gates signals and the corresponding drain-source voltage (V_{DS}) across the SiC power switch. Channel 1 and Channel 3 are the high-side gate and V_{DS} signals while Channel 2 and Channel 4 are the low-side gate and V_{DS} signals. Figure 13 shows the same signals operating at 250 °C. A close examination of Figures 12 and 13 shows no significant degradations of the gate or drain to source signals over temperature.

The high-temperature MCPM operated with a resistive load drawing minimal power. Figure 14 shows load currents of phase A (Channel 1), phase B (Channel 2), and phase C (Channel 3) at 250 °C. The scope capture of the phase currents show sinusoidal operation at about 60 Hz.

The line-line voltages of the load were measured and are shown in Figure 15. Channel 1 represents VAB, Channel 2 represents VAC, Channel 3 represents VBC and Channel 4 represents the DC-bus voltage.

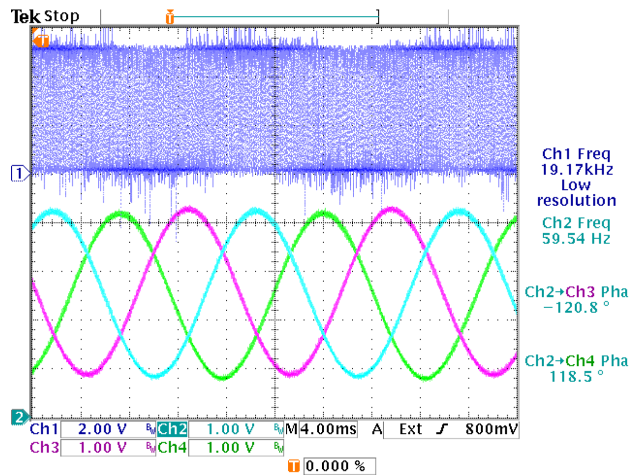

Fig.10: Microcontroller PWM signals at 25 °C.

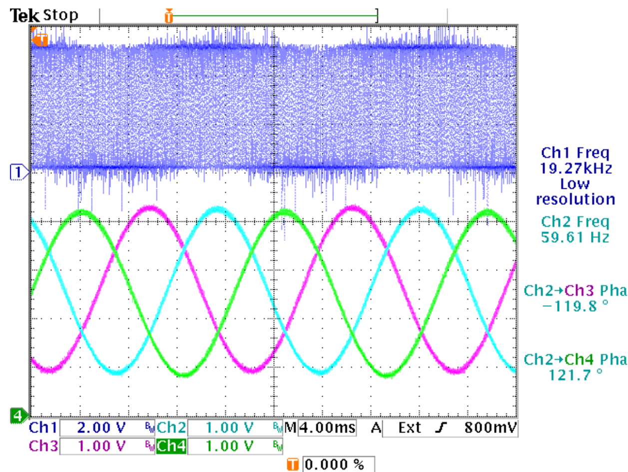

Fig. 11: Microcontroller PWM signals at 250 °C.

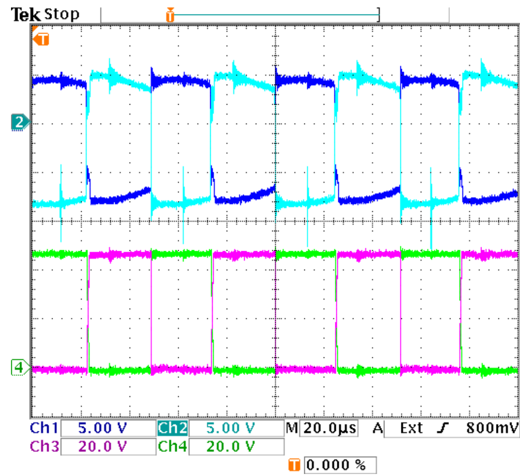

Fig. 12: Phase B signals at 25 °C.

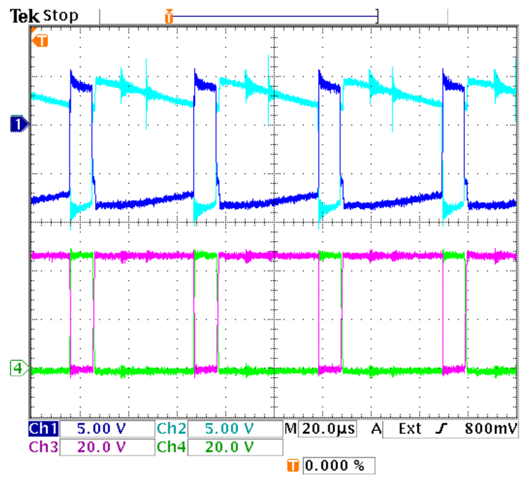

Fig. 13: Phase B signals at 250 °C.

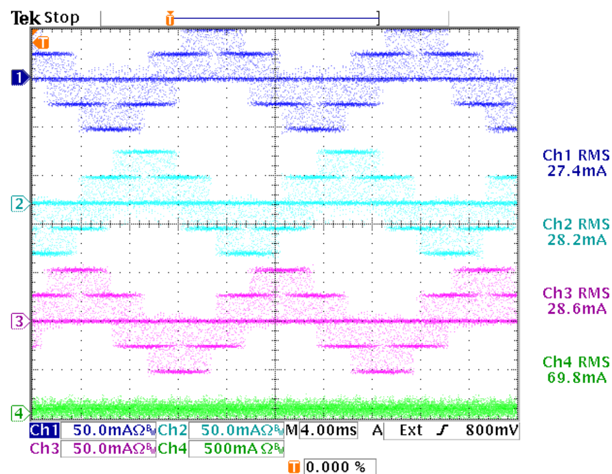

Fig. 14: Currents of phases A, B and C at 250 °C.

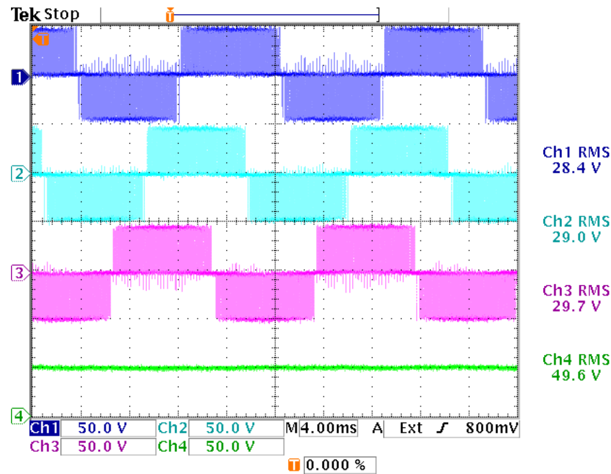

Fig. 15: Line-to-line voltages at 250 °C.

C. Full Power Testing

After successful testing of the low-power module, a high-temperature module was built to extend the power to 4 kW. To begin, the high-power module was configured as a single-phase H-bridge inverter. In this manner the inverter requires only two-thirds of the components minimizing cost.

The inverter was tested successfully for high-power (~ 3 kW) operation at room temperature with a resistive/inductive load. The inverter was also tested successfully at high-temperature (250 °C) at reduced power levels. The inverter operated with a load processing 2.7 kW at 195.2 Vrms at the load. The test load includes a T-filter consisting of L1, L2, and C1 as shown in Figure 16.

Figure 17 shows the voltage across Rload (Vload), the current through the load (Iload), and the power at the load (Pload). The input real power was calculated to be 3.158 kW. Figure 18 shows the input voltage (Vdc), the input current (Idc), and the input power (Pin). The instantaneous input and output power were calculated using the recorded instantaneous input and output voltages and currents.

The calculated input and output power are based on the fundamental frequency (60 Hz) components. In order to account for the real power losses in the filtering stage formed by L1, L2 and C1, the filter efficiency was characterized for various input voltages, and it has been determined to be 97 %. Based on preliminary calculations the efficiency of the power module, while operating at room temperature, is a minimum of 90 %. Since these efficiency calculations do not take into account the high-frequency harmonics dissipated in the output filter, it is estimated that the actual efficiency of the power stage is significantly higher; however, the exact efficiency requires the use of a calorimeter or high-frequency power measurement device (i.e., power analyzer). A set of detailed efficiency measurements will be carried out in the future.

V. Conclusion

This paper has presented the successful testing of both the three-phase high-temperature module and, the single phase high-power module, showing feasibility of SiC MCPM technology. The initial testing of these SiC MCPM inverter modules shows high potential for an increase in power density. When compared with state-of-the-art Si-based modules, a size reduction of up to 7 × may be achievable using APEI, Inc. high-temperature MCPM design approach.

This work will continue by building a three-phase 4 kW module and testing to high-temperature and full power for a high power dense inverter with greatly reduce size and weight when compared to conventional inverters. Additional work will include advanced power efficiency measurements. These efficiency measurements will allow more accurate estimation of thermal loss contributing to overall size minimization. Lastly, improvements on high-temperature power electronics packaging will be pursued with the objective of improving long term module reliability.

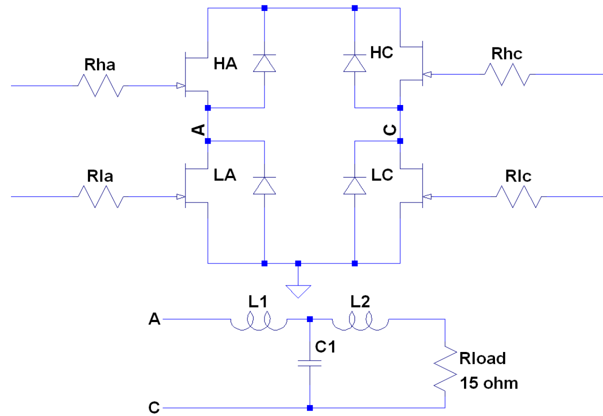

Fig. 16: Power stage, filtering stage, and test load.

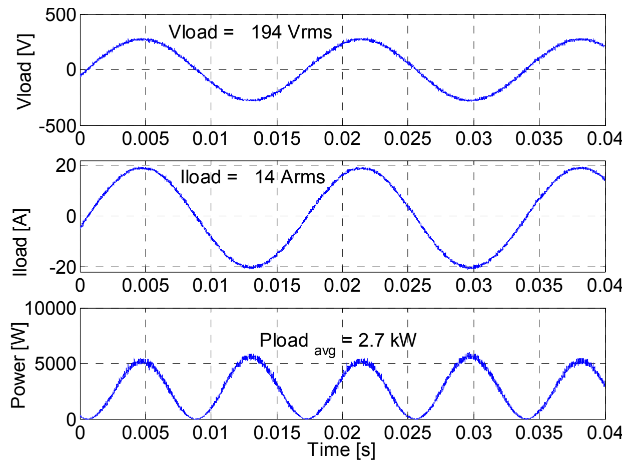

Fig. 17: Voltage across load resistor (Vload), current through the load (Iload), and power dissipated by the resistive load (Pload).

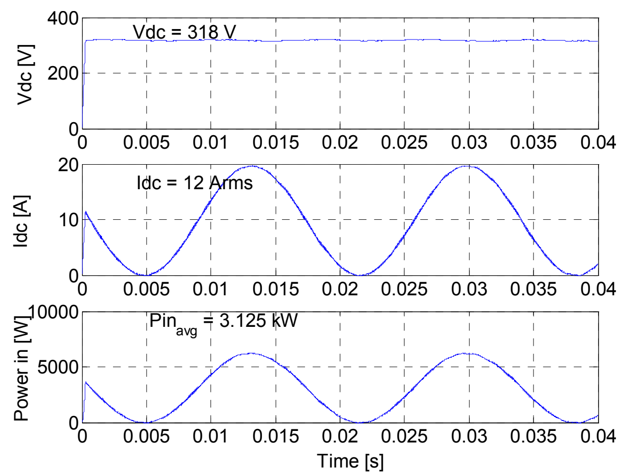

Fig. 18: Input voltage (Vdc), input current (Idc), and input power (Pin).

Acknowledgment

The work presented in this paper was funded in part by the U.S. Army Research Laboratories, the U.S. National Science Foundation, and the U.S. Department of Energy's energy storage division.

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CHAPTER 9

A HIGH-TEMPERATURE SILICON CARBIDE (SIC) MULITCHIP POWER MODULE (MCPM) INVERTER FOR DOWN-HOLE APPLICATIONS

J. Hornberger, E. Cilio, B. McPherson, R. Schupbach, A.Lostetter, and H. Alan Mantooth

© 2006 IMAPS. Reprinted, with permission, from Hornberger et al, A High-Temperature Silicon Carbide (SiC) Mulitchip Power Module (MCPM) Inverter for Down-Hole Applications, International Conference on High Temperature Electronics, May 2006.

Abstract

The power electronics industry is constantly seeking to reduce the size and increase efficiency of power electronic systems. As a result, silicon carbide (SiC) power semiconductor devices have seen a steady increase in research due to the advantages they posses over silicon devices and is on the way to revolutionize the power electronics industry.

The researchers at Arkansas Power Electronics International, Inc. have performed extensive research in the area of SiC device applications and extreme environment packaging and have developed a three-phase 4 kW multi-chip power module (MCPM) inverter capable of high-temperature operation. This paper will overview SiC and Silicon-on-Insulator (SOI) devices; overview the application of this technology to a down-hole orbital vibrator (DHOV); discuss the challenges associated with high-temperature operation of power electronics; present the electrical, mechanical, and thermal designs of a high-temperature MCPM; discuss the multitude of packaging issues that were solved to achieve high-temperature operation; illustrate the high power density and miniaturization achieved by the SiC MCPM; and present the experimental test results of the fully operational SiC MCPM.

Key words:

Silicon carbide (SiC), Silicon on Insulator (SOI), High-temperature electronics, High-temperature packaging, and Multichip power modules (MCPMs)

Introduction

The requirements of modern high-performance power electronic systems are quickly growing beyond the limitations set by the intrinsic properties of silicon (Si) devices that are conventionally employed in this area. There is constant push to reduce size and weight, increase power with higher voltages and currents, increase switching speeds to decrease size and need of passive components, and greatly improve power electronic systems. Silicon carbide exceeds the capabilities and limitations of Si power devices with higher blocking voltages, increased switching frequency, lower switching losses, and much higher operating temperatures. These advantages translate to lighter, more efficient, and higher power dense power electronic systems.

The desire to use SiC power electronics to miniaturize power converters also leads to the necessity of high-temperature control, gate drive circuits, and passive components. The ultimate desire would be to use SiC control/digital ICs with SiC power switches and/or integrate SiC control with the SiC power switches. Since SiC control is not expected in the near future, SOI control electronics is the next best option for higher temperature operation.

1.1 Silicon Carbide

SiC is a wide bandgap semiconductor material capable of high temperature operation, theoretically up to ~600 °C. When compared to silicon based devices, SiC can be utilized at much higher temperatures (approximately 5 times higher than Si), possess a higher breakdown voltage (10 times that of Si), possess lower switching losses, and are capable of higher current densities (approximately 3-4 times higher than Si). The potential applications of SiC are widespread and all encompassing in the area of power electronics. Some applications include military and space exploration vehicles, more electric aircraft, electric and hybrid-electric vehicles, nuclear power reactors, and petroleum and geological exploration instrumentation.

Ultimately, any system that would see improvement from high-density, high-temperature or high-efficiency power electronics would benefit from SiC.

1.2 Silicon on Insulator

Typical bulk Si integrated circuits (ICs) and power devices are designed to operate at temperatures not exceeding 75 °C while military grade ICs and devices typically operate up to 125 °C. Beyond these temperatures, the device will cease to function according to specification or completely fail. Effects such as current leakage and decreased threshold voltages occur at elevated temperatures, resulting in MOSFETs that fail to turn off or experience thermal runaway. To reduce these effects associated with high-temperatures in Si devices, an insulating oxide layer can be utilized to create Silicon-on-Insulator.

A basic SOI building block consists of three layers; a silicon substrate, a buried oxide such as silicon dioxide as an insulator, and a thin layer of silicon on the surface where the transistors are formed. SOI completely isolates the transistor from its neighboring transistors and other circuit components with a layer of insulator material. This reduces the junction capacitance, which in turn reduces the amount of current required to switch a device [1]. In general, SOI devices are 25%-30% faster, have lower supply voltages, are more densely packed, are more immune to latch-up, and have leakage currents that are reduced by 100-1000 times at high-temperatures over bulk Si devices [2]. Additionally, some SOI devices have been characterized up to 500 °C [3].

2.0 High-Temperature Power Electronic Applications

Researchers at APEI, Inc. and the University of Arkansas have performed extensive research in the area of SiC device applications, packaging, and modeling for power electronic

systems [4-6]. One of the high-temperature applications the researchers are currently working on is a three-phase inverter for use in geological exploration.

Energy companies are interested in SiC power electronics for deep earth petroleum exploration where hostile environments with high ambient temperatures are encountered. The down hole orbital vibrator (DHOV) from Cole Engineering is a 3-phase 4 hp motor driven instrument that searches for oil reservoirs through acoustic sensing. The DHOV motor operates off-axis to emit acoustic waves at depths up to 3 miles beneath the earth's surface and at temperatures up to 250 °C. Sensors placed on the surface (See Figure 1) pick up the waves and map the underground makeup, layers, dimensions, etc. Due to the high temperatures deep beneath the surface, the motor drive electronics are currently kept on the surface. Problems associated with the electronics on the surface include noise and control lag-time for motor control operations, frequency of operation is limited, and overall power capability is limited. With the use of SiC motor drives, the electronics would be positioned directly within the DHOV housing as shown in Figure 2. Integration of the power electronics into the instruments would increase frequency of operation (allowing for more accurate mapping), would increase control capability, and would increase power (allowing for wider area mapping).

It is difficult to place Si electronics down hole because of the extreme environment found within the oil wells. With SiC and SOI electronics, it is possible to send the electronics down hole with the motor, thus greatly improving motor drive control and efficiency.

2.1 MCPM Electrical Design

The electrical design of the MCPM stems from a demonstration three-phase motor control developed by APEI, Inc. for high temperature operation for use in the Army Future Combat Systems (FCS) program. The high-temperature motor controller shown in Figure 3

operated in an ambient environment of 250 °C and is detailed in [7]. Figure 4 illustrates the circuit block diagram of the current MCPM design.

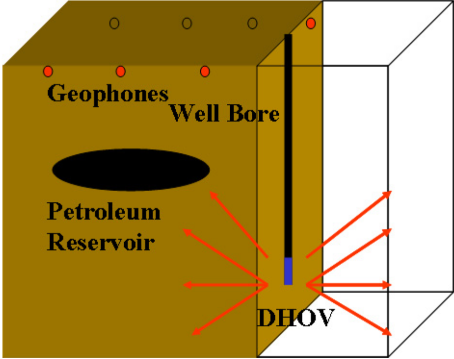

Figure 1. DHOV geological mapping diagram.

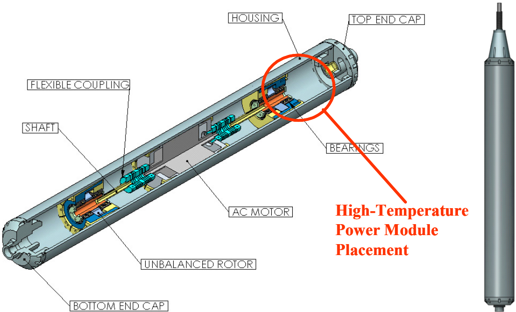

Figure 2. DHOV system showing integration of power electronics.

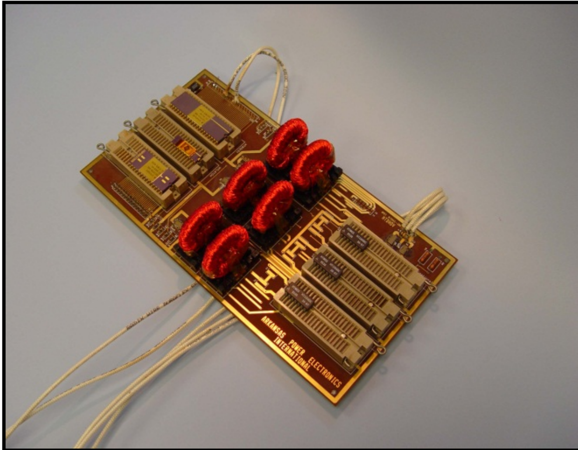

Figure 3. Original high-temperature three-phase motor controller.

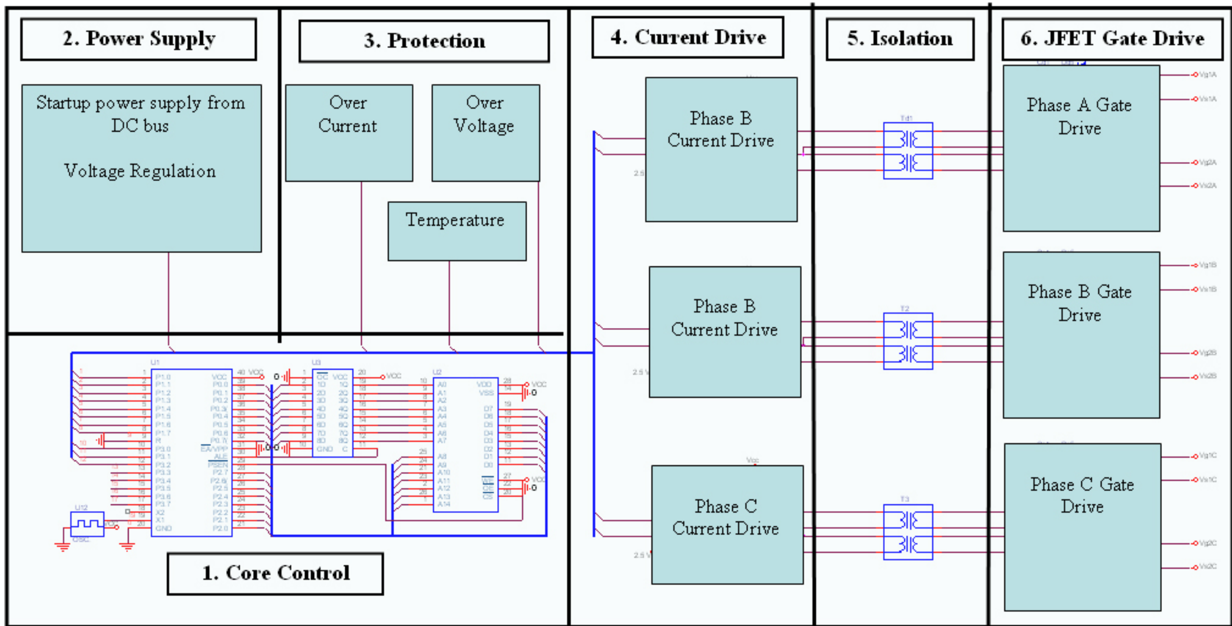

Figure 4: Schematic diagram of the three-phase MCPM.

The core control block (block 1) contains an SOI microcontroller, latch, SRAM, and in-house developed software to generate the control signals required for a three-phase motor drive. The MCPM design contains start up circuitry to deliver power from the DC bus to the low voltage control logic (block 2). Another feature of the MCPM design is the feedback of critical conditions such as over voltage, current, and temperature (block 3). Block 4 takes the low voltage digital signals from the microcontroller and amplifies the voltage and current to drive the isolation transformers in block 5. Block 6 can be customized to drive different types of power switches. In this case the design drives the gate of a SiCED JFET from -40 V (fully off) to 0 V (fully on). The JFET gate drive circuitry also ensures that there is adequate dead-time between the high and low side switches.

2.2 MCPM Mechanical Design

SiC devices are capable of operating into the GHz frequency range; a great reduction in the size of passive components such as capacitors, inductors, and other magnetic components is expected. Integrating control and power layers into a single module significantly reduces size, weight, and parasitic effects. This approach is known as a multichip power module where multiple layers are utilized to separate the power and control circuitry [8-11]. Figure 5 illustrates a cross-section of the MCPM package design while Figure 6 illustrates an isometric view of the conceptualized design. The MCPM is built in two major stages. The first stage consists of the direct- bond-copper (DBC) power substrate, where Ni plated copper plates are directly bonded to either side of an AlN ceramic substrate. The metallization traces on this power substrate are designed specifically for the capability to transmit large amounts of current at high voltages.

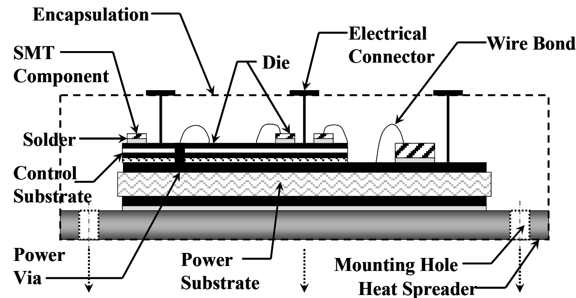

Figure 5: Cross-section of the MCPM design.

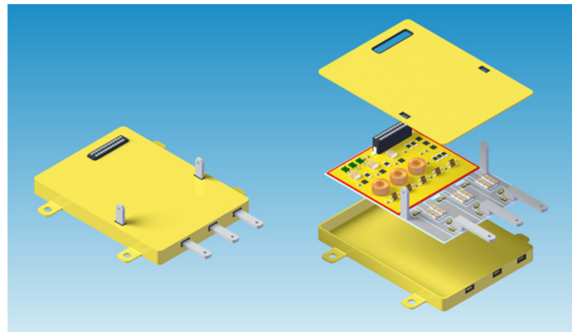

Figure 6: Conceptualized High-Temperature MCPM.

The high power bare-die SiC devices are mounted with a 310 °C 92.5Pb-5In-2.5Ag solder directly to the AlN DBC substrate, where a good thermal path can be traced to the heatspreader. Because of the demanding power and thermal requirements, the power substrate metallization traces can not be tightly patterned for high density control electronics. Instead, the control board is fabricated from a high temperature multilayer polyimide substrate. The metallization traces on these layers are flash gold plated for improved reliability. The control components are bare-die devices (wirebonded with high reliability gold wire), surface mount passives, and magnetic components. The control board is mounted to the high power substrate by a high temperature adhesive laminate. The heatspreader of the MCPM is a metal-matrix-composite material which is a ceramic matrix injected with a metal, in this case AlSiC is used. The heatspreader offers excellent thermal conduction capabilities while simultaneously providing a close CTE match to the DBC ceramic substrate (thus reducing stresses and the chances of thermal cycle / thermal shock failures).

3.0 Thermal Modeling

To verify the design for high-temperature operation, a thermal model was generated in FLOTHERM for detailed 3D thermal analysis. The goal of the thermal simulations was to closely estimate and simulate the actual conditions experienced in the test set-up of the MCPM. One-dimensional calculations were used to determine the proper heatsink required for a temperature rise at the power switches of 100 °C in a 150 °C ambient environment, resulting in a max operating temperature of 250 °C. Neglecting the die attach layer, the thermal resistance per SiC device was calculated as in Eq. 1 where t is the thickness of the material (m), k is the thermal conductivity (in watts/m·K) and A is the cross-sectional area (m^2).

$$R_{\theta Total} = \left(\frac{t_{Copper1}}{k_{Copper1} \cdot A}\right) + \left(\frac{t_{AlN}}{k_{AlN} \cdot A}\right) + \left(\frac{t_{Copper2}}{k_{Copper2} \cdot A}\right) + \left(\frac{t_{Baseplate}}{k_{Baseplate} \cdot A}\right) + R_{\theta SA}$$ **Eq. 1**

The total thermal resistance represents the path through the top copper layer, the AlN ceramic, the bottom copper layer, and the AlSiC heatspreader. The cross-sectional area used in the thermal resistance calculation can be assumed to start at the base of the SiC power die generating the heat (due to electrical losses). The thermal contact area increases as the path moves through the varying layers. The angle of this spreading is a function of the thermal conductivities of the two materials in contact, and is determined quantitatively by Eq. 2, and the change in thermal contact area is governed by Eq. 3, where α is the angle of thermal spreading and L is the length of the thermal interface [12]. This increase in contact area results in an effective decrease in the thermal resistance of the material.

$$\alpha_a = \tan^{-1}\left(\frac{k_a}{k_b}\right)$$ **Eq. 2**

$$L_2 = 2 \cdot t_a \cdot \tan(\alpha_a) + L_1$$ **Eq. 3**

Layer thicknesses, calculated thermal contact areas, and their thermal resistance are presented in Table 1.

Table 1. Thermal resistances of each layer

Material	Thickness (m)	Area (m^2)	Thermal Conductivity (W/mK)	Thermal Resistance (°C/W)
Copper 1	3.048×10^{-4}	1.54×10^{-5}	385	0.051
Aluminum Nitride	6.35×10^{-4}	2.01×10^{-5}	170	0.186
Copper 2	3.048×10^{-4}	3.19×10^{-5}	385	0.025
AlSiC Baseplate	5.08×10^{-3}	1.66×10^{-4}	200	0.153
TOTAL				0.415

The theoretical worst case scenario for efficiency is assumed to be 83% at 250 °C, where the increased resistance of the power devices results in an increase in losses. The actual losses are much lower at room temperature. The assumed thermal loss of the entire module at full power (4kW) is estimated to be approximately 650 W (27 W per SiC JFET). This loss is assumed to be completely generated in the twenty four different SiC JFETS used in the power stage. Thus, the total junction to sink thermal resistance of all the JFETS is required. The devices are far enough away from each other that they will not interfere with the thermal spreading of the neighboring die, a total junction to sink thermal resistance can be found by adding the twenty four thermal resistances in parallel, resulting in an $R_{\theta JS}$ value of 0.017 °C/W. The maximum thermal resistance allowable for the heatsink for a 100 °C rise is calculated to be 0.183 °C/W.

High fin density profiles were examined, and the most effective profile (lowest thermal resistance vs. weight) is selected. To minimize the heatsink length to the dimensions of the module (5.4 inches), a forced convection airflow of 2.4 m/s was necessary. A three-dimensional conceptual model was then developed for the module, and is displayed below in Figure 7.

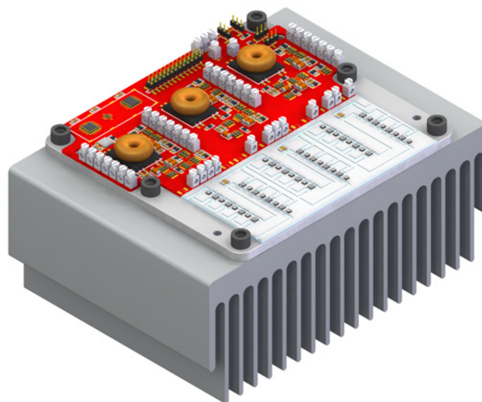

Figure 7. Conceptual design of the module.

In order to verify the one-dimensional calculations, the air speed required to obtain a 100 °C junction temperature rise was determined through a number of simulations. It was found that this occurs by setting the fan model to produce an airflow of 50 CFM, resulting in a temperature of 258 °C with an air speed through the heatsink of ~ 4 m/s.

Thermal results of this simulation are displayed in Figures 8 (the plane at the base of the bare die power devices), 9 (the plane passing through the heatsink), and 10 (the plane going across the heatsink). Additionally, the velocity plot is shown in Figure 11. In a down-hole system, heat transfer can be introduced via a dewer in place of forced air convection.

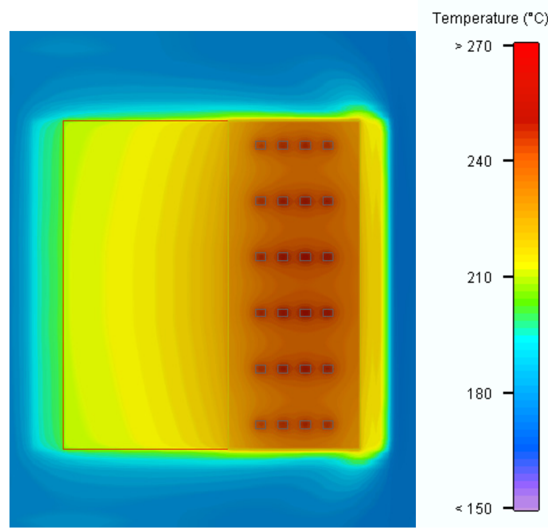

Figure 8. Y-Axis temperature plot.

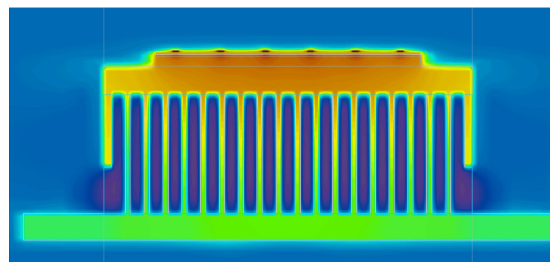

Figure 9. X-Axis temperature plot.

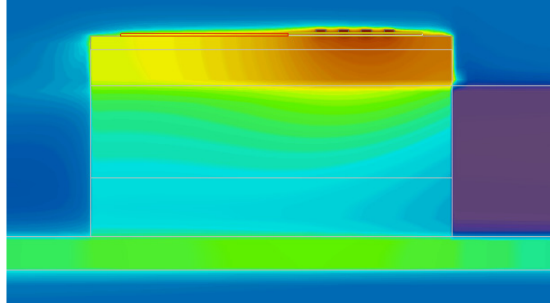

Figure 10. Z-Axis temperature plot.

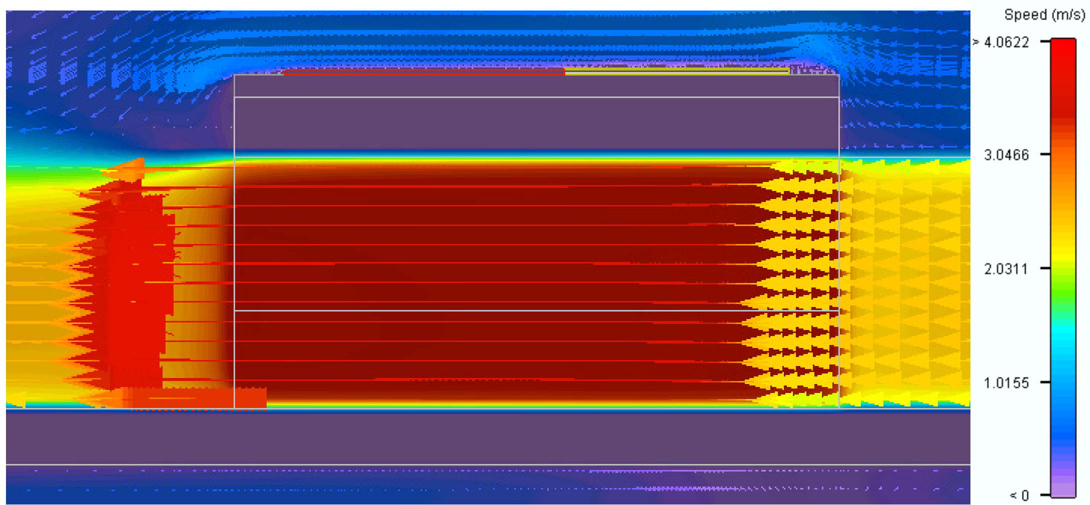

Figure 11. Z-Axis air velocity vector plot.

4.0 Inverter Testing

In order to demonstrate proof of concept and feasibility, a high-temperature single phase MCPM prototype inverter shown in Figure 12 is fabricated and tested. The prototype is a full-bridge topology with the integrated SOI control electronics. Four SiC power JFETs along with four SiC Schottky anti-parallel diodes are placed in parallel on the high and low sides of each switching pair. These power devices are mounted to an AlN DBC substrate that is mounted to a low CTE AlSiC heatspreader. The control circuitry including the SOI devices and passive components are mounted to a multilayer polyimide PCB that is attached to the heatspreader as well.

The inverter was tested successfully for high-power (~ 3 kW) operation at room temperature with a resistive/inductive load. The inverter was also tested successfully at high-temperature (250 °C) with the same load but with reduced power levels.

Figure 12. Single phase MCPM SOI/SiC prototype inverter.

4.1 High-Temperature Testing

The single phase inverter module is tested over temperature. It is operated with a load drawing 177 W at 126 V_{rms} from room temperature up to 250 °C at the base plate. The control signals for each switching position are monitored in order to determine the control circuitry response to extreme temperatures. Figure 13 shows a basic schematic representation of the power stage and the oscilloscope's probes location for each channel.

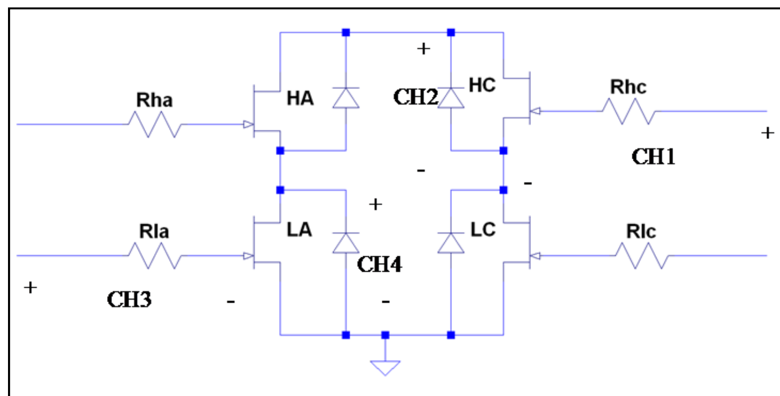

Figure 13. Power inverter stage schematic representation and probe positioning.

Figures 14 and 15 show the control signals and drain to source voltages operating at 25 °C, and 250 °C respectively with a dc bus voltage of approximately 200 V.

Comparison of the signals do not show noticeable degradation over the temperature range from 25 °C to 250 °C.

4.2 High-Power Testing

The inverter operated with a load processing 2.7 kW at 195.2 V_{rms} at the load. The test load includes a P-filter consisting of L1, L2, and C1 as shown in Figure 16.

Figure 17 shows the voltage across Rload (Vload), the current through the load (Iload), and the power at the load (Pload).

The input real power was calculated to be 3.158 kW. Figure 18 shows the input voltage (Vdc), the input current (Idc), and the input power (Pin).

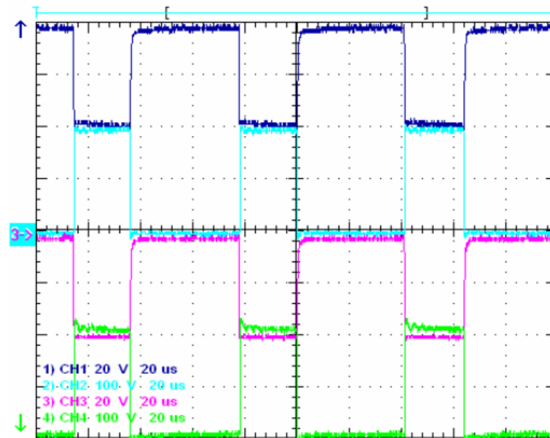

Figure 14. Control and drain to source voltages T = 25 °C.

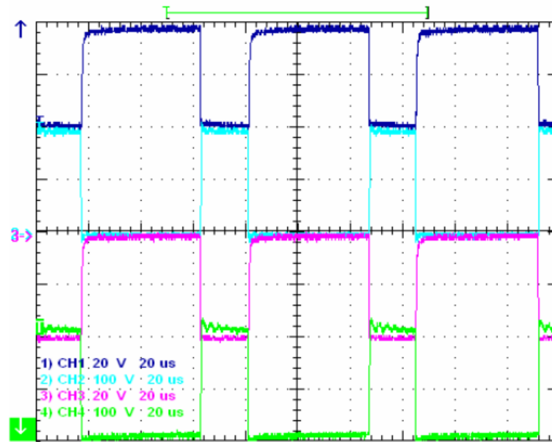

Figure 15. Control and drain to source voltages T= 250 °C.

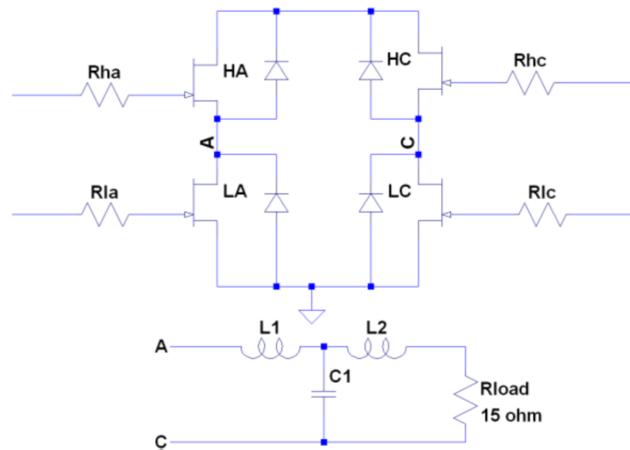

Figure 16. Power stage, filtering stage, and test load.

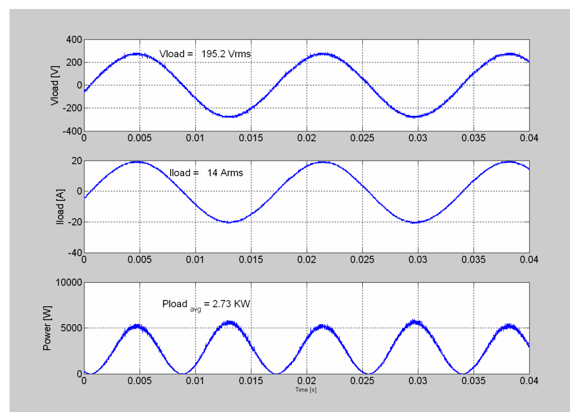

Figure 17. Vload, Iload, and Pload.

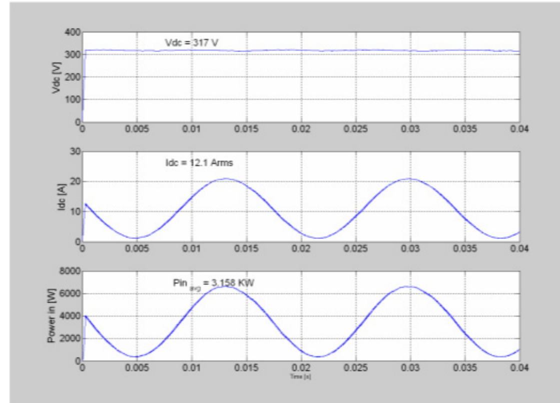

Figure 18. Vdc, Idc, and Pin.

The calculated input and output power are based on the fundamental frequency (60 Hz) components. In order to account for the real power losses in the filtering stage formed by L1, L2 and C1, the filter efficiency was characterized for various input voltages, and it has been determined to be 97 %. Estimated calculations put the efficiency of the high temperature inverter prototype at approximately 89%.

The inverter module has proven to be fully operational at high power with significantly reduced size (~7 × smaller) for comparable power inverters of the same voltage and power levels.

5.0 Conclusions

The full three-phase MCPM inverter with integrated SOI control electronics and SiC JFETs capable of driving a three-phase induction machine up to 4 kW at temperatures in excess of 250 °C is currently under test. The successful testing of the H-bridge inverter demonstrates proof of concept and is a step forward for SiC power converters. The power density was increased as expected and high-temperature packaging techniques were a success.

Acknowledgment

The work presented in this paper was funded in part by the U.S. Army Research Laboratories, the U.S. National Science Foundation, and the U.S. Department of Energy's energy storage division.

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APPENDIX

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CHAPTER 10

PACKAGING OF A HIGH-TEMPERATURE SILICON CARBIDE (SIC) THREE-PHASE 4KW MOTOR DRIVE

J. M. Hornberger, B. McPherson, E. Cilio, R.M. Schupbach,

A.B. Lostetter, and H. Alan Mantooth

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Abstract

The researchers at Arkansas Power Electronics International, Inc. have designed, developed, packaged, and manufactured the first complete multichip power module (MCPM) integrating SiC power transistors with silicon on insulator (SOI) control electronics. The 3 kW MCPM was detailed at IMAPS 2005 in Philadelphia, PA including the packaging of bare die low power SOI control components integrated with high-power SiC power transistors for operation at temperatures in excess of 250 °C. Significant advances have been made to the module since then including a miniaturization in size and volume and an increase in power handling, efficiency, functionality, and reliability. In this paper, the researchers will present results of high-temperature packaging techniques and advanced thermal modeling that was used to greatly improve the MCPM. Test results of a single phase version of the module operating at 250 °C and at 3 kW are presented along with initial test results of the full three-phase module.

Key words:

Silicon carbide (SiC), Silicon on Insulator (SOI), High-temperature electronics, High-temperature packaging, and Multichip power modules (MCPMs)

Introduction

During the late 1960's, the electronics industry was revolutionized by the silicon integrated circuit (IC), resulting in microelectronics applications shrinking by orders of magnitude in comparison with their discrete component counterparts. In the near future, the same type of revolution will occur in the power electronics industry. In this case, however, the change will not be driven by microelectronic ICs, rather it will be driven by the SiC power switch.

The future of power electronics will be greatly influenced by the commercialization of SiC semiconductor devices due to the promise of lighter, smaller, and more efficient systems. Since the first SiC power device was released to the commercial market (SiC Schottky diode in 2001), there has been an extensive effort to transfer other SiC power devices from the R&D labs [1]. These devices include the metal-oxide-semiconductor field effect transistor (MOSFET), junction field effect transistor (JFET), static induction transistor (SIT), gate-turn-off (GTO) thyristor, and bipolar junction transistor (BJT). With these SiC power devices the potential is present to develop highly miniaturized electronics modules and packages that will revolutionize the power electronics industry.

1.1 Silicon Carbide versus Silicon

SiC is a wide bandgap semiconductor material capable of high temperature operation. When compared to Silicon, SiC has 1/10th the switching losses, 10× the blocking voltage, 4× the thermal conductivity, 10× the switching speeds, and a junction temperature threshold in excess of 600 °C. All of these physical advantages will greatly increase power density capability (the chief limiting factor of today's power electronic systems) and drive those systems to shrink in size by orders of magnitude. Whereas the microelectronics IC drove computer mainframes the

size of wall cabinets to shrink in size to fit on a desktop, so too will SiC technology be the primary mover behind shrinking wall sized motor drive systems to fit in a briefcase.

Researchers and designers have already utilized some of the advantages of SiC through the use of zero reverse recovery SiC Schottky diodes in conjunction with Si power switches, realizing increases in converter efficiencies [2].

Many developments are yet to be made as SiC power device technology is still maturing and materials and device yields are greatly improving. As SiC power devices have been slowly developing and improving, manufacturers have produced SiC power switches that rival today's state-of-the-art Si technology [3, 4].

1.2 High-Temperature, High-Power Density Power Electronics

A powerful argument for using SiC power electronics is the size and weight reductions that can be achieved. To clearly illustrate these advantages, the researchers developed and analyzed Si and SiC half-bridge models in Flotherm thermal analysis software [5]. The simulations showed that a Si module with a 3 kg heatsink can achieve a maximum power of 5 kW assuming a junction temperature of 150 °C while a SiC module with a 0.3 kg heatsink can achieve a maximum power of 7.5 kW assuming a junction temperature of 600 °C. This implies that the use of a SiC module allows for a 50 % increase in power and a 90 % decrease in weight and volume.

To take full advantage of the high power density capabilities offered by SiC electronics, the development of high-temperature electronics as well as high-temperature packaging technologies and design methodologies are required. In particular, the integration of high temperature power devices and high temperature control electronics into a single module greatly minimizes parasitics, allowing very high frequencies of operation. The researchers are pursuing

these areas of development. Specifically, the authors have developed high-temperature multichip power modules (MCPMs) utilizing SiC power JFET devices integrated with silicon-on-insulator (SOI) control electronics.

1.3 SiC applications

The potential applications of SiC are widespread and all encompassing in the area of power electronics. Some applications include military vehicles (tanks, troop transports, unmanned vehicles, and ships), space exploration vehicles and landers, more electric aircraft, electric and hybrid-electric vehicles, nuclear power reactors, and petroleum and geological exploration instrumentation, Ultimately, any system that would see improvement from high-density or high efficiency power electronics would benefit from SiC.

Researchers at APEI, Inc. and the University of Arkansas have performed extensive research in the area of SiC device applications, packaging, and modeling for power electronic systems. Three high-temperature applications the researchers are currently working on that relate to the MCPM discussed here are: (1) three-phase motor drives for use in geological exploration (2) three-phase motor drives for use in the US Army's Future Combat Systems (FCS) vehicles and (3) three-phase inverters for portable grid-tie applications.

Energy companies are interested in SiC power electronics for deep earth petroleum exploration where hostile environments with high ambient temperatures are encountered. The down hole orbital vibrator (DHOV) from Cole Engineering requires the integration of a high-temperature motor drive with a three-phase induction machine in order to perform deep earth geological mapping. It is difficult to place Si electronics down hole because of the extreme environment found within the oil wells. With SiC and SOI electronics, it is possible to send the

electronics down hole with the motor, thus greatly improving motor drive control and efficiency [6].

The goal of the U.S. Army's FCS hybrid-electric combat vehicles is to decrease vehicle weight (by as much as one-half), increase maneuverability, and increase survivability over today's state of the art systems. In order to accomplish these goals, the vehicles must use high-power converters and motor drives that are capable of operating in harsh environments. By utilizing SiC power devices, high power densities can be achieved with little or no heatsinking, resulting in a reduction of the size and weight of the converters, thereby reducing the overall size and weight of the combat vehicle.

The US Department of Energy is seeking high-power density, high-efficiency three-phase inverters for renewable energy applications. A smaller lighter weight SiC based inverter will reduce the size of today's state leading edge cabinets and will be more portable in applications where a power grid is not near by. Additionally renewable energy sources such as solar arrays that may be near a grid, could tie in and feed back excess power to the power system.

2.0 Three-Phase Multichip Power Modules

SiC devices are capable of operating into the GHz frequency range; a great reduction in the size of passive components such as capacitors, inductors, and other magnetic components is expected. Integrating control and power layers into a single module significantly reduces size, weight, and parasitic effects. This approach is known as a multichip power module where multiple layers are utilized to separate the power and control circuitry [7-9].

2.1 Electrical Design

The electrical design of the MCPM stems from a demonstration three-phase motor control developed by APEI, Inc. for high temperature operation. The high-temperature motor

controller shown in Figure 1 operated in an ambient environment of 250 °C and is detailed in [10]. The high-temperature controller was expanded to a full MCPM utilizing SOI control components and SiC JFET power switches as pictured in Figure 2.

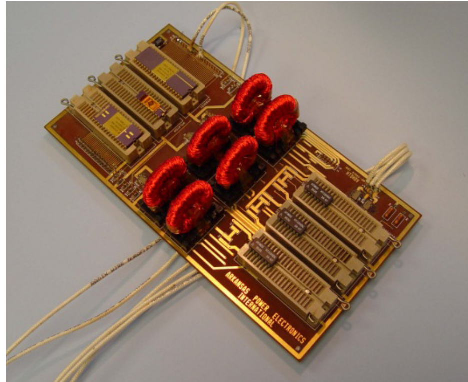

Figure 1: 250 °C 3-phase motor control prototype.

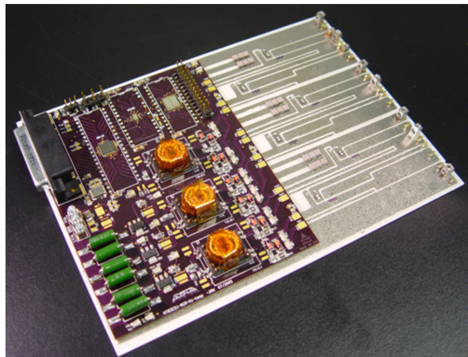

Figure 2: 250 °C 3-phase multichip power module.

The core control contains an HT80C51 SOI microcontroller from Honeywell, latch, SRAM, and in-house developed software to generate the control signals required for a three-phase motor drive. The MCPM design contains start up circuitry and voltage regulation to deliver power from the DC bus to the low voltage control logic. The module incorporates isolation between the high-voltage power stage and the low voltage digital control with the use of high-temperature surface mount transformers built by APEI, Inc. The gate driver stage can be

customized to drive several different types of SiC power switches including MOSFETs, JFETs, and BJTs.

2.2 MCPM Package Design

The MCPM has two main stages, the low voltage control and the high voltage power stage. The mechanical design and power electronic packaging aspect of the MCPM focuses on combining 1) a high-power, high-temperature dual layer ceramic substrate and 2) a high-density, high-temperature multi-layer PCB. The cross-section of this design methodology is illustrated in Figure 3, while Figure 4 illustrates an isometric view.

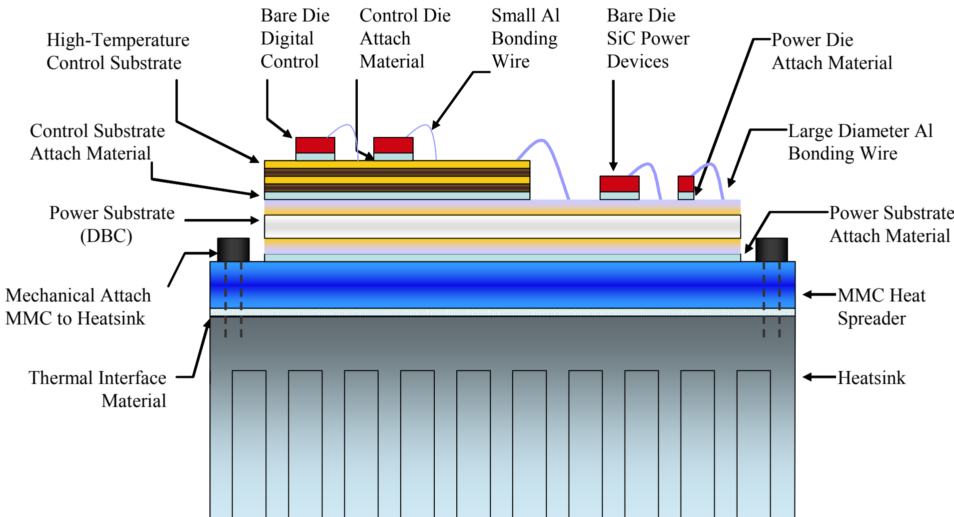

Figure 3: Cross-section of the MCPM design.

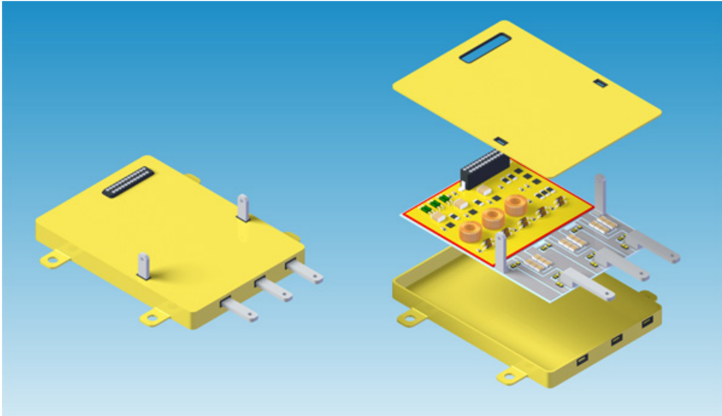

Figure 4: Conceptualized High-Temperature MCPM.

The major components to consider in the package design consist of the power substrate, heat spreader or base plate, control substrate, wirebonds, die attaches and passivations.

An important step in choosing packaging materials for power electronics is matching the coefficient of thermal expansion (CTE) for adjoining parts. Since SiC transistors will be used in the power stage, it is important to closely match the CTE of the power substrate, and heat spreader to that of SiC (between 4.6 and 5.1 ppm/°C) to reduce failure due to thermal stress. Table 1 compares the characteristics of common substrates used in power electronics to that of SiC.

Table 1: Material properties of power substrates.

Material	CTE *(ppm /°C)*	Thermal Conductivity *(W/m °K@25 °C)*	Max. Use Temp *(°C)*	Elastic Modulus *(GPa)*	Tensile Strength *(MPa)*
Alumina	6.0	24 - 33	1600	310	130
Aluminum Nitride	4.6	150 - 180	1000	310	310
Beryllium Oxide	7.0	270	1093	345	230
Silicon Carbide	4.6 - 5.1	120	1000	412	17
Silicon Nitride	3.0	70	1000	314	96

For the MCPM, Aluminum Nitride (AlN) with 12 mil thick copper on both sides plated with a thin Ni layer was chosen for the power substrate for three main reasons. First, AlN has a CTE that matches closely with SiC and therefore will help eliminate thermal stresses. Second, AlN has a high thermal conductivity and will dissipate heat better than alumina and silicon nitride. Thirdly, AlN is cost effective (compared to silicon nitride) and widely available through companies like Curamik.

The selection of a heat spreader or base plate is important to the package as it provides mechanical strength and is in the direct line of heat transfer from the power substrate to the heat sink or heat exchanger. Heat spreaders are often made out of metals such as copper, aluminum and metal-matrix-composites (MMCs). Table 2 compares the characteristics of different base plate materials.

The heat spreader implemented in the MCPM is that of AlSiC. The selection of the heat spreader is made from three main criteria. First, the CTE of an MMC can be adjusted to match the CTE characteristics of the rest of the package to reduce the stresses of thermal expansion within the MCPM. Second, the thermal conductivity of the AlSiC is excellent for heat transfer. Thirdly, AlSiC is available commercially.

Table 2: Base plate material comparison.

Material	CTE *(ppm /℃)*	Thermal Cond. *(W/m℃K@25℃)*	Max. Use Temp *(℃)*	Elastic Modulus *(GPa)*	Tensile Strength *(MPa)*
Aluminum	23.4	222	660	70	455
Copper	17.3	398	1083	131	220
AlSiC	7 - 14	170 - 200	--	188	488
BeBeO	6 - 9	210 - 240	--	--	--

The control circuitry typically has many connections requiring dense trace routing on multiple layers to achieve compactness. This type of routing is not typically achievable with thick power substrates and must be done with printed circuit board (i.e., FR4-type) substrates. In order to reduce stresses on plated through holes caused by movement in the Z-direction and reduce trace delamination from the surface when operating at high-temperatures, a high-Tg material must be used.

To operate at high-temperatures, a substrate with a high Tg is needed such as Isola P96 (Tg > 260 °C), Rogers 4000 (Tg = 280 °C) or Arlon 527 (Tg=350 °C). Since the MCPM is targeted to operate at 250 °C, the researches utilized a 5 layer Isola P96 polyimide PCB for the control substrate.

The SiC power devices are wirebonded with large diameter (10 mil) Al bonding wire to carry the power from the top-side contacts to the Ni plated DBC traces. The researchers have performed thermal cycling experiments that show Al wire bonding to Ni DBC substrates and Au wirebonding to Au substrates are reliable above the targeted 250 °C operation temperature [11, 12].

Since the SiC power devices are vertical devices, the connection between the die and the substrate are not only important for heat transfer, but also for electrical or current transfer as well. This attachment must be accomplished by a metallurgical process such as soldering. Since the operating temperature of the MCPM will be approximately 250 °C, a solder above 300 °C solidus is preferred. The solder used in the MCPM is 92.5Pb / 5.0In / 2.5 Ag (310 °C liquidus) from Indium corporation. This solder is also used to mount the control die to the polyimide substrate.

3.0 Thermal Modeling

To verify the MCPM design for high-temperature operation, a thermal model was generated in FLOTHERM for detailed 3D thermal analysis. The goal of the thermal simulations was to closely estimate and simulate the actual conditions experienced in the test setup of the MCPM. One-dimensional calculations were used to determine the proper heatsink required for a temperature rise at the power switches of 100 °C in a 150 °C ambient, resulting in a maximum junction operating temperature of 250 °C. Neglecting the die attach layer, the thermal resistance

per SiC device was calculated as in Eq. 1 where t is the thickness of the material (m), k is the thermal conductivity (in Watts/m·K) and A is the cross-sectional area (m^2).

$$R_{\theta Total} = \left(\frac{t_{Copper1}}{k_{Copper1} \cdot A}\right) + \left(\frac{t_{AlN}}{k_{AlN} \cdot A}\right) + \left(\frac{t_{Copper2}}{k_{Copper2} \cdot A}\right) + \left(\frac{t_{Baseplate}}{k_{Baseplate} \cdot A}\right) + R_{\theta SA} \qquad \text{Eq. 1}$$

The total thermal resistance represents the path through the top copper layer, the AlN ceramic, the bottom copper layer, and the AlSiC heatspreader. The cross-sectional area used in the thermal resistance calculation can be assumed to start at the base of the SiC power die generating the heat (due to electrical losses). The thermal contact area increases as the path moves through the varying layers. The angle of this spreading is a function of the thermal conductivities of the two materials in contact, and is determined quantitatively by Eq. 2, and the change in thermal contact area is governed by Eq. 3, where α is the angle of thermal spreading and L is the length of the thermal interface [13]. This increase in contact area results in an effective decrease in the thermal resistance of the material. Layer thicknesses, calculated thermal contact areas, and their thermal resistance are presented in Table I.

$$\alpha_a = \tan^{-1}\left(\frac{k_a}{k_b}\right) \qquad \text{Eq. 2}$$

$$L_2 = 2 \cdot t_a \cdot \tan(\alpha_a) + L_1 \qquad \text{Eq. 3}$$

Table 3: Thermal resistances of each layer.

			Thermal	
Material	Thickness (m)	Area (m^2)	Conductivity (W/mK)	Resistance (°C/W)
Copper 1	3.048×10^{-4}	1.54×10^{-5}	385	0.051
Aluminum Nitride	6.35×10^{-4}	2.01×10^{-5}	170	0.186
Copper2	3.048×10^{-4}	3.19×10^{-5}	385	0.025
AlSiC Baseplate	5.08×10^{-3}	1.66×10^{-4}	200	0.153
TOTAL				0.415

The theoretical worst-case efficiency is assumed to be 83% at 250 °C, where the increased on-resistance of the power devices results in an increase in losses. The assumed thermal loss of the entire module at full power (i.e., 4kW) is estimated to be approximately 650 W (27 W per SiC JFET). This loss is evenly distributed among the twenty four different SiC

JFETs used in the power stage. The devices are far enough apart from each other that they will not interfere with the thermal spreading of the neighboring die. A total junction to sink thermal resistance can be determined by adding the twenty four thermal resistances in parallel, resulting in an $R_{\theta JS}$ value of 0.017 °C/W. The maximum thermal resistance allowable for the heatsink for a 100 °C rise is calculated to be 0.183 °C/W.

High fin density profiles were examined, and the most effective profile (i.e., lowest thermal resistance vs. weight) was selected. To minimize the heatsink length to the dimensions of the module (5.4 inches), a forced convection airflow of 2.4 m/s was necessary. A three-dimensional conceptual model, displayed in Figure 5, was also developed for the three-phase SiC-based MCPM.

In order to verify the one-dimensional calculations, the air speed required to obtain a 100 °C junction temperature rise was determined through a number of simulations. Thermal results of this simulation are displayed in Figures 6 (the plane at the base of the bare die power devices), 7 (the plane going across the heatsink), and 8 (the plane passing through the heatsink).

The results in Figure 6-8 display excellent thermal spreading, and an effective removal of generated heat through the heatsink. Figure 7 shows that a maximum die junction temperature of 258 °C occurs under maximum power and with an airflow of 50 CFM implying a 108 °C rise in junction temperature over the ambient of 150 °C.

4.0 Testing Results

In order to demonstrate proof of concept and feasibility a 4 kW prototype module was built but with only two of the phases populated for single-phase full-bridge operation, Figure 9 shows the fabricated 4 kW module. Four SiC power JFETs along with four SiC Schottky anti-parallel diodes are placed in parallel on the high and low sides of each switching pair. These

power devices are mounted to an AlN DBC substrate that is mounted to a low CTE AlSiC heatspreader. The control circuitry including the SOI devices and passive components are mounted to a multilayer polyimide PCB.

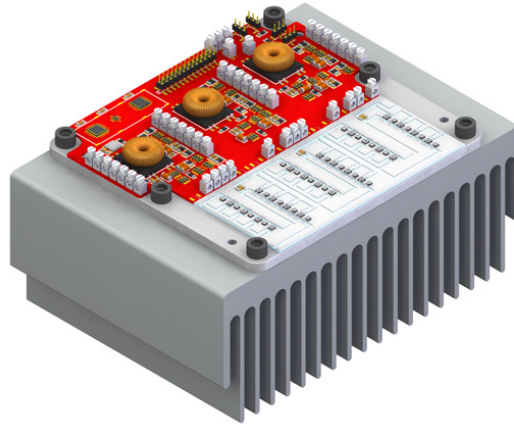

Figure 5: Conceptual design of the module.

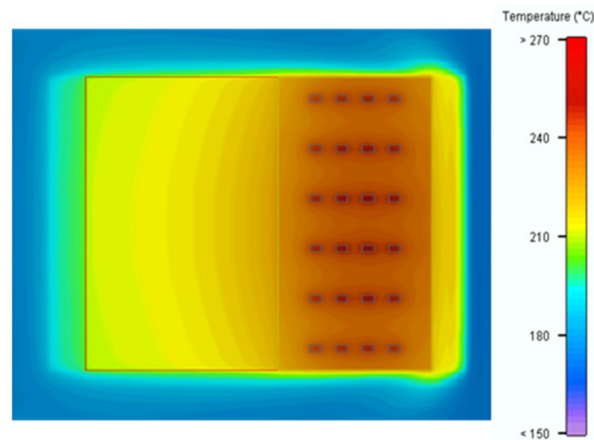

Figure 6: *Y*-Axis temperature plot.

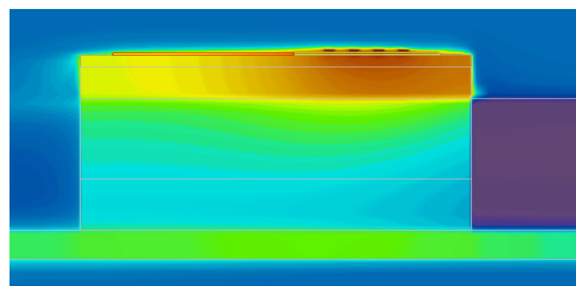

Figure 7: *Z*-Axis temperature plot.

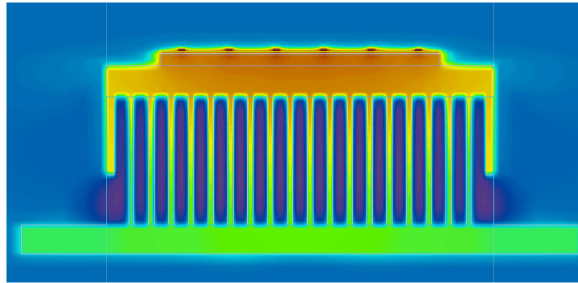

Figure 8: X-Axis temperature plot.

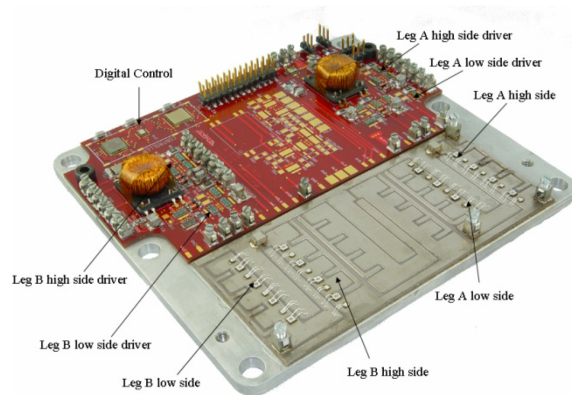

Figure 9: Single-phase MCPM inverter module without heatsink.

4.1 High-Temperature Testing

The single phase inverter module was tested over temperature. It was operated with a load drawing 177 W at 126 V_{rms} from room temperature up to 250 °C at the base plate. The control signals for each switching position are monitored in order to determine the control circuitry response to extreme temperatures. Figure 10 shows a basic schematic representation of the power stage and the oscilloscope's probes location for each channel.

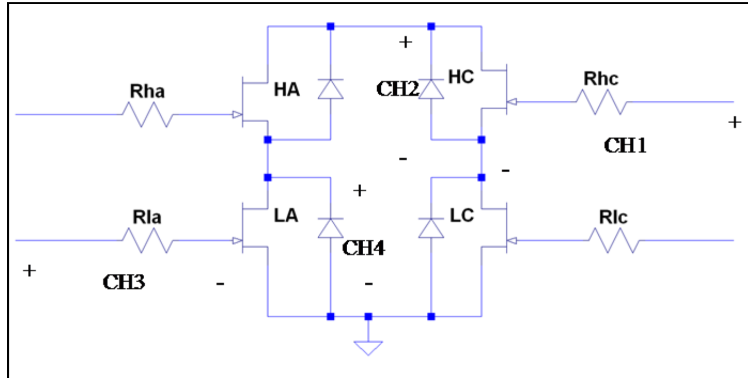

Figure 10. Power inverter stage schematic representation and probe positioning.

Figures 11 and 12 show the control signals and drain to source voltages operating at 25 °C, and 250 °C respectively with a dc bus voltage of approximately 200 V. Comparison of the signals do not show noticeable degradation over the temperature range from 25 °C to 250 °C.

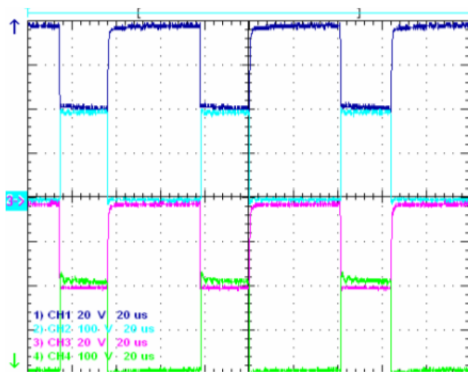

Figure 11: Control Signals and V_{DS} T = 25 °C.

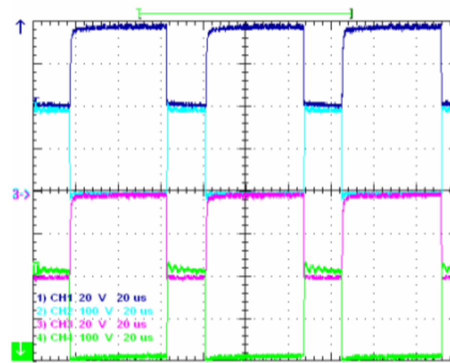

Figure 12: Control Signals and V_{DS} T = 250 °C.

4.2 Full Power Testing

After successful testing at high-temperature, the single-phase module was tested successfully for high-power (~ 3 kW) operation at room temperature with a resistive/inductive load. The inverter operated with a load processing 2.7 kW at 195.2 Vrms at the load. The test load includes a T-filter consisting of L1, L2, and C1 as shown in Figure 13.

Figure 14 shows the voltage across Rload (Vload), the current through the load (Iload), and the power at the load (Pload). The input real power was calculated to be 3.158 kW. Figure 15 shows the input voltage (Vdc), the input current (Idc), and the input power (Pin). The instantaneous input and output power were calculated using the recorded instantaneous input and output voltages and currents.

The calculated input and output power are based on the fundamental frequency (60 Hz) components. In order to account for the real power losses in the filtering stage formed by L1, L2 and C1, the filter efficiency was characterized for various input voltages, and it has been determined to be 97 %. Based on preliminary calculations the efficiency of the power module, while operating at room temperature, is a minimum of 90 %. Since these efficiency calculations do not take into account the high-frequency harmonics dissipated in the output filter, it is estimated that the actual efficiency of the power stage is significantly higher; however, the exact efficiency requires the use of a calorimeter or high-frequency power measurement device (i.e., power analyzer), which has not yet been performed.

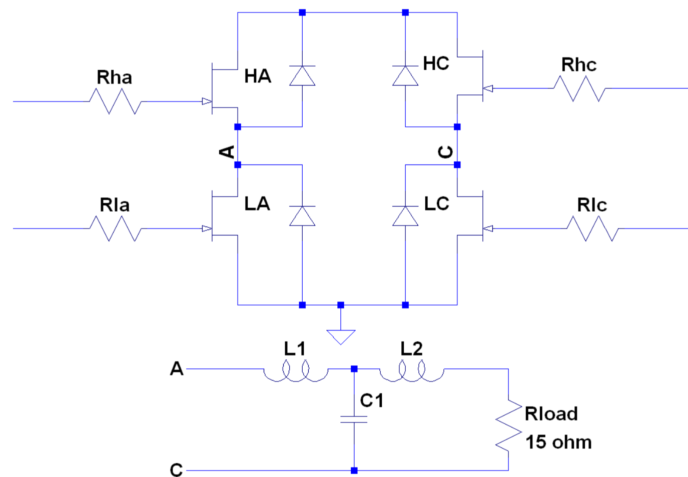

Figure 13: Power stage, filtering stage, and test load.

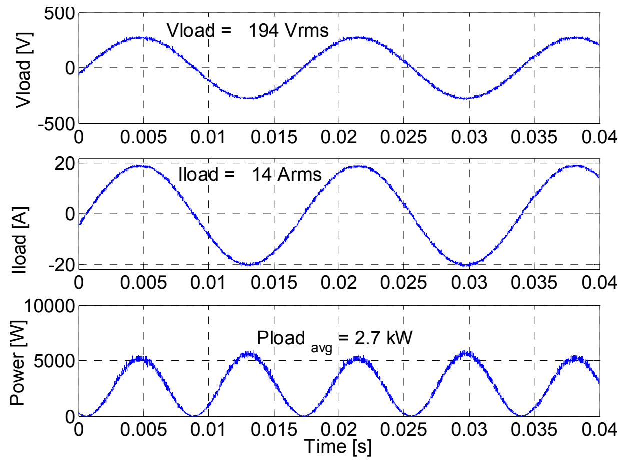

Figure 14: Voltage across load resistor (Vload), current through the load (Iload), and power dissipated by the resistive load (Pload).

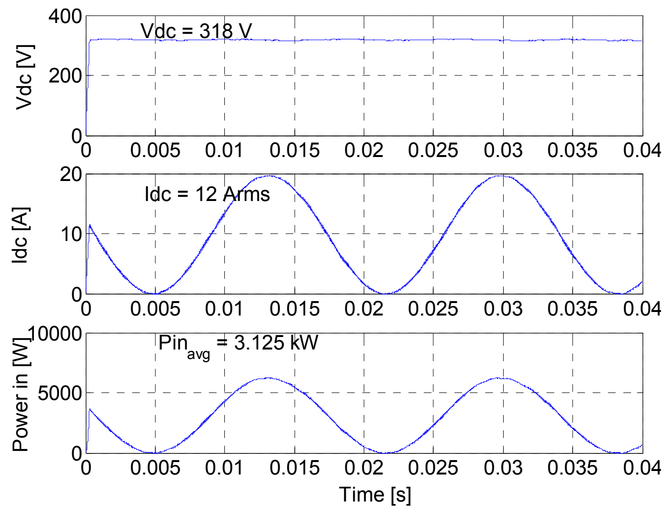

Figure 15: Input voltage (Vdc), input current (Idc), and input power (Pin).

Conclusions

This paper has presented the electrical, packaging, and thermal design a three-phase MCPM. Additionally, testing of a dual-phase (single-phase H-bridge) high-temperature module has shown feasibility of SiC MCPM technology. The initial testing of the SiC MCPM shows high potential for an increase in power density. When compared with state-of-the-art Si-based

modules, a size reduction of up to 7 × may be achievable using APEI, Inc. high-temperature MCPM design approach.

A full three-phase module has been built and is pictured in Figure 16. Testing of the three-phase module is underway and initial results are promising. The module will be tested at high-temperature and full power to further demonstrate the MCPM concept and its ability to reduce the size of power electronic systems.

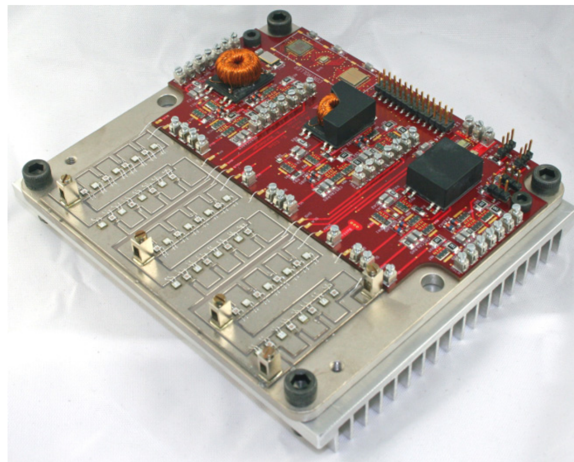

Figure 16: Three-phase SiC MCPM module.

Acknowledgments

The work presented in this paper was funded in part by the U.S. Army Research Laboratories, the U.S. National Science Foundation, and the U.S. Department of Energy's energy storage division.

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APPENDIX

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Brian Schieman – Director, Program Development and Technology

CHAPTER 11

A FULLY INTEGRATED 300°C, 4 KW, 3-PHASE, SIC MOTOR DRIVE MODULE

Jared M. Hornberger, Edgar Cilio, Brice McPherson, Roberto M. Schupbach,

Alexander B. Lostetter, and H. Alan Mantooth

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Abstract

The researchers have designed, developed, packaged, and manufactured a complete multichip power module (MCPM) that integrates silicon carbide (SiC) power transistors with silicon on insulator (SOI) control electronics. The SiC MCPM approach targets the reduction of size and the increase in efficiency of power electronic systems resulting in a highly miniaturized, high power density module. The researchers previously presented a single phase 3 kW SiC inverter that was also proven operational to 250 °C at 500 W. In this paper APEI, Inc. will present a new SiC three-phase inverter that has been fully tested to 4 kW at 300 °C operation. In this paper, the researchers discuss the challenges associated with high-temperature operation of power electronics, including the electrical, mechanical, and thermal design. Many electronic packaging problems have been solved to enable high-temperature operation of these modules. These packaging issues will be discussed as well as remaining problems that still need advancing. Finally, the full temperature and full power (300 °C at 4kW) test results are presented.

I. INTRODUCTION

The past decade has seen an intense and steady increase into the research of the viability of silicon carbide (SiC) device technology. This technology has the potential to solve many of the current limitations associated with silicon (Si) electronics; in particular, limitations with

respect to switching speeds, junction temperatures, and power density. The utilization of high-power SiC devices is set to revolutionize the power electronics industry and bring the benefit of improved efficiency and improved reliability to the commercial markets while simultaneously benefiting society through improving energy savings on a global scale.

A. Aadvantages of SiC

SiC is a wide bandgap material capable of high temperature operation theoretically up to 600 °C. When compared to the state-of-the art Si devices, SiC can be used at much higher temperatures (~ 5 times higher), possess a higer breakdown voltage (~10 times higher), possess lower switching losses, and are capable of higher current densities (~ 3-4 times higher).

B. High-Temperature, High-Power Density Electronics

The most advantageous aspects of using SiC power switches are the size and weight reductions that can be achieved. To clearly illustrate these advantages, the researchers developed and analyzed Si and SiC half-bridge models in Flotherm thermal analysis software [1]. The simulations showed that a Si module with a 3 kg heatsink can achieve a maximum power of 5 kW assuming a junction temperature of 150 °C while a SiC module with a 0.3 kg heatsink can achieve a maximum power of 7.5 kW assuming a junction temperature of 600 °C. This implies that the use of a SiC module allows for a 50 % increase in power and a 90 % decrease in weight and volume.

To take full advantage of the high power density capabilities offered by SiC electronics, the development of high-temperature electronics as well as high-temperature packaging technologies and design methodologies are required. In particular, the integration of high temperature power devices and high temperature control electronics into a single module greatly minimizes parasitics, allowing very high frequencies of operation. The researchers are pursuing

these areas of development. Specifically, the authors have developed high-temperature multichip power modules (MCPMs) utilizing SiC power JFET devices integrated with silicon-on-insulator (SOI) control electronics.

II. MULTICHIP POWER MODULES

SiC devices are capable of operating into the GHz frequency range; a great reduction in the size of passive components such as capacitors, inductors, and other magnetic components is expected. Integrating control and power layers into a single module significantly reduces size, weight, and parasitic effects. This approach is known as a multichip power module where multiple layers are utilized to separate the power and control circuitry [2-5].

A. MCPM Electrical Design

The electrical design of the MCPM stems from a demonstration three-phase motor control developed for high temperature operation. The high-temperature motor controller operated in an environment of 250 °C and is detailed in [6]. Figure 1 illustrates the circuit block diagram of the current MCPM design.

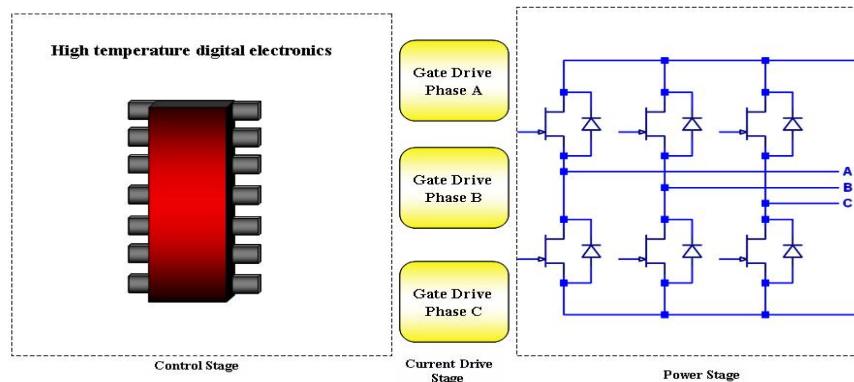

Fig 1: Schematic diagram of the three-phase MCPM.

Electrically, the SiC-based three-phase MCPM is divided into three main stages, namely: control, gate drive, and power stage (see Fig. 5). The characteristics and electrical design of each of these high-temperature stages are discussed below.

1) Control Stage:

The core of the control stage is the silicon-on-insulator (SOI) HTMOS 83C51 high-temperature microcontroller manufactured by Honeywell's Solid State Electronics Center (SSEC). The HT83C51 is a monolithic 8-bit high-temperature (up to 300 ºC) microcontroller that is pin equivalent to the Intel 8XC51FC microcontroller. Other key components within the control stage are the oscillator, voltage regulator, and random access memory.

The 16 MHz oscillator is a 5 V extended temperature (above 250 °C) oscillator. This oscillator replaces the function of a typical crystal/capacitive network combined with the onboard oscillator. The HTPLREG05 is an onboard 5 V linear regulator used to provide stable power to the controller stage from an unregulated 12 V to 15 V supply. A 8-bit latch is used to interface the HT83C51 with the external RAM. This latch was custom-packaged by APEI, Inc. to withstand temperatures of up to 250 ºC. The 32K (32,768 word × 8-bit) external RAM (HT6256) is a high temperature static random access memory manufactured by Honeywell, with industry-standard functionality.

2) Gate Drive Stage:

The output of the microcontroller does not have the correct voltage level and current carrying capabilities to drive the gate of a switching position. The voltage level is conditioned to deliver the right voltage amplitude, polarity, and current through the gate drive stage. High temperature electronics and passives make up the amplifying stage that provides the correct voltage.

3) Power Stage:

Three single-phase legs make up the power stage (see Fig. 5). Each switching position is composed of two paralleled 4-A, 600-V SiC Schottky diodes manufactured by Cree and two SiC

JFETs manufactured by SiCED. The SiC power switches used here are experimental devices, available only as engineering samples; therefore, their electrical ratings are based upon design and not guaranteed by experimental characterization. These ratings are 1200 V and 5 Amps.

B. MCPM Mechanical / Package Design

One of the major contributors to the overall size and weight of a power conversion system is the cooling system (i.e., heatsink). High temperature electronics allow the minimization of the cooling system requirements due to the increased allowable temperature rise over ambient. Moreover, high temperature electronics allow implementing passive cooling strategies while still achieving very high power densities. Because SiC devices are capable of operating into the GHz frequency range; a great reduction in the size of passive components such as capacitors, inductors, and other magnetic components is expected. The MCPM design approach reduces parasitic effects in high frequency operation.

Figure 2 illustrates a cross-section of the MCPM package design while Figure 3 represents the conceptualized isometric view of the packaging approach . The MCPM design utilizes a multiple layer design approach separating the power and control circuitry. The MCPM is built in two major stages. The first stage consists of the direct bond-copper (DBC) power substrate, where Ni plated copper plates are directly bonded to either side of an AlN ceramic substrate.

The metallization traces on this power substrate are designed specifically for the capability to conduct large amounts of current at high voltages. The high power bare-die SiC devices are mounted with a 310 °C Pb-In solder directly to the AlN DBC substrate providing an excellent thermal path to the heatspreader. The second stage is the control board. Because of the demanding power and thermal requirements, the power substrate metallization traces cannot be

tightly patterned for high density control electronics. Instead, the control board is fabricated from a high temperature multilayer polyimide substrate. The metallization traces on these layers are flash gold plated for improved reliability. The control components are bare-die devices wirebonded with gold wire, surface mount passives, and magnetic components. The control board is mounted to the high power substrate by a high temperature adhesive. The heatspreader of the MCPM is a metal-matrix-composite material, in this case AlSiC is used. The heatspreader offers excellent thermal conduction capabilities while simultaneously providing a close CTE match to the DBC ceramic substrate reducing stresses and the chances of thermal failures. Thermal simulations were performed using Flotherm to estimate the size of heatsink needed and the SiC device junction temperature at full power and temperature and are detailed in [7].

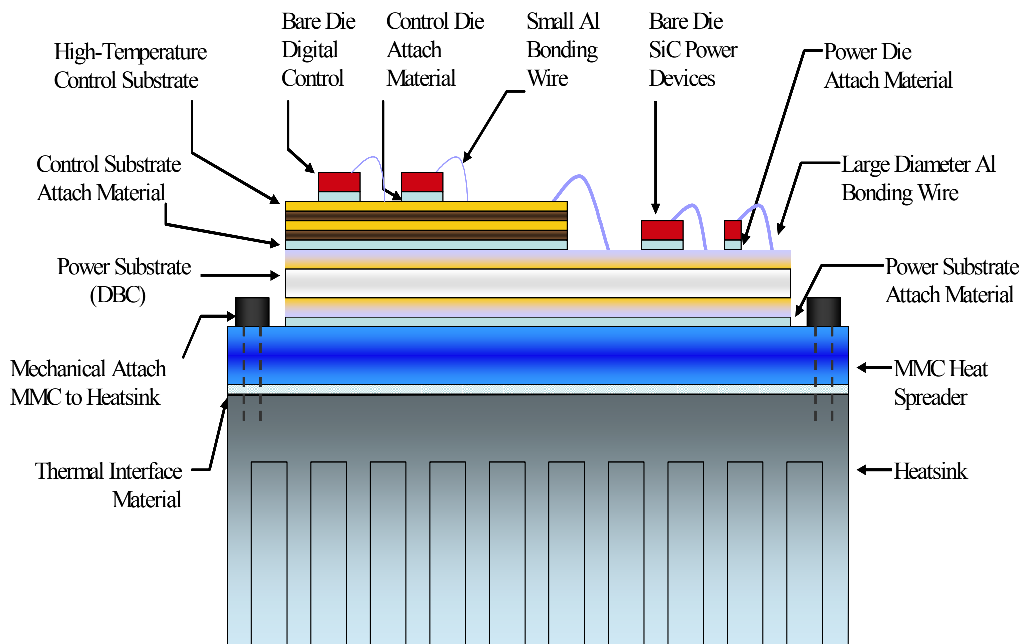

Fig. 2: Cross-section of the APEI, Inc. MCPM design.

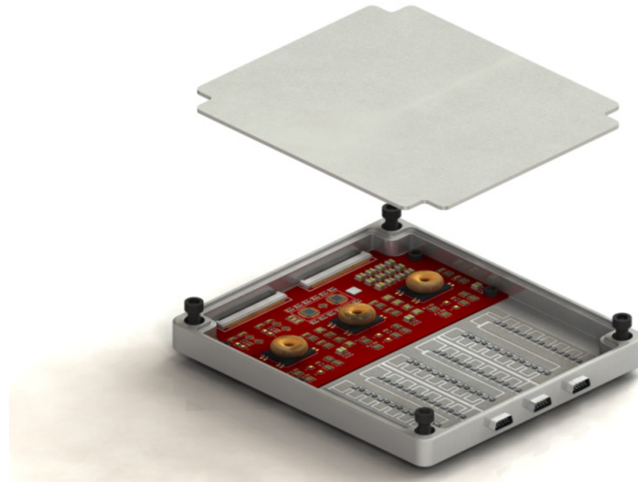

Fig. 3: Conceptualized High-Temperature MCPM.

APEI, Inc. has performed many studies on different packaging techniques for use at high-temperature. Of particular interest are wire bonds that are qualified for high-temperature operation (up to 600 °C) of small diameter (0.7 to 3 mil) gold wires as well as large diameter (5 to 26 mil) aluminium wires [8]. Substrate technology is also very important as temperatures rise above 150 °C care must be taken that proper barriers are in place to stop the diffusion of metals layers within a substrate, the researchers have successfully modelled and tested substrates at temperatures above 500 °C. [9].

Other unpublished advances that have been made by the researchers include die attach and substrate attachment for operation above 500 °C. Current issues that are being solved include the encapsulation of SiC power devices for high-voltage blocking at high-temperature operation. Figure 4 is an SEM capture of a SiC JFET encapsulated with an experimental material. The device underwent thermal cycling and 12 hour 300 °C storage. As a result, fractures appeared in the capsulation around the edges and across the top of the die. These fractures compromise the high-voltage blocking capabilities of the device. Figure 5 is a cross section of the encapsulation of a JFET after curing showing the non-uniformity of coverage on the edges of the device. These

non-uniformities can lead to catastrophic device failures due to voltage breakdown during operation.

In short, there are still many packaging issues left on the table that need to be solved to enable the full potential of SiC.

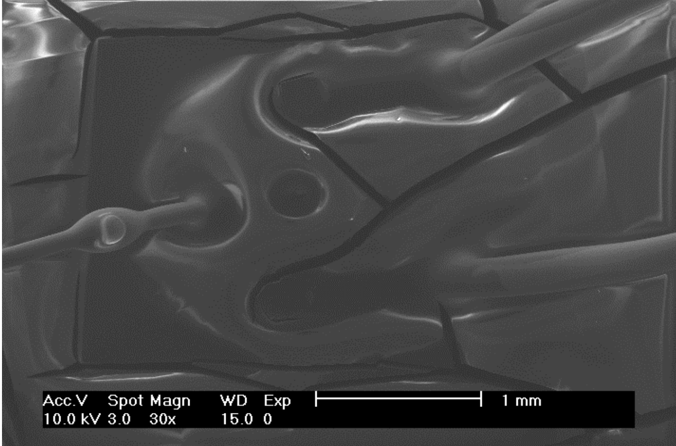

Fig. 4: Encapsulated SiC JFET.

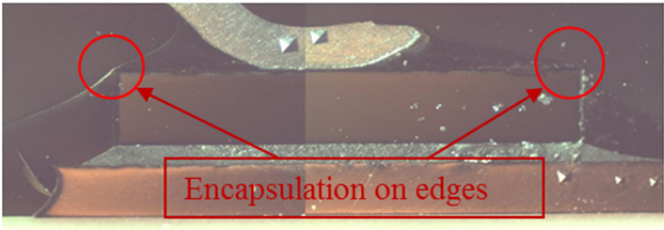

Fig. 5: Cross section of an encapsulated SiC JFET.

III. High Temperature Testing

The module was tested at two different power levels through various balanced Y-connected three phase resistive loads. A three phase Y-connected T-type LCL load filter was connected between the MCPM outputs and a resistive load in order to filter out the higher order PWM switching harmonics. The filter inductors used were three phase line reactors and the

capacitors were a metal polypropylene dielectric. Figure 6 shows the assembled MCPM mounted for testing while pointing out the various portions of the circuit.

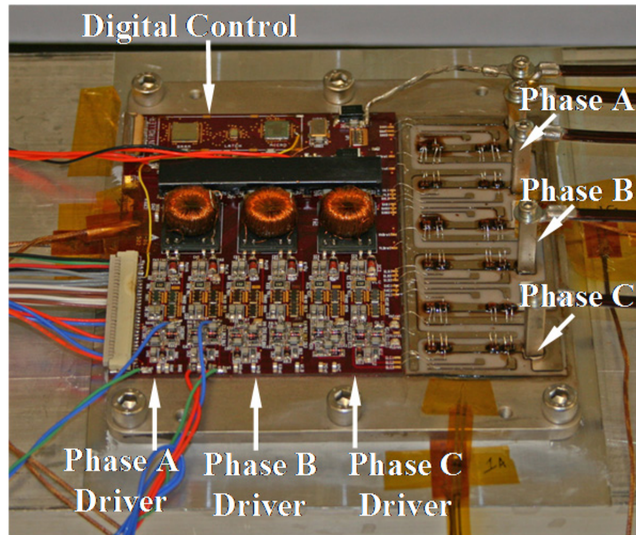

Fig. 6: Fully integrated three-phase MCPM inverter.

The objective of the low power test was to demonstrate functionality of the module while at a high temperature baseplate environment and operating under high voltage (up to approximately 600 V DC).

Mechanically, die attaches and substrates performances were monitored. Both room temperature measurements and high temperature (250 ºC at the baseplate) measurements were taken while the module was supplying approximately 1 kW to a resistive load.

Fig. 7 (25 ºC) and Fig. 8 (250 ºC), show the unfiltered output voltage (Ch. 1-blue) of a single phase of the module and the three output voltages of the module after passing through the LCL output filter (Ch. 2-cyan, Ch. 3-magenta, Ch. 4-green). It can be seen that the filtered outputs are sinusoidal with the appropriate phase angle associated with each waveform. Fig. 9 and Fig. 10, show the unfiltered output current (Ch. 1-blue) of a single phase of the module and the three output currents of the module after passing through the LCL output filter (Ch. 2-cyan,

Ch. 3-magenta, Ch. 4-green). It can be seen that the filtered outputs are sinusoidal with the appropriate phase angle associated with each waveform.

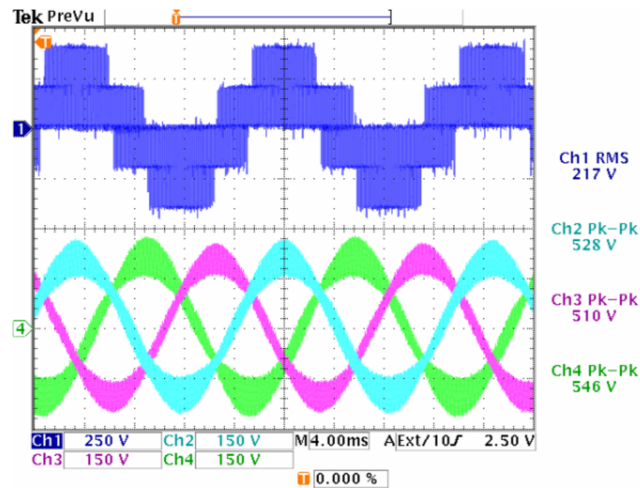

Fig. 7: Module output voltages. Unfiltered single phase output voltage (blue) and filtered three phase output voltages. T = 25 ºC.

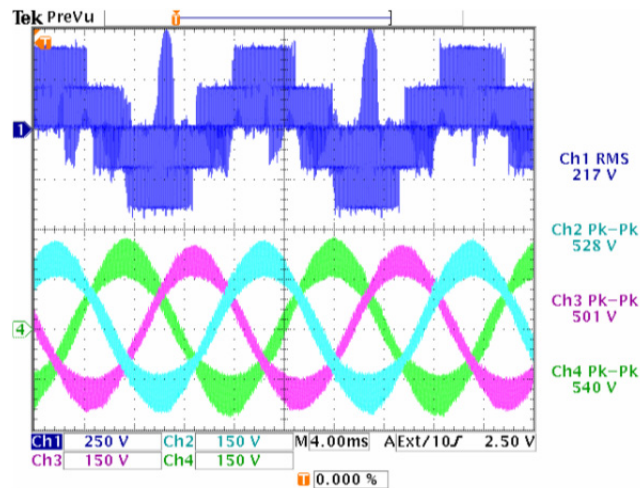

Fig. 8: Module output voltages. Unfiltered single phase output voltage (blue) and filtered three phase output voltages. T = 250 ºC.

After the module was tested to 1 kW, the load setup was changed to perform 4 kW testing. This test was performed to ensure correct operation of the power stage primarily. The thermal distribution measurements helped determine the accuracy of the preliminary thermal assumptions and also measure the actual temperature difference between the heatsink, the base plate, and the power substrate at full power operation. The voltages shown in Fig. 11 (25 ºC)

follow the same order as described for Fig. 7 and 8. Similarly, the currents shown in Fig 12 (25 ºC) follow the organization detailed for Fig. 9 and Fig. 10. Table II summarizes the thermal distribution at different stages of the module under this test.

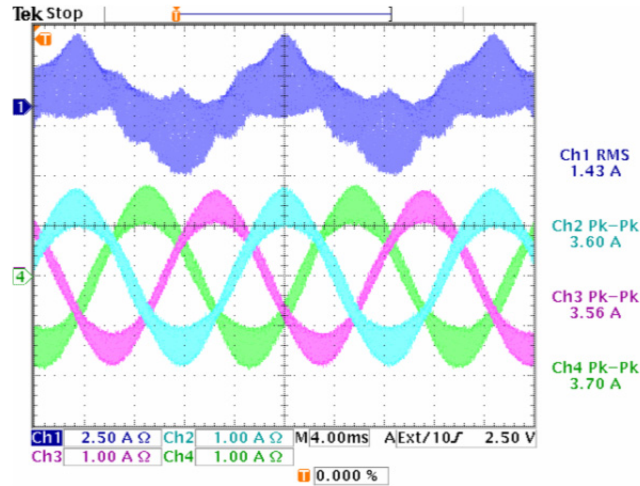

Fig. 9: Module output currents. Unfiltered single phase output current (blue) and filtered three phase output currents. T = 25 ºC.

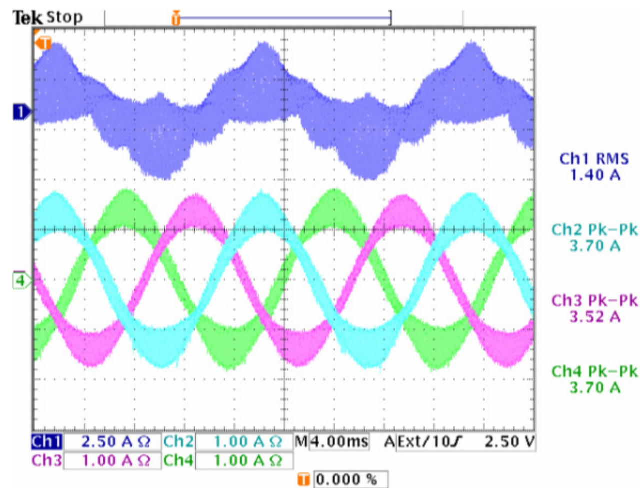

Fig. 10: Module output currents. Unfiltered single phase output current (blue) and filtered three phase output currents. T = 250 ºC.

From the temperature data in Table II and the thermal resistance of the materials in Table III, the power loss of the module can be calculated. By taking the temperature difference from

the top of the power substrate and dividing it by the total thermal resistance of the DBC and heatspreader, the power loss of the module comes out to be ~ 30W.

TABLE II: Measured Thermal Distribution (25 ºC Base plate)

Time (hours:minutes)	Control Board (ºC)	Power Substrate (ºC)	Heat-spreader (ºC)	Heatsink (ºC)
00:00	29	29	29	29
00:41	40	56	47	44

TABLE III: Thermal resistance of each layer.

			Thermal	
Material	Thickness (m)	Area (m^2)	Conductivity (W/mK)	Resistance (°C/W)
Copper 1	3.048×10^{-4}	1.54×10^{-5}	385	0.051
Aluminum Nitride	6.35×10^{-4}	2.01×10^{-5}	170	0.186
Copper2	3.048×10^{-4}	3.19×10^{-5}	385	0.025
AlSiC Baseplate	5.08×10^{-3}	1.66×10^{-4}	200	0.153
TOTAL				0.415

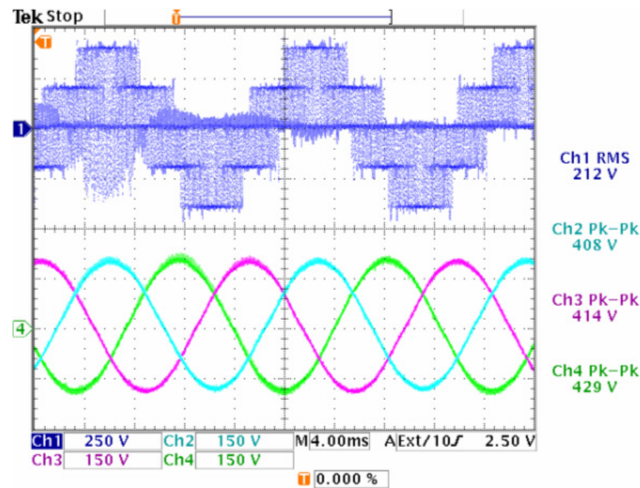

Fig. 11: Module output voltages. Unfiltered single phase output voltage (blue) and filtered three phase output voltages. T = 25 ºC.

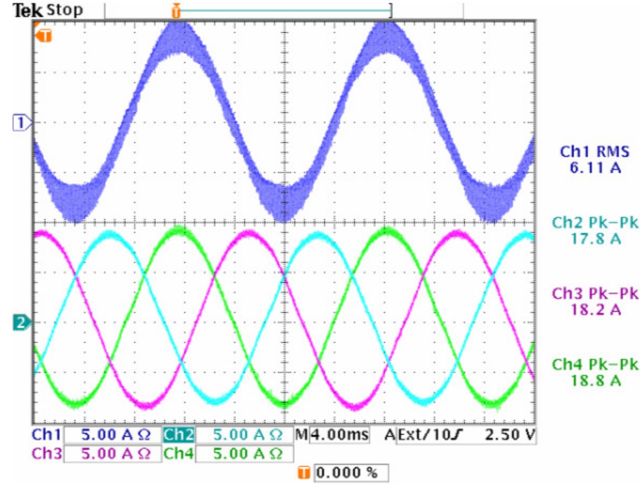

Fig. 12: Module output currents. Unfiltered single phase output current (blue) and filtered three phase output currents. T = 25 ºC.

IV. Power Testing at High temperature

The total power output of the module during this test was estimated at approximately 3.3 kW. Accurate input power measurements were not obtained during this test, but they can be calculated by adding the thermal power losses to the output power of the module. Table III summarizes the thermal distribution at different stages of the module under this test. By taking the temperature difference and the thermal resistance from the power substrate to the heatsink, the power loss in the module at 250 °C is approximately 50 watts. This leads to a module efficiency of ~98%.

TABLE III: Measured thermal distribution (250 °C base plate).

Time (hours:minutes)	Control Board (ºC)	Power Substrate (ºC)	Heat-spreader (ºC)	Heatsink (ºC)
0:00	28	28	28	28
0:28	109	130	128	127
0:58	154	196	187	185
01:41	193	250	240	234
01:48	206	270	258	250

Fig. 13 displays the three phase line to neutral load voltages after the LCL load filter (Ch. 1-blue, Ch. 2-cyan, Ch. 3-magenta) and the DC bus voltage (Ch. 4-green) supplied to the module. Fig. 14 shows the three phase currents supplied to the resistive load following the LCL filter (Ch. 1-blue, Ch. 2-cyan, Ch. 3-magenta).

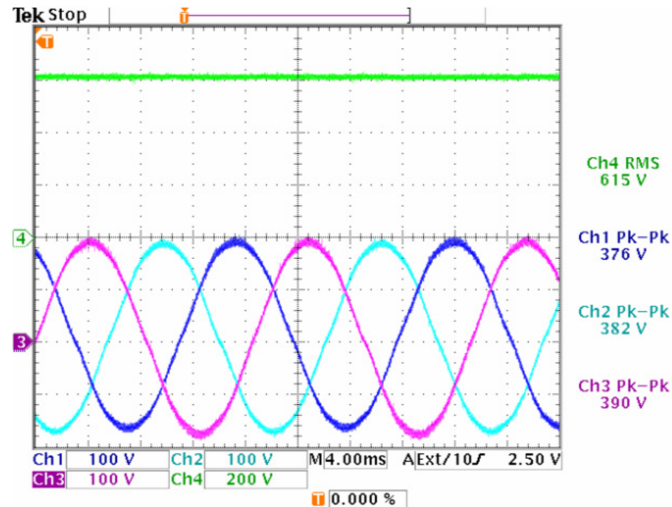

Fig. 13: Filtered three phase line to neutral voltages and DC bus voltage (green). T= 250 ºC.

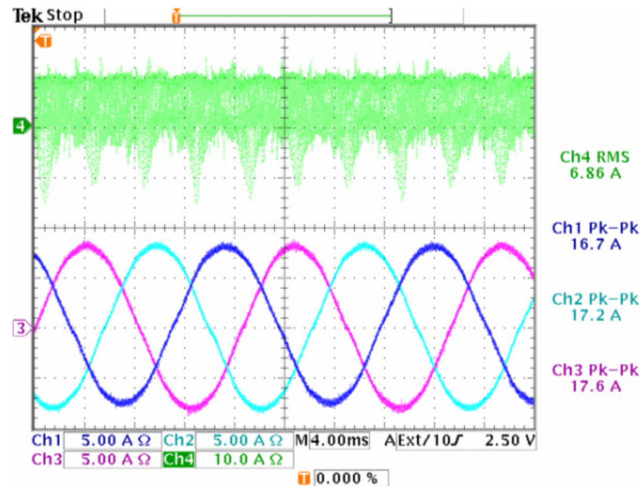

Fig. 14: Three phase filtered load currents (blue, cyan, magenta).

Finally, a Hioki power meter was used to accurately measure the input and output power of the MCPM including the filter to determine the efficiency at full power. A few adjustments to

the control software were made to increase the amplitude of the sinusoids in order to achieve full 4 kW operation. During this test, the input measured 4.02 kW while the output of the filter was measured at 3.77 kW. This results in an overall system efficiency of 93.8%. Since the module itself is about 98% efficient, further steps such as removing or optimizing the output filter can increase the system efficiency.

Conclusion

This paper was a continuation of work from the single phase inverter presented in [7]. The design, packaging, and successful testing of the three-phase high-temperature 4 kW module, continues to prove the feasibility of SiC MCPM technology. Testing of the SiC MCPM inverter module shows high potential for an increase in power density. When compared with state-of-the-art Si-based modules, a size reduction of up to 7 × may be achievable using APEI, Inc's high-temperature MCPM design approach. The biggest portion of size reduction comes from the ability that SiC offers to reduce and/or remove large cooling systems.

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CHAPTER 12

SILICON CARBIDE POWER ELECTRONICS PACKAGING

Cressler J. D., Mantooth H. A., *Extreme Environment Electronics 1st ed.*, CRC Press

Chapter 69 Silicon Carbide Power Electronics Packaging

Authors: Jared Hornberger Additional Authors: Brice McPherson, Brandon Passmore

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Significant advances in Silicon Carbide (SiC) power switch technology over the past decade are driving a technology revolution in the commercial power electronics industry. SiC is the ideal material for a power device. It has a substantially higher voltage breakdown strength compared to Si, allowing devices to be fabricated with voltage blocking layers up to an order of magnitude thinner and more heavily doped, ultimately resulting in a drastic increase in electrical conductivity and switching speed. SiC can theoretically operate as a semiconductor at temperatures up to 600°C (compared to 150-175°C for Si), has a thermal conductivity 3x higher than Si, and possesses outstanding mechanical properties [1]. If properly exploited, the extraordinary performance of these devices could result in electronic systems that are revolutionarily more efficient, smaller, and capable of being implemented in environments where conventional technology simply cannot operate.

Considerable resources on the order of 100s of millions of dollars globally have been invested towards the improvement of SiC wafer quality and the development of advanced power devices. A wide and constantly expanding selection of high performance SiC Schottky diodes, JFETs, MOSFETs, and BJTs are becoming available on the international market [2-6]. However, in order to take full advantage of these devices, similar efforts must be concentrated in the

development of power package technology specifically tailored for the performances and challenges associated with SiC. Many characteristics of must be considered when designing SiC power modules, including the increased temperature of operation, high switching frequencies, large current densities, and high blocking voltages. Notably, conventional power modules are not capable of handling the extreme switching speeds and elevated ambient and junction temperatures characteristic of SiC devices.

With a lower on resistance per unit area (when compared to Si), current densities are much higher on SiC die. Correspondingly, the thermal performance of each device at the package level becomes increasingly important as the size of the devices continues to shrink. An additional factor affecting thermal performance is that SiC substrate material technology is not as far advanced as Si. Because of device yield due to wafer defects, SiC die are currently manufactured on the order of 10 to 50 amps per device thus requiring the paralleling of many components to reach high power operation. This requires careful consideration to thermal spreading and electrical parasitics when placing die and laying out substrates. Stray electrical parasitics (particularly inductances) are a critical issue which seriously limit device switching speeds (e.g., di/dt’s and dv/dt’s), and often result in large voltage or current spikes during switching events. Furthermore, to achieve higher power densities limitations must be overcome in power packaging materials, thermal performance, assembly technologies, and peak temperature capability. It is paramount that new packaging technologies are developed and implemented in order to take advantage of the opportunity presented by the arrival of SiC power devices.

69.1 Materials for Power Electronics Packaging

A myriad of material properties are important to evaluate in the selection and design of each package component, ranging from physical (density, stiffness, yield strength), electrical (conductivity, dielectric properties, permeability), thermal (coefficient of thermal expansion (CTE), thermal conductivity, specific heat), and practicality (availability, processing methods, ease of manufacture, cost). Paramount to the selection process is not only considering the relative merits of a singular material, but analyzing how multiple material choices interact when incorporated in a system. As in any engineered product, the art of design lies in extracting the most effective tradeoff between various materials and conflicting goals (e.g. weight vs. thermal performance).

While each material property is significant, operation at extremely high temperatures exacerbate many reliability issues and concerns, particularly with the thermal properties and power dissipation. Specifically, CTE differences between bonded layers are of dominating importance. As materials expand and contract due to changes in temperature, stresses increase in areas where movement is restricted (such as a solder bond interface). Mismatches in the CTE accelerate this thermally generated stress, particularly during repeated thermal cycles, and must be addressed through the combined use of low stress geometrical features, reinforcement, and CTE matching. Accordingly, careful selection of materials with similar CTEs is often of upmost importance in the design of a power module.

Power packages must be capable of readily transferring heat (generated through conduction and transient losses in the devices, components, and conductors) from highly concentrated and geometry restricted sources towards the heat removal system (heat sink, cold plate, radiator, etc.). Thermal conductivity represents the capability of a material to conduct heat,

with larger numbers corresponding to more efficient heat dissipation. Additionally, when high transients of energy are expected, such as in pulse power applications, the density and specific heat of the material are important factors to consider. When implemented in a package, these values ultimately influence the thermal resistance of the system, conventionally identified as the die junction-to-case or die junction-to-ambient temperatures in a straightforward temperature rise per power ($^{\circ C}/_{W}$) relationship.

Reliability and heat removal concerns are further complicated by the fact that many material properties vary as the temperature changes; namely, the CTE and thermal conductivity. In general, as the temperature rises, the CTE increases and the thermal conductivity will decrease. Materials become softer and more ductile. As the temperature lowers, components are tougher and more brittle. As such, each design must carefully consider the effects of the operational environment in conjunction with the materials themselves for peak effectiveness.

69.1.1 Base Plates

Base plates are the foundation and core of a power module. They concurrently provide structural support, mounting features, and thermal spreading to the assembly. Ideally, the base plate material would exhibit a high thermal conductivity and a CTE closely matched to the bonded components (principally the power substrate). Important secondary factors include high stiffness, ease of machining, plating options, and cost. Achieving the perfect balance is often challenging; in general, the thermal conductivity and CTE for metals and alloys are antithetical. As an example, copper and aluminum have extremely high thermal conductivities but will displace greatly when heated.

An effective compromise is found in composites – solid solutions (i.e. not alloys) of two metals, a metal and a ceramic, or a metal and an organic compound. These materials, identified

as Metal Matrix Composites (MMCs), are extremely effective base plate materials, offering an excellent compromise between competing properties, albeit at a higher cost. These materials may be formed in a variety of manners, including powder sintering, casting, and diffusion bonded foils. Conductivities and CTE values may be "tailored" to match the corresponding system by varying the composition of each material. It is important for the designer to be cognizant of the type of forming process each manufacturer employs, as some forms (notably rolled foils and carbon fiber based sheets) exhibit anisotropic material properties in which the in-plane material characteristics differs from the vertical characteristics. Suitable base plate materials for high temperature power modules are identified in Table 69.1 [7-9].

TABLE 69.1: Base Plate Materials and Their Thermal Mechanical Properties

Base Plate Material	Composition	CTE (ppm/°C)	Thermal Conductivity (w/m K)	Density (g/cm³)	Specific Heat (/kg.k)	Young's Modulus (MPa)	Yield Strength (MPa)
Copper (Cu)	100Cu	17.8	398	8.9	385	128,000	210
Aluminum (AL)	100AL	26.4	230	2.7	397	70,000	50
Copper tungsten (CuW)	10Cu/90W	6.51	150	17.3	163	n/a	483
	15Cu/85W	7.36	162	16.45	175	n/a	517
	20Cu/80W	8.21	175	15.68	188	n/a	662
	25Cu/75W	9.06	186	14.98	201	n/a	655
Copper moly (CuMo)	85Mo/15Cu	6.8	165	10.01	n/a	274,000	n/a
	80Mo/20Cu	7.2	175	9.94	n/a	274,000	n/a
	75Mo/25Cu	7.8	185	9.87	n/a	274,000	n/a
	65Mo/35Cu	9	205	9.74	n/a	274,000	n/a
	60Mo/40Cu	9.5	215	9.68	n/a	274,000	n/a
Copper graphite (CuGr)	Not listed	7(X,Y) 16(Z)	285–300(X,Y) 210(Z)	6.07	433	75,842	84
Aluminum graphite (Carb AI™)	CarbAI-N	7	200(X,Y) 350–488(Z)	2.1	750	12,000	40
	CarbAI-G	2	150(X–Y) 350(Z)	1.75	690	12,000	40
Aluminum graphite (AIGr)	Not listed	4(X,Y) 24(Z)	220–230(X,Y) 120(Z)	24	852	98,595	110
Aluminum silicon carbide (AISiC)	37AI/63SiC	8	200	3.01	741	188,000	488
	45AI/55SiC	9.77	200	2.96	786	167,000	450
	63AI/37SiC	10.9	180	2.89	808	167,000	471
Aluminum beryllium (AIBeMet)	38AI/62Be	13.9	212	2.1	1506	196,500	226
	60AI/40Be	16	210	2.28	1280	158,500	207
Beryllium beryllium oxide (BeBeO)	80Be/20BeBeO	8.7	210	2.06	n/a	303,000	n/a

Base plate geometry must be thoroughly analyzed in the design process to achieve an effective performance. The base plate is the heaviest element in a module, often comprising 50-75% of the overall mass. It expresses both a positive (thermal spreading) and negative (due to the thickness) influence on the thermal performance. In addition, the geometry of the plate will have a significant effect on thermal-mechanical displacement. As an example, thin and large plates will displace substantially more than small, thick plates when heated. A careful balance must be achieved such that the thermal, mechanical, and weight requirements of the module are met within reason.

Figure 69.1 [10] displays two design surfaces (thermal and mechanical) extracted through finite element analysis (FEA) simulation for a power module design incorporating a CuMo base plate. These results represent the case of sixteen power devices dissipating a total power of 500W mounted on a power substrate soldered to the base plate, with individual simulations performed as the geometry (side length and thickness) of the plate is varied. As shown, the thermal performance is heavily driven by the area of the plate and increases with thickness. The negative thermal effect of thickness is diminished as the area increases, but the displacement will correspondingly rise. It should be noted that the specific shape of these curves will greatly depend on the characteristics of each individual system and must be analyzed in detail for each new power module design. Performance curves such as these are invaluable for the designer to make effective and informed choices for both the base plate material and final geometry.

69.1.2 Substrates

Power substrates are an essential element in a power module, providing electrical interconnection, high voltage isolation, low impedance current paths, and heat spreading. An ideal power substrate would offer a close CTE match to the attached devices (4-6 $^{ppm}/_{°C}$),

efficient thermal performance, high fracture toughness, and high flexural strength. High temperatures limit the available technologies, as few isolating materials outside of ceramics offer acceptable dielectric properties alongside a high thermal conductivity.

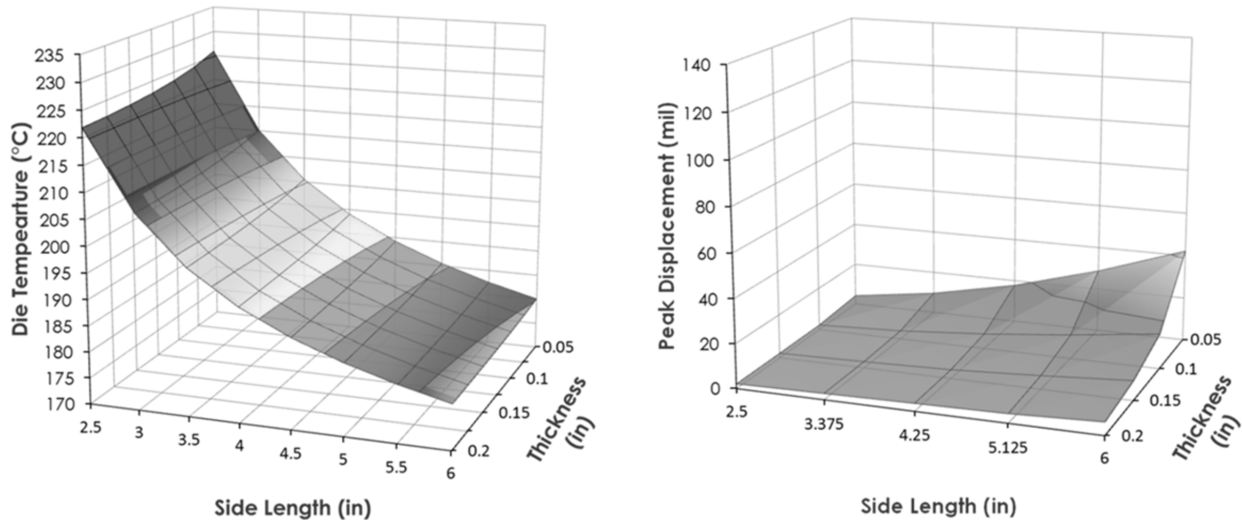

Figure 69.1 Three-dimensional surface graphs from simulation of a power module depicting the trade-off of base plate geometry (length and thickness) vs. the resultant die junction temperature and base plate displacement. (From McPherson, B. et al., High temperature silicon carbide power modules for high performance systems, in *IMAPS International Conference on High Temperature Electronics Network (HiTEN 2011)*, St. Catherine's College, Oxford, England, July 18–20, 2011).

Power substrates consist of a three layer structure, comprised of a ceramic substrate sandwiched between two thick metal sheets. Selecting materials for these elements requires a tradeoff among material properties, geometrical constraints, processing techniques, and pricing to meet the specific requirements of a module. Due to the CTE difference between the metal and ceramic, the thickness of the bonded metal, and the brittleness of ceramics, thermal stress is a daunting and prevalent issue with all power substrate choices.

Four ceramic materials are typically utilized in power packaging, including Alumina (Al_2O_3), Beryllium Oxide (BeO), Aluminum Nitride (AlN), and Silicon Nitride (Si_3N_4). Characteristics of each are compared in Table 69.2. [11-14]. Alumina is the most widely used

and least expensive material, but has the lowest thermal conductivity by more than an order of magnitude compared to BeO and is often a poor choice for high power systems, particularly at elevated temperatures. Beryllium oxide displays a compellingly high thermal conductivity; however, this can be misleading as the thermal conductivity of BeO is heavily temperature dependent. High temperature operation will largely eliminate the thermal margin of BeO in comparison to competing materials. Additionally, dust particles from machining BeO present a health hazard, which requires special processing procedures during fabrication and machining (increasing cost). Aluminum nitride possesses a high thermal conductivity and an excellent CTE, with the drawback of a poor mechanical strength and difficulty in bonding. Silicon nitride has a moderate thermal conductivity but offers outstanding mechanical properties which can be exploited to compensate for the conductivity differences. It is clear to see that there is no perfect solution for a power substrate, and the designer must choose which technology best suits a given application.

Table 69.2 Properties of Ceramic Substrate Material for Power Electronics Packaging

Ceramic Substrate Material	CTE (ppm/°C)	Thermal Conductivity (W/m K)	Dielectric Strength (kv/mm)	Fracture Toughness (MPa $m^{1/2}$)	Flexural Strength (MPa)	Tensile Strength (MPa)
Alumina 96% (AI_2O_3)	60	24	12	3.5	317	127
Alumina 99% (AI_2O_3)	7.2	33	12	4.0	345	207
Aluminum nitride (AIN)	4.5	170	15	2.6	360	310
Beryllium oxide (BeO)	7.0	270	12	4.0	250	230
Silicon nitride (Si_3N_4)	2.7	60	10	5.0	850	17

Power electronic systems process large amounts of current at very high voltages. The metal type and geometry of the power substrate must be selected such that current paths exhibit low impedances while traces are spaced to provide adequate isolation. A variety of methods are present for metallizing ceramics, ranging from thin film deposition, printed thick films, plated metals, or bonded metal sheets. Thin and thick film processes provide metal thicknesses less than 25 µm, which are not conducive for carrying high currents. However, they can provide a suitable

seed layer for a plate up process adding additional thickness (usually up to 200 μm). Metal sheets may be bonded directly or brazed to the ceramic, and may reach thicknesses >400 μm. Metal thickness has an impact on the stress of the substrate, as well as minimum etched trace resolution.

Direct Bond Copper (DBC) and Direct Bond Aluminum (DBA) are formed by pressing and heating copper or aluminum foils into Al_2O_3 or BeO which is carried out in a slightly oxidizing environment to temperatures just below the melting temperature of the metal [15]. A metal-oxygen eutectic is formed at the interface, creating a strong bond between the metal oxide and the ceramic oxide. This process may be performed on AlN ceramics by first oxidizing the ceramic surface to form a bondable layer for the copper oxide [16].

In comparison to DBA, DBC has the advantage of a lower resistivity ($1.7e^{-6}$ vs $2.65e^{-6}$ Ω-cm), higher thermal conductivity (390 vs. 240 W/m·K), and ease of etching. DBA exhibits the distinguishing factors of improved thermal cycling reliability, reduced weight (2.70 vs 8.94 g/cm^3), and the potential for a mono-material wire bond interface (Al-Al) which limits high-temperature metallurgical interfacial issues. The bond between the aluminum oxide and ceramic is much stronger than the copper oxide bond and aluminum is softer and has a greater resistance to strain hardening. As a result, DBA has superior thermal cycling performance and high-temperature reliability as compared to DBC [17-18].

For ceramics where direct bonding is not practical, such as Si_3N_4, an Active Metal Brazing (AMB) process is employed. This process allows a metal to be bonded to a ceramic without a deposited seed layer. It is performed by adding a small percentage of active metal powder (usually titanium or zirconium) to a brazing paste (generally CuSil, a 72% copper 28% silver alloy). The active elements readily form a reaction layer with the ceramic when the braze

alloy melts, creating an exceptionally strong bond between the metal foil and ceramic. Copper is the standard metal due to the high processing temperature of this process (well above the melting point of aluminum). These substrates require a high initial tooling cost (due to the brazing process), and have special processing considerations. In addition, the reaction layer is very difficult to etch. Accordingly, the braze paste is pattern printed on the ceramic such that there is no reaction layer in the regions where trace isolation is required. The metal foil is then etched to match this pattern. This increases the cost of AMB substrates for low volumes or prototyping, as custom tooling is required for each specific design.

There are numerous reliability benefits to utilizing an active braze in comparison to a direct bond. The strength of the brazed interface is substantially stronger than a direct bond. The braze layer forms a bond line which acts as a stress buffer between the ceramic and metal. Additionally, the alloy forms a natural fillet at the edges of the metal, creating a smooth transition instead of an abrupt edge. Substrate manufacturers often overprint the braze paste, forming a “foot” at the edge of the metal, further buffering the stress.

The bare copper or aluminum surfaces are usually plated with nickel and/or gold in order to protect the surfaces from oxidation (in the case of copper) and to promote solder adhesion and wetting. Copper surfaces may be directly plated through either electroless or electrolytic processes. The nickel layer acts as a diffusion barrier, inhibiting the migration of copper to the surface (where it will oxidize) or to the capping gold layer (where it will alloy with the gold and oxidize). Aluminum generally requires preparation through zincating prior to plating operations, during which the surface oxides are stripped from aluminum and replaced with a protective layer of zinc through a chemical reaction. The zinc is then absorbed in the succeeding bath and replaced by nickel.

Care must be taken in selecting the nickel plating chemistry (phosphorous, boron, sulfur, etc.) and thickness, depending on the maximum service temperature. In temperatures in excess of 350°C for long periods of time, the effectiveness of the nickel layer diminishes, allowing accelerated diffusion of copper [19]. In the case of nickel phosphide, the phosphorous has been shown to separate, diffuse, and degrade the upper surface, potentially contaminating interconnects and bond quality. Energy Dispersive X-ray (EDX) analysis was performed on the surface of a nickel phosphide (6-8%) plated AlN substrate before and after 400°C annealing [20]. EDX analysis outlines the electrical composition of a thin layer of a surface; the peaks represent the concentration of detected elements and the x-axis indicates acceleration voltage in kV (peaks at higher acceleration voltages represent elements further in depth). The resultant EDX plots are presented in Figures 69.2 (before) & 69.3 (after thermal exposure). They reveal the concentration of the surface phosphorous more than doubling. If the substrate must be placed in service at these temperatures, a more stable nickel chemistry (nickel boron, etc.) or a different diffusion barrier must be considered.

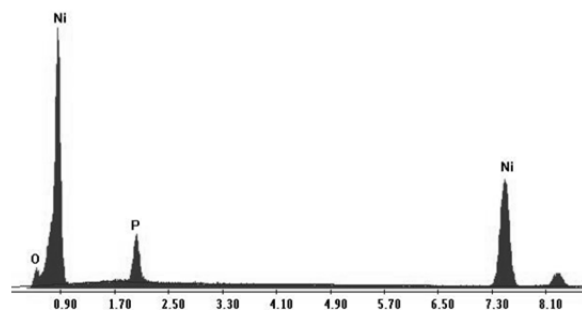

Figure 69.2 EDX analysis of a DBC substrate before thermal cycling. (From Hornberger, J. et al., High-temperature integration of silicon carbide (SiC) and silicon-on-insulator (SOI) electronics in multichip power modules (MCPMs), in *11th European Conference on Power Electronics and Applications (EPE2005)*, Dresden, Germany, September 2005).

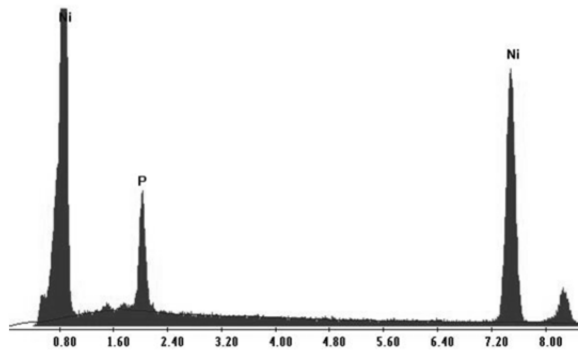

Figure 69.3 EDX analysis of a DBC substrate after 400°C thermal cycling. (From Hornberger, J. et al., High-temperature integration of silicon carbide (SiC) and silicon-on-insulator (SOI) electronics in multichip power modules (MCPMs), in *11th European Conference on Power Electronics and Applications (EPE2005)*, Dresden, Germany, September 2005).

Selecting the best substrate for a given application is crucial for an advanced power module. While DBC substrates are quite effective at high temperature dwells, they are known to have reliability issues when subjected to repeated thermal cycling, particularly when brought to lower temperatures (-25 to -55°C). DBC failures encountered after 100 thermal cycles (-50 to 250°C) are illustrated in Figure 69.4 Similar results and failure mechanisms of thermal cycled DBC have been reported in literature [21]. For some applications, this limitation is acceptable (if the module will only see long isothermal dwells); however many industries, such as automotive and aerospace, will have converters which must withstand a wide range of temperatures while in operation. For these high reliability systems, the preference is to use DBA or AMB substrates, which can withstand more aggressive thermal cycling environments. DBA and AMB substrates were exposed to the same thermal cycle as the DBC (-50 to 250°C) and at this point in the test have survived >500 cycles without any failures.

In addition to extreme environment reliability, the thermal performance of the substrates must be evaluated. The varying thermal conductivities of copper, aluminum and the multiple ceramic choices must be considered during the design process. A thorough understanding of the

materials themselves is essential in accurately comparing the materials. A salient example of this is found when comparing Si_3N_4 to AlN. On paper, AlN has a superior thermal conductivity which implies superior thermal performance. In practice, AlN has poor strength and must be formed in relatively thick 0.64mm sheets to withstand the stress of the bonding process. On the other hand, Si_3N_4 is exceptionally strong and may be formed in sheets half the thickness (0.32mm). These substrates are also capable of handling thicker layers of copper. Figure 69.5 displays the effects of ceramic and metal thickness of the die temperature of an example system. Metal thicknesses are listed based on available manufacturer configurations. As shown, nearly analogous thermal performance (and all of the mechanical benefits) can be obtained with Si_3N_4 if the materials are thoughtfully considered.

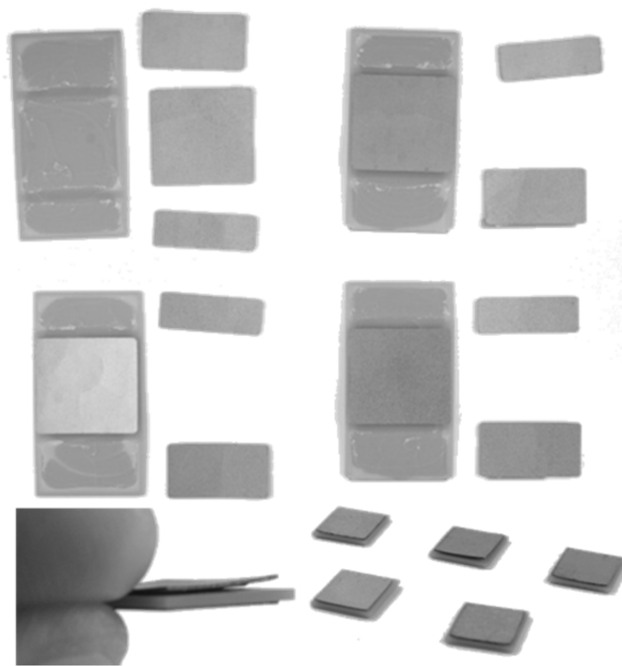

Figure 69.4 Direct bond copper (DBC) substrates showing metal delamination after being thermal cycled 100 times from −50°C to 250°C.

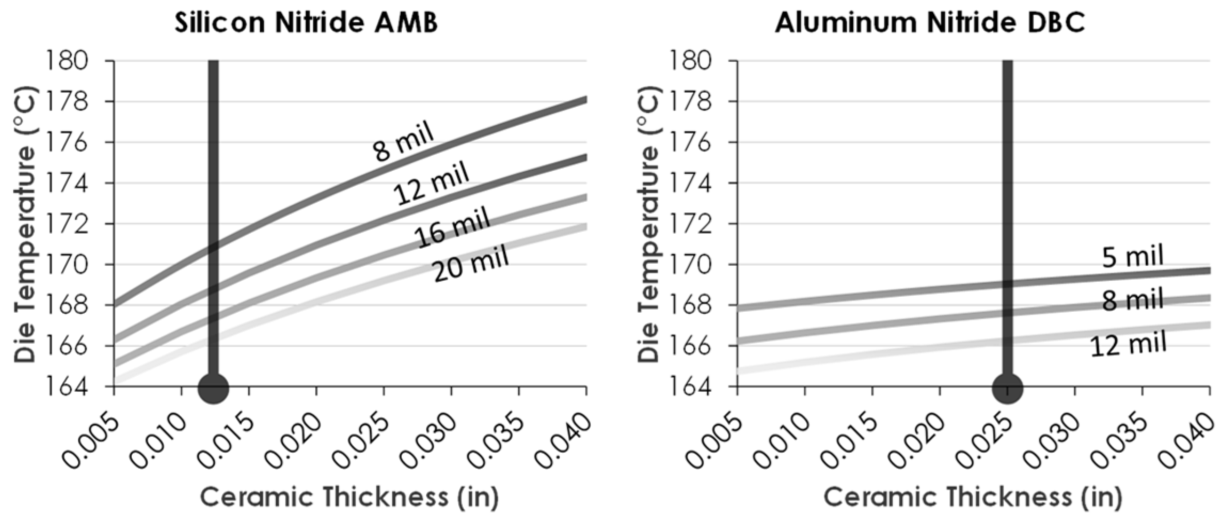

Figure 69.5 Graphs from an example power electronics system demonstrating the effects of ceramic and metal thickness on die temperature. The vertical line represents the commonly available thickness for AlN and Si3N4 substrate material.

Identifying an optimal metal thickness is a tradeoff between thermal and electrical performance and stress (thicker layers are less reliable). Figure 69.6 presents the thermal effect of the substrate thickness for common ceramic thicknesses, while Figure 69.7 depicts electrical resistance of varying trace geometries. As the metal thickness increases, thermal performance improves and electrical resistance reduces. Each characteristic exhibits diminishing returns (the die temperature levels out and the resistance curves converge). It is the role of the package designer to utilize curves such as these as a tool to make informed and effective design decisions.

69.1.3 Die & substrate Attach

Power devices are predominately vertical (i.e. power flows through the entire area of the die). The electrical connection from the lower die contact to the power substrate is a critical factor in the performance and reliability of the system. In comparison to the substrate and base plate (which have ample room for lateral thermal spreading), the die attach is constrained to the geometry of the device. Hence, the die attach has a pronounced influence on the transfer of electrical and thermal energy.

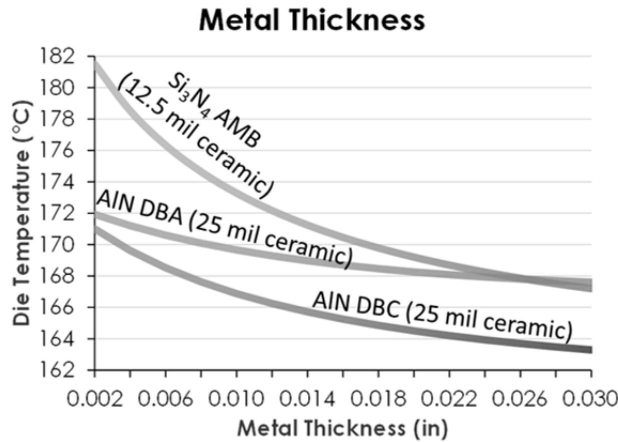

Figure 69.6 Graph from an example power electronics system demonstrating the thermal effect of the substrate thickness for common ceramic thicknesses.

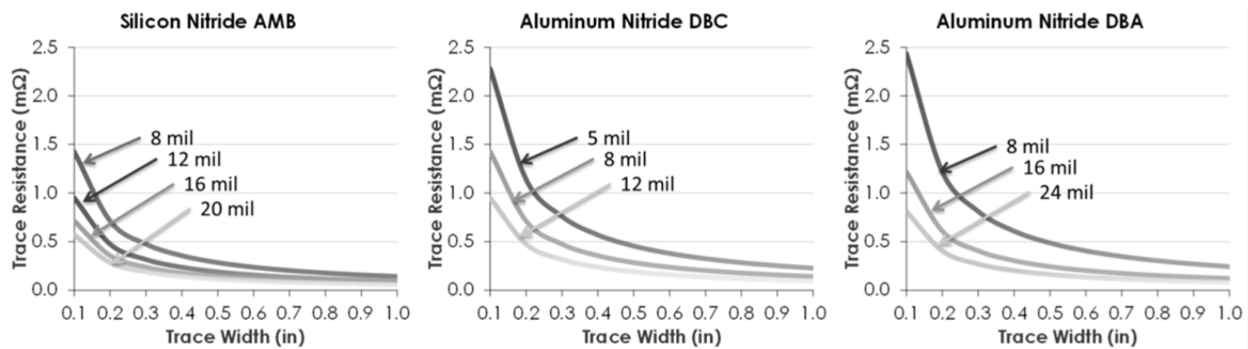

Figure 69.7 Electrical resistance vs. metal trace width for common substrate metal thicknesses.

Traditionally, electrical and thermal connections in power package assemblies are formed through soldering and brazing. Soldering and brazing alloys consist of two or more metals that alloy to form a homogenous mixture with a lower melting temperature than the constituent elements. One of the most common examples is the combination of 37% lead (melting point 328°C) and 63% tin (232°C), resulting in a melting temperature of 183°C. This composition is referred to as eutectic, which means that the melting point occurs exactly at the indicated temperature and the melting temperature is the lowest possible combination of the alloying elements. Non-eutectic alloys experience a transition region between solid and liquid (called the plastic region) where it exhibits traits of both. Table 69.3 [22] presents a list of many common

alloys used in metal joining applications. While functionally similar, solders and brazes are primarily distinguished by the materials utilized and processing temperatures required. Brazes typically begin at melting temperatures greater than 450°C, require more aggressive flux, and are rarely eutectic outside of the gold based systems.

Table 69.3 Solder Alloys and Their Mechanical Properties

Solder Alloy	Solidus (°C)	Liquidus (°C)	Density (g/c_m^3)	Thermal Conductivity (W/m K)	CTE (ppm/K)	Electrical Conductivity (%IACS)
Pb60, In40	197	231	9.3	19	26	5.2
Sn91, Zn9	199	199	7.27	61	—	15.0
Sn96.5, Ag3.5	221	221	7.5	33	30	16.0
Sn95, Sb5	235	240	7.25	28	31	11.9
Pb75, In25	240	260	9.97	18	26	4.6
Pb81, In19	260	275	10.27	17	27	4.5
Sn10, Pb88, Ag2	267	290	10.75	27	29	8.5
Sn10, Pb90	275	302	10.75	25	29	8.9
Au80, Sn20	280	280	14.51	57	16	—
Sn5, Pb92.5, Ag2.5	287	296	11.02	26	29	8.6
Sn2, Pb5.5, Ag2.5	299	304	11.2	—	—	—
Pb92.5, 5In, 2.5Ag	300	310	11.02	25	25	5.5
Sn5, Pb95	308	312	11.06	23	30	8.8
Pb97.5, Ag1.5, Sn1	309	309	11.28	23	30	6.0
Au88, Ge12	356	356	14.67	44	13	—
Au96.8, Si3.2	363	363	15.4	27	12	—
Au75, In25	451	465	13.7	—	—	—
Sn100	232	232	7.28	73	24	15.6
Pb100	327	327	11.35	35.0	29.0	7.9
Au100	1064	1064	19.3	318	14	73.4

SiC power devices have the potential to operate at extremely high junction temperatures (250°C and greater) and require higher temperature attaches than conventional 63Sn/37Pb. The high concentration of heat generated in the devices (due to the higher power density of SiC) requires a solder alloy that is capable of efficiently transferring this heat to the substrate. Care must be taken in selecting an alloy that has an acceptably high reflow temperature, high thermal

conductivity, high bond strength, and metallurgical compatibility with the soldering surfaces (to prevent gold leaching, for example).

Solders often have relatively low thermal conductivities which can be heavily reduced at high temperatures especially as the solder approaches its melting temperature. This must be taken into account in any high temperature design. Figure 69.8 presents a sweep of die attach thermal conductivities performed during the design of a power module. Two high temperature solders (95Pb/5Sn and 80Au/20Sn) are highlighted, with the width of the region representing the range of the thermal conductivity from room temperature (upper limit of the region) to 250°C (lower limit). As shown, the die temperature is heavily driven by the attach conductivity at lower values. Interestingly, as the conductivity increases, the resulting die temperature experiences diminishing returns. Essentially, while significant thermal gains can be achieved by replacing a 95Pb/5Sn die attach with 80Au/20Sn at high temperatures, replacing the 80Au/20Sn alloy with a higher thermal conductivity alternative will not bring the same thermal benefits. It should be noted that the shape of this curve (including the rate of change and the location of the 'knee') is heavily driven by the rest of the system and is important to analyze for each particular design or configuration (some systems will greatly benefit from high conductivity attaches while some will show negligible differences).

While soft solders are ideal for temperature cycling due to their ability to absorb stress, their strength vastly diminishes at elevated temperatures. The Materials Information Society suggests that solder joints under constant loading should not have a maximum operating temperature greater than 70% of the solidus temperature (in Kelvin) of the solder [23]. Practical soft alloys that fit these requirements are limited. As such, more rugged hard solder options which have demonstrated improved high temperature reliability (such as 80Au/20Sn and

88Au/12Ge) may be required. Gold based solders and brazes have long been employed in the electronics industry as reliable and effective die attaches.

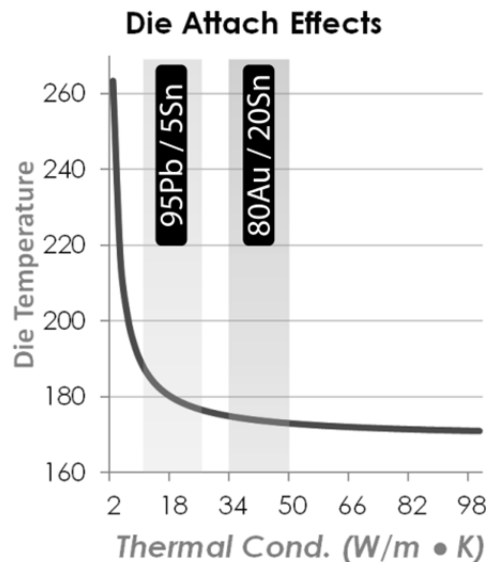

Figure 69.8 Power module simulations showing the die junction temperature vs. die attach thermal conductivity with the thermal conductivity range of two solder alloys highlighted.

Higher temperature attaches necessitate high temperature attach processes. Metallurgical bond quality is of paramount significance in a high power density electronic module. Most metal surfaces (particularly Al and Ni) develop a thin, native oxide which must be removed prior to soldering operations to promote adhesion. Conventionally, this is accomplished with flux: a reducing and cleaning agent that prepares and protects metal surfaces during soldering. While effective, flux has many issues for the large area attaches encountered in a power module. As the flux activates and boils, gasses are generated between the faying surfaces. The larger the bond, the more difficult it is for these gasses to escape. When the joining alloy solidifies, these trapped gasses will leave voids, which may substantially interfere with the thermal performance of the system. Common void fractions in industry for solder bonds using flux are 10-25% (according to classifications in the IPC-A-610D standard [24]). Flux also leaves residues that must be cleaned,

may burn or corrode delicate surfaces, cause issues for wire bonds, often outgases, and is altogether not preferred for the assembly of advanced power modules.

Flux free assembly of power modules may be performed in a vacuum/pressure reflow oven. Surfaces and solder preforms are prepared prior to assembly chemically with a mild acid (if necessary) and through heavy plasma cleaning (Ar and O_2). Additional cleaning occurs in the oven itself through the use of a dry reducing gas (hydrogen or formic acid) and heat. The gas will react with and remove surface oxides, which is then flushed from the system prior to reaching the joining temperature. Under high vacuum, the surface tension of the molten solder alloy promotes wetting and flow between surfaces, creating extremely high quality bonds with low void fractions (1-5%). Figure 69.9 shows a scanning acoustic microscope (SAM) image of a substrate attached that used 95Pb 5Sn solder paste with flux (left) and the same substrate attached using a preform of the same alloy reflowed in a vacuum oven using no flux (right). The images show ~20% voiding in the application with flux and little or no voiding in the flux free sample.

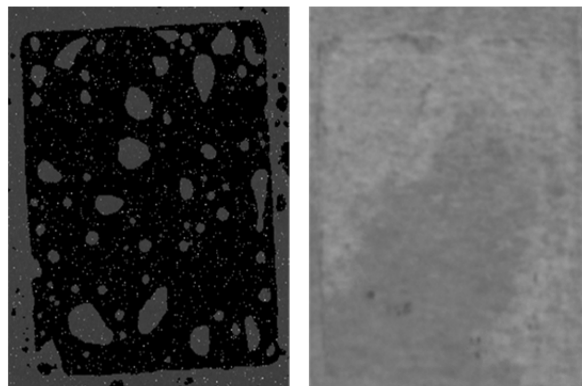

Figure 69.9 Scanning acoustic microscope images of the solder interface between a power substrate and package base. The sample on the left shows ~20% voiding when performing the attach with flux compared little to no voiding in the figure on the right when performing the attach without flux in a vacuum reflow oven.

Temperature ramp rates, isothermal dwells, gas type, gas pressure, and vacuum level are individually controlled in the vacuum/pressure reflow profile. This allows process engineers to develop precision solder reflow processes to carefully account for the requirements of each attach. In the design process, monitoring thermocouples are placed in critical positions to measure the actual temperature on the components. These measurements provide valuable data such that the temperature profile can be adjusted to account for the thermal mass of the assembly, resulting in a reduction in the overall process time. Once the solder has melted and subsequently solidified and the module begins to cool, stress begins to build up in each layer. Accordingly, the method in which the assembly is cooled becomes significant, particularly for high temperature attaches. Allowing parts to freely cool may cause distortion and fracture of brittle materials. A superior alternative is to control the cool down such that the assembly reaches room temperature gradually to allow for the stresses to equalize.

One of the major limitations of soldering and brazing is the need for a hierarchy: multiple attaches must either be formed simultaneously or in subsequent operations with lower melting temperature alloys than the previous process which is also known as step soldering. Due to the lack of available high temperature solder options, this can be a major issue in complicated assemblies. Two promising alternatives are found in solid state and transient liquid phase (TLP) diffusion processes [25]. The concept behind each is similar in that the end goal is the creation of a very high temperature bond with a relatively low temperature process.

Diffusion bonding is performed by encouraging solid state diffusion of soluble materials (often the same material) through the use of temperature and pressure. Many metals (notably gold) will readily self-diffuse, joining together without the use of a filler material. This is best performed with high pressure and moderate temperatures on relatively thick layers of each

material. The difficulty when adapting this to electronic devices lies in the challenge of safely applying the pressure without damaging the device and dealing with the extremely thin layer of metal on the die backside. Stress is also a concern for diffusion bonds, as there is no bond line to buffer thermally generated stresses.

TLP bonding is an advanced process formulated in a reaction to the challenges of traditional diffusion attaches. This process comprises of the melting of a material of low melting temperature (tin, indium, solder alloy, etc.) in intimate contact with compatible high temperature surfaces (silver, nickel, gold, copper, etc.) which are soluble in the molten precursor. A concentration gradient is present between the materials, which drives a diffusion reaction as the low temperature melt dissolves into the base metal surface. As the dissolution continues the composition of the filler begins to shift. If the materials are selected carefully (based on their phase diagrams) and the proper thermal conditions are met, the composition will shift towards a region of the phase diagram where the alloy solidifies. The well-known metal system of gold and tin is used as an example of this process. If a eutectic composition (representing the lowest melting temperature) of 80Au/20Sn alloy is melted in contact with a heavy gold surface, the composition will shift towards higher gold concentrations as gold enters the melt and tin diffuses into the gold, ultimately resulting in solidification. As shown in the phase diagram in Figure 69.10, the phase line becomes very steep as the gold concentration increases (changing approximately 40°C for every percent reduction in tin).

A table of metals that are compatible with this process can be found in [26]. TLP bonding is significantly faster and requires less pressure than solid state diffusion bonding due to the liquid phase accelerating the process. Many others have demonstrated the viability of processing at low temperatures using TLP bonding for high temperature operation including the following

alloys; Ag-Sn [27], Zn-Al [28], Ag-In [29], and Au/In-Sn/Cu & Cu/In-Sn/Cu [30]. The difficulty in adapting this process for a bare die is similar to traditional diffusion bonding in that typical metallization thicknesses on the device are very thin and processing times (while accelerated from solid state diffusion bonding) are long in comparison to conventional soldering.

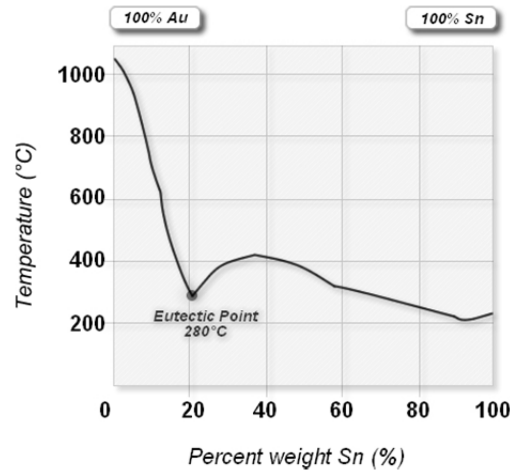

Figure 69.10 Phase diagram of gold-tin alloy showing 80/20 Au/Sn eutectic point.

69.2 Thermal Considerations and Modeling

One of the biggest challenges in any power electronics system, especially in high temperature power electronics, is the removal of heat generated from the semiconductor device's conduction and switching losses. The temperature that a device reaches while under operation depends on the thermal resistance of the package and the power loss in the device. Equation 69.1 demonstrates the calculation of the temperature rise (ΔT) of the device junction temperature (T_j) over the ambient temperature (T_a) when the thermal resistance (R_{th}) and the power loss (Q) of the system are known.

$$\Delta T = R_{th} \cdot Q \qquad \text{where } \Delta T = T_j - T_a \qquad \text{Eq. 69.1}$$

The thermal resistance of the package is determined by summing the thermal resistance of each individual material in the thermal conduction path. The thermal resistance of a material

due to conduction can be found from Equation 69.2 where t is the thickness (m), k is the thermal conductivity ($^{W}/_{m\cdot K}$), and A is the effective cross-sectional contact area (m^2)

$$R_{th} = \frac{t}{kA} \qquad \text{Eq. 69.2}$$

These equations show that paramount to the performance of a power module, is an optimized and efficient thermal path from the heat generating components (power devices, resistors, conductor losses, etc.) to the heat removal system (heat sinks, cold plates, etc.). Minimizing the thermal resistances encountered along the path has numerous key advantages; most notably achieving higher power densities by allowing for more power to be processed and reducing the requirements and the corresponding size of the heat removal systems.

For a multilayered structure, the thermal resistance is analytically modeled as a network of resistors corresponding to each layer. The channels for each heat source are considered to be parallel "legs" under the assumption that the thermal paths are not overlapping. Consequently, the thermal path for each leg is the summation of the thermal resistance of each layer and interface encountered, as described in Equation 69.3. As the heat travels along the path, it will spread in every direction, and thus the effective thermal contact area expands along the path. This change in area is determined by the angle of thermal spreading (α_a). Equation 69.4 and the length (L_2) of the thermal interface after spreading, Equation 69.5. L_1 represents the contact length entering each layer, while L_2 is the length at the exit after thermal spreading, The angle of thermal spreading is a function of the thermal conductivities of the two materials in contact, k_1 represents the thermal conductivity of the first material while k_2 is the thermal conductivity of the second material, t_a is the thickness of the material where thermal spreading is taking place. The concept of thermal spreading, depicted in Figure 69.11, plays a major factor in the overall thermal resistance of a power module package [11, 31].

$$R_{th-total} = \Sigma_{layers}\left(\frac{t_{layer}}{k_{layer} \cdot A_{layer}}\right) \qquad \text{Eq. 69.3}$$

$\alpha_a = \tan^{-1}(k_1/k_2)$ *Heat Spreading angle* Eq. 69.4

$L_2 = 2 \cdot t_a \tan(\alpha_a) + L_1$ *Length of Thermal Effect* Eq. 69.5

Inspection of these relationships reveals the following methods to reduce the thermal resistance: (1) minimizing layer thicknesses, (2) increasing thermal conductivity of contributing layers, and (3) increasing the effective contact area.

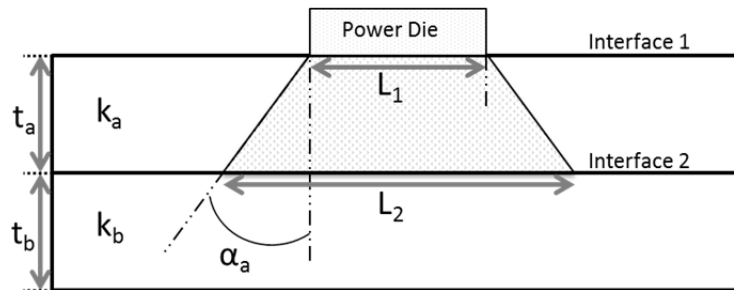

Figure 69.11 Pictorial view of thermal spreading through layered materials.

The effects of contact area are significant; as the thermal resistance equation depicts, the area is amplified by the thermal conductivity of each layer. Hence, a scaled exponential relationship exists between the contact lengths and the resulting thermal resistance. To further illustrate this point, a concept structure was analyzed, the specifics of this package stack are as follows: 2 mil thick 95Pb/5Sn die attach, 12 mil thick Cu doubled sided DBC substrate with 25 mil thick AlN ceramic, 2 mil thick 95Pb/5Sn substrate attach, and 200 mil thick copper-moly (80/20) MMC base plate. Each material was modeled at 150°C with temperature dependent thermal conductivities. A parametric sweep of this system was performed, where the length and width of the power die were increased from 0.02 mm to 0.2 m. The results are presented in Figure 69.12 [32]. The plot reveals that the size of the power die itself has a profound effect on

the thermal path, particularly at smaller sizes. As described by this surface, the thermal resistance will be optimal at or after the 'knee' of the curve, which occurs at approximately 7.5 mm per side.

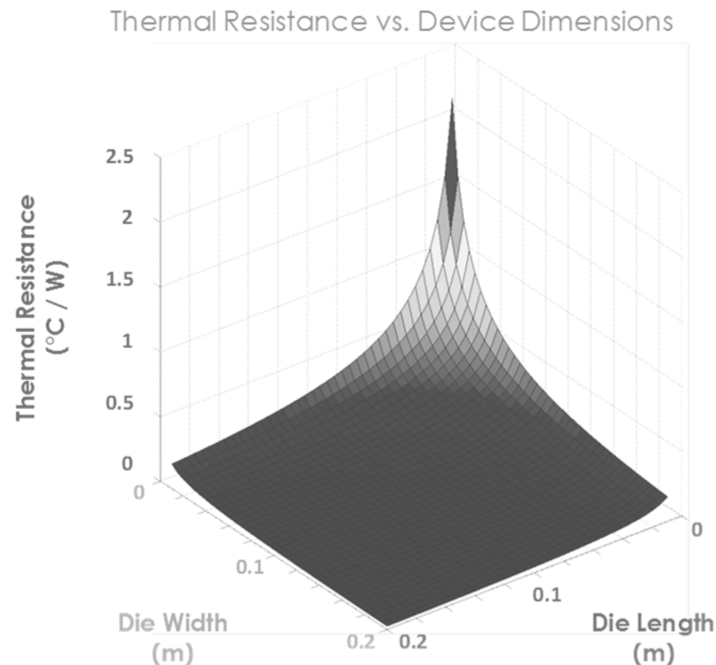

Figure 69.12 3-D graph of the simulated effect that device area has on the thermal resistance of a package. (From McPherson, B. et al., Packaging of high temperature 50 kW SiC motor drive modules for hybrid-electric vehicles, IMAPS 2009, San Jose, CA, pp. 663–670, November 2009).

Figure 69.13 [33] shows an image of a multi-chip power electronic package and the fundamental layers to take into account for thermal evaluation. The layers include die attach, upper substrate metal, substrate dielectric, lower substrate metal, substrate attach, and the base plate / heat spreader. A hand calculation using the thermal spreading equations could be performed to get a rough idea of thermal resistance, however when trying to take advantage of the properties of SiC (i.e. high temperature operation) a more accurate estimate of the system would be ideal to maximize junction temperature without exceeding the device limits. In order to have a more accurate estimation, thermal modeling can be performed with finite element analyses (FEA) software for heat transfer through materials and computational fluid dynamics

(CFD) software for air flow heat transfer in and around electronic packages. Examples of FEA and CFD software include ANSYS, FloTHERM®, SolidWorks, COMSOL, and many others.

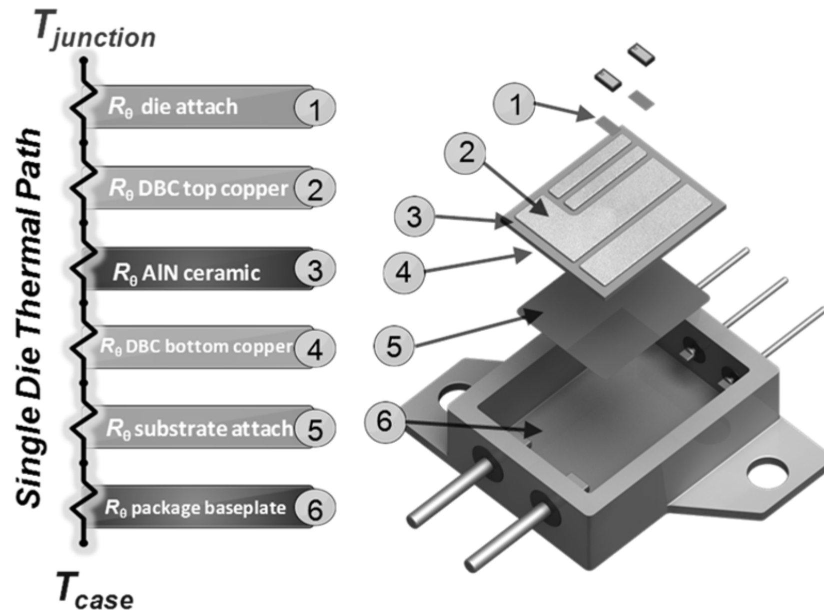

Figure 69.13 Thermal resistance network of a multi-chip power package showing material layers used to calculate thermal resistance. (From Shaw, R. et al., Thermal verification of a high-temperature power package utilizing silicon carbide devices, IMAPS 2008, pp. 1152 1159, Providence, RI, November 4–6, 2008).

One of the keys to develop high temperature high power density packaging technologies is to know and understand material properties and how they behave over temperature so that accurate thermal models can be implemented. For example, a thermal model of a SiC power module was developed using material properties such as thermal resistance from manufacturers datasheets [33]. Most data from manufacturers of die attach materials, thermal interface materials, and various packaging materials are usually given at room temperature. What is not typically pointed out is how these properties change with respect to temperature. The package shown in Figure 69.13 was modeled using non-temperature dependent thermal properties given by the manufacturers, the simulations showed that junction temperature of the SiC devices would reach a maximum of 260 °C under certain operation conditions. The same system was modeled

again using measured temperature dependent properties showing the SiC devices reaching a maximum junction temperature of 300 °C, a 40 °C difference over using room temperature properties.

The previous example displays the importance of understanding material properties with respect to temperature. The thermal conductivity of SiC and AlN both change significantly over temperature and these properties must be taken into account when designing for high temperature operation. Some materials and their properties are commonly known and thus can easily be taken into account when performing thermal simulations on a system. On the other hand, materials such as solders and thermal interfaces do not have temperature dependent data readily available. To consider these materials in a thermal model the properties over temperature have to be determined experimentally.

With careful use of material properties, a thermal model can be used to accurately predict the performance of a system. Figure 69.14a shows a model developed by obtaining and measuring temperature dependent properties of each material utilized in the package such as solders and thermal interface materials. The actual system was implemented and imaging via a thermal camera shown in Figure 69.14b confirmed the models accuracy.

Ceramics tend to have some of the most drastic changes in thermal properties with elevated temperature. Figure 69.15 is a chart of thermal conductivity of substrate materials versus temperature illustrating the decay of thermal performance at high temperatures. At room temperature the thermal conductivities range from ~ 35 W/m·K for Al_2O_3 to ~260 W/m·K for BeO, in comparison, at 350 °C, those values change to 15 W/m·K and 90 W/m·K respectively. At high temperatures, the thermal advantage of BeO is not as well pronounced as it is at room temperature.

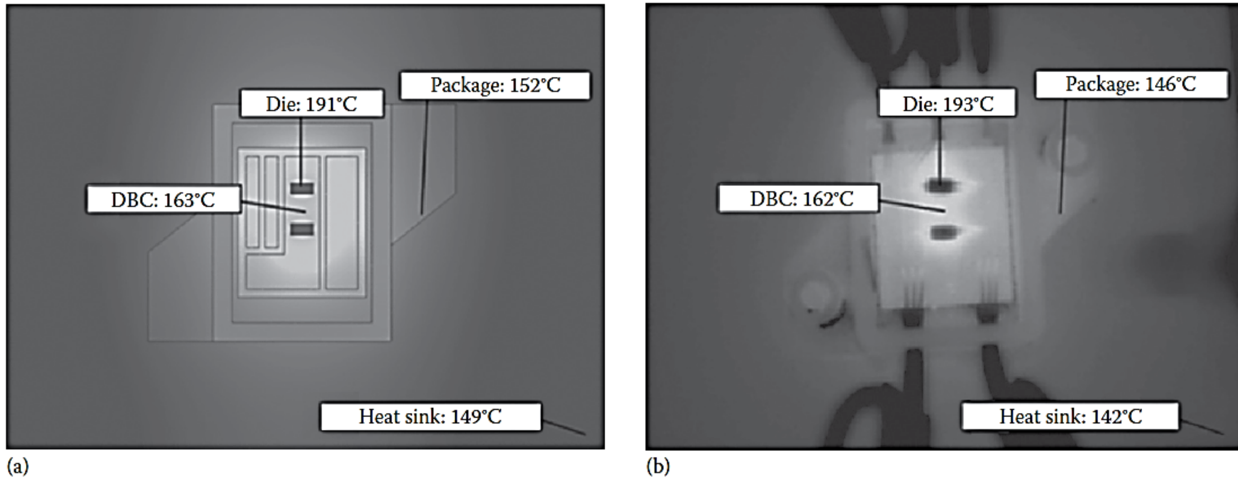

Figure 69.14 Thermal model of SiC power module using temperature-dependant properties (a) and thermal imaging of actual SiC module operating with a known power loss (b).

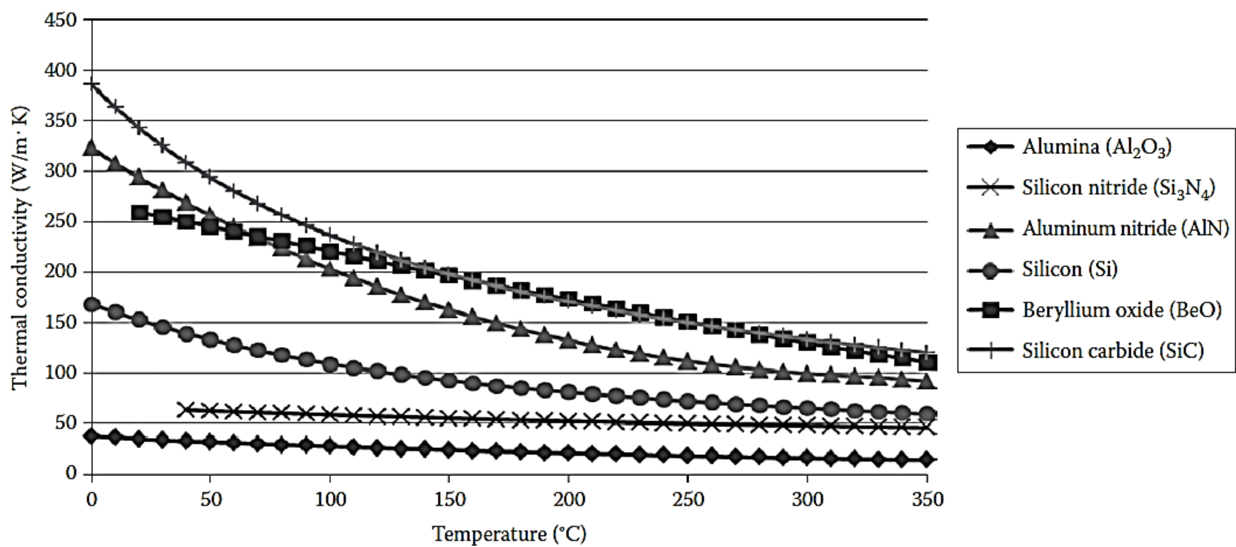

Figure 69.15 Thermal conductivity vs. temperature for substrate materials.

69.3 Power Electronic Packages

A crucial aspect in the development of a power module packaging approach is the selection and/or design of the package housing. Key specifications that need to be considered for SiC modules are voltage, current, thermal resistance, and reliability.

There are a few types of packages for discrete devices: metal, ceramic, and plastic packages can be found in footprints such as TO-254/258. Plastic injection molded packages are common for standard power electronics, and can be made inexpensively and in very high volumes. However, plastic packages degrade quickly due to the elevated operation temperatures of SiC power die. One advantage of metal and ceramic packages is that they are capable of withstanding high temperatures, however, the user must be careful when selecting the pin seal material (typically glass or ceramic). The seals may pose a reliability risk as they are prone to cracking under lead bending and thermal cycling conditions as well as voltage arcing from pin to case under high voltage conditions. Another advantage of metal and ceramic packages is that they can be hermetically sealed to protect the device from environmental vulnerabilities such as moisture.

Discrete metal and ceramic packages are available from several manufacturers; however their larger counterparts that house several devices are not. Figure 69.16 is an image of a 26 pin power package. These packages have a base plate material comprised of GlidCop® or a metal matrix composite such as CoMo and either a glass or ceramic seal for the pin. The pin material is a 52 alloy copper core at 0.06 inches diameter and is capable of a continuous current rating of 35 A. A power substrate is required for electrical routing and isolation. This style of package may also be customized and manufactured with different base materials such as copper moly or copper tungsten to reduce CTE mismatches. An advantage with this type of package is flexibility – with variations in the power substrate, a variety of topologies (half-bridge, full-bridge, three phase, etc.) may be housed in the same footprint.

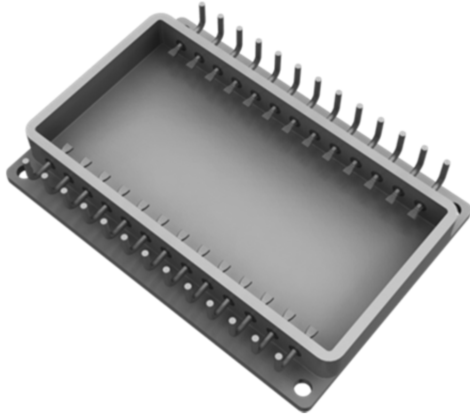

Figure 69.16 Metal 26 pin power Package for housing multiple die with Flexible layout options.

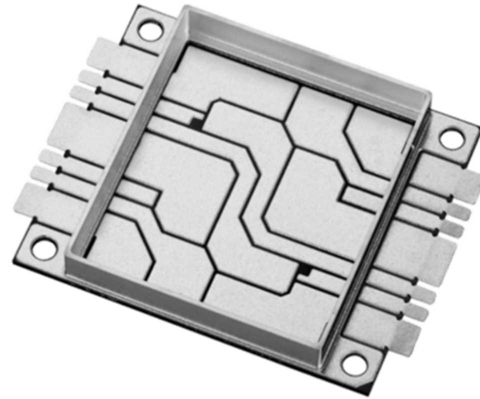

Figure 69.17 Multilayer silicon nitride hermetically sealable power package From Kyocera. (Courtesy of Kyocera Corporation).

Multi-chip ceramic packages such as the one shown in Figure 69.17 take advantage of Kyocera's multilayer Si_3N_4 substrate technology, have a metal hermetic seal ring and offers similar advantages as the metal packages. With a multilayer substrate, external connections can be made through metal tabs protruding from the sides of the package and a metal sealing ring brazed to the substrate. This approach eliminates the glass/ceramic seals that are found around each of the pins in the previously described package and therefore eliminates the dominating reliability concern faced in the metal packages. The disadvantage with this type of approach is the limited flexibility in the design configuration for multiple uses, and high cost for custom low volume systems due to fabrication and tooling.

Another type of power package that is more common in high power systems is the power brick module. Figure 69.18 shows an image of three different types of power pricks, the two modules on the right are standard modules typically housing silicon MOSFET and IGBT's configured in a half-bridge topology. The module on the left [34] is a high temperature (225 °C) low parasitic module designed by APEI, Inc. to take advantage of the high operating temperature and high switching speed capabilities of SiC. These power brick modules are not hermetically

sealed but commonly use gel or other potting compounds to protect the devices. A big advantage to this type of package is that they have high current handling capabilities typically in the 100-1000 A range.

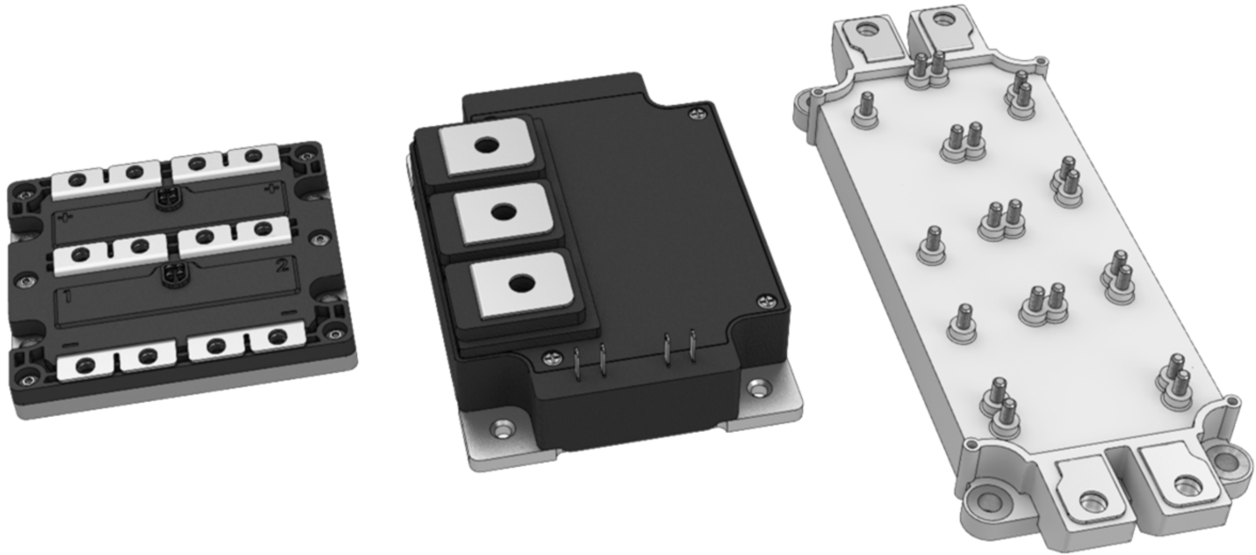

Figure 69.18 Example CAD drawings of three different power brick modules.

To take full advantage of the high switching speeds and high power density capabilities offered by SiC electronics, the integration of high temperature power devices and high temperature control electronics into a single module was developed. This approach is known as a multichip power module (MCPM) [20,-35-37]. Integrating the control and power sections of a power electronics platform greatly minimizes parasitics, allowing very high frequencies of operation. These modules utilize high temperature silicon-on-insulator (HTSOI) integrated circuits for the control and gate drive and have the capability to operate at temperatures in excess of 225 °C [28]. Figure 69.19 shows an image of a 4 kW 3-phase induction motor drive MCPM on the left and a half bridge 50 kW module with integrated gate drive on the right.

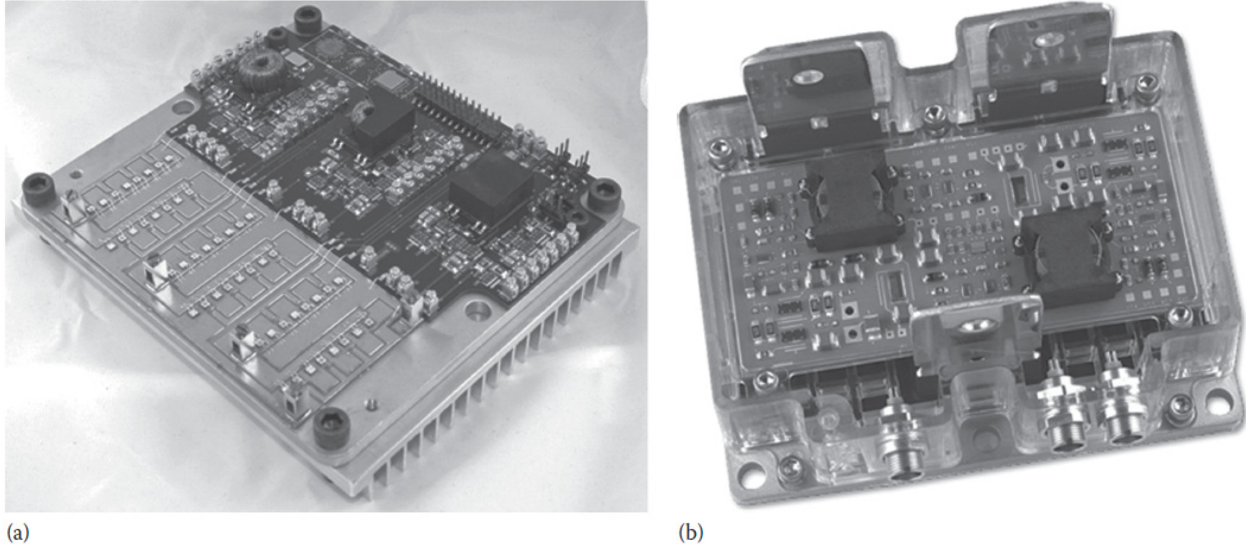

Figure 69.19 Examples of multichip power modules (MCPMs). Integrated three-phase induction motor drive (a) and 50 kW half-bridge power module with integrated gate drive (b).

Many design engineers strive to find "the" solution to a problem. However, it is imperative to realize that when designing a packaging solution for power electronics, there is rarely one ideal solution. Every material selection involves tradeoffs in thermal conductivity and CTE, as well as cost, long term reliability, and manufacturability. Rather than simply selecting each component material based on its own superior characteristics, the designer must first be aware of the critical design requirements of the system as a whole, and then select materials which will best work together in concert to meet those criteria. There is an almost infinite array of possible combinations of materials, and all of them will display some advantages and disadvantages over the others. The most successful approach will not only consider the properties of the individual materials, but their roles and interactions as part of the total integrated packaging system.

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APPENDIX

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CHAPTER 13

SUMMARY OF PUBLICATIONS

13.1 Publication One

J. Hornberger, A. B. Lostetter, K. J. Olejniczak, T. McNutt, S. M. Lal, and A. Mantooth, "Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments," in the *Proc. of the IEEE Aerospace Conference*, vol. 4, pp. 2538 – 2555, March 2004.

This paper discusses SiC materials, and early SiC power devices such as Schottky diodes, MOSFETs, and static induction transistors (SITs) including the theoretical benefits of SiC power switch technology as it relates to power electronics systems in harsh environments. The beginning work of the researcher, high-temperature control electronics for SiC motor drive systems, is introduced. Additionally, two NASA applications are discussed including: 1) probes & landers that operate in high-temperature environments, and 2) ultra-lightweight power electronics for satellite and spacecraft. Other applications discussed are for military electric vehicles and down-hole energy exploration.

There is a section in this publication entitled "Improving SiC Technology" that gives an introduction to SiC as a substrate material in the late 1950s and its development today into usable wafers for device fabrication. This section also lists the major areas for SiC development at the time of publication (2004); these areas include:

1. Increasing the yield in substrate fabrication i.e., reducing micropipes and other physical defects,
2. Developing practical SiC devices and working through issues such as gate oxide layers,

3. Improving on and developing new models for these SiC devices so that end users could simulate such devices in their systems,
4. Developing high-temperature and extreme environment electronics packaging so that the end user could reap the full benefits from the device, and,
5. Getting these new SiC devices into power electronics systems and applications.

The device section of this paper, the work of Dr. Ty McNutt (co-author), includes a discussion of SiC device physics and structures of the Schottky diode, DMOSFET, and the SIT.

The author's contributions begin in the section titled "Current Work" where the concept of a multichip power module (MCPM), introduced by Olejniczak [14] for silicon-based power electronics, is introduced for SiC-based power electronics in order to solve the space-limited motor drive application of a down-hole orbital vibrator (DHOV). The MCPM concept includes the integration of control electronics with power electronics to make a high-temperature, compact, all-inclusive motor drive system that can fit in a down-hole tool for energy exploration.

The author's overall goal is to develop the high-temperature SiC concept of the MCPM three-phase motor drive as depicted in Figure 5 of this publication. At the time of this publication, the author developed the base controller (research milestone one in Figure 2.1) that consisted of standard temperature components equivalent to the high temperature silicon-on-insulator (HTSOI) analog/digital integrated circuits (IC) available from Honeywell that were specifically developed to operate in extreme temperatures. A schematic block diagram explanation of the controller, shown in Figure 7 of the publication, is broken up in to sections that include:

1) Core microcontroller and memory
2) Voltage regulation

3) Current drive or amplification of signals

4) Signal isolation of the control from the power stage

5) Circuit protection.

Additionally, a high-temperature testbed (research milestone two in Figure 2.1) developed by the author is introduced consisting of a printed-circuit board (PCB), test sockets for the ICs, transformers, and solders, all capable of high-temperature operation (> 250 °C).

An introduction of packaging for high-temperature power electronics relating to discrete packaged devices as well as MCPM packaging approach are discussed.

13.2 Publication Two

J. Hornberger, A. B. Lostetter, K. J. Olejniczak, S. Magan Lal, and A. Mantooth, "A Novel Three Phase Motor Drive Utilizing Silicon on Insulator (SOI) and Silicon-Carbide (SiC) Electronics for Extreme Environment Operation in the Army Future Combat Systems (FCS)," in the *Proc. of the 37th International Symposium on Microelectronics* (IMAPS 2004), vol. 2, pp. 649 – 654, November 2004.

One of the major advantages of SiC power electronics is its capability to operate at much higher temperatures (theoretically up to 600 °C) than standard commercial silicon components. In the early stages of this research, the author recognized that electronics packaging is a key element in the realization of a high-temperature MCPM motor drive because current packaging technologies designed around silicon devices were typically capable of operation up to 125 °C. Therefore, this publication focuses on the packaging techniques to enable high-temperature operation. One of the author's funding sources was through an Army Research Labs (ARL) contract to develop and demonstrate high-temperature motor drive functionality geared toward

the Army's Future Combat Systems (FCS) program. This publication introduces the FCS program goals and how SiC power electronics plays a major role.

Additionally the high-temperature testbed (research milestone two in Figure 2.1) is detailed further and specific components including magnetic materials, resistors, capacitors, solders, and substrate materials are brought to light. One of the problems with the initial high-temperature testbed was that the high-temperature magnetics were limited in frequency of operation and were quite large due to the large number of windings required. With the help of Magan Lal (co-author of the paper), a new transformer was developed that is capable of operating from 5 kHz to 1 MHz and peak temperatures of 400 °C; transformer test results are shown in Figure 7 of the publication.

13.3 Publication Three

J. Hornberger, S. Mounce, R. Schupbach, H. A. Mantooth, and A. B. Lostetter, "High-Temperature Silicon Carbide (SiC) Power Switches in Multichip Power Module (MCPM) Applications," in the *Proc. of the IEEE Industry Applications Society Annual Meeting*, vol. 1, pp. 393 – 398, October 2005.

Over the next several months the author began to develop the SiC MCPM from concept to reality. This publication details the steps taken to prove feasibility by building a single-phase MCPM with the HTSOI control circuitry previously described, except implemented in bare die form for the MCPM packaging approach (research milestone three in Figure 2.1). Additionally, bare die SiC junction field-effect transistors (JFET) were obtained and integrated into the single-phase MCPM. Accordingly, the control and gate drive circuitry were modified to drive these JFET switches that had a turn-off voltage of approximately -15 V and are normally on at a gate voltage of 0 V.

With any power electronic system, thermal dissipation is a key factor to be cautious about. With the help of McPherson and Lostetter (co-authors), a FlowTherm model of the MCPM was created and simulations to detect power device junction temperature versus power loss dissipation were performed. A thermal comparison was performed between a SiC MCPM that can operate to 300 °C at the die junction and a Si MCPM that is limited to 150 °C at the die junction. The results showed that if everything about the system was equivalent, with the exception of device material, the Si system could process 1.3 kW of power while the SiC system could process 3.6 kW of power demonstrating an ~ 3× increase in power density.

Finally, this publication introduces the single-phase MCPM prototype shown in Figure 8 of the publication and electrical testing results (Figures 9-11) of the MCPM operating at the target temperature of 250 °C.

13.4 Publication Four

J. Hornberger, S. Mounce, R. Schupbach, B. McPherson, H. Mustain, A. Mantooth, W. Brown, and A. B. Lostetter, "High-Temperature Integration of Silicon Carbide (SiC) and Silicon-on-Insulator (SOI) Electronics in Multichip Power Modules (MCPMs)," in the *Proc. of the 11th European Conference on Power Electronics and Applications* (EPE 2005), pp. 1 – 10, September 2005.

The next paper, presented at the European Power Electronics Conference in Dresden Germany, highlights again the single-phase MCPM (research milestone three in Figure 2.1) but adds information relating to packaging issues that are encountered when operating at high-temperature. Specifically the power substrates, which are typically aluminum nitride (AlN) or alumina (Al_2O_3) ceramics laminated with thick (125 um – 500 um) copper (Cu), can be a significant reliability issue during wide temperature swings due to the coefficient of thermal

expansion (CTE) mismatch of the materials. These power substrates are typically nickel or nickel/gold plated to aide in solder attach and wire bonding.

This publication also presents studies by Mustain (co-author) on electroless nickel phosphide plating solution containing 6-8% phosphorus used as a diffusion barrier to keep copper from moving to the surface and oxidizing. Substrates were gold plated over the top of electroless nickel plating and were cycled and annealed at temperatures up to 350 and 400 °C. Energy Dispersive X-ray (EDX) analysis showed that after this annealing, large amounts of phosphorus were present at the surface indicating the breakup of the nickel phosphide plating. These results led the researchers to consider other metals to be used as diffusion barriers. Titanium-tungsten (TiW) and tungsten carbide (WC) diffusion barriers are also presented in the publication.

In addition to the substrate plating, the publication relates tests that were performed on 75 um gold wire bonds to determine degradation at high temperatures. The results showed that gold wire bonds on Ni/Au plated substrates degraded in pull strength at temperatures of 300 and 400 °C but still met U.S. MIL-STD-883 pull strength requirements.

13.5 Publication Five

J. Hornberger, B. McPherson, E. Cilio, R. M. Schupbach, S. Mounce, A. B. Lostetter, and H. A. Mantooth, "Packaging of a High-Temperature Silicon Carbide (SiC) Mulitchip Power Module (MCPM)," in the *Proc. of the 38th International Symposium on Microelectronics* (IMAPS 2005), vol. 2, pp. 579 – 585, September 2005.

In this publication, the mechanical design of the SiC MCPM is discussed and more details focus on the high-power portion of the packaging where previously the low-power (analog/digital controller) block was discussed. Information such as materials for power

substrates, solders for high-temperature die attach, and metal-matrix composite (MMC) base plates are introduced.

A key component in the MCPM that tends to be one of the most difficult to find for high-temperature operation are capacitors; therefore, the author conducted a study of a dozen capacitor technologies to determine which technologies have the most promise for high-temperature operation. With the help of Mounce (co-author), these capacitors were biased and tested to temperatures as high as 400 °C while the capacitance was measured. Figure 8 in the publication contains the results of this test showing that ceramic NPO/COG capacitors were the most stable across the entire temperature range.

The research also introduced the next step in the research which was to move from a single-phase MCPM to a three-phase MCPM (research milestone four in Figure 2.1). Figure 13 of the publication shows an image of a three-phase MCPM that the researcher fabricated with the gate driver and controller on the PCB on the left and the power stage on the AlN substrate on the right. This step was again a testbed to ensure the feasibility of integration of an entire three-phase system.

13.6 Publication Six

Jared M. Hornberger, Edgar Cilio, Roberto M. Schupbach, Alexander B. Lostetter, and H. Alan Mantooth, "A High-Temperature Multichip Power Module (MCPM) Inverter Utilizing Silicon Carbide (SiC) and Silicon on Insulator (SOI) Electronics," in the *Proc. of the 37th IEEE Power Electronics Specialists Conference* (PESC 2006), vol. 1, pp. 9 –15, June 2006.

This publication was presented at the plenary session of the Power Electronics Specialist Conference (PESC) in South Korea. The publication overviews the use of SiC in power

electronics and provides reference to how a SiC system has the capability to be smaller, lighter, and process more power than that of a Si system.

The MCPM power module concept is discussed and results from electrical testing of the SiC MCPM three-phase demonstrator (research milestone four in Figure 2.1) are shown. Figures 10 and 12 of the publication show signals from the control and gate drive at 25 °C while Figures 11 and 13 show the same waveforms at 250 °C. Additionally, Figures 14 and 15 show the three-phase output currents and line-to-line voltages of the MCPM switching at 20 kHz while generating 60 Hz sinusoidal outputs.

13.7 Publication Seven

J. Hornberger, E. Cilio, B. McPherson, R. Schupbach, A. Lostetter, and A. Mantooth, "A High-Temperature Silicon Carbide (SiC) Mulitchip Power Module (MCPM) Inverter for Down-Hole Applications," in the *Proc. of the International Conference on High Temperature Electronics* (HiTEC 2006), vol. 1, pp. 279 – 286, May 2006.

At the High-Temperature Electronics Conference (HiTEC 2006) the author focused more on the application of the DHOV that was mentioned in Publication 1. Further details of how the DHOV operates are presented here. Additionally, the next research milestone (research milestone five in Figure 2.1), the final SiC MCPM design and two-phase implementation are presented in this paper.

There is a good discussion about thermal modeling that includes a way to calculate the effective thermal resistance of a bare die based off area and the angle of thermal spreading; this calculation was used as a baseline for McPherson (co-author) when implementing a 3-D CAD model in FloTHERM®. Using the thermal simulations a proper heatsink was selected to be used for the full-power SiC MCPM.

The two phase demonstrator was configured in an H-bridge configuration as shown in Figure 13 of the publication. With the help of Cilio (co-author), the MCPM was electrically tested operating as an inverter; the results of the testing (shown in Figures 14-18 of the paper) show a filtered sinusoidal output while processing ~ 3 kW of electrical power.

13.8 Publication Eight

J. M. Hornberger, B. McPherson, E. Cilio, R. M. Schupbach, A. B. Lostetter, and H. A. Mantooth, "Packaging of a High-Temperature Silicon Carbide (SiC) Three-Phase 4 kW Motor Drive," in the *Proc. of the 39th International Symposium on Microelectronics* (IMAPS 2006), vol. 2, pp. 721 – 728, October 2006.

This publication moves the reader into the final research milestone (research milestone six in Figure 2.1) showing the fabricated full-power, three-phase SiC MCPM in Figure 16 of the publication. More details of the packaging technologies developed are shown; in particular, Figure 3 of the publication shows a cross-section of the entire MCPM packaging stack from heatsink to interconnections to bare die. The publication discusses details about selecting proper power substrates and baseplate materials and includes tables of material properties to help the reader understand the differences in these materials.

13.9 Publication Nine

Jared M. Hornberger, Edgar Cilio, Brice McPherson, Roberto M. Schupbach, Alexander B. Lostetter, and H. Alan Mantooth, "A Fully Integrated, 4 kW, 3-Phase, SiC Motor Drive Module," in the *Proc. of the 38th IEEE Power Electronics Specialists Conference* (PESC 2007), vol. 1, pp. 1048 – 1053, June 2007.

This publication wraps up the work of the author and presents a full-power (4 kW), high-temperature (>250 °C) operation of the three-phase motor drive system (research milestone six in

Figure 2.1). One of the electronic packaging challenges that presented itself during testing of the two-phase MCPM was that high voltage operation of the SiC devices could not be obtained without protecting the device in a dielectric layer to prevent electric breakdown (drain-source) of the device in air. This material, referred to as encapsulation, is discussed and examples of materials that were tested for high-temperature operation are shown.

Finally, the high-temperature testing setup shown in Figure 6 of the publication was implemented to demonstrate 600 V, 4 kW, three-phase operation of the SiC MCPM at a baseplate temperature of 250 °C. Waveforms showing the unfiltered output voltage and current at 25 °C and at 250 °C are shown in Figures 7-10 of the publication, while Figures 11-14 show the filtered output signals of the system. Thermal measurements were taken to monitor the temperature of the control board, power substrate, heat spreader, and heatsink and an estimated power loss is calculated. Finally, overall system efficiency - including the output filter - was measured at ~ 94% while the MCPM efficiency at the output of the power devices is estimated to be ~98%.

13.10 Publication Ten

Hornberger et al., "Silicon Carbide Power Electronics Packaging," Cressler J. D., Mantooth H. A., *Extreme Environment Electronics 1st ed.*, Boca Raton, FL, CRC Press, 2012, Ch. 69, pp. 803-817.

The author was invited to compose a chapter on SiC power electronics packaging for an extreme environment electronics book published by CRC Press and edited by John D. Cressler and H. Alan Mantooth. This publication brings the author's work in packaging up to date and thoroughly covers the key components in power electronics packaging including baseplates, substrates, die and substrate attach, thermal modeling, and packaging approaches.

This publication steps the reader through the process of material evaluation and selection when designing for high temperature. Table 69.1 in the publication is a compilation of baseplate materials and their properties while Table 69.2 and 69.3 is a compilation of the same for substrates and solders, respectively. There is much discussion on the importance of knowing material properties versus temperature of operation as many of the material properties change significantly from their room temperature values to their high temperature values. A good discussion of solder thermal conductivity and void free soldering is contained within Section 69.1.3 of the publication indicating that even though a solder has a much lower thermal resistance than another solder, depending on the actual system, it may only make marginal gains in the system over a less expensive higher thermal resistance solder alloy (see Figure 69.8 of the publication).

Section 69.2 of the publication, focusing on a thermal design approach, shows again the importance of taking into account thermal properties of materials. Figure 69.15 of that section shows a comparison of thermal conductivities over temperature (0 °C to 350 °C) for different power electronics substrate materials, aluminum nitride (AlN) for example has a thermal conductivity of ~300 W/m·K at room temperature versus a drop to about 100 W/m·K at 300 °C.

This publication ends with a discussion on power packages for discrete devices as well as power modules with many die in parallel and finally multi-chip power modules with integrated gate drivers. Example pictures of these packages are shown in Figures 69.16-19 of the publication.

REFERENCES

[14] Olejniczak, K., Burgers, K., Ang, S., Porter, E., "Conversion of Electrical Energy from One Form to Another, and its Management through Multichip Module Structures," Patent Number US 6,462,976 B1, United States Patent Office, Granted on October 8, 2002.

CHAPTER 14

CONCLUSIONS AND RECOMENDATIONS

The goal of the author to advance the state of the art for power electronics through the packaging of emerging SiC power semiconductor technology and implementation in systems and applications has been accomplished. Through the course of the work presented here, a high-temperature, high-efficiency, multichip power module (MCPM) motor drive was developed and demonstrated to operate at a temperature of 250 °C and power levels up to 4 kW. The research demonstrated that SiC high temperature systems are possible for applications such as down-hole oil exploration and that high power density and high junction temperatures are possible for applications such as electric and hybrid electric vehicles. Also demonstrated through high power density SiC systems is the ability to reduce or remove cooling systems and reduce the size of power electronic systems by as much as an order of magnitude.

At the component level several active and passive devices such as capacitors, resistors, transformers, ICs, and power semiconductors have been proven to operate in extreme temperature environments. Additionally packaging technologies such as the MCPM approach including solder attaches, wire bonding, substrates, and surface plating have all been demonstrated for use at high temperatures.

Finally, there have been much resources across the globe that have been put into the development of these new SiC devices resulting in the commercialization of diodes, MOSFETs, BJTs, and JFETs. In order to take full advantage of the high power density, high temperature, high performance capabilities of these SiC devices and insertion into power electronic systems, more resources will need to be placed into the development of the packaging technologies demonstrated here to prove feasibility and reliability over time.

APPENDIX

Statement of Work Performed

I, Dr. Alan Mantooth, verify that Jared Hornberger has performed at least 50% of the work represented in the papers listed for re-publication in Chapters 3-12 of this dissertation titled “The Development and Packaging of a High-Density, Three-Phase, Silicon Carbide (SIC) Motor Drive.”

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Dr. H. Alan Mantooth