University of Arkansas, Fayetteville
ScholarWorks@UARK

Theses and Dissertations

12-2012

A Silicon Carbide Based Solid-State Fault Current Limiter for Modern Power Distribution Systems

Erik Darnell Johnson
University of Arkansas, Fayetteville

Follow this and additional works at: http://scholarworks.uark.edu/etd

Part of the Polymer and Organic Materials Commons, Semiconductor and Optical Materials Commons, and the VLSI and Circuits, Embedded and Hardware Systems Commons

Recommended Citation
Johnson, Erik Darnell, "A Silicon Carbide Based Solid-State Fault Current Limiter for Modern Power Distribution Systems" (2012). *Theses and Dissertations*. 585.
http://scholarworks.uark.edu/etd/585

This Dissertation is brought to you for free and open access by ScholarWorks@UARK. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of ScholarWorks@UARK. For more information, please contact scholar@uark.edu, ccmiddle@uark.edu.

A SILICON CARBIDE BASED SOLID-STATE FAULT CURRENT LIMITER FOR MODERN POWER DISTRIBUTION SYSTEMS

A SILICON CARBIDE BASED SOLID-STATE FAULT CURRENT LIMITER FOR MODERN POWER DISTRIBUTION SYSTEMS

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering

By

Erik Darnell Johnson
University of Arkansas
Bachelor of Science in Electrical Engineering, 2006

December 2012
University of Arkansas

ABSTRACT

The fault current limiter represents a developing technology which will greatly improve the reliability and stability of the power grid. By reducing the magnitude of fault currents in distribution systems, fault current limiters can alleviate much of the damage imposed by these events. Solid-state fault current limiters in particular offer many improved capabilities in comparison to the power system protection equipment which is currently being used for fault current mitigation. The use of silicon carbide power semiconductor devices in solid-state fault current limiters produces a system that would help to advance the infrastructure of the electric grid.

A solid-state fault current limiter utilizing silicon carbide super gate-turn off thyristors (SGTOs) and silicon carbide PiN diodes was designed, built, and tested as a technology demonstrator. The impact of using silicon carbide (SiC) devices in this application was assessed, as well as the associated design challenges. The feasibility of implementing SiC based solid-state fault current limiters for 15 kV class distribution systems was investigated in order to determine the practicality of wide-scale deployment.

This dissertation is approved for recommendation
to the Graduate Council.

Dissertation Director:

____

Dr. H. Alan Mantooth

Dissertation Committee:

____

Dr. Simon Ang

____

Dr. Juan Balda

____

Dr. Alex Lostetter

____

Dr. Roy McCann

DISSERTATION DUPLICATION RELEASE

I hereby authorize the University of Arkansas Libraries to duplicate this dissertation when needed for research and/or scholarship.

Agreed______________________________
Erik Darnell Johnson

Refused______________________________
Erik Darnell Johnson

ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisor Dr. Mantooth for all of this guidance and support over the years. He has offered advice to me in a number of different areas over the duration of my graduate studies, and it is greatly appreciated. I would also like to thank my graduate committee members Dr. Balda, Dr. Ang, Dr. McCann, and Dr. Lostetter for always finding time to offer feedback despite their busy schedules. I am also grateful to Mr. T.A. Walton and Mr. Thomas Carter III for always offering words of encouragement and looking after my best interests. Special thanks to Osama Saadeh, with whom I have worked on this project for the past several years. I have learned a lot from him over the years, and I am glad to count him among my good friends. I would like express appreciation the other students that I have had the pleasure to work alongside over the years for great conversation and many outstanding memories, including Mahmood Saadeh, Javier Valle Mayorga, Mihir Mudholkar, Jake Williams, Brian Stalling, Tavis Clemmer, Scott Guerin, and Derik Trowler.

Lastly, but certainly not least, I am deeply appreciative for my family. They have been a constant source of encouragement and support, and I am extremely blessed to have them in my life. Thanks to my grandmother Lucille Smith and my aunts, all of whom have provided a strong model of faith that I aspire to achieve. My aunt has Lori has always provided me with dependable advice and unwavering support. My aunt Dorothy has always offered calming words to get me through many difficult times. Thanks to my brother Wayne for always being someone that I always count on for a laugh. I have looked up to him my entire life and am proud to call him my big brother. Most importantly, I would like to thank my mother Helen Johnson. I could not ask for a better parent, and she has been there for me every time I have ever needed. Thanks for being my source of encouragement and always reminding me to turn to prayer in the difficult

times. Thanks for always lending an ear to listen and for reminding me of the things that are truly important in this life. Words cannot adequately express my gratefulness. Above all, I hope to honor Christ in all that I do and achieve. It is by his grace and mercy that I am here, and through his strength that I can do all things.

TABLE OF CONTENTS

Chapter 1: Introduction 1
1.1 Fault Currents in Power Systems 1
1.2 Protection Against Fault Currents 2
1.3 Fault Current Limiters in Power Systems 4
1.4 Dissertation Structure 8
Chapter 2: Overview of Fault Current Limiter Technologies 9
2.1 Superconductivity in Power Systems 9
2.2 Superconducting Fault Current Limiters 12
2.2.1 Resistive Superconducting Fault Current Limiter 12
2.2.2 Bridge Type Superconducting Fault Current Limiter 14
2.2.3 Shielded-Core Superconducting Fault Current Limiter 15
2.2.4 Saturated Core Superconducting Fault Current Limiter 16
2.2.5 Flux Lock Type Superconducting Fault Current Limiter 17
2.3 Solid-State Protection Devices in Power Systems 18
2.4 Solid-State Fault Current Limiters 21
2.4.1 Impedance Solid-State Fault Current Limiters 21
2.4.2 Bridge Type Solid-State Fault Current Limiters 23
2.4.3 Resonant Solid-State Fault Current Limiters 26
2.4.4 Programmable Fault Current Limiters 29
2.5 Fault Current Limiter Development 32
Chapter 3: Silicon Carbide Overview 34
3.1 Silicon Carbide Background 34
3.1.1 The Need for Silicon Carbide Power Devices 34
3.1.2 Silicon Carbide Structure 35
3.1.3 History of Silicon Carbide 37
3.1.4 Issues with Silicon Carbide 38
3.1.5 Characteristics of Silicon Carbide 39
3.2 Silicon Carbide Devices and Applications 43
3.2.1 Silicon Carbide Power Devices 43

3.2.2 Silicon Carbide Applications ... 46
3.2.3 SiC in Power Electronics ... 48
3.3 The Use of Silicon Carbide in Solid-State Fault Current Limiters ... 50
Chapter 4: Silicon Carbide Solid-State Fault Current Limiter Design ... 54
4.1 SiC SSFCL Switching Position ... 55
4.1.1 Silicon Carbide Super Gate Turn-Off Thyristor ... 55
4.1.2 Parallel Operation of SiC SGTOs ... 60
4.1.3 SiC SSFCL Power Module ... 65
4.2 Gate Driver for SiC SGTO ... 68
4.3 Snubber Circuit Design ... 71
4.3.1 Snubber Considerations and Topology Selection ... 71
4.3.2 Snubber Component Design ... 75
4.3.3 Snubber Circuit Simulation ... 78
4.3.4 Varistor Selection ... 84
4.4 SSFCL Controller ... 86
4.4.1 Controller Hardware ... 86
4.4.2 SSFCL Control Algorithm ... 92
Chapter 5: Silicon Carbide Solid-State Fault Current Limiter Simulation ... 96
5.1 Components of the SiC SSFCL Simulation ... 96
5.2 Simulation Results ... 100
Chapter 6: Silicon Carbide Solid-State Fault Current Limiter Testing ... 107
6.1 Testing Using Scaled-Down Silicon Carbide SSFCL Prototype ... 107
6.1.1 120 V Testing ... 110
6.1.2 208 V Testing ... 117
6.1.3 System Analysis ... 122
6.1.4 Testing Challenges ... 126
Chapter 7: Feasibility Analysis of Silicon Carbide Fault Current Limiters ... 128
7.1 Cost Analysis of Current SiC SSFCL Systems ... 128
7.2 Analysis of SiC SSFCLs for 15 kV Distribution Systems ... 133
7.2.1 Potential Issues with the SiC GTO in SSFCL Applications ... 134
7.2.2 The Potential for SiC IGBTs in SSFCL Applications ... 137

7.3 Case Study of 15 kV Class SiC SSFCL 141
7.4 System Overvoltage 151
7.5 SiC Power Semiconductor Device Research for SSFCL Applications 155
7.6 Key Points of Analysis 159
7.7 Potential for SiC SSFCL Use in Microgrid Applications 160
Chapter 8: Conclusions and Future Work 163
8.1 Conclusions 163
8.2 Recommendations for Future Work 164
References 167

CHAPTER 1

INTRODUCTION

1.1 Fault Currents in Power Systems

Since initial development, the power system infrastructures of many countries have undergone only slight changes. The stresses that many power systems must endure due to an increase in the number of connected loads create an extensive number of issues. These concerns typically involve the quality of power being delivered to consumers, and also the reliability and stability of the overall system. A continuous increase in both the magnitudes and occurrences of fault currents is among the most devastating problems related to power systems today.

Most fault currents are attributed to lightning and wind, which can cause objects to come into contact with the line and create short circuits. Other causes of fault currents are foreign objects in the equipment, loose connections, equipment overheating, and insulation failure [1], [2]. Fault currents cause mechanical and thermal stress to equipment such as transformers and motors, while also contributing considerable wear to the insulation of the conductors in the system due to overheating. Increased occurrences of faults decrease the lifetime power system components while also reducing the overall stability and reliability.

In more extreme circumstances, fault currents are often the source of widespread power outages. One of the largest blackouts in history, which occurred in southern Brazil during March 1999, was attributed to a lightning strike. As a result, almost 25 GW of load was lost for approximately 260 minutes [3]. This blackout is estimated to have left upwards of 90 million people without power [4]. In 2003, a blackout impacted the northeastern United States and a portion of Canada. One part of the sequence that was determined to have led to the cascading outages is a tree that made contact with a 345 kV transmission line. This blackout resulted in the

loss of 63 GW of load and impacted over 50 million people [5]. Large power outages such as these not only result in physical damage to power system components and periods of inconvenience for residential consumers, but they are often the source of economic turmoil because many industrial processes are hindered during this time. Other factors, such as lost labor and food spoilage also have to be taken into account. It is estimated that the 2003 Northeast Blackout resulted in approximately $6 billion in economic losses [6], [7]. Even small periods of outages could end up costing large amounts of money. Various sources place the amount of money lost by Americans during blackouts anywhere between $80 billion to $150 billion annually [8], [9]. Perhaps more importantly, places like hospitals and clinics need constant and reliable electrical power and outages of any duration could be deemed unacceptable. Because of these ongoing problems, it becomes critical to deal with fault currents as quickly as possible in order to avoid the possible ramifications. It is estimated that a majority of the complaints regarding power quality issues on transmission and distribution lines are actually because of the voltage sags that accompany faults [10]. Voltage sags are the cause of brownouts, which are also taken into account when evaluating the economic losses previously reported. It is for these many reasons that fault currents must be dealt with appropriately.

1.2 Protection Against Fault Currents

Conventionally, transmission and distribution lines have been protected against fault currents by equipment such as circuit breakers, fuses, reclosers, and sectionalizers [2]. These devices are often sized in conjunction with the short-circuit capability of the line which they are protecting. In the event of a fault, these devices usually open the line such that the current flow is interrupted and potential damage to the equipment and conductors is limited. While in use extensively for a long period of time, many issues have been exposed with traditional protection devices.

One of the main concerns is the reaction time of the traditional devices to the fault currents. It usually takes several cycles at the ac line frequency (50 or 60 Hz) for the current to be interrupted, at which point peak magnitude of the fault current has been reached. This peak is the portion of the fault current that is the most devastating. Fuses are one-time devices, meaning that once they are blown due to excessive current they must be replaced. This process can prove to be both tedious and time consuming. Circuit breakers, on the other hand, are designed to have long lifetimes and can be auto-resettable. A drawback of circuit breakers and reclosers is that they contain moving parts which are susceptible to wear over time. This reduces the overall reliability of these protection devices, especially as they are subjected to more fault currents. Even though these conventional devices are still widely used in modern transmission and distribution systems, extensive research is being conducted on developing more effective fault current mitigation devices. The development of new methods of handling fault currents will increase overall system reliability and lead to fewer occurrences of widespread power outages.

There has long been a need to overhaul the nation's electric power grid. The infrastructure is no longer sufficient in order to meet the increased electricity demands and changes must be made in order to protect the ever increasing number of critical loads. Thus, the GRID 2030 plan was developed which states several ways in which every aspect of the grid can be improved. Included in this plan are several provisions for increasing reliability, and this means that the need for new fault protection devices is now more urgent than ever [11], [12].

1.3 Fault Current Limiters in Power Systems

Current limiting devices are among the most popular of the new breed of fault protection devices. As stated in [13], in National Electric Code (NEC) Article 240.2, a current limiting device is one that "reduces peak let-through current to a value substantially less than the potential peak that would occur if the current limiting device is not used." The need for current limiting devices has been present in transmission and distribution systems for quite some time. Due to population increases and high energy demand, generating capacity has to be increased and as a result transmission and distribution systems often are re-sized to deal with the increased demand. However, replacement of conventional circuit breakers due to the increased capacity of the line is often a costly and time consuming process. In the 1970s, the Electric Power Research Institute (EPRI) determined that because of this problem the useful life of circuit breakers had decreased from twenty years to only about eight years, despite the fact that the re-sizing of distribution lines was often taken into account when the circuit breakers were installed. It was anticipated that the magnitude of the fault currents would approximately double each decade, making it necessary to continuously upgrade the circuit breakers so that the interrupting capacity would not be exceeded [14],[15]. The replacement of these breakers was expensive, time consuming, and caused reliability issues during the replacement period. This, coupled with the fact that replacement was needed more frequently, posed a number of problems [16]. Thus, they began looking at methods for delaying the installation of new circuit breakers and began more actively researching current limitation techniques.

Along with delaying the installation of new circuit breakers, other benefits of current limitation include longer transformer lifetimes, allowing for transformers to operate at higher capacities, and minimizing the damage done to conductors and other equipment during fault

conditions [17]. EPRI reported that a utility company contacted a manufacturer about the need for a current limiter on one of its feeders as early as 1970 after spending significant amounts of money on the frequent replacement of circuit breakers [14]. Previously, current limitation techniques included passive methods such as the use of series reactors along transmission and distribution lines, the splitting of buses in order to constrict the amount of current that flows to a fault location during fault conditions, sequential tripping techniques, and even high impedance transformers [16]. The problem with these methods is that they altered the configuration of the distribution network, and in some instances required inserting permanent impedances into the system. This lowered the overall efficiency and required increased thermal management in order to deal with the extra power losses. These problems, along with the previously mentioned need for fault currents to be handled in an expedient manner, prompted the development of a list of characteristics for the ideal current limiting device. Over the years, other entities have also made such lists. There are many overlapping concepts on these lists, and a summary of these are presented below [14], [15], [17–20]:

- Zero losses (low impedance) during normal operation
- High impedance during fault conditions
- Instantaneous response to faults
- Limitation of first current peak
- Permit let-through current to flow
- Operation that does not interfere with other protective devices
- High reliability and low maintenance
- No overvoltage or harmonics during operation
- Reasonable cost and complexity

- Quick transition from normal to current limiting mode (and back to normal after fault)
- Discrimination between overcurrent due to transients and true fault currents

The expected implementation of the fault current limiter (FCL) is shown below.

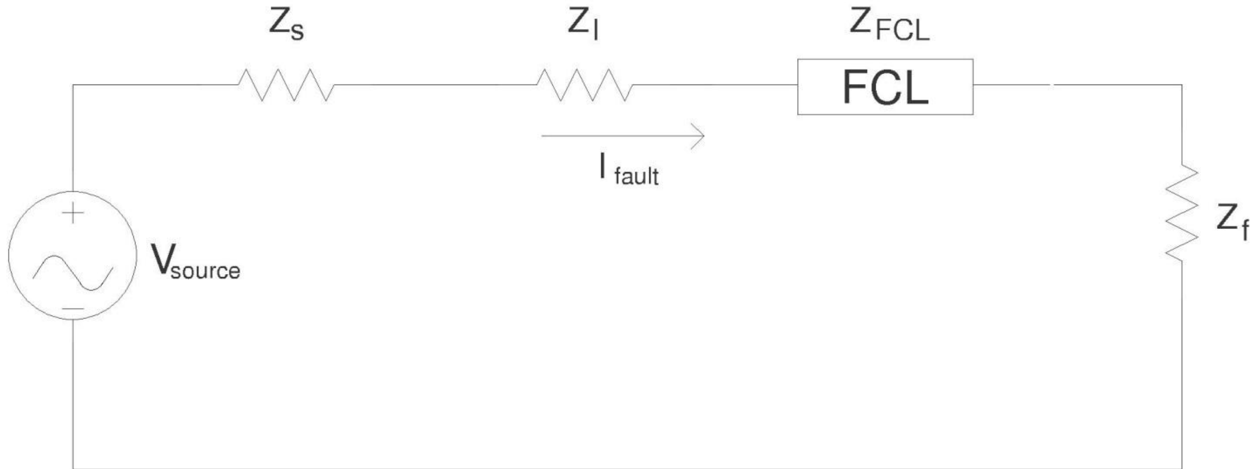


Fig. 1.1. Equivalent fault circuit diagram with fault current limiter.

During fault conditions, the magnitude of the fault current is changed due to the insertion of impedance by the fault current limiter. Thus, the equation for the fault current becomes:

$$I_{fault} = \frac{V_{source}}{Z_S + Z_L + Z_F + Z_{FCL}} \quad (1.1)$$

In this equation, Z_S is the source impedance, Z_L is the line impedance, Z_f is the fault impedance, and Z_{FCL} is the impedance inserted by the fault current limiter. It is expected that this impedance is sufficiently high in order to limit the magnitude of the fault current to an acceptable value. During normal operating conditions in which no fault is present, the value of Z_{FCL} is relatively low in order to keep losses minimal. Fig. 1.2 shows the prospective fault current of a system and a limited fault current that can be obtained by the action of a fault current limiting device.

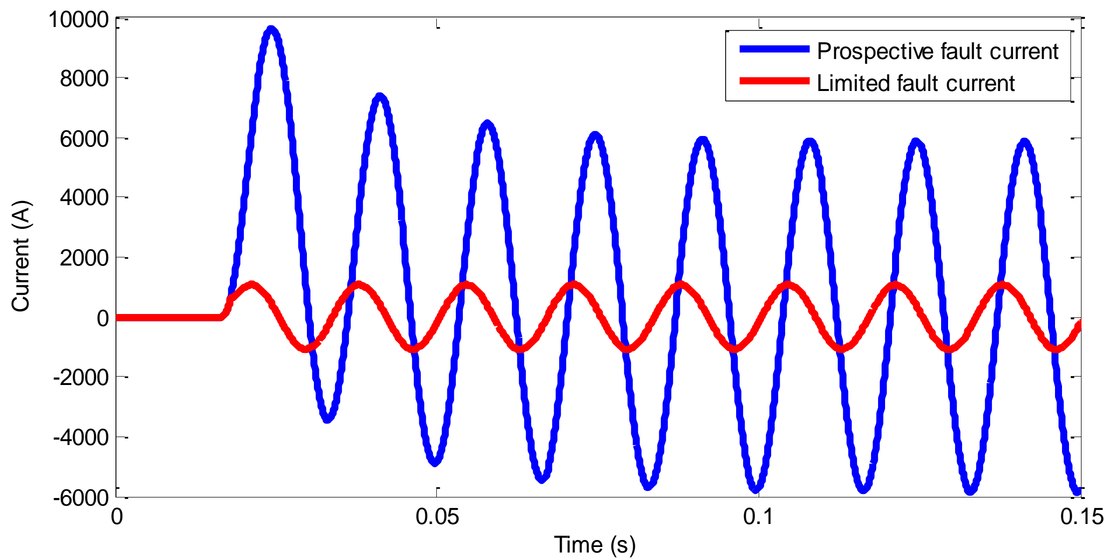


Fig. 1.2. Prospective fault current versus limited current using a fault current limiter.

Besides the insertion of impedance into the circuit in order to limit currents, other methods have also been widely investigated and analyzed.

From examination of the list of desired fault current limiter characteristics, it can be seen that many of these are only possible in theory. Realistically, a trade-off will need to be made between these parameters with the application dictating which are the most important. While fault current limiters were originally designed to be used with circuit breakers, the flexibility that these devices offer makes them attractive for potential future use in many power systems applications, including as stand-alone protection devices. Surveys of various utilities and power system operators have shown that many would be interested in replacing conventional circuit breakers with fault current limiters if the price of the new equipment was reasonable [19]. Part of the GRID 2030 initiative specifically calls for the use of fault current limiters in an effort to boost grid reliability and security. Many electric service providers have come to the realization that conventional protection devices, which are typically electromechanical, fall short of the standards needed in order adequately anticipate and respond to fault currents as part of the vision

for a more robust, reliable, and secure electric grid [12]. Over time, many types of fault current limiters have been researched extensively. These topologies all have some variation of the characteristics on this list, with inherent benefits and drawbacks. Perhaps the most popular classes of fault current limiter devices are superconducting fault current limiters (SCFCL) and solid-state fault current limiters (SSFCL). Advances in superconducting material technology and in the development of power semiconductor devices have made these FCL types the most practical for potential power systems applications. These technologies make FCLs attractive not only for immediate applications, but for applications in the grid of the future as well.

1.4 Dissertation Structure

The research in this dissertation is focused on the design and development of a silicon carbide (SiC) solid-state fault current limiter (SSFCL) system. Chapter 2 will present an overview of current topologies of fault current limiters, while examining the inherent benefits and drawbacks of each. Chapter 3 includes a brief description on silicon carbide material properties, history, and the usefulness of this material as it relates to power electronic systems and fault current limiters in particular. Chapter 4 describes the design of a 4.16 kV fault current limiter system using silicon carbide power semiconductor devices and Chapter 5 shows the simulation of the SiC SSFCL in the selected test setup. Chapter 6 includes some testing results of a scaled-down SiC SSFCL, while some of the challenges associated with wide-scale deployment of SiC SSFCL for 15 kV class distribution networks are analyzed in Chapter 7. The findings and conclusions of the research are in Chapter 8, as well as recommendations for future work.

CHAPTER 2

OVERVIEW OF FAULT CURRENT LIMITER TECHNOLOGIES

2.1 Superconductivity in Power Systems

Superconductivity is characterized as a state of a material in which it exhibits zero (or near zero) electrical resistance. This property was initially observed as the temperature of the material approached absolute zero, or 0 K. Superconductivity occurs in a material below a specific characteristic temperature; once this temperature is exceeded in the material, the resistance drastically increases [21]. The temperature at which this transition occurs is called the critical temperature T_c. Hence, superconductivity is temperature dependent, with an abrupt change in resistance occurring near the critical temperature. Normal conductors have resistance that is also temperature dependent, though this relationship is typically linear.

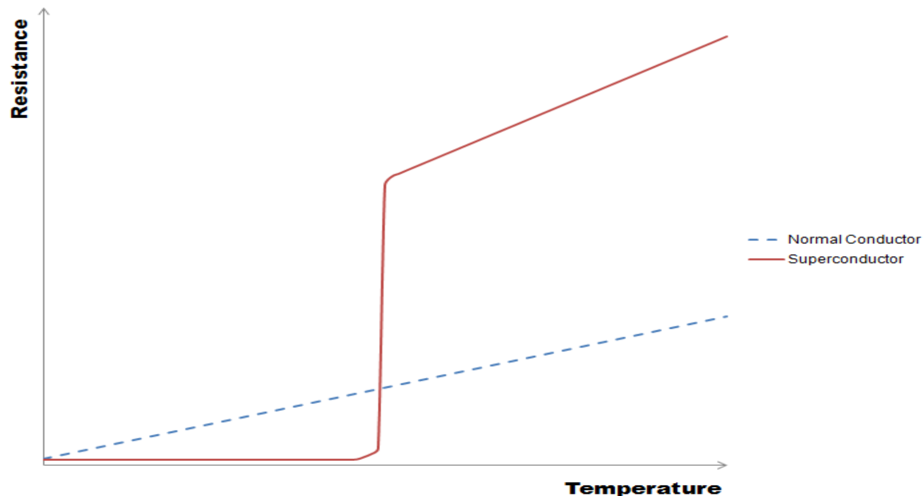


Fig. 2.1. Resistance of superconductor and normal conductor versus temperature from [22].

Even though superconductivity was discovered over a century ago, there have been many challenges in its practical implementation. Early superconductors were unable to sustain appreciable amounts of current while retaining the superconductivity characteristics. It was later discovered that this was because the superconductivity was not only a function of the material

temperature, but also of the magnetic field to which the superconductor was subjected. Above a certain critical magnetic field H_c, the superconducting characteristics are lost [23]. The critical magnetic field H_c is related to the critical current density J_c of the superconductor. These parameters, as well as the critical temperature T_c, are the defining characteristics of any superconducting material. Superconductivity is lost through quenching when any one or some combination of these three parameters is exceeded. Quenching is the process by which the superconductor transitions from its zero resistance state to a state of normal conductivity [24].

The development of type II superconductors in the 1950s and 1960s led to significant developments towards their use in electrical systems [25]. These conductors were defined by having two critical magnetic fields, H_{c1} and H_{c2}. Once the first critical magnetic field value is exceeded, the superconductor enters an intermediate phase in which superconductivity is not completely lost. Superconductivity is not lost until the second critical field is exceeded. Thus, the superconductors were able to be operated at much higher currents while still retaining the desired low resistance state. Previous superconductors, classified as type I, have a transition from their superconductive to resistive states that is characterized by only one critical magnetic field above which the material quickly changes from superconducting to resistive state. While the introduction of type II superconductors capable of operating at transmission and distribution level currents was significant, it was not until 1987 that superconductors showed the great promise they originally incited when discovered. This year marked the discovery of high temperature superconductors (HTS) [26]. This was important because superconducting systems were seen as impractical since they were required to be cooled by large and complicated refrigeration methods, and often required liquid helium in order to keep them below the critical temperature T_c. High temperature superconductors had critical temperatures above 77 K, and in

many instances this temperature approaches 100 K. This meant that these superconductors were able to be cooled using liquid nitrogen, which is much less costly. This has helped generate renewed excitement for the use of superconductors in power systems.

Naturally, there are many benefits to using superconducting cables in electric power systems. Reduced losses in the system equates to better system efficiency. EPRI estimated that the losses of conventional copper and aluminum conductors alone amounts to economic losses in the range of billions of dollars [27]. Superconductors in power systems will also result in increased power flow and help alleviate several issues associated with line overloading, especially during periods of peak demand. Superconductors are largely seen as being a central part of a renewed grid infrastructure due to the many benefits they provide. Beyond the previously mentioned uses, superconductors make several technologies possible that otherwise would have been impractical or impossible.

One of the most encouraging uses for superconductors in power systems applications is in the development of fault current limiters. The nature of the superconductor itself lends itself nicely to use in fault current limiters. Under normal operating conditions, the superconductor is able to conduct the system current with minimal losses as long as the temperature is maintained below the critical temperature of the cable using cryogenic systems. In the event of a fault, the critical current density of the superconductor is exceeded, causing the superconductor to quench. As such, the superconductor suddenly has high impedance capable of limiting the magnitude of the fault current. The transition from low impedance state to high impedance state is able to limit the fault current before the first peak, which is a critical requirement of FCLs. However, there are many stability issues with superconductors that prevent the superconductor itself from performing the current limitation. Superconductors are susceptible to localized heating due to

the fact that the resistance throughout the cable is non-uniform. Localized heating can lead to "hot spots" which can cause damage to the superconducting cable. Another issue with SCFCLs is the recovery time. After a fault occurs and the critical current density of the cable has been exceeded, there is usually a temperature rise along the cable as well. Thus, it takes some time for the cryogenic refrigeration to get the temperature back to a level where superconductivity can again be achieved [28]. This process is seen as a problem for the implementation of SCFCLs. In order to combat the aforementioned problems, more sophisticated superconducting fault current limiter topologies have been developed. The most popular of these are the resistive, saturated core, bridge type, and shielded core fault current limiters. There is also a newer superconducting FCL topology called that flux lock type that will be briefly reviewed.

2.2 Superconducting Fault Current Limiters

2.2.1 Resistive Superconducting Fault Current Limiter

Resistive superconducting fault current limiters are composed of a superconducting cable and a shunt resistance. Under normal operating conditions, the superconductor carries the system current. Cryogenic refrigeration systems are used to keep the superconductor well below its critical temperature, and as a result there are no resistive losses in the cable. In the event of a fault, the critical current density J_c of the superconductor is exceeded and it undergoes quenching. The resultant resistance of the superconductor is larger than the shunt resistor, and the fault current is diverted through the resistor which limits the current [24]. Even though this type of superconducting fault current limiter is classified as resistive, the resistor could easily be replaced with an inductor in order to provide the same limiting effect. In the figure below, the superconductor R_{SC} is represented as a variable resistive element. The shunt resistor R_{shunt} is the current limiting element.

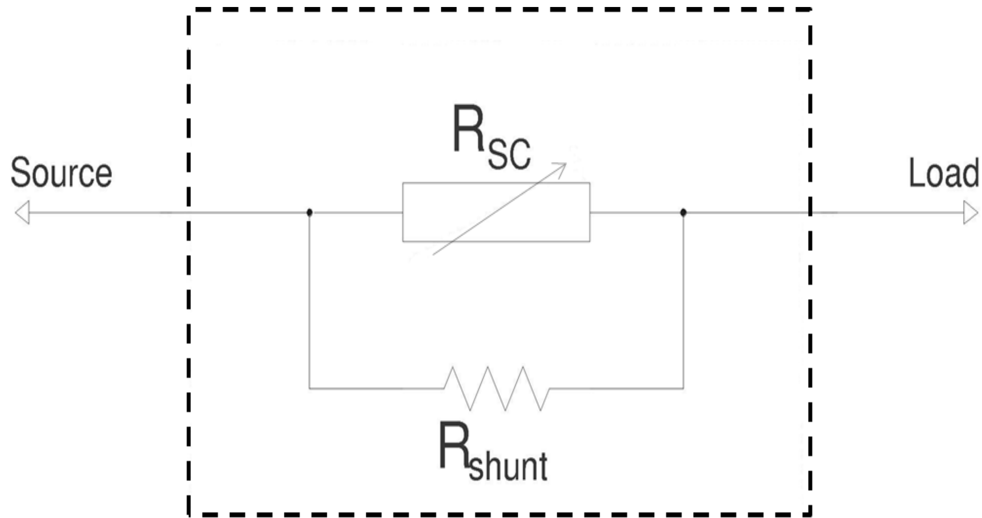


Fig. 2.2. Resistive SCFCL.

The advantages of this topology are in its simplicity and straightforward operation. As with most superconducting fault current limiters, there is no control circuitry or fault detection circuitry necessary. The SCFCL automatically responds to fault currents when the critical current density is exceeded. This may cause issues with regards to discriminating between faults and other types of high current transients. The resistive SCFCL also requires that the shunt element be connected across the entire length of the superconducting cable. This is to avoid the undesirable hot spot formation that may occur if the fault current were to flow through any portion of the superconductor. The size of this type of SCFCL may prove impractical, with both the resistor and cryogenic refrigeration needing to be physically substantial. Another issue with this type of SCFCL is that the superconductor goes through the quenching process. After undergoing quenching, the superconductor must also go through the recovery process of retaining its superconductive state. This could prove problematic because it has been indicated that the period of recovery could be up to several minutes [29]. This is unacceptable in many power system applications. Also, like other superconducting fault current limiters, the resistive SCFCL

has no current interruption capability. In order for the resistive SCFCL to have this functionality it must be used in series with a circuit breaker or some other type of fast acting switch.

2.2.2 Bridge Type Superconducting Fault Current Limiter

The bridge-type SCFCL consists of a diode bridge, a superconducting coil, and a dc bias source. In the following figure, L is the superconducting coil, D1-D4 represent the diodes comprising the bridge, V_b is the bias source, and I_o is the dc bias current established through the diodes by V_b.

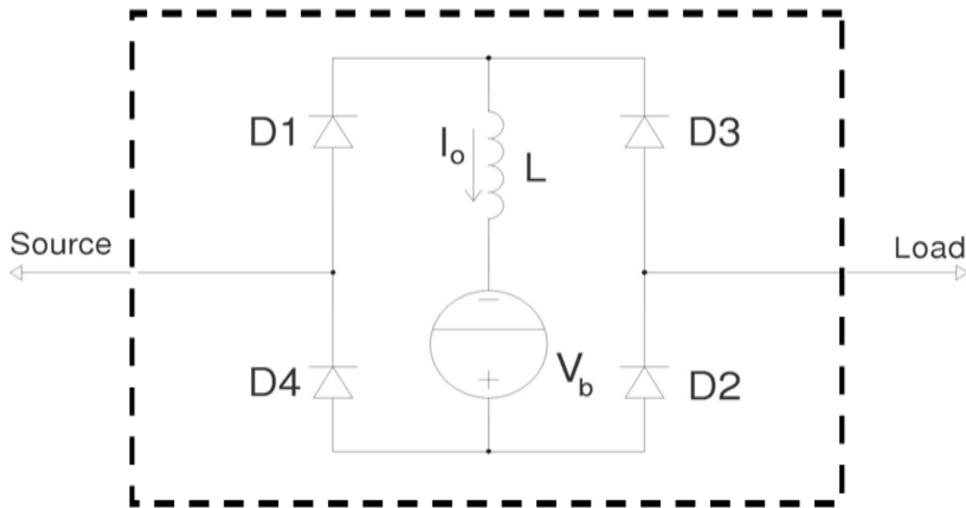


Fig. 2.3. Bridge-type SCFCL.

Under normal operating conditions, a dc current is established through each of the diodes by the bias source. As long as the operating current is smaller than the dc bias current, the impedance of the coil remains negligible, resulting in small losses during normal operation. During fault conditions, the line current rises to a value that exceeds that of the bias current. As a result, one of the diode pairs will become reverse biased, depending on whether the fault occurs during the positive or negative half cycle. Once the diodes stop conducting, the impedance of the coil increases which limits the current [30]. The superconducting coil only serves to reduce overall losses, which would be substantial if a normal coil were used. The superconducting coil

does not undergo quenching; consequently, one of the advantages of this type of SCFCL is the absence of a recovery process. Because this SCFCL utilizes diodes, a circuit breaker is typically used in series for current interruption. This is done in order to reduce the amount of time the fault current has to flow through the superconducting coil, which can lead to an excessive temperature rise.

2.2.3 Shielded-Core Superconducting Fault Current Limiter

The shielded core SCFCL behaves like a transformer with a shorted secondary winding. In actuality, it consists of a primary winding, a superconducting cylinder, and an iron core.

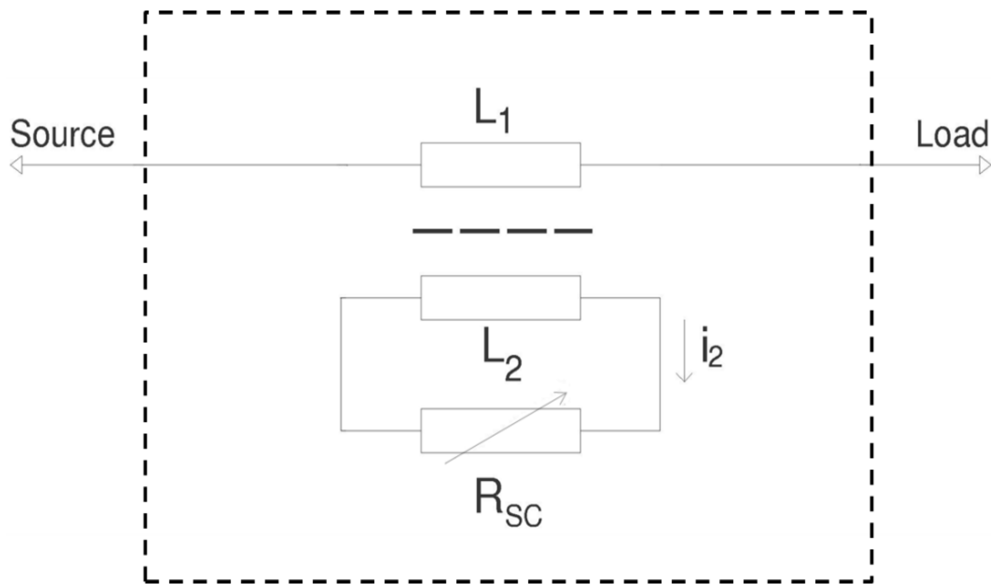


Fig. 2.4. Shielded-core SCFCL.

For simplicity, the superconducting cylinder can be thought of as the secondary winding of a transformer. In the above figure, L_1 is the primary winding, which is mutually coupled to the superconducting secondary. The secondary winding is therefore denoted as L_2 shorted with a superconducting resistance R_{SC}. The current i_2 is the current through the superconducting secondary winding.

In this configuration, the primary and secondary are wound around the same iron core. The primary is directly connected to the power system which is to be protected. Under normal

operating conditions, the flux from the primary winding is prevented from entering the core, resulting in a low inductance value. The ampere-turns of the primary are balanced by the superconducting secondary. This balance is unable to be sustained during fault conditions. This is because the critical current of the superconductor is exceeded and it undergoes quenching. As a result, flux permeates the iron core and causes an increase in inductance. The increased inductance provides the basis for the current limiting action [28], [31]. This type of fault current limiter undergoes quench, which means that it is subject to the undesirable recovery process. In order to reduce the duration of the recovery process to a time suitable for distribution network needs, a large cryogenic system may be required. This will increase the overall footprint, which is already quite large due to its configuration.

2.2.4 Saturated Core Superconducting Fault Current Limiter

The saturated core SCFCL consists of an iron core that contains a dc bias.

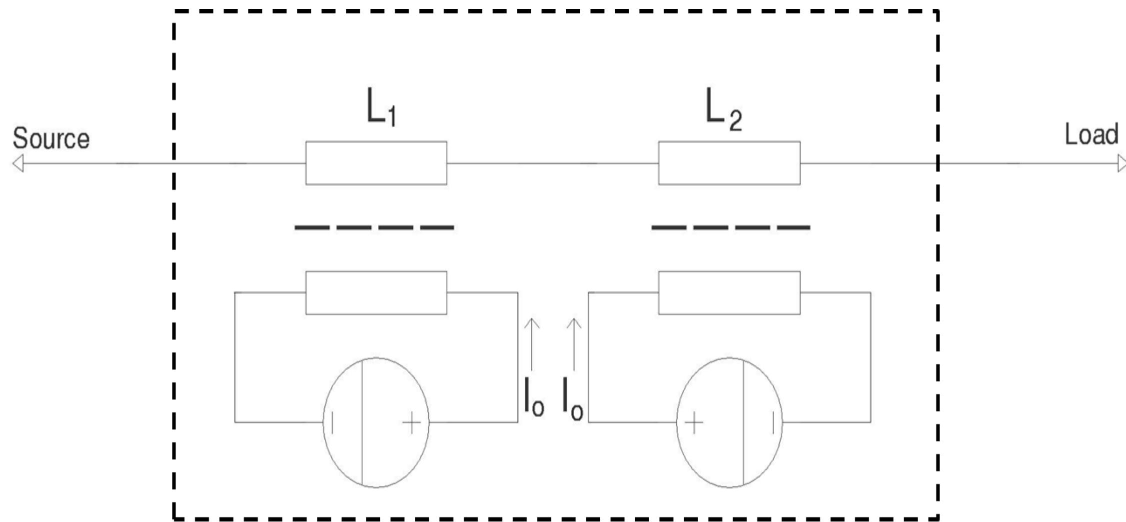


Fig. 2.5. Saturated core SCFCL.

It takes advantage of the fact that the impedance of an inductor is much different when the core is saturated in comparison to normal conditions. The direct current bias is used establish to a dc current, labeled as I_o, to keep the core in saturation through the use of superconducting cables.

Since the core of the inductor is in saturation, the overall impedance of the inductor under these conditions is low. The ac line current value is small enough to keep the core in saturation. Under fault conditions, the core is driven out of saturation by the large alternating current of the system. As a result, the inductance increases and the current is limited [24]. The superconductor does not undergo quenching in this type of SCFCL. Also, not much superconducting cable is needed. This could keep cost down and also reduce cryogenic requirements. A disadvantage is that two of the inductor configurations are needed for each phase in order to provide current limiting in both directions. As a result, the size can become a problem for this configuration as well.

2.2.5 Flux Lock Type Superconducting Fault Current Limiter

Another type of superconducting fault current limiter that has been researched more recently is the flux lock type SCFCL. This type of SCFCL consists of three coils wound around an iron core, along with a high-temperature superconductor (HTS) element, a magnetic field coil, and some type of magnetic field control [32] .

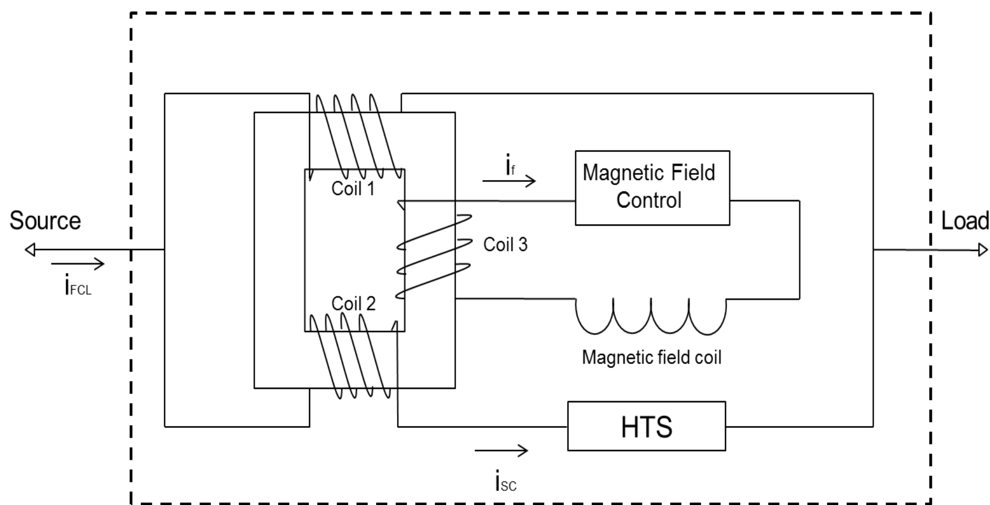


Fig. 2.6. Flux lock type SCFCL configuration.

Two of the coils, Coil 1 and Coil 2, are connected in parallel and wound such that the flux of each counteracts the other during normal operating conditions. The voltage across all of the

coils, as well as the HTS element, is zero. During a fault the resistance of the HTS rapidly increases and voltages are induced across Coils 1 and 2. This in turn leads to current limitation during the fault conditions. Since a voltage is now induced across all three coils, including Coil 3, the magnetic field control can be used to apply an external magnetic field to the HTS element via a field current. This magnetic field control can be in many forms, typically a phase adjusting capacitor, a tap changing element, or even power electronic control [32–34]. The application of the external magnetic field to the HTS will further increase its resistance and provide further current limitation capabilities, leading to a greater percentage of fault current reduction. The advantage in this type of SCFCL lies in the fact that the use of the magnetic field control circuit provides enhanced current limiting beyond what can typically be achieved with other types of SCFCLs. The downside is that this means that there must be additional components included in this type of SCFCL, which increases the overall size and complexity in comparison to the other variations.

2.3 Solid-State Protection Devices in Power Systems

Most traditionalists in the power industry see conventional fault protection devices as serving the purpose for which they are designed, and for this reason they have changed very little since they were first introduced. While there has been some progress in improving the characteristics of conventional circuit breakers, most notably the interruption time, power systems engineers have started to look to power semiconductor devices in order to provide the type of fault protection that will lead to increased grid stability and reliability.

The evolution of power semiconductor devices has led to their inclusions in many aspects of power engineering. In the mid-20th century, power engineers relied on devices such as vacuum tubes and mercury arc devices to perform many of the functions required in high power

systems. These devices proved to be very large, inefficient, and unreliable [35]. In the 1950s and 1960s, power diodes and thyristors became widely available. The diodes were the first semiconductors used in power engineering, but the thyristor provided real change within the industry [36], [37]. It was able to handle large voltages and currents, but, in contrast to the diode, it was also a three-terminal semi-controllable device. It gave power engineers a degree of flexibility that had never been attained before and allowed for more advanced power control methods that could help improve grid stability. Over the years, the characteristics of power semiconductor devices have steadily improved. Not only are the thyristor and diode still among the devices heavily used in power systems, but the insulated gate bipolar transistor (IGBT) and other members of the thyristor family, such as the gate turn-off thyristor (GTO), integrated gate commutated thyristor (IGCT), and the emitter turn-off thyristor (ETO), have been developed and enhanced as well. The superb voltage and current ratings of these devices have led to the development of solid-state protection circuits, most notably solid-state circuit breakers (also called electronic circuit breakers or semiconductor circuit breakers) and solid-state fault current limiters.

Solid-state circuit breakers are able to overcome the deficiencies of conventional circuit breakers through the use of power semiconductor devices. They are certainly revolutionary devices, but the problem is that it is impractical to attempt to replace all conventional circuit breakers. The problem that many power systems engineers currently face is that the replacement of circuit breakers is a costly and time consuming process. Also, the installation of new solid-state circuit breakers would completely change coordination protection schemes, further complicating the process. They are looking for ways to delay the installation of new circuit breakers whose interruption capability has been exceeded due to growing power demands. A

natural progression is to utilize the benefits of solid-state circuit breaker technology and develop solid-state fault current limiters.

Solid-state fault current limiters utilize the same semiconductor device technologies and can also overcome many drawbacks of conventional circuit breakers. SSFCLs can reduce the magnitude of the fault current, and are fast enough to respond before the first peak of the fault current. They can reduce the fault current to acceptable levels that fall within the ratings of existing switchgear, which reduces the amount of wear while extending the operation lifetime. Also, they can be added to existing networks without the need to replace the current protective devices. Some SSFCLs can be used to implement the functionality of solid-state circuit breakers, providing backup protection in the event of conventional circuit breaker failure. Since SSFCLs have such great flexibility, they will be instrumental not only in increasing reliability in future power systems, but in current configurations as well. The research on these types of fault current limiters has been extensive, especially over the past couple of decades. EPRI's early attempts at fault current limiters designs utilized fast acting switches, which were prone to many of the response issues that plague other electromechanical circuit protection devices [14]. Through the advances in semiconductor device development, many of those concepts have been applied to the research of SSFCLs, and many other breakthroughs have been made as well. There are many topologies of solid-state fault current limiters to be described in the following sections.

2.4 Solid-State Fault Current Limiters

2.4.1 Impedance Solid-State Fault Current Limiters

Impedance fault current limiters are the most common type of solid-state fault current limiters. The basic configuration of these protection devices consists of power semiconductor devices in parallel with an impedance element such as a resistor or inductor [38]. A schematic is shown below.

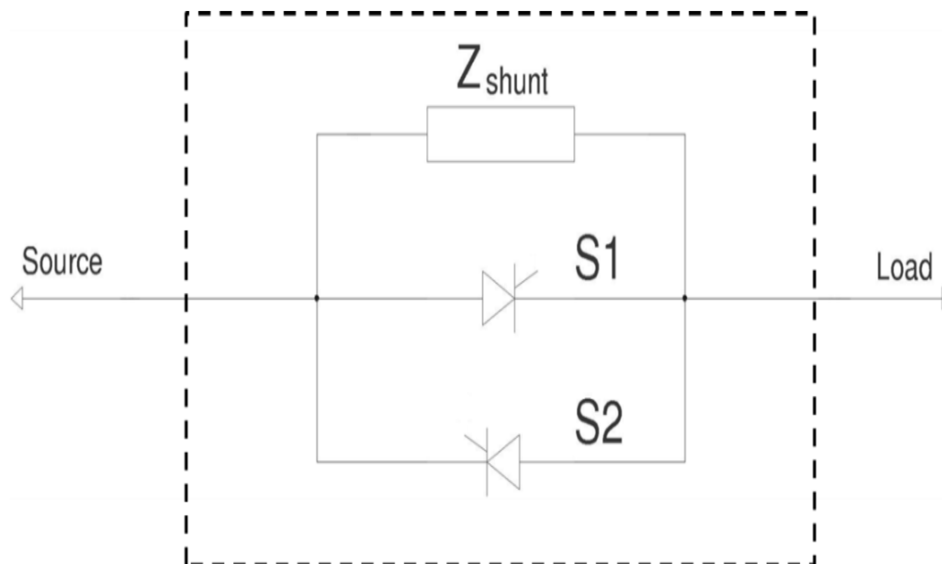


Fig. 2.7. Impedance solid-state fault current limiter.

In most applications, the power semiconductor device will belong to the thyristor family, due to the high current carrying capability of these devices coupled with the relatively low on-state losses. Recently, there have been devices such as IGBTs that have proven to have great potential in high power circuit designs. Since many power devices are unidirectional, an anti-parallel configuration is often implemented in order to conduct both the positive and negative half cycles of the system current during normal operation.

During the positive half cycle, the device designated to carry the positive current (S1) is triggered at the zero crossing of the current. Once the current begins to flow in the negative

direction, the device naturally commutates to the off-state, and the other device that is designated to carry the negative current (S2) is triggered at the zero crossing. This continues as long as no fault current is present in the system. Under normal operating conditions, the impedance of this type of fault current limiter is equal to the on-state resistance of the power semiconductor device.

$$Z_{FCL} = R_{on} \tag{2.1}$$

Often, there is a serial and/or parallel combination of devices in the main conduction path in order to attain the desired voltage and current ratings of the system. In these instances, R_{on} represents the resistance of that configuration, which will be referred to henceforth as the switching position. R_{on} is the resistance of the positive or negative leg of the switching position (not the sum of the two), since only one is conducting at a given time. These legs should have the same number of devices, and hence, equal resistance.

In the event of a fault, the main switching devices S1 and S2 are shut off and the current is diverted to the shunt impedance Z_{shunt}, which limits the fault current to a magnitude much lower than its prospective level. If the main switching device is a thyristor, a commutation circuit has to be utilized in order to turn off the devices. If devices such as GTOs or IGBTs are used, then the turn-off is accomplished via gate control of the device. Because of the fast turn-off of the main devices, overvoltage protection is often necessary and typically implemented using a varistor. During fault conditions, the impedance of this type of fault current limiter is equal to the impedance inserted into the path of the fault current.

$$Z_{FCL} = Z_{shunt} \tag{2.2}$$

The impedance during fault conditions is typically several orders of magnitude larger than it is during normal conditions. The inserted impedance should be sufficiently sized in order to

limit the current to a magnitude that can still be interrupted by downstream protection devices such as circuit breakers and fuses.

There are several advantages to using this type of fault current limiter. The operation is fairly straightforward and reliable. There is little harmonic distortion introduced into the system during fault conditions, and the power quality of the system is preserved. Also, this type of fault current limiter has proved very useful for mitigating voltage sags [39]. There are some disadvantages to the impedance type SSFCL as well. One issue that is common to all SSFCLs is the semiconductor losses during normal operation. In order to keep the junction temperature of these devices to an acceptable level, thermal management is necessary. Active cooling techniques may need to be implemented, and this adds to the overall size, cost, and complexity of the system. Also, the impedance needed to accomplish current limiting, whether it is a resistor or an inductor, is quite large in size. Depending on the fault duration, the power losses in this element can become sizeable as well. Because this impedance is fixed in magnitude, there is no way to control the magnitude of the fault current. Fault current magnitude changes with location and is also dependent on the type of fault, so the impedance has to be sized according to worst-case fault projections. Also, this type of SSFCL has to be used in conjunction with other protection devices with interrupting capabilities.

2.4.2 Bridge Type Solid-State Fault Current Limiters

The bridge-type fault current limiter was previously introduced as a classification of the superconducting fault current limiter. The configuration consists of a diode bridge, an inductor, and a dc bias source. In the case of the superconducting bridge-type limiter, the inductor was actually a superconducting coil that was utilized in order to reduce system losses. Functionally, the bridge-type solid-state limiter is similar to the bridge-type superconducting limiter, and the

schematic is the same as that shown in Fig. 2.3, with the exception that L is not a superconducting coil. The dc bias current is established through the inductor and all diodes in the bridge. As long as the ac line current is lower than the dc bias current, the impedance of the inductor remains small, and the line current is unaffected. Considering the impedance of the inductor to be negligible, the fault current limiter impedance under normal conditions is:

$$Z_{FCL} = 2 \times R_{on} \tag{2.3}$$

If the magnitude of the line current exceeds that of the dc bias current, one of the diode pairs will become reverse biased and cease to conduct. This will lead to an increase in the impedance of the inductor and the current will be limited. Assuming that the impedance of the inductor is much larger than that of the devices, the impedance of the SSFCL then becomes:

$$Z_{FCL} = j\omega L \tag{2.4}$$

There are several variations of the bridge type SSFCL. As hinted in the description of bridge type SCFCLs, some or all of the diodes can be replaced by switches such as thyristors. This will add interruption capability. If a current limiting impedance is placed in parallel to the bridge configuration, the use of controllable switches adds the ability divert the fault current and bypass the bridge [40]. If the controllable switches are used in order to reroute the current through a parallel impedance element, the switches on one side of the bridge can remain gated on in order to provide a freewheeling path for dc current flowing through the inductor. The schematic for this configuration is shown in Fig. 2.8.

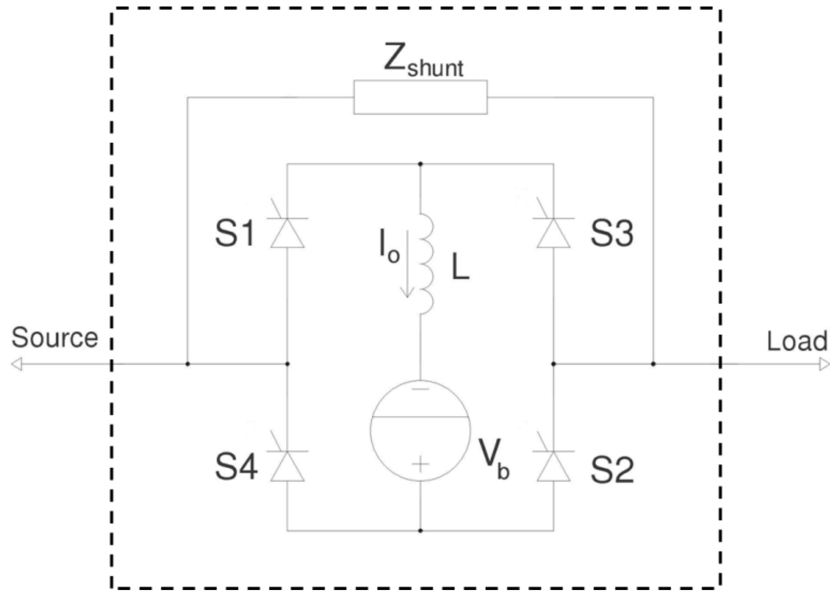


Fig. 2.8. Bridge-type SSFCL with controllable switches and bypass impedance.

Yet another method is to use a single controllable switch in series with the inductor. This can also provide interruption or facilitate the current commutation from the diode bridge to the impedance limiting branch. In this case, a diode is used in parallel with the inductor in order to provide a freewheeling path [40].

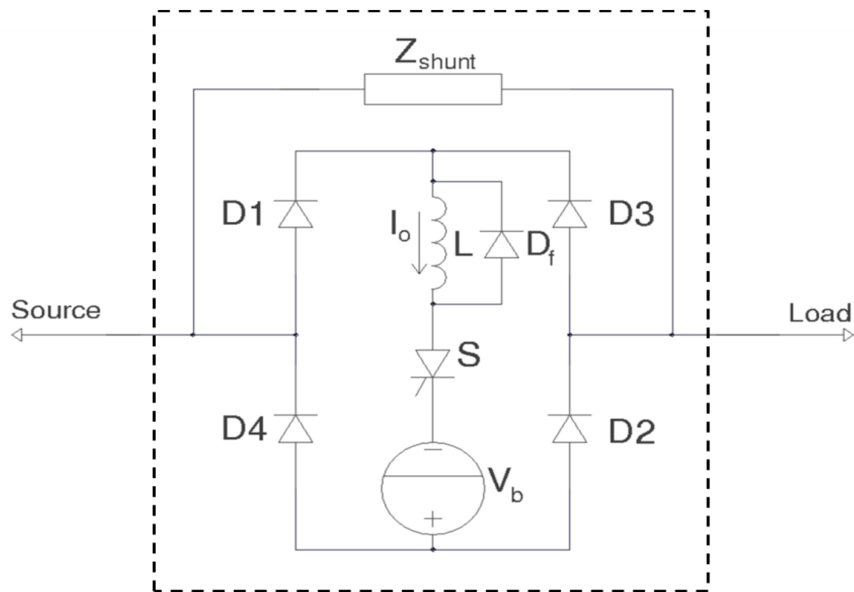


Fig. 2.9. Bridge-type SSFCL with single controllable switch.

The conventional bridge type SSFCL gains its advantage in that there is no fault detection circuitry needed. Also, complexity is reduced due to the fact that no controllable devices are used and thus, no gate drive circuitry is needed. Other types of bridge type limiters add interruption capabilities and reduce the amount of stress on the power semiconductor devices during fault conditions by redirecting the current through the parallel impedance. Problems with bridge type limiters include the fact that during normal operation, current has to flow through multiple power semiconductor devices, as well as the biased inductor. This contributes greatly to losses in the system. The conventional bridge type SSFCL produces distorted waveforms during fault conditions, and the power semiconductor devices have to sustain high current magnitudes for extended periods of time during faults.

2.4.3 Resonant Solid-State Fault Current Limiters

Resonant fault current limiters are among the earliest types of fault current limiters. The early renditions featured a combination of inductors, capacitors, and mechanical switches. Over time power semiconductor devices have been used in order to increase reaction time. The resonant FCL features an L-C circuit that has been tuned such that the resonant frequency is equal to the grid frequency; therefore, the impedance is minimal under normal operating conditions. Under fault conditions, switches are used to either switch in or bypass a circuit element such that the impedance is drastically increased, and the fault current is limited to a reasonable value. There are typically three types of resonant solid-state fault current limiters: series, shunt, and combination.

Series resonant SSFCLs feature the inductor and capacitor in series, with a pair of anti-parallel switches also in parallel with the capacitor element [38].

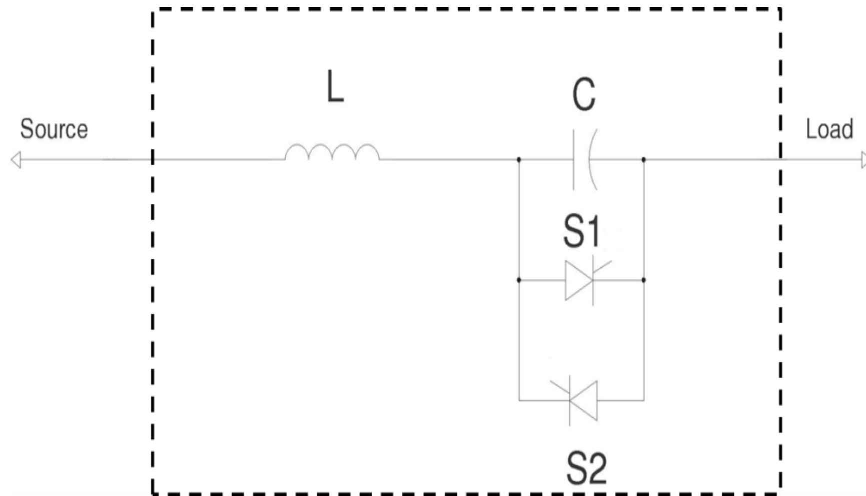


Fig. 2.10. Series resonant SSFCL.

During normal conditions, the switches are gated off, forcing current through the LC circuit. The impedance of the series resonant SSFCL during normal operating conditions is:

$$Z_{FCL} = j\omega L - \frac{j}{\omega C} \tag{2.6}$$

During fault conditions, the switches are turned on and the current bypasses the capacitor. Thus, the impedance during fault conditions is equal to that of the inductor:

$$Z_{FCL} = j\omega L \tag{2.7}$$

Shunt resonant SSFCLs feature a capacitor in parallel with a series combination of an inductor and switches.

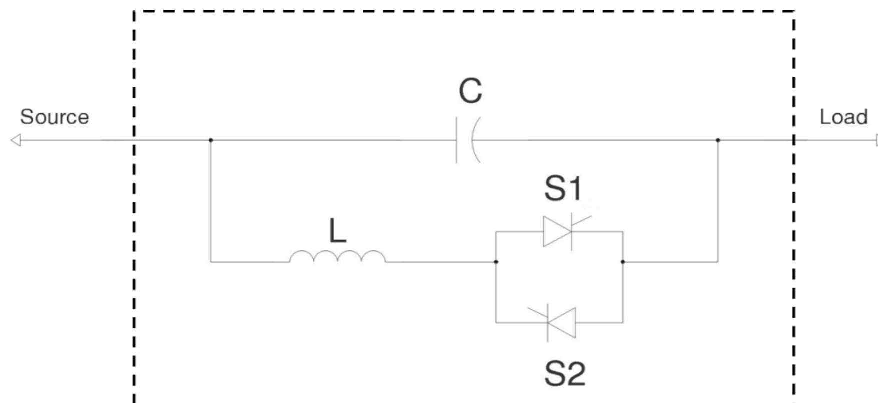


Fig. 2.11. Shunt resonant SSFCL.

The system current flows through the capacitor during normal operation. This capacitor is used in order to provide series compensation for the system as well. The impedance of the system is therefore:

$$Z_{FCL} = \frac{-j}{\omega C} \tag{2.8}$$

Under fault conditions, the switches are gated on and the new impedance of the system becomes:

$$Z_{FCL} = \frac{j\omega L}{1 - \omega^2 LC} \tag{2.9}$$

To a lesser extent, combination resonant SSFCLs have also been explored [38]. These combine the principles of operation of both the series resonant SSFCL and the shunt resonant SSFCL.

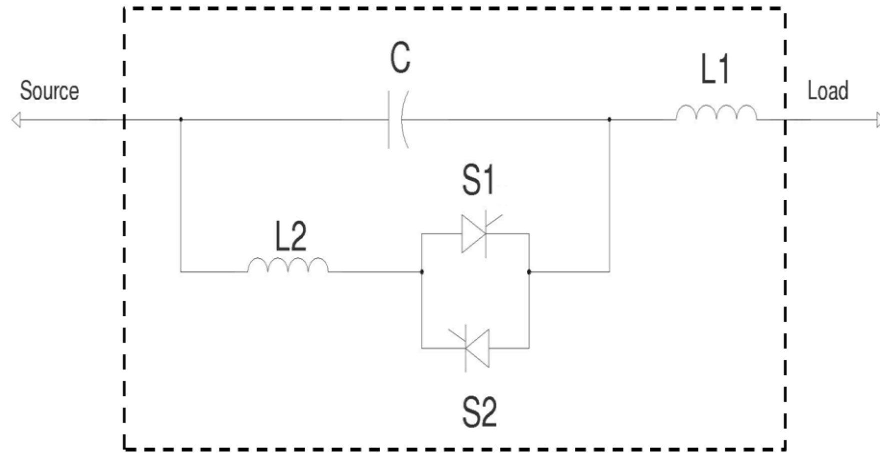


Fig. 2.12. Combination series-shunt resonant SSFCL.

During normal operation, the SSFCL operates as a series tuned resonant circuit, with an impedance equal to:

$$Z_{FCL} = j\omega L_1 - \frac{j}{\omega C} \tag{2.10}$$

During fault conditions, an additional inductance is switched into the circuit and the overall impedance becomes:

$$Z_{FCL} = \frac{j\omega L_2}{1 - \omega^2 L_2 C} + j\omega L_1 \quad (2.11)$$

Among the advantages of resonant solid-state fault current limiters are the fact that some configurations are able to provide series compensation. Also, because the switches are typically gated off during normal operation conditions, then there are no on-state losses due to the power semiconductor losses most of the time. However, these switches do have to be adequately sized to handle the fault current that may flow through them. This type of fault current limiter does not provide adequate voltage sag mitigation during faults and produces switching harmonics.

2.4.4 Programmable Fault Current Limiters

For this section, programmable fault current limiters will be a classification used to described a group of solid-state fault current limiters typically given names such as voltage-controlled fault current limiters, current-controlled fault current limiters, or fault current limiting and interrupting devices [10], [41]-[42]. While the names differ, the function of each is similar. The fault current limiters that have been described have functioned by altering the impedance of the system under fault conditions. The fault current limiters in this class employ switching control of the main power semiconductor devices in order to limit the peak magnitude of the current that is seen during fault conditions.

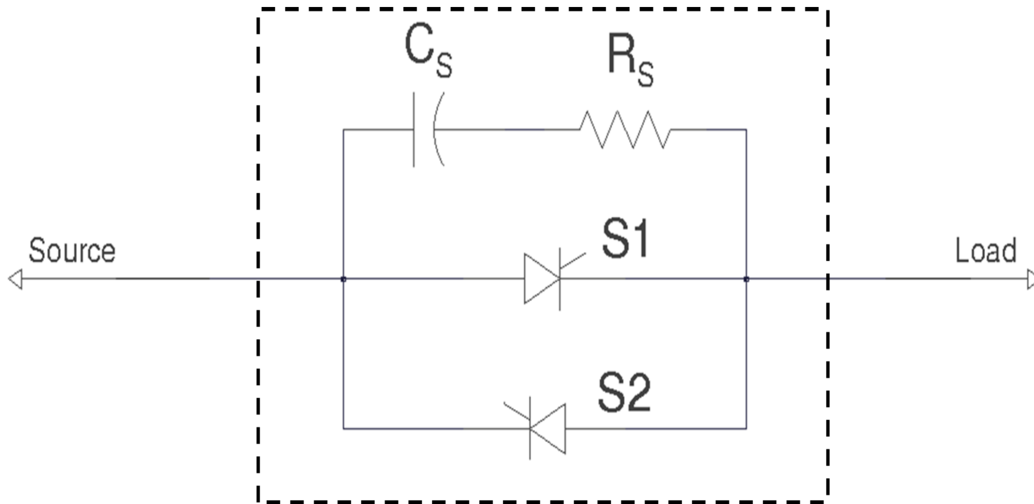


Fig. 2.13. Basic configuration of programmable fault current limiter with main switching devices and snubber circuit.

Most operate using phase angle control in a method made popular in [41]. Phase angle control is a concept that was popularized with controlled rectifiers, which relied on semi-controllable thyristor devices in order to regulate the output voltage of the rectifier to a specific value. There is no current through the device until the gate is triggered at $\omega t = \alpha$, after which the current follows the ac waveform and naturally commutates when the current through the device again falls to zero. During normal operating conditions, the main devices are gated on for the entire duration of the ac cycle in order to allow the current to flow unimpeded. During the fault, phase angle control is implemented in order to control how much current is allowed to flow downstream of the fault current limiter. The delay angle α is selected such as the predetermined current threshold value is not exceeded. This is how the name current-controlled fault current limiter was adopted. The voltage-controlled fault current limiter operates using the same principle, with the idea behind the name being that the phase angle control is used to limit the voltage that is applied to the fault impedance. Fig. 2.14 illustrates the principle of phase angle control and how it is used to limit the fault current. Notice that increasing the delay angle α can further reduce the peak magnitude of the fault current.

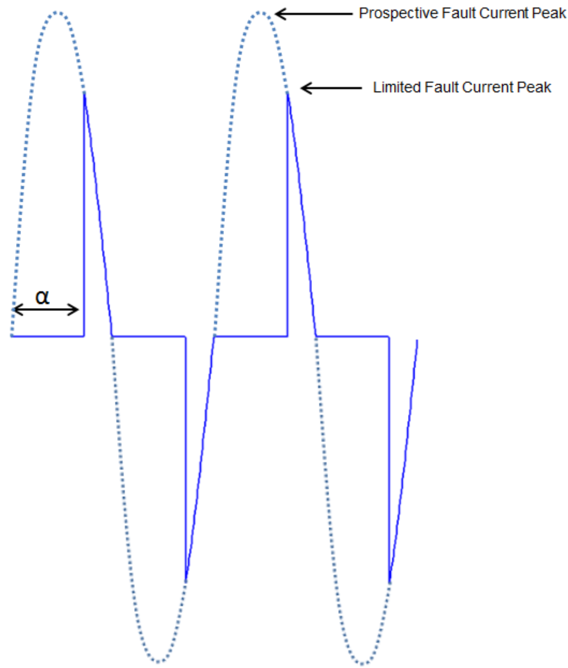


Fig. 2.14. Concept of phase angle control used to limit fault with prospective fault current (dotted line) and actual fault current (solid line).

Other types of fault current controllers utilize a different switching scheme. During phase angle control, each switch is only turned on once per cycle and naturally commutates at the current zero crossing. The switching scheme for the other types include multiple switching instances during each cycle, based on selected minimum and maximum current thresholds. During the fault, the device is switched off when the maximum threshold is reached. Once the current falls to the minimum threshold, the device is gated on again. This process is repeated for the duration of the current cycle until such time as the current reaches its zero crossing [10], [43].

For these types of solid-state fault current limiters, there is no bypass impedance during fault conditions, and consequently there is an inherent interruption capability as well. The main advantage of this type of SSFCL is in the amount of flexibility that it can provide. Microcontroller or digital signal processors are typically used for control, so a number of

advanced functions can be used. Since it does not contain any bypass impedance element (such as impedance SSFCLs) or passives in the main conduction path (such as resonant SSFCLs) the size can be drastically reduced in comparison to other types of fault current limiters. One of the drawbacks of this type of FCL is the waveform distortion that is introduced during fault conditions due to the switching of the main devices. Another problem is that the power semiconductor devices must conduct the initial fault current surge for a quarter cycle of the system fundamental frequency. Also, in order to meet the specification of reducing the fault current before it reaches its peak magnitude during the first cycle, the current must be interrupted. This results in a large overvoltage due to the amount of inductance present in power systems. Snubber circuits and varistors are normally utilized in this type of SSFCL.

2.5 Fault Current Limiter Development

Currently, the development of superconducting fault current limiter prototypes far outpaces that of solid-state fault current limiters. Different superconducting FCL prototypes and demonstrations are detailed in [24], [44], and [45], and recently companies such as Zenergy Power and Nexan Superconductors have moved closer to the commercialization of superconducting FCL technologies. The low losses of superconducting technologies make them extremely attractive, as well as the relatively straightforward operation. Thus far, there have been limited attempts at developing solid-state fault current limiter topologies. There are still major concerns about the long term reliability of semiconductor devices operating under the high voltage and current conditions of distribution networks, as well as the power losses developed during conduction. There are a number of auxiliary systems needed in order to construct functional SSFCL systems, adding to the overall complexity of the system. On the other hand, solid-state fault current limiters provide several distinct advantages that make them a promising

alternative to SCFCLs, such as the ability to perform advanced fault detection algorithms such that erroneous operation is largely avoided. Another benefit is that SSFCLs allow for greater flexibility in the control of the protective device. Furthermore, the reaction time is much quicker than that of a SCFCL. For these reasons, it is expected that solid-state fault current limiter development will be on the rise in the immediate future. Perhaps the most high profile of the SSFCL prototype attempts is the collaborative effort between the Electric Power Research Institute (EPRI) and Silicon Power to develop a 15 kV, 1200 A single phase system [46]. This fault current controller (FCC) was to utilize silicon super gate turn-off thyristors (SGTOs) developed by Silicon Power as the main switching devices. It was an impedance type SSFCL, diverting the current through a parallel inductance in order to provide current limitation. The design for the system was completed, but concerns about the thermal performance and reliability delayed the testing of this prototype, as there were many unforeseen factors to be explored. One of the ways in which solid-state fault current limiter performance and reliability can be greatly improved is through the use of silicon carbide power semiconductor devices. These devices will provide many advantages in the use of fault current limiter systems. The advantages, as well as the potential issues, of developing a silicon carbide based fault current limiter system will be explored in great detail in this dissertation.

CHAPTER 3

SILICON CARBIDE OVERVIEW

3.1 Silicon Carbide Background

3.1.1 The Need for Silicon Carbide Power Devices

As indicated earlier, power semiconductor device technology has developed rapidly since the introduction of high power diodes and thyristors in the middle of the 20th century. Though the performance of these devices were initially modest, over time the processes used to develop and fabricate the devices were refined which resulted in the mass production of devices with extremely high performance characteristics. The family of power semiconductor devices has since grown to include power metal oxide semiconductor field effect transistors (MOSFETs), bipolar junction transistors (BJTs), junction field effect transistors (JFETs), insulated gate bipolar transistors (IGBTs), and a plethora of devices belonging to the thyristor family, such as the gate turn-off thyristor (GTO), integrated gate controlled thyristor (IGCT), MOS-controlled thyristor (MCT), and the emitter turn-off thyristor (ETO). These devices have all been developed using silicon semiconductor technologies. The community of power electronics designers and power systems engineers has become familiar with these devices, and for many applications, are generally pleased with the high voltage and current capabilities of thyristor devices, as well as the potential IGBTs and MOSFETs in high frequency applications. Even though the characteristics of these devices have steadily improved, they have now been pushed to the brink of the theoretical limits of silicon.

Power electronic systems are currently being utilized in everything from data centers and electric vehicles to extreme environment applications, and the performance specifications imposed on these systems are now more stringent than ever. The market is currently demanding

that these systems be smaller, more efficient, faster, and more robust while enduring a wide range of operational conditions. It can easily be seen that yet another revolution in power semiconductor device technology is needed in order to keep up with the emerging trends. Subsequently, the investigation of silicon carbide (SiC) power devices, which has many projected improvements over silicon power devices, has been an area of great focus over the past couple of decades.

3.1.2 Silicon Carbide Structure

Silicon carbide is a compound composed of equal parts of silicon and carbon. The basic unit of SiC consists of a tetrahedron of either four carbon atoms covalently bonded to a silicon atom at the center, or similar arrangement with a carbon atom surrounded by four silicon atoms. The SiC molecule has a layer of silicon atoms bonded with a layer of carbon atoms, in what is referred to as a double layer of Si-C or the Si-C bilayer [47].

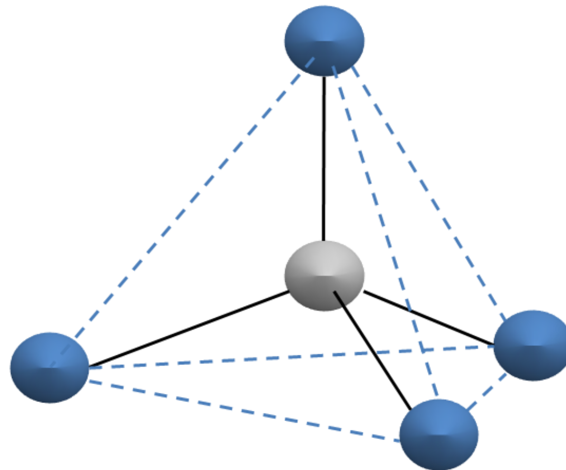


Fig. 3.1. Basic unit of SiC, with silicon (grey) covalently bonded to carbon (blue).

The crystalline structure of SiC is a closely packed stacking of double layers of Si-C. The stacking of the double layers follows three relative positions with respect to the lattice, which are labeled A, B, and C. For a given bilayer, the next bilayer in the sequence can never be the same. For example, a bilayer in the 'A' position can be followed by bilayer 'B' or 'C', but never by

‘A’. By utilizing different stacking sequences of these bilayers, different stable structures of SiC can be made. These are referred to as polytypes of SiC, of which there are currently more than 250 [48]. Polytypes are named in accordance to the stacking sequence. The Ramsdell notation describes each of these polytypes by a number and a letter, in which the number represents the number of bilayers in the stacking sequence, and the letter indicates the crystal structure. There are three crystal structures of SiC: cubic (C), hexagonal (H), and rhombohedral (R). Thereupon, based on the naming convention, 2H-SiC has two double layers in the stacking sequence in the hexagonal structure. The stacking sequence is of this polytype ‘AB’ in regards to the relative positions of the bilayers. SiC in the cubic structure is also referred to as β-SiC, while the hexagonal and rhombohedral types are referred to as α-SiC [49].

The most common polytypes of silicon carbide are 3C-SiC (stacking sequence ABC), 4H-SiC (ABCB – though denoted in some sources as ABAC), 6H-SiC (ABCACB), and 15R-SiC (ABACBCACBABCBAC) [50], [51]. It should be noted that 3C-SiC is the only polytype with the cubic structure. Each polytype differs from the others in regards to its properties. While 6H-SiC is the most common type of α-SiC, 4H-SiC is finding the most use in electronics applications. The stacking sequences are shown in Fig. 3.2.

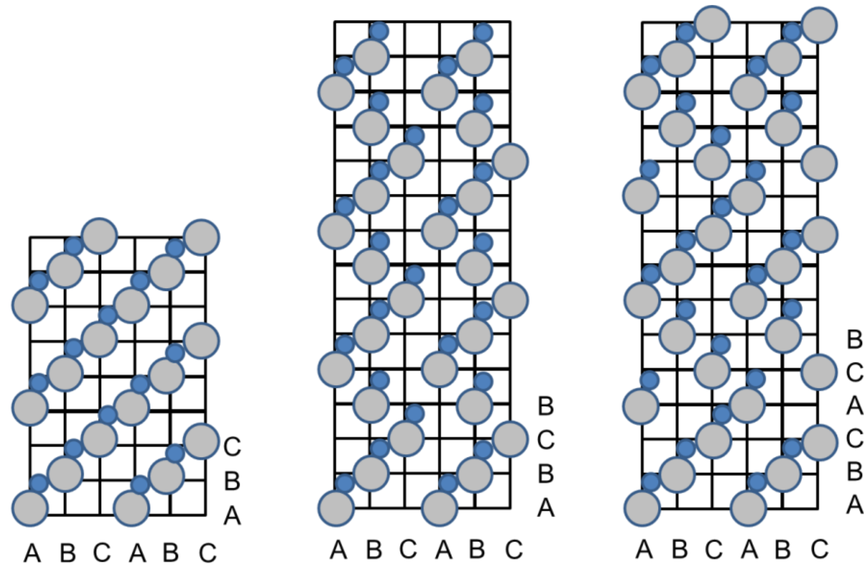


Fig. 3.2. Stacking sequences of 3C-SiC, 4H-SiC, and 6H-SiC from [52].

3.1.3 History of Silicon Carbide

The progression of SiC material has been a long one. Though discovered much earlier, it was not until 1907 that the material was first used in an electronic application. It was then that Henry Round produced the first light emitting diode (LED) utilizing a SiC crystal. Fifteen years prior, in 1892, Edward Goodrich Acheson developed a process for the growth of SiC, which was previously difficult to produce. It was many years later in 1955 when a method was developed to produce single SiC crystals by Lely [53]. While this method, appropriately called the Lely method, was successful and produced high quality SiC crystals, these crystals were limited in quantity and unpredictable in size. In 1978, Tairov and Tsvetkov developed a highly controlled method of producing SiC crystals of a specific size and with high yield. This modified Lely method, also referred to as the seeded sublimation technique, opened the doors for wide scale SiC production [54]. The first commercial material become available from Cree Inc. in 1993 and since that time the development of SiC semiconductor devices has been rampant [55].

3.1.4 Issues with Silicon Carbide

SiC has been hampered by material defects such as micropipes and screw dislocations that have directly impacted its performance and yield. Micropipes, which are small holes in the SiC wafers, were a major hindrance in the development of SiC devices. In 1993, micropipe density was at 1000 micropipes per cm^2 and wafer sizes were only one inch. By 2010 the processing had advanced to the point where micropipe density was less than 5 micropipes per cm^2, with some developers even reporting zero micropipe density wafers [56]. Drastic reduction in the amounts of defects led to the introduction of the first commercial SiC device, a Schottky diode, in 2001 by Infineon.

Another one of the major issues of SiC technology is the cost of wafer processing. A few years ago, it was estimated that the average substrate price for SiC power devices was about twelve times that for silicon devices [57]. This has led to the assumption of many that the price of SiC will simply be too expensive for the material to achieve widespread utilization. The high cost is associated with some of the processing problems and defects that continue to plague SiC. Many believe that due to the progress that has already been made in minimizing these problems, they will largely be alleviated over the next couple of decades allowing SiC to be cost competitive with silicon. Also, SiC packaging techniques need to be refined in order to allow for the full exploitation of the material, such as its potential for high temperature and high power operation. Much research has been undertaken in this area, and it is believed that packaging issues will ultimately be resolved.

3.1.5 Characteristics of Silicon Carbide

Silicon carbide has found promise in its use as a wide bandgap (WBG) semiconductor. Wide bandgap semiconductors are those which have a bandgap energy E_g such that [58]:

$$2.0 < E_g < 7.0$$

All semiconductors have an energy bandgap which separates the valence band of the material from the conduction band. The size of the bandgap is the distinguishing characteristic among insulators, semiconductors, and conductors. It gives an indication of the amount of energy which is needed in order to excite bound electrons from the state of low energy known as valence band into the higher energy conduction band in which they are free to move within the atomic lattice of the material. Insulators have large bandgaps, while conductors have none at all. Semiconductors have varying bandgaps that are intermediate between those of insulators and conductors. Those with small bandgaps can have electrons excited into the conduction band by small amounts of energy, while those with larger bandgaps require more. Wide bandgap semiconductors have a number of other advantages over traditional semiconductor materials such as silicon and gallium arsenide (GaAs). In addition to silicon carbide, the class of wide bandgap semiconductors also includes diamond and gallium nitride (GaN). Several key parameters are shown in Table 2.1.

Table 3.1. Physical Properties of Semiconductors from [59].

Property	Symbol	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap (eV)	E_g	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant	ε_r	11.9	13.1	9.66	10.1	9	5.5
Electric Breakdown Field (kV/cm)	E_c	300	400	2500	2200	2000	10000
Electron Mobility (cm^2/V·s)	μ_n	1500	8500	500 80	1000	1250	2200
Hole Mobility (cm^2/V·s)	μ_p	600	400	101	115	850	850
Thermal Conductivity (W/cm·K)	λ	1.5	0.46	4.9	4.9	1.3	22
Saturated Electron Drift Velocity (cm/s)	v_{sat}	1×10^7	1×10^7	2×10^7	2×10^7	2.7×10^7	2.7×10^7

Diamond has the most superior characteristics of the wide bandgap semiconductors, but it is costly and currently plagued with processing problems. Gallium nitride is beginning to be researched extensively for device applications and has shown promise in opto-electronic applications. It has characteristics similar to those of silicon carbide, and better in many cases, although its thermal conductivity is much lower. Silicon carbide is by far the most mature of the wide bandgap materials and for this reason has been the most widely used in electronics applications [59].

The parameters of Table 3.1 have many impacts on the device performance. It can clearly be seen that for silicon carbide, the bandgap, electric breakdown field, thermal conductivity, and

saturated electron drift velocity are all higher than in silicon. The impacts of each of these will be examined.

As a direct result of having higher bandgap, silicon carbide is able to operate at higher temperature. In silicon, which has a bandgap of 1.12 eV, once the temperature exceeds 150°C uncontrolled conduction can occur due to the excitation of electrons in the valence bands into the conduction band by excessive thermal energy. In applications in which the ambient temperature may exceed this level, silicon is no longer a viable option. However, silicon carbide can theoretically reach temperatures of up to 900°C before this uncontrolled conduction occurs [60]. As a result, there is a market for SiC semiconductors in high temperature applications. While uncontrolled conduction can be induced thermally, electrons in a material can be excited from the valence band into the conduction band by other means as well. Radiation is another mechanism by which this can occur. This radiation can be in the form of cosmic rays, gamma rays, or high speed photons, depending on the application. The large bandgap of silicon carbide allows for its classification as a radiation hard material since a large amount of energy due to radiation is required in order for electrons to reach the conduction band.

The electric breakdown field of 4H-SiC is significantly higher than that of silicon. The high electric breakdown field of silicon carbide equates to a number of distinct advantages. One of the benefits of high electric breakdown field is that it allows for higher doping levels within the device. According to [61], the doping concentration of the drift region of a unipolar device for a given breakdown voltage is:

$$N_D = \frac{\varepsilon_r E_c^2}{2qBV} \tag{3.1}$$

In this equation, N_D is the doping concentration of the drift region, E_c is the critical electric field, ε_r is the dielectric constant for the semiconductor of choice, q is the charge of an electron,

and BV is breakdown voltage. Because of the higher critical electric field, higher doping can be achieved within the drift region. This higher doping also means that the drift region will be thinner in SiC for a given breakdown voltage, resulting in smaller devices.

If the previous equation is solved for breakdown voltage, the following is obtained:

$$BV = \frac{\varepsilon_r E_c^2}{2qN_D} \tag{3.2}$$

The high critical electric field of silicon carbide means that it has a higher breakdown voltage than a silicon device for the same doping concentration. The specific resistance of the drift region is also related to the critical electric field [61]:

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_r \mu_n E_c^3} \tag{3.3}$$

From this equation it can be seen that for a given breakdown voltage, it can be expected that the on-resistance of the silicon carbide device will be much lower than a comparable silicon device.

As shown in Table 3.1, the saturation drift velocity of 4H-SiC is twice that of silicon. The high saturation drift velocity of silicon carbide gives an indication of how quickly charge in the drift region can be removed. The rate of this charge removal is correlated to the maximum switching frequency of the device; therefore, because this parameter is much higher in silicon carbide, the maximum switching frequency is much higher in devices developed using this material in comparison to silicon. The high saturation drift velocity also means that the reverse recovery time is much lower in silicon carbide materials [62]. Lastly, the high value of this parameter will reportedly allow for a higher theoretical current density in silicon carbide devices in comparison to what can be achieved in silicon. It is reported that the maximum current density in some SiC dies can be higher than 300 A/cm^2 [63].

The thermal conductivity λ of a material gives an indication of how easily heat is removed from the material. The heat generated in the device during operation can be more readily transferred to the ambient in silicon carbide due to its high thermal conductivity. This is indicated by the junction-to-case thermal resistance $R_{th\text{-}jc}$ with respect to the device length d and area A which is given in [64]:

$$R_{th-jc} = \frac{d}{\lambda A} \tag{3.4}$$

The higher thermal conductivity produces slower thermal buildup in the device and allows for operation at higher junction temperatures. The net effect is that the thermal management used for the devices, whether it is in the form of heat sinks or active cooling techniques, can be much smaller. This, in turn, leads to smaller overall footprint of a system that utilizes silicon carbide devices.

3.2 Silicon Carbide Devices and Applications

3.2.1 Silicon Carbide Power Devices

Since the introduction of the first commercial silicon carbide wafers, development of SiC based power semiconductors has been evolving at a rapid pace. Silicon carbide technology has been used to develop many of the semiconductor devices that have gained prevalence through the use of silicon; SiC MOSFETs, JFETs, BJTs, thyristors, GTOs, diodes, and IGBTs have all been demonstrated successfully and some have even been commercialized.

As noted before, the first commercial SiC Schottky diode was introduced in 2001, and since that point many more have been developed. They are now available with voltage ratings up to 1700 V [65]. SiC Schottky diodes have no reverse recovery, which has proven to drastically decrease switching losses and improve overall efficiency in converter applications even though the devices are typically paired with silicon switches such as IGBTs. SiC PiN diodes are not as

fast as Schottky devices, but they are suited for use in high voltage applications above 10 kV and will exhibit much lower on-resistance than Schottky diodes.

The progression in SiC switching devices has been such that SiC MOSFETs have been demonstrated up to 10 kV and 10 A [66]. It is anticipated that SiC MOSFETs will be competitive with silicon IGBTs in applications where a switching frequency of over 5 kHz is required. While there have been some concerns about the long-term operation of SiC MOSFETs due to threshold voltage variation with temperature and gate oxide reliability, these devices have shown a great deal of promise [67]. In early 2011, Cree, Inc. was able to overcome many of these issues when they introduced the world's first commercial SiC MOSFET, rated at 1200 V and roughly 33 A [68]. JFETs have also been widely utilized in SiC. Even though they offer good performance characteristics, the main cause of hesitancy towards the use of this device has been its classification as a normally-on device. To combat this issue, SemiSouth has developed a normally-off SiC JFET structure [69]. This structure is definitely more attractive for electronics applications. In addition, a number of other SiC JFET devices have been developed commercially by this company with blocking voltages up to 1700 V.

Consideration for the use of SiC BJTs has been hindered by relatively low current gain that would require complex gate drive circuits, since a base current is required at all times for BJT operation. SiC BJTs otherwise have excellent switching characteristics, high temperature operation, and robustness. They, and other bipolar silicon carbide devices, are subject to voltage degradation of the on-state voltage. This is a gradual increase in the on-state voltage of the device after sustained operation due to defects known as basal plane dislocations [70]. This is an issue that continues to be dealt with in bipolar SiC devices and must be handled appropriately. SiC BJTs have an on-resistance that increases with temperature which equates to a positive

temperature coefficient of on-state resistance [65]. This means that they have relatively good current sharing capabilities, in contrast to what is typically expected of bipolar devices.

Both n-IGBTs and p-IGBTs have been developed, though not commercially. While n-IGBTs are expected to be faster and have better current sharing capabilities, p-IGBTs have higher surge current capabilities and larger safe operating areas. The wide-scale use of n-IGBTs would require the use of p-type substrates, which have been hampered by both high cost and high resistance. Both types of SiC IGBTs have conductivity modulation within the drift layer during operation, contributing to lower on-state resistance, and are expected to be operational at high voltages [71]. SiC IGBTs of up to 12 kV have been demonstrated, with 15 kV devices on the horizon.

SiC thyristors and GTOs are considered to be devices suitable for high voltage applications, where its only competitor will potentially be the SiC IGBT. They both exhibit low on-state losses, good thermal conductivity, and much faster switching speeds than silicon GTOs and thyristors. Most silicon carbide thyristors and GTOs are developed for pulsed circuits in military applications, but the ratings of these devices will prove suitable for power applications as well. Of course, the main drawback of the SiC thyristor is its lack of turn-off capability via the gate. SiC GTOs have turn-off capabilities, but require a relatively large gate current for this to occur. Most SiC thyristors and GTOs are p-type devices, as n-type devices will require the same p-type substrates that are necessary for n-IGBTs. To date, Cree has demonstrated a 9 kV GTO with excellent pulse current capabilities (3 kA for 1 ms) and GeneSiC was awarded an R&D 100 award for their 6.5 kV, 80 A SiC thyristor capable of operating at frequencies in excess of 5 kHz [72]. The ratings and characteristics of these devices to this point have been impressive, but it is

expected that these will continue to improve in the future. A projected roadmap for the ratings of major SiC devices is presented in the figure below.

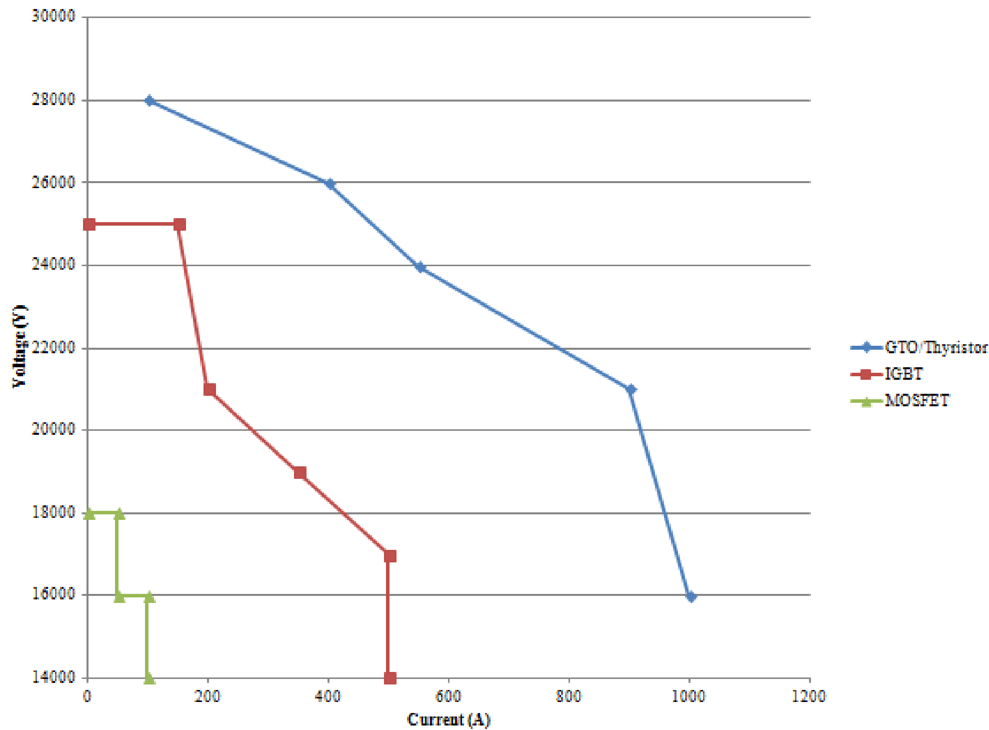


Fig. 3.3. Anticipated device ratings for SiC devices from [66], [73].

3.2.2 Silicon Carbide Applications

Due to the advantages that silicon carbide offers over conventional silicon, the market for silicon carbide devices will be in a number of specialty areas. Applications in high temperature or extreme environments, as well as those requiring high frequency and/or high power will all benefit from the inclusion of silicon carbide devices. This is not just a case of replacing silicon devices with those developed in SiC, but an opportunity for full-scale system redesign that allows for higher efficiency, more robustness, and overall smaller costs and volume than what has previously been achieved. In many cases, the inclusion of SiC allows for the development of systems that were impossible to implement practically at some point.

For extreme environment applications, (i.e. automotive, aerospace, and deep well drilling), ambient operating temperatures for electronics may easily exceed 300°C. Silicon technology is typically restricted to operation at temperatures of less than 125°C. This means that when silicon sensors and control electronics are used in these applications, they often must be located in separate parts of the system or be subjected to aggressive active cooling requirements. If located in a distant part of the system, they often must be interfaced using long wires and interconnections that can add undesirable parasitics that can have an adverse impact on critical operations. Active cooling systems are quite sizeable and can contribute handsomely to the size and cost. Silicon-on-insulator (SOI) technology has been used in applications up to 300°C, but above this temperature silicon carbide is the viable alternative. There have been several demonstrations of silicon carbide sensors and components for control electronics at high temperatures for use in such applications.

SiC has even been demonstrated in integrated circuit (IC) technology. This is any area which is currently strongly dominated by silicon CMOS technology. However, the leakage current of the MOS devices, as well as the stability of the gate oxide, becomes disadvantageous at high temperature. Unfortunately, the gate oxide issue still remains when implementing ICs in SiC. In spite of this setback, researchers have still managed to demonstrate many SiC integrated circuits, often utilizing JFETs or even SiC BJTs in transistor-transistor logic (TTL) circuits [74]–[77]. SiC CMOS circuits have been demonstrated, but the technologies utilizing JFETS and BJTs are the most promising due to the fact that they only rely on p-n junctions and do not have the oxide issues of MOS devices. Also, for integrated circuit use, 6H-SiC has been the material of choice due to its superior behavior at high temperature in comparison to 4H-SiC.

Beyond these uses, SiC is making its way into many other electronics systems, including wireless sensors and microelectromechanical systems (MEMS) [78]. In each case, SiC is expected to bring a number of distinct advantages on a system level that would be attractive to both circuit designers and consumers. Nevertheless, the most effective and widely anticipated use of SiC will be in power electronics applications.

3.2.3 SiC in Power Electronics

Below 600 V, the benefits of including SiC devices in power electronics systems are few, and they are not widely believed to supplant silicon MOSFETs and IGBTs for these applications. On the other hand, as the voltage of the application increases, the reduced on-resistance, high thermal conductivity, and higher switching frequency offered by the devices can prove to be drastic.

In power converters, the inclusion of SiC devices will result in a number of distinct advantages. Due to the low reverse recovery that is expected of the devices, they will be able to operate at much higher switching frequency. The net effect is that the passives associated with the output filter of the system can be drastically reduced in size, which will contribute significantly to a smaller system volume and weight and lower overall cost [79], [80]. This will be critical in applications requiring grid-connected converters, where the output filter will be necessary. The lower reverse recovery can also lead to the elimination of snubber circuits in many applications, leading to a further decrease in size and cost. Also, due to the higher temperature operation and better thermal conductivity offered by SiC power devices in comparison to their silicon counterparts, the thermal management system requirements can also be reduced. This will lead to a reduction in the size of heatsinks associated with the power semiconductor devices. This will also mean less stringent active cooling specifications, and

possibly even the replacement of such a system with conventional or forced air heatsinks if the switch is made from silicon devices to silicon carbide. Added to this is the fact that SiC devices are expected to have both reduced conduction losses due to lower on-resistance, and less switching losses due to the faster switching times. Thus, the efficiency of a SiC power converter is expected to be much better than that of an equivalent system implemented using silicon devices [80].

Silicon carbide devices will have ratings that far exceed those of silicon devices, allowing for the use of fewer devices in power electronics systems. The higher voltage and current ratings will lead to the use of fewer devices in series or parallel in order to achieve desired system ratings. From a power electronic circuit designer's perspective, the reduced number of devices will result in less complex switching positions and power modules, which in turn lead to less complex auxiliary systems (i.e. gate drivers). The overall impact is an increase in the overall reliability of the system. The compound effect of SiC on power electronics systems will allow for its inclusion in a wide variety of unique high power applications. The converters included in electric vehicle drivetrains will be more efficient, more stable, smaller, lighter, and more reliable under the operating conditions that will be encountered within the car. This will eventually lead to lower costs for the manufacturer, which in turn will be passed on to the consumer. SiC is being heavily investigated for wind generation systems, where similar converter advantages will lead to lower operating costs and higher net energy production than what can currently be attained [81]. The use of SiC in a solid-state fault current limiter system will allow for the development of fault current limiter that has nearly ideal characteristics, and the advantages of such a system will be fully investigated in this dissertation.

3.3 The Use of Silicon Carbide in Solid-State Fault Current Limiters

In order to properly assess the advantages of using silicon carbide power semiconductor devices in SSFCLs, one should refer to the list of characteristics of an ideal fault current limiter device. In particular, the impact of silicon carbide would be greatest in regards to the overall losses of the SSFCL, the response of the SSFCL to fault currents, and in increasing the overall reliability of the system. A quick examination of the benefits of a SiC SSFCL follows.

SSFCLs will be heavily utilized in power distribution systems, in which the voltage ratings can range anywhere from 2.4 kV to 69 kV. The 15 kV distribution class is the most prevalent distribution class in the United States, and the nominal current in these systems is typically in the range of 600 A [82], [83] . The superior ratings of SiC power devices will make them more acceptable for use in these systems. Due to the fact that SiC power devices are expected to have much higher voltage ratings (and theoretically, much higher current ratings as well) the number of devices needed to construct a switching position for an SSFCL will be much lower than the number of silicon devices that would be needed. The net effect of this is twofold: the losses and complexity of the system are both decreased. There will be less SiC devices connected in series than silicon devices for a given voltage rating. Although a SiC power device has a higher on-state voltage drop than a similar silicon device, more of these silicon devices will be required at the voltage ratings encountered in power distribution systems. This will make the on-state voltage drop, and consequently the total conduction losses, of the entire switching position higher than in the case with SiC devices.

Fewer devices in series will also simplify gate drive requirements, voltage sharing networks, and snubber circuit specifications. This will reduce the complexity of the overall system, and

will also reduce the cost of many of these auxiliary systems. The use of SiC will eventually lead to fewer devices in parallel, which will also increase the overall reliability of the system.

The fast switching times of SiC power devices will lead to the limitation and clearing of fault currents much more quickly than with conventional devices. In FCL applications, the fault current needs to be limited within a quarter of a cycle, before reaching its peak magnitude. This includes not only the time that it takes for the semiconductor device to turn-off, but the total time that it takes for the fault to be detected and for the appropriate control methods to be implemented. The fast switching time of SiC power devices will be extremely useful in both meeting this specification and in mitigating the fault current before it reaches a dangerous level.

The superior thermal conductivity of SiC and its ability to operate in higher temperature environments will also serve well in the SSFCL application. Due to the high voltage and current ratings typically seen in power distribution systems, active cooling techniques would likely need to be utilized in order to keep the junction temperature of the device in an allowable range. This system could add greatly to the overall size and cost of the system, while adding yet another set of components that require frequent maintenance to the system. Using SiC would allow for much less stringent thermal management requirements. The footprint and weight of the SSFCL system is of extreme importance, since in many cases it will be located in an area where space is critical. Typically, switchgear and transformers for power distribution systems are located in enclosures of a specific size. It is of great importance to minimize the overall volume of the SSFCL as much as possible if the goal is to allow for it to be contained within one of these standard containers. Moreover, the temperature inside these enclosures can elevate quickly, and remain that way for extended periods of time. The SiC SSFCL is able to withstand these high temperatures and maintain proper operation more reliably.

The SSFCL will have to handle currents of high magnitude for prolonged periods of time. Even though the current is limited, the let-through current during a fault is higher than the nominal system current in order to allow for the proper operation of relays and other coordinated protection devices. Also, the initial current surge through the device at the onset of the fault will be quite substantial. The failure of power semiconductor devices is usually associated with the rapid and extreme temperature rise within the device when the device is subjected to high stress. During turn-off, the devices in the SSFCL will be subjected to high current and high voltages simultaneously. SiC devices, with the higher ratings and higher thermal capabilities, are simply better suited to handle these conditions. They are robust devices, and will be less susceptible to failure. Also, the fact that the SiC devices switch faster means that they will be subjected to the harsh transients associated with the fault currents for shorter periods of time, increasing the likelihood of continued successful operation of the SSFCL.

Silicon based SSFCLs in power distribution systems would be comprised of power semiconductor devices from the thyristor family. These devices have outstanding on-state characteristics, such as low on-state losses, but suffer from long turn-off times. Also, these current driven devices require complicated gate drive circuitry. This problem is further exasperated in SSFCL systems. The development of SiC power devices could eventually lead to devices like IGBTs being utilized in fault current limiter applications. These devices will have voltage ratings that far exceed those of any silicon device. The ease of control, due to the fact that this is a voltage-controlled device, makes it even more attractive. Also, these devices would still have relatively low losses due to the conductivity modulation in the on-state, and would also have much faster switching times. Based on the roadmaps of SiC devices, the development of these IGBTs is still quite some time away, but they do provide a great deal of promise for future

SSFCL systems. For the immediate future, the SiC GTO is the best device for these SSFCLs, and the design of a system utilizing these devices will be detailed in the following chapter.

CHAPTER 4

SILICON CARBIDE SOLID-STATE FAULT CURRENT LIMITER DESIGN

A SiC voltage-controlled SSFCL prototype was designed for testing at the University of Arkansas National Center for Reliable Electric Power Transmission (NCREPT) facility. The decision was made to implement this topology of SSFCL due to the flexibility it provides, as well as its smaller volume in comparison to the other topologies. The schematic for the SiC SSFCL is shown below.

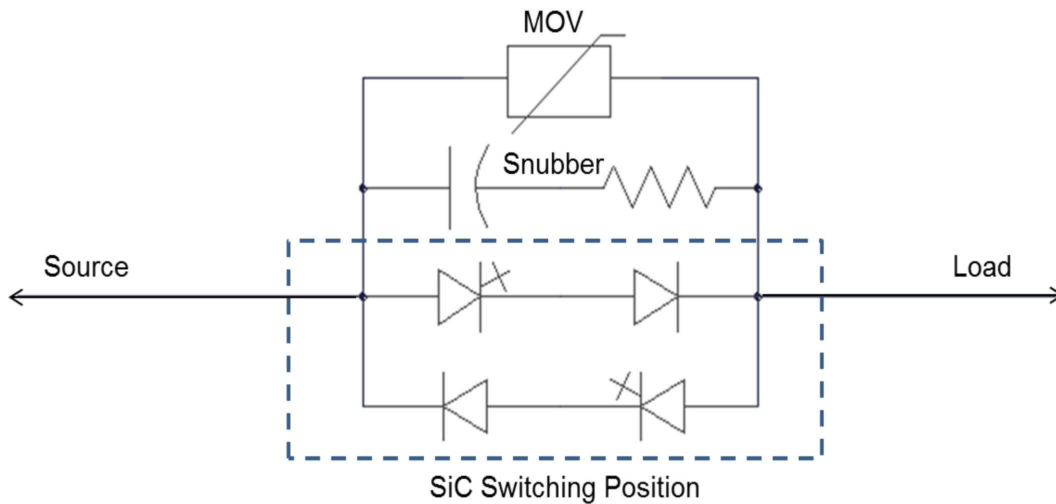


Fig. 4.1. SiC SSFCL schematic.

The development of this prototype was intended to highlight some of the design challenges associated with building a solid-state fault current limiter utilizing SiC power devices. This chapter will detail the different aspects of the SSFCL design, from the implementation of an appropriate switching position to the description of each of the various subsystems and tasks involved in the overall system.

The following is a block diagram of the SiC SSFCL system. This diagram includes the subsystems which needed to be developed for the SiC voltage-controlled SSFCL prototype. The design and implementation of each of these subsystems will be detailed.

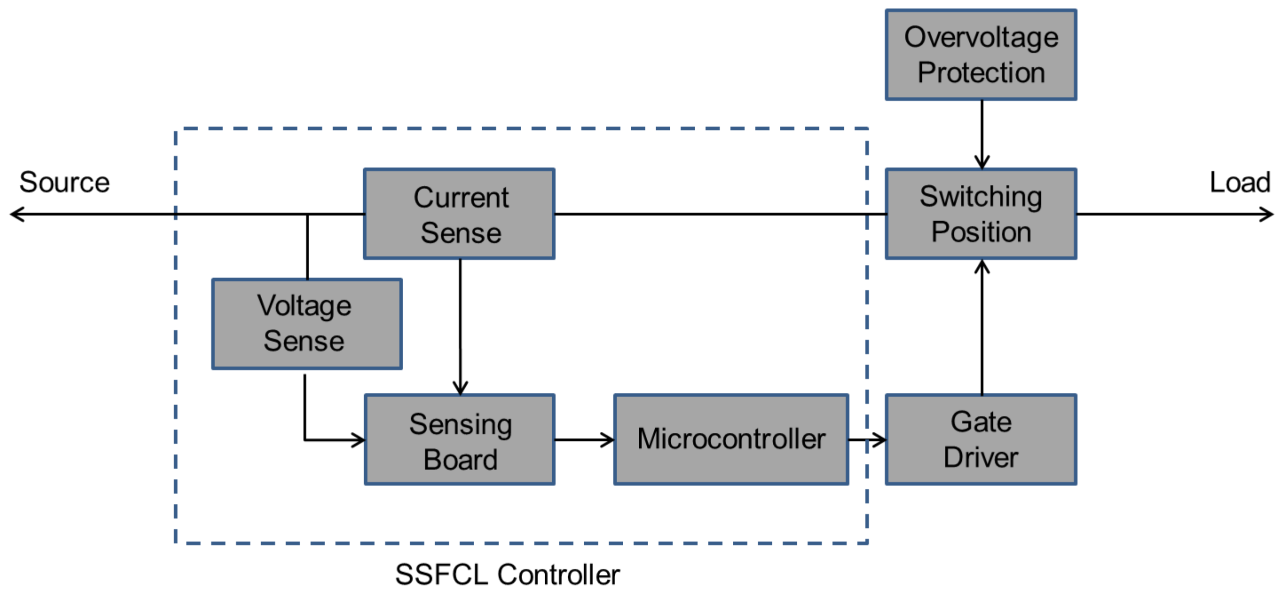


Fig. 4.2. SSFCL block diagram.

4.1 SiC SSFCL Switching Position

4.1.1 Silicon Carbide Super Gate Turn-Off Thyristor

Thyristor type devices are presently considered the optimal devices for applications such as the fault current limiter due to the high voltage and current ratings. The power semiconductor device selected for use in the SiC SSFCL prototype is the SiC Super Gate Turn-Off Thyristor provided by Cree, Inc., also known as the SGTO. This device, like most in the thyristor family, is a three junction device, comprised of four layers that alternate between p-type and n-type doping. The SGTO has the same structure as a conventional GTO, with the difference between the devices being an improved gate structure for the SGTO that allows for faster switching. Though gate turn-off thyristors (GTOs) have the same structure as thyristors, both turn-on and turn-off of the device can occur through the gate terminal. This makes them fully controllable devices, in contrast to thyristors which can be turned on via the gate terminal, but not turned off.

Recall that the devices in the thyristor family are current controlled devices. Operation of the device is best explained by utilizing the two-transistor equivalent circuit. The structure of

thyristors and GTOs consists of two BJTs coupled together. The upper device is a PNP transistor and the lower is a NPN transistor. The base of the PNP BJT is connected to the collector of the NPN, and the collector of the PNP is connected to the base of the NPN. For turn-on, current is provided into the base of the lower NPN. This produces a collector current in the NPN, which also serves as the base current of the PNP. The gate current in the PNP produces a collector current which is the base current for the NPN, further amplifying the base current that initiated the whole process. Thus, the entire thyristor or GTO is turned on through this regenerative process. The equation describing thyristor and GTO current based on the two-transistor equivalent circuit from [61] is shown below.

$$I_A = \frac{\alpha_{NPN} I_G + I_L}{1 - \alpha_{PNP} + \alpha_{NPN}} \quad (4.1)$$

In this equation, I_A is the anode current α_{NPN} is the common base gain of the NPN BJT, α_{PNP} is the common base gain of the PNP BJT, I_G is the gate current and I_L is the leakage current. It can be seen that as long as the sum of the gains of the individual transistors approach unity, there will be substantial current conduction. As such, only a small pulse of current is needed for device turn-on.

Conventional thyristors are typically n-type devices. The current required for device turn-on is supplied via a positive gate-cathode voltage. However, the SiC SGTO is a p-type device, since the n-type substrates needed to fabricate these devices have a much lower resistivity and less processing issues. This makes the structure of the SiC SGTO different than that of the conventional GTO device. The structures and equivalent circuits of both are shown in the figure below (Fig. 4.3).

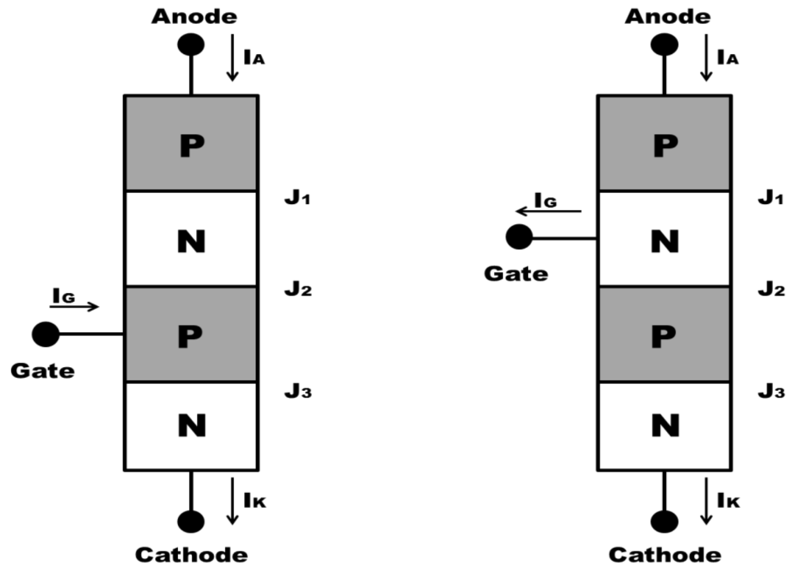


Fig. 4.3. Structure of silicon GTO (left) and SiC GTO (right).

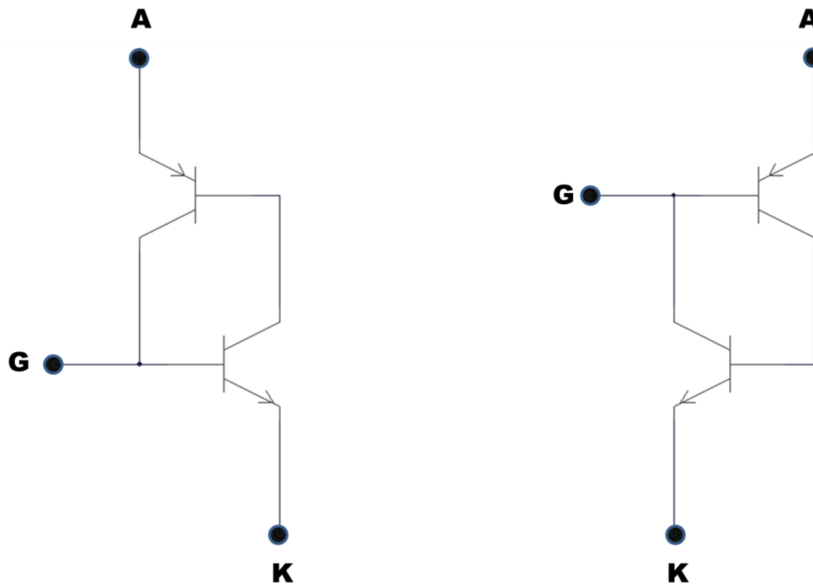


Fig. 4.4. Equivalent circuits of silicon GTO (left) and SiC GTO (right).

The difference in device structure means that the SiC SGTO used for the SSFCL prototype has a positive anode-gate voltage for device turn-on. Control of the device is provided via the upper PNP transistor, which differs from the case in silicon. As such, at device turn-on, current is extracted from the gate. A negative anode-gate current is needed for device turn-off, meaning that current is directed into the gate.

The SiC SGTO used for the SiC SSFCL prototype is rated for 8 kV in terms of breakdown voltage. The die size is 8 mm × 8 mm. Each die is rated at a current density of 100 A/cm^2, meaning that the rated current of these die is approximately 64 A. The cross section of the SiC SGTO is shown below.

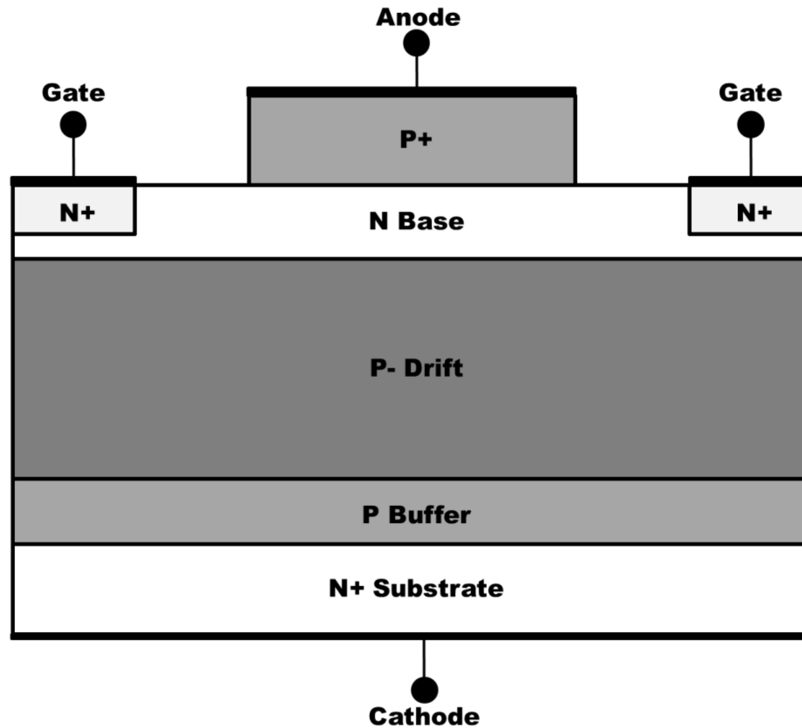


Fig. 4.5. SiC SGTO cross section from [71].

The SGTO is a device optimized for dc pulsed power applications. Thus, it is designed for low on-state voltage drop in the forward direction. It is also capable of blocking significant voltage in the forward direction, as the voltage can be supported by the junction formed by the n-base and p-drift regions. The lightly doped drift region will support the blocking voltage in this direction. On the contrary, the SiC SGTO is incapable of blocking sufficient voltage in the reverse direction. The heavily doped buffer layer, which will reduce the on-state voltage by injecting many carriers into the drift region, cannot support the depletion layer in high voltage applications. In the SSFCL configuration, this is of extreme importance. Therefore, series SiC

PiN diodes will be necessary in the application in order to provide reverse blocking capabilities. The PiN diodes obtained were 1 cm × 1 cm, with a rated blocking voltage of 10 kV and a current rating of 100 A.

The SiC SGTO was characterized for this SSFCL application in [84]. A summary of some of the device characteristics deemed critical for the SSFCL application are presented in the table below.

Table 4.1. SiC SGTO Characteristics.

Characteristic	Symbol	Value
On-Resistance	R_{on}	12 mΩ
Turn-On Time	t_{on}	7 μs
Turn-Off Time	t_{off}	7 μs
Holding Current	I_H	275 mA
Minimum Gate Current	I_G	35 mA
Turn-Off Gain	β_{off}	1.43

These are characteristics that will be important in designing the switching position and associated circuits. There are several challenges involved in developing a suitable switching position utilizing the SiC SGTOs. First of all, in order to achieve the desired ratings of the system several of these devices have to be operated in parallel. The SiC SGTOs and the SiC diodes both exhibit a negative temperature coefficient of on-state resistance. This means that parallel operation is not straightforward and many different aspects have to be considered. Also, there was no gate driver available for this application. Typically, high power thyristors come with integrated gate drivers in order to minimize the inductance, since current of both high magnitude and high *di/dt* is typically needed for proper device turn-off. Lastly, is the fact that the SiC SGTOs were received as bare die. This means the devices have to be packaged before they can be used in the SiC SSFCL. Since this is a high voltage, high current application

utilizing multiple devices in parallel, the packaging effort needed to build a module for the SiC SSFCL is both extensive and intricate.

4.1.2 Parallel Operation of SiC SGTOs

SiC SGTOs exhibit a negative temperature coefficient (NTC) of on-state resistance at a current density below 300 A/cm^2 [72]. This is typically not an issue at the high current densities encountered in pulsed power applications for which the device was originally designed. For continuous operation the rated value of current density is typically 100 A/cm^2. The NTC at this current density means that as the temperature of the device increases, its on-state resistance decreases. This is undesirable when considering the parallel operation of devices, as the device which has the lowest on-resistance will initially conduct more current than the other devices. This will elevate the junction temperature of the device, which in turn will further decrease its resistance. This feedback process will perpetuate itself and possibly lead to thermal runaway. Thermal runaway will lead to catastrophic failure of the SiC SGTO, and the current that was previously carried by the failed device will have to be redistributed among the remaining devices. This in turn could lead to excess current conduction in each of the devices, which may ultimately lead to the failure of the entire switching position. Great care must be taken in order to ensure proper current sharing in this application.

The negative temperature coefficient of the SiC SGTO is confirmed by the I-V curves of the device over temperature, which is shown in Fig. 4.6.

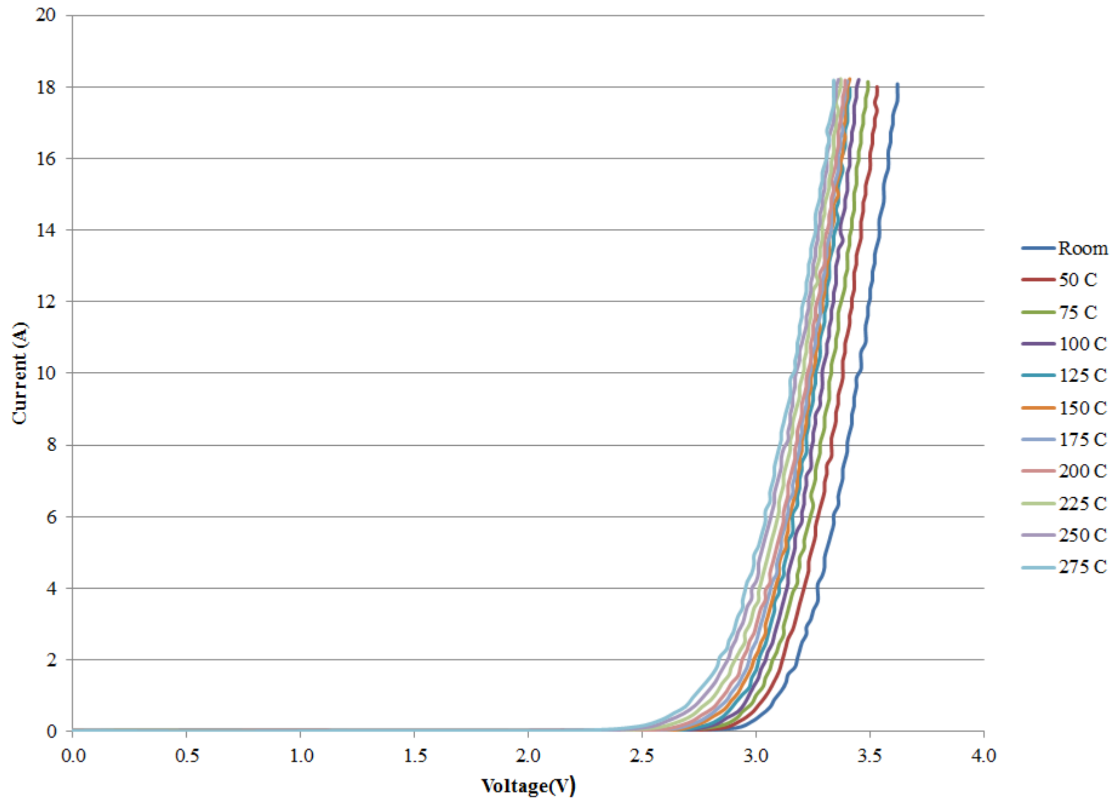


Fig. 4.6. 8 kV SiC SGTO I-V over temperature from [84].

From this graph it can be seen that for a given voltage, the current increases with temperature, which equates to decreasing resistance with temperature. Though the thermal management applied to the device will keep the temperature from varying over such a wide range during operation, it can clearly be seen that this can become problematic. Another issue that makes paralleling of the SiC SGTOs difficult is the wide variance in the device characteristics, even for devices fabricated on the same wafer. Though silicon carbide processing techniques have greatly improved, the yield and consistency of the devices remains much lower than desired. Several methods were investigated as to how to promote current sharing between the paralleled devices. Table 4.2 summarizes some of the approaches that were analyzed.

Table 4.2. Overview of Current Sharing Methods.

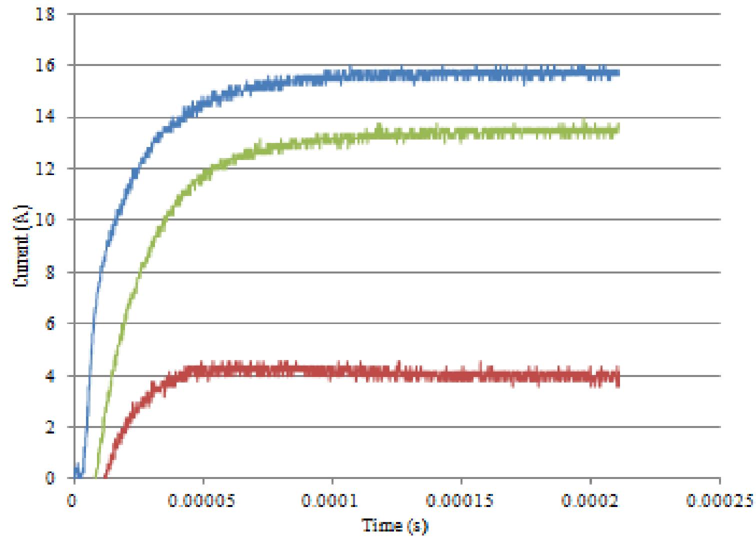
Method	Approach	Advantages	Disadvantages
Using series resistors of the same value	Insert a resistor of the same value in series with each of the SGTOs	Simplicity Promotes current sharing	Power losses in resistors
Using series resistors of the different values	Insert resistors of different values in series with each of the SGTOs	Simplicity	Power losses in resistors Changes in device characteristics over temperature make resistor selection difficult
Skip firing	Turn-off overheated SGTOs for several cycles allowing device to cool	No additional power losses	Requires temperature measurement of each device Requires access to gate and anode of every device Does not promote current sharing
Phase angle control	Turn-off SGTOs with excessive current until beginning of next cycle	No additional power losses	Requires access to gate and anode of every device Does not promote current sharing
Gate control	Alter turn-on times of devices via gate control using impedances or gate drive techniques	Simplicity No additional power losses	Does not promote current sharing

Ultimately, it was decided to use a series resistor of equal value in series with each of the SGTO devices. While this is not the ideal approach, it is the only method that ensured that the current through each SGTO would be fairly equal. Also, other approaches would require a large number of gate drivers in order to be effective. This increases the overall cost and complexity of the system. Using resistors of different values would prove to be a self-defeating process. The

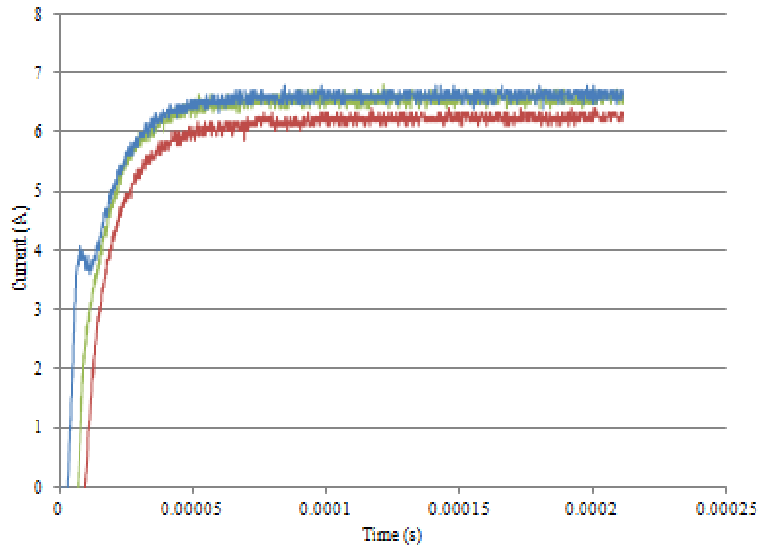
resistors would be selected based on specific operating conditions. However, as indicated by the I-V curves, the device parameters change with temperature which could render the selected resistors useless. The main problem with this method is that in order to be effective, the resistor value has to be on the same scale or much greater than the on-state resistance of the SiC SGTO. This is so any variation in the on-state resistance of the device will represent only a small percentage of the total resistance in the branch.

Paralleling studies for SiC bipolar devices was carried out in [85] in the initial stages of the SiC SSFCL prototype development. SiC thyristors were used for this analysis, but the devices have similar structures to the SiC SGTOs used in the SiC SSFCL prototype so the results will be similar. Fig. 4.7 shows the impact of the current sharing resistors on the SiC bipolar devices.

The resistors used are 8.5 mm × 8.5 mm SiC resistors also provided by Cree, Inc. These resistors actually have a positive temperature coefficient (PTC), exhibiting a resistance of 60 mΩ at 45°C and 200 mΩ at 200°C. Any change in resistance of the SGTO device will be counteracted with an opposing change in resistance, which should keep the current fairly steady in each branch of the parallel configuration. At rated current, the additional losses of each resistor equate to approximately 245 W of additional I^2R power loss. Even if the current is de-rated to 50 A, which is approximately 80% of the rated value, the power losses are 150 W in each resistor. This represents an excessive loss, and while it may be manageable for purposes of building the SiC prototype, the issue of paralleling SiC bipolar devices must be addressed more thoroughly in order for SiC SSFCLs to become a viable commercial possibility.



(a)



(b)

Fig. 4.7. Current through paralleled SiC thyristors (a) without series resistors and (b) with series resistors. Graphs from [85].

4.1.3 SiC SSFCL Power Module

One of the most critical aspects of the design of a SiC SSFCL is the development of adequate power modules. It is desirable to have multiple SiC SGTO and SiC PiN diode die in parallel on the same substrate, but this could present a power packaging challenge. As demonstrated previously, these SiC bipolar devices exhibit a negative temperature coefficient of on-state resistance. In addition to using series resistors, other methods were determined to lead to better current sharing among the devices. Several SiC die attached to the same substrate would ultimately produce thermal sharing among the die, stabilizing the thermal feedback loop and keeping the temperature of each of the die relatively close to others in the module. This is critical in preventing a potential thermal runaway situation. As such, module development for the SiC SSFCL prototype focused on having four to eight SiC devices in a single module, with the goals of attaining individual modules that were rated for operation at 4.16 kV and upwards of 200 A. Not only would the ratings of such a module need to be substantial, but the power dissipated within the module under rated operated conditions, especially when considering the impact of the series resistors, would generate an excessive amount of heat requiring removal.

Ultimately, a SiC SGTO module and a SiC diode module were developed at the University of Arkansas for use in the SiC SSFCL application. These modules consisted of four SiC devices operating in parallel, for maximum current ratings of approximately 200 A and 400 A for the SGTO and diode module, respectively. The modules are shown in the figure below.

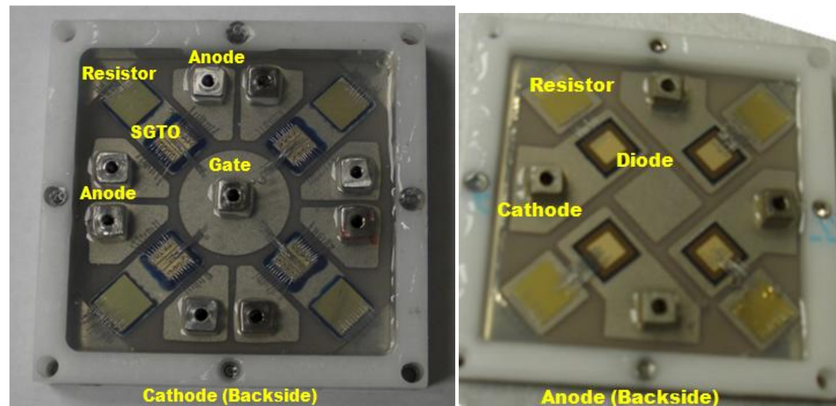


Fig. 4.8. Multi-device SiC SSFCL SGTO module (left) and diode module (right).

Upon examination of the modules there are a few things of note. Each module has an electrically active baseplate. For the SiC SGTO module, this baseplate is the common cathode for the devices in the module; the baseplate is the anode of the SiC diode module. In the SGTO module, there is a common gate connection at the center of the device, as well as individual anode connections. This will allow for individual device evaluation during operation. The current sharing capabilities can be monitored. In the event of a device failure, the module can be configured such that the connections to the damaged device can be removed with minimal impact of the rest of the devices in the module. A similar configuration was developed for the diode module.

Although the SiC modules were developed, it was determined that initial testing should be performed with individual device modules. Concerns about operation with an electrically active cooling plate led to the decision that a secondary design, in which the baseplate of the module was not electrically active, should be implemented for the testing of the SiC SSFCL prototype. Though the use of individual modules would not provide the thermal coupling that is inherent in the aforementioned design, it would still allow for evaluation of the parallel capabilities of the modules under high current conditions, and would minimize the risk involved in testing. The supply of SiC devices available for module development was limited; therefore, testing of the

developed modules with multiple devices would only be carried out after successful testing of the SiC SSFCL using individual device modules. The individual device modules, along with the associated I-V curves, are shown in Figs. 4.9 and 4.10 below. Each module has dimensions of 2.3 in. × 2.2 in. (55.88 mm × 58.42 mm). The modules are limited to a maximum current rating of a single device, which is 64 A and 100 A for the SGTO and diode module, respectively. A direct bond copper (DBC) substrate is used for the power module, and wire bonds are used to establish the connections between the resistors and the SiC devices. The SiC SGTOs are lidded using ThinPak technology developed by Silicon Power Corporation (SPCO). The ThinPak lidding is designed typically used to eliminate the wire bonds within the module, but wire bonds were included in this design in order to reduce the potential for gate-anode shorts caused when using a patterned DBC substrate to connect the gate and anode electrodes using solder paste.

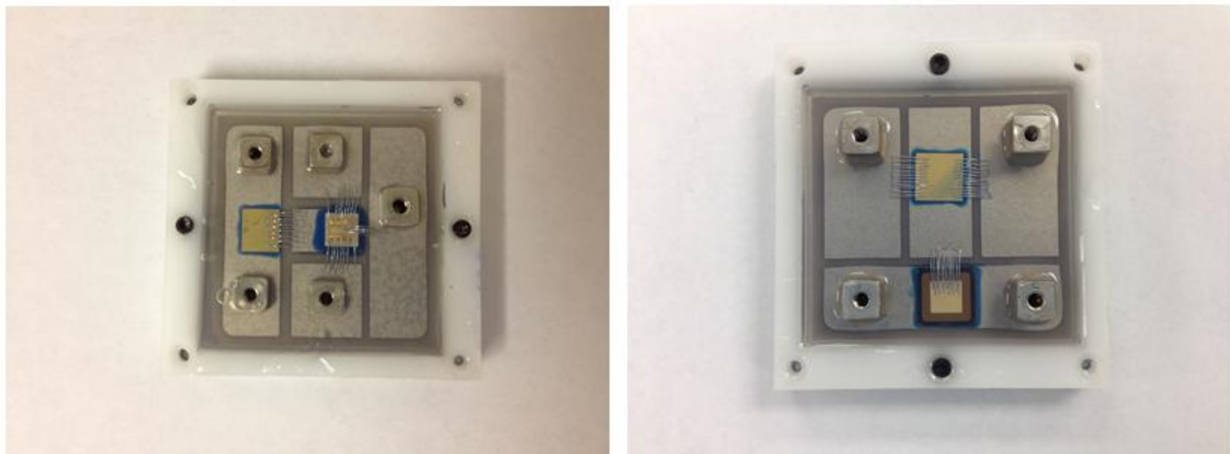


Fig. 4.9. SiC SGTO module (left) and SiC diode module (right).

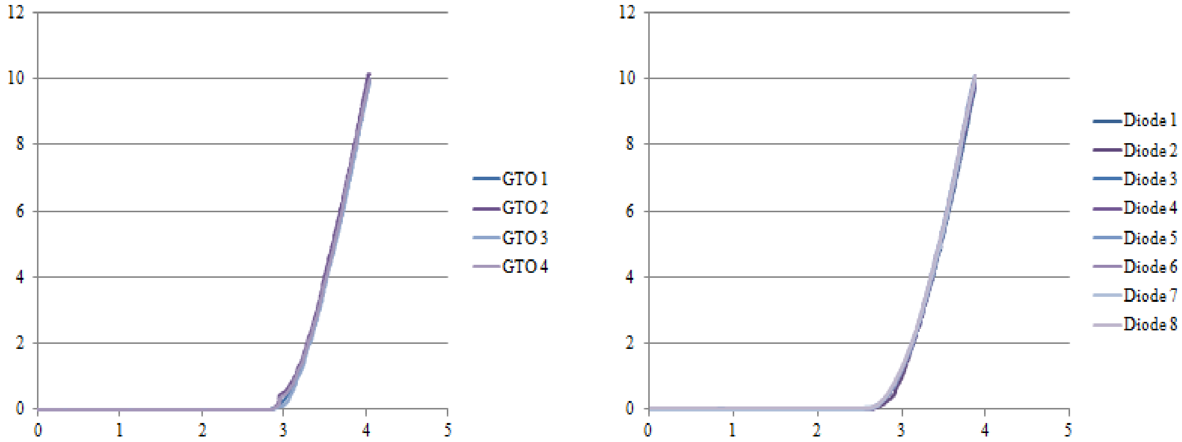


Fig. 4.10. Measured I-V curves for selected SiC SGTO modules (left) and SiC diode modules (right).

The I-V measurements for the SiC SGTO modules yield an on-state resistance of approximately 97 mΩ at room temperature, which would equate to module power losses of 242.5 W during operation at 50 A. The measured on-state resistance of the SiC diode module was found to be roughly 98 mΩ, nearly identical to that of the SiC SGTO module. Each module successfully passed breakdown tests of up to 8 kV.

4.2 Gate Driver for SiC SGTO

The turn-off gain for a GTO device is given as follows:

$$\beta_{off} = \frac{I_A}{I_G} \tag{4.2}$$

As indicated in Table 4.1, the turn-off gain β_{off} for the SiC SGTO is approximately 1.43. Based on the above equation, the gate current required for turn-off of the SiC SGTO was measured to be roughly 70% of the anode-cathode current through the device. This is much higher than the typical ratio for silicon GTOs, which typically have a turn-off gain of more than 3. Moreover, it is highly realistic that the turn-off gain will approach unity for many of the devices, meaning the amount of gate current needed is approximately equal to the anode-cathode current.

For an application such as the fault current limiter, the task of developing of suitable gate driver becomes challenging. Not only does a large magnitude of current need to be interrupted before a quarter of a cycle at the ac mains frequency, but the gate drive must have isolation well beyond the nominal voltage of the distribution system. Another point of concern is that the gate of the SiC SGTO is referenced to the anode, which is the high side of the device. All of these factors were considered as part of the gate drive design for the SiC SSFCL.

The SiC SSFCL design has nominal ratings of 4.16 kV with an interruption capability of 500 A. As noted in the previous section, several devices would have to be paralleled in order to attain the desired current. This means that multiple devices will be packaged within a single power module. The gate driver must be capable of driving one of the power modules, not just a single device. Multiple gate drivers would suffer from discrepancies in turn-on times and also the *di/dt* required for device turn-on. A high rate of current rise is required for fast and uniform device turn-off, and it is best to have a single pulse supplying the gate current for all devices. The gate driver would supply roughly 1 A of current during the turn-on period, but it is designed to provide 700 A of current for 100 μs at turn-off for a system with a maximum current of 1000 A. The full design and simulations of the gate driver developed for this application are detailed in [84].

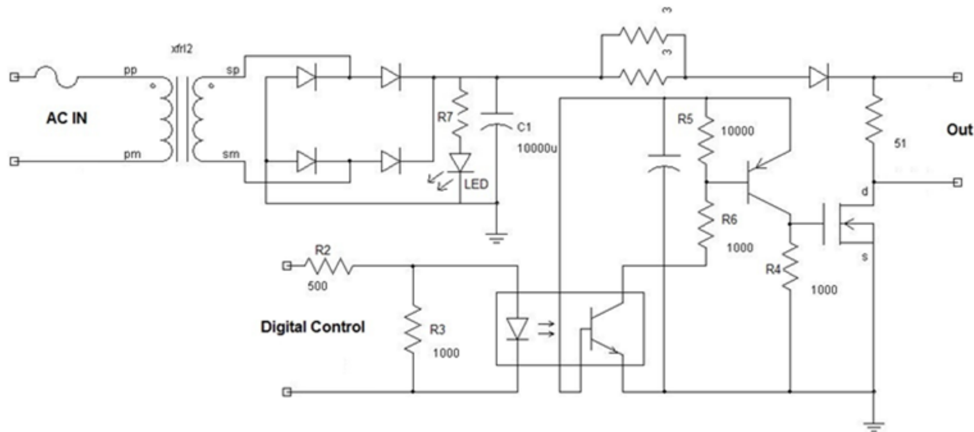


Fig. 4.11. SiC SGTO gate driver circuit schematic from [84].

The schematic for the gate driver is shown in Fig. 4.11. It contains a 120:18 V transformer with 10 kV of voltage isolation. For the SiC SSFCL application, there are actually two gate drivers: one for device turn-on and another for device turn-off. At turn-on, the digital control is used to drive the optocoupler. The optocoupler output is fed into a biasing circuit which controls a power MOSFET. When this power MOSFET is on, a fast rising current pulse is supplied via the 10 mF capacitor at the output of the rectifier bridge. This current is limited at turn-on by the parallel combination of high power resistors. The output terminals of the gate driver are connected anode-gate, with the anode as the positive reference.

The turn-off gate driver is the same, with the exception that the current limiting resistors are removed. Also, the positive reference becomes the gate with respect to the anode. As such, the SGTO will draw the necessary current in order to remove the excess charge that is stored within the drift region the device. A photo of a completed turn-on gate driver is shown in Fig. 4.12.

Fig. 4.12. SiC SGTO turn-on gate driver from [84].

4.3 Snubber Circuit Design

4.3.1 Snubber Considerations and Topology Selection

The inclusion of a snubber circuit for the solid-state fault current limiter is necessary. The selection of the appropriate component values can prove somewhat challenging for this particular application. Snubber circuits are often utilized in order to reduce the stresses to power semiconductor devices in switching applications due to transients at device turn-on and turn-off. For the voltage-controlled solid-state fault current limiter, transients at device turn-off are a significant issue.

Under normal operating conditions, device turn-on is established at what is essentially zero-current. Also, device turn-off during normal conditions is due to natural commutation and occurs when the current of the GTO thyristor falls below the holding current. This is the minimum value of anode-cathode current needed to sustain the device in the on-state. The main switching devices are not subjected to a great deal of stress during normal operating conditions.

There is no repetitive hard switching of devices at an escalated switching frequency, as is the case for power converter applications. For this reason, the snubber circuit in the SSFCL has minimal impact on the circuit during normal operating conditions. As indicated earlier, one of the main requirements of fault current limiters is that the current must be limited within a quarter of a cycle, such that the maximum possible value of the fault current is not seen by the system. In order for this to occur with the chosen topology of the solid-state fault current limiter, the current must be interrupted. Since the magnitude of fault currents can be on the order of tens of kiloamperes and the SiC SSFCL has a worst-case interruption time equivalent to a quarter of a cycle of the fundamental frequency, the main switching devices are subjected to a great deal of stress during this period. The snubber components must be carefully chosen in order to avoid a catastrophic failure.

Another important specification of fault current limiters is the need for minimal overvoltage in the system due to FCL operation. The interruption of the fault current will lead to a large overvoltage value due to the large amount of inductance in power systems coupled with the high magnitude of current that is being interrupted. The overvoltage is directly related to rate of change of current through the inductance upstream of the fault current limiter, since:

$$V = L\frac{di}{dt} \tag{4.3}$$

The snubber circuit is needed in order to reduce the value of this overvoltage as well as the rate of rise of the voltage across the power semiconductor devices. The overvoltage problem is especially complicated for this application. Typically, great care is taken in order to minimize the inductance in circuits in which switching is required. However, there is nothing that can be done to avoid large amounts of inductance within power distribution systems. Furthermore, the use of silicon carbide GTOs can actually contribute to a larger magnitude of overvoltage than

would be achieved with comparable silicon devices due to the fact that the turn-off times are theoretically much faster. This will contribute to a larger value of *di/dt*. The rate of rise of this overvoltage across the device must be managed as well. For thyristor type devices, high values of *dv/dt* across the device can induce currents which can either retrigger the device or lead to the breakover current of the device being exceeded, leading to failure.

An RC (resistor-capacitor) snubber topology was selected for the silicon carbide SSFCL. RCD (resistor-capacitor-diode) snubbers are popular for many switching applications, but they are useful in minimizing the switching losses. Since hard turn-off is infrequent in SSFCL applications, this is of little consequence. Also, RCD snubbers are polarized, meaning that two separate snubbers would be needed for protection against overvoltages in both the forward and reverse directions. Lastly, the diode in the RCD snubber has to be sized to withstand the peak magnitude of current that would flow through the system at turn-off. This would require the use of several diodes in parallel, and add to the overall complexity of the system. RC snubbers are unpolarized, which is ideal for the anti-parallel switches used in SSFCL applications because only one snubber is needed. Consisting of only passive elements, the cost and potential for failure is much lower in comparison to a RCD snubber as well. While the common conception is that RC snubbers are only effective for rate of rise control at device turn-off, they can also effectively reduce the overvoltage. This is due to the fact that after the device is turned off and enters the blocking state, the resulting circuit is essentially a series RLC circuit. The energy that was previously stored in the inductance will be transferred to the capacitance of the snubber, and the resistor and capacitor values can be chosen such that the RLC circuit has a damped response in which the overvoltage is significantly lower than its potential value.

As mentioned previously, the capacitor is charged during turn-off when the energy of the inductance is transferred to the capacitor. This energy is then dissipated in the snubber resistor at the next instance of device turn-on. The energy stored in the capacitor is given by:

$$E_r = \frac{C_s V_C^2}{2} \tag{4.4}$$

In this equation, C_s represents the snubber capacitance, shown for the SiC SSFCL in Fig. 4.1, and V_c represents the peak voltage of the capacitor.

For the SSFCL, the energy stored in the capacitor during turn-off is dissipated in the resistor during the device turn-on. Power is related to energy by the equation:

$$P = \frac{E}{t} \tag{4.5}$$

Using the term for E_r, and considering that the time of dissipation is over a half-cycle of the fundamental frequency, the average resistor power dissipation is:

$$P = \frac{E}{t} = \frac{E_r}{0.5T_{ac}} = C_s V_c^2 f_{ac} \tag{4.6}$$

The large magnitude of voltage in power distribution systems will contribute to much energy being stored in the snubber capacitor and in turn, much power dissipation in the snubber resistor. This equation can be misleading for the SSFCL application, as current interruption does not occur frequently due to natural commutation of the SiC SGTOs during normal operation; as such, there is no energy in the capacitor to be dissipated in the resistor under normal operating conditions.

Another concern for snubber design is the amount of current that will flow through the capacitor-resistor combination when the SSFCL is “open.” During normal operation, the current path is through the lower impedance path of the switching devices. When the devices are not conducting, the low impedance path is through the snubber circuit. This current is of concern

because it is constantly being dissipated in the snubber resistor which could create thermal issues. Also, in a system in which no current is expected to flow, this current through the snubber network could pose a safety concern. During the blocking state, the SiC switching position will block the entire system voltage. Since the snubber network is in parallel with this switching position, the amount of current flow is dictated by the impedance of the snubber network:

$$Z_{snubber} = \frac{1}{j\omega C_s} + R_s \tag{4.7}$$

There are many trade-offs that must be made in snubber network design. As seen in the previous equation, larger values of snubber capacitance contribute to larger current flow when the SSFCL is in the off-state. This leads to higher power dissipation in the snubber resistor. Yet, larger values of snubber capacitance more effectively limit the peak value of the overvoltage that occurs during the device turn-off period. Snubber capacitors are easily one of the most expensive parts of the entire SSFCL system, with the high voltage and energy rating requirements. The snubber resistor must limit the current flow at device turn-on, and the RC constant of the snubber network must be chosen such that it is short compared to the switching period, but long compared the voltage rise time [86]. The fast rise times of the SiC GTOs and the 60 Hz fundamental frequency means that this generally should not be a problem.

4.3.2 Snubber Component Design

The method chosen for the snubber design is a popular method implemented in [87] and further expounded in [88]. While there are many approaches to snubber design, it is commonly accepted that the calculated values will provide a starting point, with the optimum values determined experimentally or through simulation. The approach chosen allows for the calculation of values based on many of the system parameters. It is based on a design procedure

that allows for selecting the capacitance and resistance in order to limit the peak voltage to specified values. For the SiC SSFCL prototype, the peak voltage during turn-off must be limited to a value that is lower than the breakdown voltage of the SiC GTOs. Thus, this is the starting point for the snubber design.

A summary of the design process as outlined in [87] and [88] is presented. In [87], an equivalent circuit for the snubber is presented and Laplace transforms for the current and voltage are derived. From these equations, normalized parameters are developed which become useful in the design of the snubber circuit. The parameter χ is referred to as the initial current factor, such that:

$$\chi = \frac{1}{E}\sqrt{\frac{L}{C}} \tag{4.8}$$

The damping factor is:

$$\zeta = \frac{R}{2\sqrt{L/C}} \tag{4.9}$$

The peak voltage is normalized as a function of both the initial current factor and the damping factor. This equation is plotted as a function of the damping factor with the initial current as a parameter. For any given value of χ there is also a value of ζ which will minimize the peak voltage ratio E_1/E_0. Selecting the value of ζ will lead to a calculation of the capacitor value that will minimize the peak overvoltage value. Using the procedure outlined in [88], the operating conditions and circuit parameters of the circuit can be used in order to determine the appropriate values of the initial current factor χ and the damping factor ζ, which in turn can be used to calculate the snubber capacitor and resistor values.

First, the operating current I_o, voltage E_o, and inductance L_p of the circuit are needed. The SiC SSFCL is designed for ac operation at 4.16 kV_{RMS}. The maximum current for interruption

was planned to be 500 A at this voltage level. The high voltage testing conditions were chosen as the worst case scenario in order to complete the snubber design. The SiC GTOs are rated for 8 kV; this means there is a low tolerance for excessive overvoltage in this test setup. Also, there is significant inductance is this setup due to the presence of transformers. At 2.5 MVA, the transformer rating at the test facility, the maximum allowable current that could be interrupted during this test setup is:

$$I_o = \frac{2.5\ MVA}{\sqrt{3} \times 4160} = 346.9\ A, rms = 490.7\ A, peak \tag{4.10}$$

A value of roughly 500 A was used for I_o in the snubber calculation. Based on the transformer specifications provided by the manufacturer, the inductance of the test setup was determined to be approximately 2 mH. The maximum peak voltage, E_1, was determined to be 8 kV and the peak value of the operating voltage E_o is approximately 5.88 kV. The ratio of E_1/E_0 is:

$$\frac{E_1}{E_0} = \frac{8\ kV}{5.88\ kV} = 1.36 \tag{4.11}$$

Using the graph from [87], repeated in Fig. 4.13, and the previously determined ratio, the damping factor and initial current factor are projected to be 1.6 and 0.45, respectively. The capacitance and resistance values were calculated according to the following equations.

$$C = L_p \left(\frac{I_0}{E\chi_0} \right)^2 = 0.002\ H \left(\frac{500\ A}{5800 \times 0.45} \right)^2 = 285.88\ \mu F \tag{4.12}$$

$$R = 2\zeta_0 \sqrt{\frac{L}{C}} = 2 \times 1.6 \times \sqrt{\frac{0.002\ H}{285.88\ \mu F}} = 8.5\ \Omega \tag{4.13}$$

These values were used as initial values in the simulation of the test setup, which was used to refine the design.

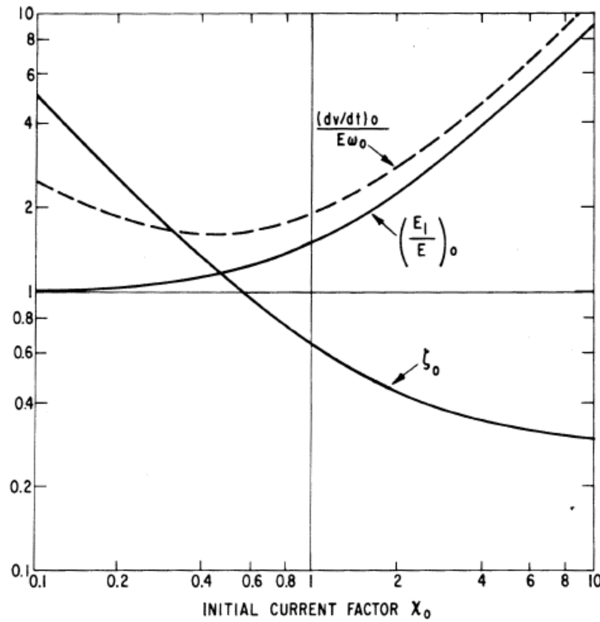


Fig. 4.13. Optimum snubber design parameters for minimum voltage spike from [87].

4.3.3 Snubber Circuit Simulation

The test setup is shown in the schematic in Fig. 4.14. The load is configured for a peak system current of approximately 500 A. The switch is used to emulate the interruption that will occur during SSFCL operation. In the simulation shown in Fig. 4.15, there is an interruption at the negative current peak at approximately t = 13 ms, and the switch is turned on again for a few cycles at around t = 25 ms. Finally, there is another interruption at the positive current peak at t = 55 ms. The switching times of the switch are selected to emulate those of a SiC power semiconductor device (around 10 μs). The simulation will allow for analyzing the overvoltage at device turn-on, the current discharged from the snubber at device turn-on, and the power dissipated in the snubber resistor.

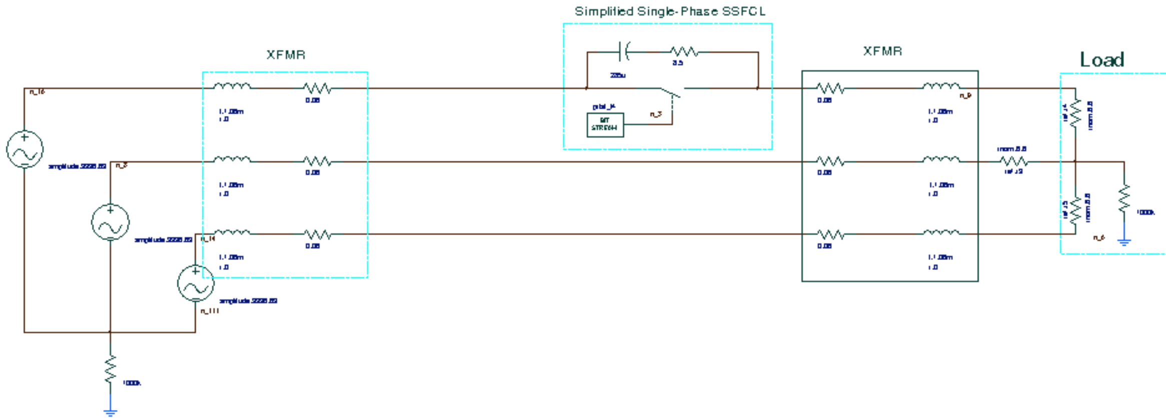


Fig. 4.14. Simulation test setup for 4.16 kV SSFCL testing.

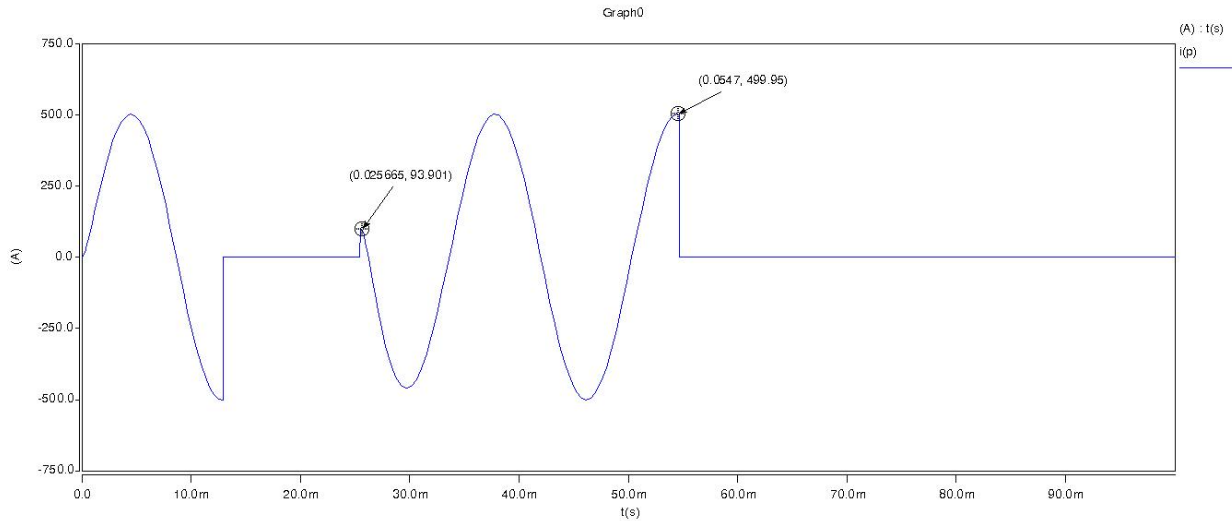


Fig. 4.15. System current for simulation.

In Fig. 4.16, it can be seen that the overvoltage across the switch is sufficiently limited using the initial values for snubber design. The peak voltage across the switch during turn-off is roughly 4.2 kV, which is much lower than the maximum peak value of 8 kV.

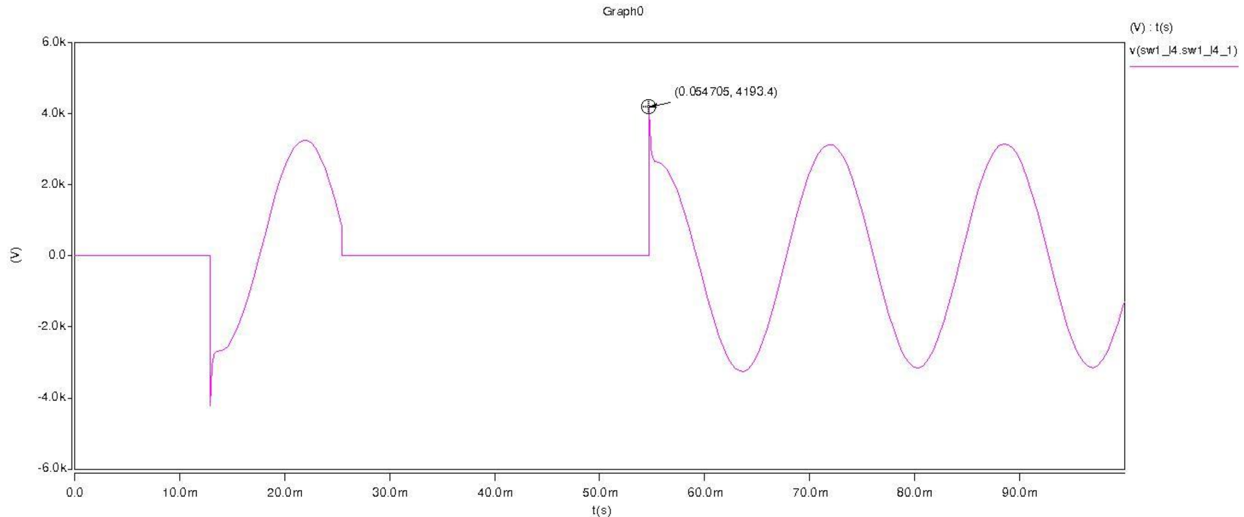


Fig. 4.16. Voltage across switch using 285 µF snubber capacitor.

Upon inspection of the current through the snubber circuit in Fig. 4.17, it can be seen that there is a peak current of about 491 A through the snubber at turn-off and that a peak current of approximately 231 A is discharged from the snubber during device turn-on. Additionally, while the SSFCL is in the blocking state, the current through the snubber path is roughly 255 A. As previously mentioned, this could pose a safety issue in instances where the SSFCL should have opened the line. Furthermore, this results in high power dissipation in the snubber resistor. According to the Fig. 4.18, the steady-state power dissipation is 550.8 kW. Although the SSFCL is rarely in the blocking state, this is much more than can be practically managed by conventional thermal management techniques.

The peak power dissipation in the snubber resistor is more than 2 MW in the immediate aftermath of device turn-off. While this surge in power dissipation lasts only for a few microseconds, it is an extremely high value. This is expected to be alleviated by the addition of a varistor, which will be mentioned later. It can be seen that while the values of the snubber circuit were calculated to limit the overvoltage, there are other practical issues that arise. These issues are of little concern in the typical applications of snubber circuits, in which high frequency

switching occurs and the devices do not block for an extended period of time. The values were optimized using simulation software.

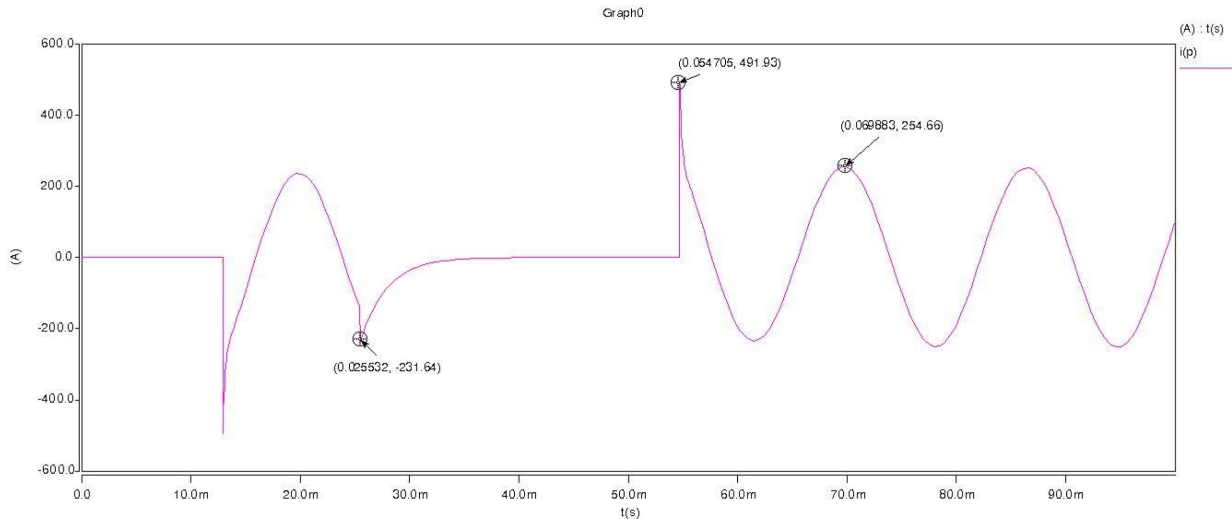


Fig. 4.17. Snubber circuit current for 285 μF snubber capacitor.

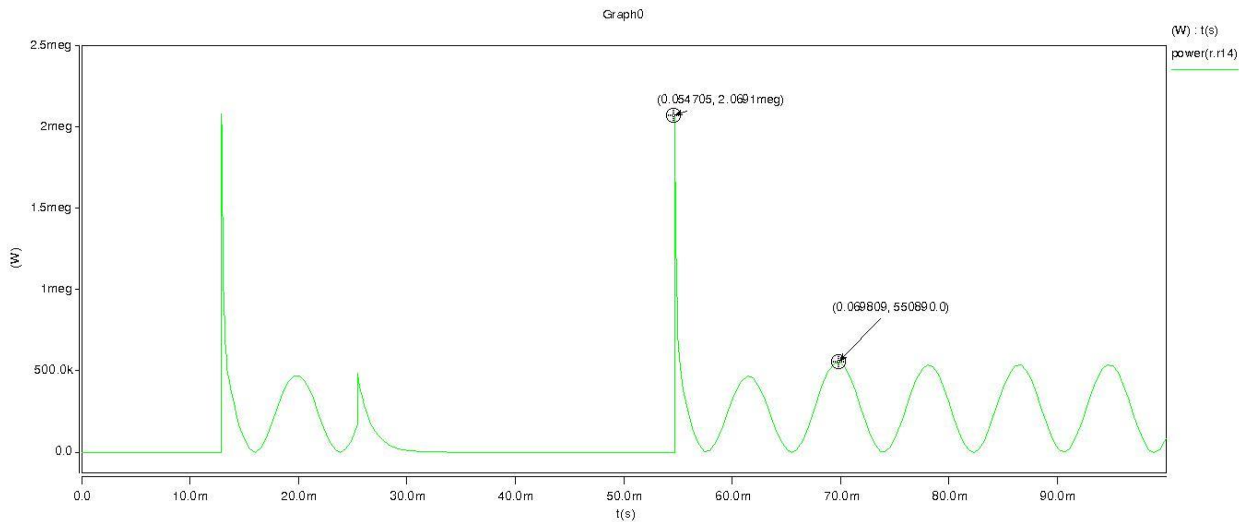


Fig. 4.18. Power dissipation in the snubber resistor.

In order to reduce the current through the snubber circuit, the capacitor value is reduced. It is known that reducing the capacitor value will also increase the peak voltage across the switch during the turn-off period. A trade-off is necessary in order to find a satisfactory value. The resistor value was held constant and the capacitor value was varied in simulations in order to find an optimal value. The current in the snubber path is dependent on the series impedance of both

the capacitor and resistor. Reduction of the resistor value would allow for an increase in current that would counteract the impact of reducing the snubber capacitance. Ultimately, a value of 15 µF was settled upon. This value allows for adequate overvoltage protection while greatly reducing the current through the snubber during the SSFCL blocking state.

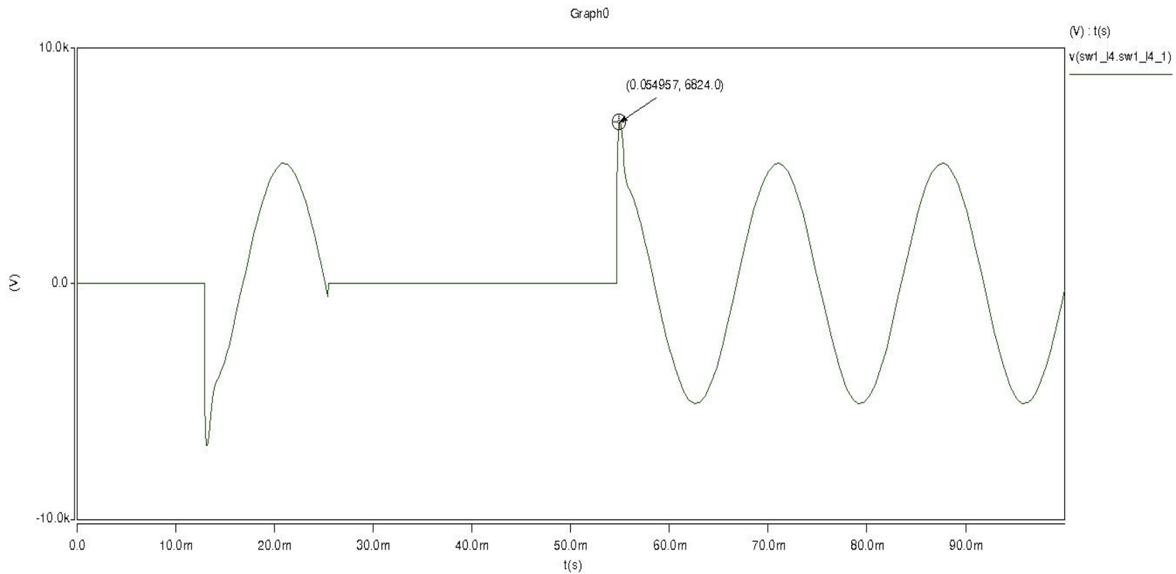


Fig. 4.19. Overvoltage across switch with 15 µF snubber capacitor.

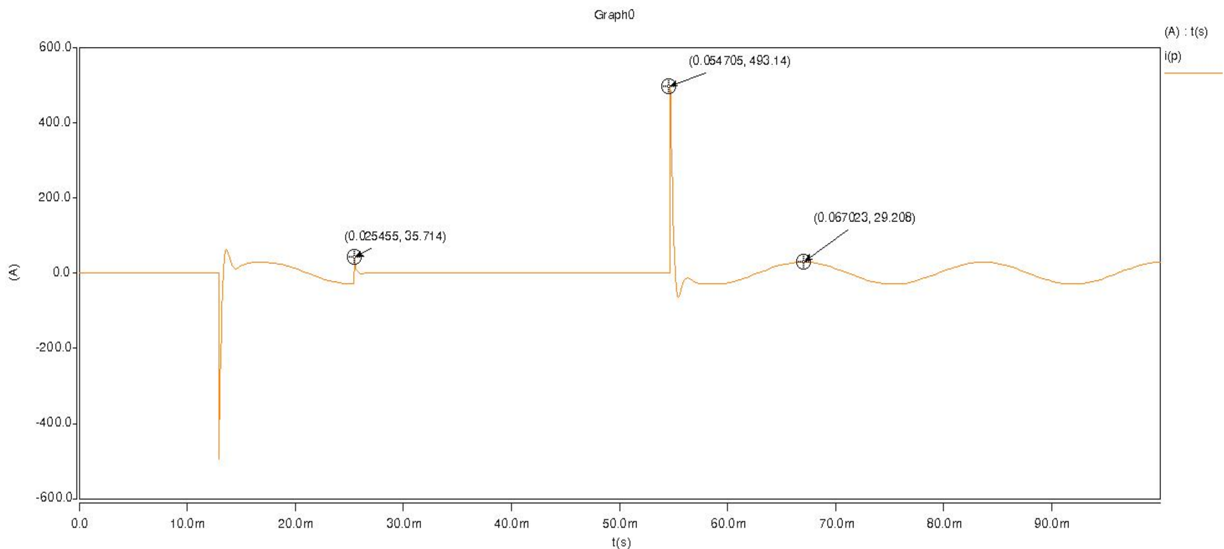


Fig. 4.20. Snubber current with 15 µF snubber capacitor.

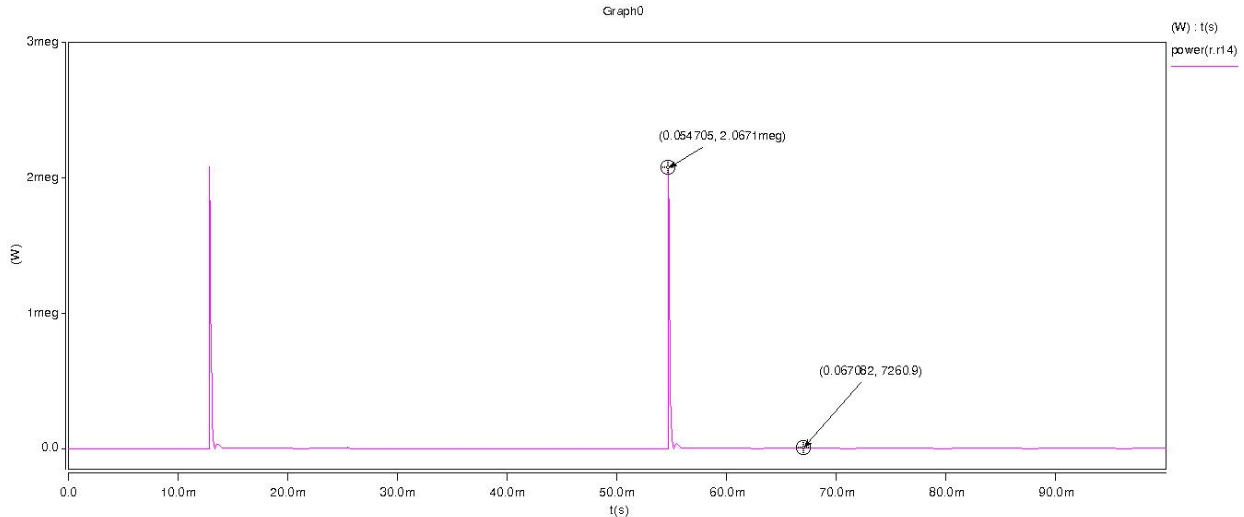


Fig. 4.21. Power dissipation in snubber resistor.

The peak value of the overvoltage in this case was about 6.8 kV. This is a satisfactory value in comparison to the absolute maximum allowable value of 8 kV. Also, this value will allow for additional tolerance in overvoltage. The additional inductance of the cables used in the test setup will also be a contributing factor to the overvoltage. The current through the snubber is limited to less than 30 A. This was chosen as the maximum threshold for snubber current in the SiC SSFCL prototype in order to provide proper thermal management, and is the main reason why the 15 μF value was chosen. While this still poses a safety issue, it allows for much lower power dissipation in the snubber resistor, which totals around 8 kW. This is a value that is much more manageable when considering the thermal management techniques available. Also, the snubber resistor would only dissipate power for short durations of time which could be properly managed during testing. There is some oscillation of the current through the snubber with this new capacitor value as indicated in Fig. 4.20, but it is quickly damped and should not pose a significant problem. As pointed out earlier, snubber design is never an exact process and typically, further optimization is required experimentally.

Custom made capacitors were ordered that would be able to handle the conditions of the SSFCL. These capacitors were rated for 1 μF with a working voltage of 4.16 kV. Fifteen of these capacitors will be paralleled in order to attain the desired snubber capacitance. For the snubber resistor, eight planar, high power, and heat sinkable resistors will be utilized. Each resistor has a continuous power rating of 800 W and up to 1200 W for short durations of time. Each resistor has a value of 15 Ω and a voltage rating of 5 kV. The snubber resistor will consist of four branches in parallel, with each branch consisting of two resistors in series. This arrangement yields a total resistance of 7.5 Ω will allow for the desired voltage and power ratings expected to be achieved during operation.

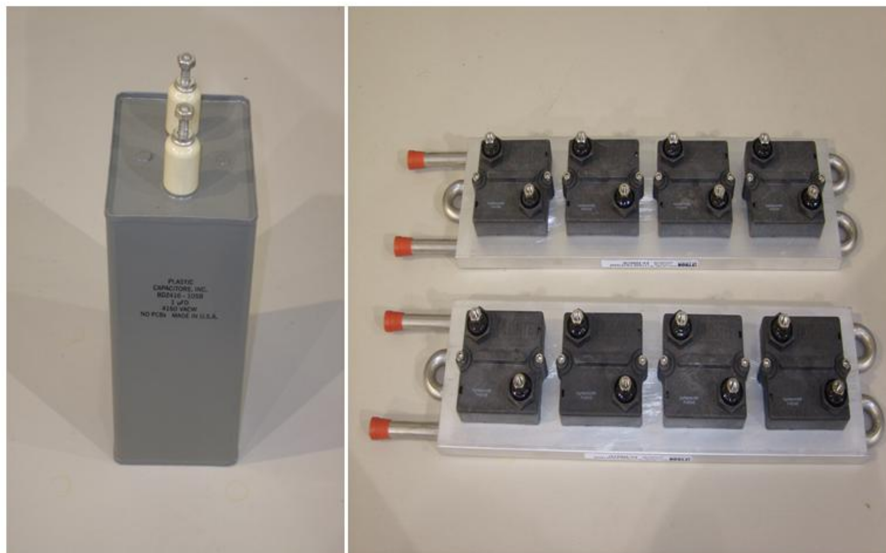


Fig. 4.22. Single snubber capacitor (left) and snubber resistors mounted on actively cooled heatsinks (right).

<u>*4.3.4 Varistor Selection*</u>

In some SSFCLs, the snubber design has been dependent on the varistor selection [10]. While this approach has its advantages, the choice was made in this instance to make snubber design and varistor selection two distinct processes. While varistors provide adequate overvoltage protection, the reliability of the components over time is questionable. The

performance of the varistor degrades with repetitive use, resulting in higher power dissipation in the steady-state, reduced clamping capabilities, and shorter lifetimes. As noted before, one of the most desirable characteristics of the SSFCL is high reliability, and the inclusion of a varistor could actually be detrimental from this standpoint. Furthermore, high energy surges, such as those that can be expected in power distribution systems under fault conditions, can lead to catastrophic failure. Varistors can fail in any number of ways, and this must be accounted for when incorporating them into a system such as a SSFCL. For instance, a varistor that fails as a short circuit while used to provide protection for a SSFCL will counteract the operation of the device.

The varistor is essentially a nonlinear resistor, and one of its main advantages is the fast transition from a high impedance state to a conductive state. Its resistance during turn-off will be much lower than that of the snubber circuit, and as a result the initial high current surges, such as those shown in Figs. 4.17 and 4.20, will flow through the varistor. As alluded to earlier, this will decrease the power dissipation in the snubber resistor during this period. Once the varistor reaches its clamping voltage, current will then flow through the snubber path as well. This should protect the varistor from long durations of sustained high energy absorption, which typically is the major contributing factor in both the degradation and failure of the component. The operation of a snubber circuit in tandem with the varistor will provide the greatest degree of protection for the silicon carbide power semiconductor devices while increasing the system reliability. In the case that irreversible damage occurs to the varistor, the aforementioned snubber design should provide adequate protection. For the SSFCL, a high energy industrial class varistor, the V202BB60 from Littelfuse, was chosen with a continuous voltage rating of 2800 V_{RMS}. Two of the varistors will have to be serially connected for testing at 4.16 kV.

4.4 SSFCL Controller

4.4.1 Controller Hardware

The SiC SSFCL prototype is a voltage-controlled SSFCL. This means that in the event of a fault, the magnitude of the current is limited using phase angle control of the SiC SGTO devices. The voltage controlled topology was chosen due to the smaller footprint and the degree of flexibility that is provided through its use. This topology of the SSFCL has interruption capability, and its control can be designed such that it has other advanced functions. Conceivably, the SiC SSFCL prototype could ultimately fulfill the functions of three power protection devices: circuit breaker, recloser, and fault current limiter. The controller of the SSFCL is used in order to detect faults and implement the limiting action. The block diagram of the controller is shown below.

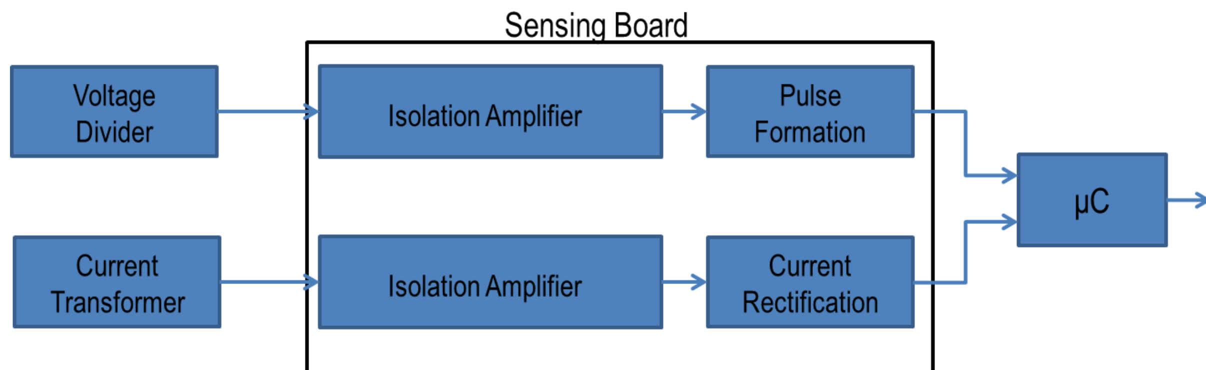


Fig. 4.23. Block diagram for SSFCL controller.

The sensing board is used to transform the outputs from the voltage divider and current transformer (CT) into signals that are compliant with the I/O port and ADC specifications of the selected microcontroller, which is the C8051F410 from Silicon Laboratories. The AD202KN isolation amplifier from Analog Devices provides up to 2000 V of isolation. The voltage divider is used to produce a scaled-down representation of the system voltage. The voltage divider can accept an input of up to 15 kV, with outputs of 100 V, 10 V, and 1 V. The pulse formation

circuitry is used in order to give an indication of whether or not the voltage is positive or negative. As long as the voltage is positive, a logic high pulse will be sent to the microcontroller. Likewise, a logic low pulse results when the voltage is negative. This information is used to trigger the appropriate SiC SGTO since these unidirectional devices have to be configured in anti-parallel for the SSFCL application. The circuitry used to implement this functionality is comprised of operational amplifiers and is shown in Fig. 4.24.

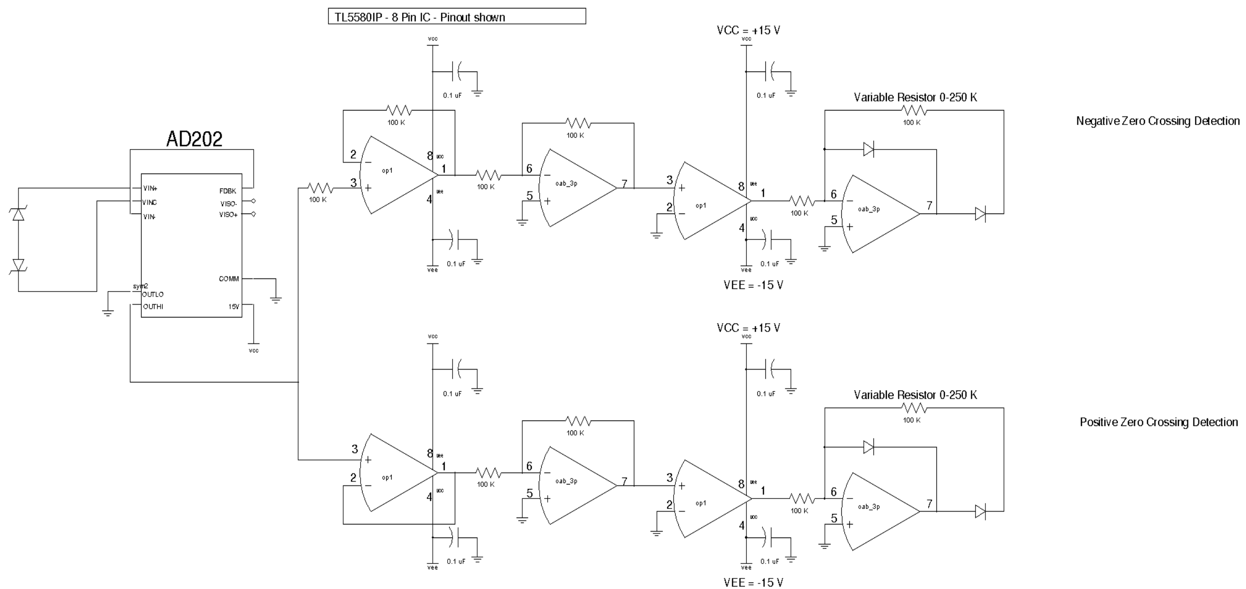


Fig. 4.24. Zero crossing detection circuitry.

The negative zero crossing circuit and the positive zero crossing circuit provide complementary signals. The input to the isolation amplifier is protected using 5.1 V zener diodes, which prevent the output of the sensor from exceeding the rated value of the isolation amplifier input. The circuits both consist of a buffer stage, an inverting stage, a comparator, and a rectifier with variable gain. The gain of the final stage is adjusted using a variable resistor such that the maximum allowable voltage of the I/O port, which is approximately 5.25 V, is not exceeded. Simulation results, performed using PSpice, are shown below based on a sinusoidal input that would be expected from the voltage divider.

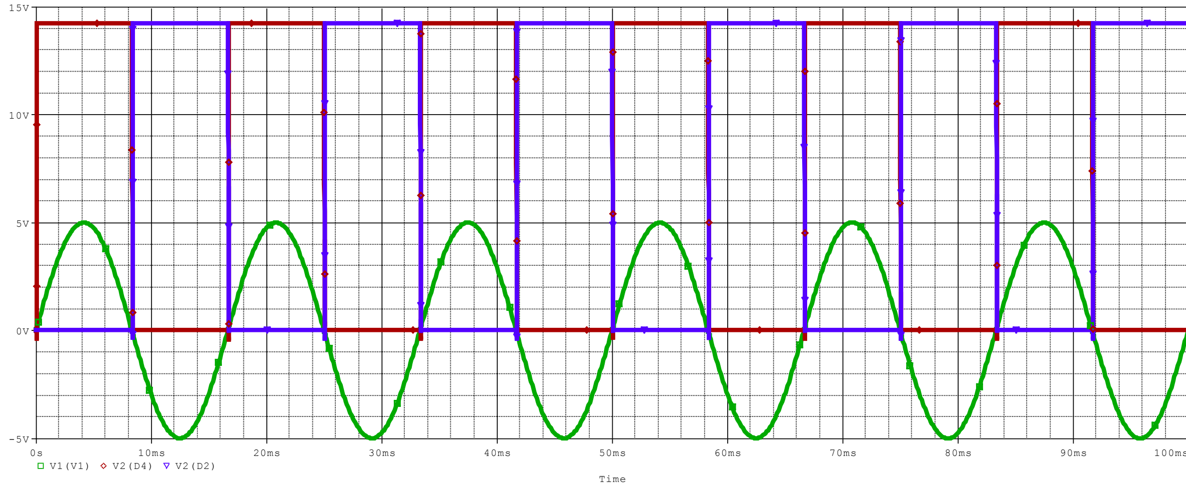


Fig. 4.25. Zero crossing circuit simulation results with sinusoidal input (green), positive voltage pulse indicator (red) and negative voltage pulse indicator (blue).

This circuitry is especially useful during the current limiting action of the SSFCL. The phase angle control is implemented based on delays with respect to the positive and negative zero crossings. The programmable counter is used to provide a delay of varying duration based on the magnitude of the current that was previously detected.

The method used to detect faults for the SiC SSFCL prototype is based on threshold detection. Once the current has surpassed a predefined limited, a fault is determined to have occurred. Ideally, FCL devices should make the distinction between faults and excessive currents caused by capacitor transients or transformer in-rush currents. Many of these techniques rely on a combination of both overcurrent detection and rate of rise calculations in order avoid false tripping. Fast fault detection techniques have been developed that will make the distinction and are of ideal use in applications such as fault current limiters [89], [90]. For initial testing of the SiC SSFCL prototype, the threshold based detection was deemed to be adequate.

The 12-bit analog-to-digital converter (ADC) of the microcontroller is employed to detect overcurrents in the SSFCL system. Since the microcontroller can only accept unipolar signals, the current signal has to be rectified. Also, the current output of the CT that is used to measure

the current must be transformed to a voltage that can be sampled by the ADC. This is accomplished via the circuitry shown in Fig. 4.26.

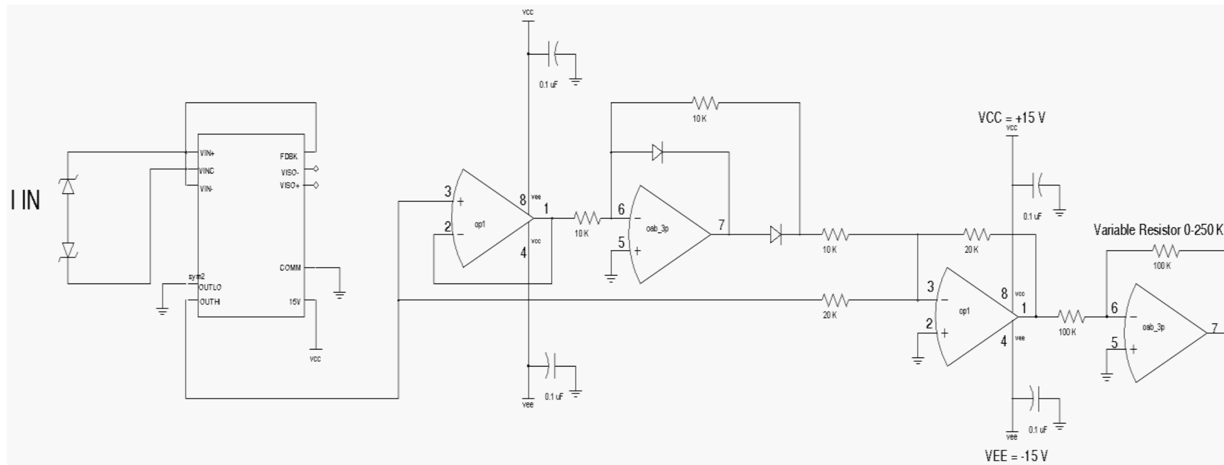


Fig. 4.26. Current rectification circuitry.

A 2500:5 A current transformer will be used in order to detect the system current. The output of the transformer uses a resistor as a load, and the voltage across this resistor is used as the input to the isolation amplifier in the figure above. The operational amplifiers are configured as a precision rectifier circuit, which is used in order to perform full-wave rectification of the input current signal. The final op-amp with variable gain is necessary in order to calibrate the ADC, which has a maximum voltage input of 2.2 V. When the calibrated signal exceeds the threshold value, a fault is determined to have occurred. A simulation using PSpice details the expected operation of the current rectification circuitry as shown in Fig. 4.27.

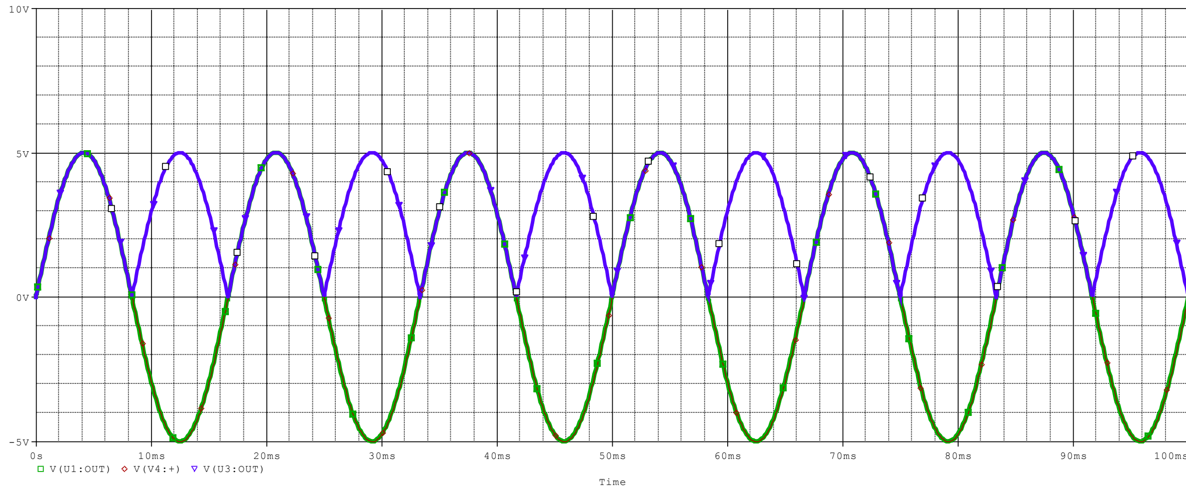


Fig. 4.27. Input current signal (green) and full-wave rectified signal (blue). The signals overlap during the positive half cycle.

A printed circuit board was developed that contained both the zero crossing detection circuitry and the current rectification circuitry. Testing of the board yielded the expected results based on a sinusoidal input.

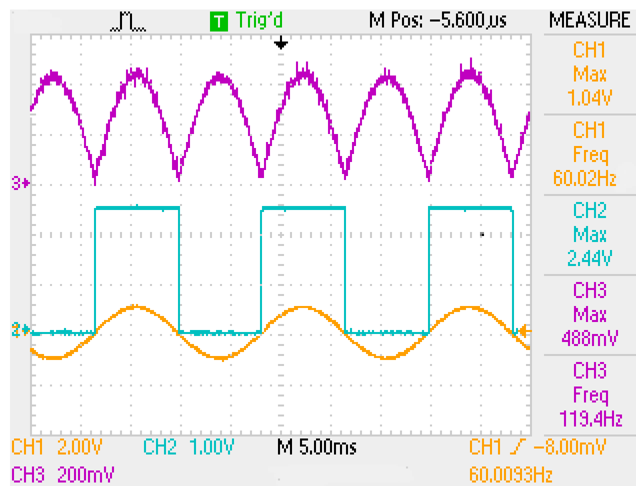


Fig. 4.28. Testing results for sensing board with sinusoidal input (orange - CH1- bottom) positive zero crossing detection (blue - CH2- middle) and current rectification used for ADC (purple - CH3-top).

Afterwards, a controller box was developed which contains the sensing board, the microcontroller, a power supply for powering the two, a USB interface for quick reprogramming of the microcontroller, and an amplifying circuit. The amplifying circuit is needed since the

output current of the microcontroller is insufficient for providing proper turn-on and turn-off of the gate driver. The amplifying circuit consists of an IRF1404 logic-level power MOSFET connected in open drain. The output ports of the microcontroller are used to drive the gate of the MOSFET. The gate drive input is connected between the 12 V supply and the drain of the MOSFET, and as such, is driven by a much larger current than can be achieved with the microcontroller alone.

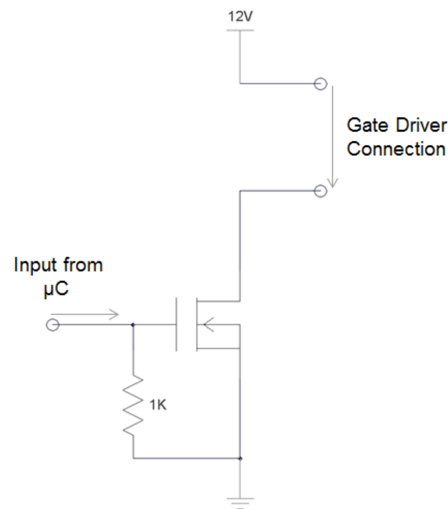


Fig. 4.29. Schematic of open drain amplifying circuit used for proper gate driver operation.

The inputs to the controller box are the signals provided from the voltage divider and current transformer, and the outputs include the turn-on and turn-off signals to be provided to the gate drivers, as well as a signal that indicates when a fault has occurred.

Fig. 4.30. Inside and outside of SSFCL controller box.

4.4.2 SSFCL Control Algorithm

The SiC SSFCL will provide current limitation via phase angle control. The operation during both normal and fault conditions is implemented using the C programming language within the Silicon Laboratories Integrated Development Environment. After the line current is determined to be higher than the threshold current, I_T, the control of the SSFCL is altered. During normal operation conditions, the control is straightforward. After detecting a zero-crossing, a gate signal is applied to the appropriate SiC SGTO based on the polarity of the input voltage. A phase angle α of $\omega t = 0°$ for is used triggering the SiC SGTO conducting the positive current, and a phase angle of $\omega t = 180°$ is used for gate triggering of the SiC SGTO conducting the negative current. This allows the full-sinusoidal current to be conducted by the SSFCL.

For current limiting action, the initial value of α is carefully chosen in order to adequately limit the current during the first cycle of phase angle control. The value of the fault current in the system varies due to a number of different values, namely the type of fault and the fault location. The SiC SSFCL control was implemented such that the value of α is allowed to vary during the fault, providing for an extra degree of flexibility. An initial value of α is specified, equating to a time delay from the occurrence of the zero crossing:

$$t_{delay} = \frac{\alpha}{360 \times f}, \quad \text{where } 0° \leq \alpha < 360° \tag{4.14}$$

In this equation, f represents the fundamental frequency of the distribution system, which is either 50 or 60 Hz. The time delay is given in seconds. The value of α is adjusted during each cycle of the current limiting, based on the maximum value of current that is detected. If the current threshold is not reached, the value of α is decreased such that the delay is shorted. As such, the maximum current value is slowly increased each cycle as long α remains greater than 90° for the positive half cycle (270° for the negative half cycle). Note that for a sinusoidal waveform the maximum values occur at 90° and 270°. As such, if the value of α is decreased such that it is less than these values for the positive and negative half cycles, respectively, it can generally be assumed that the fault is no longer present, since the controller has determine peak value of the ac current waveform is less than the threshold current I_T. Conversely, if the current threshold is exceeded at any time during limiting, the value of α is increased such that the maximum current is lower during the subsequent half-cycle. The optimal value of α during this mode will be one that allows the maximum amount of current to flow without exceeding the threshold. This method of control is somewhat analogous to the "observe and perturb" method of control that is popular in the use of maximum peak power trackers (MPPT) in solar applications. Using this operational method, the SSFCL control will allow for the seamless transition back to normal conduction mode if the fault is no longer present, while limiting the current as long as the fault is present. If the fault is present after a predetermined number of cycles, the line is opened. This control gives the SSFCL recloser capability, distinguishing between temporary and permanent faults. If the fault is temporary, the SSFCL has the ability to return to normal operation, but will open the line for faults that are not cleared in a timely fashion [91].

The limitation of the first current peak is performed via hard turn-off, while the subsequent limitation is performed using phase angle control. There is typically a multi-cycle delay between these actions. This delay is not necessary, but can protect the SiC SGTOs from a potentially dangerous operating situation. Note that the equation for a fault current, as given in [92], is:

$$i = \frac{\sqrt{2}V}{|Z|}\sin(\omega t + \phi - \theta) + \frac{\sqrt{2}}{|Z|}\sin(\theta - \phi)\, e^{-(R/L)t} \tag{4.15}$$

In this equation, |Z| represents the magnitude of the impedance in the system, and θ is an angle whose tangent is ωL/R [93]. The first current component is the steady-state current, while the other represents the transient dc offset. Asymmetrical fault currents decay in accordance with the time constant τ which is equal to L/R, and such a current was illustrated in Fig. 1.2. This dc component can prove problematic for proper current limitation, as the value of current for a given α during the positive half cycle is much higher during this period than it will be once the current has reached its steady-state value. Consequently, the same value of α used during the negative half cycle will result in a current that is not identical to that of that positive half cycle. The delay can be implemented such that current limitation occurs once the fault current has reached its steady-state value.

A block diagram of the control algorithm is shown in Fig. 4.31 on the following page. For the SiC SSFCL, a five cycle delay is implemented between initial current interruption and the beginning of phase angle control. Also, twenty cycles of current limiting are performed before a determination is made as to whether the fault is permanent or temporary. This is the counter value, which is used by the microcontroller to determine the number of limiting cycles that have taken place. The initial value of α, using the positive half cycle as the reference, was chosen to be approximately 170°, which represents a delay of 7.87 ms. For twenty cycles of limiting, the Δα

value is 8.5°. At the conclusion of the twenty cycles, if the fault is no longer present, the phase angle α is 0°.

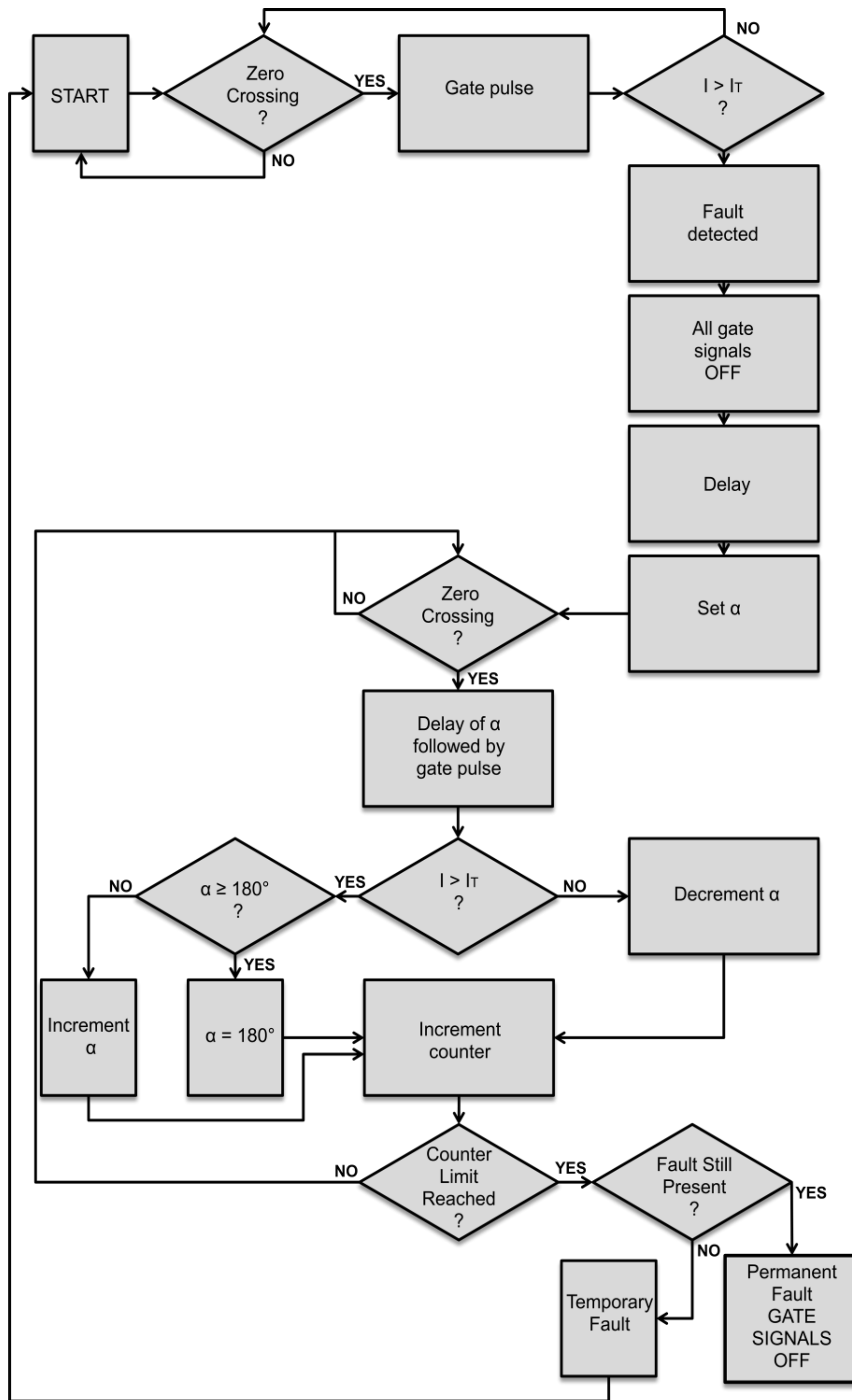


Fig. 4.31. Flow chart for SiC SSFCL control.

CHAPTER 5

SILICON CARBIDE SOLID-STATE FAULT CURRENT LIMITER SIMULATION

5.1 Components of the SiC SSFCL Simulation

Preliminary evaluation of the single-phase SiC SSFCL system was conducted using Saber and Simulink co-simulations. The simulations were conducted for the expected testing conditions at a system voltage of 4.16 kV. The maximum fault condition of the test setup at this voltage is approximately 500 A.

The 4.16 kV test setup consists of contains two transformers, one immediately upstream and the other immediately downstream of the SiC SSFCL. These transformers are rated 2.5 MVA, 480:13800 V with specified %R of 0.89% and %X of 5.67%. The transformers were modeled as equivalent series impedances for the simulations in Saber. The single phase equivalent of the test setup used for simulations is shown below.

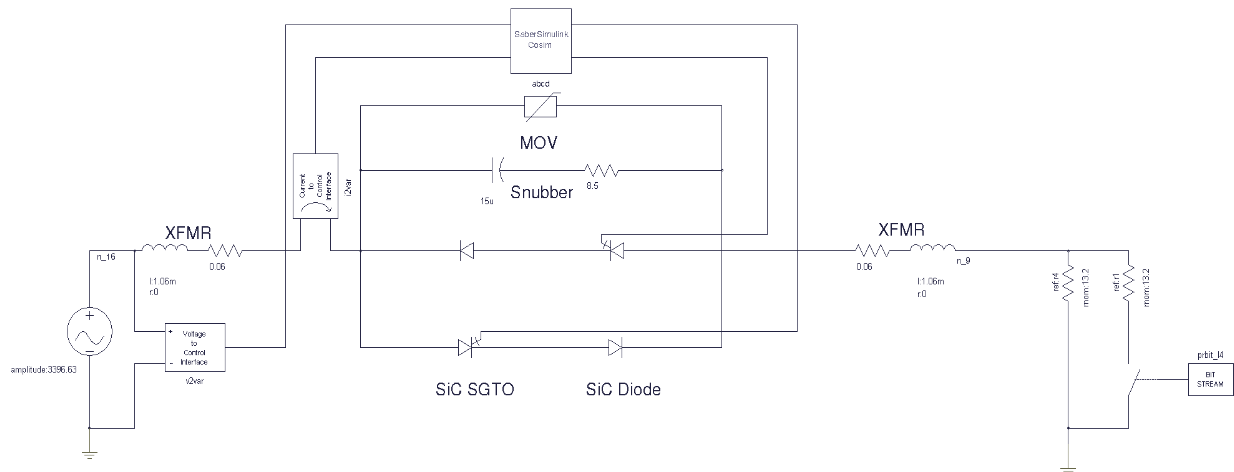


Fig. 5.1. Test circuit for simulation in Saber.

The source voltage magnitude is 3396 V, which is the peak magnitude of the 4160 V single phase equivalent circuit. Voltage and current measurements are sent to the Saber/Simulink co-simulation interface via control interfaces. There are several elements used to ensure signal compatibility between Saber and Simulink, such as a multiplier element and a block for digital signal conversion. The nominal load is 13.2 Ω, which decreases by 50% to 6.6 Ω for fault current emulation. The previously determined snubber capacitor and resistor values of 15 μF and 8.5 Ω, respectively, were used in the simulation for overvoltage protection. The varistor is modeled using the I-V characteristics of the selected V282BB60, which has a nominal voltage V_N of 4700 A at 1 mA, and a maximum clamping voltage V_C of 7400 V for a maximum current I_{max} of 70 kA. The series resistance of the varistor above the nominal voltage is modeled according to the equation:

$$R_{varistor} = \frac{V_C - V_N}{I_{max}} \tag{5.1}$$

The SiC SSFCL system has two distinct operating modes. During normal operation, the control is configured such that current flow to the load is unimpeded by the presence of the fault current limiter. The system current is fully sinusoidal, with no distortion. In the event of a fault, the current must be interrupted before the first peak of the fault current. Afterwards, the second mode of operation begins, which is phase angle control. The gate signals are delayed by an angle α resulting in fault current limitation. In order to successfully detect an overcurrent condition and facilitate the transition between the two modes, an embedded MATLAB function was written and incorporated within Simulink. The following figure shows the control elements of the system as implemented in Simulink.

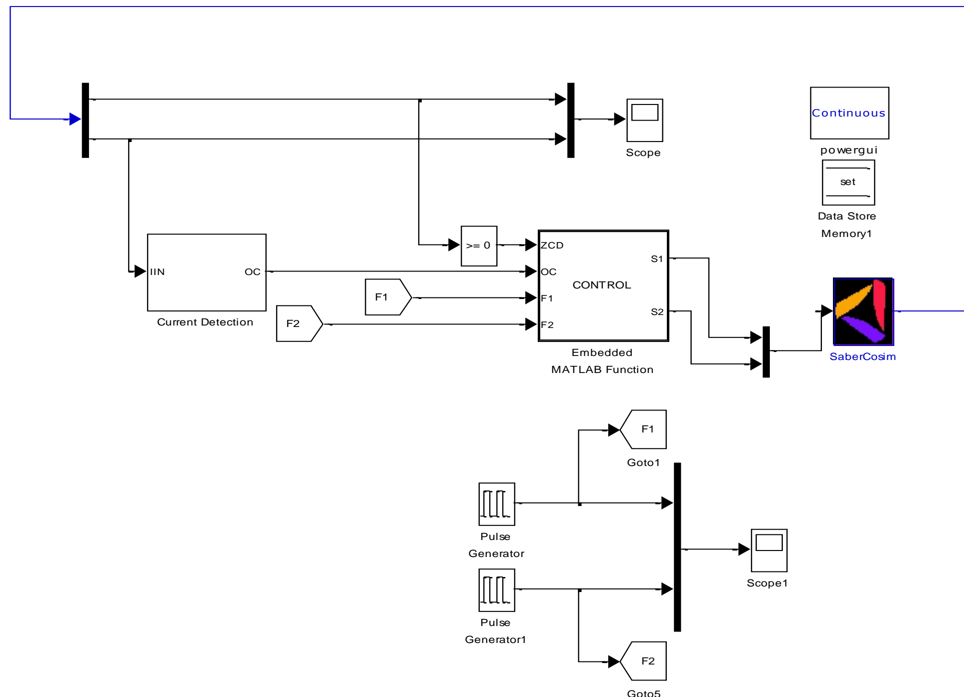


Fig. 5.2. Simulink control elements.

Saber and Simulink exchange information during the co-simulation; the voltage and current measurements are passed from Saber to Simulink. The voltage measurements are compared to zero within Simulink in order to determine the voltage polarity, which is used in order to provide the gate pulses during normal operation. There is a current detection subsystem that identifies fault conditions within the system using a current measurement from Saber. In the event of the fault, the current is interrupted based on the specified threshold, and after a short delay, phase angle control commences. The phase angle control is performed via pulse generator blocks in Simulink.

The SiC SGTO device model used in the simulation consists of three elements: a power semiconductor switch, a diode, and a resistor. The power semiconductor is used in order to maintain compatibility with Simulink signals for use in a co-simulation. Also, the turn-on and turn-off times of the SiC SGTO can be set within the power semiconductor switch. The times used for the simulation are 7 μs, based on characterized data from the previous chapter. The

diode is used in order to define the turn-on voltage of the SiC SGTO and also ensures that the SiC SGTO model only has unidirectional current conduction. The turn-on voltage as determined through device characterization is 2.8 V. Lastly, the resistor is used in order to emulate the drift layer resistance of the SiC SGTO, as well as the series resistor used to maintain current sharing. This value was determined to be 98 mΩ for a single device based on the on-state I-V curves. The SiC SGTO model is also helpful in that it can be used to emulate the characteristics of a single device or those of a SiC SGTO module consisting of several devices in parallel. For the specified simulation conditions, ten 8 kV SiC SGTO devices would be needed for proper operation. Thus, the equivalent resistance can be altered in order to reflect this situation. Likewise, the SiC diode can be modeled using a diode model within Saber, with the turn-on voltage of 2.8 V changed to reflect those of actual diode used in the application. The series resistance of 60 mΩ used with the diodes in the actual application can also be accounted for in this model. An external resistor is used for emulating the drift resistance and series resistor, with a value of 98 mΩ.

For the simulations, the maximum fault current is 500 A, while the current threshold is specified to be approximately 300 A. Under normal operating conditions, the system power factor is 0.993 lagging. The SiC SSFCL would require ten SiC SGTOs and ten SiC diodes operating in parallel in order to withstand the maximum fault current in the test setup. Based on this specification, the voltage drop across the SiC switching position used for the simulation during normal operating conditions is 10.76 V. With a system current of 243 A under non-fault conditions, the total I^2R losses in the series resistors will be 709 W and the total conduction losses of the devices will be 449 W.

5.2 Simulation Results

The fault is initiated at simulation time of 100 milliseconds. Fig. 5.3 shows the current interruption in the system, as well the subsequent current limitation via phase angle control. For simulation, the delay between the interruption and phase angle control is equivalent to a half-cycle of the fundamental frequency.

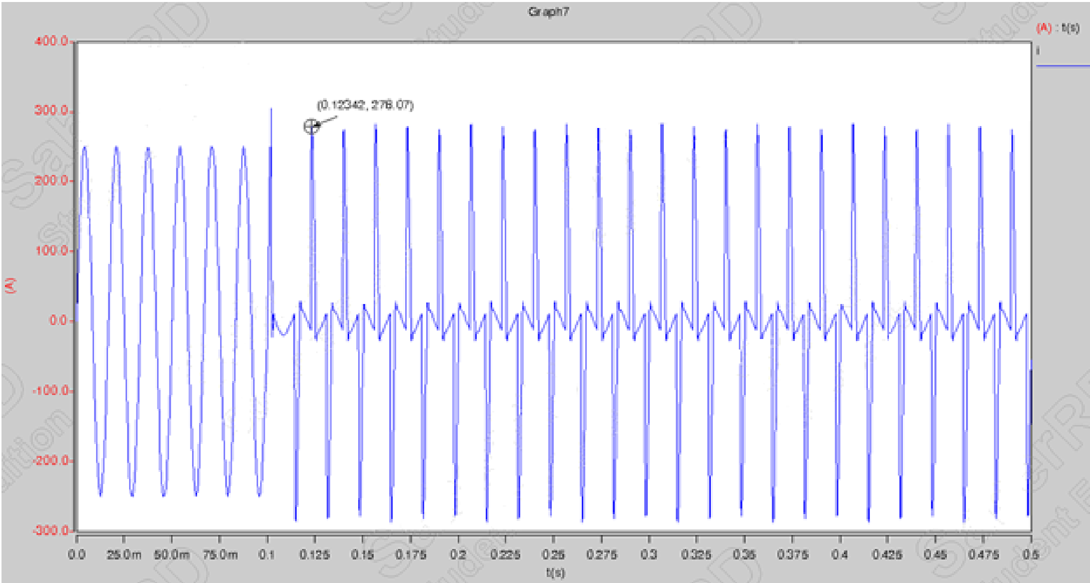


Fig. 5.3. Fault current interruption and phase angle control.

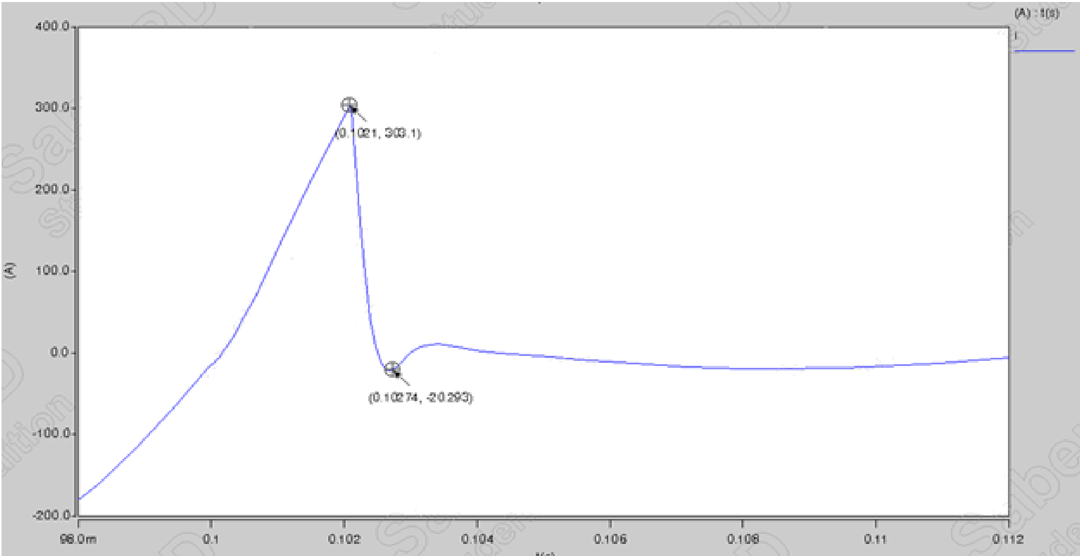


Fig. 5.4. Interrupted fault current.

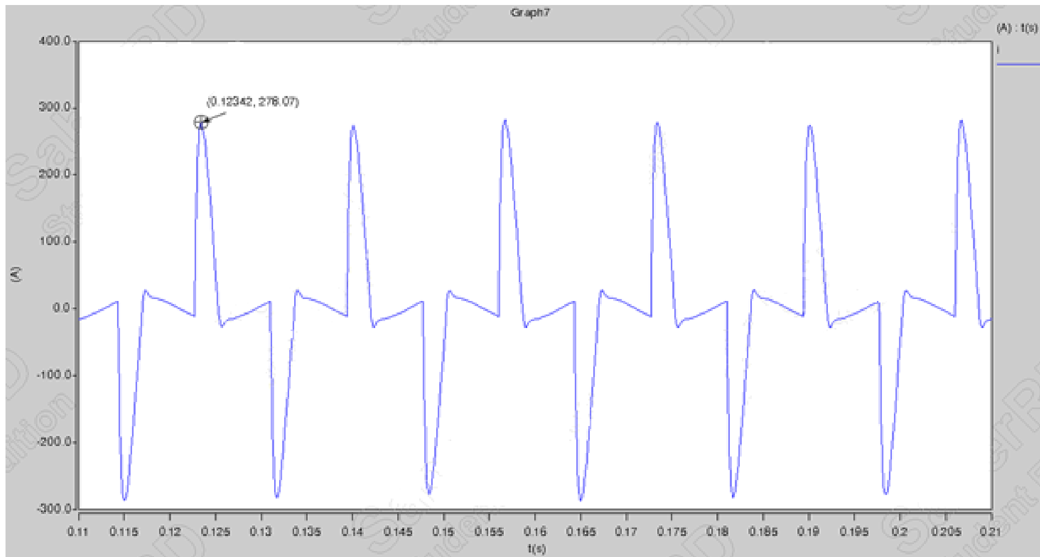


Fig. 5.5. Limited current using phase angle control.

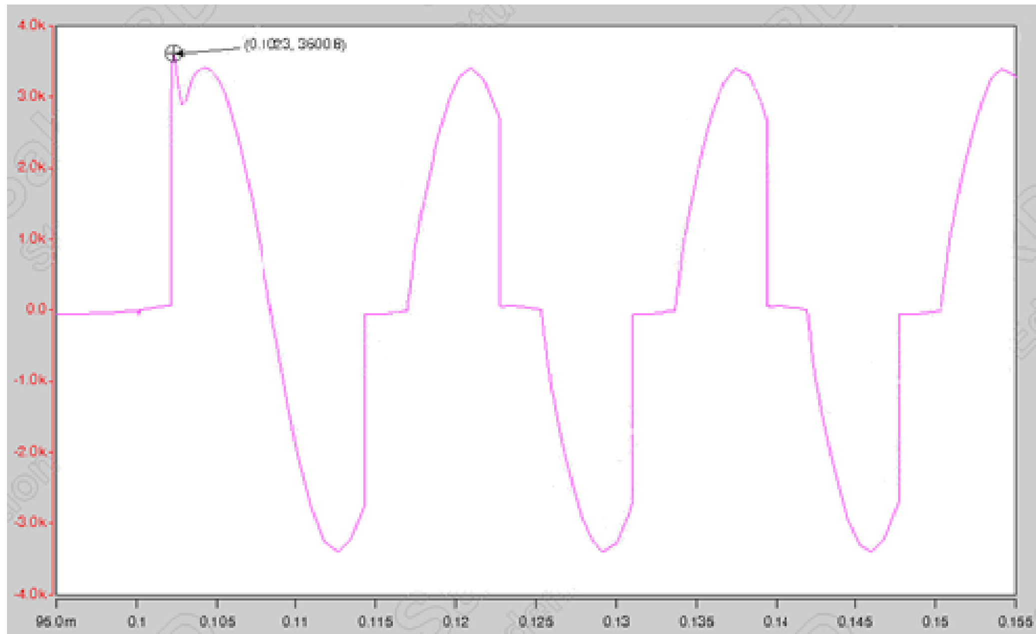


Fig. 5.6. Voltage across SSFCL at fault interruption and during current limiting.

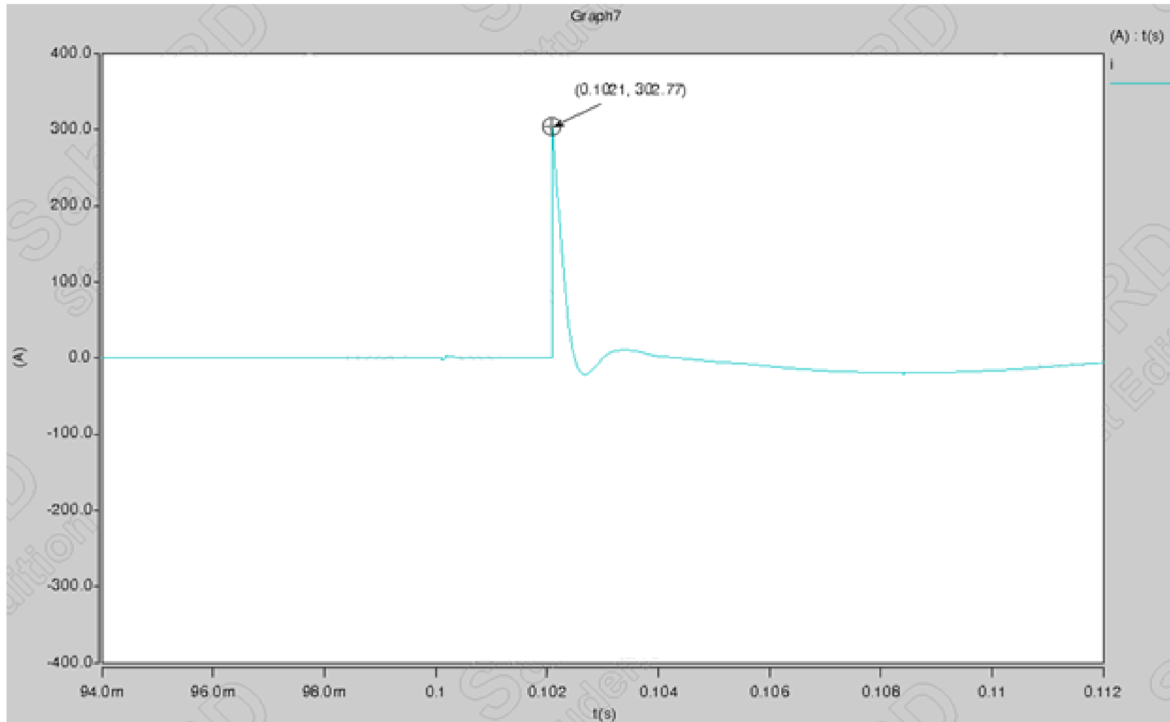


Fig. 5.7. Snubber current at turn-off.

Current interruption occurs at a value of 302 A. As shown in Fig. 5.4, the duration between the turn-off of the fault current and the time during which current has been completely commutated to the snubber circuit is roughly 600 μs. The peak overvoltage value at current interruption, as shown in Fig. 5.6, is 3600 V. This is well below the maximum allowable value of 8 kV. The overvoltage does not reach a sufficient value for the varistor to clamp the voltage based on its characteristics; hence, the path of current flow after current interruption is through the snubber path. The peak fault current flows through the snubber circuit for 350 μs during this period as shown in Fig. 5.7.

After current interruption, phase angle control begins in order to limit the current. The phase angle α is 145°, resulting in a fault current reduction of 42% once the fault current has reached steady-state. This phase angle value limits the fault current to 278 A. During fault current limitation, the system current is expected to be distorted due to the chosen method of control. For fault current limitation, the duration of the distorted signal is of little consequence, and only

becomes an issue if the period of phase angle control becomes longer than several seconds. However, examination of the current during phase angle control shows that the current waveform is distorted beyond what is expected. The current appears to be oscillatory during the periods in which neither of the SiC SGTOs is conducting. This is due to the presence of the snubber circuit. One contributing factor is that the size of the snubber components was slightly changed from the optimal values in order to minimize current flow when the SiC power devices are not conducting. There is another reason as well. When the current flows through the snubber circuit, the power factor of the system becomes 0.47 leading. This is due to the fact that the 15 μF capacitance is the dominant impedance in the system configuration during this period. This leads to a phase shift between the system voltage and current of 61.96°. This causes the seemingly oscillatory response during this brief period, which in actuality is the sinusoidal current flow through the snubber circuit. The snubber current is shown in the figure below along with the system current.

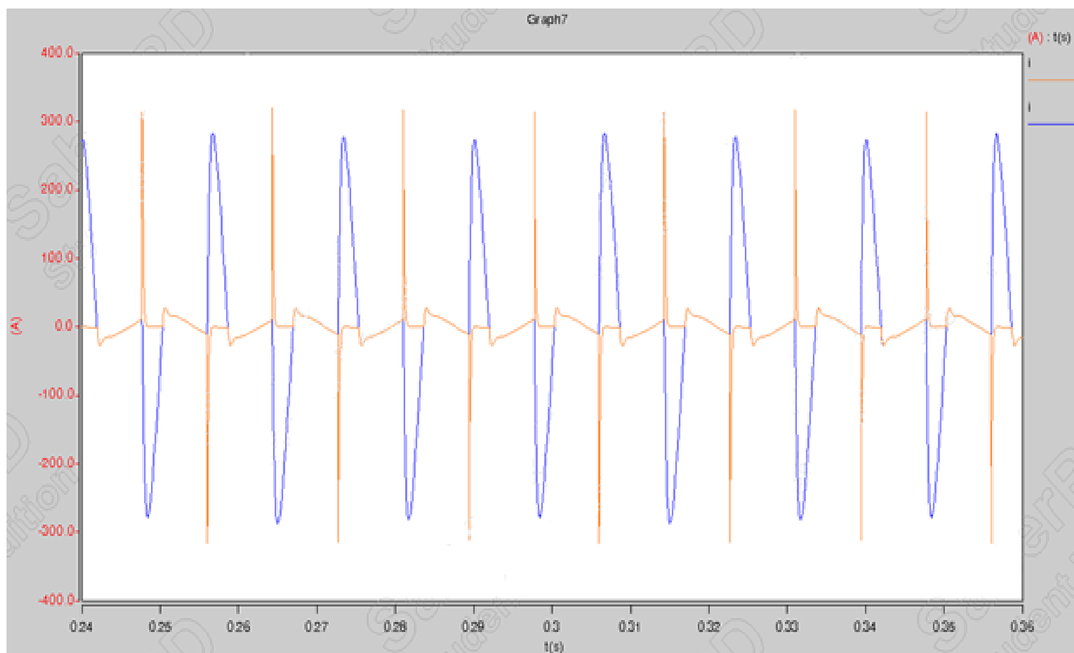


Fig. 5.8. Snubber current (orange) and system current (blue).

As illustrated in Fig. 5.8., during phase angle control there are several distinct changes in the snubber current. At device turn-on, there is a current spike with a magnitude of 314 A through the snubber path due to the abrupt change in the snubber capacitor voltage. Fig. 5.6 shows how the voltage across the SiC SSFCL decreases from 2.79 kV to 10.76 V over this period of 315 μs. After the main SiC SGTO device begins current conduction and becomes the low impedance path for system current, the snubber current falls to zero. Lastly, as the main conducting device naturally commutates at the zero crossing, sinusoidal current flow ensues through the snubber path, with a peak value of 22 A for the specified testing conditions.

In order to further analyze the system impact during fault conditions, a Fourier analysis was conducted for the system. The current waveform under the fault conditions was simulated over 30 cycles for this investigation. This is longer than the fault current limiter system would have to operate under most conditions, as the rated interruption time for most circuit breakers in the 4.16 – 13.8 kV range is 50 to 83 ms as specified in IEEE Std. C37.06-1999.

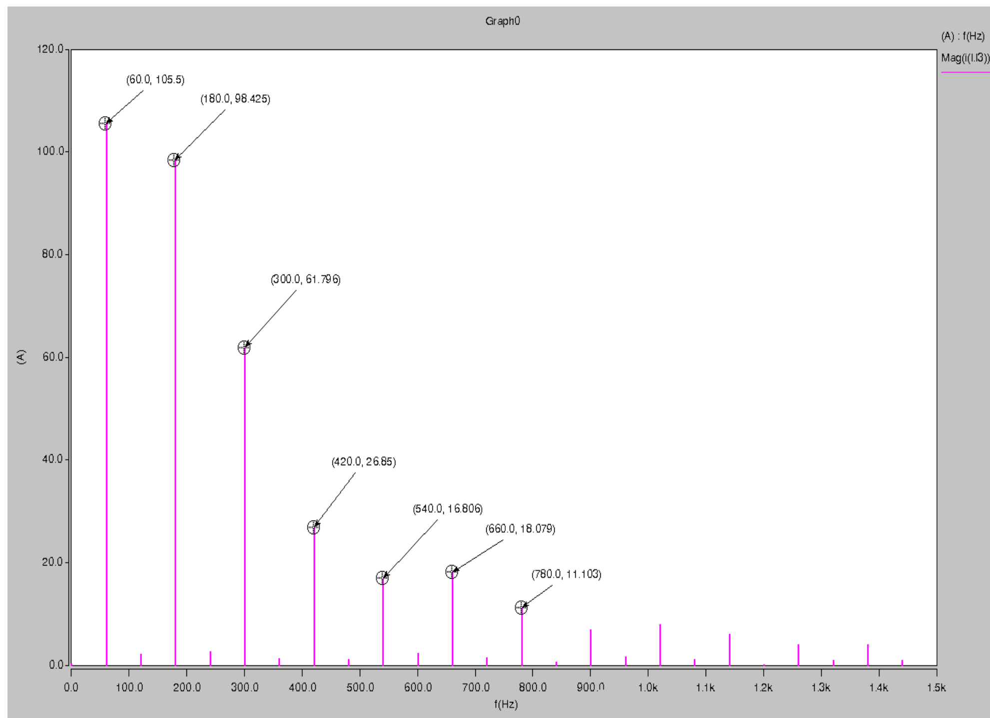


Fig. 5.9. Fourier analysis of current limited signal.

The odd harmonic components of the system are shown in the table below as a percentage of the fundamental frequency component.

Table 5.1. Harmonic Components of System Current During Current Limiting.

Harmonic Component	Percentage of Fundamental (%)
1 (60 Hz)	100
3 (180 Hz)	93.29
5 (300 Hz)	58.51
7 (420 Hz)	25.45
9 (540 Hz)	15.93
11 (660 Hz)	17.14
13 (780 Hz)	10.52

For further evaluation, the total harmonic distortion of the current limited waveform was calculated. The total harmonic distortion (THD) is calculated the following equation:

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \cdots + I_h^2}}{I_1} \tag{5.2}$$

Using the normalized component values from Table 5.1, the THD is calculated for odd harmonic components 1-13 as:

$$THD = \frac{\sqrt{93.29^2 + 58.51^2 + 25.45^2 + 15.93^2 + 17.14^2 + 10.52^2}}{100} = 1.15 \tag{5.3}$$

The value of THD is extremely high in this instance, and is further complicated by the large value of the third harmonic component in the single phase test setup. While this is well above what is acceptable for long-term duration by IEEE Std. 519, which specifies that the harmonic components be less than 4% of the fundamental for long-term duration, the interval of this distortion is only for a few cycles. The standard allows THD in excess of nominal limits for short periods, but it is evident that the inclusion of the snubber circuit in the SiC SSFCL leads to

high levels of distortion that could become problematic if operation is extended beyond the sub-second intervals that are used for the initial SiC SSFCL evaluation. The distortion could also lead to the incorrect operation of protective relays or other equipment in the feeder system during the current limiting period. The distortion can be decreased if the phase angle is reduced, as this will produce a more sinusoidal waveform. However, in the actual test setup, the phase angle is not predetermined; it will be a function of both the maximum potential fault current and the threshold value chosen for current limiting.

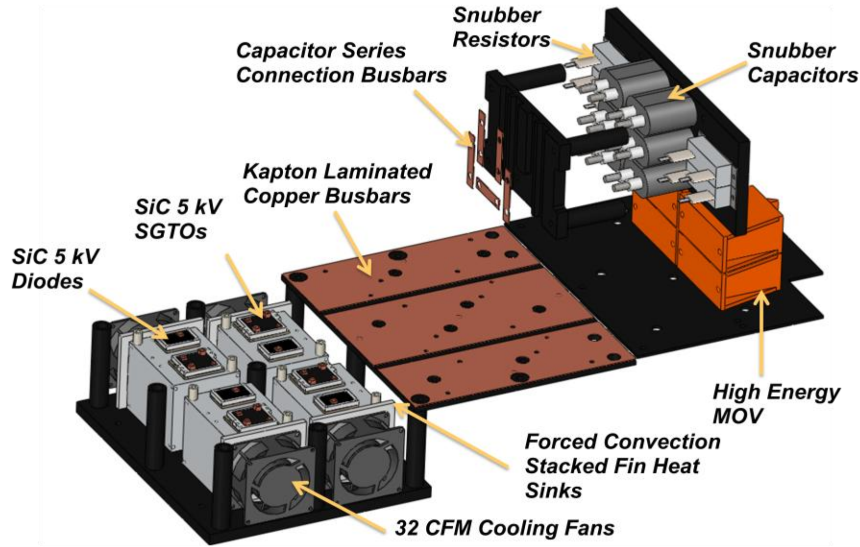
CHAPTER 6

SILICON CARBIDE SOLID-STATE FAULT CURRENT LIMITER TESTING

6.1 Testing Using Scaled-Down Silicon Carbide SSFCL Prototype

Initial test results for a silicon carbide based solid-state fault current limiter were obtained using a scaled-down prototype. This prototype uses the same topology and control as the full-scale system, and is used for validation of the auxiliary circuits (i.e. gate driver and controller) before moving on to full power testing at the National Center for Reliable Electric Power Transmission (NCREPT) testing facility. There are a number of considerations involved with testing at NCREPT, so this system is able to be tested in the University of Arkansas Power Electronics Laboratory.

The scaled-down prototype was designed by a University of Arkansas research team. The initial ratings for the system were 4.16 kV and 50 A. The system required two SiC SGTOs and two SiC diodes serially connected to form each leg of the switching position, for a total of eight SiC devices in the circuit. These devices each had a voltage rating of 5 kV, which is lower than the 8 kV devices to be used in the full scale system. The biggest difference between the scaled-down SSFCL prototype and the full scale system is the targeted current ratings. The scaled-down prototype requires no paralleling of devices and the current rating of the system matches that of a single (de-rated) SiC SGTO or SiC diode. The same type of varistors were used for this initial circuit (the V202BB60), only with the four of them connected in series in order to attain the desired voltage. The snubber circuit values were chosen using similar analysis as previously outlined, and the final values were determined to be 1 μF and 30 Ω for the snubber capacitor and resistor, respectively. A SolidWorks diagram and photograph of the original system are shown in the Figs. 6.1 and 6.2.



(a)

(b)

Fig. 6.1. 10 kV, 50 A SiC SSFCL prototype with (a) exploded view in SolidWorks and (b) system photograph.

For the testing to be detailed, the prototype was slightly modified. A single module, consisting of a SiC SGTO and SiC diode connected in series and having dimensions of 2 in. × 1.625 in. (50.8 mm × 41.275 mm), was used. The SiC SGTO was rated for 7 kV and the SiC

diode was rated for 10 kV. Thus, the module has bidirectional blocking capability of up to 7 kV. A photograph of the module is shown below, as well as the I-V curve.

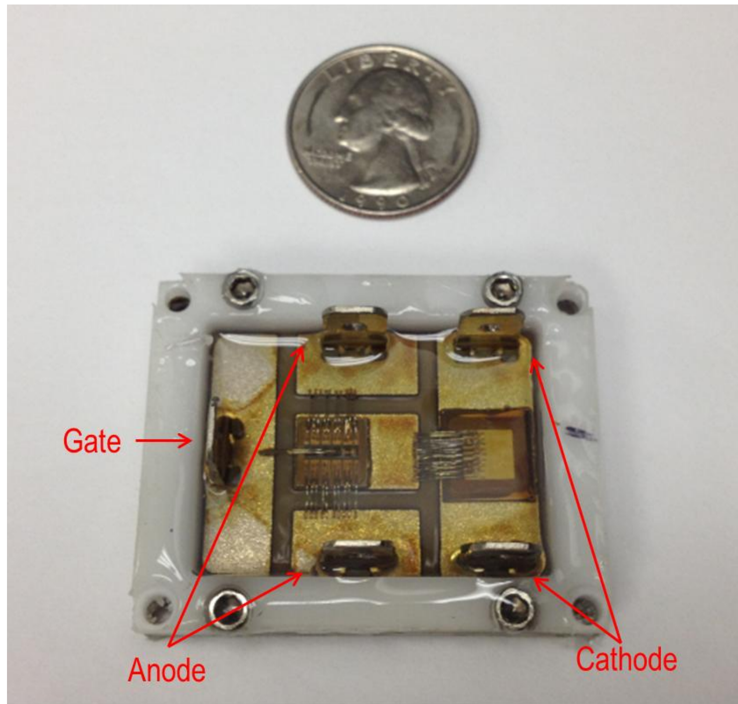


Fig. 6.2. SiC power module with SGTO (left die) serially connected to diode (right die) via wire bonds.

Since this system was originally designed for the 5 – 10 kV range, the snubber circuits and varistors are designed to operate at a much higher voltage. No upstream inductance was used for this initial testing in order to limit overvoltages with high *dv/dt* values since the clamping voltage of the varistors was well beyond that which was expected to be encountered with this testing. Lastly, the maximum voltage with this phase of testing was conducted at 120 V and 208 V, which are well below the rated capability of the devices. As noted before, this test setup is intended to verify the operation of the controller and the control algorithm, as well as the performance of the gate drivers before full scale testing was to begin.

6.1.1 120 V Testing

A schematic and photograph of the test setup are shown below.

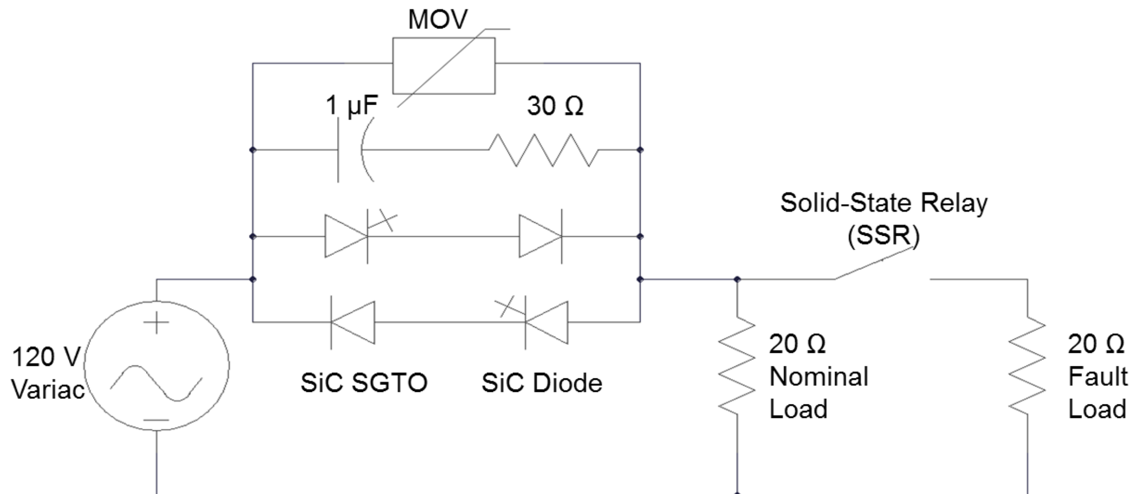


Fig. 6.3. Schematic of 120 V test setup.

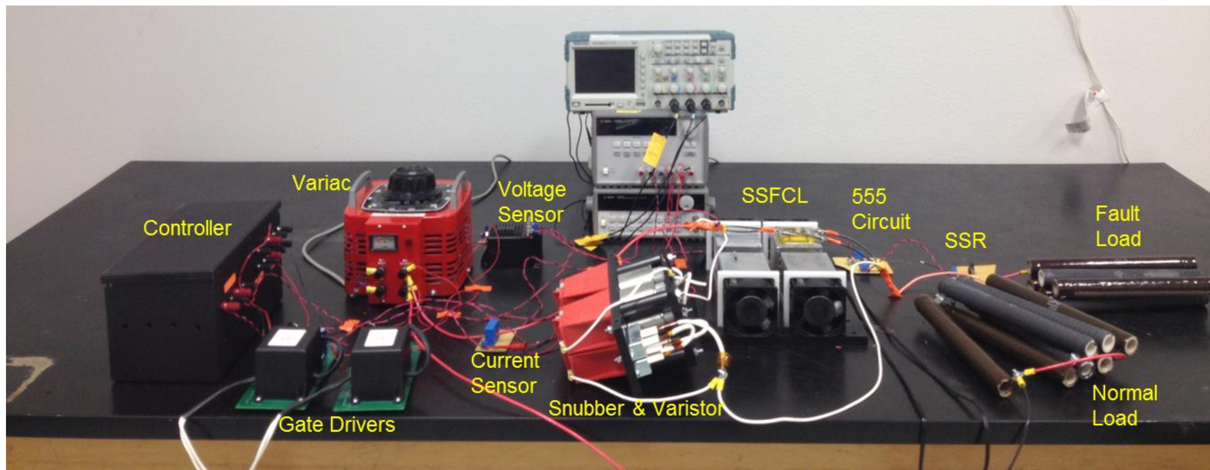


Fig. 6.4. Scaled-down SiC SSFCL test setup.

An additional load is connected in parallel with the nominal load via a Crydom CX240D5 solid-state relay. This relay was driven by a 555 one-shot circuit, with variable pulse width so that both temporary and permanent fault situations could be emulated. A LEM CV3-500 voltage sensor was used for zero crossing detection, and a LEM LA55-P current transducer was used for

sensing the value of the line current. The system was designed to be operated at a nominal current of about 6 A_{RMS} with a fault current of 12 A_{RMS}.

Some of the fundamental characteristics of the system were evaluated. For a 120 V_{RMS} system with a RMS current of 6 A (8.5 A_{PEAK}), the voltage drop across the device was measured to be 8 V. This equates to system losses at normal operating conditions of 68.8 W. The efficiency of the SiC SSFCL at this reduced voltage level is therefore approximately 95%. It is expected that the efficiency of the SiC SSFCL will improve at higher voltage levels; the large built-in potential of SiC power devices is somewhat disadvantageous when operating at lower voltages. The gains in SiC device efficiency may be negated by the addition of the series resistors that are required for proper current sharing.

One critical element of SiC SSFCL development was the gate driver design. Device characterization showed that SiC SGTOs required higher turn-off currents than traditional silicon GTO devices, and this is viewed as a potential setback in the development of SiC SSFCL systems for distribution systems. For the scaled-down system, current interruption during the first cycle of the emulated fault current was performed. The controller was programmed for 10 A_{RMS} (14.1 A_{PEAK}) for fault current interruption. The peak interrupted value was consistently recorded in the range of 13.0 A to 14.0 A over the duration of testing. Fig. 6.5 below shows the current interruption performed by the SiC SSFCL prototype.

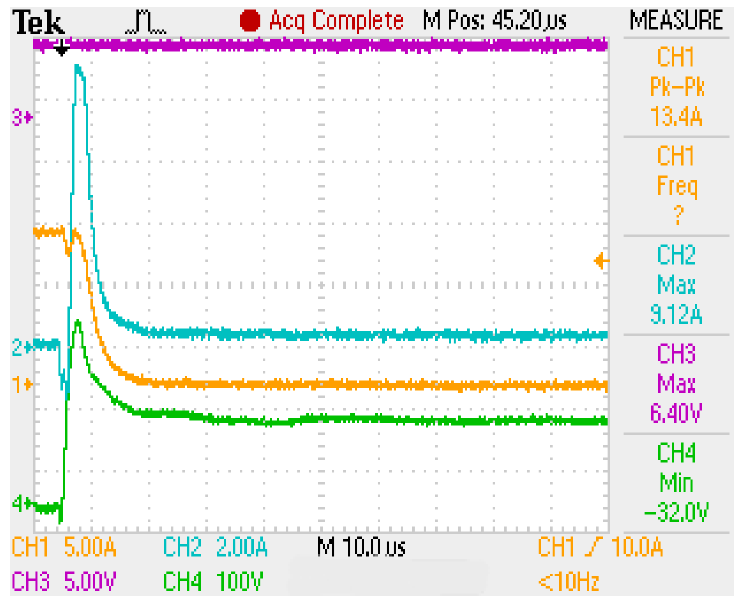


Fig. 6.5. Current interruption in 120 V test setup: CH1 (orange) – system current, CH2 (blue) - gate current, CH3 (purple) - solid-state relay control voltage, CH4 (green) -voltage across SiC module.

As indicated in the figure, the peak fault current interrupted was 13.4 A, equating to an RMS value of about 9.5 A, producing highly accurate results. The turn-off gate driver is constructed with no limiting impedance at the output; this means that the current required to turn-off the SiC SGTO is dictated by the anode-cathode current of the device. As seen in the figure, the maximum gate current provided during this period is 9.12 A. The ratio of the gate current required for turn-off to the anode-cathode current through the device is 0.68, which is close the value of 0.7 that was determined through device characterization. The rise time of the gate current is 2 μs before reaching its plateau. The gate current is then fairly constant, with only a slight decrease over 2 μs. It is at the end of this period that the device is able to sustain a blocking voltage, and the system current rapidly begins to fall thereafter. In all, the total turn-off time required as measured from the beginning of the upward slope of the turn-off gate driver to its return to a steady-state value is 11 μs. The amount of upstream inductance used in this test

setup was minimal, and it is anticipated that an increase in the inductance will directly correlate to a prolonged turn-off period.

Initial testing also included evaluating the ability of the system to distinguish between faults deemed to be temporary and those deemed to be permanent. The control algorithm is developed such that after a fault is detected, the current is immediately interrupted and after a five cycle delay, a twenty cycle period of current limiting ensues.

Fig. 6.6 shows the current of the system being limited during a permanent fault condition. This fault lasts more than 500 ms. During the first cycle of the fault current, interruption occurs at a peak value of 14.0 A. During limiting, the initial phase angle is specified as 170°, equating to a phase delay of 7.9 ms. The percentage of fault current reduction at this phase angle is 82.7% in comparison to the steady-state fault current value. Each cycle, the phase angle is reduced by 8.5° if the current is below the fault threshold.

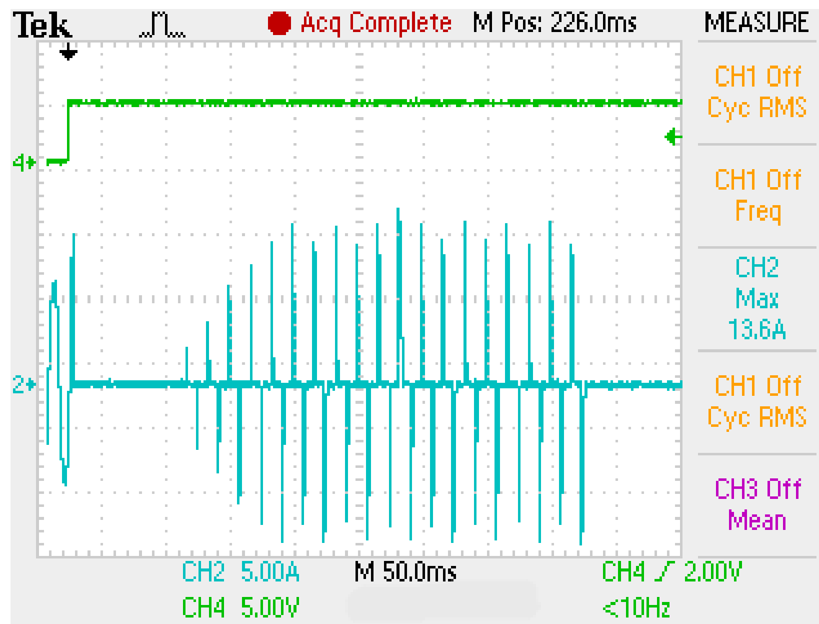


Fig. 6.6. SiC SSFCL reaction to permanent fault: CH2 (blue) – system current, CH4 (green) – relay signal used to indicate fault.

The phase angle is reduced to a value of 127.5° before the system current reaches the threshold value. In this instance, the threshold value during current limiting is the same as the current threshold value used to determine that a fault has occurred. This is 80% of the potential peak current value of 16.97 A due to the fact that the maximum fault current value in this test system is not much higher than the selected threshold value. During the next current cycle, the phase angle is again increased to 136° (69% of maximum steady-state fault current), which is below the threshold value. The system control is configured such that the phase angle is varied each cycle, even during current limiting, in an attempt to continuously evaluate the system state and determine if the fault has subsided. There is a maximum current limit that is never exceeded during any point in the operation. The phase angle increment is 8.5° in this configuration due to the fact that the limiting period is 20 cycles. A greater degree of accuracy and resolution can be attained if longer limiting periods are used. At the end of the twenty cycles, the system current is interrupted after it is determined that the fault is still present.

Fig. 6.7 shows simulations results of the scaled down prototype in the 120 V test setup for permanent fault conditions. The circuit was simulated in Saber using the schematic of Fig. 6.3. The experiment and simulations produce comparable results, verifying the accuracy of the simulation for the control algorithm implemented.

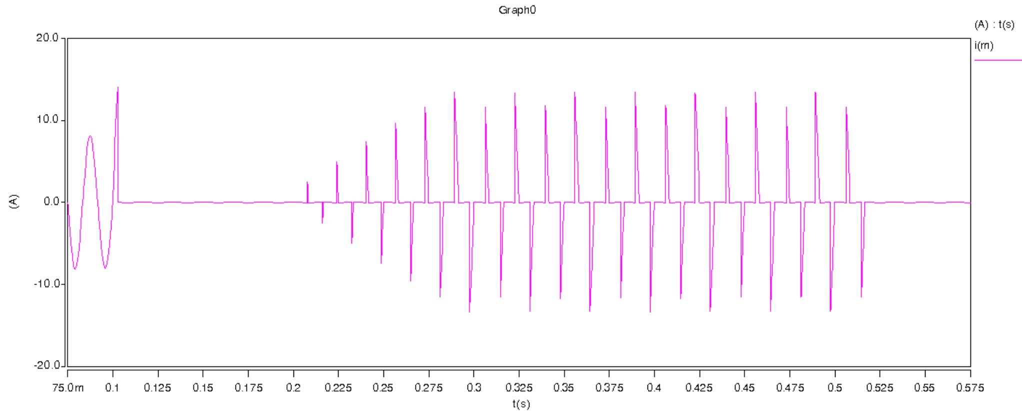


Fig. 6.7. Simulation results for 120 V test setup. System current under temporary fault with results comparable to those shown in Fig. 6.6.

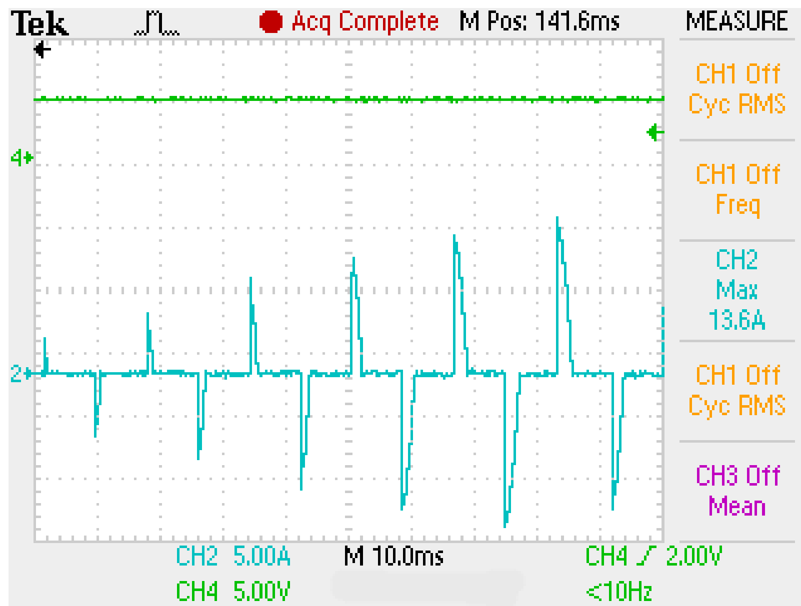


Fig. 6.8. The beginning of phase angle control during which the phase angle is reduced from 170° to 127.5°: CH2 (blue) – system current, CH4 (green) – relay signal to indicate fault.

In the event of a temporary fault, the SiC SSFCL control is configured such the system returns to normal operation automatically without the need for a manual reset. Testing results for the system response to a fault duration of approximately 100 ms is shown below. At the beginning of the limiting period, the fault has already subsided as indicated by the relay signal in the figure.

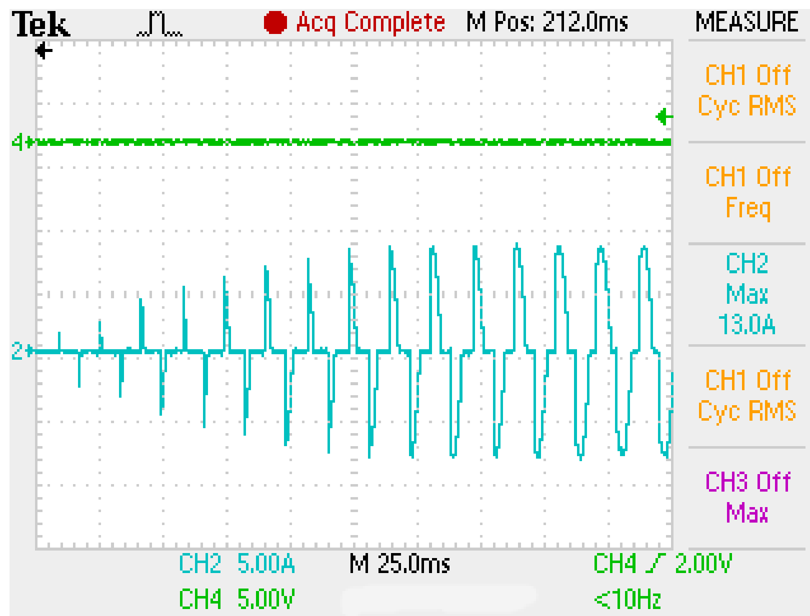


Fig. 6.9. System response to temporary fault: CH2 (blue) – system current, CH4 (green) – relay signal used to indicate fault presence.

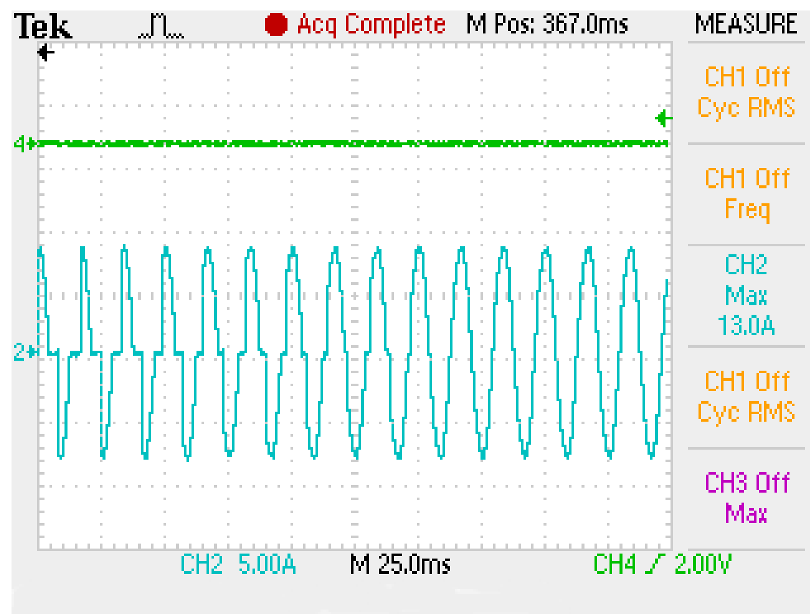


Fig. 6.10. Seamless return to normal conduction mode at end of current limiting: CH2 (blue) – system current, CH4 (green) – relay signal used to indicate fault.

The SiC SSFCL prototype demonstrated the required functionality at lower current levels by successfully interrupting an emulated fault current. The system was also able to limit the fault current to a predetermined value in the event of a permanent fault event. In a temporary fault

event, the system was able to successfully return the system to normal operation after determining that a fault event was no longer present.

Simulation results for these conditions were also obtained, as shown in Fig. 6.11. For temporary fault conditions, the angle is gradually decreased by 8.5° each cycle until normal conduction is re-established. The results obtained in the simulation match those of the experimental test setup.

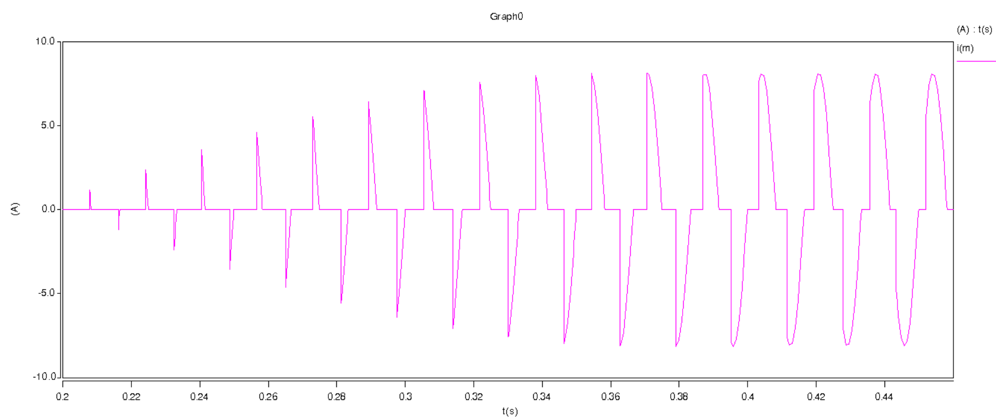


Fig. 6.11. Simulation results for 120 V test setup. System current under temporary fault conditions with results comparable to those in Fig. 6.9.

6.1.2 208 V Testing

Testing was conducted in a three phase test setup in order to evaluate system operation at higher current levels. The system line-to-line voltage was 208 V, and with a potential fault current of 42 A_{PEAK}. A schematic of the test setup is shown in Fig. 6.12.

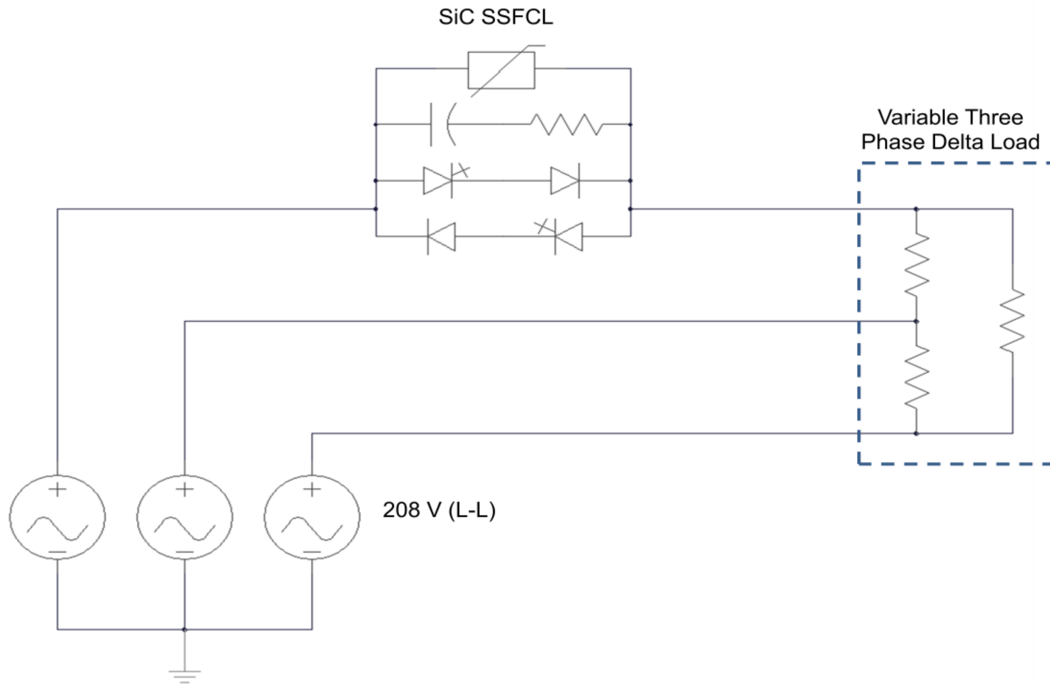


Fig. 6.12. Schematic of 208 V test setup.

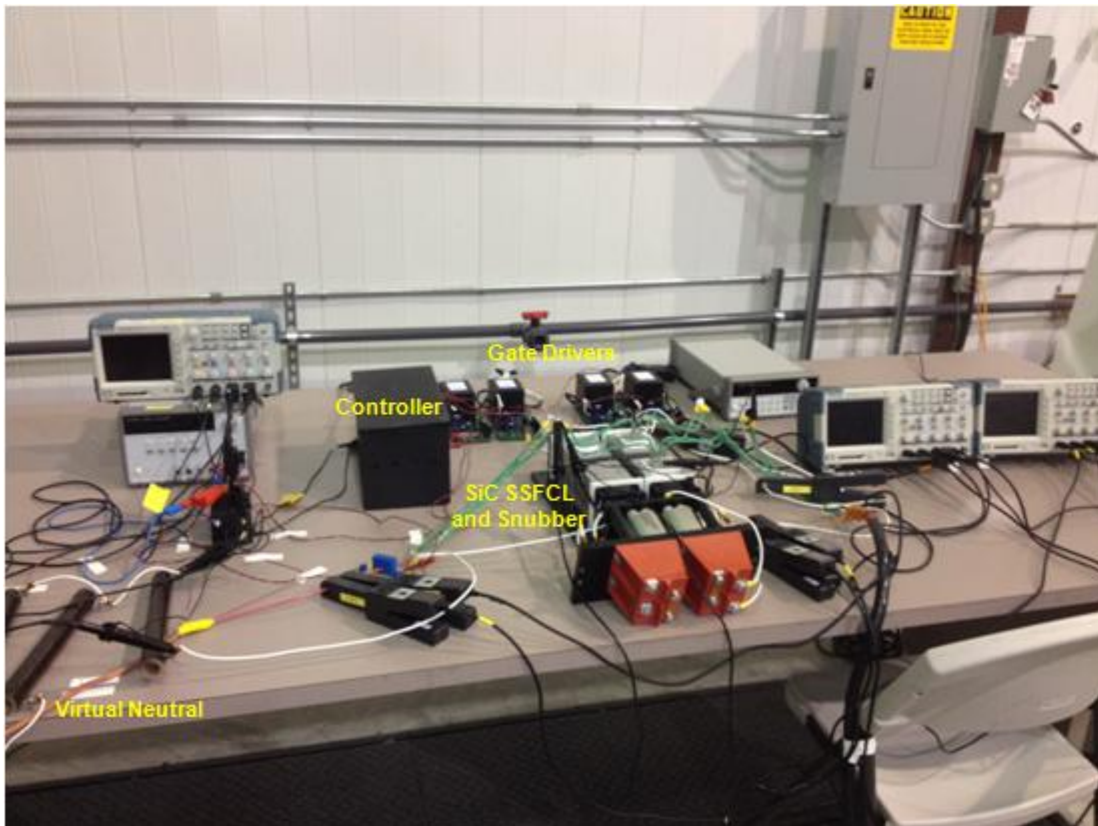


Fig. 6.13. Photograph of 208 V test setup.

The sensors utilized for this test setup were the same as those in the 120 V setup. Instead of using a solid-state relay to switch in an additional load for fault emulation, a digitally controlled three-phase delta-connected load bank was used in order to handle the higher current. The SiC SSFCL controller requires a phase-to-neutral voltage measurement for proper operation. The gate signals are delivered to the appropriate SiC SGTO at the beginning of each half cycle. The system neutral is not accessible in the test setup, and accordingly a virtual neutral is used for this testing. This consists of three wye-connected 1 kΩ resistors connected upstream of the SiC SSFCL, with the midpoint used as the neutral for the controller measurements (not shown in Fig. 6.12).

The nominal peak current for the 208 V test setup was 14 A. Under these conditions, the voltage drop across the SiC SSFCL is measured as 10.4 V, which equates to system conduction losses of 145.6 W. The system efficiency at this level is measured as 94.9%, which is consistent with the calculation as determined for the 120 V testing setup.

Testing was performed in order to evaluate the ability of the system to interrupt and limit the fault current to a peak value of 30 A. Fault emulation was performed by a step change in load from 5 kW to 15 kW. The load has fast response time for accurate fault emulation, but since the load is manually operated, there is only the potential to evaluate current limiting under permanent fault conditions. Fig. 6.14 shows the fault current interruption and subsequent current limiting.

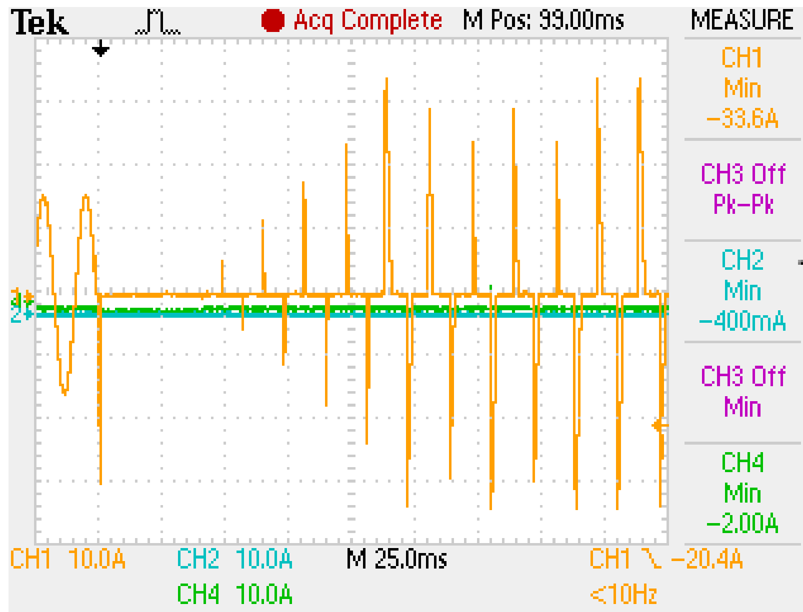


Fig. 6.14. Fault interruption and current limiting: CH1 (orange) - system current, CH2 (blue) - snubber current, CH4 - (gate drive current).

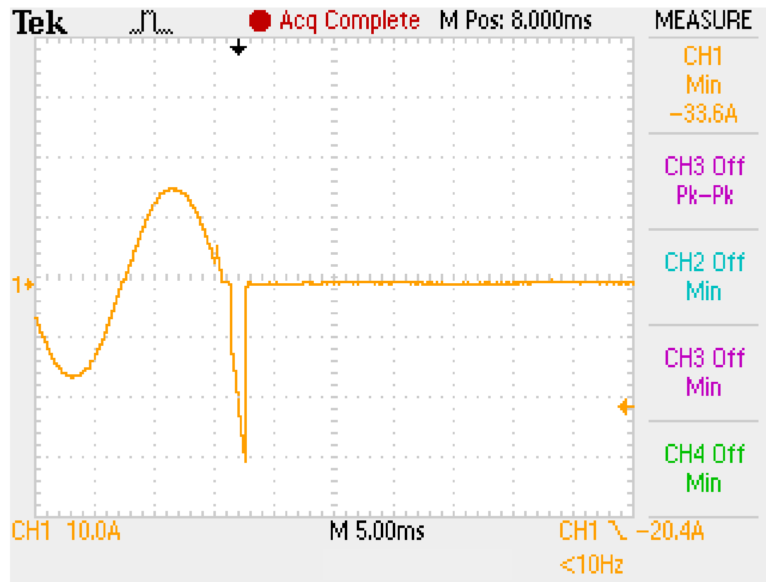


Fig. 6.15. Current interruption at 30 A: CH1 (orange) – system current.

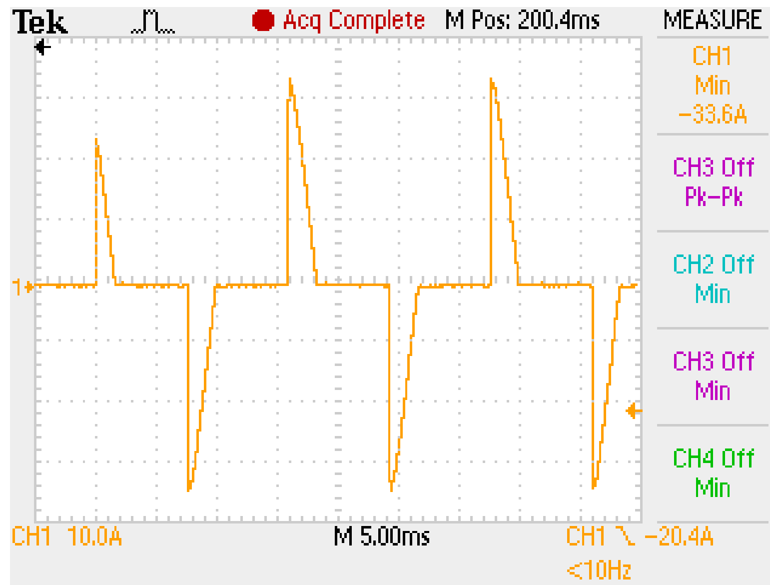


Fig. 6.16. Current limiting via phase angle control with phase angle decreasing from 136° to 127.5°: CH1 (orange) – system current.

Current interruption occurs during the negative half cycle, at a value of 30.0 A. Phase angle control begins, during which the phase angle is decreased from the initial value 170° to the limiting value, which is 127.5°. The sampling rate of the current probes, which was 5000 samples/s, used for data acquisition in this setup did not accurately capture the current peaks during the limiting period of the positive half cycle in Fig. 6.14, but examination of the negative half cycle show the intended effect is obtained. The maximum value of the current during the limiting period is 33.6 A, which is obtained at the phase angle of 127.5° and slightly above the threshold value. As mentioned before, smaller resolution of the phase angle increments during each period of current limiting could prevent such a matter from occurring in future testing.

Simulation of the 208 V test setup for the specified conditions yielded the results in Fig. 6.17, which align closely with those of the experimental results in Fig. 6.14. Current interruption occurs during the negative current peak at a magnitude of approximately 33 A, with current limiting to the same value. Slight differences between the simulated and experiment results can attributed to the current probe resolution errors, as explained previously.

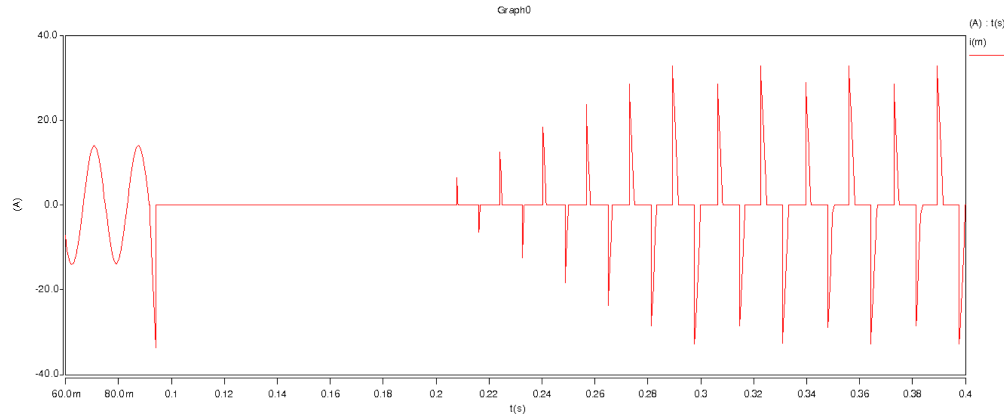


Fig. 6.17. Simulation results for 208 V test setup. System current with results comparable to those in Fig. 6.14.

6.1.3 System Analysis

Potential system concerns for this type of SSFCL include the overvoltage that occurs during the current interruption and the harmonic distortion of the current signal during phase angle control. For the 120 V test setup, overvoltage issues were largely non-existent due to relatively small system inductance and interrupted current value. Inductance values of up to 234 μH used upstream of the SiC SSFCL yielded no significant overvoltage upon current interruption in this setup. Overvoltages in the 208 V test setup proved insignificant as well due to lack of system inductance.

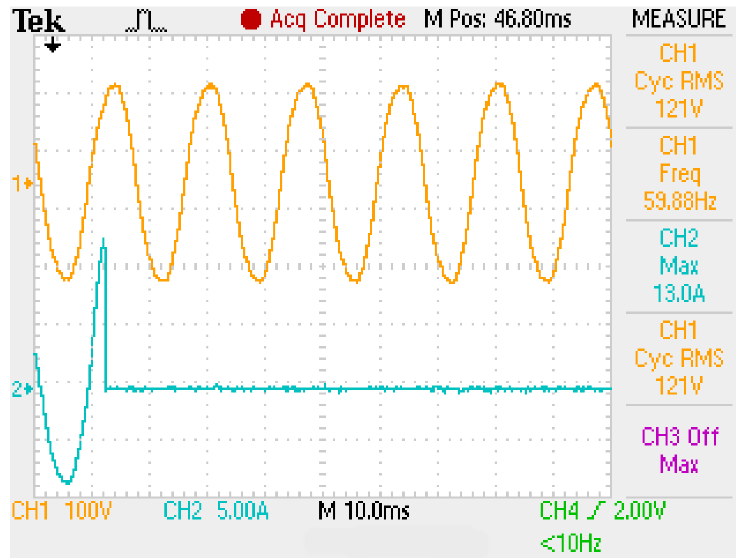


Fig. 6.18. System voltage at current interruption: CH1 (orange) – system voltage, CH2 (blue) – system current.

The system current was analyzed during current limitation in order to determine the extent of the harmonic distortion. In order to do this, the signal of Fig. 6.6 was sampled over 10 cycles of current limiting and a Fourier analysis was performed. The frequency spectrum of the signal is shown below.

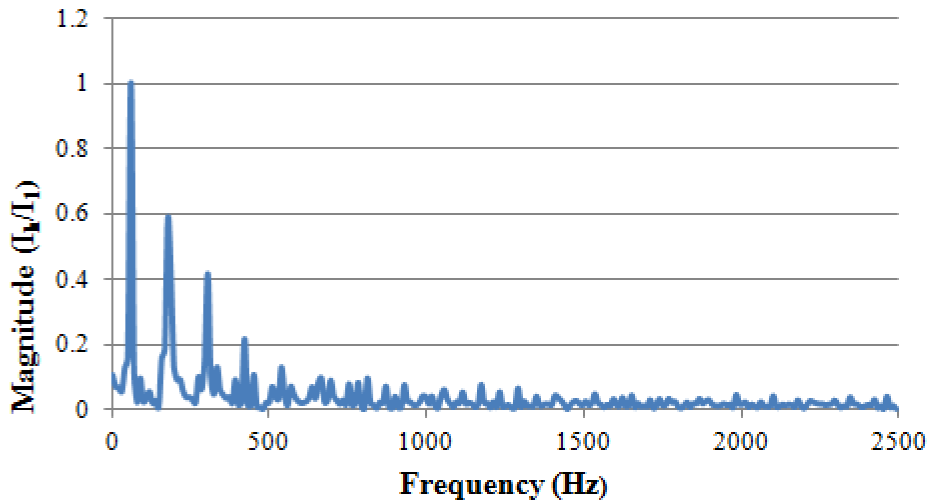


Fig. 6.19. Fourier analysis of current signal during fault current limiting.

Table 6.1. Harmonic Components of Current Signal During Current Limiting.

Harmonic Component	Percentage of Fundamental (%)
1 (60 Hz)	100
3 (180 Hz)	58.21
5 (300 Hz)	41.63
7 (420 Hz)	21.69
9 (540 Hz)	13.00

As indicated in the graph, there is a significant amount of harmonic distortion in the system during current limiting. Using the values of Table 6.1 and substituting into Equation 5.2, the total harmonic distortion of the current during this period is calculated as 0.76. The high magnitude of the third harmonic component could prove especially problematic if operation in the current limiting mode was to take place over an extended period. The value is still high, but lower than that obtained in the simulation conditions of the previous chapter. Two factors likely contribute to this reduction. The phase angle is for current limiting has a maximum value of 136°, which is slightly less than the 145° obtained in the simulation. Also, the smaller value of the snubber capacitor, along with the larger value of the snubber resistor, restricts the current flow through the snubber path in this small-scale setup during current limiting. As mentioned before, current limiting operations will likely be limited in duration, and as is the case here, sub-second durations will be typical. These types of events are generally classified as transients, and tolerances for the harmonic components are allowed to exceed what would generally be seen in steady-state operation.

Concerns regarding SiC devices in an application such as the SSFCL are related to the long-term stability of the devices, and also the paralleling capability. SiC bipolar devices have been prone to voltage degradation when subjected to long-term operation and temperature increases.

Voltage degradation is a condition in which the on-state resistance of the device is permanently increased due to SiC material defects known as basal plane dislocations. Sustained operation under high current density and increased temperature leads to stacking faults within the device, which in turn cause a shift in the permanent on-state characteristics of the device. While this problem has largely been mitigated over the past couple of years, this phenomenon was investigated using the scaled-down version of the SiC SSFCL. The scaled-down prototype was operated under steady-steady conditions for an extended period, and the I-V curves of each of the modules within the SiC SSFCL were evaluated before and after. The maximum current during this period was 10 A. Fig. 6.20 also shows the I-V curve of Module 3, which was used exclusively in the 208 V testing setup.

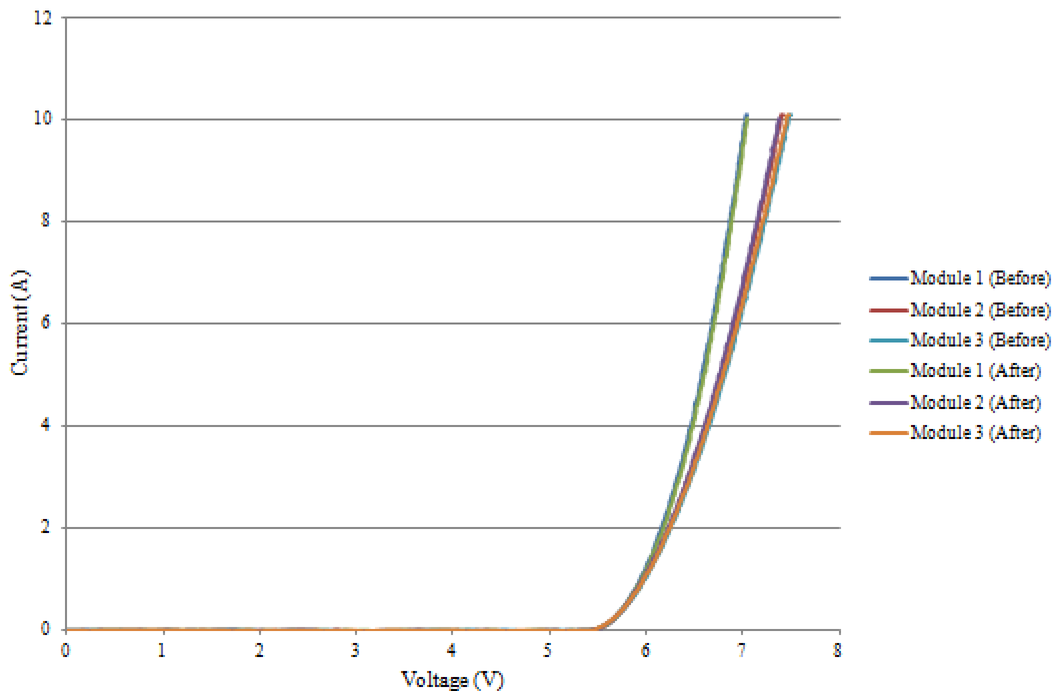


Fig. 6.20. On-state characteristics of SiC modules before and after testing.

These results indicate no shift in the on-state characteristics of any of the modules used in testing. The on-state resistance of Module 1 is 103 mΩ before and after testing, compared to 145 mΩ for module 2. Module 3 has a constant resistance value of 145 mΩ as well. While the

devices used for this testing showed no change in characteristics, the potential for voltage degradation needs to be investigated continuously when evaluating SiC devices for fault current limiter applications. For testing that occurs at a greater percentage of the rated device current, this issue can be better analyzed. The advantage to using these devices in the SiC SSFCL is that it is an alternating current circuit application, and the onset of any potential adverse effects is delayed since the devices only conduct for a half-cycle of the fundamental frequency for normal operation. The voltage degradation of the device is typically a function of the device steady-state current and operating temperature, and needs to be re-evaluated under rated conditions of the SiC SSFCL.

Another condition that was evaluated was the parallel operation of the SiC devices modules under the specified conditions of the 120 V test setup. Module 1 and Module 2 were used for this testing. As evidenced by the I-V curves in Fig. 6.20, there is a difference in the on-resistance of the two modules. Parallel operation of the modules at 10 A resulted in only a slight mismatch of current, with Module 1 carrying 54% of the current. Sustained steady-state operation yielded no change in the ratio of the currents in the two modules. However, as is the case with the investigation of voltage degradation, the paralleling capability is best evaluated under full-scale conditions.

6.1.4 Testing Challenges

Testing of the full-scale prototype is still an ongoing process. During 208 V testing, a catastrophic failure of one of the SiC SGTOs was encountered. Fig. 6.21 shows the gate and anode connections of the failed device after testing.

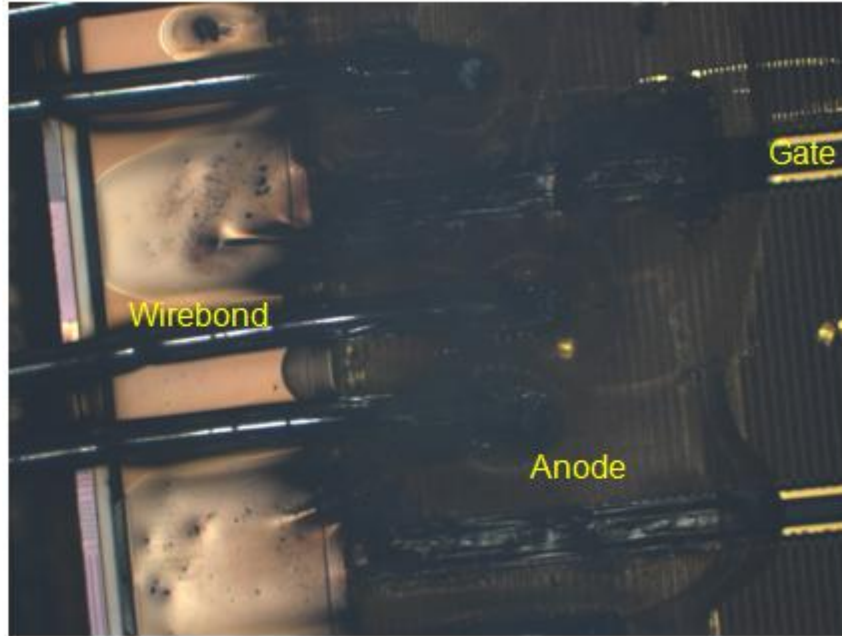


Fig. 6.21. Photograph of failed SGTO indicating damage to gate, anode, and wirebonds.

It can be seen that there is extensive damage to the anode, gate, and wirebonds of the SiC SGTO device. During the initial phases of this testing, the gate current gain required for turn-off was approaching unity; meaning for a 30 A fault, nearly 30 A of gate current was needed for turn-off. Due to the visible damage to the gate connections, it is anticipated that this current may have been too high for this particular device based on the gate area, which caused thermal complications that damaged both the device and wirebonds. Thus, in order to adequately evaluate the problem before continuing testing with more of the SiC diodes, evaluation of the device failure and device packaging are being further investigated before moving on to testing of the system designed in Chapter 4 at high voltages and currents.

CHAPTER 7

FEASIBILITY ANALYSIS OF SILICON CARBIDE FAULT CURRENT LIMITERS

7.1 Cost Analysis of Current SiC SSFCL Systems

One of the main issues in the development of the SiC SSFCL will be the cost. SiC SSFCLs not only have to offer superior performance, but they must have competitive costs as well. Naturally, most fault current limiter systems will cost more than conventional protection equipment such as circuit breakers. Many utilities have expressed a willingness to pay for a fault current limiter system provided that the cost is no more than twice that of a similarly sized circuit breaker, with some expressing a readiness to spend five times the amount [19].

The performance advantages that will be offered by SiC SSFCLs over silicon systems have been stated in detail in previous chapters. For distribution systems in the 15 – 35 kV range, silicon carbide based SSFCLs are considered better suited than superconducting systems as well. Superconducting fault current limiter systems are viewed as having the most potential in transmission systems, but are not being widely considered for use in distribution systems. This is because the power transfer capacity advantages offered by superconducting cables are not as substantial at distribution level voltages, giving utilities pause when considering replacing existing cable systems in this range [94]. Furthermore, superconducting fault current limiters are considered by some to be cost effective only at transmission level voltages above 138 kV [95]. For this reason, the 15 – 35 kV distribution range is a market for which the use of silicon carbide could be critical. Currently, SiC power semiconductor device ratings will restrict SSFCL system to the 4.16 kV level. Hereafter follows an examination of the current costs of a silicon carbide based SSFCL for power distribution systems.

The expenses associated with the construction of a 4.16 kV SiC SSFCL system will be compared with those of a sample set of 4.16 kV circuit breakers. The construction of a 15 kV class SiC SSFCL will require devices with much more substantial voltage and current ratings than what is currently available, and as such a detailed cost analysis of such a system was not conducted in the absence of these devices. The 4.16 kV circuit breakers under examination have current ratings of 1200 A, 2000 A, and 3000 A, which are standard current ratings for utility scale circuit breakers. Upon examination of various circuit breakers with similar ratings, the prices tended to lie within the $30K - $40K range, with most being towards the upper limit. Within the sample set of 4.16 kV, 350 MVA circuit breakers, the price was largely influenced by the current rating of the system. The cost difference between a 1200 A system and a 2000 A system was roughly $15,000, while a further increase from 2000 A to 3000 A warranted an additional increase of nearly $20,000. Based on current silicon carbide prices for 8-10 kV devices, which was calculated to be roughly $1822 per device, the cost per amp of each of these protection devices is illustrated in the graph below.

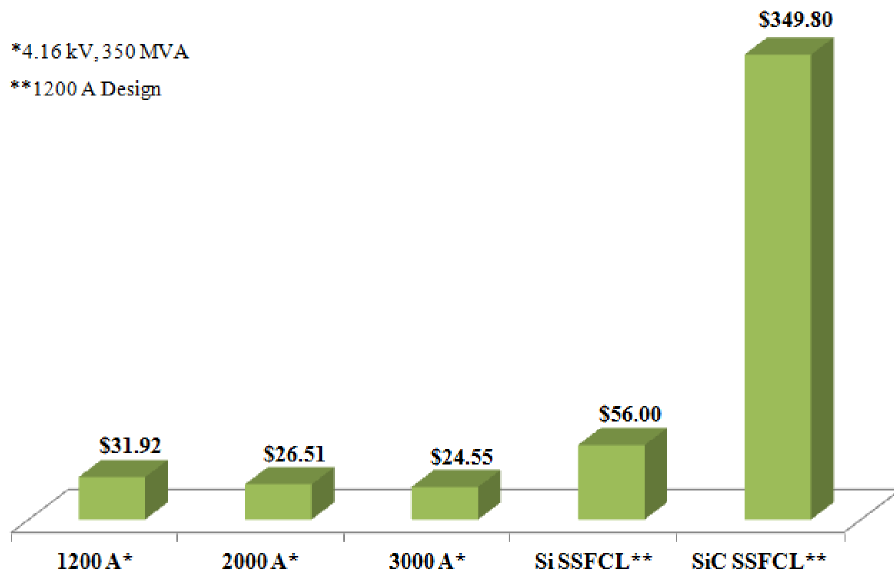


Fig. 7.1. Cost per amp of comparable 4.16 kV protection systems.

For this analysis, it was presumed that 8 mm × 8 mm 64 A SiC devices would be used in the construction of the three phase system. Future 4.16 kV systems will necessitate devices with higher current ratings, which could keep the overall part count to a minimum. Also, this analysis considers the costs of the devices alone, not additional components such as the cooling system, gate driver circuits, and controller. Presently, the cost per amp of a 4.16 kV SiC system is nearly eleven times greater than that for a 1200 A system with a 350 MVA rating.

A comparison between the SiC SSFCL and one constructed using silicon devices is also presented, but does not reflect a truly accurate assessment at the current time. The main reason is because SiC device costs are just starting to decline, while silicon represents a more mature and stable technology. Silicon processing techniques are more advanced, and the associated costs are much lower than those of silicon carbide. Also, silicon power module development allows for packages with substantial current ratings, while the cost analysis of silicon carbide presented earlier takes into account the cost of individual devices. Such devices with modest current ratings will not be used in the development of future SiC SSFCL systems, but are currently among the highest rated devices available. Power module development, especially for SSFCL applications, is still progressing. Nonetheless, the costs of developing a SSFCL system using a suitable power semiconductor device, chosen to be the silicon integrated gate commutated thyristor (IGCT) from ABB, are presented.

There are many choices for an appropriate silicon power semiconductor device for SSFCL applications. This device is chosen because it has substantial voltage blocking capability (4.5 kV) and it also has higher current ratings than most silicon devices available on the market. It has also been demonstrated for use previously in solid-state protection circuitry. It has a maximum average on-state current of 1700 A, and a maximum RMS on-state current of 2760 A

[96]. Thus, one device would be sufficient for 1200 A operation, which is the basis of comparison used for the SiC SSFCL and circuit breakers for this cost analysis. This is an asymmetrical device, and as such a reverse blocking diode would be needed for SSFCL operation. The average cost of these devices is approximately $2800. For a 4.16 kV, 1200 A three phase SSFCL, 24 devices would be needed (four IGCTs and four diodes per phase), equating to about $67200 in device costs. When compared on an equal scale to the silicon carbide and circuit breaker systems of Fig. 7.1, this puts the cost per amp at roughly $56. As is the case with the SiC analysis, this does not even factor in the maintenance costs or the costs of auxiliary systems. However, it can clearly be seen that for a device with a much higher current rating, the cost of a single silicon device suitable for an SSFCL system is much more reasonable. Another added advantage is that IGCT devices come with integrated gate drivers. Silicon carbide technology simply has not progressed to this point. Furthermore, the fact that silicon devices suitable for SSFCL systems are available commercially gives the manufacturers an incentive to be cost competitive, knowing that there are other viable options on the market. It is to the advantage of the consumer to have SiC power semiconductor devices such as the GTO and IGBT commercialized in order to create a competitive market that ultimately drives the prices down. According to independent research performed in [97], the average selling price of SiC power MOSFETs, the current driver for SiC commercial devices, is expected to drop nearly 45% between 2013 and 2021. Availability of these devices from different manufacturers can drive the prices down further, and this will be essential in making SiC power devices affordable for SSFCL use.

A breakdown of the costs of the single phase SiC SSFCL prototype is shown below. This includes only initial costs, and does not take into account the maintenance costs and the cost of power module development.

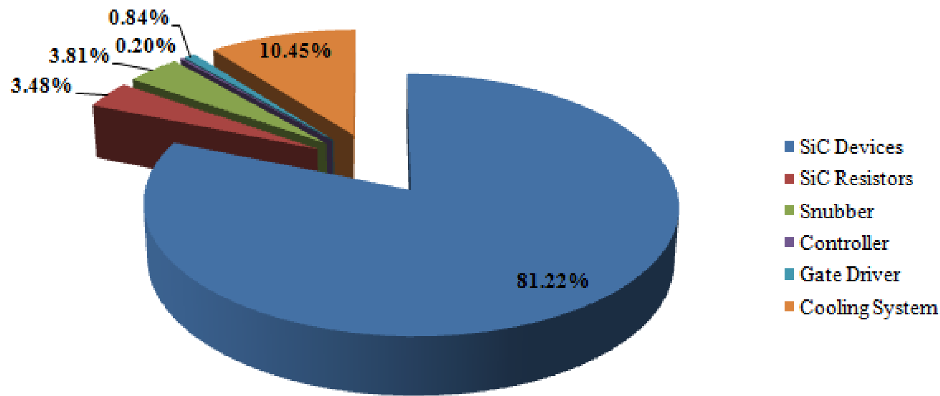


Fig. 7.2. Cost breakdown of single phase 4.16 kV SiC SSFCL.

As can be seen in the figure, the cost of the SiC devices constitutes more than 81% of the overall system expenses. In order to make the system economically feasible, the costs of the SiC devices have to decline dramatically. One of the issues with the use of SiC GTOs is that they are available only as experimental devices at this point. A dedicated fabrication run is needed for these devices, and estimates place the cost of a SiC wafer fabrication at an order of magnitude higher than that of a similar silicon wafer fabrication. It is well documented that the price of SiC devices is expected to decrease immensely once 4" and 6" wafers become available [98]. At this point, the devices can be produced using the same equipment and processing that is currently used for silicon devices. It is expected that this will drive the prices down as much as 50%. It is

anticipated that these wafers will become available in 2012 or early 2013. As mentioned earlier when discussing trends of SiC power MOSFETs, the prices of most, if not all, silicon carbide power devices will decrease steadily over the course of the next decade [97], [99]. Based on these estimates, a price reduction of approximately 82% would be presently needed in order to reduce the initial price of the system to a level attractive to utilities based on the rating of the available SiC devices. This is predicated on use of 8 kV, 64 A devices for the system. As device technology progresses, SiC devices of higher voltage and current ratings will be used for the development of SSFCLs for this distribution class.

Current SiC SSFCL costs for 15 kV class systems pose even more of an issue. The price of 13.8 kV circuit breakers of the sample set chosen for the analysis ranged from about $42,000 for a 500 MVA, 1200 system to about $82,000 for a 1000 MVA, 3000 A system. Based on the present costs and device ratings, a SiC system currently would be unfeasible at this level. The cost per amp of the system is at least three times that calculated for the 4.16 kV SiC SSFCL based on the number of 8 kV devices required to be connected in series. For this reason, a combination of factors such as increased wafer size and quality, larger die area, and reduced processing costs are all needed in order for these systems to become economically viable.

7.2 Analysis of SiC SSFCLs for 15 kV Distribution Systems

Although SiC based SSFCLs have many potential benefits in power distribution system applications, there are many issues that still need to be investigated and resolved. This is especially true when evaluating the use of SiC based SSFCLs at the 15 – 35 kV level. As illustrated in the previous section, the costs of SiC power devices needed to construct such systems remain high for the foreseeable future. Many of the other issues are related to the use of silicon carbide power semiconductor devices in such a demanding application. The SiC SSFCL

has a unique circuit design in that the ratings that must be endured are unlike those for any other power electronic based system. While not subject to high frequency switching, the devices used in the SiC SSFCL have to conduct large values of current. Nominal system currents for 15 kV systems are 600 A, and can easily surpass this value during peak demand periods. Furthermore, these devices have to be able to reliably operate under repeated fault conditions. According to IEEE Std. C37.06-2009, some circuit breakers for 15 kV class systems are expected to endure up to 2000 operations before servicing is required, and SiC SSFCL systems will have similar expectations [100]. The SiC devices in these systems not only have to withstand these high fault currents and subsequent transient overvoltages, but also must operate consistently and predictably under normal conditions. Presently, the best devices for use in SiC SSFCL applications are the SiC GTO and the SiC IGBT, even though both are still under development. In order to determine the feasibility of 15 kV class SiC SSFCLs, a brief comparison of the devices is conducted.

7.2.1 Potential Issues with the SiC GTO in SSFCL Applications

The SiC GTO was used for development of the SiC SSFCL prototypes developed for this research. There are a number of benefits to the use of this device, but as demonstrated through the investigations made during the design of the prototype, there are a number of disadvantages as well. The SiC GTO, just like its silicon counterpart, is the most robust of the power semiconductor devices. Its ratings and ruggedness will remain unmatched among its silicon carbide counterparts. Anticipated ratings of SiC GTO devices are expected to ultimately end up in the 40 kV range, with current ratings close to 900 A for device with lower voltage ratings [66], [101]. It is not anticipated that the structure of this device will change. The power losses of these devices will remain lower than those of other semiconductors, especially as the ratings increase,

and the surge capabilities will make it most suitable for use in SSFCL systems. Simulations performed in [102] for 20 kV SiC IGBTs and GTOs showed that based on a power density limitation for 300 W/cm^2, which is a presumed limitation of the power package, SiC GTOs can operate at current densities that exceed 80 A/cm^2, while the nearest competitor, the SiC IGBT, can function in the 40-50 A/cm^2 range. As such, aggressive thermal management is needed in order to push these devices into the desired 100 A/cm^2 range of operation. For these devices, the main challenge for its use in a SiC SSFCL will still remain in its ability to be utilized in parallel configurations as part of a suitable switching position.

For silicon carbide bipolar devices, specifically diodes and thyristor devices, a positive temperature coefficient of on-state voltage drop is only experienced at relatively high current densities. Silicon devices undergo a phenomenon called inversion, in which the temperature coefficient of the device transitions from negative to positive at current densities on the order of less than 100 A/cm^2. At lower current densities, the voltage drop reduces with increasing temperature due to the reduction of built-in potential, but as the current density increases, the mobility and diffusion coefficient within the device reduce as well. Also, some of the nonlinear device processes, such as electron-hole scattering, bandgap narrowing, and Auger recombination, become the dominating effects within the device during steady-state operation and lead to an increase in voltage drop with increasing temperature [103]. This same effect occurs within silicon carbide devices, but at a much higher current density. As detailed earlier, the current density of inversion for the SiC GTO is at 300 A/cm^2. For a material that is typically rated by wafer manufacturers at 100 A/cm^2 it is impractical to anticipate steady-state operation of the device at three times this current density, even with aggressive thermal management. As the voltage ratings of these devices increase and the drift region thickness increase, the effect is

likely to be compounded. Thus, for high voltage SiC GTOs in the 20 – 40 kV range, paralleling will remain the prominent issue. The shortcoming with GTOs and all thyristor type devices is the lack of gate control during the on-state. Once the latching current of the device is exceeded and the device turns on due to regenerative action, the output characteristics of the device can no longer be influenced by the gate. Various gate control methods that may be implemented to promote current sharing have little impact. The current sharing issue in SiC GTOs is not one related to material defects, but rather one governed by fundamental material properties.

Another concern related to the use of SiC GTOs in the development of SSFCLs for distribution systems is the turn-off of the device under fault conditions. While GTO devices have turn-off capability through the gate, it is typically ill-advised to perform gate turn-off during surge conditions, such as would be experienced during fault conditions. For this reason, EPRI's silicon based FCC prototype utilizing GTOs employed a commutation circuit similar to those used with conventional thyristors in order to achieve forced turn-off. The energy required to successfully turn-off the device dictates that the size and volume of the capacitors be quite substantial in comparison to the rest of the system components. Earlier investigations into SiC SSFCL use with SiC thyristors utilizing forced commutation circuits demonstrated that the use of SiC devices would reduce the size of the commutation capacitor to one that was $1/10^{th}$ the value of a comparable capacitor used in a silicon system, due to the much faster turn-off times [91]. Due to more robust device development in recent years, SiC GTOs have been demonstrated for pulsed power applications well beyond the currents typically seen in distribution systems with gate turn-off. The gate structure of these devices must be further improved if the use of bulky commutation circuits is to be avoided.

7.2.2 The Potential for SiC IGBTs in SSFCL Applications

Due to the potential drawbacks of using the SiC GTO in fault current limiter applications, the SiC IGBT will be investigated as a possibility. The device ratings for the IGBT are not expected to be nearly as high as the SiC GTO, but the ratings may suffice for operation in 15 kV class distribution systems. The device roadmap for SiC power devices suggests that SiC IGBTs with ratings of up to 20 kV will be available, with 15 kV, 100 A SiC IGBT modules already being investigated for development [104]. Many SiC power device manufacturers have predicted that the SiC IGBT will be the dominant device for 10 – 20 kV device applications in the future [71]. As is the case with SiC GTOs, most SiC IGBTs currently in use are p-type devices due to the issues involved in developing p-type substrates for SiC. The device structure is shown below.

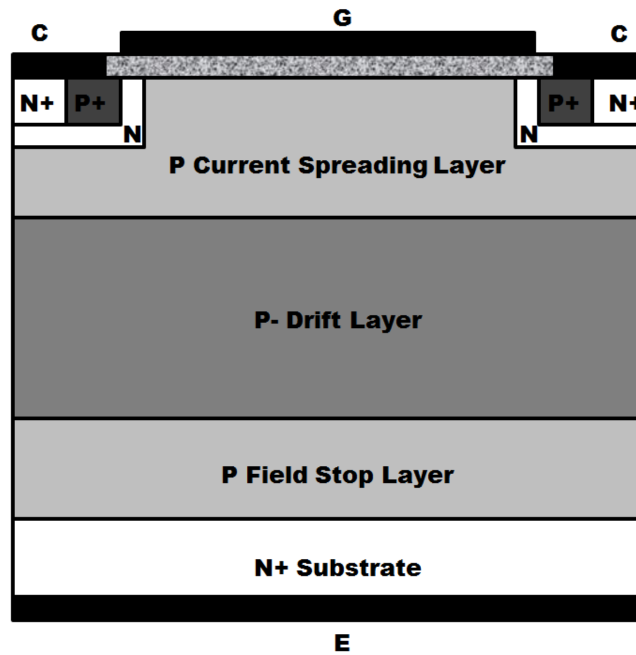


Fig. 7.3. SiC p-IGBT with collector/anode (C), emitter/cathode (E), and gate (G).

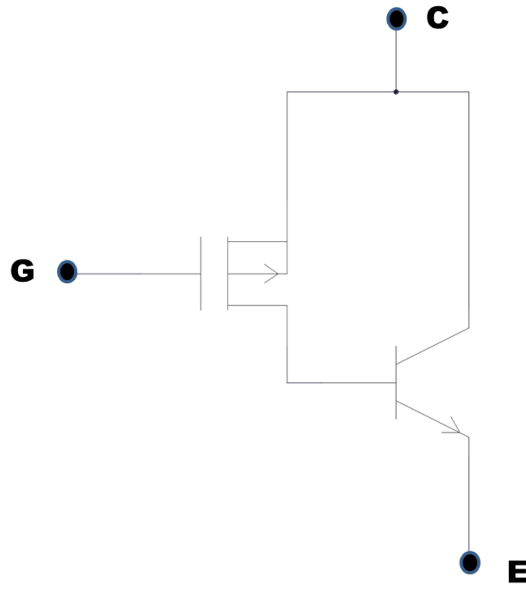


Fig. 7.4. Equivalent circuit of SiC p-IGBT.

There are several obvious advantages to investigating the usage of SiC IGBTs for SSFCLs. As seen by examining the equivalent circuit of the SiC IGBT, it is a voltage-controlled device, requiring the application and removal of a gate voltage (or the application of a negative gate voltage) for turn-on and turn-off, respectively. During fault conditions, turn-off of the device is less complicated than the case in which a SiC GTO would be used. It can be argued that one of the most challenging aspects of developing a SiC SSFCL using GTOs would be the development of a gate driver capable of providing the current that would be needed at turn-off. A less complex gate drive for SiC IGBTs would boost the reliability of the entire system, and make the usage of the device in this application more appealing to potential customers. IGBT devices also benefit from conductivity modulation during the on-state, making the conduction losses fairly low. A distinctive characteristic of IGBTs is the tail current that is present during device turn-off. After the gate voltage is removed, the channel of the MOSFET portion of the device disappears and the current drops rapidly, but recombination of the excess carriers in the drift

region must occur before the device can sustain its blocking voltage. This is a much slower process, and the reason for the tail current. The device turn-off time is still much shorter than that of a thyristor type device, which is why they are ideal for high power converter applications that require a relatively high switching frequency.

An issue with SiC IGBTs, as with all SiC bipolar devices, is paralleling capability. With current ratings that will likely be substantially less in comparison to a SiC GTO with similar voltage ratings, the need for operating multiple devices in parallel becomes necessary. The reports differ on the ease with which these devices parallel. Some have claimed to develop IGBTs with a slightly positive temperature coefficient (PTC), while others claim that a PTC is only possible at current densities of greater than 500 A/cm^2 [105–107]. Given the increased thickness of the drift layer at higher voltages, and the findings that the inversion in SiC materials does not occur until extremely high current densities, the latter claim is the more valid one. The on-state operation of these SiC IGBTs will be dominated by the carrier effects that occur within the drift region of the device, and it can be expected that as the blocking voltage and thickness of the drift region increase, the on-state characteristics of the IGBT will be dominated by the same nonlinear effects that cause a negative temperature coefficient in SiC diodes and thyristors.

The major advantage in using a voltage-controlled SiC IGBT in SSFCL applications is that gate control can be utilized in order to influence the output characteristics of the device. Thus, the fact that the devices may not share current can possibly be overcome through proper control techniques. Several gate control techniques have previously been studied for this purpose with silicon devices, and these methods can be used with SiC IGBTs as well. The main issue is that by using these techniques the system becomes more complex, which equates to less reliability for many potential customers. There will likely need to be individual gate drivers for each

device, and this could complicate power module development for SiC SSFCL applications. In [108] several techniques are outlined. In the end, the analysis is consistent with the approach that was taken for the design of the SiC SSFCL prototype, which declares that adding series balancing impedances may be the most reliable solution with the least amount of complexity.

Another drawback to using SiC IGBTs is the limited surge capabilities of the devices. Analysis of 15 kV SiC IGBTS showed that the short circuit capability of the devices was somewhere in the range of 20 μs, which is insufficient for FCL applications [109]. On the contrary, SiC SGTOs have been demonstrated for pulsed power applications, sustaining significant overcurrents for periods beyond 1 ms. Improvements in the short circuit capabilities of the SiC IGBT could be attained, but it requires a trade-off of larger on-state voltage drop in the device. Furthermore, IGBT devices exhibit a saturation current, meaning that they have an inherent current limiting characteristic for a given gate voltage. While this may seem advantageous for an application such as this, this may actually prove to be problematic for a device operating under fault conditions, and the rapid temperature rise that the device undergoes in this condition could lead to failure of the device.

Based on the present characteristics of the SiC GTO and the SiC IGBT, the SiC GTO will likely remain the best device for the application. The main disadvantages of its use are its inability to parallel based on its negative temperature coefficient of on-state resistance and the complexity of the gate drive circuit that would be required. However, the lower losses and higher device ratings in comparison to SiC IGBTs, as well as its superior operation under surge conditions, make it more suitable. In order to determine the advances that will be required in SiC GTO technology in order for this application to be successful, a 13.8 kV feeder and its fault conditions were evaluated.

7.3 Case Study of 15 kV Class SiC SSFCL

Since nearly 80% of all distribution systems are in the 15 kV class (i.e. 12.47 – 14.4 kV), an examination of this type of system is necessary. The example system consists of a 115-13.8 kV 20 MVA transformer, with equivalent impedance Z_{eq} of 0.62 + j8.91%, supplying a 13.8 kV radial distribution feeder with the conditions specified in Tables 7.1 and 7.2.

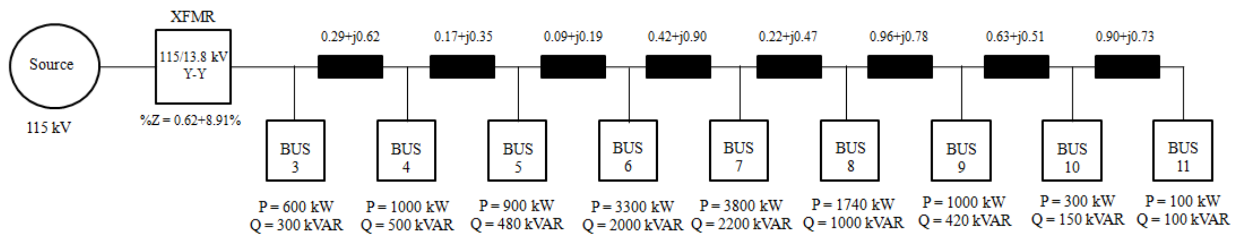


Fig. 7.5. One-line diagram of feeder system used for case study.

Table 7.1. Three-Phase Peak Loads for 13.8 kV Feeder.

Bus	P (kW)	Q (kVAR)
3	600	300
4	1000	500
5	900	480
6	3300	2000
7	3800	2200
8	1740	1000
9	1000	420
10	300	150
11	150	100

Table 7.2. Feeder Impedances.

Segment	Impedance (Ω)
Bus 3 to Bus 4	0.29 + j0.62
Bus 4 to Bus 5	0.17 + j0.35
Bus 5 to Bus 6	0.09 + j0.19
Bus 6 to Bus 7	0.42 + j0.90
Bus 7 to Bus 8	0.22 + j0.47
Bus 8 to Bus 9	0.96 + j0.78
Bus 9 to Bus 10	0.63 + j0.51
Bus 10 to Bus 11	0.90 + j0.73

The maximum fault current occurs when there is a fault at Bus 3, with the equivalent impedance of the transformer as the only impedance between the transformer secondary and the point of the fault. Based on the transformer impedance, the maximum available fault current at the transformer secondary is 9369 A_{RMS}, equating to a peak value of 13250 A. For analysis of SiC SSFCLs the worst case fault condition will be analyzed.

A SiC SSFCL in the 15 kV class will be subject to the same specifications as other equipment present in the distribution systems, such as circuit breakers and transformers. IEEE Std. C37.06-2009 outlines that such equipment must have a power frequency voltage withstand rating of 36 kV, with a basic impulse rating (BIL) of 95 kV. In systems with a specified maximum operating voltage of 15.5 kV, these ratings rise to 50 kV and 110 kV, respectively [100]. This poses an intriguing design challenge in the development of SiC SSFCLs for such systems. Lightning induced transients are typically mitigated by using surge arresters and varistors. The margin of protection, calculated as the difference between the maximum operating voltage and the BIL rating, is used as the basis of the selection of a suitable surge arrester scheme. Typically, varistors are employed across the terminals of the SSFCL in order to

protect the power semiconductor devices from catastrophic failure. This varistor is intended to provide an alternate current path in the event of high energy transients, and is chosen such that the breakdown voltage ratings of the devices are not exceeded. For power distribution system equipment such as transformers and circuit breakers, varistors and surge arresters are connected between line-to-ground or line-to-line in order to provide adequate insulation protection and satisfy BIL requirements. In fact, the maximum continuous operating voltage (MCOV) for an arrester chosen to protect a system with a maximum possible line-to line voltage of 15 kV is typically on the order of 12.7 kV, as line-to-ground installation of the arrester is expected. Thus, a combination of these varistor protection schemes will likely be needed for SiC SSFCLs in order to maximize the protection against transients, in order to insure that the devices are protected while also meeting all BIL requirements. For solid-state protection circuits, the minimum blocking voltage of the system should be equal to the power frequency withstand voltage. It is cost prohibitive to design a solid-state system using SiC power semiconductors to satisfy the BIL requirements, and this would also introduce more conduction losses into the system due to the number of additional devices that need to be connected in series. The power frequency withstand voltage rating of 36 kV_{RMS} will dictate that SiC devices with high blocking voltages be developed for SSFCL applications. It becomes evident that substantial increases in SiC device ratings are needed for 15 kV class SiC SSFCLs.

Ultimately, at least 20 kV devices will be needed for such systems. Likewise, the standard current rating for circuit breakers in the 15 kV class is typically 1200 A, and it follows that a similar rating for the SiC SSFCL system would be needed. Since best case device estimates place the device ratings in the range of 900 A for 20 kV devices, paralleling will remain necessary. SiC GTO devices with a nominal current rating of 900 A would effectively require an

increase in device area of more than three times than what is presently available. This would require devices with an active area of 3 cm × 3 cm based on a current density of 100 A/cm^2. The die would likely have to be larger given the power density limitations imposed by the power packaging. Die sizes of this magnitude would require significant advances in SiC processing technologies and material quality.

One of the most important characteristics for the SiC SSFCL system is the ability to repeatedly and reliably interrupt fault currents. For the system under investigation, the worst case fault condition (at Bus 3) is analyzed in order to determine the required pulse current capability for SiC GTO devices needed. For a sinusoidal fault current, the pulse current energy, I^2t, for a half cycle is found according to the following equation.

$$I^2t = \frac{I_{peak}^2 \times t}{2} \tag{7.1}$$

In this equation, *t* is equal to the period of the half cycle, which is 8.33 ms based on a 60 Hz signal. For a maximum available fault current of 9369 A_{RMS} for the example system, this equates to the following:

$$I^2t = \frac{(9369\,A \times \sqrt{2})^2 \times (\frac{1}{120}\,s)}{2} = 738484.68\,A^2s \tag{7.2}$$

Though quarter cycle interruption is a requirement of the SiC SSFCL system, the worst scenario is that the device would have to endure a full half cycle of fault current in the case of a gate driver malfunction. A number of factors must be taken into consideration when evaluating the potential for SiC GTOs in this system. The pulse current rating of a SiC GTO device is largely a function of the active device area. The maximum peak current capability for previously developed devices in the 6 kV to 9 kV range has been stated to be linearly proportional to the

device area. The peak current pulse capability for 1 cm × 1 cm devices is approximately 3.5 kA, with a measured I^2t capability (action rate) of 6000 A^2s for these devices [110]. For the larger area devices previously mentioned (nine times the area of present devices), a peak current capability of 31.5 kA is assumed based on a linear progression of capability of the device. This equates to an action rate of 496125 A^2s. For parallel devices, the total I^2t value is calculated as:

$$Total\ I^2t = I^2t \times N^2 \tag{7.3}$$

In this equation, N is the total number of devices in the parallel configuration. Based on the previously determined I^2t value calculated for a quarter cycle of fault current, the number of devices that presumably would be needed for this distribution system is:

$$N = \sqrt{\frac{I^2t\ (System)}{I^2t\ (Device)}} = \sqrt{\frac{738484.68\ A^2s}{496125\ A^2s}} = 1.22 \tag{7.4}$$

So, under these best case conditions, which assumes a 900 A device will be available, the two paralleled SiC GTO devices needed for steady-state operation will handle the system fault current. Based on the action rate of current devices with an area of 1 cm × 1 cm, and using Eq. (7.4), at least eleven devices would be needed to handle the fault current. This illustrates that major advances in the current handling capabilities of SiC devices are needed to avoid complex power module and gate drive requirements for SiC SSFCLs. Based on the previous determinations for the system ratings, twelve 900 A SiC devices will be needed in order to comprise an adequate 36 kV (50.9 kV_{PEAK}) switching leg for the example 13.8 kV feeder systems. This assumes a switching position that is composed of three SiC GTOs and three SiC diodes to attain the desired blocking voltage, and two branches of these devices to handle the

maximum fault current. An identical set of devices is needed for current flow in the opposite direction, which equates to 24 devices per phase, and 72 total devices for a three phase system. As SiC fabrication processes mature and material quality improves, unique fabrication techniques will have be adapted in order to make the development of such devices for SiC SSFCL systems less daunting.

Another important factor that must be investigated for determining SiC SSFCL use in 15 kV class systems is the on-state voltage drop and conduction loss of the system. Furthermore, since the system operates at 60 Hz with no high frequency switching under normal operating conditions, an estimate of system losses is beneficial in determining the appeal to utilities. In order to examine these characteristics, an estimate of the on-state resistance of the 20 kV SiC power devices is obtained.

The resistance was determined by performing an evaluation of current SiC high power devices. The resistance of a power semiconductor device is influenced by a number of phenomena during on-state operation (i.e. conductivity modulation). The device on-state resistance is a function of the doping of the drift layer and the drift layer thickness:

$$R_{on,sp} = \frac{W_{drift}}{q\mu N_D} \tag{7.5}$$

In this equation, W_{drift} is the thickness of the drift region and N_D is the doping concentration within the region. For the current generation of SiC power devices, the drift layer doping concentration is typically 2×10^{14} dopants/cm^3. The following table shows the doping levels of the drift region of previous silicon carbide power devices, as well as the width of the regions.

Table 7.3. Drift Region Thickness of SiC Power Devices [23], [111], [112].

Device Blocking Voltage (kV)	Drift Region Width (μm)	Doping Concentration (cm^{-3})
1.77	30	5×10^{14}
5	70	2×10^{14}
8	90	2×10^{14}
12	90	2×10^{14}
15	140	2×10^{14}

Based on the above data, the blocking voltage of the device for a given doping concentration is a linear function of the drift region thickness. An extrapolation of the data to 20 kV design for a doping concentration of 2×10^{14} dopants/cm^3 was performed, and the thickness required for a 20 kV device was found to be 225 μm. More liberal estimates by silicon carbide manufacturers place the required drift region thickness at 175 μm, but the upper bound is used in this analysis. When normalized to the on-state characteristics obtained for the packaged 8 kV SiC devices with a 90 μm drift layer thickness, the on-state resistance is approximated as 11.6 mΩ for a 20 kV 900 A SiC device, since the on-state resistance is also proportional to device area. For current balancing, a 20 mΩ is added in series with each device. The properties of the SiC GTO and SiC PiN diode are considered analogous for on-state operation, and as such the same values were used in approximating the diode. Based on a total blocking voltage required to reach the 36 kV_{RMS} system rating, the total resistance of the series branch used for analysis in simulations is 189.6 mΩ, and 94.8 mΩ for the entire switching position.

Simulations were conducted for the example 13.8 kV feeder system using Saber. The system is modeled from the secondary of the 115:13.8 kV transformer. Results yielded a system current of 715 A under peak load conditions. The same SiC GTO and SiC diode models from

simulations in Chapter 3 were used, with the parameters updated to reflect the characteristics of 20 kV devices. Each SiC SSFCL block as shown in Fig. 7.6 contains the equivalent representation of 24 20 kV SiC devices (12 SiC SGTOs and 12 SiC diodes). Two branches in parallel are each composed of six (three SiC SGTOs and three SiC diodes) serially connected 20 kV devices for bidirectional blocking capability. Another identical branch is used for conducting current of the opposite polarity.

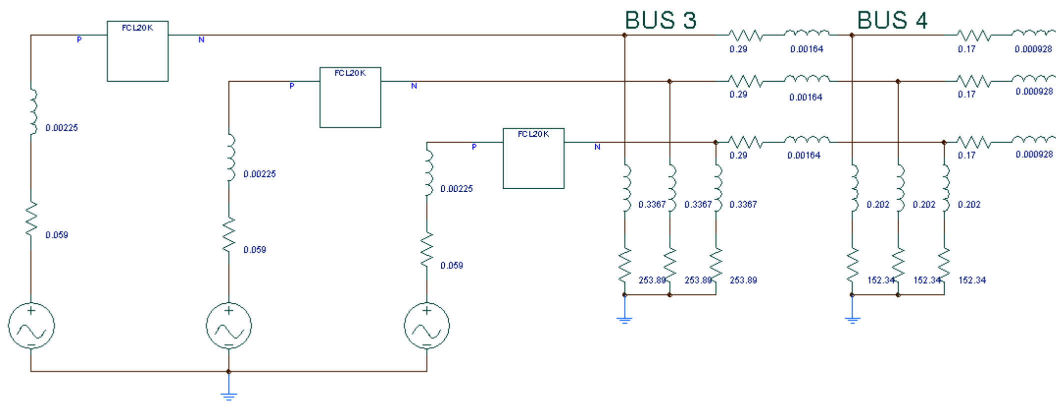


Fig. 7.6. Partial schematic of 13.8 kV in Saber as used for simulations, with SiC SSFCLs shown. Buses 5-11 omitted for clarity, but modeled in simulation using values from Tables 7.1 and 7.2.

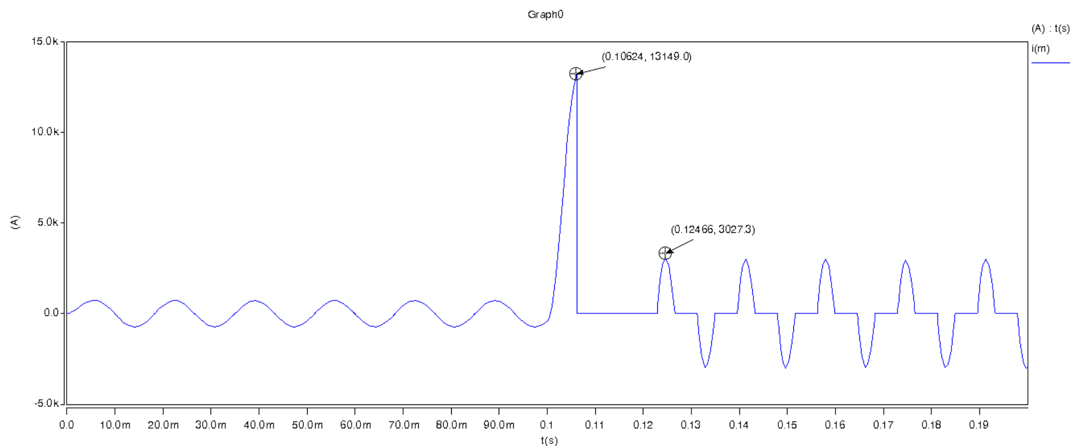


Fig. 7.7. Current interruption and current limiting for 13.8 kV feeder for single phase fault. Current interruption is performed for worse case condition for a fault current approaching 13250 A.

For this system, the current was interrupted at a value that is fairly close to the maximum available fault current of the system, which is 13250 A_{PEAK}. Current limiting is performed via phase angle control in order to limit the fault current to a value of approximately 3000 A. This current reaches a peak magnitude of 3027 A in the simulation.

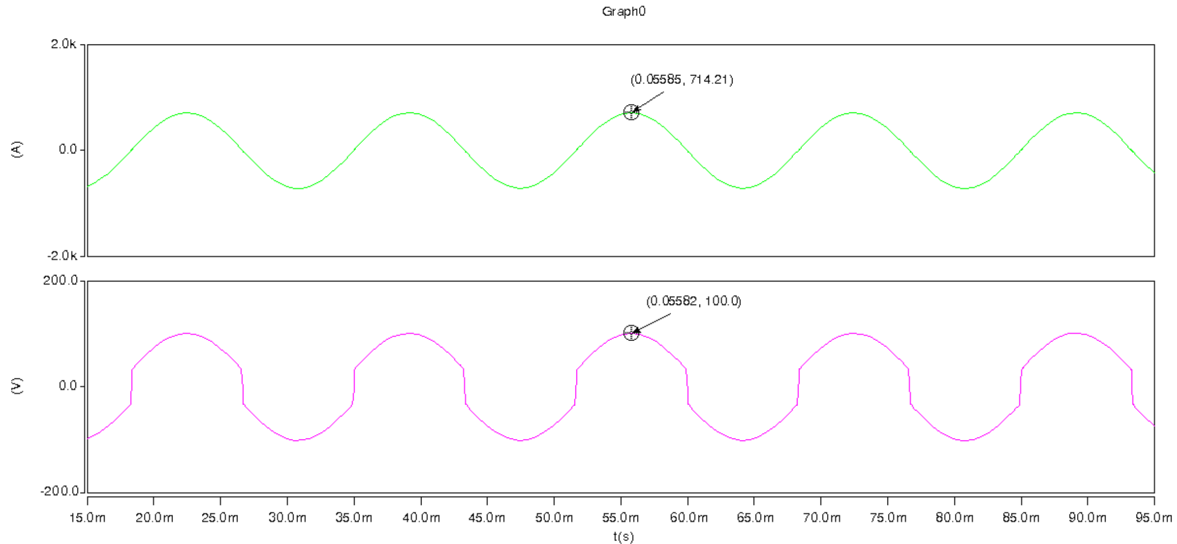


Fig. 7.8. Voltage (top) and system current (bottom) for SiC SSFCL under peak load conditions.

The voltage drop across the system under these peak load conditions is 100.0 V. This is 0.5% of the total system voltage. The conduction losses of the SiC devices in the SSFCL on Phase A are 29.8 kW, based on the simple formula:

$$P_{on} = V_{on} I_o \tag{7.6}$$

The total losses in the series resistors equate to 30.6 kW. The losses of the resistors, as expected, more double the electrical and thermal losses of the entire system, and can complicate the thermal management requirements of the SiC system and the appeal to potential customers in the event that SiC devices are not able to share current. Table 7.4 shows the important parameters as determined for the SiC SSFCL for the 13.8 kV feeder system.

Table 7.4. Parameters of 13.8 kV SiC SSFCL for Example Feeder.

Number of Devices (Per Phase)	24
Voltage Drop	100 V (0.5%)
Conduction Losses	29.8 kW
Resistor Losses	30.6 kW
Gate Drive Turn-Off Current	9725 A

As a basis for comparison, the losses of the SiC SSFCL are compared with those of a conventional circuit breaker and a SSFCL with silicon devices. Based on specifications provided by circuit breaker manufacturers, the losses of circuit breakers are between 50 and 200 W for the peak current of this system [113]. This is a value that varies depending on the circuit breaker type. The circuit breaker power loss is several orders of magnitude lower than the losses calculated for the 13.8 kV SiC SSFCL system. Solid-state protection systems are expected to have sufficiently higher losses than circuit breakers, and the additional losses are a contingency of the system for enhanced fault mitigation. For an equivalent system constructed using silicon IGCTs, the total conduction losses would be approximately 25 kW, based on a specified maximum on-state voltage drop of 2.7 V. Thus, the calculated conduction losses for the SiC system are not much higher than those for a silicon based system. The I^2R losses of the series resistors required for the SiC SSFCL present the most problems.

There has to be a practical expectation for the losses expected from a SSFCL. Considering a 13.8 kV distribution system, the system design conditions (36 kV_{RMS}) will lead to losses in the range of tens of kilowatts per phase for these systems. In comparison to conventional circuit breaker systems, and the superconducting fault current limiters that will be employed at the transmission level, these losses seem excessive. However, the voltage drop across the entire system will remain fairly low in comparison to the system voltage. Results from the previous

section revealed a voltage drop that is less than 1% of the system voltage. For solid-state systems operating in excess of 600 A, the conduction losses are not far beyond what is expected. Still, this does not mean that measures should not be taken in order to lower the losses of the SiC SSFCL.

There are several factors to be considered when evaluating the SiC SSFCL for the 13.8 kV feeder. The on-resistance is liable to be much lower for a 20 kV, 900 A device than was calculated. For this analysis, the on-state resistance is normalized to that of a 8 kV, 8 mm × 8 mm device. However, the on-resistance of the bare die, as shown in Table 4.1, is 12 mΩ. This is much lower than the on-resistance associated with the packaged device used for calculation, which is approximately 40 mΩ. Optimization of the SiC module design can reduce parasitic resistance and drastically decrease the losses that are present in the system.

7.4 System Overvoltage

From a system perspective, the biggest challenge in implementing the voltage-controlled SiC SSFCL at the 15 kV level is the overvoltage that is present at the interruption of the fault current. Even though such systems will be designed for a power frequency withstand voltage of 36 kV at a minimum, the overvoltage will likely exceed this period for a short duration. As mentioned earlier, surge arresters will be placed at the terminals of the SiC SSFCL (line-to-ground) in order to provide protection against lightning transients. Snubber circuit design was implemented as part of the overvoltage mitigation, but this could potentially cause problems with voltage distortion. Furthermore, the calculated snubber may not provide adequate overvoltage protection in the absence of a suitable surge arrester or varistor scheme.

For the analysis, a single phase fault on Phase A was initiated using the SiC SSFCL to perform interruption. Fig. 7.7 shows that for the example distribution system, the voltage peak is roughly 75 kV with calculated snubber values of 50 μF and 5 Ω.

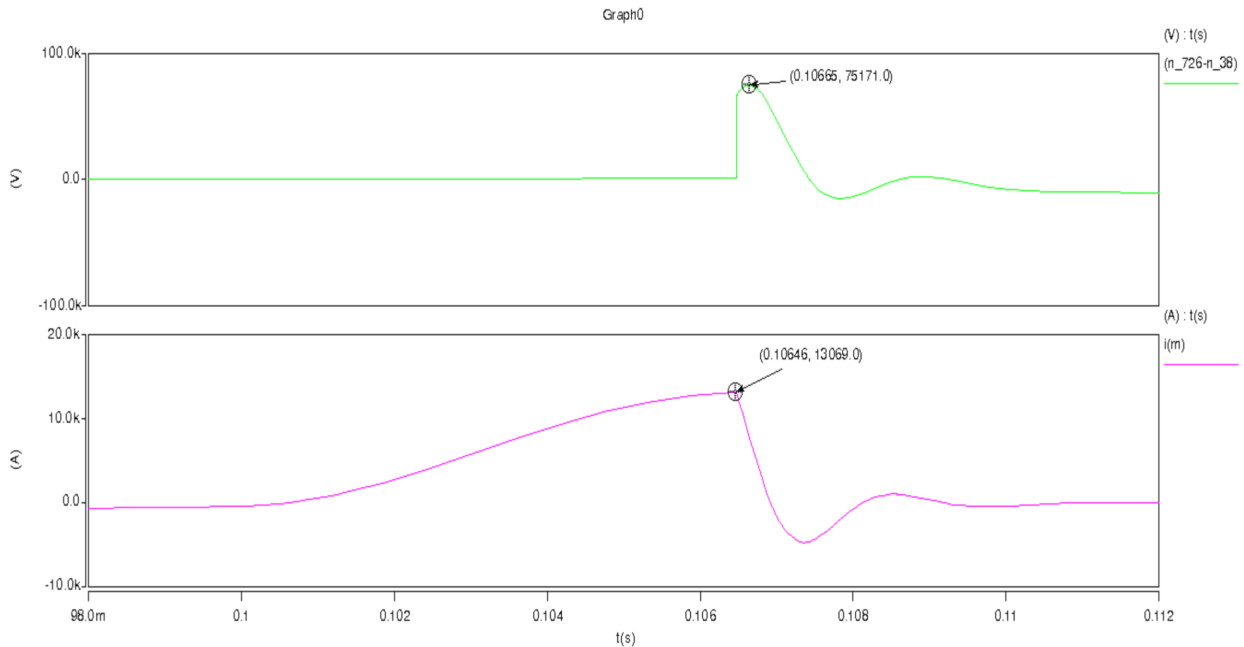


Fig. 7.10. System overvoltage at fault interruption for feeder system.

The overvoltage at device turn-off exceeds the ratings of the system for a period of 410 μs. Surge arrester and varistor protection schemes are typically employed in order to mitigate these transient overvoltages to an acceptable level for distribution systems applications. Likewise, the BIL rating, used for lightning induced impulses, is typically achieved for solid-state systems using adequate protection schemes in which the margin of protection of the system is achieved using adequate surge arrester protection. However, the BIL rating of a system is tested using a 1.2/50 μs waveform, meaning that the ramp time to the peak voltage is 1.2 μs, and then the voltage decays to 50% of the peak value in 50 μs. It is conceivable that the protection scheme is inadequate for an overvoltage of duration of 410 μs. There are four practical solutions to the

overvoltage problem that would adequately ensure reliable device operation in the presence of overvoltage:

1. Increase the voltage rating of the SiC SSFCL system.
2. Allow the first peak of the fault current to flow impeded, allowing for natural commutation of the main SiC power semiconductor devices and hence, zero-current turn-off.
3. Interrupt the current at a sufficiently low value such that the *di/dt* is reduced at device turn-off, resulting in a reduced overvoltage.
4. Selection of a different SiC SSFCL topology.

In the absence of suitable protection schemes for the SiC based voltage-controlled SSFCL, each of these alternatives can be considered. An examination of each of these options is presented.

For 13.8 kV systems, the BIL is 95 kV. An increase of the number of devices to reach this voltage level would adequately protect the system against overvoltages and lightning induced transients. The downside to this approach is that it would require an increase in the number of 20 kV devices needed for system design to 156 based on the aforementioned current characteristic assumption of 900 A. This would undoubtedly increase system cost and steady-state conduction losses, but would eliminate issues associated with the use of a snubber circuit as well as reduce the margin of protection required of the surge arresters and varistors in the system.

The second option would eliminate hard switching of the fault current during the first current peak and eliminate overvoltage associated with the high *di/dt* of the system under these conditions. The issue with this approach is that fault current limiter requirements currently

dictate that limitation occurs within a quarter-cycle of the fundamental frequency, and this method would violate that principle.

The third option is the most feasible from a cost perspective. Analysis of the example 13.8 kV system was performed for worst-case conditions, with fault current interruption occurring at or near the peak of the maximum available fault current of the system. For instance, if the current threshold is chosen to be 2 – 5 times the magnitude of the nominal system current, the overvoltage and required pulse ratings of the devices are both drastically decreased. For the distribution system under investigation, the third technique is implemented and it is shown that the overvoltage is limited to 18.5 kV for current interruption performed at a value of 3568 A, which is approximately 5 times the current supplied to the feeder at the SiC SSFCL terminals under peak load conditions.

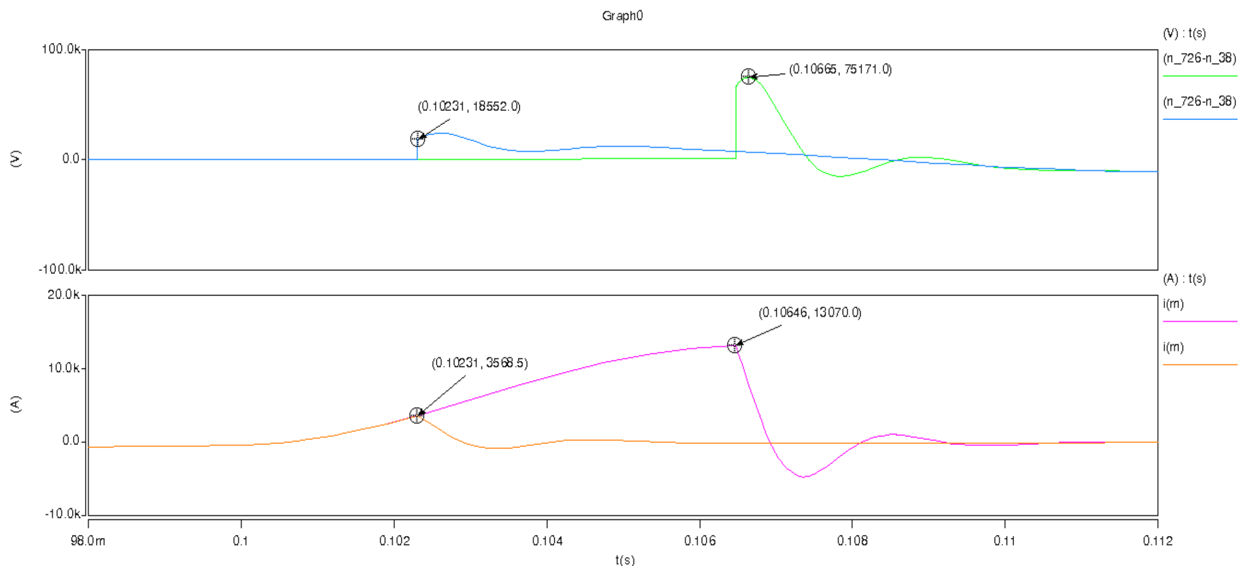


Fig. 7.11. System current and voltage across the SiC SSFCL at peak fault interruption and for interruption at a reduced value.

The last option for eliminating overvoltage is the consideration of alternate topologies for the SiC SSFCL system. The voltage-controlled topology has a number of inherent advantages, such as flexibility of control and the ability to limit the maximum fault current to anywhere in the

range of 0-100% of the maximum potential value. Choosing an impedance-type SiC SSFCL could reduce the required current ratings of the devices, as well as the electrical stress endured by these devices, as current is diverted into an impedance branch to perform current limiting. This would reduce the *di/dt* of the current as well, leading to reduced overvoltage. The downside is the size of this type of system, as mentioned before, and the lack of interruption capability.

7.5 SiC Power Semiconductor Device Research for SSFCL Applications

From the SiC SSFCL research that has been conducted throughout this chapter, as well as the prototype development challenges, it is apparent that there is currently not a SiC power semiconductor device that is ideal for this application. Table 7.4 indicates high conduction losses and gate turn-off current requirements. These are potential areas for concern in the development of SiC SSFCLs. The two best available candidates for this application, the SiC SGTO and the SiC IGBT, each have shortcomings that were discussed previously and are impossible to overlook. Other SiC power semiconductor devices, such as the MOSFET and JFET, simply do not have the ratings necessary to make them feasible for use. The SSFCL is a unique application in that it has to endure high voltages and currents during normal operation, while being subjected to unusually high transients during fault conditions.

As the move is made towards smart-grid capable technologies and FACTS (Flexible AC Transmission Systems) devices are more readily utilized, there will need to be an emphasis on developing SiC power semiconductor devices for these applications. The SSFCL is an application for which power semiconductor device research and development should be a priority, especially since these devices will play a major rule in fault current mitigation for the future grid. Currently the performance of these systems is limited by the devices available. Many of the drawbacks of the SiC SSFCL can be attributed directly to the available SiC power

semiconductor devices. However, by having the requirements of the application dictate the device specifications, SiC SSFCL system performance can progress in a direction that more closely resembles the ideal FCL, the characteristics of which are listed in Chapter 1. Thus, an examination of the device characteristics that would be necessary for this application will be presented.

Obviously, the ideal power semiconductor device for the SiC SSFCL application should have sufficient voltage blocking capability and current ratings. While SiC devices will have higher voltage ratings than their silicon counterparts, there is still a need for further improvement. The projected roadmaps for these devices put the device ratings in the 20 – 40 kV range, but based on the system specifications for SSFCL systems (i.e. power frequency withstand voltage, basic impulse level) this could still require a substantial amount of devices to be connected in series. This increases the number of devices needed while also requiring more complex subsystems for the SSFCL configuration, such as gate drivers and overvoltage protection. An issue is that SiC power semiconductor devices typically have asymmetrical voltage blocking capability, as well as unidirectional current conduction. Each of these factors results in a larger device count for a fully functional SSFCL system. A device with bidirectional voltage and/or current capabilities would greatly simplify the system design.

The paralleling capability of the SiC SGTO and SiC IGBT is hindered by their negative temperature coefficient. Either one of two factors is needed from power semiconductor devices for SSFCL use: sufficient current ratings such that is paralleling is not necessary, or device operation that allows for a positive temperature coefficient within the drift region. This would eliminate the need for current balancing resistors, which introduce substantial losses to the system during normal operation as indicated in Table 7.4.

Current controlled devices such as the SiC SGTO or thyristor that are typically used in SSFCL applications are turned off via the gate or through the use of forced commutation circuitry. In either circumstance, there is an added complexity to the overall system design. A significant amount of current is required for device turn-off in the event of a fault current. A voltage controlled device would be best suited for the SSFCL since gate driver design would be less complicated and device turn-off could be achieved much more reliably.

There are several other critical characteristics of an ideal power semiconductor device for the SSFCL application. Low on-state losses are essential, so a bipolar type device that benefits from conductivity modulation is desired. The surge capabilities need to be extensive as well. The device should have sufficient short circuit capabilities, and should also be robust enough to deal with multiple fault current events. The absence of a gate oxide within the SiC power semiconductor device would be ideal, as this typically leads to stability issues at higher voltages and temperatures. Since the SSFCL operates at a fundamental frequency of 60 Hz and under most conditions turns off under natural commutation, the device need not have high frequency capability. A list of the desired characteristics for a SiC device for SSFCL use is shown in Table 7.5.

Table 7.5. List of Characteristics for Ideal SiC SSFCL Power Semiconductor.

Characteristic	Benefit
High voltage and current ratings	Less devices in SiC SSFCL switching position
Voltage-controlled gate	Gate driver simplicity and device turn-off ease
Symmetrical voltage blocking capability	Reduction of number of devices by a factor of at least 2
Bidirectional current conduction capability	Reduction of number of devices by a factor of at least 2
Low conduction losses	Lower power losses and better thermal stability
Positive temperature coefficient of on-state resistance	Elimination of series resistors due to natural paralleling capability
High surge current capability	Ability to adequately withstand fault currents

SiC device research has to be oriented such that many of these factors can be attained with a single SiC power semiconductor device. The SiC SGTO is currently predicted to be the best device for this application in the future based on current specifications and the device roadmaps, but this is largely in part to the low on-state losses in combination with the expected high voltage and current ratings. The structure of thyristor type devices lend themselves nicely to an application such as the SSFCL, due to its simplicity and ruggedness. However, these factors alone will not be adequate in causing a potential customer to overlook the other challenges. There is not a device that currently approaches having many of the characteristics shown in Table 7.5; however, advanced research into the area could help resolve this issue. Novel thyristor devices, such as the MOS-controlled thyristor, or the emitter turn-off (ETO) thyristor, could potentially alleviate the gate control issues while maintaining the benefits of the thyristor. The problem is that device structure of each is complex and will likely not bode well for high power applications. Practical expectations for power semiconductor device research for the SiC SSFCL should focus on making adequate improvements to the SiC IGBT in order to resolve many of the issues as presented in Section 7.2.2. As a voltage controlled bipolar device, it benefits from ease of control and relatively low on-state losses. However, progress has to be made into producing IGBTs with significant voltage and current ratings. Reverse blocking IGBTs have been developed in silicon, and SiC IGBTs with reverse blocking capabilities would be beneficial for this application. There are two types of IGBT devices: punch-through (PT) and non-punch-through (NPT). Most development of SiC IGBTs has focused on PT devices, which have a highly doped buffer layer that drastically decreases on-state losses and switching times. While maintaining low conduction losses is necessary, the switching times are of little importance as long as quarter cycle interruption is maintained. NPT-IGBTs have near

symmetrical reverse blocking capabilities, higher short circuit capabilities, and better paralleling capabilities in comparison to PT-IGBTs. Thus, many of the desired characteristics of a SiC power semiconductor device for an SSFCL can potentially be realized through the use a NPT-IGBT. Even if the development of NPT-IGBTs with sufficient performance parameters is realized, there must be an effort to further reduce the on-state losses. Gate oxide stability and the magnitude and duration of the device tail current at turn-off need to be improved for this device if it is to be used in this application, and continuing device research is needed in order to develop SiC bipolar devices of all types for the solid-state fault current limiter.

7.6 Key Points of Analysis

The presented analysis is intended as a basis on which to evaluate the feasibility of SiC SSFCL systems. A number of aspects must be considered. The example feeder system has a maximum fault current rating of approximately 9369 A_{RMS} and the fault currents of modern power distribution systems are continuously increasing due to the proliferation of distributed generation. The devices chosen for the analysis are based on the ideal expectations; in actuality, the current ratings of 20 kV SiC devices that become available could only be a small percentage of the desired rating of 900 A. Calculations of the pulse ratings and the on-state resistance were based on present SiC device trends and processing procedures, which are steadily evolving and expected to continue to do so over the course of the next decade. Yet, with all factors considered, it is evident that SiC SSFCL system design for 15 kV class distribution systems can pose a challenge. Steps must be taken towards developing high power, efficient SiC power devices and modules specifically for SSFCL applications, the characteristics of which were indicated in the previous section. Furthermore, in the case of current SiC power devices available for SSFCL use, gate drive challenges will have to be overcome, as each GTO in the

example system would require a high gate current for turn-off. However, potential customers will be looking for ways to increase stability on power distribution networks, so the potential drawbacks of such a system may prove to be surmountable. By preventing catastrophic failures of other power distribution equipment and reducing service interruptions, the SiC SSFCL will likely prove to be a worthwhile investment.

7.7 Potential for SiC SSFCL Use in Microgrid Applications

As indicated earlier, there is a lot of flexibility in using the voltage-controlled SiC SSFCL. Thus, there has to be consideration for using this circuit in other applications besides radial distribution systems. Fault current limiters for these systems are expected to adhere as closely as possible to the list of desired characteristics as presented in Chapter 1. For the SiC SSFCL in 15 kV – 35 kV systems, the losses and paralleling capability of the devices have to be addressed. Time will be required in order to resolve these issues. Thus, an investigation into alternate applications that are in immediate need for such a power electronic based circuit was conducted. There is use for these systems beyond conventional fault current limiting. One such application is deployment in microgrid systems. Microgrids are decentralized, localized systems which utilize distributed generation such as renewable energy sources, as well as various forms of energy storage, in order to provide highly reliable power to critical loads [114], [115]. As the grid is restructured and renewable energy technologies become more prevalent as part of the GRID 2030 plan, microgrids will become more commonplace. Due to the nature of the loads on the microgrid system, the emphasis is on providing continuous service with little or no power quality disturbances. The SiC SSFCL can be utilized in order to control fault currents within microgrids in order to preserve the integrity of delivered power. Microgrids often have two modes of operation: grid-connected mode and islanded mode. The grid is source of power

during normal operating conditions, and during the event of a fault or other power quality problem (i.e. voltage sag) the microgrid is operated in islanded mode, during which the renewables become the sole source of power in order to provide enhanced protection to the critical loads.

The transition between these two modes is facilitated by a static switch, and this is another area in which the SiC SSFCL could be of use. The static switch element has to quickly transition between the modes of operation, and also has to have the capability to detect power quality disturbances. Static switch specifications are similar to those of fault current limiters in that sub-cycle disconnection is necessary when a fault or voltage sag occurs. Since there is inherent overlap between the functionality of the static switch and SiC SSFCL, this system could be useful in the microgrid. With its interruption capability, disconnecting the grid form the microgrid within a cycle is not a problem. Furthermore, since the static switch specifications do not dictate interruption before the peak current, the control of the SiC SSFCL in this instance could be configured such that zero current turn-off is achieved, eliminating the need for extensive overvoltage protection that is necessary for SiC in radial distribution feeders.

A significant advantage is that microgrids are typically employed at voltages close to utilization levels (i.e. 240 V) and as such, the issues of conduction losses become fairly non-existent. Such system could even utilize SiC MOSFETs, more mature technologies with better established costs. The ratings of SiC devices, along with the fast reaction times, make the SiC SSFCL system ideal for use. Furthermore, the SiC SSFCL can provide functionality beyond what is typically offered from a static switch. The current from the grid to the microgrid can be limited in the event of a fault using the SiC SSFCL as well, whereas the static switch only provides disconnection capability. As the shift is made towards more decentralized power

generation, there will be a need for FCL systems at a local level, and SSFCLs, and specifically SiC SSFCLs, can be adequately utilized in these applications without encountering many of the potential issues that may be present at the 15 kV distribution level.

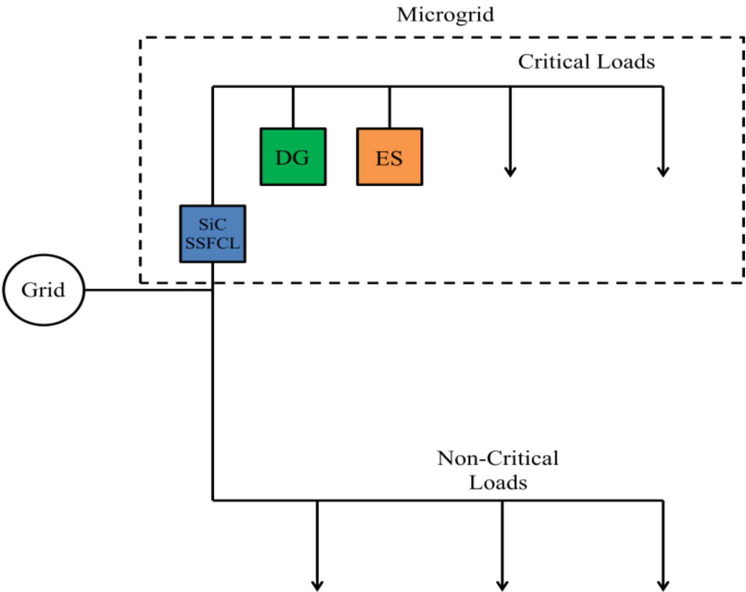


Fig. 7.12. Microgrid configuration included a SiC SSFCL with distributed generation (DG) and energy storage (ES).

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

The silicon carbide based solid-state fault current limiter shows a great deal of potential for use in power distribution systems. Mature silicon carbide power semiconductor devices, when used in this application, can increase the reliability of the system, while lowering the overall system losses and footprint when compared to using silicon power semiconductor devices. Furthermore, silicon carbide devices are better suited to withstand the increasing fault currents that are present in distribution networks. In investigating silicon carbide devices and designing a technology demonstrator, several challenges were also uncovered. Namely, the devices have a negative temperature coefficient of on-state resistance, and the gate current required for turn-off must be a large percentage of the system current which complicates the design of gate drivers for SiC SSFCLs to be used in distribution systems. The ratings for SiC devices are increasing, but substantial increases must be realized before SiC SSFCLs can be deployed in the most common class of distribution systems, which is the 15 kV class. Trends suggest that paralleling may remain an issue with future SiC GTO devices, and as such, suitable solutions must be found. The use of series resistors to balance the current may prove to be a deterrent for potential utility customers due to the additional losses in the system. The current costs of developing a SiC SSFCL are prohibitive, and unless significant advances in silicon carbide processing techniques are developed, these could remain a major roadblock to the commercialization of these systems.

Ultimately, the advances in silicon carbide over the next decade will determine whether these systems will find use in modern power distribution systems. As such, the design of such systems and the associated challenges were explored in great detail in this dissertation, both for 4.16 kV

and 13.8 kV systems. Several of these challenges were identified as potential roadblocks, and in response the characteristics needed for suitable SiC power semiconductor devices were identified. The construction of an ideal SiC SSFCL device begins at the device level, and research has to be conducted with a goal of building SiC power semiconductors that are specifically suited for use in the SiC SSFCL and other grid applications using this list of characteristics as a roadmap. The use of SiC SSFCLs for microgrids was also examined, since systems utilizing decentralized generations will become more common in the immediate future.

8.2 Recommendations for Future Work

There is still much more experimental testing to be done in the evaluation of silicon carbide solid-state fault current limiters. Testing at higher voltage and current ratings is needed. Such testing will allow for proper qualification of such systems for full-time operation in power distribution systems. Currently, IEEE Working Group P.37.02 is working on requirements for fault current limiter testing. Once the list of requirements has been completed, the silicon carbide solid-state fault current limiter prototype should be tested in accordance with these guidelines.

Improvement of some auxiliary system components could also prove useful. Presently, the snubber circuit is needed in order reduce the overvoltage and *dv/dt* across the SiC power semiconductor devices at turn-off. These snubbers are necessary, but not frequently utilized due to the nature of SiC SSFCL operation. Simulations have shown that the inclusion of the snubber circuit may actually produce more drawbacks than benefits for inclusion for SiC SSFCLs. Also, investigations can be made into reducing the size of the gate driver circuitry for SiC SGTOs while still providing suitable current for turn-off conditions.

One of the most obvious steps that must be taken in order for the SiC SSFCL to become a viable commercial reality is the development of a three-phase prototype. At the present time, there are a number of factors preventing such a development, namely the availability of suitable SiC power devices. Another concern is that three-phase prototype development becomes complicated because one must develop three-phase control for the system. For the prototype developed for this work, a topology was chosen that allowed for the smallest possible system footprint when used in conjunction with a silicon carbide based system. If the voltage-controlled topology is to be maintained, then the development of a three phase prototype becomes even more challenging. Phase angle control in a three phase system presents a number of unique challenges, but is beneficial in that it eliminates the bulky bypass impedance and allows for zero current turn-off during current limiting. Fault current behavior is dependent on the type of fault, the location of the fault, and also on the moment at which the fault occurs. Thus, there are a number of different possibilities to be considered when developing the control. Knowledge of the fault type and location would typically be needed in order to perform adequate phase angle control. Developing an algorithm that can determine fault type and location within a quarter of a cycle is quite an undertaking itself. After this is determined, the phase relationship between the system voltage and system current must be known. Under unbalanced system conditions, this is difficult. Further complicating matters is the fact that the phase relationships will be altered *during* phase angle control, and that conceivably, phase angle control could be occurring on only one phase, or on as many as all three.

Adequate fault detection and prediction methods should be incorporated into the SiC SSFCL controller. This will eliminate erroneous operation of the SiC SSFCL due to transient events. Many of these fast fault detection methods have already been thoroughly researched and

implemented. Furthermore, fault prediction methods could also reduce the potential for incorrect operation, but could prove useful in developing accurate phase angle control methods during three phase fault conditions. For example, Kalman filtering based techniques, which have been useful in other power systems applications for both fault detection and variable estimation, could prove useful in SSFCLs.

Lastly, 35 kV SiC SSFCL feasibility should be investigated. The 15 kV distribution class remains the most common, but evidence suggests that 35 kV systems will become more widespread in the future. Thus, SiC SSFCL systems will be needed that can provide adequate protection at the increased voltage level. The development of these systems will largely depend on the ratings of SiC semiconductor devices that become available.

REFERENCES

[1] *IEEE Recommended Practice for Calculating Short Circuits in Industrial and Commercial Power Systems*. IEEE Std. 551. 2006.

[2] L. M. Faulkenberry and W. Coffer, *Electrical Power Distribution and Transmission*, 1st ed. Englewood Cliffs, NJ: Prentice Hall, 1996.

[3] P. Gomes, “New strategies to improve bulk power system security: lessons learned from large blackouts,” in *IEEE Power Engineering Society General Meeting 2004*, Denver, CO, 2004, pp. 1703–1708.

[4] C. A. Ruiz, N. J. Orrego, and J. F. Gutierrez, “The Colombian 2007 black out,” in *Transmission and Distribution Conference and Exposition: Latin America 2008 IEEE/PES*, Bogota, Colombia, 2008, pp. 1–5.

[5] G. Andersson, P. Donalek, R. Farmer, N. Hatziargyriou, I. Kamwa, P. Kundur, N. Martins, J. Paserba, P. Pourbeik, J. Sanchez-Gasca, R. Schulz, A. Stankovic, C. Taylor, and V. Vittal, “Causes of the 2003 major grid blackouts in North America and Europe, and recommended means to improve system dynamic performance,” *IEEE Transactions on Power Systems*, vol. 20, no. 4, pp. 1922– 1928, Nov. 2005.

[6] Electricity Consumers Resource Council “The Economic Impacts of the August 2003 Blackout,” Feb. 2004. [Online]. Available: http://www.elcon.org/Documents/EconomicImpactsOfAugust2003Blackout.pdf.

[7] P. L. Anderson and I. K. Geckil, “Northeast Blackout Likely to Reduce US Earnings by $6.4 Billion,” Anderson Economic Group, AEG Working Paper 2003, Aug. 2003. [Online]. Available: http://www.andersoneconomicgroup.com/Portals/0/upload/Doc544.pdf.

[8] S. DiSavino, “Insight: Power reliability will cost Americans more | Reuters,” *Reuters*, 13-Sep-2011. [Online]. Available: http://www.reuters.com/article/2011/09/13/us-utilities-sandiego-blackout-id.

[9] R. Longley, “Power Interruptions Cost Nation $80 Billion Annually,” *About.com US Government Info*, Feb-2005. [Online]. Available:http://usgovinfo.about.com/od/consumerawareness/a/poweroutcosts.htm.

[10] M. M. R. Ahmed, “*Development of a solid-state fault current limiting and interrupting device suitable for power distribution networks*.” Ph.D. Dissertation, Northrumbia University. Newcastle, UK. 2002.

[11] U.S. Department of Energy, "Grid 2030: A National Vision for Electricity's Second 100 Years," Department of Energy Office of Electric Transmission and Distribution, Washington, D.C., Jul. 2003. [Online]. Available: http://energy.gov/sites/prod/files/oeprod/DocumentsandMedia/Electric_Vision_Document.pdf.

[12] U.S. Department of Energy, "National Electric Delivery Technologies Roadmap: Transforming the Grid to Revolutionize Electric Power in North America," U.S Department of Energy Office of Electric Transmission and Distribution, Washington, D.C., Jan. 2004. [Online]. Available: http://energy.gov/sites/prod/files/oeprod/DocumentsandMedia/ER_2-9-4.pdf.

[13] J. M. Bene, "Current limiting devices-Benchmark comparison," in *Conference Record of the 1988 IEEE Industry Applications Society Annual Meeting*, Pittsburg, PA, 1988, pp. 1355–1359.

[14] R. Kennan, "Fault Current Limiter: Problems and Prospects," *EPRI Journal*, pp. 14–20, Feb. 1976.

[15] V. H. Tahiliani and J. W. Porter, "Fault Current Limiters an Overview of EPRI Research," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-99, no. 5, pp. 1964–1969, Sep. 1980.

[16] C. A. Falcone, J. E. Beehler, W. E. Mekolites, and J. Grzan, "Current Limiting Device - A Utility's Need," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-93, no. 6, pp. 1768–1775, Nov. 1974.

[17] A. J. Power, "An overview of transmission fault current limiters," in *IEE Colloquium on Fault Current Limiters - A Look at Tomorrow*, 1995, pp. 1/1–1/5.

[18] P. Barkan, "The Current-Diverting FCL-A Practical Solution to Fault Current Limiting," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-99, no. 2, pp. 488–498, Mar. 1980.

[19] S. Eckroad, "Utility Needs Survey for Fault Current Limiters" in *International Workshop on Coated Conductors for Applications*, Dec. 2008, p. 7.

[20] P. M. Duggan, "Integration issues for fault current limiters and other new technologies- a utility perspective," in *IEEE Power Engineering Society General Meeting,* 2006, pp. 3-8.

[21] W. V. Hassenzahl, "Applications of superconductivity to electric power systems," *IEEE Power Engineering Review*, vol. 20, no. 5, pp. 4–7, May 2000.

[22] M. P. Oomen, "AC loss in superconducting tapes and cables," Ph.D. Dissertation, Universiteit Twente, Enschede, The Netherlands, 2000.

[23] A. Geim, S. Dubonos, J. Lok, M. Henini, and J. Maan, “Paramagnetic Meissner effect in small superconductors,” *Nature*, vol. 396, no. 6707, pp. 144–146, 1998.

[24] M. Noe and M. Steurer, “High-temperature superconductor fault current limiters: concepts, applications, and development status,” *Superconductor Science and Technology*, vol. 20, p. R15, 2007.

[25] D. U. Gubser, “Superconductivity: an emerging power-dense energy-efficient technology,” *IEEE Transactions on Applied Superconductivity*, vol. 14, no. 4, pp. 2037–2046, Dec. 2004.

[26] P. M. Grant, “Superconductivity and electric power: promises, promises ... past, present and future,” *IEEE Transactions on Applied Superconductivity*, vol. 7, no. 2, pp. 112–133, Jun. 1997.

[27] C. H. Rosner, “Superconductivity: star technology for the 21st century,” *IEEE Transactions on Applied Superconductivity*, vol. 11, no. 1, pp. 39–48, Mar. 2001.

[28] Electric Power Research Institute, “Superconducting Fault Current Limiters: Technology Watch 2009,” EPRI, 2009. [Online] Available: http://www.smartgridnews.com/artman/uploads/1/000000000001017793.pdf.

[29] S. M. Blair, N. K. Singh, C. D. Booth, and G. M. Burt, “Operational control and protection implications of fault current limitation in distribution networks,” in *Universities Power Engineering Conference (UPEC), 2009 Proceedings of the 44th International*, 2009, pp. 1–5.

[30] H. Boenig and D. Paice, “Fault current limiter using a superconducting coil,” *IEEE Transactions on Magnetics*, vol. 19, no. 3, pp. 1051– 1053, May 1983.

[31] W. Paul, J. Rhyner, and F. Platter, “Superconducting fault current limiters based on high Tc superconductors,” in *IEE Colloquium on Fault Current Limiters - A Look at Tomorrow*, 1995, pp. 4/1–4/4.

[32] T. Matsumura, T. Uchii, and Y. Yokomizu, “Development of flux-lock-type fault current limiter with high-Tc superconducting element,” *IEEE Transactions on Applied Superconductivity*, vol. 7, no. 2, pp. 1001–1004, Jun. 1997.

[33] Sung-Hun Lim, Hyeong-Gon Kang, Hyo-Sang Choi, Seong-Ryong Lee, and Byoung-Sung Han, “Current limiting characteristics of flux-lock type high-TC superconducting fault current limiter with control circuit for magnetic field,” *IEEE Transactions on Applied Superconductivity*, vol. 13, no. 2, pp. 2056– 2059, Jun. 2003.

[34] Sung-Hun Lim, Hyo-Sang Choi, and Byoung-Sung Han, “Operational characteristics of a flux-lock-type high-Tc superconducting fault current limiter with a tap changer,” *IEEE Transactions on Applied Superconductivity*, vol. 14, no. 1, pp. 82– 86, Mar. 2004.

[35] F. Gentry and R. York, “High power semiconductor devices,” in *IRE International Convention Record*, 1965, vol. 13, pp. 35– 43.

[36] J. J. Bates and R. E. Colyer, “The impact of semiconductor devices on electrical power engineering,” *Radio and Electronic Engineer*, vol. 43, no. 1.2, pp. 115–124, Feb. 1973.

[37] F. W. Gutzwiller, “Thyristors and rectifier diodes-the semiconductor workhorses,” *IEEE Spectrum*, vol. 4, no. 8, pp. 102–111, Aug. 1967.

[38] G. Tang, “A fault current limiter for minimizing impacts of distributed generation on coordinated relay protection in radial systems,” M.A.Sc. Thesis, University of Toronto, Canada, 2005.

[39] B. Boribun and T. Kulworawanichpong, “Solid-state fault current limiter for voltage sag mitigation and its parameters design,” in *Proceedings of the 4th international conference on Circuits, systems and signals*, Stevens Point, WI, 2010, pp. 91–95.

[40] A. Abramovitz and K. Smedley, “Survey of Solid State Fault Current Limiters,” *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2770-2782, June 2012.

[41] B. Damsky, V. Gelman, and J. Frederick, “A Solid-State Current Limiter.” Jan. 2003 [Online] Available: http://www.epa.gov/electricpower-sf6/documents/conf02_damsky_paper.pdf.

[42] M. M. Ahmed, “Comparison of the performance of two solid state fault current limiters in the distribution network,” in *4th IET Conference on Power Electronics, Machines and Drives, 2008. PEMD 2008*, York, UK, 2008, pp. 772–776.

[43] T. Nguyen, “A comparison of selected thyristor-based fault current limiters,” M.S. Thesis, University of Arkansas, Fayetteville, 2008.

[44] M. Steurer, P. F. Ribeiro, and M. Noe, “Superconducting magnetic energy storage and fault current limiters-projects, considerations, and outlook,” in *Transmission and Distribution Conference and Exposition, 2003 IEEE PES*, Dallas, TX, 2003, vol. 3, pp. 1102– 1107.

[45] S. Orpe and N.K. Nair, “State of art of fault current limiters and their impact on overcurrent protection,” in *IEEE Power & Energy Society General Meeting 2009.* Calgary, Alberta, Canada, 2009, pp. 1–5.

[46] California Energy Commission, "Development of Fault Current Controller Technology: Prototyping, Laboratory Testing, and Field Demonstration," California Energy Commission, Public Interest Energy Research Program Final Project Report, Jun. 2011. [Online]. Available:
http://uc-ciee.org/downloads/FaultCurrentController.pdf.

[47] Z. C. Feng, *SiC Power Materials: Devices and Applications*. New York, NY: Springer, 2004.

[48] A. Semenov, A. Lopin, V. Puzikov, V. Baumer, and I. Dmitruk, "Fabrication of heterostructures based on layered nanocrystalline silicon carbide polytypes," *Semiconductors*, vol. 44, no. 6, pp. 816–823, 2010.

[49] T. R. McNutt, "Modeling and characterization of silicon carbide power devices," Ph.D. Dissertation, University of Arkansas, Fayetteville, 2004.

[50] G. L. Harris, *Properties of Silicon Carbide*. London, England: IET, 1995.

[51] M. Chinthavali, "Silicon Carbide GTO Thyristor Loss Model for HVDC Application," Master's Thesis, University of Tennessee, Knoxville, 2003.

[52] J. Wang, "Design, characterization, modeling and analysis of high voltage silicon carbide power devices," North Carolina State University, Raleigh, 2010.

[53] W. J. Choyke, H. Matsunami, and G. Pensl, *Silicon Carbide: Recent Major Advances*. Berlin, Germany: Springer, 2004.

[54] P. Raaback, "Modeling of the sublimation growth of silicon carbide crystals," Tech. D. Dissertation, Helsinki University of Technology, Espoo, Finland, 1999.

[55] M. Bakowski, "Roadmap for SiC power devices," *Journal of Telecommunications and Information Technology*, no. 3–4, pp. 19–30, 2000.

[56] P. Friedrichs, "SiC power devices for industrial applications," in *Power Electronics Conference (IPEC), 2010 International*, Sapporo, Japan, 2010, pp. 3241 –3248.

[57] M. O□stling, "Silicon carbide based power devices," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, San Francisco, CA, 2010, pp. 13.3.1–13.3.4.

[58] J. B. Casady and R. W. Johnson, "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid-State Electronics*, vol. 39, no. 10, pp. 1409–1422, Oct. 1996.

[59] L. Tolbert, B. Ozpineci, S. K. Islam, and M. Chinthavali, “Wide Bandgap Semiconductors for Utility Applications,” in *IASTED International Conference on Power and Energy Systems (PES 2003),* Palm Springs, FL, 2003, pp. 317–321.

[60] B. Ozpineci and L. M. Tolbert, *Comparison of Wide-Bandgap Semiconductors for Power Electronics Applications*. United States Department of Energy, 2004. [Online]. Available: http://www.ornl.gov/~webworks/cppr/y2001/rpt/118817.pdf.

[61] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Berlin, Germany: Springer, 2008.

[62] M. Saadeh, “Modeling of SiC P-channel insulated gate bipolar transistors (IGBTS),” M.S. Thesis, University of Arkansas, Fayetteville, 2011.

[63] D. A. Marckx, “Breakthrough in power electronics from SiC,” *National Renewable Energy Laboratory (NREL), Subcontract Report NREL/SR-500-38515*, 2006.

[64] B. Ozpineci, “System impact of silicon carbide power electronics on hybrid electric vehicle applications,” Ph.D. Dissertation. The University of Tennessee, Knoxville, 2002.

[65] M. Ostling, R. Ghandi, B. Buono, L. Lanni, B. G. Malm, and C. M. Zetterling, “SiC bipolar devices for high power and integrated drivers,” in *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2011 IEEE*, Atlanta, GA, 2011, pp. 227–234.

[66] Qingchun Zhang, R. Callanan, M. K. Das, Sei-Hyung Ryu, A. K. Agarwal, and J. W. Palmour, “SiC Power Devices for Microgrids,” *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 2889–2896, Dec. 2010.

[67] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, “Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments,” *Device and Materials Reliability, IEEE Transactions on*, vol. 10, no. 4, pp. 418 –426, Dec. 2010.

[68] J. Vobecky, “Design and technology of high-power silicon devices,” in *Mixed Design of Integrated Circuits and Systems (MIXDES), 2011 Proceedings of the 18th International Conference*, Gliwice, Poland, 2011, pp. 17 –22.

[69] M. Ostling, R. Ghandi, and C.-M. Zetterling, “SiC power devices — Present status, applications and future perspective,” in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Kanazawa, Ishikawa, Japan, 2011, pp. 10–15.

[70] M. Skowronski and S. Ha, “Degradation of hexagonal silicon-carbide-based bipolar devices,” *Journal of applied physics*, vol. 99, p. 011101, 2006.

[71] Q. (Jon) Zhang and A. K. Agarwal, “Design and technology considerations for SiC bipolar devices: BJTs, IGBTs, and GTOs,” *physica status solidi (a)*, vol. 206, no. 10, pp. 2431–2456, Oct. 2009.

[72] A. Agarwal, C. Capell, Q. Zhang, J. Richmond, R. Callanan, M. O’Loughlin, A. Burk, J. Melcher, J. Palmour, V. Temple, H. O’Brien, and C. J. Scozzie, “9 kV, 1 cm×1 cm SiC super GTO technology development for pulse power,” in *IEEE Pulsed Power Conference, 2009.* Washington, D.C., 2009, pp. 264–269.

[73] J. W. Palmour, J. Q. Zhang, M. K. Das, R. Callanan, A. K. Agarwal, and D. E. Grider, “SiC power devices for Smart Grid systems,” in *Power Electronics Conference (IPEC), 2010 International*, Sapporo, Japan, 2010, pp. 1006–1013.

[74] A. C. Patil, “Silicon Carbide JFET Integrated Circuit Technology for High-Temperature Sensors,” Ph.D. Dissertation, Case Western Reserve University, Cleveland, OH, 2009.

[75] S. Singh and J. A. Cooper, “Bipolar Integrated Circuits in 4H-SiC,” *Electron Devices, IEEE Transactions on*, vol. 58, no. 4, pp. 1084 –1090, Apr. 2011.

[76] S. Singh, “High-performance TTL bipolar integrated circuits in 4H-SiC,” Ph.D. Dissertation, Purdue University, West Lafayette, IN, 2010.

[77] P. G. Neudeck, S. L. Garverick, D. J. Spry, L. Y. Chen, G. M. Beheim, M. J. Krasowski, and M. Mehregany, “Extreme temperature 6H-SiC JFET integrated circuit technology,” *physica status solidi (a)*, vol. 206, no. 10, pp. 2329–2345, 2009.

[78] M. Mehregany, C. A. Zorman, N. Rajan, and Chien Hung Wu, “Silicon carbide MEMS for harsh environments,” *Proceedings of the IEEE*, vol. 86, no. 8, pp. 1594–1609, Aug. 1998.

[79] M. Shen, S. Krishnamurthy, and M. Mudholkar, “Design and performance of a high frequency silicon carbide inverter,” in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, Phoenix, AZ, 2011, pp. 2044 –2049.

[80] Hui Zhang and L. M. Tolbert, “Efficiency Impact of Silicon Carbide Power Electronics for Modern Wind Turbine Full Scale Frequency Converter,” *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 21–28, Jan. 2011.

[81] Hui Zhang and L. M. Tolbert, “SiC’s potential impact on the design of wind generation system,” in *34th Annual Conference of IEEE Industrial Electronics, 2008. IECON 2008*, Orlando, FL, 2008, pp. 2231–2235.

[82] G. T. Heydt, “The Next Generation of Power Distribution Systems,” *IEEE Transactions on Smart Grid*, vol. 1, no. 3, pp. 225–235, Dec. 2010.

[83] P. G. Slade, J.-L. Wu, E. J. Stacey, W. F. Stubler, R. E. Voshall, J. J. Bonk, J. W. Porter, and L. Hong, "The utility requirements for a distribution fault current limiter," *IEEE Transactions on Power Delivery*, vol. 7, no. 2, pp. 507–515, Apr. 1992.

[84] O. Saadeh, "Modeling and characterization of p-type silicon carbide gate turn off thyristors," Ph.D. Dissertation, University of Arkansas, Fayetteville, 2011.

[85] E. Johnson, O. S. Saadeh, H. A. Mantooth, J. C. Balda, S. S. Ang, and A. K. Agarwal, "An analysis of paralleled SiC bipolar devices," in *IEEE Power Electronics Specialists Conference, 2008. PESC 2008*, Rhodes, Greece, 2008, pp. 4762–4765.

[86] P. C. Todd, "Snubber circuits: Theory, design and application," in *Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM-900. Unitrode*, 1993. [Online]. Available: http://space.dianyuan.com/blog/u/50/1170381240.pdf.

[87] W. McMurray, "Optimum Snubbers for Power Semiconductors," *IEEE Transactions on Industry Applications*, vol. IA-8, no. 5, pp. 593–600, Sep. 1972.

[88] R. Severns and E. Reduce, "Design of snubbers for power circuits," *International Rectifier Corporation*, 2006. [Online]. Available: http://www.newark.com/pdfs/techarticles/cornell/design.pdf.

[89] M. Öhrström and L. Söder, "Fast fault detection for power distribution systems," Thesis, Royal Institute of Technology, Stockholm, Sweden, 2003.

[90] M. Ohrstrom and L. Soder, "Fast Protection of Strong Power Systems With Fault Current Limiters and PLL-Aided Fault Detection," *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 1538–1544, Jul. 2011.

[91] H. A. Mantooth, O. Saadeh, E. Johnson, J. C. Balda, S. S. Ang, A. B. Lostetter, and R. M. Schupbach, "Solid-state fault current limiters: Silicon versus silicon carbide," in *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century 2008*, Pittsburg, PA, 2008, pp. 1 –5.

[92] D. P. Kothari, *Modern Power System Analysis*, 1st ed., Boston, MA: McGraw-Hill, 2006.

[93] J. W. Nilsson and S. A. Riedel, *Electric Circuits*, 6th ed., Upper Saddle River, NJ: Prentice Hall, 2000.

[94] American Superconductor, "New Transmission Option: Case Study for Superconductor Cables," Denver, CO, April 2011. [Online]. Available: http://www.naruc.org/grants/Documents/MCCALL%20NARUC%204-2011.pdf.

[95] J. Minervini, “Superconductors for Power Transmission and Distribution,” Princeton, New Jersey, May 2009. [Online]. Available: http://www.pppl.gov/colloquia_pres/WC13MAY09_JMinervini2.pdf.

[96] ABB, “5SHY 35L4510 Asymmetric IGCT Datasheet.” ABB, May 2008. [Online]. Available: http://www05.abb.com/global/scot/scot256.nsf/veritydisplay/faee9d678a30fb23c125744b00287a56/$file/5shy%2035l4510_5sya1232-03may%2008.pdf

[97] J. W. Palmour, M. Das, S.H. Ryu, B. Hull, L. Cheng, Q. Zhang, R. Callanan, M. O’Loughlin, A. Burk, and A. K. Agarwal, “SiC Power Devices for Next Generation Energy Efficiency,” *220th ECS Meeting and Electrochemical Energy Summit*, Boston, MA, 2011, pp. 3–7.

[98] R. Eden, “Market Forecasts for Silicon Carbide and Gallium Nitride Power Semiconductors.” 2012. [Online]. Available: https://apec-conf.org/2012/images/PDF/2012/Industry_Sessions/is1.5.5.pdf.

[99] J. Palmour, “High Voltage Silicon Carbide Power Devices,” Cree. 2010. [Online]. Available: http://arpa-e.energy.gov.

[100] *IEEE Standard for AC High-Voltage Circuit Breakers Rated on a Symmetrical Current Basis - Preferred Ratings and Related Required Capabilities for Voltages Above 1000 V. IEEE Std. C37.06. 2009.*

[101] R. Singh, “Ultra High Voltage SiC Bipolar Devices for Reduced Power Electronics Complexity.” GeneSiC Semiconductor. 2011. [Online]. Available: http://arpa-e.energy.gov.

[102] Y. Sui, G. G. Walden, X. K. Wang, and J. A. Cooper, “Device Options and Design Considerations for High-Voltage (10-20 kV) SiC Power Switching Devices,” in *Materials science forum*, 2006, vol. 527, pp. 1449–1452.

[103] M. Shur, S. Rumyantsev, and M. Levinshtein, *SiC Materials And Devices*. World Scientific, 2006.

[104] “Utility Scale Silicon Carbide Power Transistors.” Cree. 2010. [Online]. Available: http://arpa- e.energy.gov.

[105] Qingchun Zhang, M. Das, J. Sumakeris, R. Callanan, and A. Agarwal, “12-kV p-Channel IGBTs With Low On-Resistance in 4H-SiC,” *IEEE Electron Device Letters*, vol. 29, no. 9, pp. 1027–1029, Sep. 2008.

[106] Qingchun Zhang, Jun Wang, C. Jonas, R. Callanan, J. J. Sumakeris, Sei-Hyung Ryu, M. Das, A. Agarwal, J. Palmour, and A. Q. Huang, “Design and Characterization of High-Voltage 4H-SiC p-IGBTs,” *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1912–1919, Aug. 2008.

[107] P. Ivanov, M. Levinshtein, T. Mnatsakanov, J. Palmour, and A. Agarwal, “Power bipolar devices based on silicon carbide,” *Semiconductors*, vol. 39, no. 8, pp. 861–877, 2005.

[108] N. Y. A. Shammas, R. Withanage, and D. Chamund, “Review of series and parallel connection of IGBTs,” *Circuits, Devices and Systems, IEE Proceedings* -, vol. 153, no. 1, pp. 34 – 39, Feb. 2006.

[109] W. Sung, “Design and Fabrication of 4H-SiC High Voltage Devices,” Ph.D. Disssertation, North Carolina State University, Raleigh, 2011.

[110] A. Ogunniyi, H. O’Brien, A. Lelis, C. Scozzie, W. Shaheen, A. Agarwal, J. Zhang, R. Callanan, and V. Temple, “The benefits and current progress of SiC SGTOs for pulse power applications,” in *Semiconductor Device Research Symposium 2009 International*, Berwyn Heights, MD, 2009, pp. 1–2.

[111] A. K. Agarwal, B. Damsky, J. Richmond, S. Krishnaswami, C. Capell, S.H. Ryu, and J. W. Palmour, “The first demonstration of the 1 cm $\times$ 1 cm SiC thyristor chip,” in *The 17th International Symposium on Power Semiconductor Devices and ICs, 2005*, Santa Barbara, CA, 2005, pp. 195 – 198.

[112] L. Cheng and A. Agarwal, “Development of Low $R_{on,diff}$ 12 kV 4H-SiC GTOs for High-Power and High-Temperature Applications,” presented at *High Temperature Electronics Conference (HiTEC)*, Albuquerque, NM, 2012.

[113] Eaton, “Evaluating Efficiency and Losses of Various Circuit Protective Devices.” Eaton Corporation, July 2010. [Online]. Available: http://www.eaton.com/Eaton/ProductsServices/Electrical/ThoughtLeadership/WhitePapers/index.htm.

[114] R. H. Lasseter, “CERTS microgrid,” in *2007 IEEE International Conference on System of Systems Engineering*, San Antonio, TX, 2007, pp. 1–5.

[115] P. Piagi, “Microgrid Control,” Ph.D. Dissertation, The University of Wisconsin - Madison, Madison, 2005.