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Design of an RF CMOS Power Amplifier for Wireless Sensor Networks

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DESIGN OF AN RF CMOS POWER AMPLIFIER FOR WIRELESS SENSOR NETWORKS

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A thesis submitted in partial fulfillment
of the requirements for the degree of
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By

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ABSTRACT

The Power Amplifier (PA) is the last Radio Frequency (RF) building block in a transmitter, directly driving an antenna. The low power RF input signal of the PA is amplified to a significant power RF output signal by converting DC power into RF power. Since the PA consumes a majority of the power, efficiency plays one of the most important roles in a PA design. Designing an efficient, fully integrated RF PA that can operate at low supply voltage (1.2V), low power, and low RF frequency (433MHz) is a major challenge. The class E Power Amplifier, which is one type of switch mode PA, is preferred in such a scenario because of its higher theoretical efficiency compared to linear power amplifiers. A controllable class E RF power amplifier design implemented in 0.13µm CMOS process is presented. The circuit was designed, simulated, laid out, fabricated, and tested. The PA will be integrated as a part of a complete wireless transceiver system using the same process.

This thesis is approved for recommendation
to the Graduate Council.

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I would like to thank Dr. Scott Smith and Dr. Randy Brown for being on my thesis committee. I also want to thank all my team members in the MSCAD lab for all the support and help they have given me.

DEDICATION

To God

"For I know the plans I have for you," declares the LORD, "plans to prosper you and not to harm you, plans to give you hope and a future." Jeremiah 29:11

To my parents, Shuyi Pan and Mengyu Hai,

for their unconditional love, support, and encouragement

And to all my best friends for always believing in me…

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

Introduction

An RF power amplifier (PA) is one of the key circuit blocks in a transceiver of a wireless system. The main objective of the PA is to raise the power level of an RF signal. Since the RF signal needs to be transmitted through an antenna in a transmitter, successful delivery of the signal requires enough signal power to conquer the power degradation while transmitting in the air. The PA is widely implemented in various wireless communication systems.

This thesis presents a design of an RF CMOS class E power amplifier for wireless sensor networks. The content of the thesis is organized according to the design flow. In the following chapters, the wireless sensor networks that utilize a PA will be introduced. It will be followed by a discussion about choosing the right PA topology among all available options. Then, the class E PA will be the focus in the thesis in terms of its basic theory, design procedures, simulation, testing, and data analysis. Finally, conclusions will be drawn and future work will be discussed.

1.1 Introduction to Wireless Sensor Networks

A wireless sensor network, WSN, is a wireless network that consists of spatially distributed nodes that can communicate to each other and monitor environmental or physical conditions [5]. A single sensor or multiple sensors that are deployed in quantity are connected to a WSN node, and each WSN can be built of nodes from a few to several hundred or even more. All these sensors collect data and pass it on to the nodes. Then the nodes wirelessly communicate with a hub so that the data collected can be processed and analyzed according to the needs.

WSNs are also becoming more common in various fields of application such as biomedical applications, industrial applications, environmental applications, and civil infrastructure applications, etc. In biomedical applications, WSNs can be utilized as part of a

wireless pacemaker that is embedded in a patient's body and used to read data such as heart rate or blood pressure so that the patient's doctor can wirelessly monitor the patient's cardiac condition. In the industrial applications, for example, WSNs can be used to collect temperature and pressure data in a gas pipe in oil and gas industries where the data can be measured and transmitted wirelessly to the main control station. The control station then can send out control signals to a local sub-controlling unit to adjust the temperature and pressure in the gas pipe according to the safety standards. What's more, WSNs can play an essential role in environmental and civil infrastructure applications. For instance, WSNs can be used to monitor harsh environmental conditions such as ice glaciers, mountains or places that could be potentially dangerous to human beings. Another good example is that WSNs can be used in monitoring the structural health of a building or a bridge for the purposes of conservation and protection.

1.2 Functional Blocks in the WSN

After learning about WSNs, it is necessary to understand how a PA works as a part of a WSN and how the PA interacts with the rest of the functional blocks within the WSN. But first, it is also necessary to learn about various functional blocks in the WSN. Figure 1.1 gives a functional block diagram of a WSN channel in which the presented PA design will be integrated. This WSN consists of RF, analog, and digital circuits. To be more detailed, the WSN includes an antenna, a receiver, a transmitter, a digital core, a multi-channel analog to digital converter (ADC) as interfacing circuitry, and a variety of sensors. Of these blocks, the blocks designed to be integrated on one chip are the receiver, the transmitter, the digital core, the multi-channel ADC, and the temperature sensor. The PA is the last block in the transmitter and directly drives the antenna. The receiver and the transmitter share one antenna.

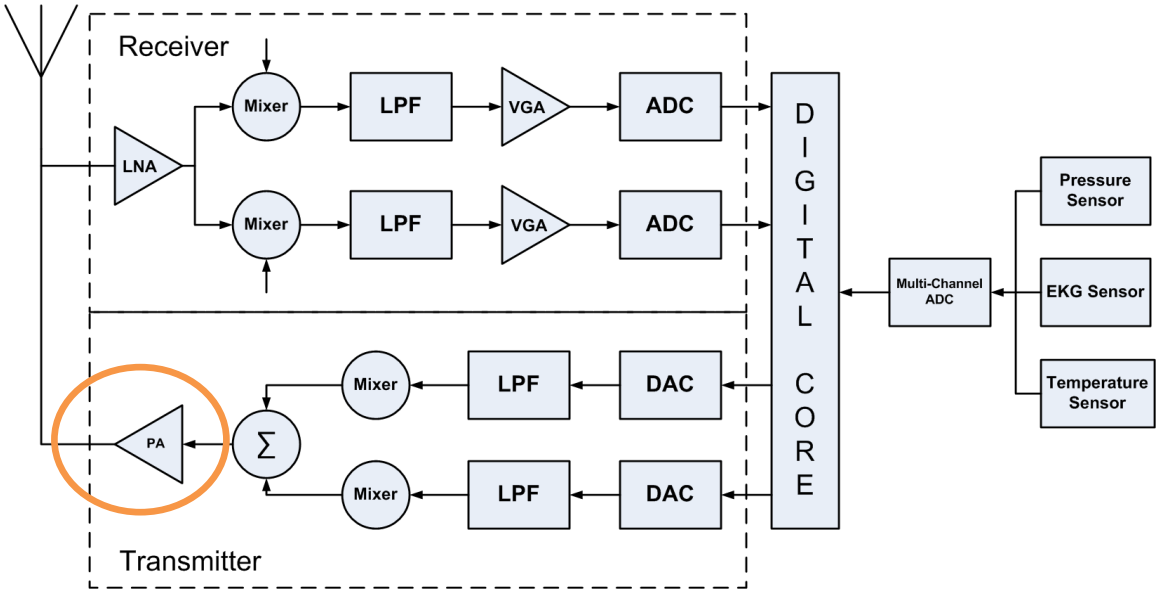

Figure 1.1. A simplified block diagram for wireless sensor networks of this design.

In Figure 1.1, an LNA is the first circuit block to receive RF signal from antenna. An LNA is a low noise amplifier. The LNA is the first RF block in the receiver and it amplifies the very weak RF signal captured by the antenna in the block diagram. The main objective of an LNA is to amplify the RF signal in voltage while adding as little noise and signal distortion as possible so that the signal can be retrieved in the later blocks in the system.

Mixers are critical components in an RF system and are used for frequency conversion. The main objective of the mixer is to shift the modulation from one carrier to another so that the signals can be processed effectively. The mixer is not only used as a down-conversion mixer right after the LNA in the receiver, but also as an up-conversion mixer right before the PA in the transmitter. When two signals at frequencies f1 and f2 are applied to the mixer, then the mixer produces signals at new frequencies at the sum, f1+f2, and difference, f1-f2. The sum or difference of higher harmonics of the original signals f1 and f2 can also be produced this way. So the frequency of the output signal of the mixer can be one of these produced frequencies.

The Low Pass Filter (LPF) is a filter that attenuates signals of all frequencies higher than its cutoff frequency but passes any frequency lower than the cutoff frequency. In the receiver, it is located between the VGA and ADC to remove the spurious signals on the mixer output. In the transmitter, it is placed between the up-conversion mixer and DAC to remove noise from the DAC sampling clock and the PCB noise on the transmitter input.

A variable-gain amplifier (VGA) is a type of amplifier that has a gain that can be varied by a control voltage. The VGA is used right after the down-conversion mixer in the receiver and right before the up-conversion mixer in the transmitter to boost the signal dynamic range according to the design needs.

The analog-to-digital converter (ADC) is a device that converts a continuous quantity to a discrete time digital representation. It functions as an interface between the real, analog world to the digital world by encoding analog inputs into digital outputs. The ADC is placed right after the LPF in the receiver and converts the filtered IF signal into a digital signal that can be used by the digital core.

Performing the reverse operation, the digital-to-analog converter (DAC) is a device that converts a discrete time digital code to a continuous analog signal. It provides interface between digital circuitry and analog circuitry. It is located between the digital core and the LPF in the transmitter.

Power amplifier (PA) is located between the up-conversion mixer and the antenna in the transmitter. This is because the output signal power produced by the mixer is too low to be transmitted by the antenna. The PA is needed in between to raise the signal power for proper signal transmission in the air. For the design presented in this thesis, the PA output power should be able to be adjusted to 4 levels according to the design needs. Multiple output power options

make it possible to use lower output power for transmission over short distances and higher for transmission over longer distances.

A voltage-controlled oscillator (VCO) is an oscillator with an oscillating frequency that is controlled by a DC voltage input. When the DC voltage varies, the frequency varies within the desired frequency range. Normally, the VCO works within a Phase Locked Loop (PLL). The objective of the VCO is to provide the needed carrier frequency for the mixers in the transceiver.

The Phase Locked Loop (PLL) is a control system that uses the VCO to keep the signal frequency produced by the VCO matched to the designed frequency. The PLL consists of the VCO and a phase detector. Not only does the PLL compare the phase of its input reference signal with the output signal phase of the VCO but also adjusts the frequency of the VCO to keep the phases matched. The voltage used to control the VCO in a feedback loop is produced by the phase detector.

CHAPTER 2

Power Amplifier Classification

There is more than one way to classify power amplifiers. A common way is to label each type of power amplifier with roman letters such as A, B, AB, C, D, E, F, etc. This is done according to either the biasing points or passive components in the output network which helps to form the drain voltage and current into a certain shape [4]. These power amplifiers can be classified as either linear amplifiers or non-linear amplifiers. The class A, class B, and class AB are normally categorized as linear amplifiers as opposed to the class C, class D, class E, and class F that are labeled nonlinear amplifiers. A brief introduction to each class of PA is shown below.

A class A amplifier shown in Figure 2.1 is a common linear amplifier. It is biased in such a way that the active device of the amplifier conducts throughout the entire cycle. Therefore, the main advantage of the class A amplifier is that it has very good linearity. However, the disadvantage is its low efficiency which is ideally only about 20%.

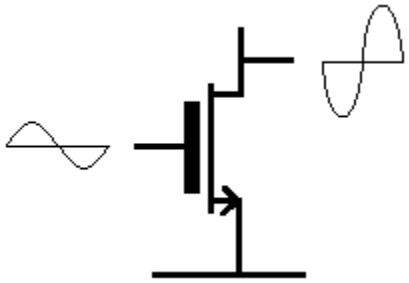

Figure 2.1. Class A amplifier.

A class B amplifier shown in Figure 2.2 is also a linear amplifier. The way it operates is similar to the class A except that the output devices of the class B amplifier only conduct for half the sinusoidal cycle. Therefore, it is common to use the class B amplifiers as a pair in a push-pull configuration. One conducts in the positive cycle and the other conducts in the negative cycle.

The class B is more efficient than the class A, about 50% [7], but has issues with linearity at the crossover point where one device turns off and the other device is turning on and vice versa.

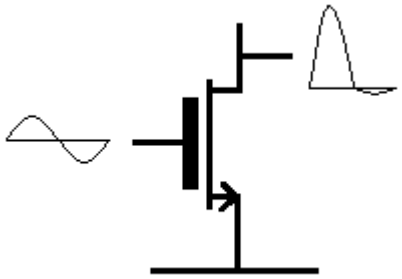

Figure 2.2. Class B amplifier.

A class AB amplifier is considered a linear amplifier shown in Figure 2.3. The class AB is a combination of the class A and the class B amplifiers. The major difference between the class AB and the class B is that the class AB allows two devices to be on at the same time near crossover but for a very short amount of time. Therefore, each device conducts for more than half a cycle but less than a full cycle. Because of this, better linearity and efficiency are both achieved at a balanced point. The linearity of the class AB is better than the class B, and the efficiency of the class AB is higher than the class A [7].

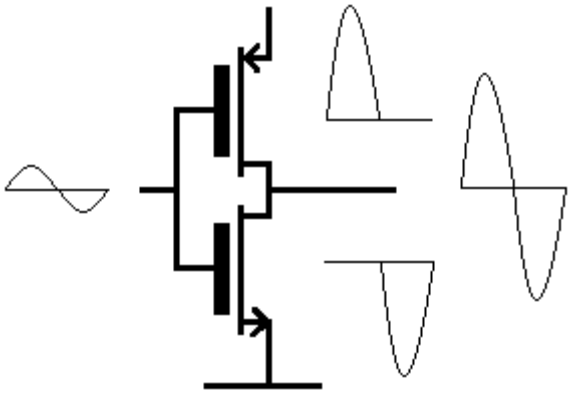

Figure 2.3. Class AB amplifier.

A class C amplifier is shown in Figure 2.4. The active device is biased in a way that the device only conducts less than half cycle of the input signal. According to [7], the class C

amplifier can reach an efficiency of 85% theoretically. However, the class C amplifiers do not have good linearity. The class C amplifier is not suitable for audio amplifiers due to its high distortion. Therefore, they are normally used for high power output applications at RF frequencies and distortion due to higher harmonics can be filtered out.

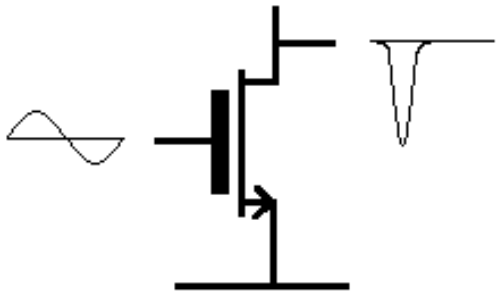

Figure 2.4. Class C amplifier.

A class D amplifier, shown in Figure 2.5, is considered to be a switching, or PWM, amplifier. It is commonly used as an audio amplifier. Compared to linear amplifiers, the power loss in the class D amplifiers can be significantly less because the active device MH or ML is either fully on or off. The transistors, MH and ML, cannot be turned on at the same time. When MH or ML is fully on, there is no power dissipation ideally in the switching active devices due to no path from the power supply to ground when one of the transistors is fully off. Therefore, efficiency can possibly be as high as 90% to 95% theoretically [8]. Normally a PWM carrier signal that is driving output devices is modulated by an audio signal. A low pass filter can be placed in the output stage to remove the high frequency components of the PWM signal [8].

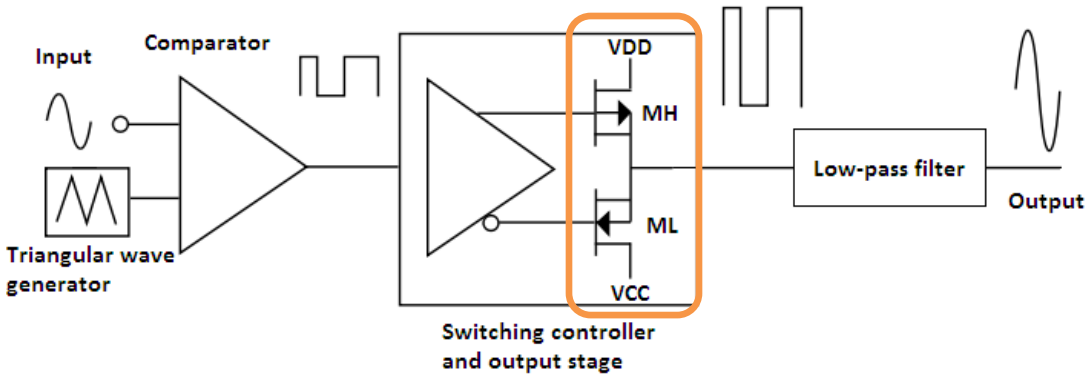

Figure 2.5. Class D amplifier.

A class E power amplifier shown in Figure 2.6 is the PA topology chosen for this design. It is considered a nonlinear or switching amplifier. The distinctive feature of the class E is that the drain voltage and current of the switching device are created in such a way that they do not occur simultaneously. This results in less power consumption. Therefore, the theoretical efficiency is very high. The class E is a popular choice for RF PA designs when compared to other options. More analysis on the class E amplifier will be discussed in the later chapters.

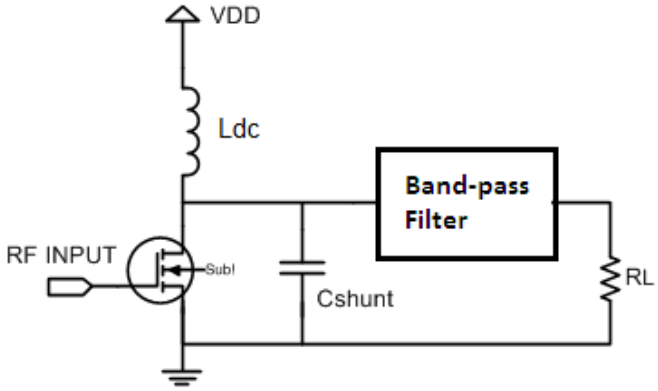

Figure 2.6. Class E amplifier.

A class F amplifier shown in Figure 2.7 is another type of switching mode amplifier which is nonlinear. Just like the class E amplifier, the class F is a switching amplifier with a unique output network that shapes the drain voltage and current so that they do not overlap each

other which reduces power dissipation. Compared to the class E PA, the major difference is in the output network. The class F PA includes two parallel LC resonant tanks. One tank serves as a matching network tuned at the fundamental frequency. The other tank is a harmonic tuning network tuned at the 3rd order harmonic. Therefore, a short circuit can be seen at the even order harmonics, and an open circuit at the 3rd order harmonic. By doing so, ideally a square wave drain voltage and a half bridge rectified sine wave drain current are created but do not overlap each other for less power dissipation.

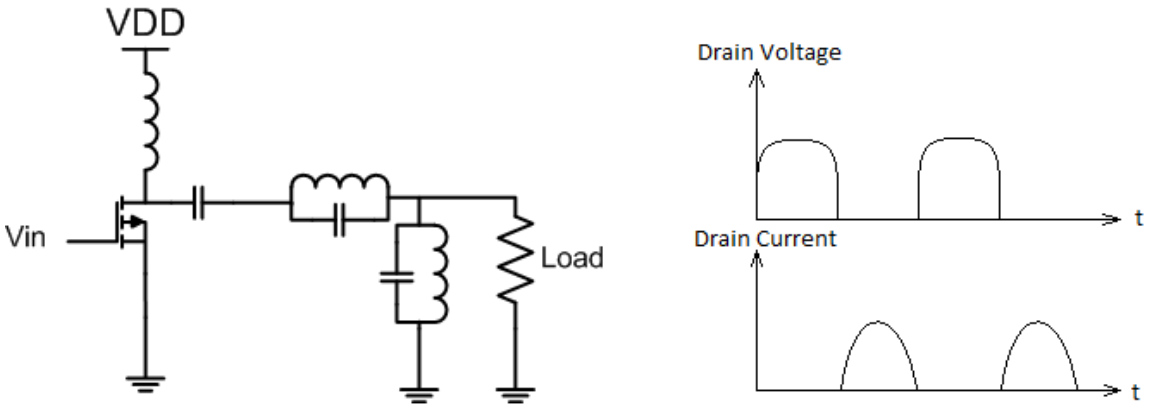

Figure 2.7. Class F amplifier.

Both linear and non-linear power amplifiers have positives and negatives. On one hand, the linear power amplifiers generally have good linearity but poor efficiency. On the other hand, the nonlinear power amplifiers generally have good efficiency but have poor linearity. So a trade-off between linearity and efficiency becomes a major factor for choosing an appropriate power amplifier.

Linearity of amplifiers refers to how an output signal is precisely proportional to an input signal of an amplifier while the signal power is amplified. The purpose of having high linearity is to make sure the content in the signal is not altered while the signal is amplified. For linear amplifiers like class A, its output signal is precisely proportional to its input signal since the

active device conducts throughout a full cycle of sine wave. The down side of the linear amplifiers is low efficiency. The class A amplifier is an example of this because the current drawn from power supply flows through the active device throughout the full cycle of sine wave so the power efficiency is much lower compared to non-linear amplifiers.

Efficiency, or power efficiency of an amplifier, is used to evaluate how well the amplifier transfers the DC power from the supply into useful AC output power without wasting it. One advantage of non-linear power amplifiers like the class E PA is their higher efficiency because the conducting angle or time for nonlinear amplifiers is much less than linear amplifiers in a cycle of a sine wave. Therefore, there is less current drawn to ground through active devices as opposed to current delivered to the output, which is good for efficiency. However, one negative about non-linear amplifiers is poor linearity. The output waveform is distorted compared to the input waveform in the process of power amplification. In Table 2.1, a comparison of the theoretical efficiency and linearity among the discussed power amplifier types is presented [7].

Table 2.1. Comparison in Efficiency Among Different Amplifier Classes.

Class	Operation	Theoretical Efficiency
A	Linear	50% max
B	Linear	78.5% max
AB	Linear	50%-78.5%
C	Non-linear	85%
D	Non-linear	90% or 100%
E	Non-linear	100%
F	Non-linear	88.4%

To choose an appropriate power amplifier requires considerations on signal modulation scheme, major performance parameters, and other factors for the benefits of this design project.

CHAPTER 3

Power Amplifier Design

3.1 Design Procedures

The design process of the RF power amplifier is presented in the flow chart in Figure 3.1. From the beginning, it is important to be clear in the design specification and aim of the design, which is helpful in achieving a successful design.

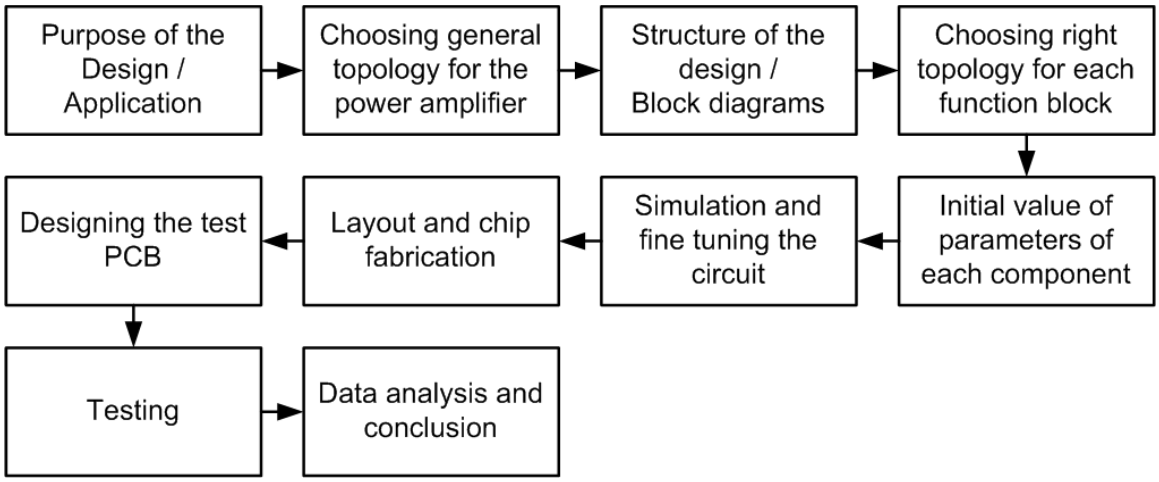

Figure 3.1. PA design flow.

Here is a list of design specifications that were known before designing the circuitry.

- Power supply: 1.2 V
- Operating frequency: 433 MHz
- Input/output impedance: 50 Ω
- Programmable power control: 4 output power levels
- High efficiency and low power application

3.2 Choosing a Suitable Topology

As mentioned in the last chapter, linear and nonlinear power amplifiers each have their own positives and negatives when it comes to a specific application. As far as this low power design is concerned, power efficiency is the most important performance parameter in choosing an appropriate topology while other parameters, such as output power, power supply consumption, S-parameters, etc., also need to be taken into consideration. Given the fact that the power supply in the future application will be batteries and the power amplifier is the most power hungry RF block in a transceiver, the efficiency plays a more important role than any other parameter. Another factor to be considered is the signal modulation scheme. PSK, phase shift keying, will be used as the signal modulation scheme for this project. Because PSK is a constant envelope modulation scheme in which information is embedded in phases, linearity of the power amplifier is not critical. Therefore, nonlinear amplifiers (class D, E, and F amplifiers) are chosen and investigated to see how efficient the nonlinear power amplifiers can be.

When choosing a suitable topology among nonlinear power amplifiers, there are many considerations to evaluate. The class E PA is preferred more than others due to factors presented below. First, class E power amplifiers are a popular choice for transceiver designs in the research field for applications where efficiency is important. Second, the class E power amplifiers have the highest theoretical efficiency compared to class D and F. This is a primary reason to choose class E to see how efficient it can be in reality in terms of this design project. Moreover, class D designs are generally used for audio power amplifications, which is not the purpose of this design project. Class F has a little more complicated output network that uses more inductors, which is clearly not desirable for this design in integrated form and given that the process being utilized has limited inductor capability. The reasons for using less on-chip inductors will be

explained in later chapters. Another reason for choosing class E over class F is that the active device in the class E can achieve "soft switching" [14] which is more advantageous than "hard switching" achieved in the class F. More details about the soft switching and the hard switching are presented in the following paragraphs.

For the hard switching shown in Figure 3.2 [9], nonzero drain current i_D and voltage v_D occur simultaneously for a finite time when an active device switches between ON and OFF states [6], which causes a substantial amount of power dissipation. This is the case for class F amplifiers.

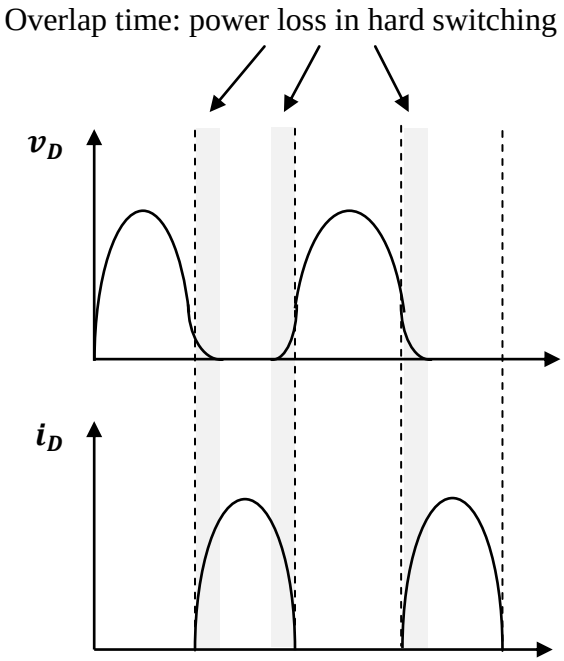

Figure 3.2. Power consumption in the hard switching.

On the other hand, the soft switching shown in Figure 3.3 is more beneficial than the hard switching in power dissipation reduction. The class E power amplifier is a soft switching architecture. This benefit comes from the class E PA output network that is designed in such a way that the drain voltage v_D returns to zero with a zero slope right before the switch turns on.

Ideally, this ensures that the nonzero drain voltage v_D and current i_D do not occur simultaneously, which is the definition of soft switching. Therefore, the power loss decreases dramatically during switching in class E power amplifiers.

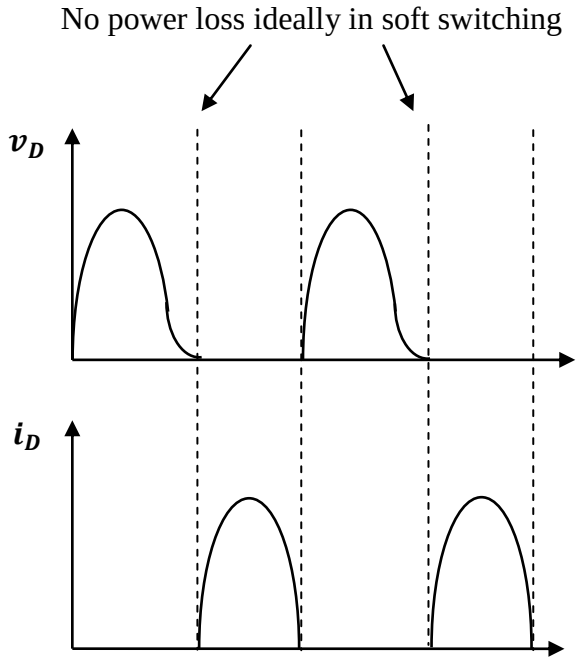

Figure 3.3. Reduced power consumption in soft switching.

3.3 A Conceptual Model for Class E Power Amplifier

The basic topology of a class E power amplifier is normally used as an output stage in a complete PA design. The class E PA topology consists of a passive load network and an active device [4]. In Figure 3.4, the active component used in this design is an NMOS transistor, and the passive load network includes a DC feed inductor L_{DC}, a shunt capacitor C_{SHUNT}, and an LC series resonant network that includes C_{TANK} and L_{TANK}. R_L is the load of the PA.

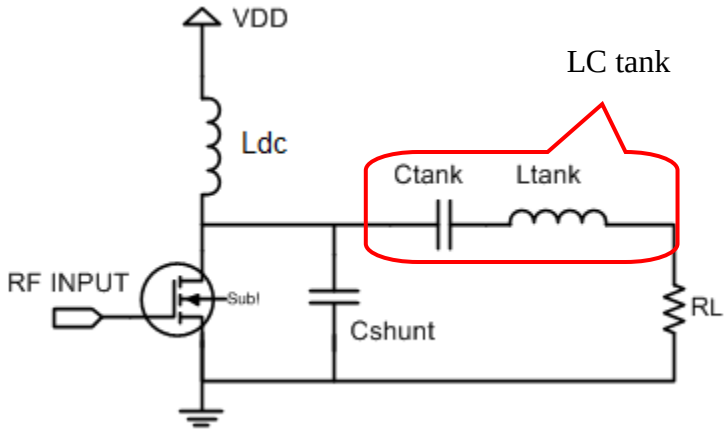

Figure 3.4. A conceptual model for the class E power amplifier.

Since the process design kit used for this project is CMOS, the switching active device is an NMOS transistor. For an NMOS, its operation includes three modes which are saturation mode, triode mode, and cutoff mode. When the NMOS transistor switches between the triode and the cutoff modes, it operates in the switching mode. When the transistor is in the triode mode the transistor is fully turned on. When the transistor is in the cutoff mode the transistor is fully turned off. The NMOS functions like a switch that has ON and OFF states, and it is controlled by a square wave on the gate of the device. The ideal duty cycle of the square wave is 50% [20].

The LC tank in series, in Figure 3.4, acts as a band-pass filter that only allows the signal at the fundamental frequency to pass to the load while removing components of higher and lower frequencies. In reality, the band pass filter, C_{TANK} and L_{TANK}, is slightly off-tuned from the operating frequency on purpose in Figure 3.5 because the L_{TANK} absorbs an extra inductance L_X. The L_X is required to compensate a phase shift generated by the DC feed inductor [22]. The L_{DC} feed inductor acts as a current source and blocks harmonics at the drain of the transistor going into the supply. The inductor also works with the shunt capacitor C_{SHUNT} as energy storage components to form the desired drain voltage and current waveforms shown in Figure 3.6 in maintaining the class E operation.

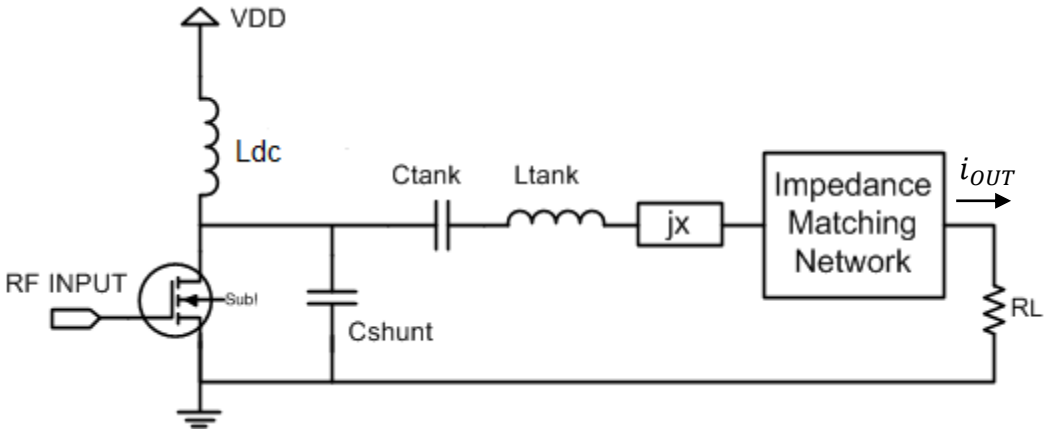

Figure 3.5. Output stage of class E power amplifier of this design.

Regarding the operation of the class E PA, more detailed analysis is shown below along with Figure 3.6. When the switch is on, the drain node is grounded ideally and the supply voltage, V_{DD}, is applied directly across the inductor L_{DC}. Since the transistor is on, L_{DC} starts the charging process. The charging process leads to an increase in inductor current from zero until reaching maximum current which is the peak at which the inductor behaves as a short circuit. Partial ramping current is used to support the sinusoidal output current [20], while the rest of the current flows to ground through the switch.

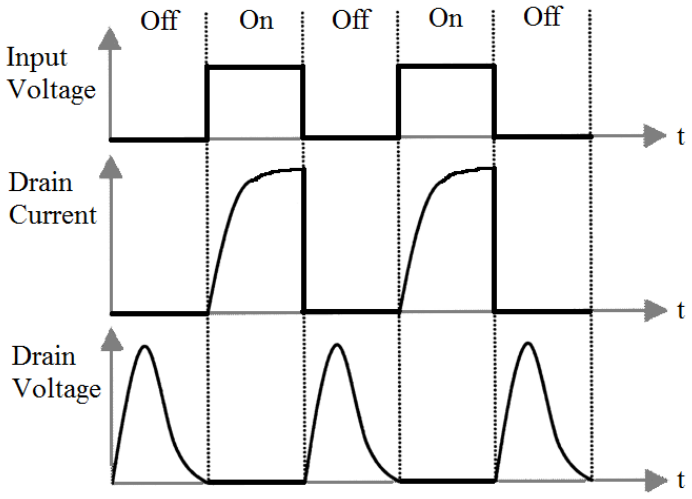

Figure 3.6. Drain voltage and current waveforms.

When the switch is turned off, there is no current going through the NMOS transistor. The drain current instantly drops to zero ideally and the capacitor C_{SHUNT} starts the charging process again. This causes the drain voltage v_D to increase from zero ideally. When the shunt capacitor is fully charged, the drain voltage reaches a peak which is about $3.56V_{DD}$ [4] due to the discharging effect of the inductor L_{DC}. The $3.56V_{DD}$ is derived from a Fourier transformed drain voltage waveform that is used to calculate the maximum drain voltage [4]. Then the shunt capacitor starts discharging from the peak and the current flows back to the inductor L_{DC}, which causes the drain voltage to decrease. When the shunt capacitor is fully discharged, the drain voltage reaches zero ideally. The shape of the voltage and the speed of the decay are determined by the combination of a few factors including operating frequency, V_{DD}, switching transistor sizing, and passive components such as C_{SHUNT}, L_{DC}, L_{TANK} and C_{TANK} as they are the components shaping the drain voltage and current by charging and discharging the current. The ideal class E operation is that the load network including these components is designed in such a way that the voltage v_{DRAIN} will return back to zero with a zero slope immediately before the switch is turned on in the Figure 3.6 [3][17], which is soft switching. This is one of optimum operating conditions from which nonlinear design equations (3.4) - (3.10) are derived, which ensures the drain voltage is fully discharged before the drain current increases. This can be observed by comparing drain voltage and current waveforms to see the drain current will not start ramping until the voltage comes back to zero with a zero slope. The optimum operation ensures that the shunt capacitor is fully discharged and the stored energy in the shunt capacitor is transferred into the inductor L_{DC} instead of being wasted when the transistor is turned on again. The main objective of the band pass filter is to only allow the fundamental component of the

drain waveform to pass through. Therefore, the embedded information in the input signal is transferred to the output with amplified power.

3.4 Circuit Design

The circuit design is the most crucial part of the whole process, from coming up with the design idea to a fabricated chip that is ready to be tested. Whether this is a successful design or not is largely determined by good reasoning and critical decision making with important design trade-offs taken into consideration.

3.4.1 Functional Blocks in the PA

In a complete class E power amplifier design, the design includes a driver stage and a class E output stage. If a power control feature is added to the PA, then a controlling circuit is also needed as the third part of the whole PA design. Initially in Figure 3.7, a simplified block diagram of the power amplifier was drawn to help to understand the circuit in a bigger picture. The overall power amplifier design contains two main blocks. One block is the power control unit and the other is the power amplifier. Since multiple output power control is required, it was decided to use a 2-to-4 decoder as a power selector.

From Figure 3.7, it can be seen that two digital control signals S0 and S1 are applied to the decoder as a selector. The S1 and S0 signals are a pure DC voltage which is either 1.2 V or 0 V. Between the 2-to-4 decoder and the power amplifier block, there are 4 control lines used to connect both blocks. Each line represents a different output power level. The power amplifier block has RF input and output signal terminals and is also biased by two DC voltages. The power supply is 1.2 V.

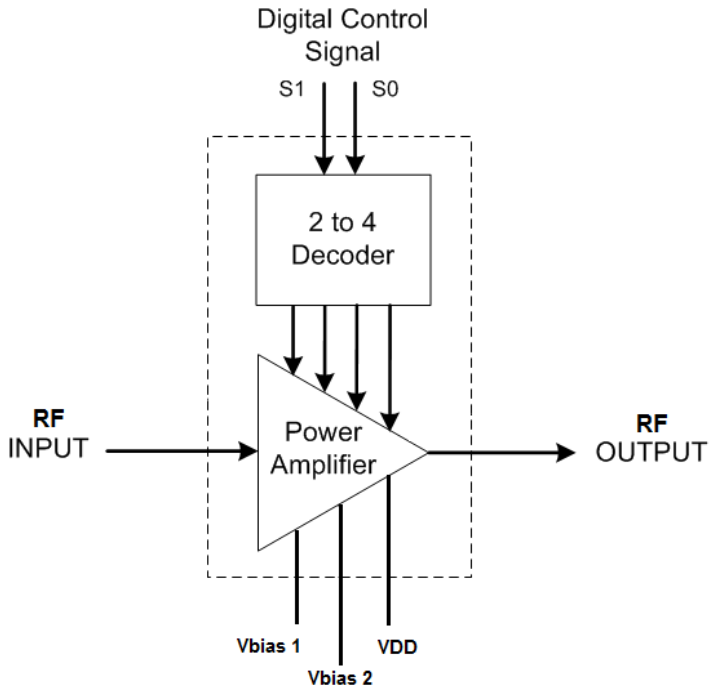

Figure 3.7. A simplified block diagram for PA.

Within the power amplifier block, it consists of several sub-blocks that are shown in Figure 3.8. The sub-blocks are the driver stage, the output stage, and four power control branches that are connected in parallel. Each power control branch is connected to one of four decoder outputs separately. During normal operation, only one control branch is turned on and the other three are off so that different output power levels are achieved at the output stage.

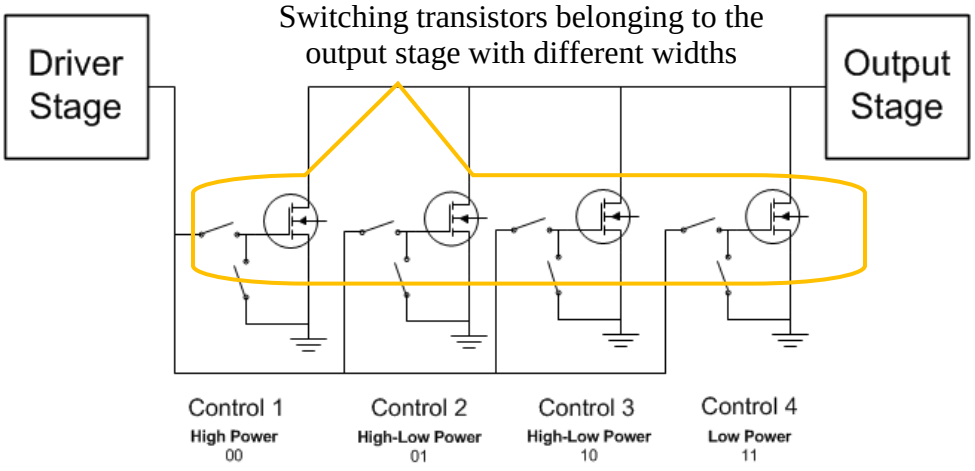

Figure 3.8. Relation between driver stage, output stage, and the controlling circuitry.

3.4.2 Output Stage

To design a power amplifier for this project, the starting point is the output stage which includes components listed in Table 3.1 except for R. The classic output stage was presented previously. The load of the output stage is just a 50 Ω resistor representing the antenna. Since the 2nd harmonic at 866 MHz is relatively close to the fundamental frequency 433 MHz in the output signal, a parallel LC tank shown in Figure 3.9 is added in the output stage to further suppress the higher harmonics.

Table 3.1. Components in the Output Stage.

Components
NMOS transistor
L_{DC}
C_{SHUNT}
C_{TANK}
L_{TANK}
L_X
Optimum resistance R

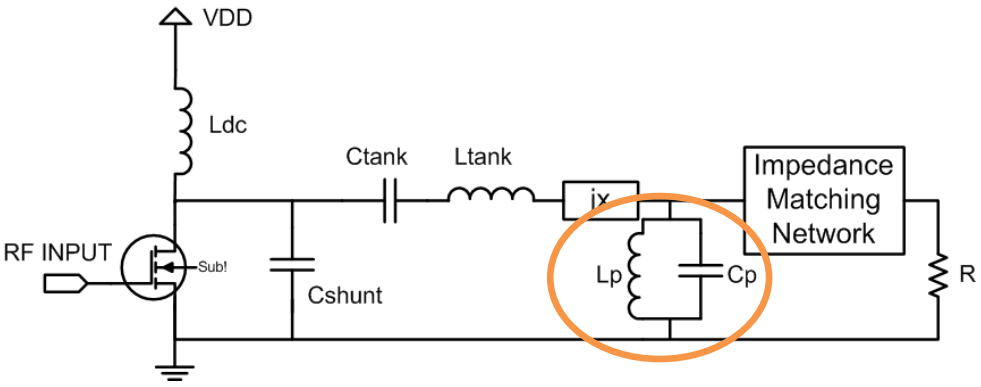

Figure 3.9. An LC resonant tank in parallel is included in the output stage.

According to Equations (3.4) – (3.10), initial values of the components in the output stage can be calculated for simulation [4], [12]. The Equations (3.4) – (3.10) describing the dependence of the components on output power, supply voltage, loaded quality factor and operating frequency are derived in [10], based on the following assumptions [4]:

1. The inductance of the L_{DC} is very high.
2. The quality factor of the series inductor L_{TANK} is high.
3. The loss in the switching transistors is negligible.
4. The drain voltage drops to zero with a zero slop before the drain current increases [12].

To make the NMOS function as a switch, a DC biasing voltage at its threshold voltage is applied between the gate of the NMOS transistor and a DC blocking capacitor. The length of the NMOS transistor is 240 nm and an optimum width is chosen to achieve the required output power. To choose the optimum width, however, there is not a simple governing equation found or mentioned in available papers [23]. However, one paper [23] mentioned the lowest value of W/L ratio of the transistor could be estimated. The method considers that there is no power dissipation in the output stage of the power amplifier ideally. Then the total power consumed from the power supply is 100% delivered to the load. Given the output power that is set to be 31.62 mW which is 15 dBm, then the average current flow from the supply can be calculated as

$$I_{DC\ average} = \frac{P_{out}}{V_{DD}} = \frac{31.62\times10^{-3}}{1.2} = 26.35\ mA \quad \textbf{(3.1)}$$

Since the current only conducts for half the signal cycle, the peak current should be at least twice the calculated value which is 52.7 mA. V_{gs} uses 1 V which is about in the middle of the range of the gate voltage of the switching transistor. V_{th}, the threshold voltage, is 0.56 V. The kn' value is 251.24 μA/V^2 which is derived from simulating the switching transistor in Cadence Spectre. Given these values, it is claimed that the W/L ratio can be calculated as

$$I_D = \frac{1}{2}K_n'\frac{W}{L}(V_{gs} - V_{th})^2 = 52.7\times10^{-3}A \quad \textbf{(3.2)}$$

$$\frac{W}{L} = \frac{W}{0.24\ \mu m} = 2166.95 \quad \textbf{(3.2.1)}$$

$$W_{MIN} = 2166.95\times0.24\ \mu m = 520\ \mu m \quad \textbf{(3.2.2)}$$

Given the initial width, the width is increased until reaching 1200 μm which shapes the drain voltage and current in a way that is closest to the optimum operation.

When ideal inductors and capacitors were used in simulations, different widths were tried from the beginning with the minimum width until the output power reached 15 dBm, where dBm or dBmW is the power radio in decibels of the measured power referenced to one milliwatt. When processed inductors and capacitors, pads, extracted parasitic components, and other non-idealities were included in the simulations, the output power dropped dramatically and the width of the transistor was increased further to make up for the drop, but 15 dBm could no longer be achieved. Given 1.2 V as the power supply voltage, the majority of the power is not delivered to the load but dissipated in parasitic resistance of on-chip inductors. Therefore, as presented in Table 4.2, the highest simulated output power that can be achieved is 9 dBm with parasitic extraction, pads, and bond wires taken into consideration.

The transistor is also sized to choose different output powers. In Equation 3.3 [4],

$$P_{out} = \frac{\pi^2+4}{8} I_{DC}^2 R \quad \textbf{(3.3)}$$

I_{DC} is the DC current flowing through the transistor when it is turned on. R in the equation is called optimum load in many papers. It is defined as a loading presented to the power amplifier for a desired output power with the highest efficiency [23]. The R is designed based upon given power supply voltage and output power. Since the optimum load varies from one design to another and normally does not equal to 50 Ω of antenna, an output impedance matching network is needed to match the optimum load to the 50 Ω for maximum power transportation. P_{out} is the output power delivered to the load. The equation shows a proportional relationship between the parameter P_{out} and I_{DC} when R is fixed. Therefore, different output powers can be achieved by using different transistor widths to allow different I_{DC} to flow through the transistors.

L_{TANK} and C_{TANK} are not uniquely determined [11]. They depend on the loaded Q-factor of the series LC resonant network. Another consideration for L_{TANK} is to use a smaller inductance for less parasitic resistance and power dissipation. Therefore, this is also a trade-off between Q_L and parasitic resistance of the inductor in determining the L_{TANK} value. L_{TANK}* is a combination of L_{TANK} and L_X.

$$R = \frac{8V_{DD}^2}{P_{OUT}(\pi^2+4)} = \frac{8\times(1.2)^2}{31.62\times10^{-3}\times(\pi^2+4)} = 26.29\ \Omega \quad \textbf{(3.4)}$$

$$\omega^2 = \frac{1}{LC} \quad \textbf{(3.5)}$$

$$L_{TANK} = \frac{8V_{DD}^2 Q_L}{\omega P_{OUT}(\pi^2+4)} = \frac{8\times(1.2)^2\times3}{2\pi\times433\times10^6\times(\pi^2+4)} = 29\ nH \quad \textbf{(3.6)}$$

$$C_{TANK} = \frac{P_{OUT}(\pi^2+4)}{\omega 8V_{DD}^2 Q_L} = \frac{31.62\times10^{-3}\times(\pi^2+4)}{2\pi\times433\times10^6\times8\times(1.2)^2\times3} = 4.66\ \text{pF} \quad \textbf{(3.7)}$$

$$C_{SHUNT} = \frac{P_{OUT}}{\pi\omega V_{DD}^2} = \frac{31.62\times10^{-3}}{\pi\times2\pi\times433\times10^6\times(1.2)^2} = 2.57pF \quad \textbf{(3.8)}$$

$$C_P = \frac{1}{L_P\times\omega^2} = \frac{1}{5\times10^{-9}\times(2\pi\times433\times10^6)^2} = 27\ pF \quad \textbf{(3.9)}$$

$$L_X = \frac{\pi V_{DD}^2(\pi^2-4)}{2\omega P_{OUT}(\pi^2+4)} = \frac{\pi\times(1.2)^2(\pi^2-4)}{2\times2\pi\times433\times10^6\times31.62\times10^{-3}\times(\pi^2+4)} = 11.12\ nH \quad \textbf{(3.10)}$$

$$L_{TANK}\ *= L_{TANK} + L_X \quad \textbf{(3.11)}$$

The capacitance C_{SHUNT} is one of the key factors affecting overall performance of the power amplifier. This is also a trade-off that needs to be considered in the design process because a lower value of the capacitance will help to achieve optimal performance for a higher frequency if it is required. However, the disadvantage of a smaller C_{SHUNT} is that it limits the maximum output power the PA can produce. So again, the C_{SHUNT} needs to be chosen carefully so that a possible maximum output power can be generated without sacrificing the high frequency of operation due to overly minimized C_{SHUNT}. The initial value of C_{SHUNT} can be determined by Equation (3.8). Q_L was chosen to be 3 according to the data that is provided along

with the design library. Several pairs of L_P and C_P values are available according to the Equation (3.5). A value of 5 nH was chosen for L_P as a smaller inductance for less parasitic resistance.

According to the paper, the value of the inductance L_{DC} is not critical, but should be high enough to be considered as a block for RF signals [11]. It can be chosen based on a rule of thumb as the following. Actually, L_{DC} can act as either an RF choke (large inductance) or a smaller DC-feed inductance. In a design that prefers smaller inductors, it is better to choose L_{DC} as the smaller DC feed inductance and small enough to still be able to shape the drain voltage and current. A smaller inductor has smaller series resistance, lower power dissipation, and higher efficiency. Moreover, this is very helpful in the design because the L_{DC} inductor is an on-chip component. An inductor with smaller inductance will consume much less space in layout. The initial value of L_{DC} was chosen to be 30 nH. The total area of the chip is very closely associated with the cost in fabrication of the chip. Regarding the impedance matching network, since the output impedance matching network is designed off chip, it will be discussed in Chapter 6.

3.4.3 Driver Stage

The main objective of the driver stage is to provide an RF square wave signal to overdrive the active device in the output stage. With the square wave, the NMOS transistor in the output stage can switch between cutoff and triode modes. The square wave is preferred over a sine wave because it takes less transition time from one switching state to another. A desirable driver stage should consume as little power as possible. Two different driver stage topologies are seen in current papers. One is using an inverter and the other one is using a class F amplifier.

To choose an appropriate driver stage, considerations include: how power hungry the driver stage is, how much chip space it consumes, and how well it provides a good square wave to drive the output stage. One advantage of using the inverter based driver stage is that the

inverter does not include any inductors, which saves space on the chip. However, a disadvantage is that it will increase the current consumption, especially at high frequencies [9], [20]. Compared to the inverter based driver stage, the class F driver stage shown in Figure 3.11 is preferred [1] because it consumes less power due to the nonlinear switching nature. The class F is also more commonly used as a driver stage than the inverter in papers, and the class F does a good job at producing a large peak-to-peak square wave to overdrive the output stage. The disadvantage of the class F driver stage is that it includes two inductors in the design. However, the size of the inductors will become less of an issue as operating frequency increases.

The class F circuitry includes two tuned parallel LC tanks that are placed in series between the power supply and the drain of the NMOS transistor. Using Equation (3.12), one LC tank is tuned to the fundamental harmonic which is 433 MHz and the other LC tank is tuned to the 3rd harmonic which is 1299 MHz. Smaller values of $L1_{TANK}$ and $L2_{TANK}$ were chosen among several L and C pairs for less parasitic resistance. Therefore, 9 nH was chosen for $L1_{TANK}$ and 3 nH was chosen for $L2_{TANK}$. Values of $C1_{TANK}$ and $C2_{TANK}$ were calculated in Equations (3.13) and (3.14).

$$\omega^2 = \frac{1}{LC} \tag{3.12}$$

$$C1_{TANK} = \frac{1}{L1_{TANK} \times \omega^2} = \frac{1}{9\times10^{-9}\times(2\pi\times433\times10^6)^2} = 15\ pF \tag{3.13}$$

$$C2_{TANK} = \frac{1}{L2_{TANK} \times \omega^2} = \frac{1}{3\times10^{-9}\times(2\pi\times433\times10^6\times3)^2} = 5\ pF \tag{3.14}$$

These two tanks attenuate signals of any frequency except the fundamental and the 3rd harmonic frequencies. The combination of these two frequencies creates a square wave ideally at the drain of the NMOS transistor in Figure 3.11. In Figure 3.10, it can be seen that the more odd harmonics that are superimposed [13], the more ideal the square wave that is produced. However, the increase in the number of the parallel LC tanks does increase the complexity of the driver

stage and power dissipation due to the parasitic resistance of the added inductors. Therefore, superposition of the 1st and the 3rd harmonics is enough for the purpose of the driver stage.

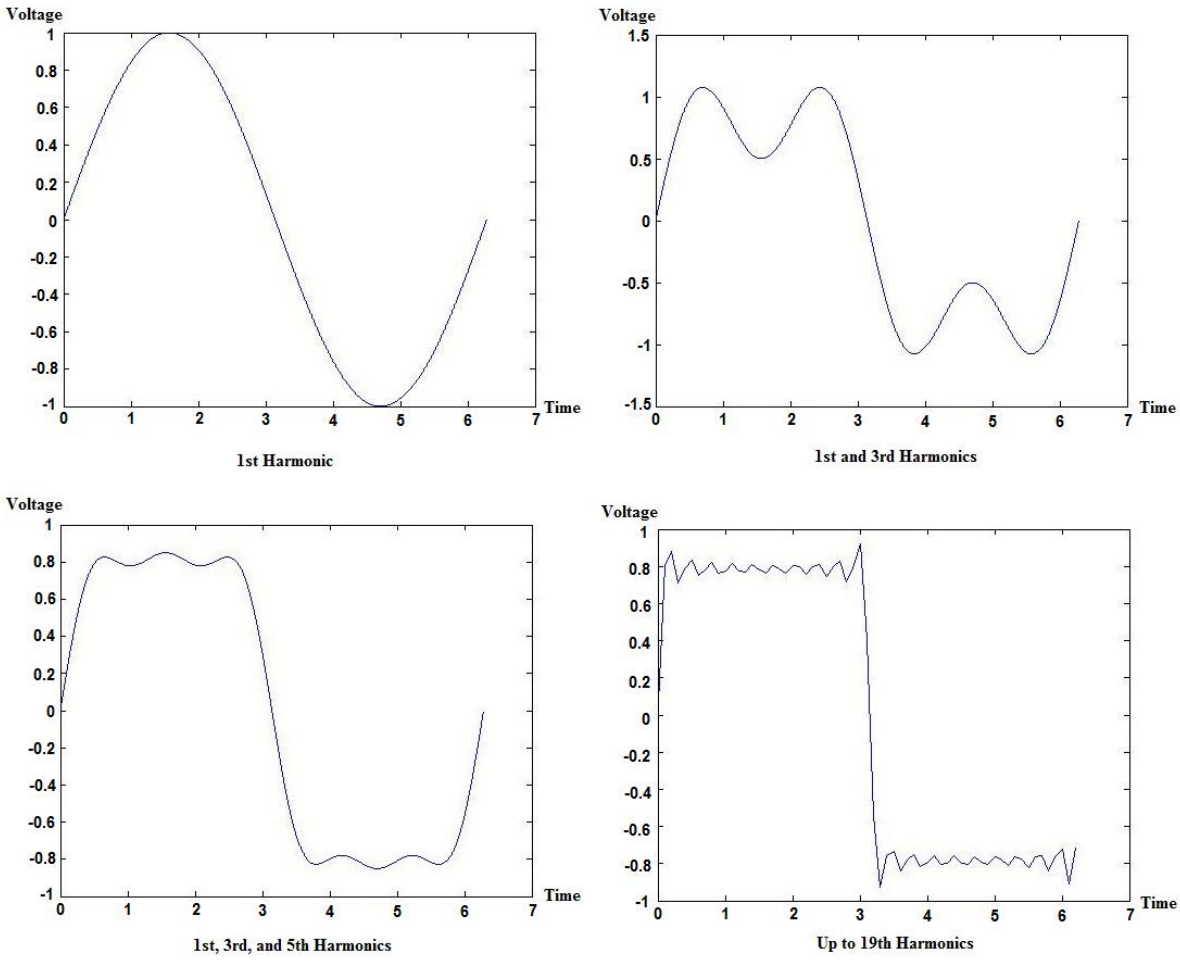

Figure 3.10. Superposition of harmonics.

To make the NMOS transistor operate as a switch, there is a DC blocking capacitor put between the input terminal and the gate of the NMOS transistor. Also, a DC biasing node is attached between the capacitor and the gate so that the gate voltage can be biased at the threshold voltage in Figure 3.11.

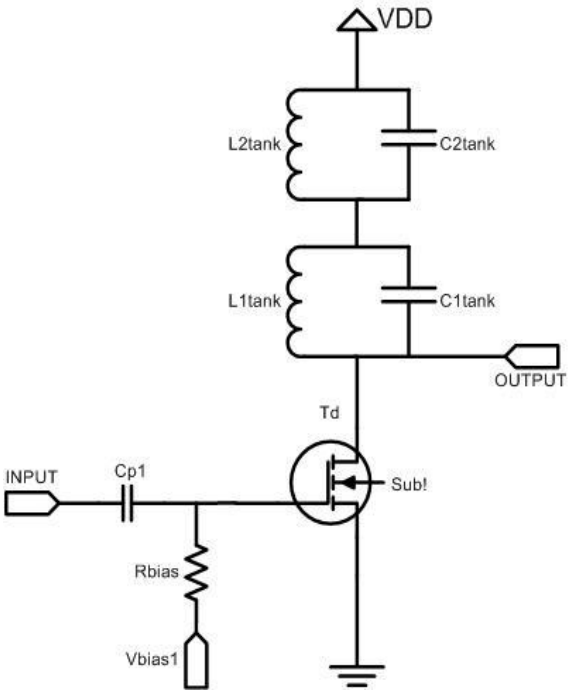

Figure 3.11. Driver stage of class E power amplifier.

3.4.4 Digital 2-to-4 Decoder

One of design specs for the PA is to provide multiple output powers. Because the transceiver will be used for low power wireless communication, it is necessary to have different output power options so that different power options can be used for transmitting signals over different distances. For signal transmission over shorter distances, a lower output power can be used to save battery life. For signal transmission over longer distances, a higher output power can be used to make sure the transmitted signal power is strong enough to be delivered to the destination. To accomplish this, the options are to use one controlling word to produce two different output powers, two controlling words to produce four different output powers, or three controlling words to produce eight different output powers. Eventually the 2-to-4 controlling scheme was chosen. This is because eight output power options are more than necessary and two output power options are insufficient.

A digital 2-to-4 decoder shown in Figure 3.12 is used in the design. The decoder uses a two-bit binary controlling word from a DSP unit to select one out of four outputs. The two-bit binary digital controlling word includes four combinations which are 00, 01, 10, and 11 according to the truth table shown in Figure 3.13. 0 represents 0 V and 1 represents 1.2 V. The controlling word 00, 01, 10, and 11 corresponds to the desired output power of 15 dBm (31.6 mW), 9 dBm (7.9 mW), 3 dBm (2 mW), and -3 dBm (0.5 mW). When the controlling word is received at the input terminals (S1, S2) of the decoder, a 1.2 V DC voltage will be generated at one of four output terminals while the other three are 0 V. This 1.2 V will turn on an analog controlling circuit in Figure 3.14 to achieve the functions explained in Section 3.4.5.

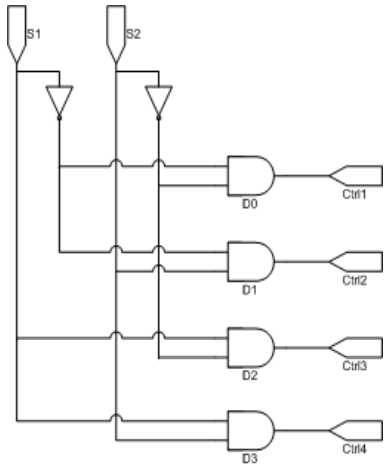

Figure 3.12. A 2-to-4 decoder.

X	Y	F0	F1	F2	F3
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

Figure 3.13. Truth table for 2-to-4 decoder.

3.4.5 Analog Controlling Circuit

Since four different output power options require four switching transistors with different widths in the output stage, only one switching transistor can be used at a time and the other three need to be turned off. What follows is the design of an analog controlling circuit to control which one out of four should be on.

An analog controlling circuit shown in Figure 3.14 is what is used in the presented design. The circuit in the Figure 3.14 is connected to one switching transistor M6 in the output stage. Since there are four different switching transistors, there are four analog controlling circuits with the same topology but different transistor sizing. The four analog controlling circuits are connected in parallel so that one of four always works at one time as shown in Figure 3.8. In the Figure 3.14, one controlling circuit includes an inverter (M1 and M2), a transmission gate (M3 and M4), and an NMOS transistor (M5) that functions as a switch.

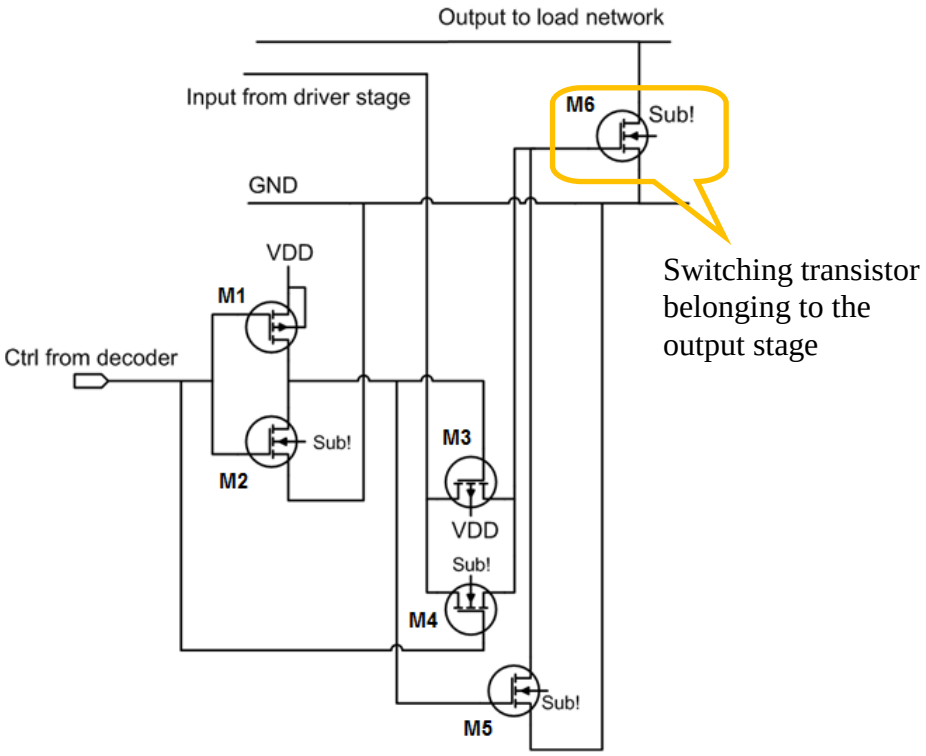

Figure 3.14. A controlling branch.

The NMOS transistor M5 is used to determine if the switching transistor M6 is turned on or not. When M5 is turned on, the gate of M6 is grounded, which means it is turned off. Otherwise, M5 is off so that M6 is on. M5 is controlled by the inverter which also controls the on and off states of the transmission gate, transistors M3 and M4. The transmission gate functions as a switch as well to pass or block the square wave produced from the driver stage to the gate of M6. When M6 is used, the transmission gate is on. Otherwise, it is off. Therefore, the transmission gate and M5 are both controlled by the inverter. The input signal fed to the inverter comes from one output of four in the 2-to-4 decoder. Therefore, there are four branches of the analog controlling circuit that function in the way described above. There is only one branch turned on to select the needed output power generated in the output stage and the remaining of three are off.

Since the inverter does not perform fast switching during operation, the transistors were sized to be smaller but still function appropriately for the design. This applies to the transmission gate and M5 transistor. The W/L ratio for M1 is twice that of M2 for the inverter. Inverters are normally sized to make sure rise and fall times are equal hence the twice as large PMOS, but it is not critical here. The W/L ratio for M3 and M4 in the transmission gate is set the same based on the same idea of using smaller active devices that still function the way they are designed.

3.4.6 RC Filters

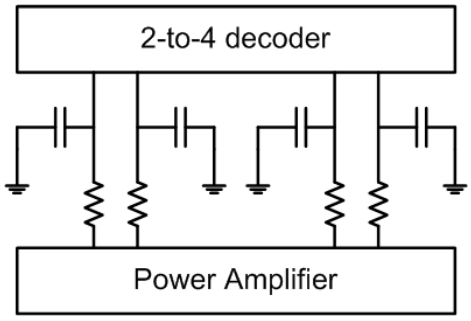

Figure 3.15. RC filters.

Since the 2-to-4 decoder is a digital circuit and the power amplifier block is an analog circuit, RC filters in Figure 3.15 should be added between two different circuit blocks to keep the noise or rich harmonics in the power amplifier block from interfering with the 2-to-4 decoder block. The RC filters in the Figure 3.15 are low pass filters. They attenuate higher frequencies and allow lower frequencies to pass through. The cutoff frequency can be calculated from Equation (3.10). The value of capacitors was chosen to be 20 pF.

$$f_C = \frac{1}{2\pi RC} \tag{3.10}$$

3.4.7 Components and Values

In Table 3.2, every component in the PA is shown in terms of its name and final value. The final values are slightly different from the initial calculated values due to ideality in the design equations and fine tuning of the component values for better performance. In Figure 3.16, a complete schematic is shown for the power amplifier block. The function blocks are the driver stage, the output stage, and the analog controlling circuits.

Table 3.2. List of Components and Values

Components	Name	Values
NMOS Transistor	Td	W=150µm, L=0.24µm
NMOS Transistor	T1	W=1200µm, L=0.24µm
NMOS Transistor	T2	W=104µm, L=0.24µm
NMOS Transistor	T3	W=40µm, L=0.24µm
NMOS Transistor	T4	W=24µm, L=0.24µm
PMOS Transistor	T11 (inverter)	W=600µm, L=0.24µm
NMOS Transistor	T12 (inverter)	W=300µm, L=0.24µm
PMOS Transistor	T13 (transmission gate)	W=240µm, L=0.24µm
NMOS Transistor	T14 (transmission gate)	W=240µm, L=0.24µm
NMOS Transistor	T15	W=36µm, L=0.24µm
PMOS Transistor	T21 (inverter)	W=320µm, L=0.24µm
NMOS Transistor	T22 (inverter)	W=160µm, L=0.24µm
PMOS Transistor	T23 (transmission gate)	W=160µm, L=0.24µm
NMOS Transistor	T24 (transmission gate)	W=160µm, L=0.24µm
NMOS Transistor	T25	W=50µm, L=0.24µm
PMOS Transistor	T31 (inverter)	W=240µm, L=0.24µm

NMOS Transistor	T32 (inverter)	W=120µm, L=0.24µm
PMOS Transistor	T33 (transmission gate)	W=180µm, L=0.24µm
NMOS Transistor	T34 (transmission gate)	W=180µm, L=0.24µm
NMOS Transistor	T35	W=72µm, L=0.24µm
PMOS Transistor	T41 (inverter)	W=200µm, L=0.24µm
NMOS Transistor	T42 (inverter)	W=100µm, L=0.24µm
PMOS Transistor	T43 (transmission gate)	W=240µm, L=0.24µm
NMOS Transistor	T44 (transmission gate)	W=240µm, L=0.24µm
NMOS Transistor	T45	W=36µm, L=0.24µm
DC Blocking Capacitor	Cd1	10pF
Driver Stage Capacitor	C1tank	12pF
Driver Stage Capacitor	C2tank	3.7pF
DC Blocking Capacitor	Cd2	10pF
Output Stage Capacitor	C_{SHUNT}	3.2pF
Output Stage Capacitor	C_{TANK}	6pF
Output Stage Capacitor	C_P	26pF
RC Filter Capacitor	C0, C1, C2, C3	20pF
Driver Stage Inductor	$L1_{TANK}$	9nH
Driver Stage Inductor	$L2_{TANK}$	2.9nH
Interstage Inductor	Lbias	72.519nH
Output Stage Inductor	L_{DC}	31.34nH
Output Stage Inductor	L_{TANK}* (including L_X)	38.924nH
Output Stage Inductor	L_P	5nH
7 Biasing Resistors	Rbias, OPrpp0~ OPrpp4	7.15K/each
28 RC Filter Resistors	R0, OPrpp4~OPrpp30	7.15K/each

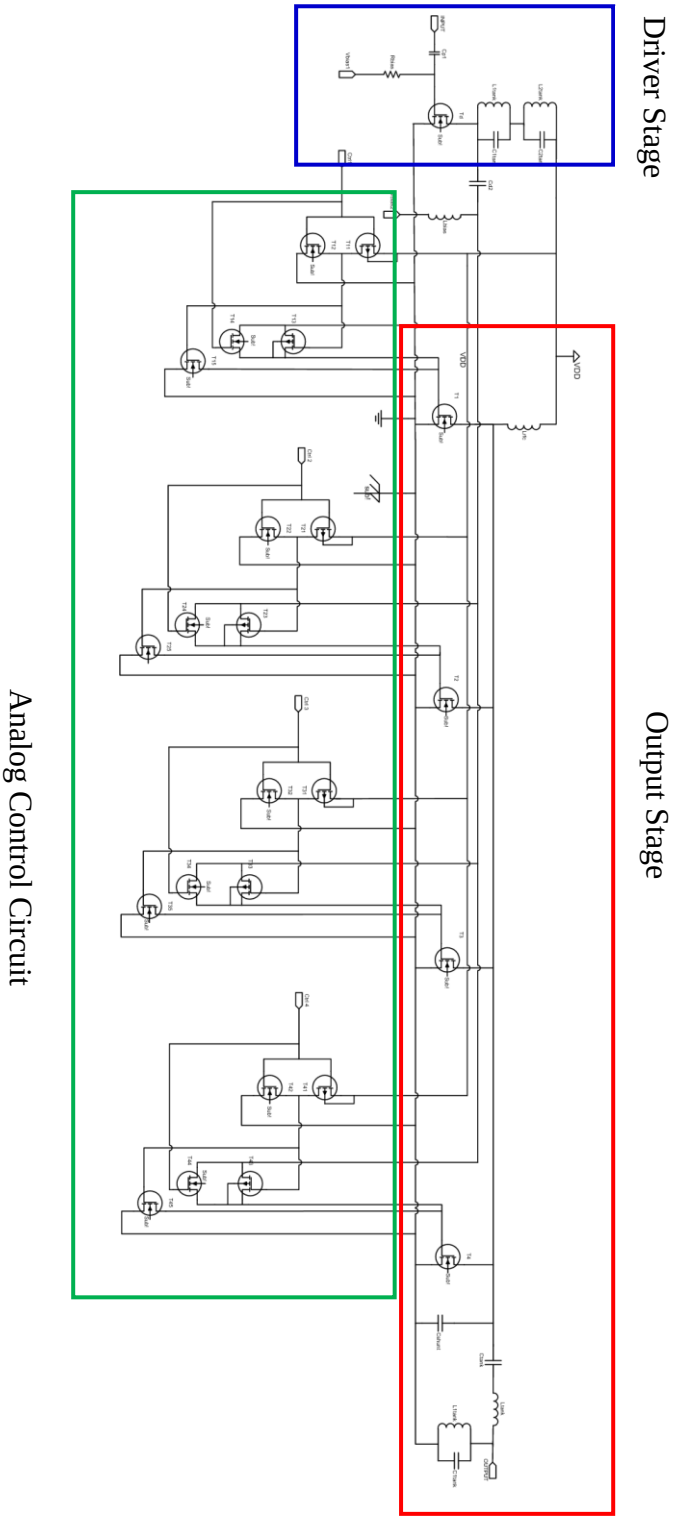

Figure 3.16. Schematic of Power Amplifier

CHAPTER 4

Simulations

After the circuit topology and all initial values of the component parameters are decided, simulation is the next step to evaluate the performance of the designed power amplifier. The performance is quantified and presented in various specs shown in the latter part of the chapter. All the simulations were performed in the Spectre simulator in Cadence Virtuoso 6.1 in UNIX environment.

4.1 Parameters and Metrics Introduction

4.1.1 Power Gain

RF amplifier power gain is defined as the difference of power in dBm between the output and the input signal or a ratio of the output to the input power. The power gain depicts how well the power amplifier delivers a much higher signal power to the load compared to the input power. The unit of the power gain is dB.

4.1.2 3 dB Bandwidth

The 3-dB bandwidth is the frequency response range where the signal frequency is within 3 dB below the peak of the power gain. It means that the PA can process a signal within that frequency range. The unit of the 3-dB bandwidth is in Hertz (Hz).

4.1.3 1dB Compression Point

The 1-dB compression point is used to depict the highest gain in its linear region. It describes the performance of the PA in linearity. When power gain is in the linear region, the increase of output power is proportional to the increase of the input power. When the gain begins dropping and the output power starts to not increase linearly with the increased input power, the

power compression occurs. When the power gain drops by 1 dB, it is defined as the 1-dB power compression point.

4.1.4 S-Parameters

Scattering parameters, or S-parameters, refer to the S parameter matrix for a generalized 2-port network. The four parameters are shown in Table 4.1.

Table 4.1. S-parameters

S11	Input port reflection coefficient
S12	Reverse isolation
S21	Forward Gain
S22	Output port reflection coefficient

S11 shows how well the input impedance is matched to the characteristic impedance which is 50 Ω, and S22 represents the output impedance matching. S11 and S22 are more of a concern than S12 and S21 since the main purpose of the S-parameters used in this design is to evaluate impedance matching at the input and the output of the PA. The lower S11 and S22 are in dBm, the better impedance matching it achieves. This is because S11 and S22 are a ratio that describes input and output signal reflection when the AC signal is treated as a wave. The lower the reflection that is present, the lower the S11 and S22 values are. Therefore, lower S11 and S22 represent better impedance matching.

4.1.5 Output Power, Input Power, and Supply Power Consumption

The purpose of output power testing is to measure the maximum power delivered at the output terminal of the PA under each power level condition. The input power is the power of the input signal fed to the PA. The supply power consumption is the total power consumed from the power supply to maintain proper operation of the PA. The unit of the three parameters is either in mW or dBm.

4.1.6 Power Added Efficiency

The power added efficiency, or PAE is the specification that evaluates how well the PA converts DC power into useful AC signal power when the input power is taken into consideration. The PAE is mathematically defined in Equation (4.1) [4]. The higher the PAE is, the better performance the PA achieves.

$$Power\ Added\ Efficiency = \frac{Output\ Power - Input\ Power}{Supply\ Power\ Consumption} \quad \textbf{(4.1)}$$

4.2 Simulated Results

In Figure 4.1, a test bench setup in Cadence is presented. In the test bench, bond wires are included. The pads are included inside the power amplifier block in the Figure 4.1. Bond wires are modeled as shown in Figure 4.2 and 4.3.

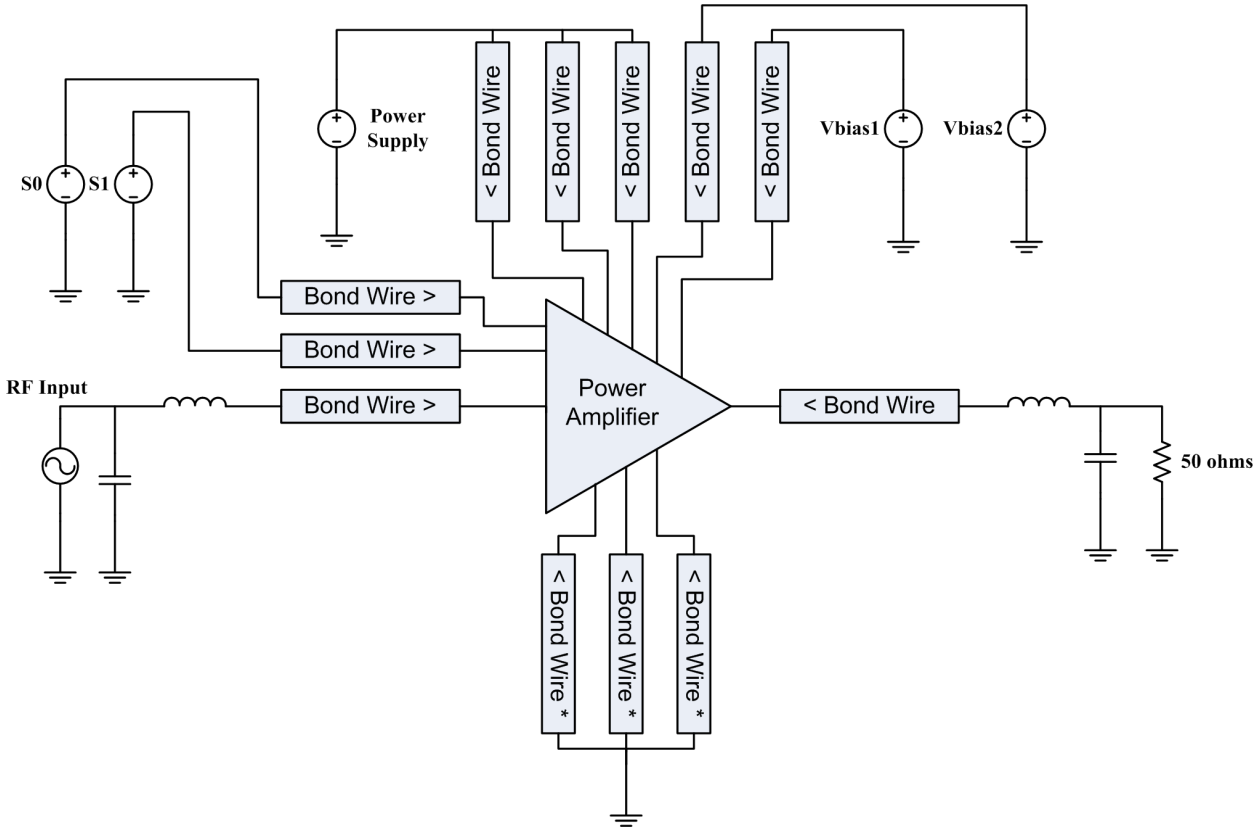

Figure 4.1. Test bench in Cadence Virtuoso.

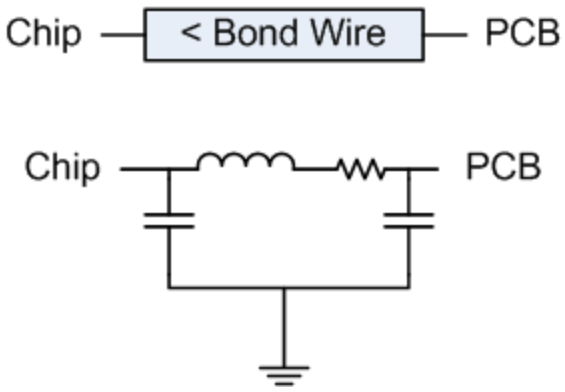

Figure 4.2. Regular bond wire model.

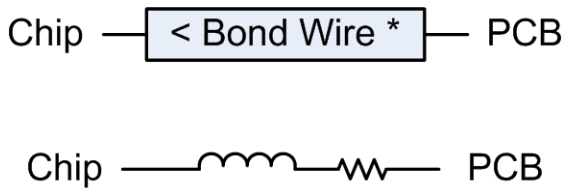

Figure 4.3. Bond wire model for ground connection.

The simulated results are collected and listed below in Table 4.2 and Figure 4.4. The simulated results listed in the Table 4.2. were derived upon the following conditions: V_{DD} = 1.2 V, input peak voltage = 200 mV, temperature = 25 ℃, RC parasitic extraction, and the highest output power level (S0=0, S1=0). The supply power consumption in the simulation is calculated as an average power of the product of power supply voltage and current. The transistor skew in the simulation was modified based on the original Fast NMOS-Slow PMOS (FS) skew and data from MOSIS for more accurate simulation that is close to actual performance of the fabricated NMOS and PMOS transistors. The PA input (blue) and output (red) transient voltage waveforms are shown in the Figure 4.4.

Table 4.2. Simulated Results for the Power Amplifier with RC Extraction.

Parameter		Value	Unit
F	Frequency	433	MHz
G	Power gain	12.79	dB
BW	3dB frequency bandwidth	128.35	MHz
P1dB	1-dB compression point	-19.91	dBm
S_{11}	Input return loss	-6.063	dB
S_{12}	Reverse isolation	-40.807	dB
S_{21}	Forward Power gain	7.549	dB
S_{22}	Output return loss	-27.869	dB
P_{OUT}	RF output power	7.916	mW
P_{IN}	RF input power	0.431	mW
P_{SUPPLY}	Supply power consumption	34.7	mW
PAE	Power added efficiency	21.57	%
Z_{IN}	Input impedance	38.22-48.78j	Ω
Z_{OUT}	Output impedance	53.39+2.20j	Ω

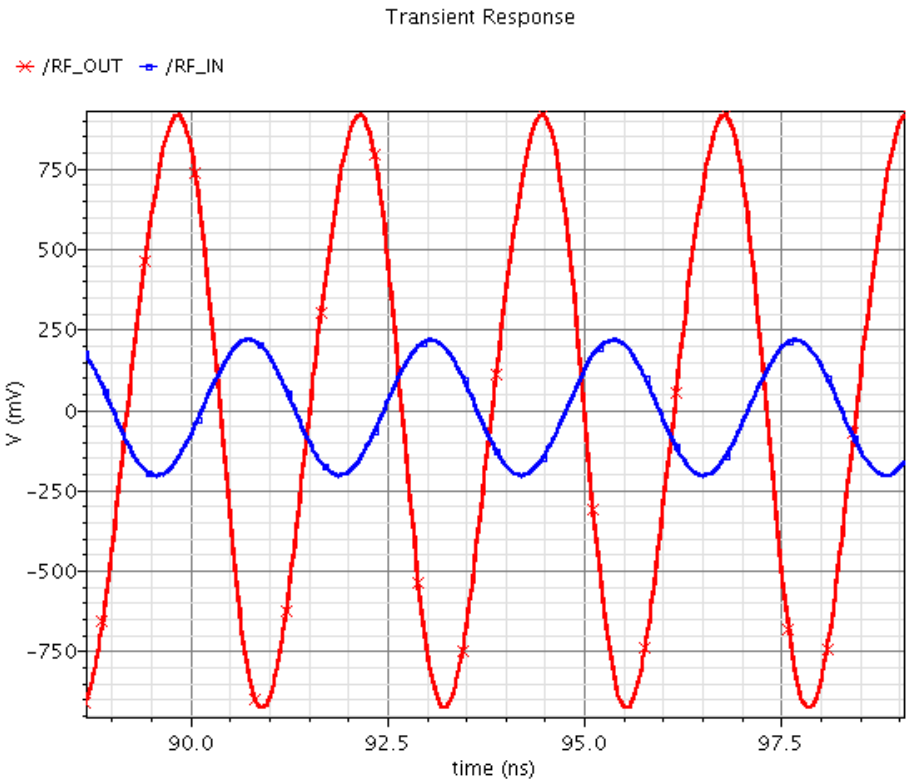

Figure 4.4. Transient waveform of input and output voltage signal.

In Table 4.2, the power added efficiency and the output power are the most important characteristics. The designed power amplifier achieves a simulated power added efficiency of 21.57% and an output power of 7.916 mW. The lower efficiency and the output power achieved in the simulations are due to several factors. Firstly, the process components used in the design are lossy in a non-ideal case, especially the process inductors. The power loss caused by the parasitic resistance of the inductors is the primary possible cause. Secondly, the power consumption in the driver stage consumes 19.36% of the total supply power consumption. A more power efficient driver stage will help boost the efficiency. Thirdly, the switching transistor has finite transition time when switching between the ON and the OFF states [6]. The longer the finite transition time is, the more power dissipation will be generated across the transistor. Therefore, the faster the transistor can switch from one state to the other, the more desirable the transistor is in the design. Last but not least, RC extraction makes the simulated PA performance drop even further. This is because the simulation with RC extraction will take parasitic resistance and parasitic capacitance from the traces into consideration to create a more accurate model of the PA. The parasitic resistance causes power dissipation and degrades the PA performance. Therefore, the simulation with RC extraction can emulate the actual PA IC responses more accurately although the performance is heavily affected. More explanation and analysis are shown in the later part of Chapter 6.

Simulations such as power supply variation and temperature variation were also performed to evaluate how much impact they would have. By varying the power supply from 1.08 V (-10%) to 1.32 V (+10%), the performance of the PA was observed. The simulated results are shown in Table 4.3. In Figures 4.5 and 4.6, the output power, the supply power consumption, the input power, and the power added efficiency are plotted over the power supply voltage range

from 1.08 V to 1.32 V. It can be seen that the PA operates better in a higher power supply voltage, achieving higher efficiency and output power.

Table 4.3. Simulated Results with Power Supply Variation and RC Extraction.

Parameter		Min	Typ	Max	Unit
V	Power supply	1.08	1.2	1.32	V
F	Frequency	433	433	433	MHz
G	Power gain	11.65	12.79	13.52	dB
P1dB	1-dB compression point	-15.37	-19.91	-21.11	dBm
S_{11}	Input return loss	-6.073	-6.063	-6.052	dB
S_{12}	Reverse isolation	-40.660	-40.807	-40.883	dB
S_{21}	Forward power gain	6.543	7.549	8.433	dB
S_{22}	Output return loss	-30.023	-27.869	-25.932	dB
P_{OUT}	RF output power	6.302	7.916	9.677	mW
P_{IN}	RF input power	0.431	0.431	0.4301	mW
P_{SUPPLY}	Power supply power	28.09	34.7	42.08	mW
PAE	Power added efficiency	20.90	21.57	21.97	%

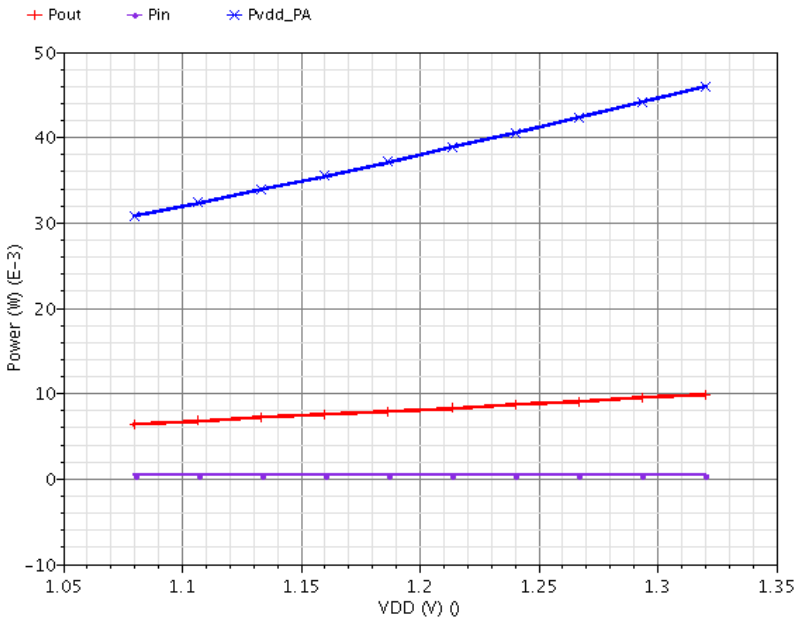

Figure 4.5. Power supply voltage versus output power, input power and power supply power.

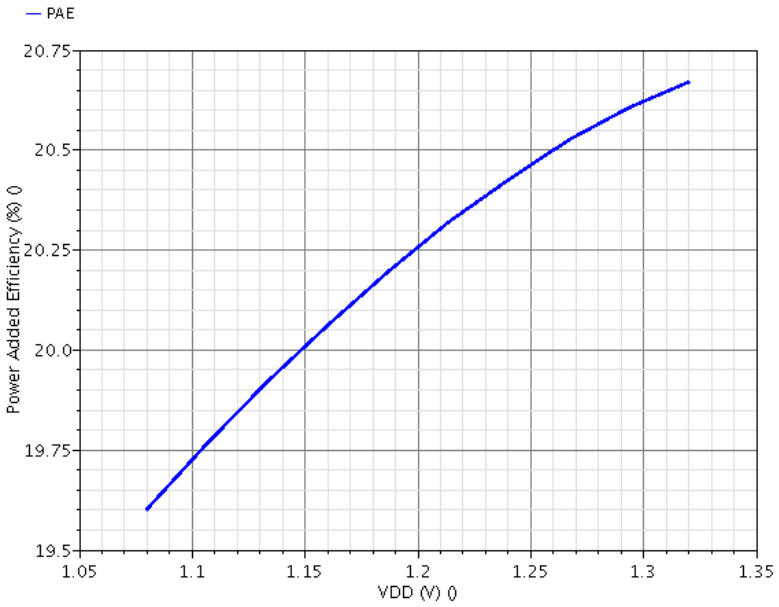

Figure 4.6. Power supply voltage versus PAE.

The PA was simulated from -55 °C to 125 °C. The simulated results are shown in Table 4.4. The power supply is 1.2 V and the frequency of the input signal is 433 MHz. According to the simulated results in Table 4.4, it can be observed that the performance of the power amplifier is better at lower temperatures than higher temperatures. The output power reaches 10.48 mW and the power added efficiency goes up to 27.84% at -55 °C. The improvements at low temperatures result from decreased resistance in the semiconductors and traces when the temperature decreases. The resistance of metal traces decreases when the temperature drops, which means there is less power dissipation in these metal traces and higher efficiency. Regarding the transistor at higher temperature, the increased temperature causes a decrease in the mobility of free carriers due to increasing lattice scattering in the semiconductor, which lowers the conduction in the channel of the transistor. The increased resistance will cause more power dissipation and lower efficiency.

Simulated plots are shown below in Figures 4.7-4.9 which demonstrate the behaviors of the output power, the power gain, and the power added efficiency across the wide temperature range. It can be seen that the output power, the power gain, and the power added efficiency vary linearly or almost linearly over the temperature sweep.

Table 4.4. Simulated Results with Temperature Variation

Parameter		Min	Typ	Max	UNIT
Temp	Temperature	-55	25	125	°C
F	Frequency	433	433	433	MHz
G	Power gain	14	12.79	10.91	dB
S_{11}	Input return loss	-7.241	-6.063	-4.762	dB
S_{12}	Reverse isolation	-40.013	-40.807	-41.811	dB
S_{21}	Forward power gain	8.973	7.549	5.908	dB
S_{22}	Output return loss	-24.928	-27.869	-35.044	dB
P_{OUT}	RF output power	10.48	7.916	5.621	mW
P_{IN}	RF input power	0.417	0.431	0.456	mW
P_{SUPPLY}	Power supply power	36.15	34.7	33.1	mW
PAE	Power added efficiency	27.84	21.57	15.60	%

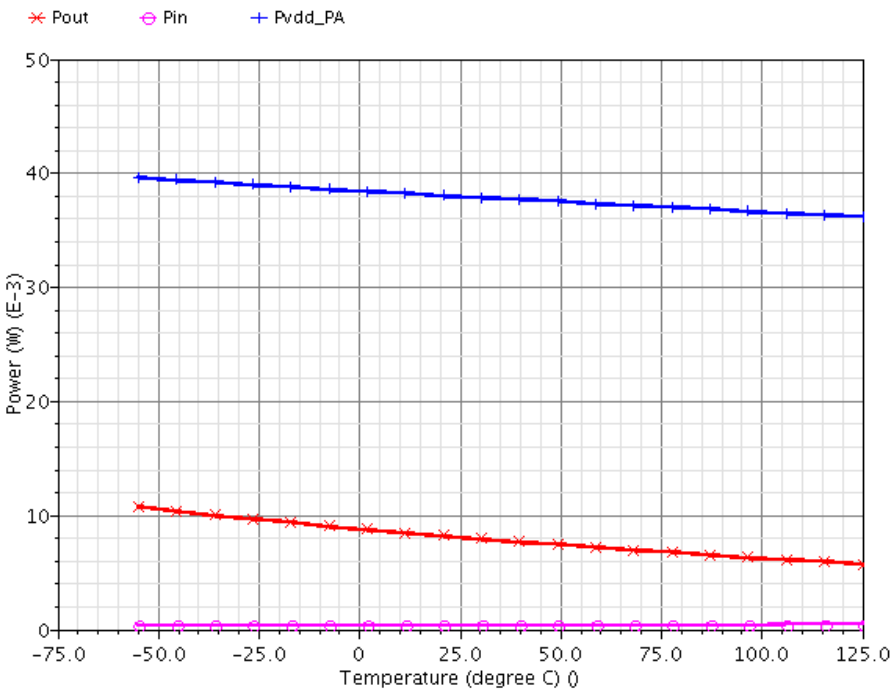

Figure 4.7. Temperature sweep versus P_{OUT}, P_{IN}, P_{SUPPLY}.

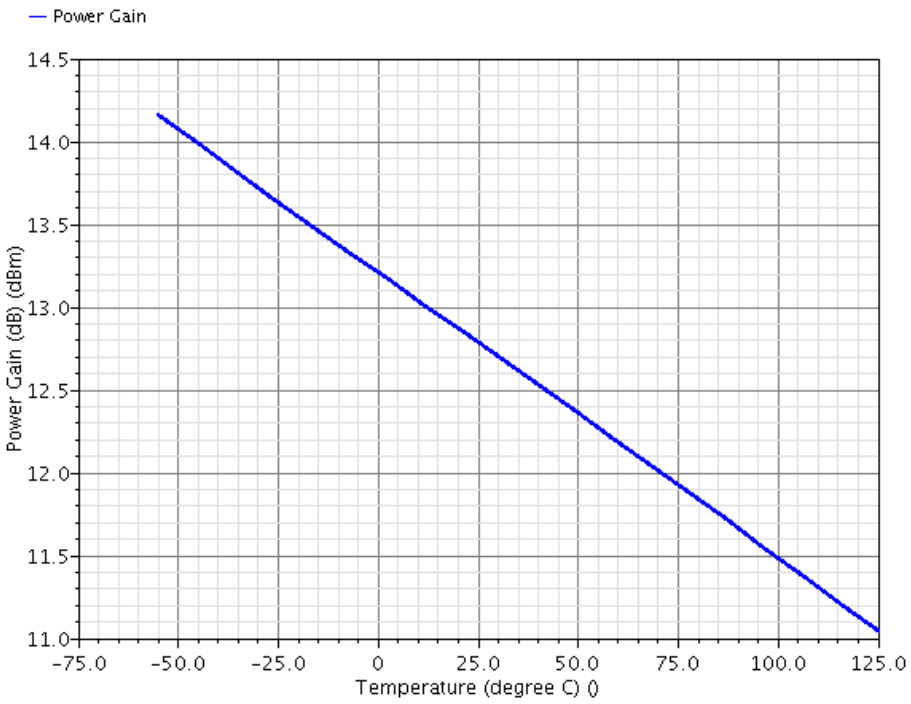

Figure 4.8. Temperature sweep versus power gain.

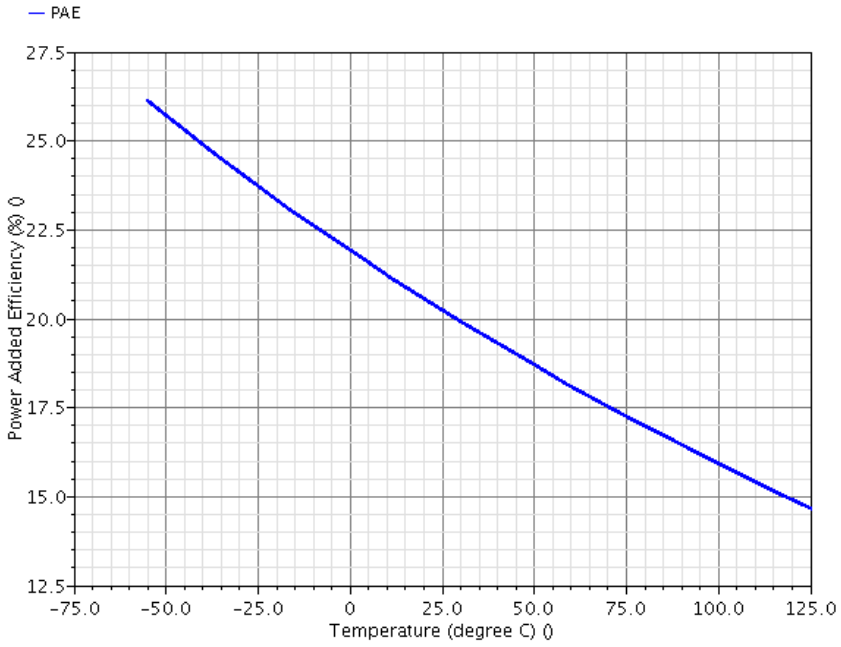

Figure 4.9. Temperature sweep versus PAE.

The simulated performance of the PA for different output power options is shown in Table 4.5. The table contains values from post-layout simulation and the theoretically expected

output power. It clearly shows that the values from post-layout simulation did not perform to the theoretical expectation. The simulations were performed at 25 °C and the power supply was 1.2 V. The frequency of the RF input signal was 433 MHz. The highest output power achieved in the simulations with 00 controlling word is not the desired 15 dBm (31.6 mW) but 9 dBm (7.9 mW). The 01 controlling word achieves an output power close to 3 dBm (2 mW). The 10 controlling word produces an output power that is a little lower than -3 dBm (0.5 mW). When 10 (Medium-Low) and 11 (Low) options are selected, the PA delivers an output power lower than the input power. This is due to the fact that the width of the switching transistor of the 10 and 11 options is not wide enough to draw sufficient current from the power supply to deliver needed power to the PA load. By increasing the width of the transistors for the 10 and 11 combinations, the desired output powers can be achieved correspondingly. Different output powers are achieved by using different widths of the switching transistors in the output stage. It was verified that increasing the transistor width produces a higher output power in the simulations before the chip tape-out. In the simulations right before the tape-out, each update from ideal to non-ideal cases will require increasing the layout size of switching transistors for 01, 10, and 11 power options. However, there was not enough time to make room in the layout for the three transistors right before the tape-out deadline.

Table 4.5. Simulated Results with Various Output Powers.

Controlling Word:	00	01	10	11	Unit
Input Power	0.431	0.428	0.426	0.426	mW
Output Power	7.916	1.775	0.366	0.138	mW
Power Supply Power	34.7	20.48	13.1	10.72	mW
PAE	21.57	6.58	N/A	N/A	%
Power Gain	12.79	6.17	N/A	N/A	dB
Expected Output Power	31.63	7.94	2.00	0.50	mW

Process variation simulations were also performed by using different process corner parameters such as SS (Slow NMOS-Slow PMOS), TT (normal), FF (Fast NMOS-FAST PMOS), FS (Fast NMOS-Slow PMOS), and modified FS (modified Fast NMOS-Slow PMOS) corners. It can be observed that the output power and the power added efficiency are higher in FF than SS corners. The modified FS is added to be able to simulate the PA performance more accurately. This is achieved by making the current and voltage characteristics of the simulated MOSFETs closer to that of the fabricated chips based on the MOSFET parameter data provided by MOSIS who fabricated the chip.

Table 4.6. Simulated Results with Corners.

Corners	SS	TT	FS	FF	Modified FS	Unit
Input Power	0.427	0.430	0.431	0.428	0.428	mW
Output Power	6.311	7.293	7.584	7.836	7.92	mW
Power Supply Power	29.42	32.52	33.52	34.39	34.7	mW
Power Gain	11.69	12.48	12.46	12.59	12.79	dB
Power Added Efficiency	20	21.1	21.34	21.54	21.57	%
S11	-5.69	-5.92	-5.97	-6.25	-6.064	dB
S21	6.78	7.16	7.33	7.58	7.55	dB
S12	-39.9	-40.36	-40.62	-40.65	-40.81	dB
S22	-26.11	-39.57	-32.62	-29.12	-27.87	dB
Input Impedance	38.28 -51.87j	38.2 -49.95j	38.25 -49.52j	38.10 -47.21j	38.22 -48.78j	Ω
Output Impedance	45.32 -0.42j	50.01 +1.19j	51.59 +1.70j	52.84 +2.10j	53.39 +2.204j	Ω

4.2.1 Other Simulations

The performance of the output power, the power added efficiency, and the power gain was simulated over frequency and input power sweep. The simulations are used to evaluate how the output power, the power added efficiency, and the power gain vary against the frequency and the input power sweep. The simulations over the frequency and the input power are plotted respectively in Figures 4.10-4.12 and Figures 4.13-4.15.

It can be observed that the output power and the power gain peak at around 400 MHz. The power added efficiency peaks at around 417 MHz which is a little off from 433 MHz. When plotted against the input power, it shows that the output power and the power added efficiency become saturated when the input power increases to a certain point. In Figure 4.15, it shows that the power gain becomes saturated when the input power is at around -20 dBm which is the 1dB compression point.

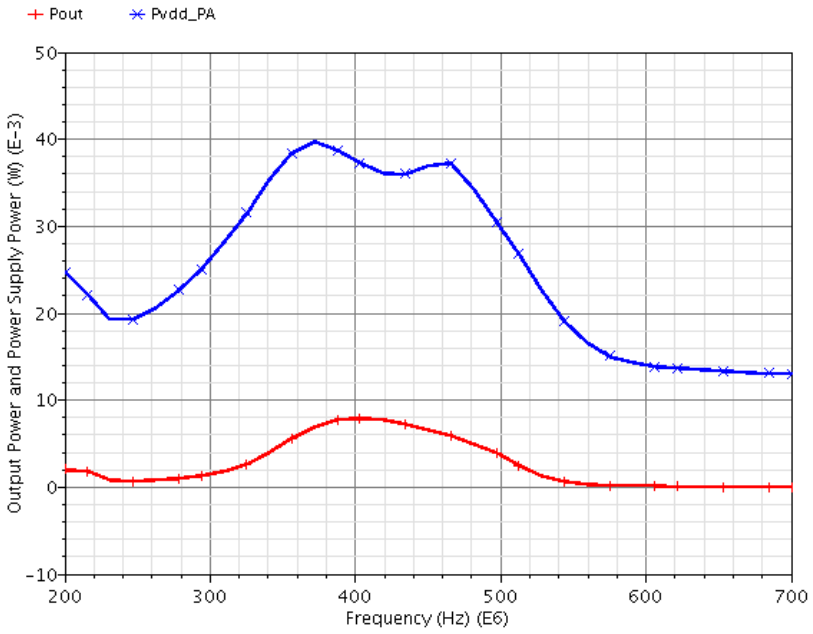

Figure 4.10. Output power and supply power consumption versus frequency.

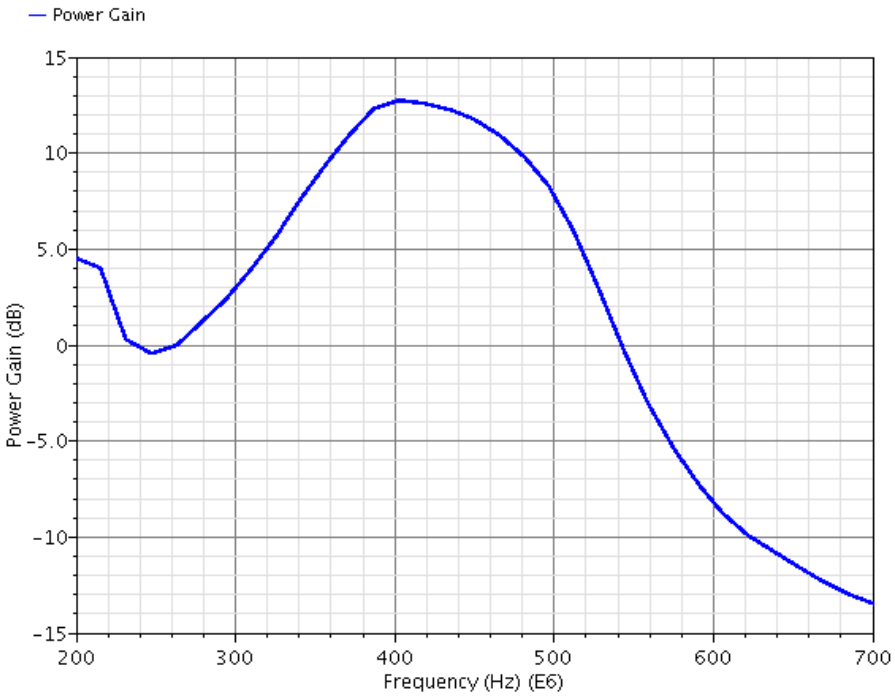

Figure 4.11. Power gain versus frequency.

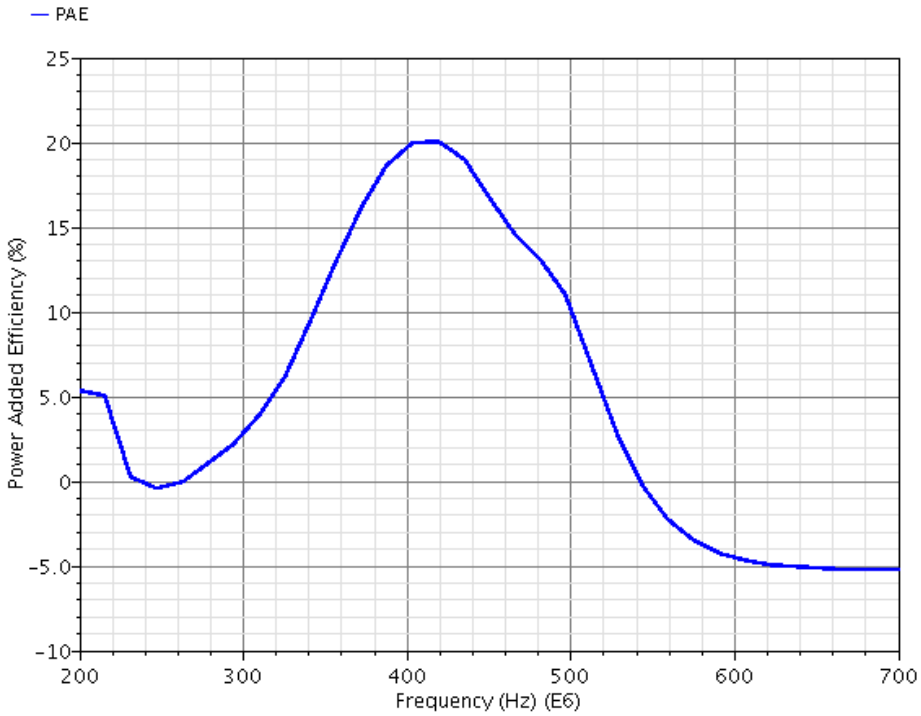

Figure 4.12. PAE versus frequency.

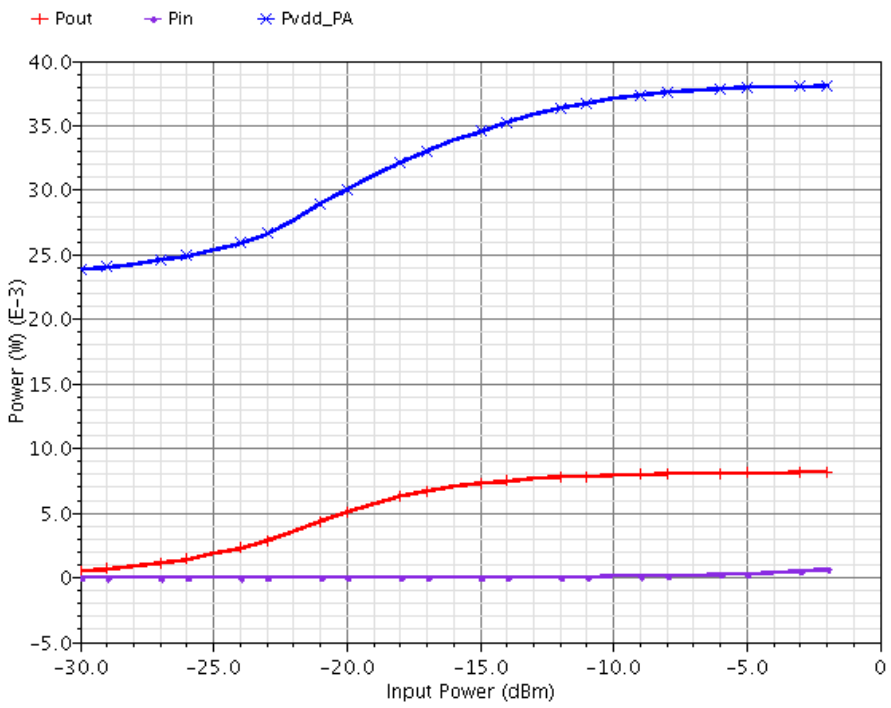

Figure 4.13. Output power and supply power consumption versus input power.

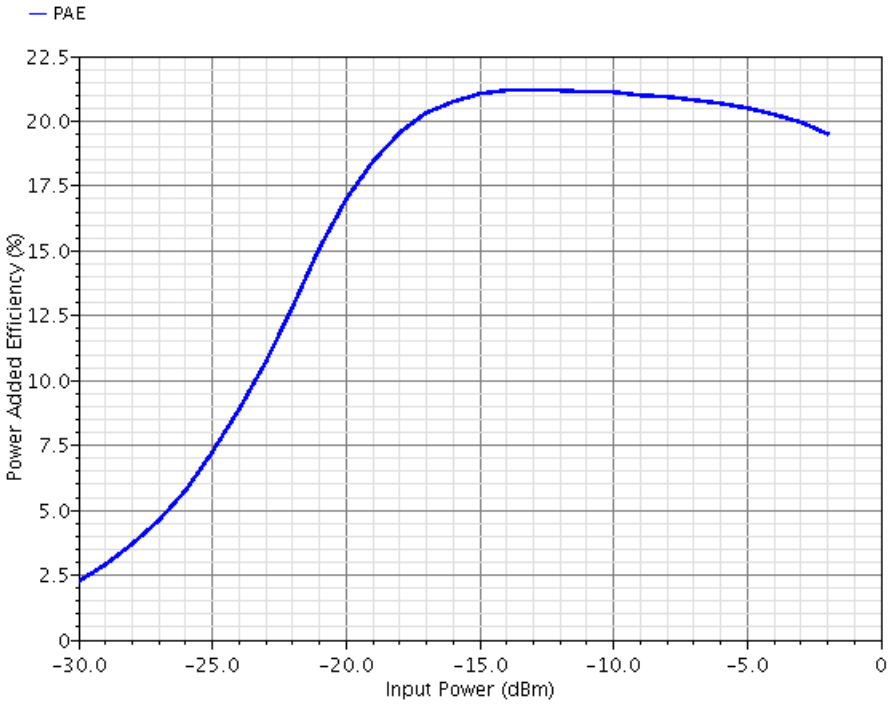

Figure 4.14. PAE versus input power.

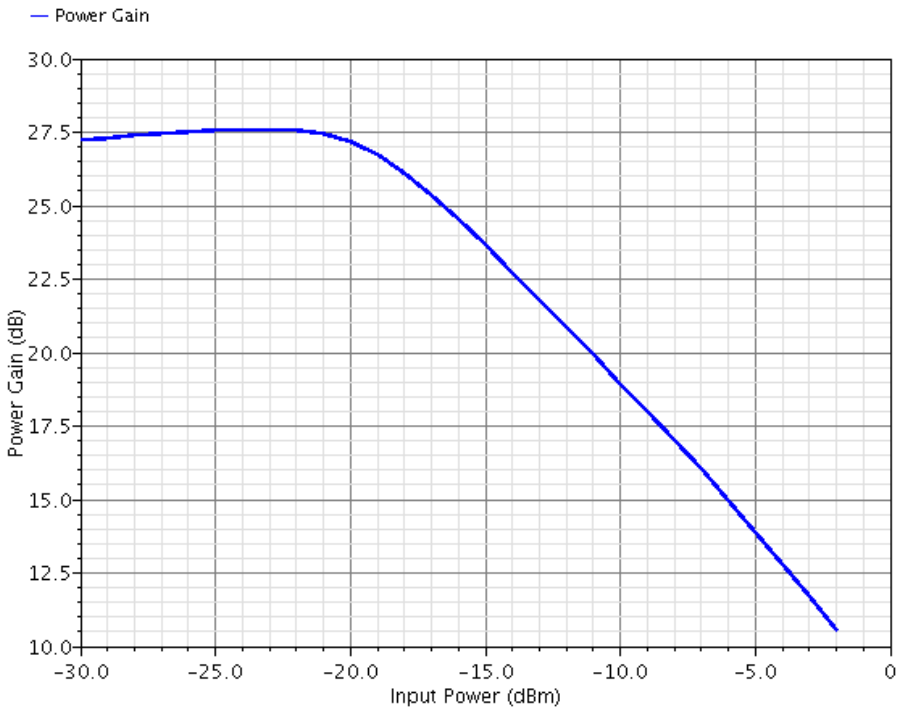

Figure 4.15. Power gain versus input power.

S-parameters were also simulated by running PSS and PSP analysis in Cadence's Spectre. The corresponding plots are shown in Figure 4.16. It can be observed that the lowest point of the S22 parameter is at 433 MHz which is the operating frequency of the PA, which means the output port of the PA has good impedance matching at 433 MHz. The simulated output impedance is 53.39+2.20j Ω which is close to 50 Ω. The lowest S11 is at around 410 MHz, which means the input impedance, 38.22-48.78j Ω, is off from 50 Ω**.**

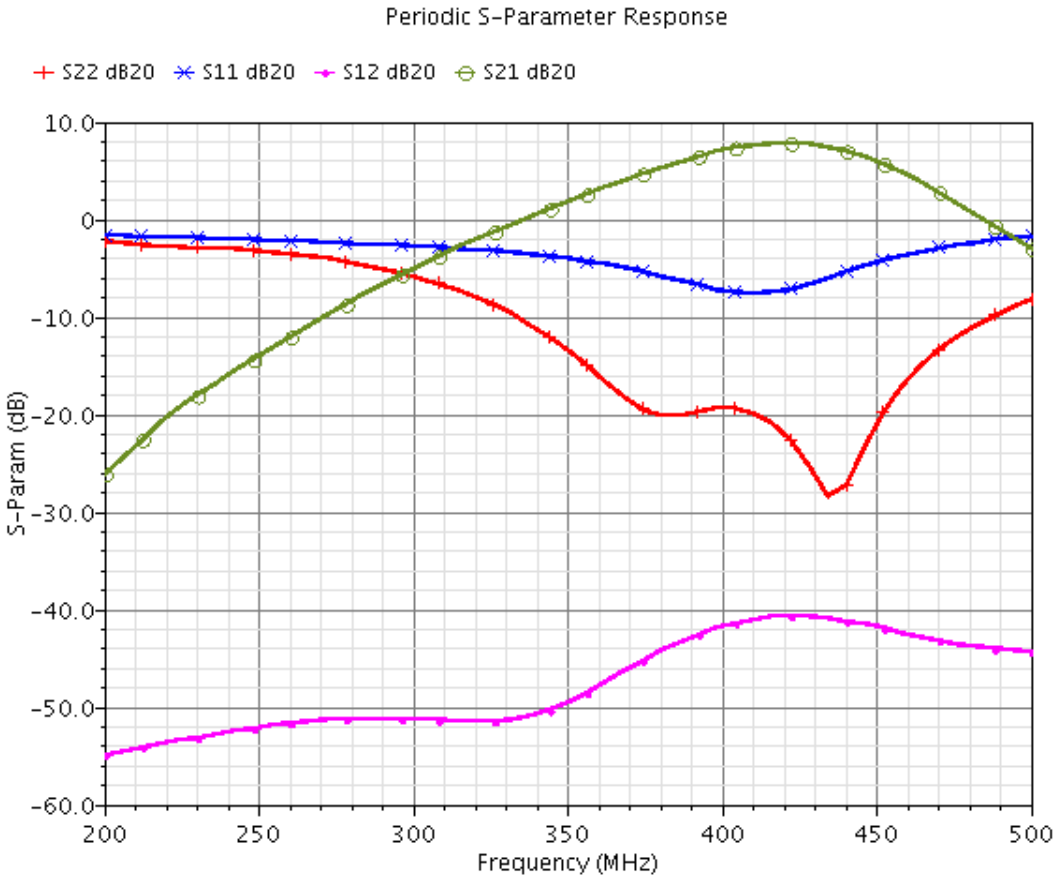

Figure 4.16. Simulated S-parameters of PA.

CHAPTER 5

Physical Design

5.1 Layout Introduction

When all the necessary simulations were performed, geometry design or layout is the next step. The RF class E power amplifier was laid out in Cadence Virtuoso Layout Editor 6.1. In Figure 5.1, the layout includes four major blocks which are the driver stage, the output stage, 2-to-4 decoder, and analog controlling circuit.

5.2 Layout Consideration

Because the class E power amplifier design includes digital, analog, and RF circuitry, it requires sufficient careful consideration in the chip layout shown blow.

1. RF runners, or traces, are placed perpendicular to biasing runners.
2. All on-chip inductors have guard rings around them.
3. All RF runners in parallel have a gap of at least three times the trace width (the wider one) between them to avoid cross talk.
4. All RF input and output terminals use GND-signal-GND pattern.
5. Because the top two metal layers, MA and E1 have much less resistance per unit length than other metal layers, the two layers are used for longer runners to reduce the voltage drop along the runners.
6. All inductors have their own patterned ground planes to avoid a current loop.
7. The RF runners should be as short as possible. Dramatic turn of the RF runners should be avoided as well.
8. All active components in the circuit are to be placed in a symmetrical pattern so that the current flowing through the transistors can be balanced.

9. A fair amount of vias should be used to allow as low a contact resistance as possible.
10. The width of the runners used is wider than the minimum width calculated according to the simulated current flowing through it to reduce the voltage drop.
11. All the components on the chip are arranged and placed as compactly as possible to save chip space.

5.3 Layout Diagram

Figure 5.1 shows the PA layout including the pads. All major function blocks are labeled in the layout including the input stage, the output stage, the analog controlling circuit, and the 2-to-4 decoder. The dimension of the layout with the pads is 1290 μm × 1495 μm.

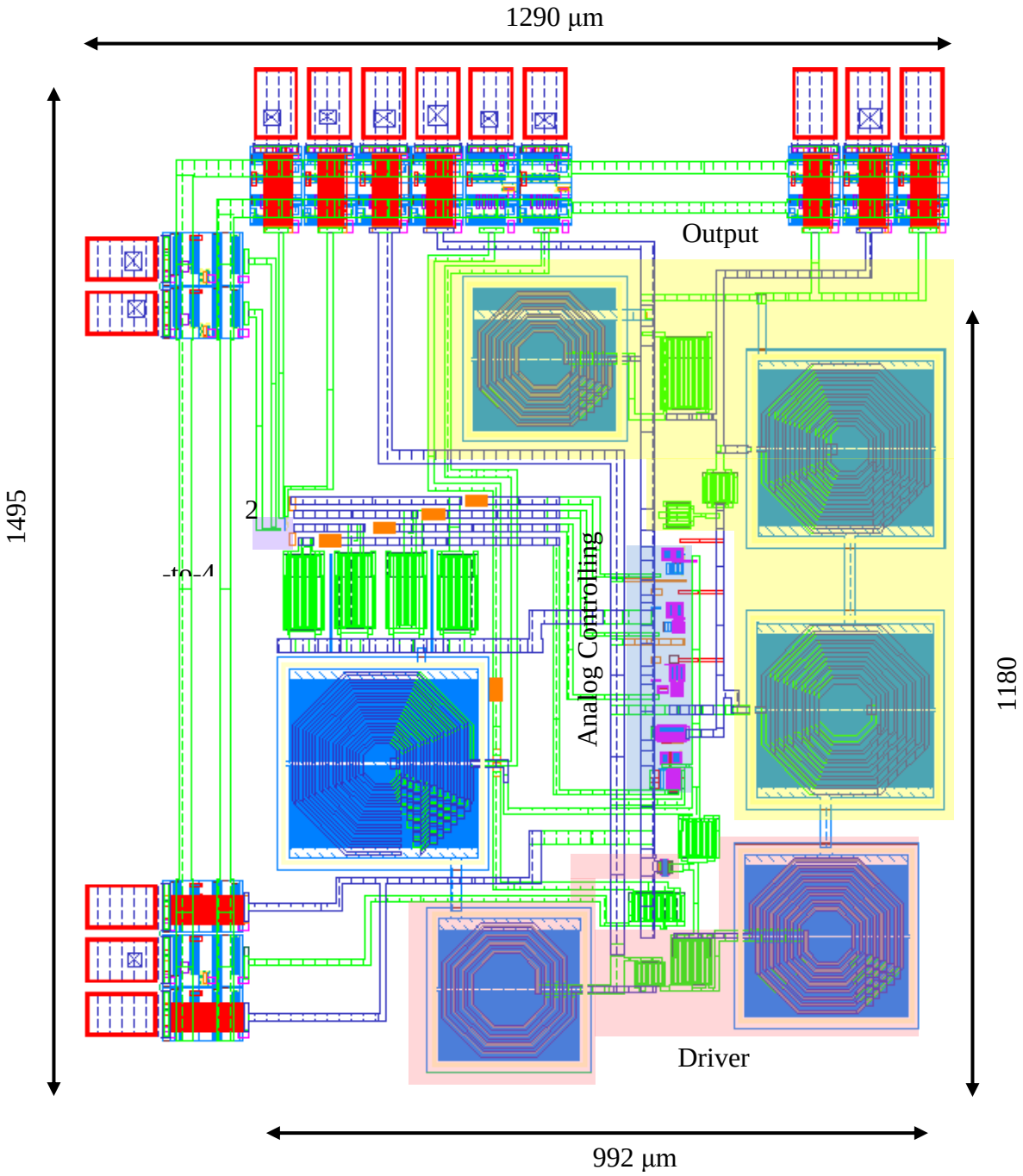

Figure 5.1. The RF class E power amplifier layout.

Figure 5.2 shows the layout diagram for the whole die. Besides the RF class E power amplifier, a VGA, a VCO, a mixer, an LNA, and some other integrated digital circuitry are included on the same die. The power amplifier is labeled in the diagram.

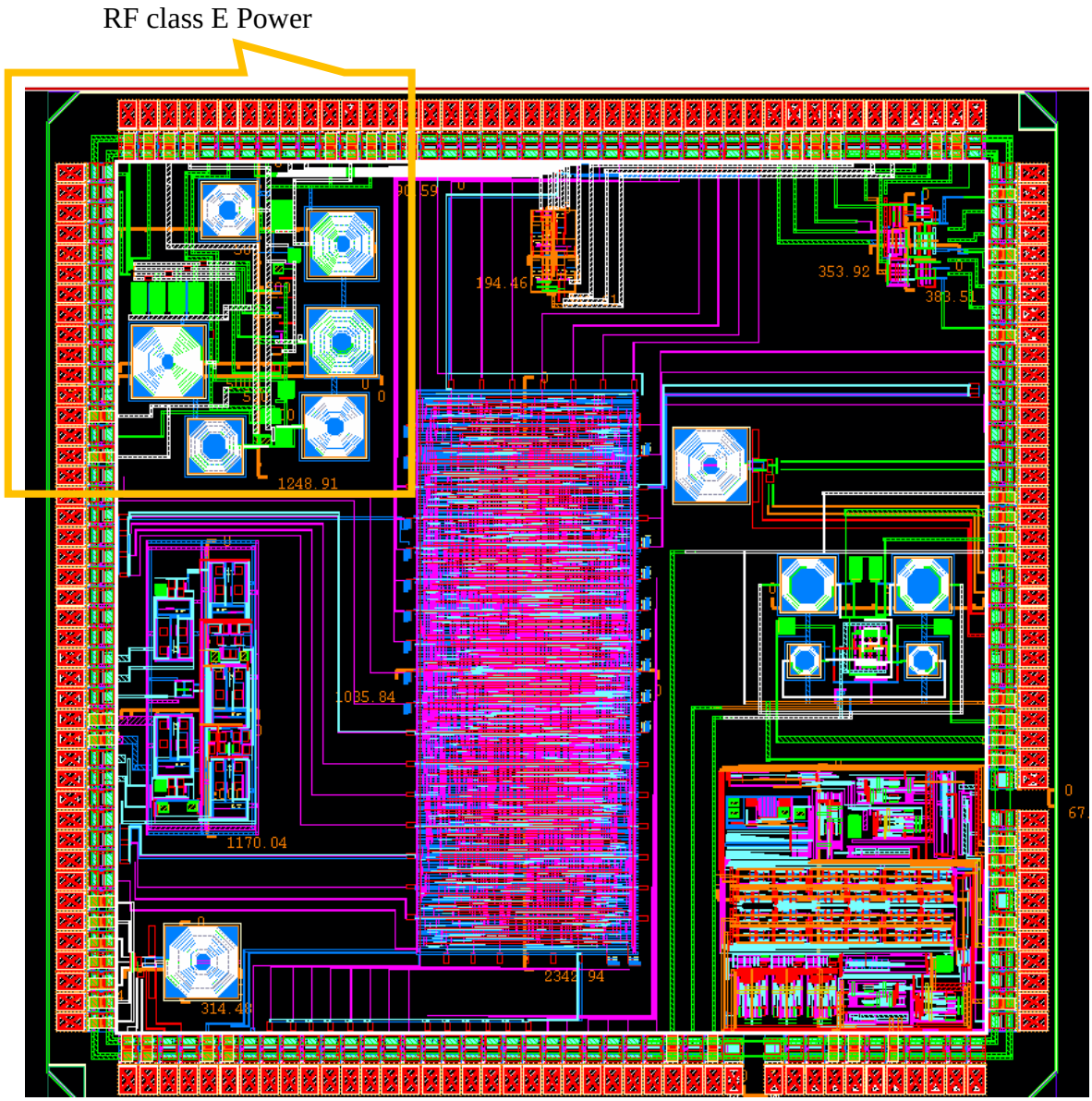

Figure 5.2. Layout of the entire chip.

CHAPTER 6

Power Amplifier Testing

The purpose of this chapter is to present the test setup and measured results of the implemented class E power amplifier. A test PCB was designed and used to test the PA. By comparing the measured with simulated results, the performance of the PA can be evaluated to see how well the PA is designed and functions in reality.

6.1 Packaging

The power amplifier design presented in this thesis was bonded and packaged at MOSIS which is a low-cost prototyping and small-volume production service for VLSI circuit development. As shown in Figure 6.1, a QFN48 package in 7 mm × 7 mm dimension was chosen for the die due to the main concern of reducing parasitic components. The advantages of using the QFN package include reduced lead inductance and parasitics, good thermal performance by using a thermal pad right underneath the die, a smaller sized footprint near chip scale, and lower weight. The bonding diagram is shown in Figure 6.2. The pin-out connections are listed in Table 6.1.

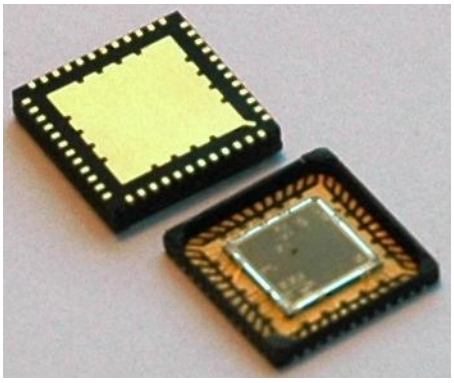

Figure 6.1. Packaging and bonding.

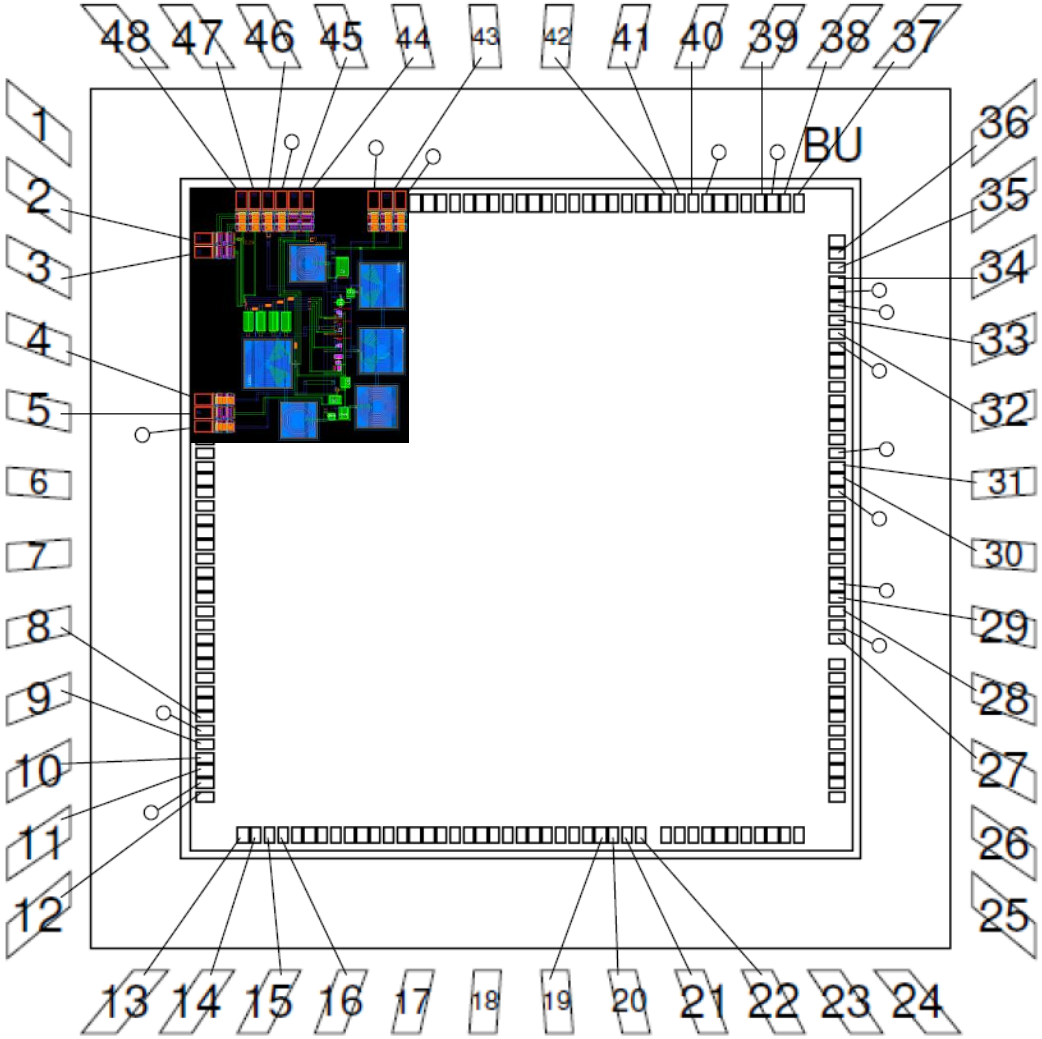

Figure 6.2. Bonding diagram.

Table 6.1. Pin Assignments

Pin#	Pin Name	Connection
2	S0	DC input voltage connected to either ground or V_{DD} of 1.2V
3	S1	DC input voltage connected to either ground or V_{DD} of 1.2V
4	GND	Analog/RF ground
5	IN_RF	RF input signal at 433MHz
43	OUT_RF	RF output signal at 433MHz
44	VBIAS2	DC biasing voltage at 0.56V generated by power supply
45	VBIAS1	DC biasing voltage at 0.56V generated by power supply
46	VDD_PA	Analog/RF power supply of 1.2V
47	VDD_DIGI	Digital power supply of 1.2V
48	GND_DIGI	Digital ground

6.2 Test PCB Introduction

The actual PCB is a custom made FR4 board with four layers. The four layers from top to bottom are: the top layer for routing, the second layer for a ground plane, the third layer for a power plane, and bottom layer is used for some routing and a small ground plane. All resistors, capacitors, and inductors on the PCB are surface mounted components. The through-hole components are potentiometers, test points, SMA female connectors, and banana jacks. The test PCB was designed in EagleCAD software.

6.3 PCB Design Consideration

The board design is more complicated than it looks. Special attention to careful PCB design is necessary when it is an RF circuit and test equipment also needs to be taken into consideration. When it comes to testing the PA in a temperature chamber for wide temperature range measurement, it is required that all the DC biasing, power supply, and input/output terminals should be equipped with SMA female connectors. This is because the only available internal connections in the chamber are SMA. To be able to have access to the test equipment outside the chamber, the SMA connections are necessary.

When measuring the supply power consumption, the average current measurement in the power supply trace becomes necessary. A 0.1 ohm resistor was placed in series in the power supply trace to measure voltage drop across the resistor. Therefore, the average current can be calculated by using Ohm’s law and the average supply power consumption is derived as a product of the current and the voltage. On the PCB, there is a test point and an SMA female connector soldered at each end of the resistor for the voltage drop measurement by using a multi-meter.

Some other factors should also be considered.

1. Multiple decoupling capacitors are placed near the biasing pins of the chip to stabilize the biasing voltage and block noise coming from the chip.
2. The runner turning is 45 degrees.
3. The widths of routes used on the PCB are 10 mils, 24 mils, and 32 mils. The route width of 10 mil is used for connection to the QFN pins because the QFN pins are small and very close to each other. The majority of the biasing routes are 32 mils wide. The 24-mil width is used to connect routes of 10 mils and 32 mils. 28.874-mil width is used only as the calculated width of the microstrip line.
4. Different components on the PCB were managed in a balanced layout manner.
5. Each banana jack mounting point has to be placed far enough from its SMA connector on the PCB so that there is enough room to mount the SMA connector and the banana jack connector.
6. Regarding the footprint size of all passive surface mount components, the smallest size is 0603 because any size smaller than 0603 is too tiny to solder by hand.
7. All the biasing routes are placed perpendicular to all RF signal routes on the PCB to avoid interference.
8. All the RF signal routes should be as short and straight as possible.

6.4 Microstrip

A microstrip line is one type of transmission line designed for conducting RF or microwave signals. It is fabricated as a top-layer conducting strip with certain width on a multiple-layer PCB and separated from a ground plane right underneath it by a dielectric layer or substrate. The characteristic impedance of the microstrip line, 50 Ω in this design, is essential and should be matched to the termination of the input and output terminals of the power

amplifier. Otherwise, signal reflection will occur in the signal path of this two-port network and maximum possible output power would not be achieved and delivered at the output of the PA due to the discrepancy in the impedance of RF signal trace.

The width of the microstrip line can be calculated using the dielectric constant of the board material, the substrate thickness, operating frequency, and the characteristic impedance of the stripline. A 4-layer PCB is preferred instead of a 2-layer one based on the consideration of using the microstripe line. This is because the width of the microstrip line on the 2-layer board could be too wide to be used in this test PCB design, which is not practical. The advantage of using a 4-layer board is that the substrate thickness of the 4-layer board is thinner than the basic 2-layer one, so that a reasonable and thinner width of the microstrip can be employed. There are thinner two layer boards available but it costs more. Here are the specification values for the 4-layer test PCB design.

Table 6.2. Spec Values for PCB Design.

Specs	Value
Dielectric constant	4.5
Substrate thickness	14.96 mils
Operating Frequency	433 MHz
Characteristic impedance	50 Ω

The width of the microstrip can be calculated by using a microstrip online calculator or Equations (6.1-6.2) listed below [15].

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left[1 + 12\left(\frac{H}{W}\right)\right]^{-\frac{1}{2}} \quad \textbf{(6.1)}$$

$$Z_0 = \frac{\frac{120\pi}{\sqrt{\varepsilon_{eff}}}}{\frac{W}{H}+1.393+0.667\ln\left(\frac{W}{H}+1.444\right)} \quad \textbf{(6.2)}$$

6.5 Off-chip Matching Network

The input and output matching networks are fabricated off chip instead of on chip due to several factors. One important factor is the chip space. An impedance transformation network includes inductors and capacitors which are space consuming components when integrated on a single chip. By moving the matching network off chip, much chip space is saved and cost of fabrication decreases dramatically since the cost is proportional to the chip area. The second reason for moving the matching networks off chip is that they can be modified later on the PCB if any change needs to be made to the network in the future. Say, the simulated impedance including the matching network may not match the actual measured impedance. Then it is still possible to change and retune the input and output impedance matching network off chip by using correct values of inductors and capacitors. If the matching network was on chip, then there would be no way to change it conveniently.

The input/output impedance matching networks used in this design are L matching networks. Depending on transferring impedance from low to high or from high to low, the following matching networks are used in the design. The value of each L and C can be calculated by using a free online tool [16] where the L and C values are automatically calculated when impedance at each end of the network is provided. The process of calculation the online tool uses is to make the impedance of B be a complex conjugate match to the impedance of A with the matching network.

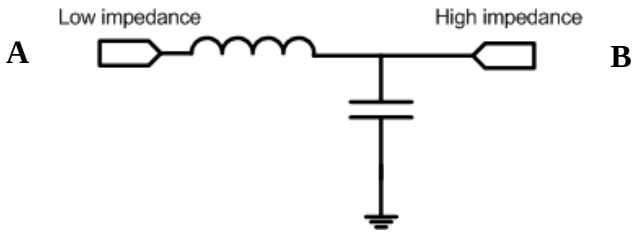

Figure 6.3. Output impedance L matching network.

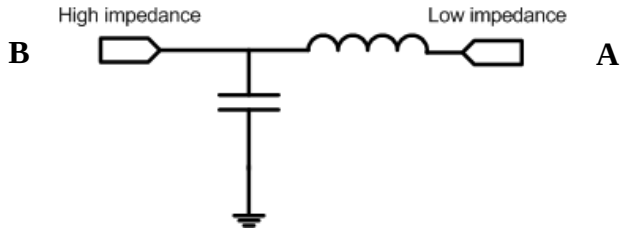

Figure 6.4. Input impedance L matching network.

Table 6.3. Component Values of Input/Output Impedance Matching Network.

Impedance matching network	L	C
Input	78nH	8pF
Output	6.2nH	5.6pF

6.6 Test PCB Design Schematic

The schematic of the test PCB is shown in Figure 6.5. Voltage regulators, TPS71701 and LT3021, are used in the test PCB circuitry to regulate the supply voltage and biasing voltage applied to the chip. Resistors of value 0.1 Ω are placed in each supply and biasing trace to measure current for power consumption measurements.

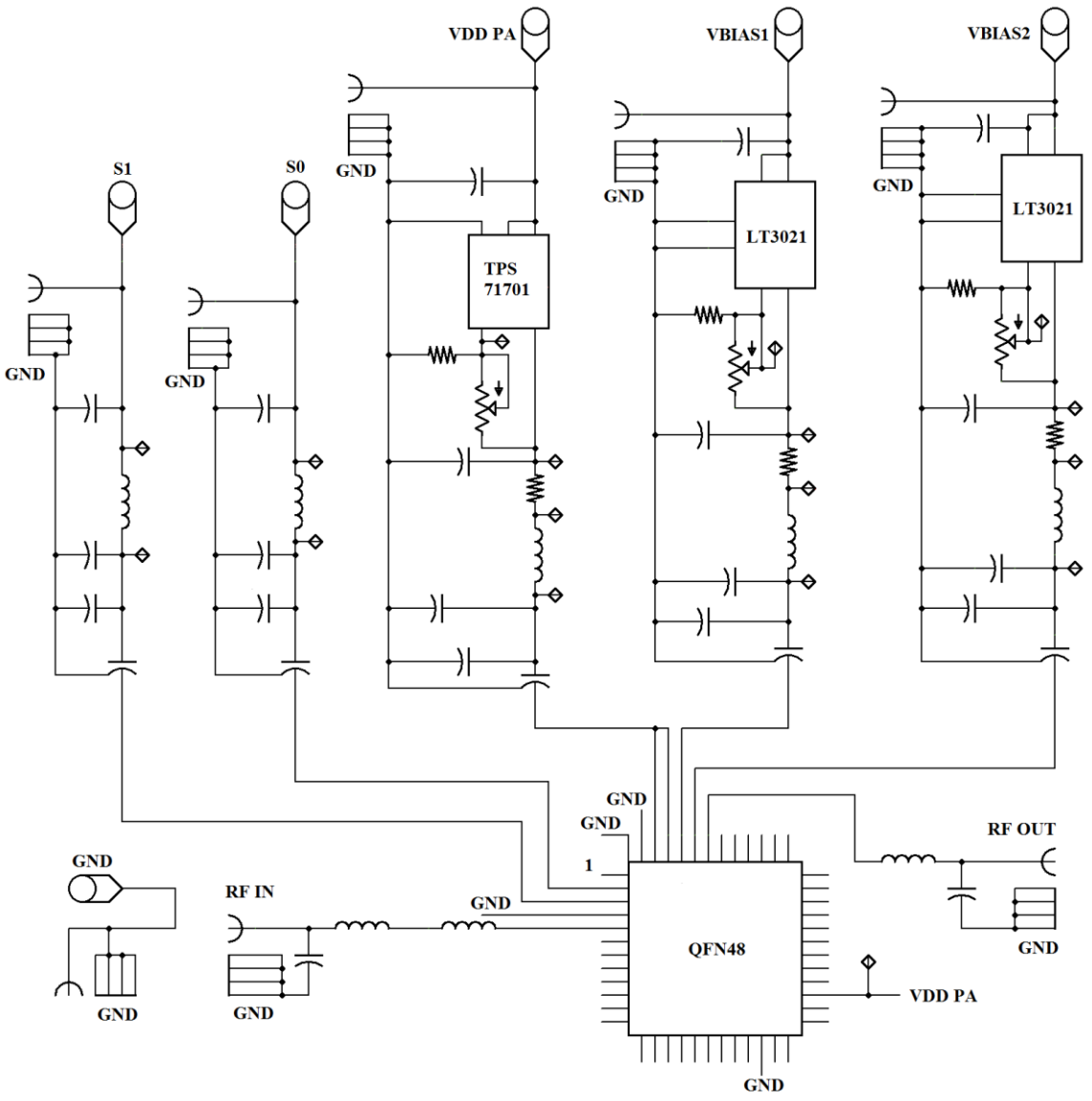

Figure 6.5. PCB schematic diagram.

6.7 Test PCB Layout

The test PCB layout is shown in Figure 6.6. The traces in red are the top layer traces. The blue ones are the traces on the bottom layer. Both the schematic and layout were designed in EagleCAD. The widest trace width, 32 mils, is used in supply and basing traces. The thinnest, 10 mils, is used for connection to the QFN package pads. The width of RF traces is calculated according the Equations (6.1-6.2).

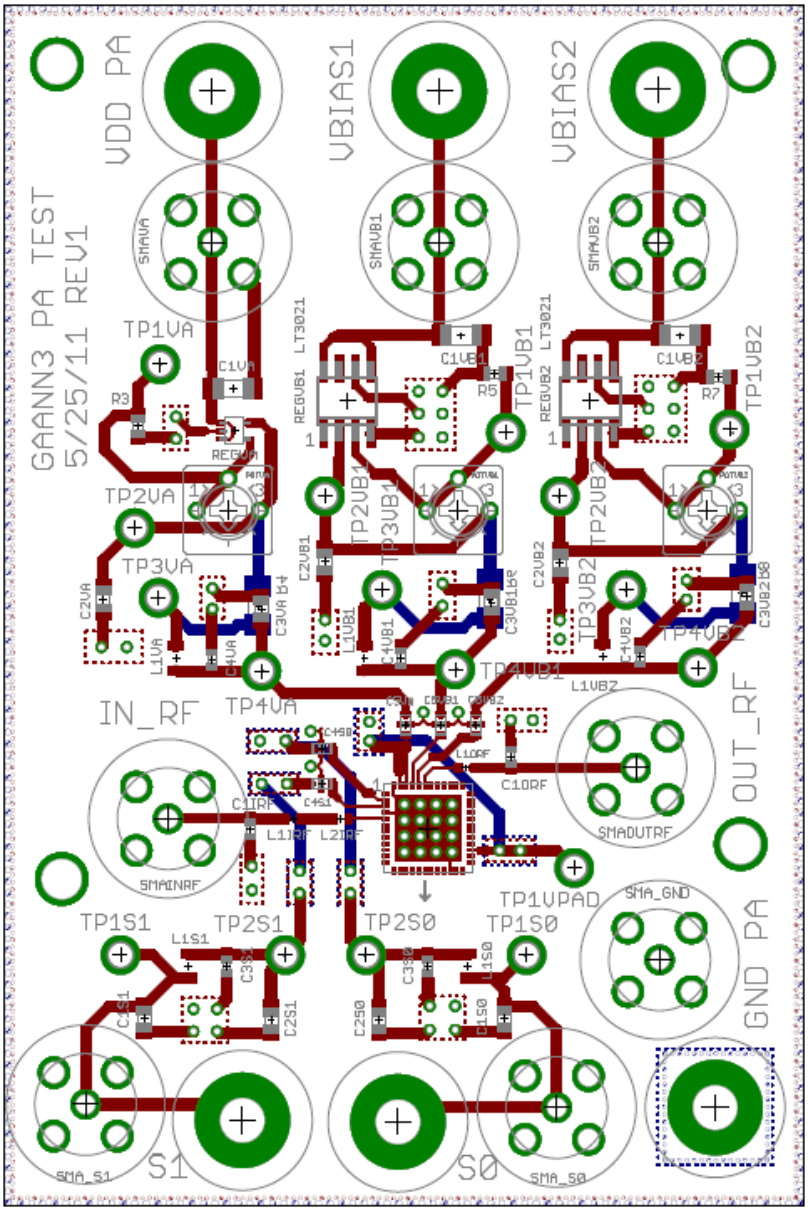

Figure 6.6. PCB layout.

6.8 Test PCB Photo

After the test PCB layout design was done, it was sent to PCB-Pool, a PCB service provider, to be fabricated. The actual fabricated test PCB is shown in Figure 6.7. All the surface mount components were reflowed. All the ports are labeled in the picture according to their functions.

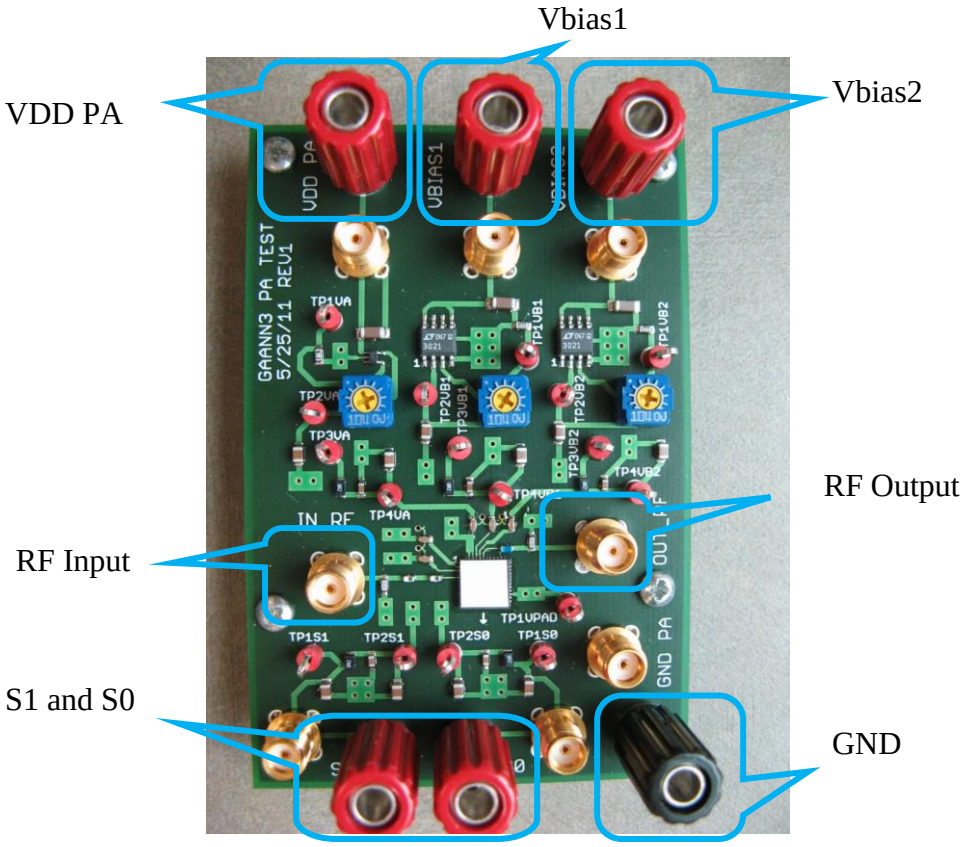

Figure 6.7. Assembled test PCB for the chip.

6.9 Test PCB Connection

The Table 6.4 lists all the components assembled on the test PCB with component values, quantities, type, and the layer on which the component was assembled. Table 6.5 shows how the PCB is connected to the testing equipment through input/output ports, biasing voltage ports and power supply port.

Table 6.4. Components on the PCB

Part Name	Values	Qty	Type	Layer
Banana plug	-	6	Through-hole	Top
Test points	-	17	Through-hole	Top
SMA connector	-	8	Through-hole	Top
Potentiometer	10Ω-2MΩ	3	Through-hole	Top
QFN package	-	1	Surface mount	Top
Voltage Regulator	.2-9.5V	2	Surface mount	Top
	.9-6.2V	1	Surface mount	Top
Capacitor	8pF	1	Surface mount	Top
	5.6pF	1	Surface mount	Top

	6.8uF	3	Surface mount	Top
	470nF	5	Surface mount	Top
	22nF	5	Surface mount	Top
	4.7uF	10	Surface mount	Top
Inductor	39nH	2	Surface mount	Top
	6.2nH	1	Surface mount	Top
	8.2nH	5	Surface mount	Top
Resistor	160kΩ	1	Surface mount	Top
	22kΩ	2	Surface mount	Top
	0.1Ω	3	Surface mount	Bottom

Table 6.5. Connection on PCB.

Connector Name	Connector Type	Connection	Voltage on the chip
VDD PA	SMA/Banana jack	Power supply 2.8 V	1.2 V
VBIAS1	SMA/Banana jack	Power supply 0.86 V	0.58 V
VBIAS2	SMA/Banana jack	Power supply 0.86 V	0.58 V
IN_RF	SMA/Banana jack	RF input signal from the function generator	N/A
OUT_RF	SMA/Banana jack	RF output signal to spectrum analyzer, oscilloscope, or network analyzer	N/A

6.10 Test Bench Setup for Test PCB

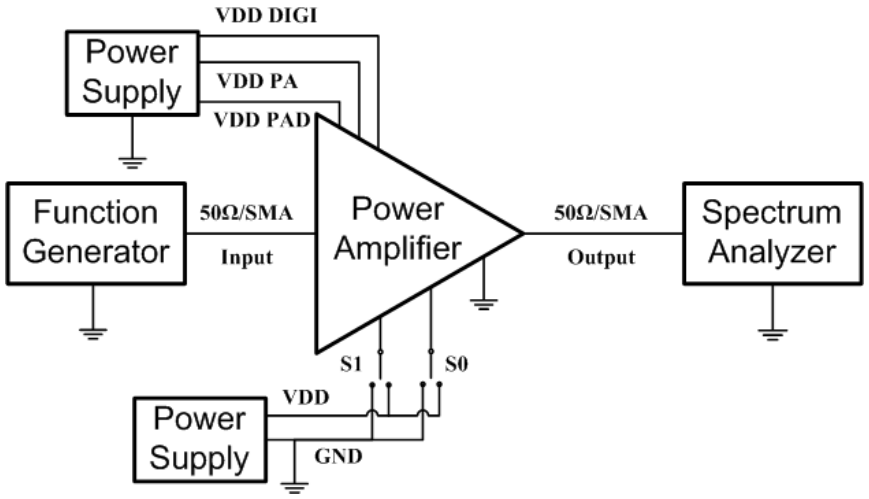

Figure 6.8. The test bench using the spectrum analyzer.

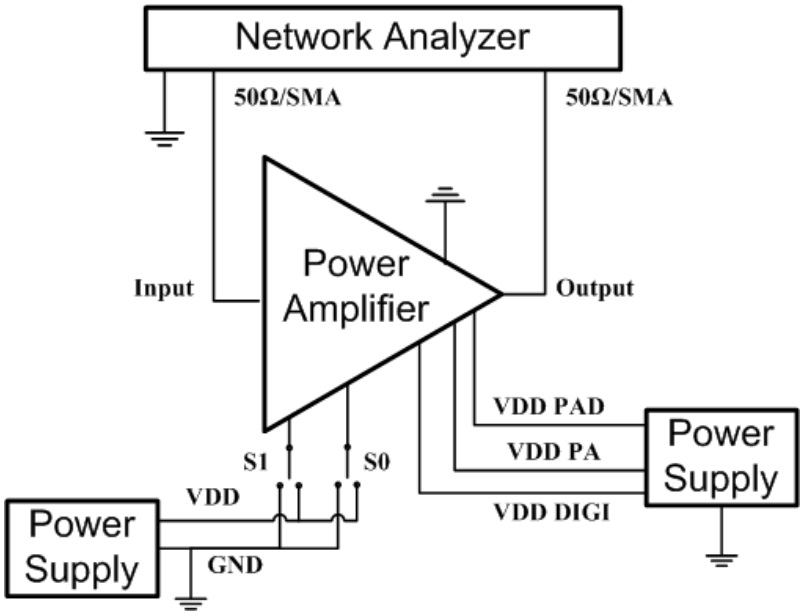

Figure 6.9. The test bench using the network analyzer.

The two different test benches are shown in Figures 6.8 and 6.9 with different testing purposes. The setup in the Figure 6.8 is used for measurement of the input power, the output power, the supply power consumption, the power gain, the PAE, the 1-dB compression point, and the 3-dB frequency bandwidth. The setup in Figure 6.9 is used for measurement of the S-parameters, the input impedance, and the output impedance. In Figure 6.10, the setup for Figure 6.8 is shown and the test PCB was connected to a power supply, function generator, and spectrum analyzer. The actual voltage applied to the VDD PA banana jack is 2.8 V and then is regulated to 1.2 V, the supply voltage of the PA, by the voltage regulators. The actual voltage applied to the Vbias1 and Vbias2 is 0.86 V and then is regulated to 0.58 V, the biasing voltage for Vbias1 and Vbias2.

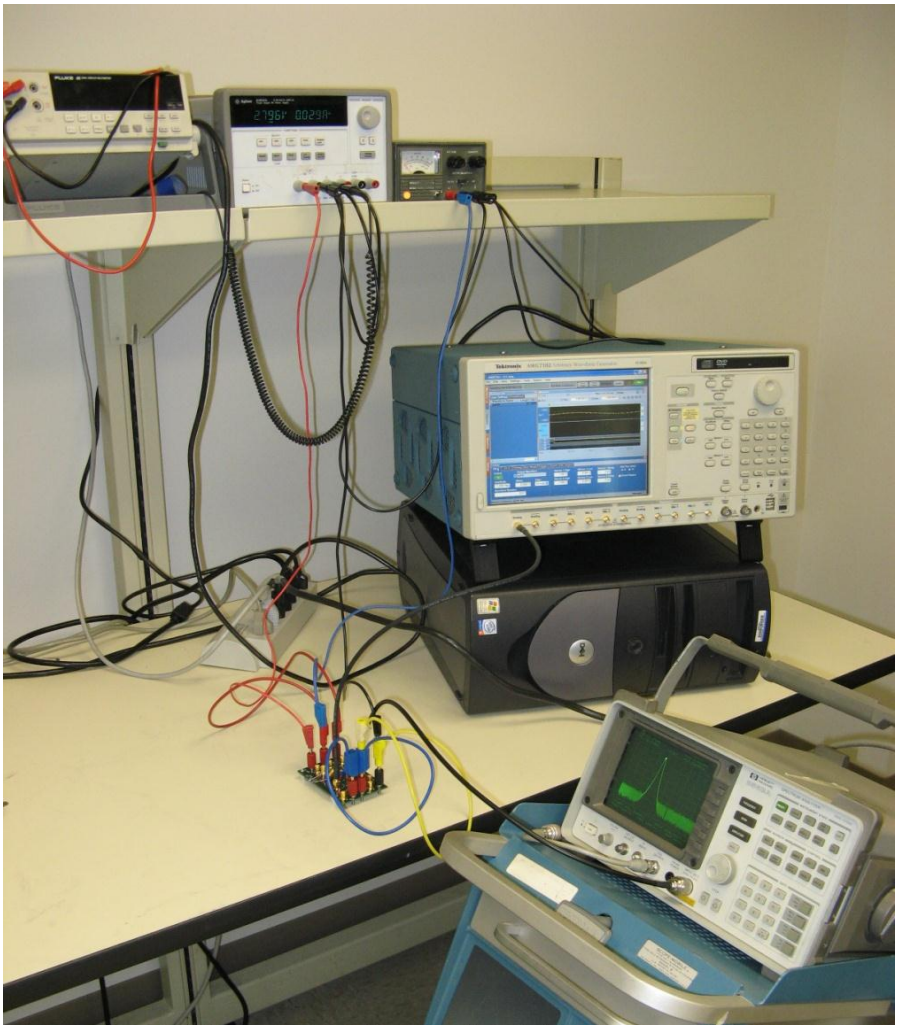

Figure 6.10. Test bench setup using spectrum analyzer.

6.11 Test Equipment

All the test equipment is listed in Table 6.6.

Table 6.6. Test Equipment.

Equipment Name	Model Number
Mixed signal oscilloscope	Tektronix MSO 4104
Function generator	Tektronix AWG7102
2 DC power supplies	Agilent E3631A, HP 6216A
Mixed signal spectrum analyzer	HP 8563A
Network analyzer	Agilent E8361A
Multi-meter	FLUKE 45
SMA cables	N/A
Thermal chamber	N/A

Test PC board	N/A
Banana wires	N/A

6.12 Measured Results and Charts

The measured results are listed in Table 6.7 and compared to the simulated results. Regarding the output power and PAE, there is a wide discrepancy between the simulated and the measured results. The analysis of the discrepancy will be explained in section 6.13 of Chapter 6. Calculated from the measured S-parameters, the input and the output impedance are off from the simulated results. However, the measured 3-dB bandwidth is wider than the simulated. The 1-dB compression point is also about the same for both results. Among the four S-parameters, the measured S12 is lower than the simulated S12, which is desirable.

The measured and the simulated PAE, the output power, and the power gain are plotted against frequency and shown in Figures 6.11-6.13. The three metrics are also plotted against the input power sweep in Figures 6.14-6.16.

Table 6.7. Measurement for the Power Amplifier

Parameter		Simulation	Measurement	Unit
F	Frequency	433	433	MHz
G	Power gain	12.79	8.33	dB
BW	3-dB bandwidth	128.35	200	MHz
P1dB	1-dB compression point	-19.91	-20	dBm
S_{11}	Input return loss	-6.063	-2.76	dB
S_{12}	Reverse isolation	-40.807	-57.33	
S_{21}	Forward Power gain	7.549	8.8	
S_{22}	Output return loss	-27.869	-15.82	
P_{OUT}	RF output power	7.916	2.71	mW
P_{IN}	RF input power	0.431	0.40	
P_{SUPPLY}	Power supply power	34.70	32.88	
PAE	Power added efficiency	21.57	7.03	%
Z_{IN}	Input impedance	38.217-48.78j	11.6-33.8j	Ω
Z_{OUT}	Output impedance	53.39+2.20j	42.6-13.3j	Ω

In Figures 6.11-6.13, it can be seen that the PAE, the output power, and the power gain all peak at a frequency that is a little lower than 433 MHz in both simulation and measurement. The simulated PAE peaks at 417 MHz and the measured PAE peaks at 420 MHz. The simulated output power peaks at 405 MHz and the measured output power peaks at 400 MHz. The simulated power gain peaks at 405 MHz and the measured power gain peaks at 400 MHz. So all the frequency peak values are lower in measurement but are at close to 433 MHz. Some slight tuning to the circuit would have been helpful in shifting the peak values a little closer to the 433 MHz, and the simulation results seem to be a good predictor for this.

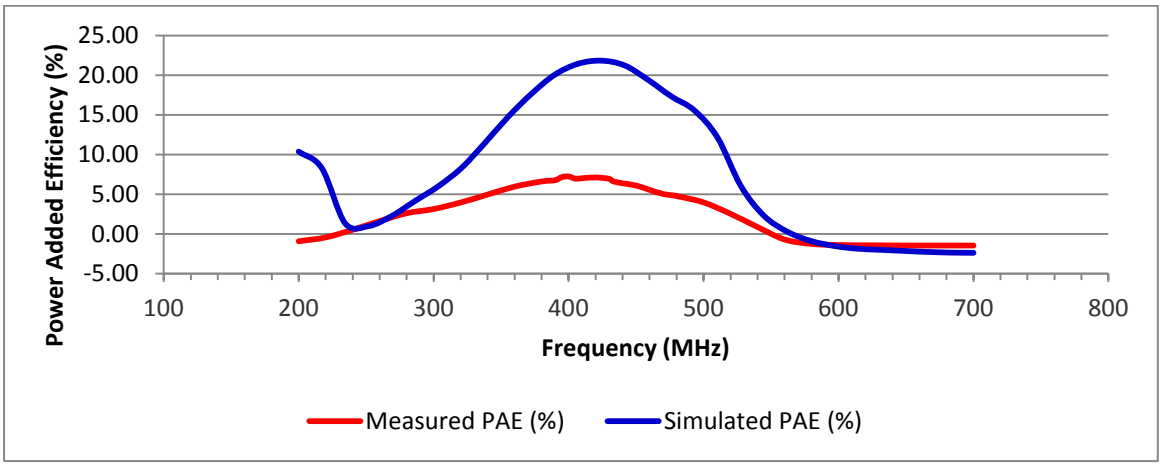

Figure 6.11. Measured and simulated power added efficiency versus frequency.

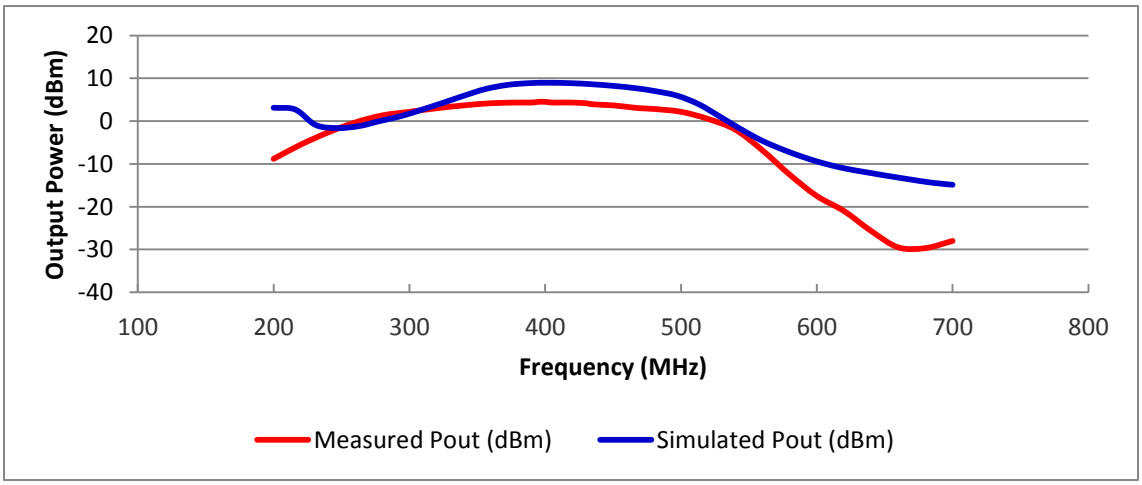

Figure 6.12. Measured and simulated output power versus frequency.

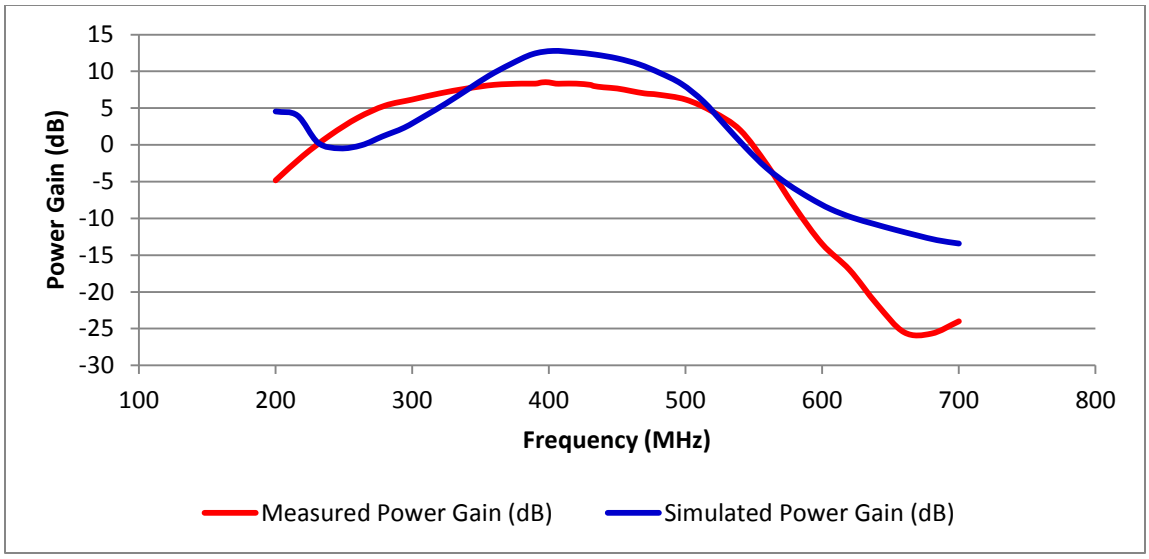

Figure 6.13. Measured and simulated power gain versus frequency.

In Figures 6.14-6.16, it is noticeable that both simulated and measured PAE and output power become saturated starting at around -20 dBm, which is the 1-dB compression point. Both the measured and the simulated plots have a similar shape of curves and show the same trend but the measured values are lower than the simulated values.

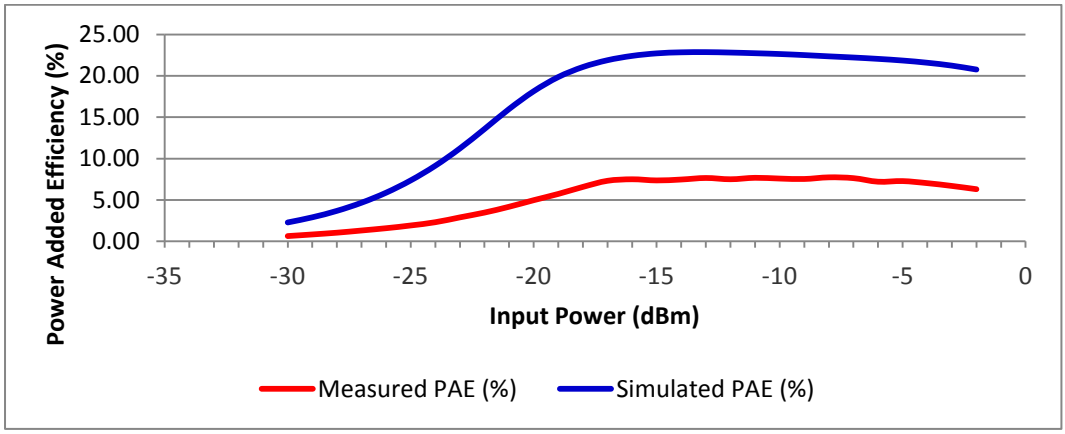

Figure 6.14. Measured and simulated power added efficiency versus input power.

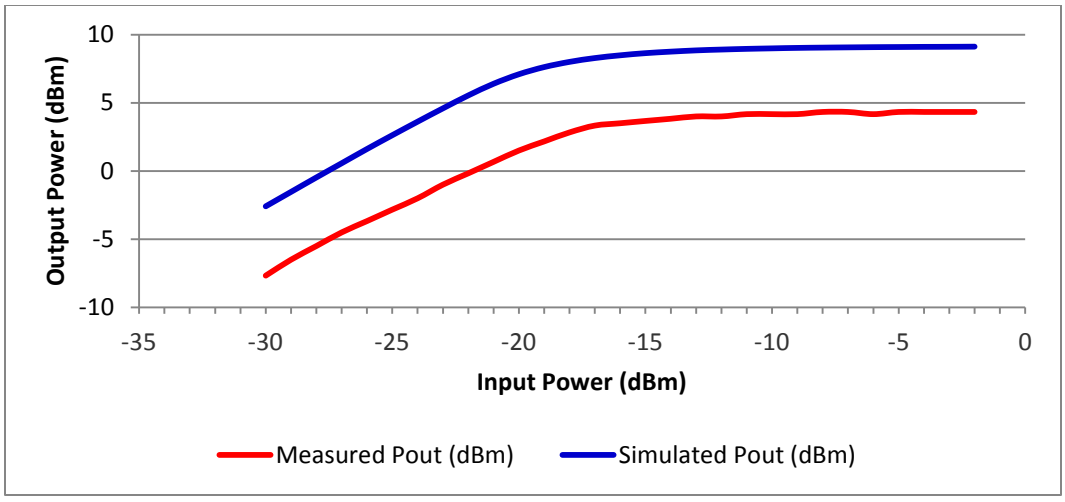

Figure 6.15. Measured and simulated output power versus input power.

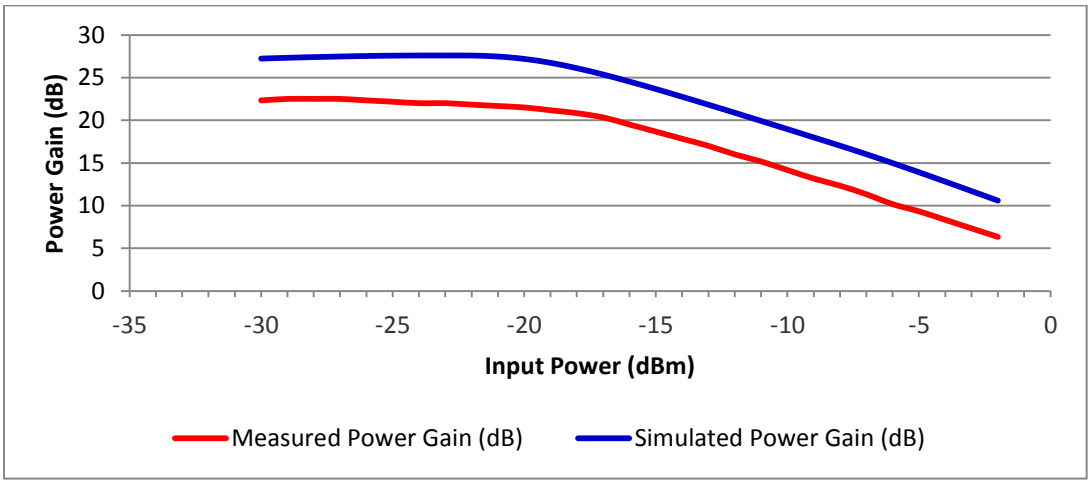

Figure 6.16. Measured and simulated power gain versus input power.

6.12.1 Power Supply Variation Comparison

The PA performance testing over power supply variation was performed. The measurements were performed at 1.2 V, 1.08 V (-10%) and 1.32V (+10%). It can be observed that output power, PAE, and power gain are higher when the power supply increases, and lower when the supply decreases. The three metrics against the power supply voltage variation are also plotted in Figures 6.17-6.19. In the plots, it can be observed that the simulated and the measured plots show the same trend.

Table 6.8. Comparison with Power Supply Variation.

Parameter		Min		Typ		Max		Unit
		Sim	Test	Sim	Test	Sim	Test	
V	Power supply	1.08	1.08	1.2	1.2	1.32	1.32	V
F	Frequency	433	433	433	433	433	433	MHz
G	Power gain	11.65	7.83	12.79	8.33	13.52	8.67	dB
P_{OUT}	RF output power	6.302	2.42	7.916	2.71	9.677	2.93	mW
P_{IN}	RF input power	0.431	0.40	0.431	0.40	0.430	0.40	mW
P_{SUPPLY}	Power supply power	28.09	27.6	34.7	32.88	42.08	33.24	mW
PAE	Power Added Efficiency	20.90	7.32	21.57	7.03	21.97	7.62	%

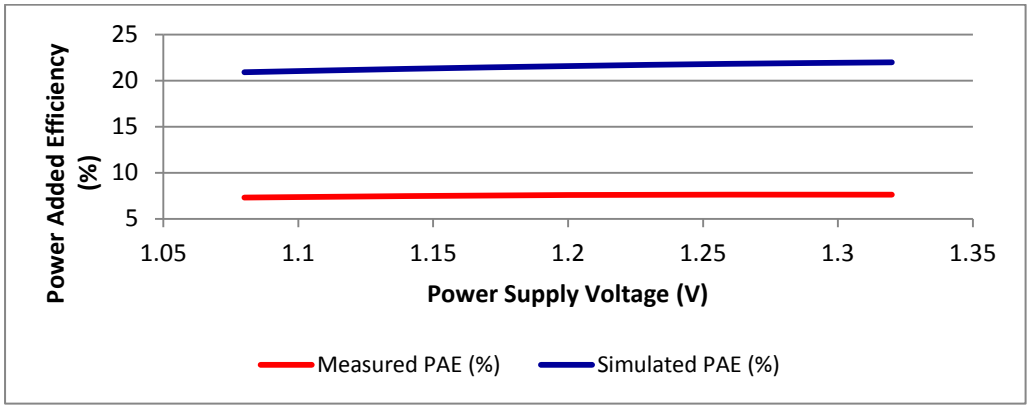

Figure 6.17. Measured and simulated power added efficiency.

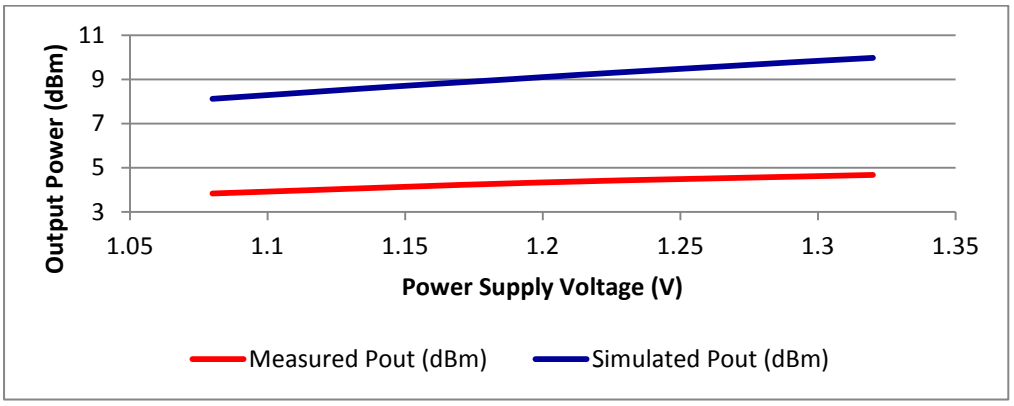

Figure 6.18. Measured and simulated output power.

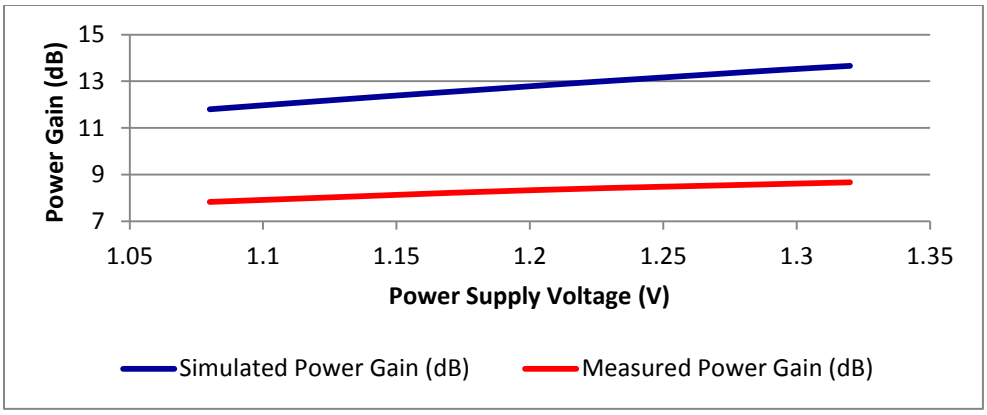

Figure 6.19. Measured and Simulated Power Gain.

6.12.2 Temperature Variation Comparison

Testing over temperature variation was performed. The measurement and simulation results are listed in Table 6.9. It can be observed that the power amplifier achieves higher output power, power gain and PAE at lower temperatures than higher temperatures in both simulation and measurement. The trend in the performance was explained in Section 4.2 on page 42. The three metrics against the temperature sweep are also plotted in Figures 6.20-6.22. The same trend in the plots can be found between the simulation and measurement.

Table 6.9. Temperature Variation Comparison.

Parameter		Min		Typ		Max		Unit
		Sim	Test	Sim	Test	Sim	Test	
T	Temperature	-55	-55	25	25	125	125	°C
F	Frequency	433	433	433	433	433	433	MHz
G	Power gain	14	9.00	12.79	8.33	10.91	6.00	dB
P_{OUT}	RF output power	10.48	3.16	7.916	2.71	5.621	1.20	mW
P_{IN}	RF input power	0.417	0.40	0.431	0.40	0.456	0.40	mW
P_{SUPPLY}	Power supply power	36.15	31.68	34.7	32.88	33.1	32.88	mW
PAE	Power added efficiency	27.84	8.71	21.57	7.03	15.60	2.43	%

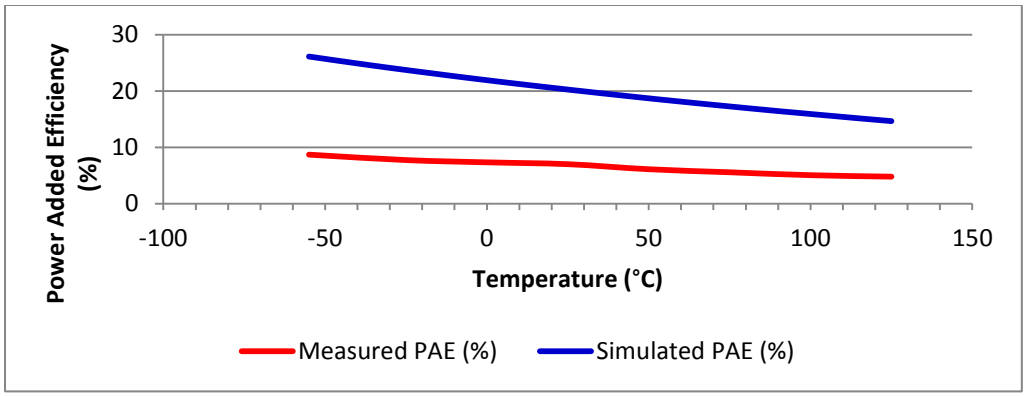

Figure 6.20. Measured and simulated power added efficiency over temperature.

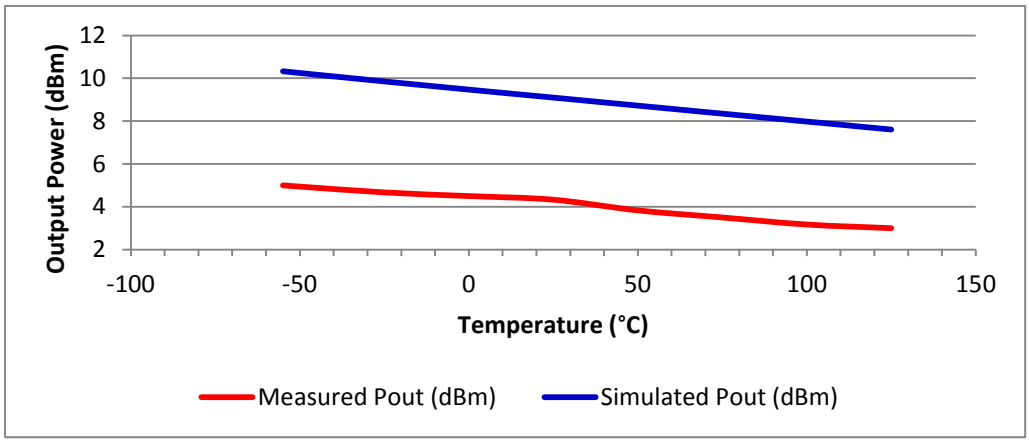

Figure 6.21. Measured and simulated output power over temperature.

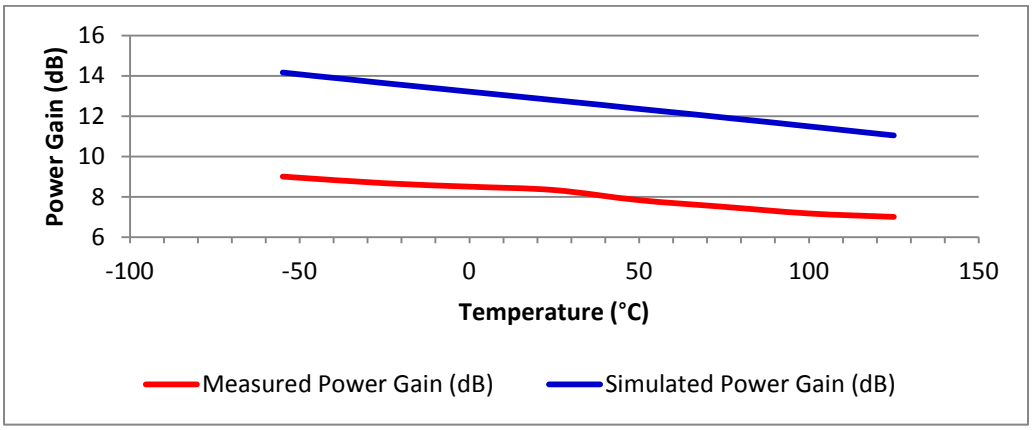

Figure 6.22. Measured and simulated power gain over temperature.

6.12.3 Measured and Simulated S-Parameters

The measured and simulated S-parameters are shown in Figures 6.23-6.26. S11 is a measure of how well the input impedance matching network is designed to match the input impedance of the PA to 50 Ω. This is the same for S22 except that the S22 value is a measure of the output impedance matching. The lower S11 and S22 are, the better matched the input and the output impedances of the PA are. This was explained in the section 4.1.4 on page 36. The frequency of the lowest S11 or S22 point is different from the measured. This is because the simulated input/output impedance is different from the measured values with the matching networks. The mismatch in the input/output impedance causes signal reflection, which results in lower delivered output power and lower PAE.

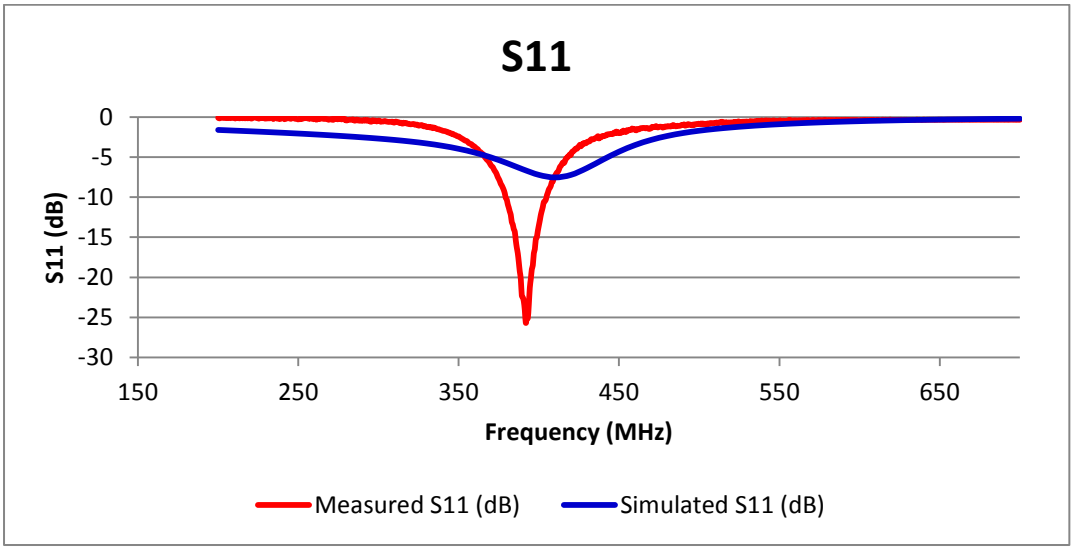

Figure 6.23. S11 plot.

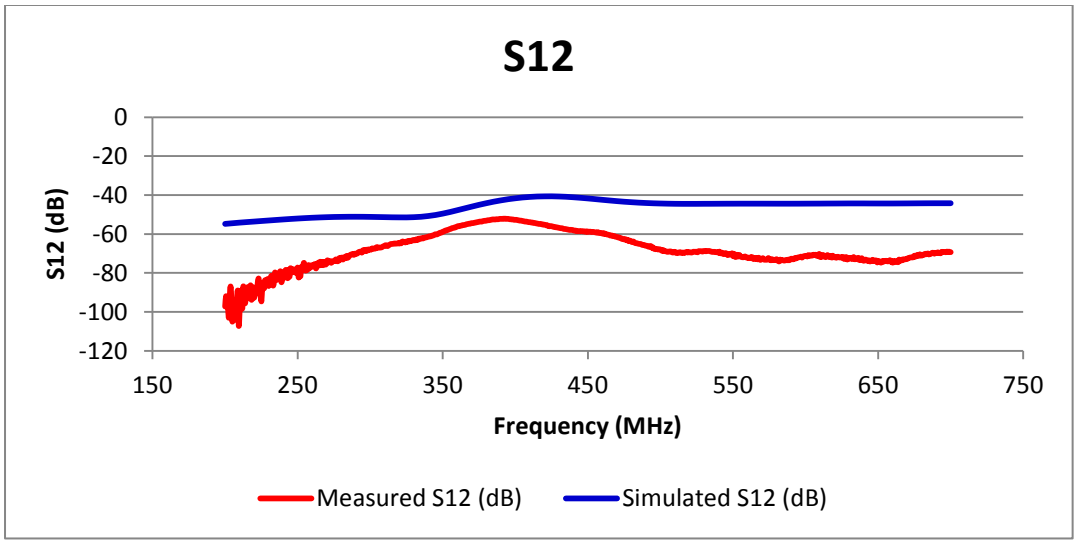

Figure 6.24. S12 plot.

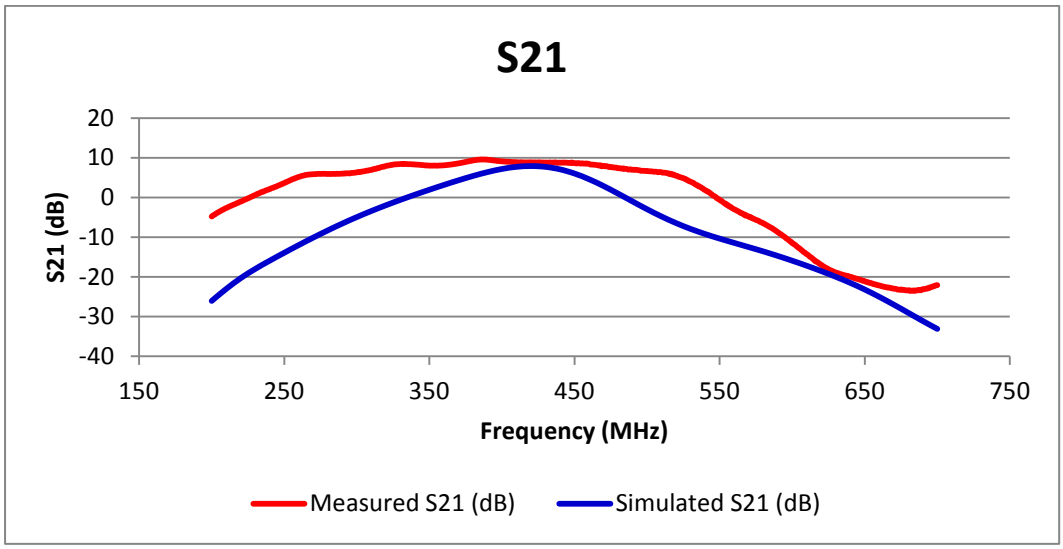

Figure 6.25. S21 plot.

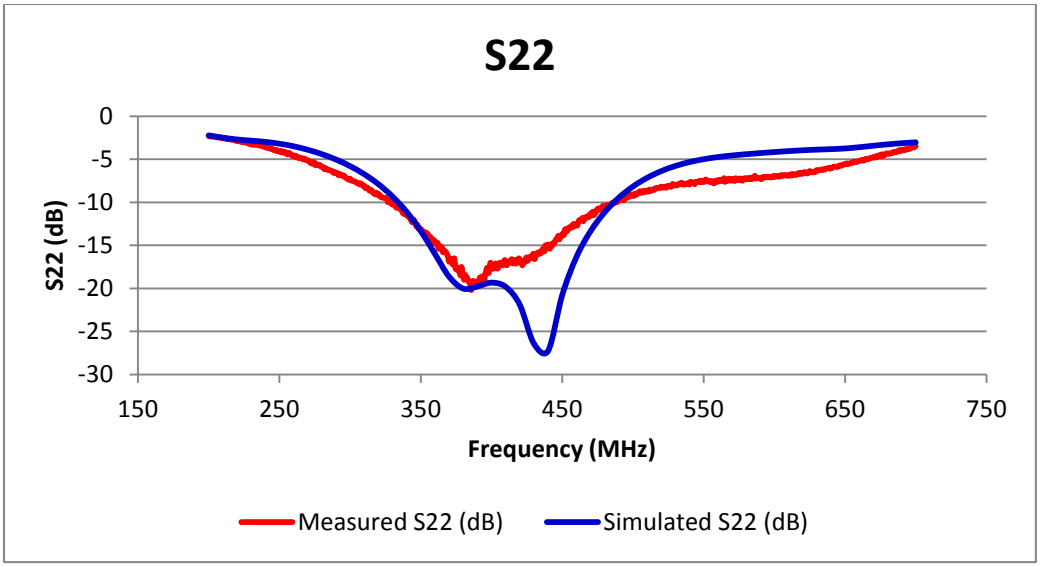

Figure 6.26. S22 plot.

A shift in the frequency of the lowest S11 and S22 points can be achieved by adjusting inductors and capacitors to more accurate values in the L matching networks. In Table 6.10, it can be verified that the frequency of the lowest S22 in simulation shifts according to the variation in the capacitance and inductance in the output matching network. The approach can be applied to the S11 value shifting as well.

Table 6.10. Frequency Shift of the Lowest S22 Caused by Variation in Matching Network.

Output impedance	L	C	Frequency	PAE	P_{OUT}
49.272+0.011j	5.4 nH	5.7 pF	434 MHz	20.8%	6.353 mW
52.718+1.576j	6.2 nH	5.6 pF	433.98 MHz	20.8 %	6.302 mW
52.639-5.909j	6.2 nH	6.6 pF	419.01 MHz	20.62 %	6.345 mW
50.906-13.23j	6.2 nH	7.6 pF	379.99 MHz	20.15 %	6.310 mW
47.574-19.827j	6.2 nH	8.6 pF	370.92 MHz	19.53 %	6.197 mW

6.12.4 Variable Output Power

Output power under different power modes was also measured. The measured results are listed in Table 6.11 and compared with the simulated results. The results prove that the PA is able to deliver 4 different output powers but the output powers are much smaller than what is

desired. It was determined that the discrepancy in power is caused by the insufficient width of the switching transistor in each output power mode. The decreased PA performance will be explained in the later part of this chapter. This issue can be solved by taking enough headroom in the width into consideration in the design for compensating the effect of non-idealities. In other words, using wider width than what is needed in simulation will make the measured results closer to what is needed. This was also mentioned on page 45 of the section 4.2 Simulated Results.

Table 6.11. Comparison with Variable Output Powers.

Selector	00		01		Unit
	Simulation	Test	Simulation	Test	
Input Power	0.431	0.40	0.428	0.40	mW
Output Power	7.916	2.71	1.775	1.04	mW
Power Supply Power	34.7	32.88	20.48	21.12	mW
PAE	21.57	7.03	6.58	3.03	%
Power Gain	12.79	8.33	6.17	4.17	dB
Selector	**10**		**11**		**Unit**
	Simulation	**Test**	**Simulation**	**Test**	
Input Power	0.426	0.40	0.426	0.40	mW
Output Power	0.366	0.26	0.138	0.10	mW
Power Supply Power	13.1	16.08	10.72	14.16	mW
PAE	N/A	N/A	N/A	N/A	%
Power Gain	N/A	N/A	N/A	N/A	dB

6.12.5 Comparison of Test Results with Other Work

A comparison in measured results between this design and three other similar designs is shown in Table 6.12. Paper 1, paper 2, and paper 3 adopt a similar design topology but use different operating frequencies and technology process. The three papers do not include the output power controlling circuitry so that their presented PA is only capable to deliver single fixed output power. The input power in the paper 2 and 3 is also unknown so the paper 1 shows more value than the other two.

Table 6.12. Comparison of Test Results with Other Work.

Parameters		This	Paper1 [1]	Paper2 [2]	Paper3 [18]	Unit
F	Frequency	433	2400	1900	2400	MHz
Process	Technology Process	0.13	0.18	0.18	0.18	µm
Vsupply	Power Supply Voltage	1.2	1.2	1.2	1.2	V
G	Power gain	8.33	9	-	-	dB
3dB BW	3dB bandwidth	200	-	-	-	dB
1dBCP	1-dB compression point	-19.91	-	-	-	dBm
P_{OUT}	RF output power	2.71	5.01	7.94	9.4	mW
P_{IN}	RF input power	0.40	0.67	-	-	
P_{SUPPLY}	Power supply power	32.88	-	-	-	
PAE	Power added efficiency	7.03	21	25	32	%

6.13 Data Analysis in the Output Power and the PAE

Since power added efficiency and output power are the two most important metrics evaluating the performance, more investigation has been performed to find out primary possible causes for the discrepancy between the measured and simulated results. This section will present the possible causes that were found, related data that was collected, and analysis that was made. The data analysis also reveals why the output power and the PAE are low in simulation and measurement for this project.

6.13.1 Discrepancy in the Power Added Efficiency

The power added efficiency or PAE is defined in Equation (6.3) below.

$$Power\ Added\ Efficiency = \frac{Output\ Power - Input\ Power}{Supply\ Power\ Consumption} \quad \textbf{(6.3)}$$

It is easy to see that the PAE is determined in the equation by only three factors which are the output power, the input power, and the supply power consumption. Therefore, the investigation performed focuses on the output power and the supply power consumption since the input power barely changes in all simulations and measurements.

6.13.2 Discrepancy in the Supply Power Consumption

Before looking into the causes, it is necessary to understand that the supply power consumption was measured and simulated in average power. This is because the supply voltage is DC and the current is not a sinusoid signal either. Therefore, it is incorrect to directly calculate the power as a product of rms voltage and rms current. In the simulations, the average power was calculated by using an average function in the Cadence Spectre Calculator. In the measurement, the average power was derived by measuring a voltage drop across the 0.1 ohm resistor in the supply trace. So the average current was calculated by using Ohm's law and the average power was derived.

Therefore, the simulated and measured supply power consumption are put together for comparison. In Table 6.13, the simulation was performed under the conditions that V_{DD} was 1.2 V, RC extraction was included, and process components were used. The measurement was performed at 1.2 V of supply and 1.2 V is used to calculate the measured supply power consumption. The average supply current is 27.1 mA.

Table 6.13. Comparison of Simulated and Measured Supply Power Consumption when V_{DD}=1.2V is Used for Supply Power Consumption Calculation.

Parameters	Simulation	Measurement	Difference
Input power	0.43mW	0.4mW	0.03mW
Output power	7.916mW	2.71mW	5.206mW
Supply power consumption	34.7mW	32.52mW	2.18mW
Power added efficiency	21.57%	7.1%	14.47%
Output impedance	53.39+2.20j	42.6-13.3j	N/A

The data in the Table 6.13 shows that the measured supply power consumption is lower than the simulated one, which is opposite to the normal case that the measured consumption should be higher than the simulated one due to non-idealities that are not considered in the simulations. Meanwhile, it was found that other RF blocks from the same tape-out within the

same project suffered from a common issue of lower power supply on the chip. Therefore, lower supply voltage was treated as a possible cause to find out how it impacts PA performance.

Investigation was performed when V_{DD} was lowered in simulations and a lower V_{DD} was used in calculating the measured supply power consumption. When 1.08 V V_{DD} (-10% off from 1.2 V) was used in the simulations and calculating the measured supply power consumption (the actual V_{DD} used in testing was still 1.2 V), the data in Table 6.14 was collected. Based upon the data, it can be noticed that the simulated supply power consumption becomes lower than the measured one, which is logical. Therefore, a lower V_{DD} voltage is likely to be what happens on the chip.

Table 6.14. Comparison of Simulated and Measured Supply Power Consumption when V_{DD}=1.08V is Used for Supply Power Consumption Calculation.

Parameter	Simulation	Measurement	Difference
Input power	0.431mW	0.4mW	0.031mW
Output power	6.302mW	2.71mW	3.592mW
Supply power consumption	28.09mW	29.268mW	1.178mW
PAE	20.9%	7.89%	13.01%

Further impact of decreased power supply on the PA performance was also investigated when RLCk extraction became available. With RLCk extraction, the simulator is able to provide more accurate simulated data that is closer to what is measured on the chip. In Table 6.15, the output power and the supply power consumption data is shown when the supply voltage decreases from 1.2 V to 0.78 V in simulations, although V_{DD} on the chip is unlikely to be as low as 0.78 V. The decreased V_{DD} are only used to investigate the impact made on the output power and supply power consumption and the trend the two metrics indicate.

Table 6.15. Simulated Output Power and Supply Power Consumption with RLCk Extraction when V_{DD} Varies from 1.2 V to 0.78 V.

V_{DD}	Percentage	Output power	Supply power consumption
1.2V	0%	7.268 mW	63.85 mW
1.08V	-10%	5.9 mW	48.41 mW
0.96V	-20%	4.708 mW	35.44 mW
0.9V	-25%	4.151 mW	29.89 mW
0.84V	-30%	3.624 mW	24.89 mW
0.78V	-35%	3.12 mW	20.44 mW

In the Table 6.15, the trend in simulated supply power consumption can be found that it decreases continuously when power supply drops from 1.2 V. The same trend was also found in the output power. Therefore, lower power supply on the chip can be one of possible causes that lead to lower output power and supply power consumption.

Another possible cause is the parasitic resistance of on-chip inductors. In Table 6.16, simulated parasitic resistance for each inductor is listed.

Table 6.16. Simulated Parasitic Resistance of Each Process Inductor.

Inductor types	Parameters	Simulated Resistance	Inductance
indp	R_{L1tank}	2.592 Ω	8.992nH
indp	R_{L2tank}	0.858 Ω	2.902nH
inds	R_{finite}	5.989 Ω	31.341nH
inds	R_{Ltank}	7.748 Ω	38.924nH
indp	R_{Lp}	1.57 Ω	5.003nH

Without any parasitic extraction considered, when extra series resistance is added to all inductors by the same percentage of its original resistive value, the simulated supply power consumption drops as shown in Table 6.17. In the table, the simulated supply power consumption drops by 3.31 mW when the inductor parasitic resistance increases from 0% to 70%.

The data in the Table 6.17 just shows a trend or an impact that output power and supply power consumption drops greatly when parasitic resistance of the on-chip inductors increases.

Table 6.17. Simulated Output Power and Supply Power Consumption when Extra Resistance is Added to All Inductors.

Added resistance	Output power (mW)	Supply power consumption (mW)
+0%	6.357	30.83
+10%	5.651	30.2
+20%	5.024	29.63
+30%	4.462	29.1
+40%	3.964	28.65
+50%	3.514	28.23
+60%	3.099	27.87
+70%	2.72	27.52

On-chip inductors used for this design use metal layer E1 and MA, the top two metal layers. The sheet resistance of both layers is provided by design manual and MOSIS but in different values. The sheet resistance provided from MOSIS is higher than the values provided by the design manual but the discrepancy is still within the tolerance provided by the design manual as shown in Table 6.18. This means the actual parasitic resistance of inductors on the chip tends to be higher than the values used in simulations. The difference in the resistive values supports that the extra added parasitic resistance in inductors can be a possible cause for discrepancy in the output power and power supply consumption between simulation and measurement.

Table 6.18. Comparison of Sheet Resistance of E1 and MA Layers

Metal layer	Sheet resistance from design manual	Sheet resistance from MOSIS
E1	6.3 mΩ ± 1.26 mΩ / square	6.5 mΩ / square
MA	7 mΩ ± 1.4 mΩ / square	7.7 mΩ / square

Moreover, skin effect is another factor causing increased parasitic resistance of the inductors operating at radio frequency. When the inductors operate at radio frequency, the RF AC current tends to travel along the surface of spirals instead of penetrating far into the body of the spirals. This means that most of the cross sectional area of the spirals is not used to conduct the current. Instead, only the spiral surface is used for conduction. Therefore, the parasitic resistance of the inductors is higher in measurement than simulation since the impact made on the parasitic resistance by the skin effect is not included in the simulations.

A further investigation was taken on the impact on the PA performance when resistance of different inductors increases. The inductors used are *indp* and *inds* inductors. *inds* inductors indicate that the traces of two metal layers are in series in connection for higher achievable inductance. However, *indp* inductors use traces of the two metal layers in parallel in connection for lower parasitic resistance. In Table 6.19, simulated data without parasitic extraction is shown when an extra series resistance is added to inductors in various cases. A noticeable trend can be found that the supply power consumption rises when the extra resistance is added to *indp* inductors, and the power consumption drops when the extra resistance is added to *inds* inductors.

Table 6.19. Impact on the PA Performance when Parasitic Resistance of Each Inductor Varies.

Resistance	P_{SUPPLY}	P_{OUT}	P_{IN}	PAE
All indp inductors	↑	↓	Same	↓
All inds inductors	↓	↓	Same	↓
$RL1_{TANK}$ (indp)	↑ & ↓ (Little)	↓	Barely changes	↓
$RL2_{TANK}$ (indp)	↑ (Little)	↓ (Little)	Same	↓ (Little)
RL_P (indp)	↑	↓	Same	↓
RL_{DC} (inds)	↓	↓	Same	↓
RL_{TANK} (inds)	↓	↓	Same	↓

The trend found in the Table 6.19 can be understood in this way. The rising trend in the supply power consumption is caused by all *indp* inductors except $L1_{TANK}$. All *indp* inductors are used in parallel LC resonant tanks which ideally have infinite impedance at its resonating frequency. The parallel LC tanks including $L1_{TANK}$ and $L2_{TANK}$ inductors act as two band stop filters and ideally do not dissipate any energy while resonating at fundamental and the 3rd harmonics. When inductor parasitic resistance is considered, there is energy dissipation due to the parasitic resistance. Therefore, the lost energy comes from the power supply. When parasitic resistance increases, more power is drawn from the supply to be dissipated into the added resistance. Therefore, the supply power consumption goes up when more extra series resistance is added to the $L1_{TANK}$ and $L2_{TANK}$. Regarding L_P, the reason for the power dissipation is the same. The only difference is that its LC tank is connected to ground. On the other hand, the trend found in *inds* inductors is that the supply power dissipation goes down when more series resistance is added to L_{DC} and L_{TANK} in the output stage. The dropped supply power consumption caused by L_{DC} is due to current limiting that occurs from the increased resistance, which leads to lower supply power consumption. What happens due to L_{TANK} is the same as that for L_{DC}.

To find out how on-chip inductors contribute to the lower PA performance in this project, power consumed by each inductor was simulated. In Figure 6.27, power consumption in each inductor is labeled on the circuit diagram. In Table 6.20, it can be found that the total power consumed (17.532 mW) by all inductors accounts for 53.39% of the supply power consumption (32.84 mW). The sum (21.932 mW) of the 17.532 mW and power dissipated at the drain of two switching transistors Td and T1 accounts for a majority, 66.78% of the power supply consumption (32.84 mW). The rest of the supply power consumption can be accounted for other

process components, bondwires, pads, and any other non-idealities in the circuit.

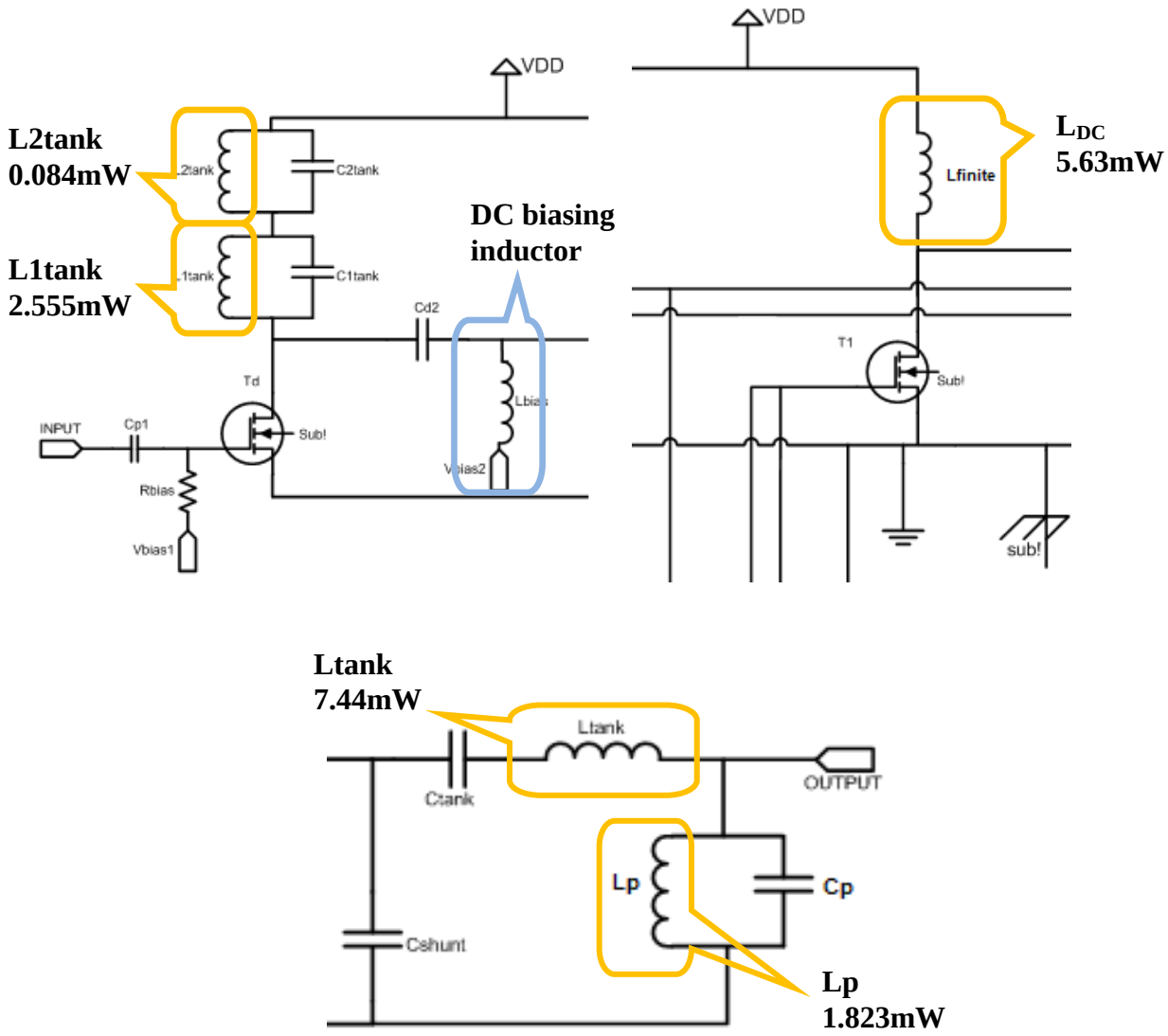

Figure 6.27. Power consumption of each inductor.

Table 6.20. Power Consumption of Each Inductor.

Component	Type	Outer dimension	Inductance	Power consumption	Note
L1TANK	indp	230µm	8.992nH	2.555mW	
L2TANK	indp	200µm	2.902nH	0.084mW	
LDC	inds	250µm	31.341nH	5.63mW	
LTANK	inds	250µm	38.924nH	7.44mW	Greatest
LP	indp	200µm	5.003nH	1.823mW	
Total power				17.532mW	

More simulations were performed to confirm the impact made by the parasitic resistance of the inductors. In Table 6.21, simulated results are listed with using only ideal inductors, only ideal inductors and capacitors, and all process components. It can be observed that the parasitic resistance in inductors itself makes output power drops greatly from 15 mW to 8 mW and PAE drops dramatically from 63% to 21.57%. However, the process capacitors have little impact on the PA performance.

Table 6.21. Simulated Results with Ideal and Process Inductors and Capacitors

Simulations	Output Power	Power Added Efficiency	Power Gain
Using ideal inductors and capacitors	15.31 mW	64.21%	13.32 dB
Using ideal inductors	14.96 mW	62.96%	13.33 dB
Using all process components	7.92 mW	21.57%	12.79 dB

Therefore, it is clear that parasitic resistance of the inductors is a primary cause for low PA performance in this project. Moreover, a conclusion can be reached that lower supply voltage can be a possible cause in the discrepancy of simulated and measured supply power consumption.

6.13.3. Discrepancy in the Output Power

Besides the supply power consumption, the output power is the other factor that determines the power added efficiency of the PA when input power stays the same.

Lower power supply voltage can be a possible factor for the discrepancy that was mentioned previously. Not only does it have a huge impact on the supply power consumption but also the output power. In the Table 6.15, it can be seen that the simulated output power drops greatly when supply voltage decreases.

Another possible cause to discrepancy in output power is extra series resistance added to the inductors. In the Table 6.19, the trend tells that the output power always drops no matter which inductor is added with more series resistance. This is because the power that is supposed

to be delivered to load of the PA is dissipated at the inductor parasitic resistance. The higher the resistance, the less power delivered to the output. Moreover, it was also found that discrepancy in sheet resistance and skin effect contribute to the increased resistance of the inductors, which helps explain that the added resistance in the inductors possibly causes the discrepancy in simulated and measured output power.

Another trend is found that the output power drops much faster than any other inductors when the same amount of extra series resistance is added to L_P inductor. This is because the parallel LC tank including the L_P inductor connects the PA output to ground. Ideally, the LC tank acts as a band stop filter which means it acts as a perfect open circuit at the fundamental frequency. When series resistance is introduced, the LC tank is no longer an idea open circuit. The LC tank allows more output power to be dumped into ground as power dissipation, which is unlike any other LC tanks in the circuit. This helps to explain why the output power is so low. The data in the Tables 6.20 and 6.21 makes it clearer that parasitic resistance in the inductors causes much lower output power.

6.13.4 Impact of the Driver Stage

The impact of the driver stage on the PA performance has been investigated. The simulation was performed to see how the possible distortion in the square wave generated by the driver stage can affect the possible overlap of drain current and voltage of the switching transistor in the output stage. The idea behind the simulation is that a distorted square wave form increases transition time between ON and OFF states, which leads to more overlap in the drain current and voltage. The overlap dissipates more power drawn from the power supply. In Table 6.22, the simulation was performed under 3 scenarios to study the trend in PA performance when driver signal varies from ideal to non-ideal cases. The trend can be seen that the supply power

consumption and average power dissipation at the drain rise and the output power drops when more non-ideal factors in the driver are included in the simulation.

Table 6.22. Impact on the PA Performance when the Driving Square Wave Varies from Ideal to Non-ideal Cases.

Ideal

Process

Cases	Pwr supply pwr	Output pwr	Drain pwr
Ideal square wave w/o driver	28.45 mW	9.676 mW	2.022 mW
Ideal L and C w/ driver	30.31 mW	8.429 mW	2.637 mW
Process L and C w/ driver	32.45 mW	8.129 mW	2.78 mW
Trend	↑	↓	↑

All in all, it can be learned that there are a few possible causes that lead to the discrepancy between the simulation and measurement. Analysis was given based on several different simulations that were performed. Major power dissipation in inductors was also investigated along with the possible impact made by the driver stage.

CHAPTER 7

Conclusions and Future Work

The presented thesis shows the design flow of the RF class E power amplifier for wireless sensor networks in a low power application. The PA was designed in a 130 nm CMOS process, simulated, laid out, and simulated again with RC and RLCk parasitic extraction to characterize the performance of the PA as accurately as possible in Cadence Spectre. After verification of the simulation, the PA was fabricated, bonded, and packaged in a QFN48 package by MOSIS. After a custom made 4-layer PCB was made, the chip was assembled on the PCB with other through-hole and surface mount components. The necessary bench characterization was performed over the desired temperature range following the test plan. The measured results were acquired, compared with simulated results, and listed in the previous chapters.

Therefore, conclusions can be drawn below according to the observation and analysis in previous chapters. The measurement results prove that the PA does work and amplifies the RF input signal power with four different output power control options over -55 °C to 125 °C. However, the PA performance is not as good as desired. The measured output power and PAE are still far from the desired values. Sufficient investigation was taken to find out the root causes. A conclusion can be drawn that lower supply voltage and extra series resistance added to the integrated inductors are possible causes in the discrepancy in the simulated and the measured data. It is also found that the resistance in the inductors is a primary cause to the low efficiency and output power for this project. Other possible causes can be a power consuming driver stage and insufficient width of some switching transistors. Non-ideality in the PCB, test equipment, and cables also need to be considered. Therefore, it is most likely a combination of several

reasons that lead to the discrepancies in the simulated and measured data, and low performance of the presented design.

This RF class E PA was made as an individual RF block at the time of writing but will be eventually integrated together in a system level design with other RF blocks and digital circuitry on a single chip. Switching to other topologies for the current design should be considered if a class E PA is not suitable for this project.

To achieve a better PA performance in the PAE and the output power, possible improvements that could be made are suggested below. Firstly, since extra series resistance in the inductors is a major problem, to use less inductors in the driver stage and smaller inductors in the output stage is desirable because less resistance means less power dissipation on the coil resistance. Another suggestion [18] for the inductors is to use circular inductors instead of square-shape or octagonal-shape for less parasitic resistance, which is beneficial but not available with the current process technology. Secondly, a driver stage that is less power consuming is helpful in reducing the supply power consumption to boost the efficiency. According to the simulated performance, power dissipation of the driver stage accounts for about 18% of the total supply power consumption. A driver stage topology that is less power consuming is desirable [18]. Thirdly, a less distorted square wave as the driver signal for the output stage is also desirable. This is because a less distorted square wave means less transition time between ON and OFF states. Therefore, less power dissipation at the drain of the switching transistors can be achieved [18]. Last but not least, it is also worth trying other possible PA design topologies that are possibly more efficient in reality for this project.

Possible improvements seen in other papers are also presented below. Some papers [19] [20] suggest using a more suitable device technology such as GaAs instead of silicon. It is

claimed that the advantages of using GaAs over silicon are GaAs has higher electron mobility, higher saturated electron velocity, relatively insensitive to heat, and tend to have less noise. Therefore, GaAs is more likely to achieve better performance. In Figure 7.1, a comparison in performance using GaAs and Si technologies [19] has been made for a GSM RF PA operating at GSM 900 MHz. It can be clearly seen that using GaAs technology achieves higher PA performance when V_{DD} is even lower than using silicon technology.

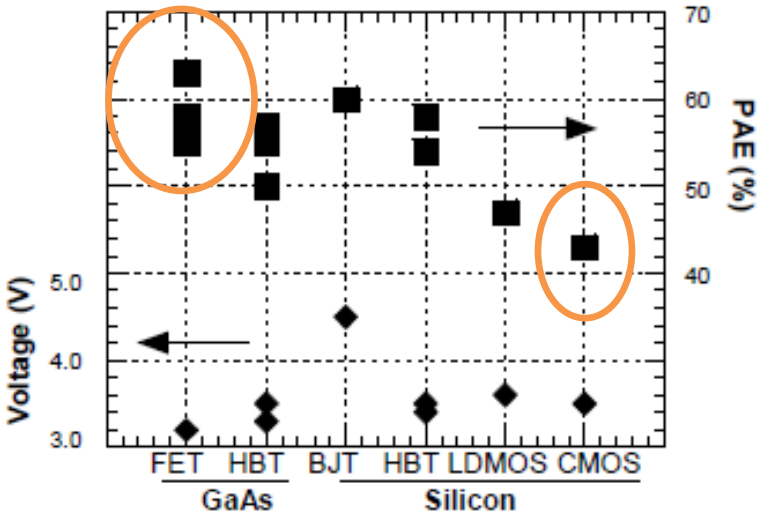

Figure 7.1. GSM RF PA operating at GSM 900MHz, using GaAs (FET and HBT) and Si (BJT, HBT, LDMOS, and CMOS) technologies.

It is also noticed that process technologies with longer transistor length tend to be used, such as 0.18 μm, 0.25 μm, and 0.8 μm, etc. Using shorter length like this PA design means down scaling the device. The disadvantage of down scaling the device (deep submicron technology) is that lower supply voltage has to be used and results in higher power dissipation, which is mentioned previously [21]. In Figure 7.2, pushpins correspond to the minimum power consumption in a technology at the nominal supply voltage for each CMOS process [21]. On the other hand, downscaling in process also results in lower breakdown voltage which causes more peak voltage stress at the drain of the switching transistors in class E PA. The peak drain voltage,

4.27 V, in the output stage of the class E PA is 3.56 times the power supply voltage, 1.2V. The breakdown voltage of *dgnfet_rf* transistors used in this design is 6 V. So there is still a little head room for the breakdown voltage before it is exceeded.

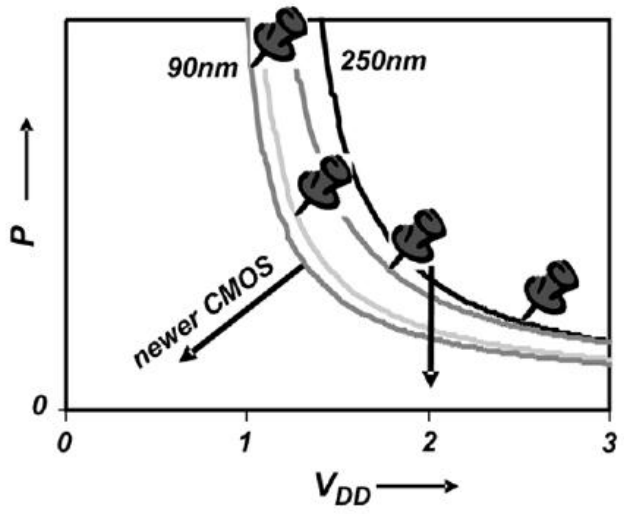

Figure 7.2. Miminum power consumption for an (arbitrary) analog circuit with fixed topology and performance as a function of the supply voltage, for four technologies.

It is found that higher supply voltages are commonly used in other papers of similar designs, such as 1.8, 2.5, 3, 3.3, 5, and 10 V. In Figure 7.2 [21], the graph shows that power consumption increases exponentially when the power supply decreases. In a lower power application design using low supply voltage, the challenge is that the input power and DC power consumption in the driver stage are no more negligible [18]. Therefore, using lower supply voltage severely degrades the overall transmitter efficiency.

What's more, higher operating frequencies tend to be used in other papers. The higher frequencies used are 835 MHz, 900 MHz, 1.9 GHz, and 2.4 GHz, etc. The advantage of using higher operating efficiency makes smaller inductors with less inductance possible, according to Equation (7.1). With smaller inductors, less parasitic resistance and less power dissipation are achieved.

$$L = \frac{1}{(2\pi f)^2 C} \quad \textbf{(7.1)}$$

Regarding the power control scheme, Dr. Peter Wilson and Dr. Reuben Wilcock of the University of Southampton mentioned a different scheme [24]. The paper presented a successive turn on of binary-weighted transistors that are connected together in parallel. Among all transistors with identical size, at least one is turned on all the time for the lowest current conduction. Other transistors in parallel can be turned on and added for more current conduction as needed.

Based on the above investigation, future modification in the design can be made for better PA performance if the class E topology is still considered for the future integration on system level. The issues addressed in this thesis are also helpful as warnings to be avoided in a future design. What is discovered in other papers or works is given as a reference on how similar PA designs perform, what possible issues have been addressed, and how these issues are solved for better performance.

BIBLIOGRAPHY

[1] Munir M. El-Desouki, M. Jamal Deen, Yaser M. Haddara, "A Low-Power CMOS Class-E Power Amplifier for Biotelemetry Applications," in *Microwave Conference, 2005 European,*vol. 1, Oct. 2005.

[2] Chien-Chih Ho, Chin-Wei Kuo, Chao-Chih Hsiao, Yi-Jen Chan, "A Fully Integrated Class-E CMOS Amplifier with a Class-F Drive Stage," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE* , pp.211-214, 2003.

[3] Steve Hung-Lung Tu, "Class E RF Tuned Power Amplifiers in CMOS Technologies: Theory and Circuit Design Considerations," in *IEEE Radio Communications*, September 2004.

[4] Hella, Mona Mostafa, and Mohammed Ismail. *RF CMOS power amplifiers: theory, design, and implementation*. Boston: Kluwer Academic Publishers, 2002. Print.

[5] NI Developer Zone. (2009, July 23). *What Is a Wireless Sensor Network? - Developer Zone - National Instruments* [Online]. Available: http://zone.ni.com/devzone/cda/tut/p/id/8707.

[6] Changsik Yoo, Qiuting Huang, "A Common-Gate Switched 0.9-W Power Amplifier with 41% PAE in 0.25-um CMOS," in IEEE Journal of Solid-State Circuits, vol.36, NO.5, May 2001.

[7] Iulian Rosu. *RF Power Amplifiers* [Online]. Available: http://www.qsl.net/va3iul/RF%20Power%20Amplifiers/RF_Power_Amplifiers.pdf.

[8] John Guy, "Class D Amplifier FAQ," National Semiconductor, 2009.

[9] King Chun Tsai, "CMOS power amplifiers for wireless communications," PhD dissertation, University of California, Berkeley, USA, pp.118, Fall 2007.

[10] Alinikula, P.; Choi, K.; Long, S.I.; , "Design of Class E power amplifier with nonlinear parasitic output capacitance," Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on , vol.46, no.2, pp.114-119, Feb 1999.

[11] Dusan Milosevic, Johan van der Tang, and Arthur van Roernund, "Investigation on technological aspects of class E RF power amplifiers for UMTS applications," Department of Electrical Engineering, Eindhoven University of Technology.

[12] N. O. Sokal and A. D. Sokal, "Class E - A new class of high-efficiency tuned single-ended switching power amplifiers," IEEE J. Solid-State Circuits, vol. 10, pp. 168–176, June 1975.

[13] Neurotrol. *Harmonics and Superposition* [Online]. Available: http://neurotrol.com/Pages/Projects/Project1.html.

[14] Reynaert, Patrick, and Michiel Steyaert. *RF power amplifiers for mobile communications*. Dordrecht: Springer, 2006. Print.

[15] SEMTECH, "RF Design Guidelines: PCB Layout and Circuit Optimization", pp. 6, 2006.

[16] John Wetherell. (2011, July 1). *Impedance Matching Network Designer* [Online]. Available: http://bwrc.eecs.berkeley.edu/research/rf/projects/60ghz/matching/impmatch.html.

[17] K. -Wai and H.C. Luong, “A 1-V CMOS power amplifier for bluetooth applications”, IEEE Trans. On circuits and syst.-II: Analog and digital signal processing, vol. 50, No. 8, pp.445-449, Aug., 2003.

[18] Hyoung-Seok Oh; Taeksang Song; Sang-Hyun Baek; Euisik Yoon; Choong-Ki Kim; , "A fully integrated 1 V, +9.5 dBm, 43%-PAE injection-locked Class-E power amplifier for wireless sensor network," Radio and Wireless Symposium, 2006 IEEE , vol., no., pp. 235-238, 17-19 Jan. 2006.

[19] Chuck Weitzel, "Will GaAs Survive for Wireless PA’s? ,“ The International Conference on Compound Semiconductor Manufacturing Technology, 2005.

[20] Sowlati, T.; Salama, C.A.T.; Sitch, J.; Rabjohn, G.; Smith, D.; , "Low voltage, high efficiency GaAs Class E power amplifiers for wireless transmitters," Solid-State Circuits, IEEE Journal of , vol.30, no.10, pp.1074-1080, Oct 1995.

[21] Annema, A.-J.; Nauta, B.; van Langevelde, R.; Tuinhout, H.; , "Analog circuits in ultra-deep-submicron CMOS," Solid-State Circuits, IEEE Journal of , vol.40, no.1, pp. 132- 143, Jan. 2005.

[22] Grebennikov, Andrei, and Nathan O. Sokal, “Switchmode RF power amplifiers,” Amsterdam: Elsevier/Newnes, pp. 253, 2007.

[23] Ho Ka Wai, “A 1-V CMOS Power Amplifier for Bluetooth Applications,” M.S. thesis, Dept. of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong, August 2002.

[24] Wilson, P.R.; Wilcock, R.; , "Operational calibration of mixed-signal integrated circuits in hostile environments," *Aerospace conference, 2009 IEEE* , vol., no., pp.1-7, 7-14 March 2009.