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Carbon nanotubes on graphene: Electrical and interfacial properties

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CARBON NANOTUBES ON GRAPHENE: ELECTRICAL AND INTERFACIAL PROPERTIES

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Abstract

An integrated circuit (IC) consists of copper (Cu) and tungsten (W) interconnects to facilitate conduction among its components such as transistors, resistors, and capacitors. As the minimum feature size in IC technology continues to scale downward into the sub-20 nm regime, interconnects are faced with performance and reliability challenges arising from increased resistance and electromigration, respectively [1]. To partially mitigate such challenges, our project aims at studying a structure as a potential replacement for Cu and W, formed by growing carbon nanotubes (CNTs) directly onto graphene, and investigating the resulting electrical and interfacial properties. Various CNT/Graphene structures are fabricated using sputtered iron (Fe), cobalt (Co), or nickel (Ni) catalyst films and subsequent thermal chemical vapor deposition (CVD) or plasma-enhanced chemical vapor deposition (PECVD) processes for CNT growth. The objective of this research is to assess the viability of CNTs directly grown on graphene as a functional alternative to Cu and W interconnects in integrated circuits. Using Co as a catalyst for CNT growth with a thermal CVD process, we have succeeded in creating a conductive all-carbon 3D interconnect structure.

Acknowledgments

We would like to acknowledge the strong support and guidance of our project and academic advisor, Dr. Cary Yang. We are grateful to the Santa Clara University School (SCU) of Engineering faculty and staff for their support in the form of encouragement, guidance, and access to their state-of-the-art Center for Nanostructures that made our research possible. We thank Changjian Zhou, Salahuddin Raju, and Mansun Chan from the Hong Kong University of Science and Technology for supplying us with graphene samples and for their continued collaboration along with Phillip Wang of Applied Materials. Additionally, we thank Anshul A. Vyas and Patrick Wilhite for their helpful advice and for their research on CNTs that helped establish a starting point for our project.

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Chapter 1: Introduction and Motivation

1.1 Challenges for Copper Interconnects

The basis of all electronic devices is the integrated circuit (IC). ICs are primarily responsible for performing the necessary operations carried out by modern electronics, and, as such, they must utilize technology that is as high-performing and reliable as possible. In keeping with the trends predicted by Gordon Moore in 1965, the semiconductor industry has to a great extent successfully followed the empirical "Moore's Law", that is, doubling the number of transistors in ICs every two years [2]. Though this is not a science-based law, it nevertheless dictated the trend by which electronics scaled up in power and ability and scaled down in size, precisely because we have been able to make feature sizes in ICs smaller to keep up with its prediction. As the minimum feature size scales down beyond the sub-20 nm regime, however, transistors have gotten so small and so numerous that there is little room left to keep the chip (IC) size continuously decreasing [3]. Any piece of electronic equipment can contain many chips such as those shown in Figure 1. With this in mind, semiconductor companies have tried scaling their packaged chips into the third dimension, though this has been shown to be unsustainable [4].

These problems alone are enough to see that the industry is in need of a major paradigm shift in order to keep up with current and future demands in computing. Directly related to these issues of scale, we observe a number of phenomena affecting IC performance [5]. Figure 2 shows the cross-section of a typical modern IC utilizing Cu interconnects for on-chip electrical connections. There have been noticeable effects contributing to increased resistance of these Cu interconnects. As the interconnect linewidths reach the nanoscale and become comparable to the electron mean free path, increased scatterings result from the interconnect wire interior walls, known as surface scattering. Further, at such linewidths, the size of polycrystalline Cu grains is becoming smaller, thus increasing the scatterings from the grain boundaries. The combined increase in surface and grain boundary scatterings leads to a significant surge in Cu resistivity as the linewidth approaches the sub-100 nm regime, as shown in Figure 3(a) [6]. In addition, decreased interconnect linewidth is accompanied by an increase in current density, giving rise to electromigration [6]. As current density increases within a wire, the local electric field is sufficiently high enough to displace the atoms from their lattice sites, creating voids and eventually an open circuit. This chip failure occurs when the maximum current density in the chip, J_{max}, exceeds the current-carrying capacity of Cu, as illustrated in Figure 3(b). In the nanoscale, current-carrying capacity generally decreases with decreasing linewidth, making it a serious reliability challenge [7]. The same challenges exist for W as well [8].

As the interconnects continue to shrink, we expect these challenges will become more acute, signaling the need for a more reliable nanoscale conductor as a replacement for Cu and W [5–7].

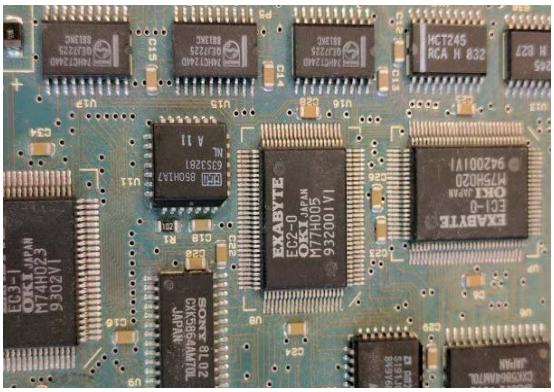

Figure 1: Typical circuit board with surface-mounted integrated circuits or chips.

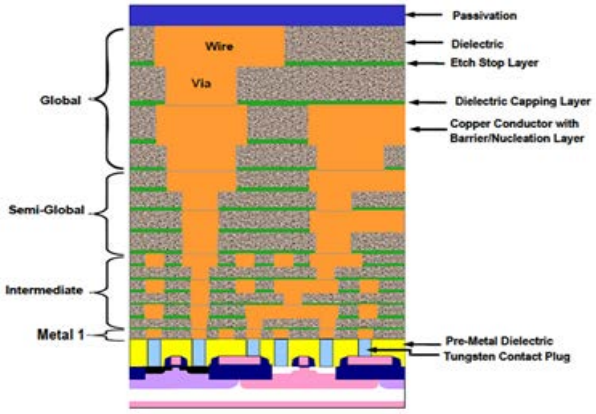

Figure 2: Cross-sectional schematic of an integrated circuit with copper interconnects (orange) [9].

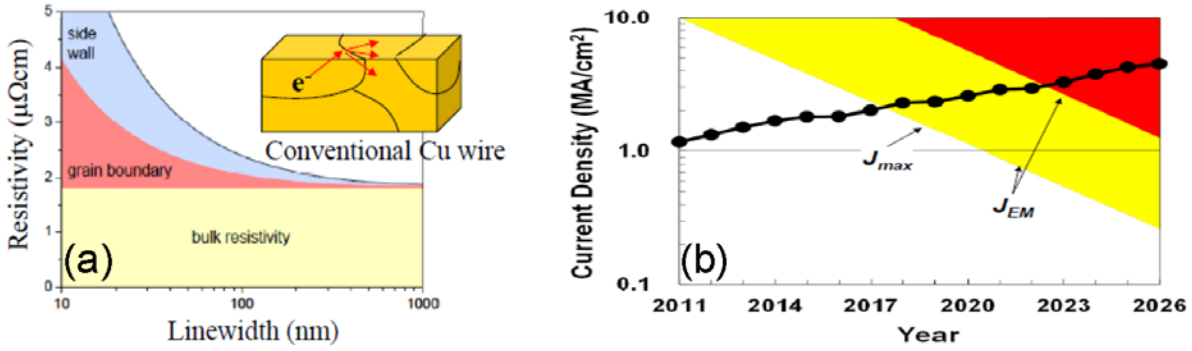

Figure 3: (a) Effect of decreasing linewidths on the Cu resistivity. (b) Existing and projected current density requirements for Cu interconnects [6].

1.2 Properties of Graphene and Carbon Nanotubes

To address the challenges faced by current Cu interconnects, our group at SCU has been studying nanocarbon materials as potential replacements. In particular, we focus on graphene and carbon nanotubes (CNTs), as shown in Figures 4 and 5, respectively, as they are electromigration resistant, have excellent electrical and thermal properties, and are among the mechanically strongest materials yet discovered [10–12]. Thus, they seem to be natural replacement candidates for Cu and W.

All existing measurements indicate current-carrying capabilities of these nanocarbon materials to be at least an order of magnitude higher than that of bulk Cu [13]. This is a highly desirable property, as it would accommodate the projected J_{max} for future generations of IC technology. As these nanocarbons possess strong bonding between atoms, they are expected to withstand high temperature as well as mechanical and electrical stress. Such superior

properties are a result of the sp^2-hybridized bonding within the honeycomb structure, with each atom surrounded by three nearest neighbors on the graphitic plane [14]. In contrast, another form of carbon, diamond, consists of sp^3-hybridized bonds for each atom with its four nearest neighbors throughout its crystal structure, giving rise to superior mechanical strength. Due to diamond's wide bandgap, however, it is a poor conductor of electricity. By having sp^2-hybridized bonding, CNTs and graphene are able to create an equally strong structure along the graphitic plane and still allow for excellent electrical and thermal conduction.

While discussing the feasibility of these nanocarbons as replacements for Cu and W, it is important to note that CNTs and graphene are not immune from a problem faced by all conductors: contact resistance at interfaces with other materials. Contact resistance results from any heterogeneous interface, and it can be the dominant resistance component in any structure involving nanocarbons [15]. Thus, it is the primary challenge for making any nanocarbon-based technology viable.

Typically, CNT devices require CNTs grown directly on a metal surface [16]. The resulting CNT-metal interface has a relatively high contact resistance, contributing to a significant portion of the overall device resistance. On the other hand, if one can take advantage of the sp^2 bonding that both CNTs and graphene share and form a structure with continuation of such bonding across the CNT-graphene interface, then the contact resistance between a vertically conductive carbon nanotube and a horizontally conductive layer of graphene can be drastically reduced [17]. This is the motivation for embarking on our study of the CNT/Graphene structure.

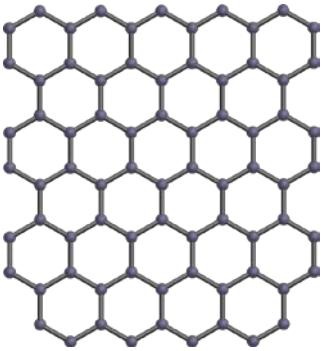

Figure 4: A single layer of graphene with the honeycomb crystal structure.

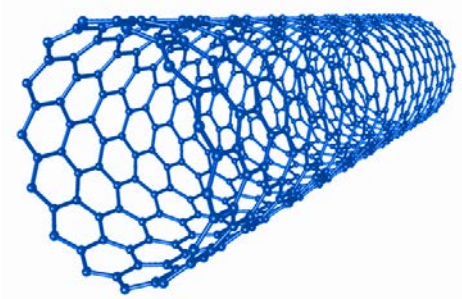

Figure 5: Single-walled carbon nanotube (SWCNT). Note how this shape can be created by folding a layer of graphene into a cylinder. A multi-walled CNT (MWCNT) results from folding more than one layer of graphene into concentric cylinders.

Chapter 2: Objectives

2.1 Project Goals

The objective of this project was to design a process to fabricate an all-carbon 3D structure with CNTs grown directly on graphene as a potential replacement for Cu and W interconnects, as depicted in Figure 6. To achieve this objective, the process must result in a conductive CNT/Graphene structure.

2.2 Project Requirements

As discussed in Section 1.2, both CNT and graphene have a structure that is mechanically strong while also allowing for excellent electrical conduction. By utilizing the C-C sp^2 hybridized bonds at and near the CNT edge and on graphene, we can create in principle an interface with minimal contact resistance. Successful fabrication of this structure would lead to a virtually homogeneous all-carbon 3D interconnect with CNTs for vertical conduction and graphene layers for horizontal conduction.

The process to fabricate this structure involves first sputtering a thin catalyst film onto the substrate, followed by either plasma-enhanced chemical vapor deposition (PECVD) or thermal chemical vapor deposition (CVD) for CNT growth. The necessary instruments are available to us at the SCU TENT Laboratory located in NASA Ames Research Center.

The fabricated structures are characterized using the following tools at the Center for Nanostructures on the SCU campus: the scanning electron microscope (SEM), wafer probe station, and nanoprober. With the SEM, we obtain images of the fabricated structures to generate statistics on various growth characteristics such as CNT height and diameter distributions. From electrical probing measurements, current-voltage (I-V) behaviors and device resistances are obtained.

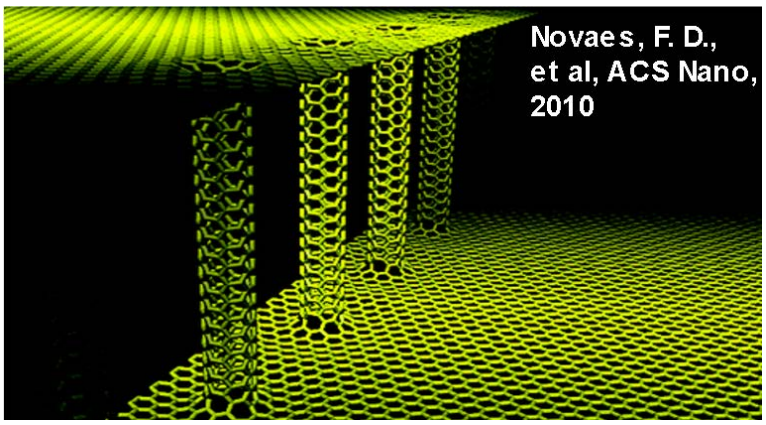

Figure 6: A computer-generated image of an all-carbon 3D interconnect structure with graphene and CNTs as the horizontal and vertical conductors, respectively [18].

Chapter 3: Experimental Methods

3.1 Test Structure Fabrication

The initial experimental steps are aimed at producing graphene layers on top of a silicon wafer. First, multi-layer graphene is grown by heating a substrate consisting of a deposited Ni catalyst film on a SiO_2-covered Si wafer, in the presence of H_2 and CH_4 inside a PECVD chamber, as illustrated in Figure 7(a)-(b) [19]. The graphene layers are subsequently transferred onto another oxide-covered Si substrate using spin-coated PMMA as a backbone that is later removed, as shown in Figure 7(c)-(e) [19]. The graphene samples were prepared at the Hong Kong University of Science and Technology as part of a collaboration between a research group there and our TENT Laboratory.

We then sputter a thin catalyst film on the transferred graphene before growing CNTs using either a PECVD or a thermal CVD process, as illustrated in Figure 7(f)-(h). Details of the CNT growth processes are described in the next section.

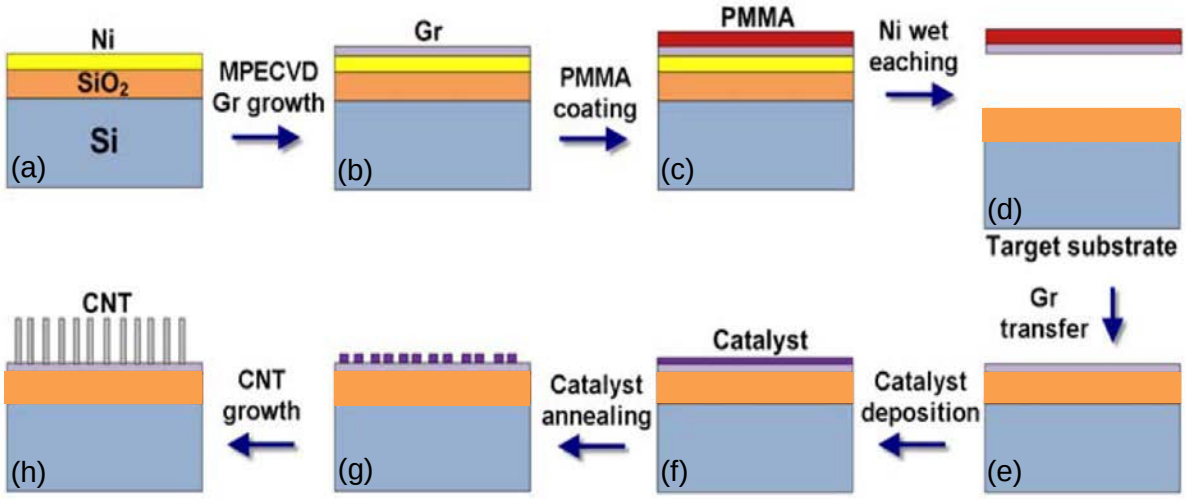

Figure 7: Process flow for test structure fabrication. (a)–(e) illustrate the steps to produce usable graphene layers on oxide-covered Si wafer. (f)–(h) summarize the CNT growth process [19].

3.2 Growth Processes

Two separate techniques are used for CNT growth, PECVD and thermal CVD. Both are rooted in the generic vapor-liquid-solid (VLS) method for producing nanowires, as illustrated in Figure 8. The VLS method uses a catalyst to facilitate the growth of nanowires [20]. In order to achieve the best possible outcome in terms of compatibility with IC technology and resistance of the fabricated structure, different catalysts are used for our growth experiments, namely, nickel (Ni), iron (Fe), and cobalt (Co) [21].

The catalyst film is deposited directly on graphene using a magnetron sputtering system. The sputtering process is illustrated in Figure 9 with a photo of the chamber during film deposition, shown in Figure 10. After depositing a thin film (<10 nm) of catalyst material onto graphene, the sample is transferred to a reactor for CNT growth. Both the sputtering and PECVD systems are located at the TENT Laboratory in NASA Ames Research Center.

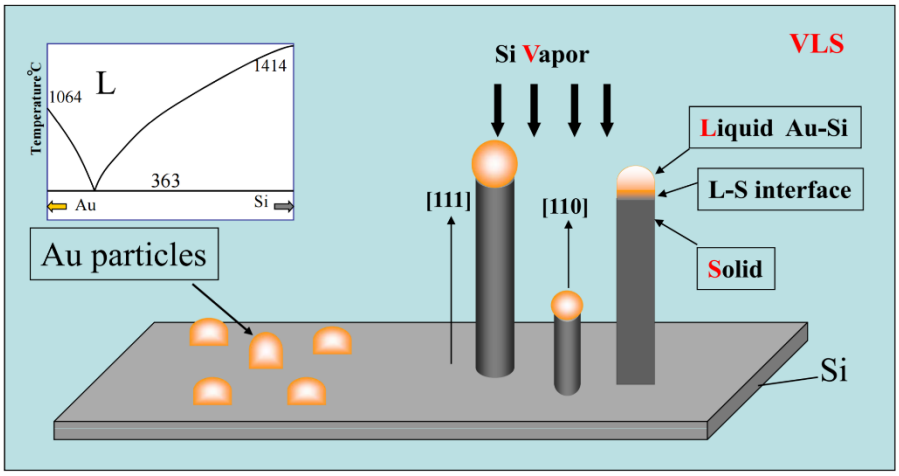

Figure 8: Generic VLS method for producing nanowires. In this schematic, gold nanoparticles are used to catalyze silicon nanowire growth. The process is similar to CNT growth using catalyst film.

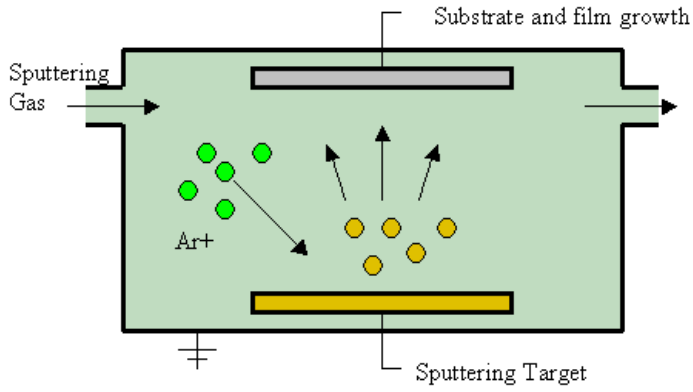

Figure 9: Schematic of film deposition using sputtering.

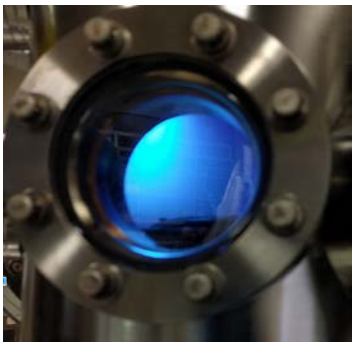

Figure 10: Photo of the sputtering process in action. The blue glow inside the chamber is produced by Ar^+ plasma during film deposition.

3.2.1 Plasma-Enhanced Chemical Vapor Deposition (PECVD)

This technique includes a plasma step not present in the generic VLS method. We refer to the collective sequence of steps for the PECVD process as the "growth recipe." Our recipes are developed based on the previous work of our group and information from the literature [19, 22, 23], as well as preliminary experiments conducted prior to the start of this project.

The sample is first heated to dewet the thin catalyst film into discrete nanoparticles, which are the growth sites for CNTs. This is followed by flowing a mixture of ammonia (NH_3) and acetylene (C_2H_2). The latter is then dissociated in a chemical reaction facilitated by the catalyst, producing carbon atoms that, in turn, form CNT beneath the catalyst particle. (In most cases, the catalyst particle remains at the CNT tip throughout the growth process, thus called "tip growth.") The electric field produced by creating a plasma from capacitive DC discharge, as shown in Figure 11(a), facilitates vertical alignment of the resulting CNT arrays [24].

3.2.2 Thermal Chemical Vapor Deposition (CVD)

Unlike PECVD, thermal CVD does not involve the generation of a plasma during CNT growth. It requires minor adjustments to the recipe while maintaining the same growth temperature. Comparisons of these two processes are given in Table 1. Since the DC electric field is no longer present, the resulting CNTs are generally not vertically aligned. The thermal CVD process is depicted in Figure 11(b).

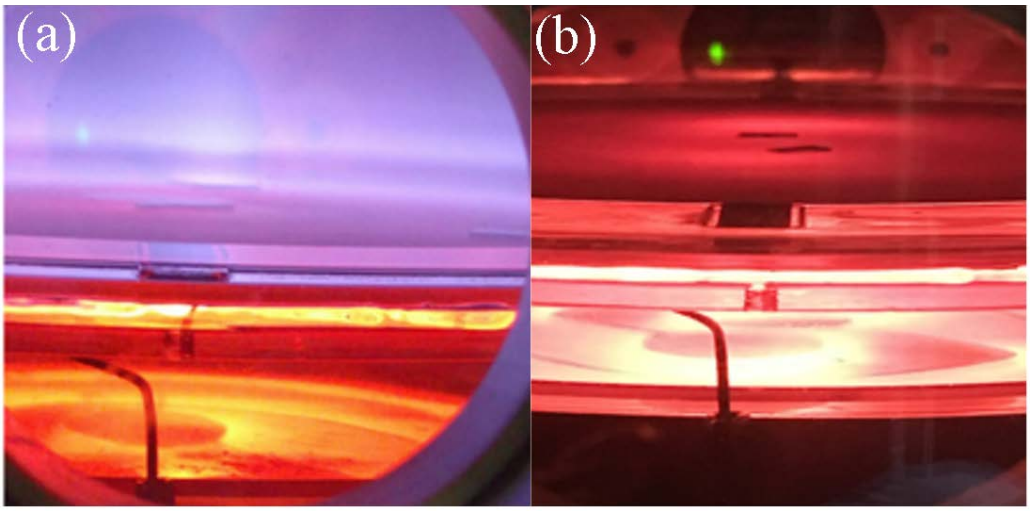

Figure 11: (a) Photo of the PECVD process in action. The orange glow is from the heater used to dewet the catalyst film to form nanoparticles. The purple haze is the plasma from gaseous species used for CNT growth. (b) Photo of the same reactor chamber as in (a) during the thermal CVD process. The red glow is from the same heater for catalyst film dewetting before growth on the substrates. In this case, however, the plasma envelope is no longer present during CNT growth.

Table 1: Summary of PECVD and thermal CVD growth processes, indicating their differences.

Step	Description	Key parameter values
1	Vent chamber	Pressure = 1000 mbar, Temperature ~ 40°C, gas flow = 0 sccm
2	Pump down chamber to pressure of .01 mbar	Temperature ~ 40°C, gas flow = 0 sccm
3	Introduce NH_3 and heat chamber to 700°C for catalyst film dewetting	NH_3 = 100 sccm, Temperature Ramp rate 325°C/min
4	Introduce C_2H_2 **For PECVD: Strike plasma at 800 V** **For CVD: No plasma**	NH_3 = 125 sccm, C_2H_2 = 31 sccm Temperature ~700-800°C
5	CNT growth step: **For PECVD: Maintain plasma** **For CVD: Maintain no plasma**	NH_3 = 125 sccm, C_2H_2 = 31 sccm Temperature ~700-800°C Time = 5 mins
6	Stop gas flows and heater power off	NH_3 = 0 sccm, C_2H_2 = 0 sccm Temperature 700-800°C Plasma = 0 V
7	Cooling step (using Ar gas)	NH_3 = 0 sccm, Ar = 2000 sccm, C_2H_2 = 0 sccm Temperature < 700°C
8	Retrieve sample from chamber	Pressure = 1000 mbar, gas flows = 0 sccm Temperature < 200°C

3.3 Process Characterization

Once fabrication of test devices is completed, we conduct a series of experiments aimed at characterizing the results of CNT growth on graphene. This includes SEM imaging, extraction of growth statistics, and electrical measurements. The instruments used in these experiments are available in the Center for Nanostructures on the SCU campus. From SEM images, data on CNT areal density, diameter distribution, and height distribution are obtained with visual observation as well as the use of available software for image analysis. Initial electrical measurements are taken using a wafer probe station. For confirmation and further investigation, a nanoprober inside the SEM chamber is employed to determine more accurately the I-V characteristics of the test devices, as well as to determine and image the precise locations of the measurements.

3.3.1 Electron Microscopic Analyses

One of the most critical instruments for characterizing our test devices is the SEM, which allows us to inspect structures one to two orders of magnitude smaller than the wavelengths of visible light, thus suitable for obtaining information from images of CNTs grown, ranging between 5 to 50 nm in diameter. The instrument is a Hitachi S-4800 SEM shown in Figure 12.

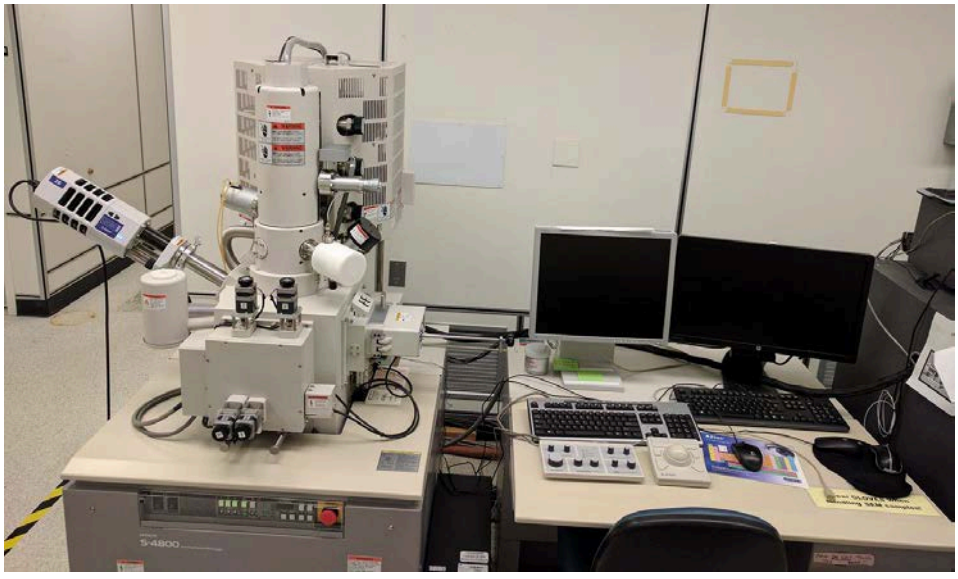

Figure 12: SEM in the Center for Nanostructures on the SCU campus. The module on the far left is an energy-dispersive x-ray (EDX) detector used to obtain elemental compositions of test samples.

For detailed information on properties of the nanostructure itself and the CNT-graphene interface, high-resolution, cross-sectional imaging using transmission electron microscopy (TEM) is needed. An example of such an image of CNT-Graphene interface from one of our test samples is shown in Figure 13, obtained by our collaborator, Dr. Phillip Wang of Applied Materials.

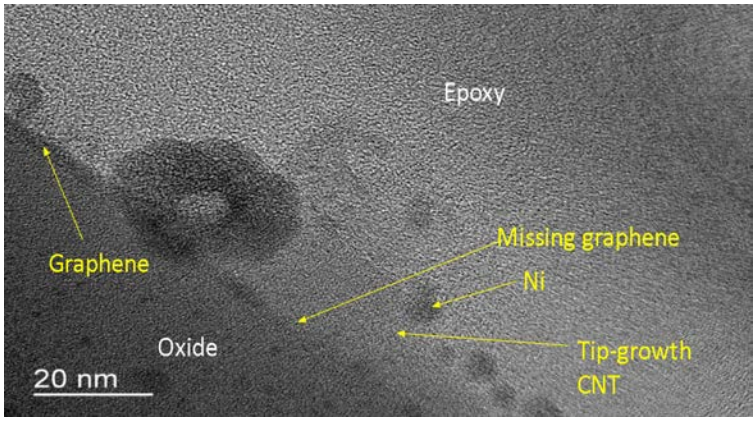

Figure 13: Cross-sectional TEM image of Ni-catalyzed CNTs on graphene. This was the image used to confirm destruction of graphene layers during the early stages of our project. The round dark spots are Ni particles, presumably from the CNT tips. Image show discontinuities in the graphene layer due to damage during the growth process [19].

3.3.2 Electrical Measurements

Another important property of the test device is its electrical behavior, which is measured using two different instruments. One such instrument is a wafer probe station, depicted in Figure 14, with the capability to probe individual regions of interest on a test sample and, together with a semiconductor parameter analyzer, to generate I-V characteristics. Using an optical microscope controlled through a computer, we can accurately collect visual and other data such as probe-probe separation for detailed analyses of test sample.

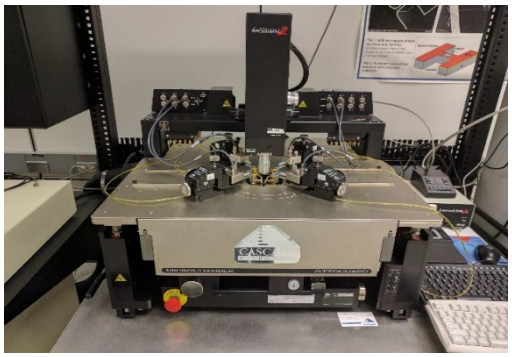

Figure 14: Wafer probe station used for preliminary electrical evaluation of our samples. This instrument features four-point probe capabilities, an optical microscope for precision measurements, and a pneumatic cushioning and vacuum system for stability.

In order to verify our wafer probing results, we use a highly precise nanoprober system shown in Figure 15. This instrument serves as a removable module for the SEM. By utilizing piezoelectric motors, it enables one to make very fine adjustments in electrical probe placement while measuring the I-V characteristics of the test device *in situ* inside the SEM

chamber under vacuum conditions. An example of such an experiment is given in Figure 16. With nanoprobe tips as small as 50 nm in diameter, we are able to obtain accurate and reliable electrical characteristics of individual CNTs.

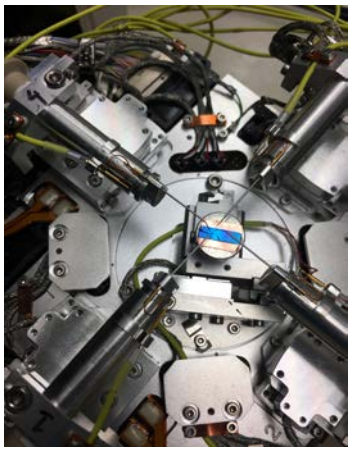

Figure 15: Nanoprober module consisting of four nanoprobes and highly precise motors and sensors to allow probing of individual CNTs.

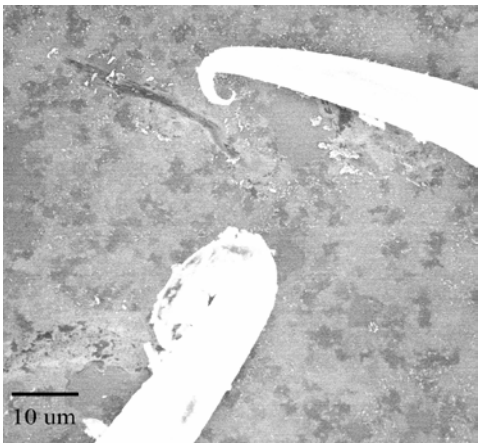

Figure 16: SEM image of nanoprobes (bright areas) landed on a CNT/Graphene sample.

Chapter 4: Results and Discussion

Throughout the course of this project, results on test devices have prompted detailed evaluation of the experimental parameters and their subsequent modifications. In particular, when a test device fails to show electrical behavior as expected, adjustments in CNT growth conditions and/or measurement setup are needed to yield desirable outcomes.

As part of our initial process design, we plan to vary the parameters of sputtering time and sputtering power in order to engage in a thorough investigation of the effects of catalyst thickness on CNT growth. In addition, we are concerned that a high sputtering power could damage or destroy the graphene layers. To address this concern, we carry out experiments using different catalysts with varying sputtering times and powers. After studying existing reports on the use of various catalysts for CNT growth [22] and based on research of past members of our team [25–28], we have selected Ni, Fe, and Co as catalysts. The outcomes from the use of each catalyst are summarized in Table 2.

Table 2: Comparison of CNT growth catalysts Ni, Fe, and Co.

CNT Growth Catalyst	Pros	Cons
Ni	-Reproducible CNT Growth -Successful fabrication of conductive all-carbon 3D structure	-Potential Damage to Graphene
Fe	-Reproducible CNT Growth -Promising preliminary electrical data	-Not viable for IC processing
Co	-Reproducible CNT Growth -Viable for IC processing -Successful fabrication of conductive all-carbon 3D structure	-Catalytic behavior for CNT growth on graphene not well established

The second major fabrication step involves adjusting specific parameters of the PECVD growth process and observing their effects on CNT growth. These parameters include volume of carbon source gas, strength of plasma envelope, time exposed to plasma, among others. The growth parameters for each catalyst are given in Tables 3-5. Finally, to prevent potential damage of graphene by the plasma, we utilize an alternative to PECVD by eliminating the gas discharge step, resulting in a thermal CVD process.

4.1 CNT Growth with PECVD

4.1.1 Nickel-Catalyzed Growths

Figure 17 shows the images of CNTs on graphene with a Ni catalyst film sputtered at 200 watts (W) for 150 seconds and grown using PECVD for 5 minutes. Figure 17(a) and (b) show a cross-sectional view and top view of the sample, respectively. The CNTs are vertically aligned, with an areal density ~10^9 /cm^2 and average diameter ~70 nm. This sample, along

with all others, is determined to be non-conducting, indicating potential problems with our growth process. A summary of the experiments for CNT growth on graphene as well as SiO_2 and their parameters is given in Table 3.

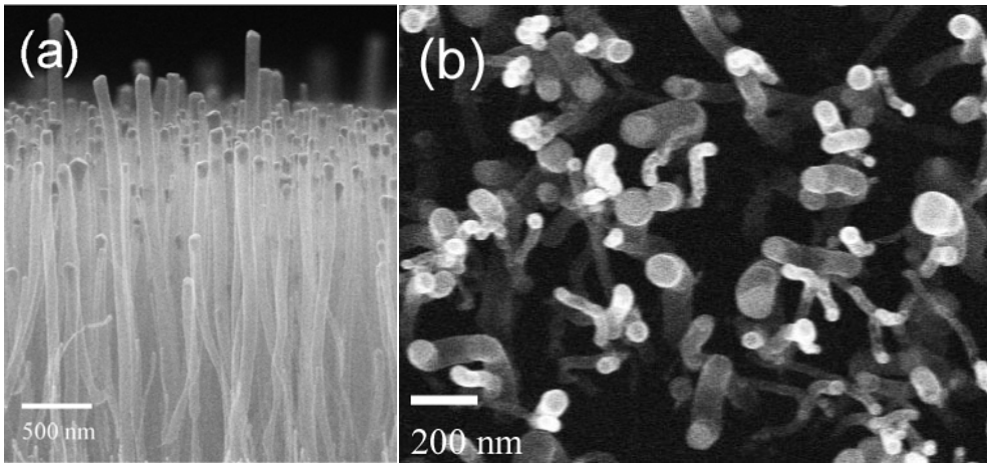

Figure 17: CNTs grown with sputtered Ni film at 200 W for 150 seconds and grown for 5 minutes using PECVD. (a) Cross-sectional view. Note the Ni nanoparticles (dark contrast) at the CNT tips (tip-growth). (b) Top view. The Ni nanoparticles (bright contrast) are visible at the CNT tips. CNT areal density ~10^9 /cm^2 and average diameter ~70 nm.

Table 3: Parameters for Ni-catalyzed CNT growth experiments using PECVD.

Substrate	Sputtering Power (W)	Sputtering Time (sec)	Growth Time (sec)	Notes
Silicon Dioxide	200	150	300	PECVD
Silicon Dioxide	200	150	300	PECVD
Silicon Dioxide	200	90	300	PECVD
Silicon Dioxide	200	75	300	PECVD
Graphene	200	120	120	PECVD: No NH_3
Graphene	200	120	120	PECVD: No NH_3
Graphene	200	120	300	PECVD: No C_2H_2
Graphene	200	120	600	PECVD
Graphene	200	120	600	PECVD: H_2 instead of NH_3

4.1.2 Iron-Catalyzed Growths

Figure 18 shows the cross-sectional and top-view images of CNTs grown on graphene with an Fe catalyst film sputtered at 100 W for 150 seconds and grown using PECVD for 10 minutes. A summary of the growth experiments and their parameters is given in Table 4. The results demonstrate the feasibility of CNT growth on SiO_2 as well as graphene with Fe catalyst using PECVD. As in the Ni case, however, all fabricated test structures are also non-conducting, further suggesting the need for adjusting the growth conditions. In addition, using Fe in any part of an IC fabrication process poses a problem for the on-chip devices, as it has a deleterious effect on their performance [29].

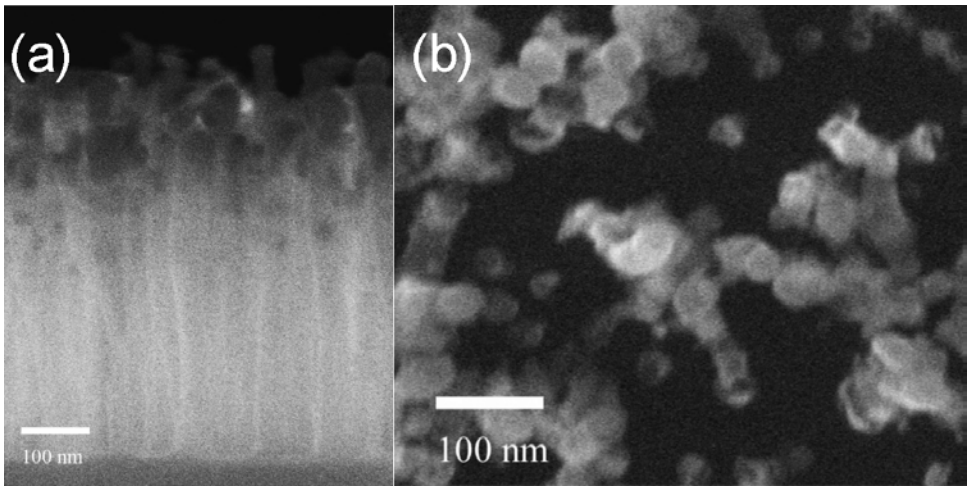

Figure 18: CNTs grown with sputtered Fe film at 100 W for 150 seconds and grown for 10 minutes using PECVD. (a) Cross-sectional view. Note the same tip-growth as Ni. (b) Top view. Fe nanoparticles are visible at the CNT tips. CNT areal density ~10^{10} /cm^2 and average diameter ~22 nm.

Table 4: Parameters for Fe-catalyzed CNT growth experiments using PECVD.

Substrate	Sputtering Power (W)	Sputtering Time (sec)	Growth Time (sec)	Notes
Silicon Dioxide	200	120	300	PECVD
Graphene	200	120	300	PECVD
Graphene	100	150	600	PECVD: Extra NH_3
Silicon Dioxide	100	150	600	PECVD: Extra NH_3
Silicon Dioxide	25	240	360	PECVD
Silicon Dioxide	25	240	360	PECVD
Silicon Dioxide	50	240	360	PECVD
Silicon Dioxide	50	240	360	PECVD
Silicon Dioxide	75	240	360	PECVD
Silicon Dioxide	75	240	360	PECVD
Silicon Dioxide	60	240	0	
Silicon Dioxide	60	240	360	PECVD
Silicon Dioxide	60	240	360	PECVD
Silicon Dioxide	75	180	Dewet catalyst film only	
Silicon Dioxide	75	180	240	PECVD
Graphene	75	180	360	PECVD
Silicon Dioxide	200	120	240	PECVD
Silicon Dioxide	200	120	240	PECVD

4.1.3 Cobalt-Catalyzed Growths

Figure 19 shows the cross-sectional and top-view images of CNTs grown on graphene with a Co catalyst film sputtered at 200 W for 120 seconds and grown using PECVD for 3 minutes. The results demonstrate the feasibility of CNT growth on SiO_2 as well as graphene with Co catalyst using PECVD. As in the previous experiments with Ni and Fe, however, the resulting test structures are also non-conducting, strongly suggesting that the problem lies with the growth conditions and not with the choice of catalyst.

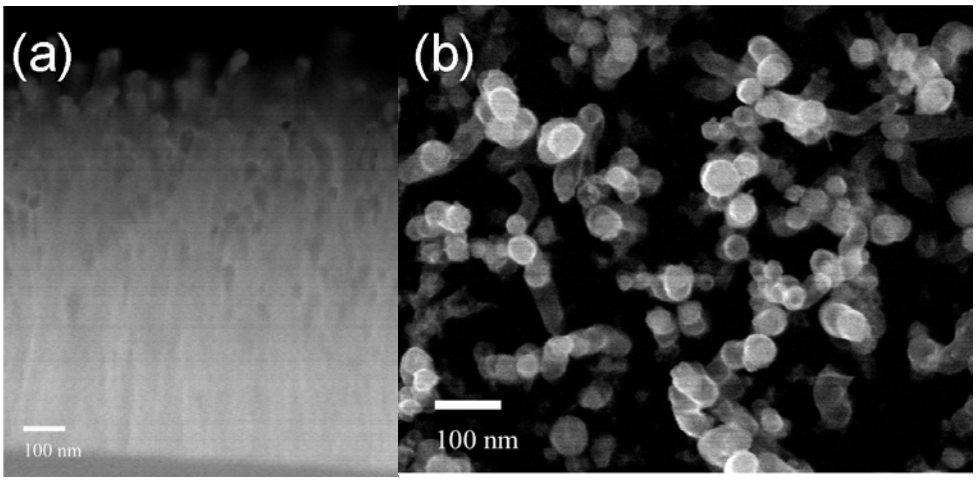

Figure 19: CNTs grown with sputtered Co film at 200 W for 120 seconds and grown for 3 minutes using PECVD. (a) Cross-sectional view. Note the same tip-growth as Ni and Fe. (b) Top view. Co nanoparticles are visible at the CNT tips. CNT areal density ~10^{10} /cm^2 and average diameter ~40 nm.

Table 5: Parameters for Co-catalyzed CNT growth experiments using PECVD.

Substrate	Sputtering Power (W)	Sputtering Time (sec)	Growth Time (sec)	Notes
Silicon Dioxide	200	90	360	PECVD
Silicon Dioxide	100	120	180	PECVD
Silicon Dioxide	200	120	360	PECVD
Silicon Dioxide	200	120	180	PECVD
Silicon Dioxide	200	120	180	PECVD
Silicon Dioxide	200	120	180	PECVD
Silicon Dioxide	200	120	180	PECVD
Silicon Dioxide	200	120	180	PECVD
Silicon Dioxide	150	120	180	PECVD
Silicon Dioxide	150	120	180	PECVD
Silicon Dioxide	100	150	180	PECVD
Silicon Dioxide	200	150	360	PECVD
Silicon Dioxide	200	150	180	PECVD
Graphene	100	120	180	PECVD
Graphene	150	120	180	PECVD
Graphene	200	120	180	PECVD
Graphene	100	120	180	PECVD
Graphene	150	120	180	PECVD
Graphene	200	120	180	PECVD

4.2 CNT Growth with Thermal CVD

As mentioned previously, the absence of an electric field in thermal CVD is expected to result in poor CNT alignment, if any at all. The CNTs grown are spaghetti-like and tangled together. As long as a sufficient number of CNTs make electrical contact with graphene and the electrical probe, however, there is conduction across the 3D structure. That being the case, the objectives of this project will be met.

4.2.1 Cobalt-Catalyzed Growths

We focus on Co as catalyst for CNT growth on graphene using thermal CVD, as the PECVD results show promise for the 3D structure and for the reasons given in Table 2. Figures 20 and 21 show the images of CNTs grown on graphene for 7 minutes through a thermal CVD process with a Co catalyst film sputtered at 75 W for 150 seconds and 75 W for 100 seconds, respectively. Both samples are conductive after CNT growth, indicating that we have successfully isolated the plasma in PECVD as the main source of graphene damage.

Based on multiple measurements across the sample, the average resistances for the fabricated CNT/Graphene structure shown in Figures 20 and 21 are 11.8 kΩ and 14.8 kΩ, respectively. The I-V behavior resulting from each two-point measurement is linear, giving further support for the existence of ohmic conduction across the entire structure and across the CNT-graphene interface as well. These results are encouraging compared to those obtained from PECVD grown CNTs on graphene, which show highly nonlinear I-V behavior with resistance values indicative of an open circuit. A summary of the growth experiments and their parameters is given in Table 6.

Combining these results with the fact that Co is currently used as an interconnect material in 10 nm technology node [30] further justifies the choice of Co as catalyst and enhances the prospect of a 3D CNT/Graphene structure as a potential interconnect building block.

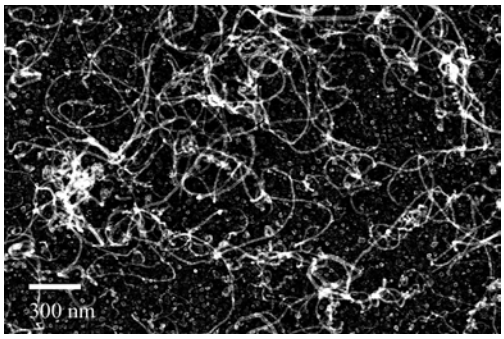

Figure 20: Top view of CNTs grown with sputtered Co at 75 W for 150 seconds and grown for 7 minutes using thermal CVD. CNT areal density ~10^{10} /cm^2 and average diameter ~19 nm.

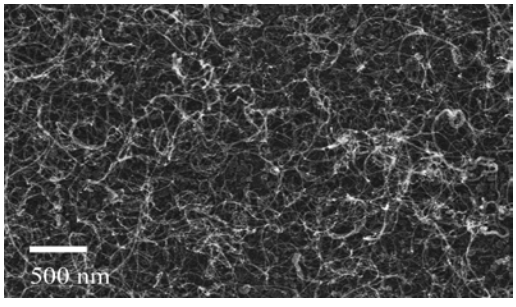

Figure 21: Top view of CNTs grown with sputtered Co at 75 W for 100 seconds and grown for 7 minutes using thermal CVD. CNT areal density ~10^{10} /cm^2 and average diameter ~19 nm.

Table 6: Parameters for Co-catalyzed CNT growth experiments using thermal CVD.

Substrate	Sputtering Power (W)	Sputtering Time (sec)	Growth Time (sec)	Notes
Graphene	200	120	180	CVD
Graphene	200	120	180	CVD: High Temp~785°C
Graphene	75	120	180	CVD
Graphene	120	120	420	CVD
Graphene	75	120	120	PECVD: 1 min, CVD: 1min
Graphene	75	150	140	PECVD: 20 sec, CVD: 2min
Graphene	75	150	420	CVD
Graphene	75	100	420	CVD 10 layer Gr
Graphene	75	100	420	CVD 10 layer Gr: Double C_2H_2

4.3 Electrical Measurements and Contact Resistance Extraction

Besides SEM imaging, the outcomes of CNT growth on graphene using thermal CVD are evaluated based on electrical characteristics of test devices. Using the wafer probe station, two-point electrical measurements are performed to obtain reproducible I-V behaviors from which the total device resistances are deduced. In addition, contact resistance is extracted from resistance versus probe-probe separation data based on the transfer length measurement (TLM) method [31]. For a CNT/Graphene structure, contact resistance consists of contributions from probe-graphene, probe-CNT, and CNT-graphene interfaces. The measurement schematic and TLM results for a graphene sample before CNT growth are shown in Figure 22. From the TLM plot, the extracted contact resistance (mainly from the probe-graphene contacts) is 2.5 kΩ.

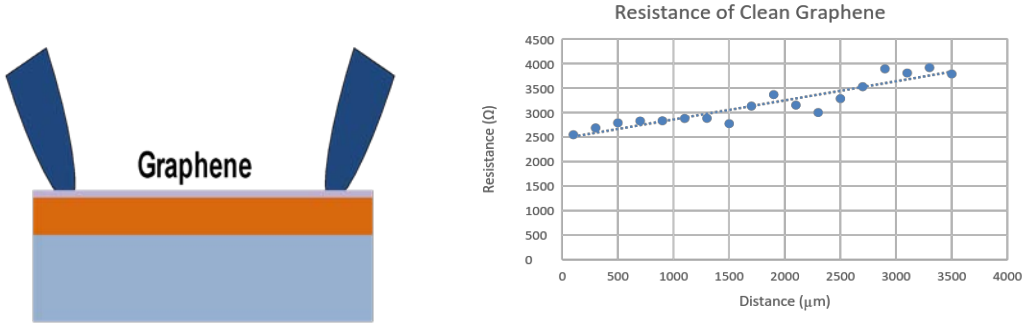

Figure 22: Electrical characteristics of graphene before CNT growth. Total probe-graphene contact resistance ~2.5 kΩ extracted from resistance vs probe-probe separation (distance).

After CNT growth on graphene, the sample undergoes similar electrical tests to obtain the graphene resistance to ensure that the graphene layers are not damaged during the growth process. The schematic for such tests and TLM results are shown in Figure 23 for the sample in Figure 20. The resistance values and the extracted contact resistance of 3.4 kΩ (compared with those in Figure 22 for a different "clean" graphene sample) suggest that the graphene suffers little or no damage during CNT growth. During the measurement, we exercise care to probe only the graphene layer in order to characterize its electrical behavior and to establish a

reference for subsequent probing of the CNT/Graphene structure. We then perform a series of measurements on the same sample as depicted in Figure 24 to characterize the electrical behavior of the 3D all-carbon structure.

A few measurements using the nanoprober on the same sample with the setup in Figure 24(a) are carried out, with resistance ranging from 32 kΩ to 133 kΩ. These are preliminary results which require extensive verifications in the future. Also, the nanoprobe contact resistances are expected to be considerably higher, accounting for the larger resistance values than those obtained using the wafer probe station. Nevertheless, they provide further evidence for the existence of a conduction path across the entire CNT/Graphene structure.

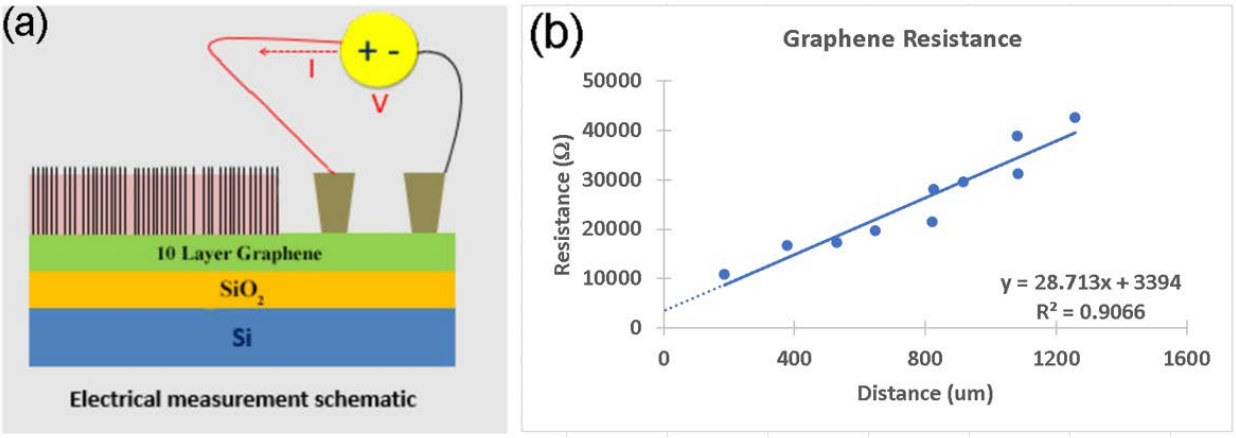

Figure 23: (a) Schematic for probing graphene after CNT growth. (b) Total probe-graphene contact resistance ~3.4 kΩ extracted from resistance vs probe-probe separation (distance), consistent with result obtained for pre-process graphene shown in Figure 22.

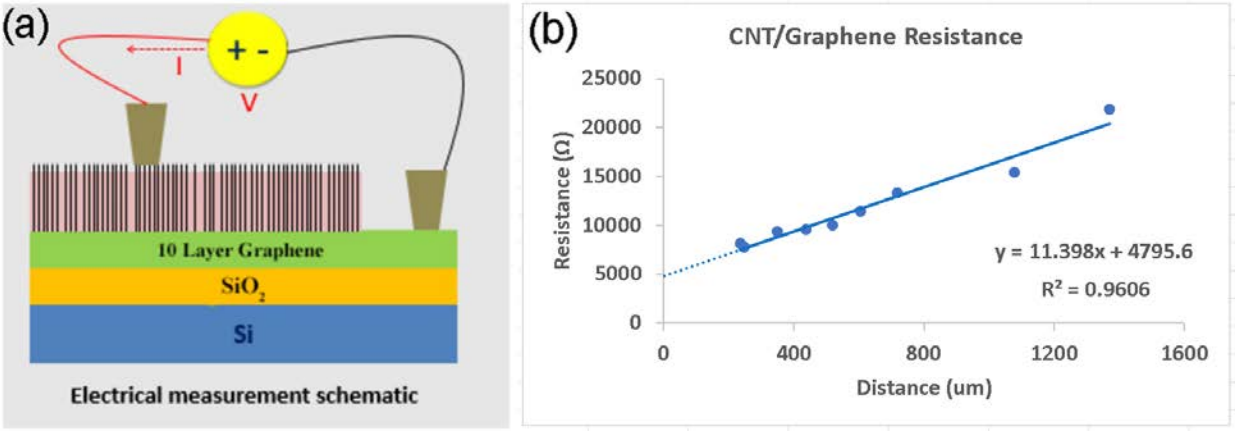

Figure 24: (a) Schematic for probing CNT/Graphene with one probe from setup in Figure 23 placed on CNTs while the other stays on the same area of "clean" graphene. (b) Total contact resistance R_c ~4.8 kΩ extracted from resistance vs probe-probe separation (distance).

Chapter 5: Final Design

5.1 Basis for Strategy Selection

We have demonstrated that Co is a viable catalyst for CNT growth on graphene using a thermal CVD process. Unlike Fe, Co is compatible with and being used in current IC process technology. Therefore, we focus primarily on cobalt as the catalyst for CNT growth.

5.2 Analysis of Final Design

While both Co samples shown in Figures 20 and 21 manifest electrical conduction after CNT growth, we focus on the former for the ensuing analysis based on the results shown in Figures 23 and 24. Since our goal is to create an all-carbon 3D structure with a resistance similar to that of graphene, we first carry out two-point measurements (using a setup shown in Figure 22(a)) for a "clean" graphene sample. This results in a resistance of 3.2 kΩ, with probes landing on specific locations. After CNT growth on the same sample and ensuring to probe the same locations with the same probe separation as before, we obtain a resistance of 3.3 kΩ. These results confirm that the CNT growth creates little damage on the multi-layer graphene, allowing us to proceed with the analysis of electrical data on the CNT/Graphene structure.

The schematic for measuring CNT/Graphene electrical characteristics and the results from these measurements are shown in Figure 24. Here the challenge in probing lies in landing one probe on CNTs only to ensure the conduction path is through CNTs and across the CNT-graphene interface while the other probe remains on the same area of "clean" graphene (as in the measurement illustrated in Figure 23(a)). The extracted contact resistance of 4.8 kΩ consists of contributions from one probe-graphene contact, one probe-CNT contact, as well as the CNT-graphene interface. Using the extracted contact resistance of 3.4 kΩ obtain from the linear fit in Figure 23(b), and assuming both probe contacts are identical, a contact resistance of 1.7 kΩ between a single probe and graphene is obtained. Thus, the (probe-CNT + CNT-graphene) contact resistance is (4.8 kΩ – 1.7 kΩ) = 3.1 kΩ.

The probe-CNT contact varies widely among measurements due to surface asperities of the probe and unaligned CNTs, but as a first-order approximation, we assume that probe-CNT contact resistance is *at best* the same value as that of the probe-graphene (but is likely to be higher). Thus, the resistance attributed to the CNT-graphene interface is estimated to be *at most* (3.1 kΩ – 1.7 kΩ) = 1.4 kΩ.

While these results are preliminary, they nonetheless indicate the existence of a conduction path through the 3D CNT/Graphene structure. Verifications of these results require extensive nanoprobing inside the SEM chamber since the nanoprobes are much smaller, making it more likely to land on CNTs only (without contacting the graphene underlayer). Further, since nanoprobing allows *in situ* experimentation, the location where the nanoprobe lands on the tangled CNT arrays can be precisely determined.

The results and analysis show that we have met our objective of fabricating an all-carbon 3D interconnect structure with carbon nanotubes grown directly on graphene, with the resulting CNT/Graphene resistance similar to that of pre-process graphene. We are further verifying these results by nanoprobing the same and additional samples and along with our collaborators, who will carry out TEM and related analyses to characterize the CNT-graphene interface to confirm that we have created a homogeneous all-carbon structure.

5.3 Bill of Materials

The materials required for this project are provided by the TENT Laboratory.

- Silicon wafers with graphene layers
- Growth catalyst sputtering targets
- Methane gas
- Ammonia gas
- Acetylene gas
- PECVD reactor

5.4 Project Timeline

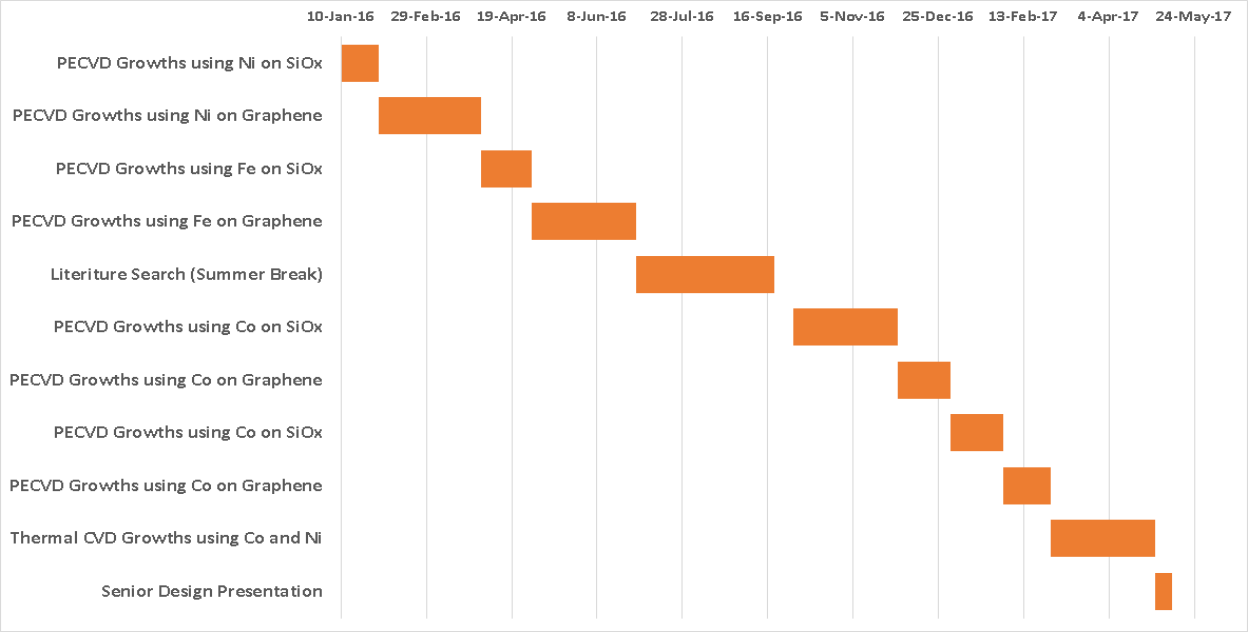

Figure 25: Gantt chart of our project timeline containing the tasks and experiments performed over its duration.

Chapter 6: Professional Issues and Constraints

6.1 Ethical Analysis

Any scientific and technological undertaking can be continuously debated as "potentially unethical" through extreme examples (e.g. drone technology is harmful since it can be used to violate privacy). With that in mind, it is hard to come up with unethical aspects about this research because the goal is to ensure IC technology can continue to advance and benefit society. This is valid so long as the tools, materials, and data used are not acquired through unethical means such as plagiarism or endangering the well-being of others. Though there are potential safety concerns when utilizing processes that involve nanomaterials and various chemicals, without malicious intent the project can be conducted ethically. As technical professionals, we carry out all our experiments with extreme care to ensure the safety of everyone and the integrity of equipment and facility.

6.2 Science, Technology, and Society

The processes used in fabricating our devices are potentially transferable to production. We have designed our processes to be compatible with current IC technology so that such a transfer can occur in the future. Furthermore, as a replacement for existing interconnect materials, the impact on IC technology development and the subsequent manufacture would have far-reaching societal implications in terms of equipment and labor cost. One potential concern is the fact that use of nanocarbons in actual products is not extensive, therefore their impact on the environment and human health is not fully known. Nevertheless, we take great care in handling these materials and expect more information on such potential impacts will be available in the coming years.

6.3 Economic Implications

In order to provide the demand for smaller and more efficient electronic devices, manufacturers have been continually investing in more expensive processes and equipment due to the limitations of using Cu and W in integrated circuits [32]. As the cost of manufacturing increases, it is felt by both the manufacturer and the consumer. For this reason, replacing Cu and W as interconnect materials may have far-reaching economic implications.

6.4 Health and Safety and Environmental Impact

As is a concern with any substance, it is important to consider the amount and/or concentration. Our project focuses on potential new technology to replace the Cu and W interconnects *inside* integrated circuits. Many modern technologies and products include harmful materials to which the consumer is generally not expected to be exposed. The silicon chips in many electronic systems in particular, contain trace amounts of arsenic that is crucial to the chip's operation, though it is not expected any user will be exposed to it. Since any IC is

packaged and hermetically sealed by the time it reaches a consumer, we do not anticipate any adverse health effects as a result of our technology if it becomes commercialized. Even if a consumer were to go out of their way to dismantle the chip package, it is unlikely they will come under any harmful exposure due to the minute amount of nanocarbon material. As mentioned above, additional knowledge on environmental and health impacts in the future would lead to better handling in manufacturing as well as a better-informed public.

6.5 Manufacturability, Usability, Sustainability, and Civic Engagement

The declining reliability and performance of Cu and W interconnects in advanced IC technology are the main issues in chip manufacturing that we set out to address. By presenting nanocarbons as a more reliable and potentially higher performing alternative, the technology can continue to follow Moore's law into sub-10 nm technology nodes. As with any new technology, competing products and technologies must be taken into account. Due to the potential ground-breaking nature of our research and the current alternatives considered by the IC industry, however, it is reasonable to expect that nanocarbons will remain a contender to replace Cu and W in the foreseeable future. Furthermore, while the potential of nanocarbons in the biomedical industry for applications such as implantable devices is outside the scope of this project, the ability to improve chip reliability and performance is a crucial step towards developing better medical devices. This may lead to a reduction in health care costs, which is a major issue throughout the world.

Regardless of the potential benefits of any new electronic technology, proper disposal of devices and systems is a very important aspect of electronic waste management and must be considered in product manufacturing. This importance is manifested in the many established methods for safely recycling and disposing of electronic parts. Fortunately, the waste disposal and processing for our devices are identical to those already in place. Part of this stems from the fact that the process developed in our project can be readily integrated into current manufacturing and product handling practices, including waste disposal and recycling.

Chapter 7: Conclusions and Future Work

7.1 Summary and Conclusions

The objective of this senior project is to design a process that results in a conductive all-carbon 3D interconnect structure with carbon nanotubes attached to a multi-layer graphene. This work is motivated by the need of current IC technology to eventually replace Cu and W as interconnect materials. Our experimental process first involves using a plasma-enhanced chemical vapor deposition process to grow CNTs directly on a graphene-covered silicon substrate after sputtering a thin layer of Ni, Fe, or Co catalyst film. The PECVD process turns out to result in non-conductive CNT/Graphene structures due to damages in the graphene during CNT growth. To mitigate this challenge, we successfully identified the source for graphene damage as the plasma in the CNT growth process and, as a result, replaced PECVD with thermal CVD in our growth process. The results for the CNT/Graphene devices fabricated using Co catalyst are encouraging with an estimated CNT-graphene contact resistance of 1.4 kΩ. Thus, we have taken the first step in demonstrating electrical conduction through a 3D all-carbon nanostructure fabricated by growing CNTs directly on graphene. While further fabrication and characterization experiments are needed to verify the results and improve on them, our objective has been met and the project has served to open up opportunities for other researchers in the future.

7.2 Future Work

We have planned a series of experiments to be carried out in the coming months to verify the results so far and to take the next steps in developing the CNT/Graphene process. Specific tasks are listed below.

1. Verify all electrical measurement results with nanoprobing.
2. Demonstrate continuous sp^2 bonding across CNT-graphene interface using TEM and related techniques in our collaborators' laboratories.
3. CNT/Graphene growth using thermal CVD at 700℃ with various Co and Ni sputtering conditions to provide more samples to confirm conduction.
4. Vary growth conditions to improve CNT alignment while preserving or enhancing conduction of CNT/Graphene structure.
5. Lower CNT growth temperature to <600℃ to be more compatible with IC fabrication process without increase in CNT/Graphene resistance.

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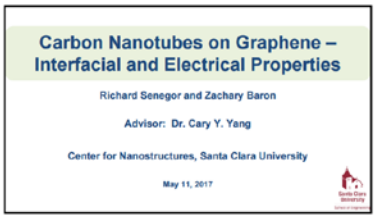
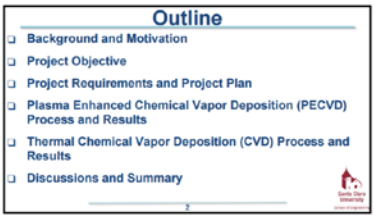
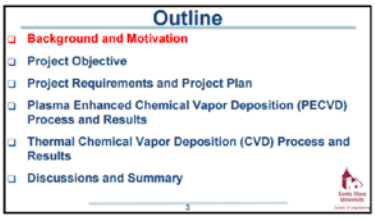
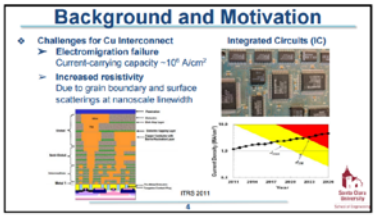
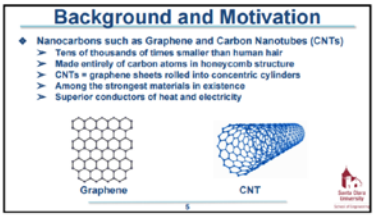
Appendix A: Senior Design Conference Slides as Presented

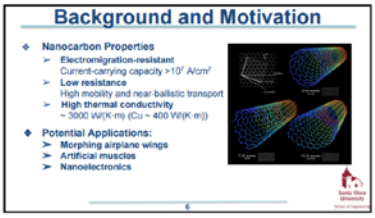


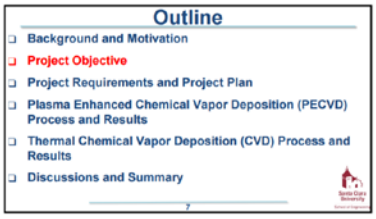


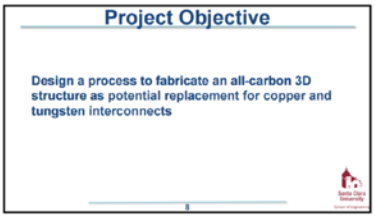


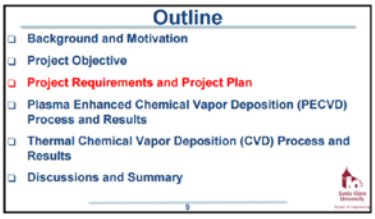






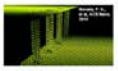






Project Requirements

- Reduce contact resistance by attempting to form C-C sp^2 bonds at CNT/graphene interface to achieve overall resistance comparable to graphene



- Create an all-carbon 3D interconnect structure consisting of CNTs grown on graphene
  - Sputtering for catalyst film deposition
  - Plasma Enhanced (PE) or Thermal Chemical Vapor Deposition (CVD) for CNT growth

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Test Structure Fabrication

- Graphene Growth

Temperature: 900°C
Ni thickness: 300nm

- Graphene Transfer onto Oxide

- CNT Growth on Graphene

Temperature: 700°C
Catalyst thickness <10nm

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Instruments for CNT Growth Characterization

Scanning Electron Microscope (SEM) | Wafer Probe | Nanoprober

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Outline

- ❑ Background and Motivation
- ❑ Project Objective
- ❑ Project Requirements and Project Plan
- ❑ Plasma Enhanced Chemical Vapor Deposition (PECVD) Process and Results
- ❑ Thermal Chemical Vapor Deposition (CVD) Process and Results
- ❑ Discussions and Summary

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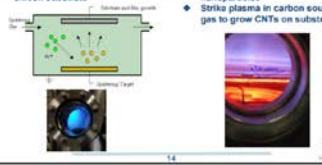
PECVD

- Sputter catalyst (Ni, Fe, Co) film on silicon substrate
- Dewet catalyst film to form nanoparticles
- Strike plasma in carbon source gas to grow CNTs on substrate



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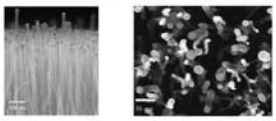
CNTs on Graphene (PECVD, Ni Catalyst)



- Proven catalyst for CNT growth
- High-quality CNTs
- Non-conductive graphene post-growth

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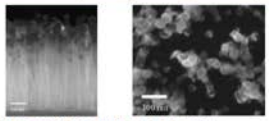
CNTs on Graphene (PECVD, Fe Catalyst)



- Proven catalyst for CNT growth on metal
- Not compatible with IC fabrication
- Non-conductive graphene post-growth

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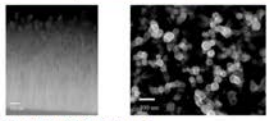
CNTs on Graphene (PECVD, Co Catalyst)



- Compatible with IC fabrication
- Demonstrated CNT growth
- Non-conductive graphene post-growth

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Outline

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PECVD

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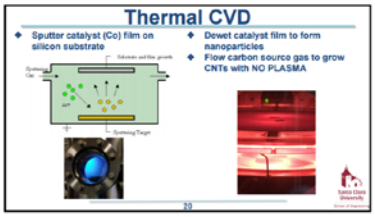
Thermal CVD

- Sputter catalyst (Co) film on silicon substrate
- Dewet catalyst film to form nanoparticles
- Flow carbon source gas to grow CNTs with NO PLASMA



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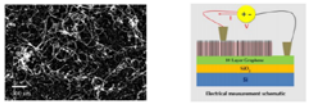
CNTs on Graphene (CVD, Co Catalyst)



Average CNT/Graphene Resistance: 774Ω

Resistance Measurements (Fixed Probe Distance)
Pre-Process Graphene: 320Ω
Post-Process CNT/Graphene Structure: 331Ω

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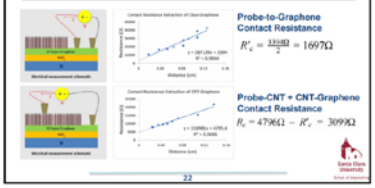
Resistance Measurements



Probe-to-Graphene Contact Resistance

$R'_c = \frac{321\Omega}{2} = 169.7\Omega$

Probe-CNT + CNT-Graphene Contact Resistance

$R_c = 479.6\Omega - R'_c = 309.9\Omega$

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Discussions

- Integrability of all-carbon structure into IC fabrication
- Impact on future nanoelectronics
- Health and environmental effects of nanocarbons

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Summary

- Current advanced IC technology needs alternatives to Cu interconnects, nanocarbons being the most promising candidates
- All-carbon 3D interconnect structure consisting of CNTs grown on graphene results in resistance comparable to graphene
- CNT growth process design using various catalysts: Ni, Fe, Co
- Demonstrated conduction in all-carbon 3D structure using Co

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Thank you !

References

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- G. Soldano, S Tellapatna, S. Kar, "Carbon Nanotubes and Graphene Nanoribbons: Potential for Nanoscale Electrical Interconnects," Electronics 2013 2(3), 280-314
- Kreupl F, Graham A P, Duesberg G, Steinhögl W, Liebau M, Unger E and Hönlein W 2002 Carbon nanotubes in interconnect applications Microelectronic Engineering 64 399-408
- Coiffic J, Fayolle M, Le Poche H, Maitrejean S and Olivier S 2008 Realization of via interconnects based on Carbon Nanotubes/Buriingame, CA: IEEE International Interconnect Technology Conference) p 153-5

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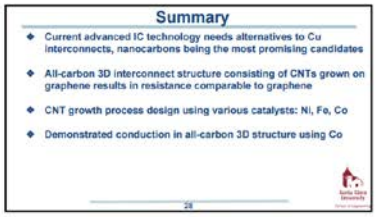
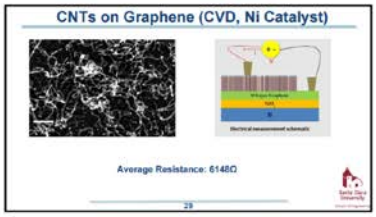
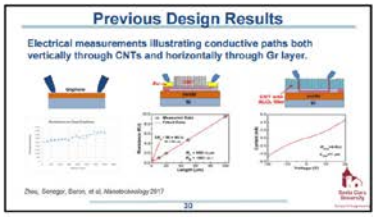
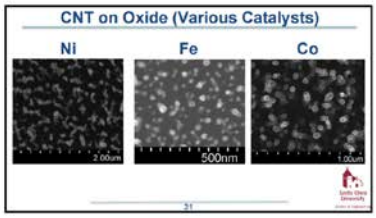
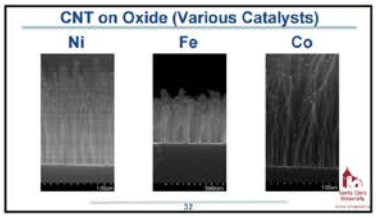
Additional prepared slides (not presented):

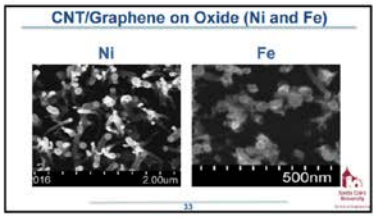


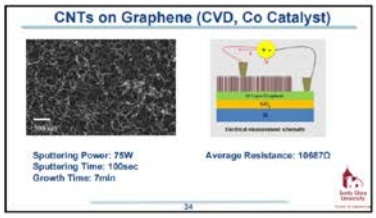


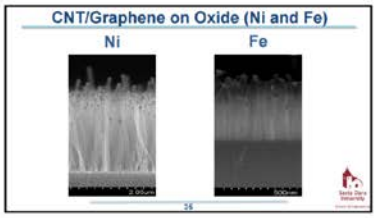


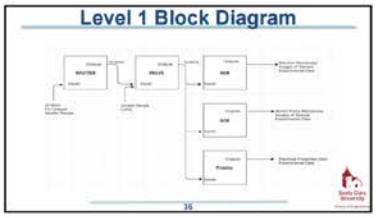


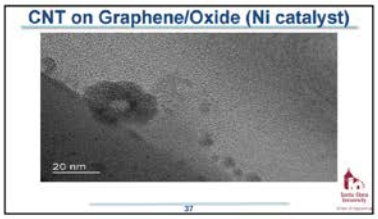


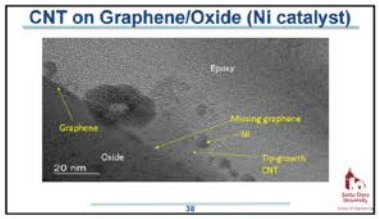


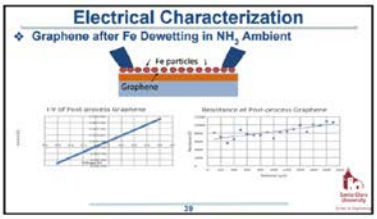


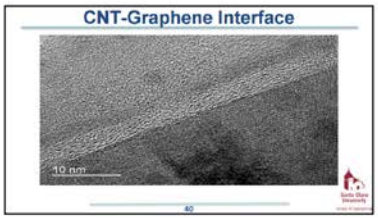


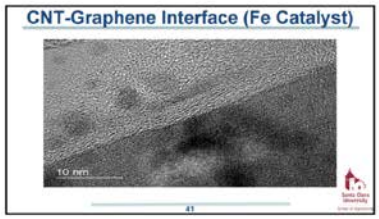


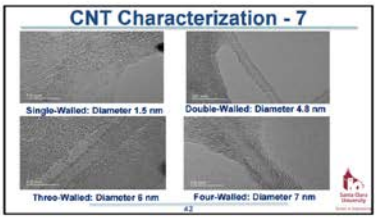




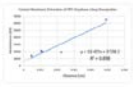








Nanoprobing Resistance Measurements



Probe to Graphene Contact Resistance

$$R_{c'} = \frac{339\Omega}{2} = 169.7\Omega$$

Probe to CNT-Graphene Contact Resistance

$$R_c = 5728\Omega - R_{c'} = 4031\Omega$$

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Appendix B: Additional SEM Information

Detailed information on the construction and use of our Hitachi S-4800 scanning electron microscope is available at the following URL:
http://cmrf.research.uiowa.edu/sites/cmrf.research.uiowa.edu/files/S-4800%20Instruction%20Manual_1.pdf

Appendix C: Additional Wafer Prober Information

Detailed information on the construction and use of our Cascade Microtech wafer probe station is available at the following URL:
https://www3.nd.edu/~nano/facilities/at_man_Cascade12000SemiAutoProbe_Nucleus_Manual.pdf

Appendix D: Additional Nanoprober Information

Detailed information on the construction and use of our Zyvex S200 nanoprober is available at the following URL:
http://www.zyvex.com/Documents/S200.pdf