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Inversion in the $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor system: impact of the $In_{0.53}Ga_{0.47}As$ doping concentration

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$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) capacitors with Al_2O_3 gate oxide and a range of *n* and *p*-type $In_{0.53}Ga_{0.47}As$ epitaxial concentrations were examined. Multi-frequency capacitance-voltage and conductance-voltage characterization exhibited minority carrier responses consistent with surface inversion. The measured minimum capacitance at high frequency (1MHz) was in excellent agreement with the theoretical minimum capacitance calculated assuming an inverted surface. Minority carrier generation lifetimes, τ_g, extracted from experimentally measured transition frequencies, ω_m, using physics based a.c. simulations, demonstrated a reduction in τ_g with increasing epitaxial doping concentration. The frequency scaled conductance, G/ω, in strong inversion allowed the estimation of accurate C_{ox} values for these MOS devices.

Historically, a variety of issues have impeded progress for the incorporation of high-*k* dielectrics on III-V semiconductors for future CMOS applications.[1,2] Not least among these is the complexity of the high-k III-V interface which typically has a high density of electrically active defects. [3,4,5] Interface state density (D_{it}) values in excess of $10^{12}cm^{-2}$ are commonly reported which is almost two orders of magnitude higher than that achievable in SiO_2/Si systems. Passivation of these defects to acceptable levels has not proved to be trivial and also renders reliable characterization and interpretation of device behavior difficult.[6] Such a high D_{it} can restrict Fermi level movement across the semiconductor bandgap and in the case of $In_{0.53}Ga_{0.47}As$, prevent surface inversion at the semiconductor/oxide interface. To date, only a limited number of studies in the literature have demonstrated sufficient reduction in D_{it} to allow the observation of true surface inversion and an associated minority carrier behavior, in the capacitance-voltage (CV) response of MOS capacitors on either *n*-type or *p*-type $In_{0.53}Ga_{0.47}As$.[7, 8, 9, 10]

In recent work we reported on a study of the minority carrier response of both *n*-type and *p*-type $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) devices formed using an optimized 10% ammonium sulfide ($(NH_4)_2S$) treatment.[7] D_{it} was sufficiently reduced such that a clear minority carrier response associated with inversion of the oxide/$In_{0.53}Ga_{0.47}As$ surface was observed for both *n*-type and *p*-type devices. In order to extend this work, in this letter we present a method to confirm true surface inversion in $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitors based on the use of a wide range of *n* and *p*-type doping concentrations, ranging over two orders of magnitude from ~$1x10^{16}cm^{-3}$ to ~$2x10^{18}cm^{-3}$. This is in order to examine if the measured minimum capacitance scales correctly with the $In_{0.53}Ga_{0.47}As$ doping concentration based on a maximum depletion width calculated assuming the surface is inverted. This follows an approach reported by Callegari *et al* for GaAs MOS devices.[11] In addition the effect of the doping concentration on the minority carrier generation lifetime in the $In_{0.53}Ga_{0.47}As$, τ_g, is examined. Finally, for these variable doping series samples, we utilize a recently reported method[12] to accurately estimate oxide capacitance, C_{ox}, where it was found that the peak magnitude of the angular frequency scaled conductance, G/ω, was equal to $C_{ox}^2/2(C_{ox}+C_D)$, in strong inversion, where C_D is the semiconductor depletion capacitance.

The details of the $In_{0.53}Ga_{0.47}As$ epitaxial layers used in this work are as follows. Firstly, using *p*-doped (Zn at ~$2x10^{18}$ cm^{-3}) InP(100) as a starting substrate, ~2μm *p*-$In_{0.53}Ga_{0.47}As$ layers were grown by MOVPE with the following dopant (Zn) concentrations (cm^{-3}): $1.4x10^{16}$, $3.3x10^{16}$, $1.8x10^{17}$, $2.7x10^{17}$, and $2.0x10^{18}$. Using *n*-doped (S at ~$2x10^{18}$ cm^{-3}) InP(100) as a starting substrate, ~2μm *n*-$In_{0.53}Ga_{0.47}As$ layers were grown by MOVPE with the following dopant (Si) concentrations (cm^{-3}): $7.8x10^{15}$, $3.0x10^{16}$, $2.0x10^{17}$, $6.0x10^{17}$, and $2.0x10^{18}$. These doping concentrations were determined by Electrochemical Capacitance-Voltage (ECV) Profiling. $In_{0.53}Ga_{0.47}As$ surfaces were initially rinsed for 1 minute each in acetone, methanol, and isopropanol, immediately followed by immersion for 20 minutes at room temperature in $(NH_4)_2S$ with a concentration of 10% in deionised H_2O. These optimized passivation parameters were determined from previous physical and electrical studies[13,14] and subsequently also reported for MOSFET devices.[15] The Al_2O_3 layers were grown by atomic layer deposition (ALD) at 300^oC (Cambridge NanoTech, Fiji F200LLC), using alternating pulses of TMA ($Al(CH_3)_3$) and H_2O. TEM indicated an Al_2O_3 thickness of ~ 7nm for the growth run on *p*-type samples and a thickness of ~ 5nm for the separate ALD growth run on *n*-type samples. Finally, gate contacts ~

160 nm thick were formed by e-beam evaporation of Ni (70nm), and Au (90nm), using a lift-off process. Electrical measurements were recorded using an Agilent E4980A, and were performed on-wafer in a microchamber probe station (Cascade, Summit 12971B) in a dry air, dark environment (dew point ≤203K).

For an MOS device in strong inversion the depletion layer width reaches a maximum value, which is related to the doping concentration and the relative permittivity of the semiconductor.[16] The equation governing the maximum depletion width, included here for completeness, is given in Equation [1] below where: ε_0 is the permittivity of free space; ε_s is the semiconductor permittivity; k is Boltzmann's constant; n_i is the intrinsic semiconductor carrier concentration; N_D is the semiconductor doping concentration.[17]

$$x_{d\_max} = \sqrt{\frac{4\varepsilon_0 \varepsilon_S kT \ln\left({N_D}/{n_i}\right)}{q^2 N_D}} \qquad [1]$$

From this equation, as the semiconductor doping level is increased this maximum depletion width is reduced, which in turn is reflected in an increase in the depletion capacitance (C_D) of the semiconductor in inversion. The theoretical minimum capacitance ($C_{min\text{-}theor}$) of a gate stack is the series combination of C_D and C_{ox}. It is thus expected that for an inverted surface, the minimum measured gate stack capacitance ($C_{min\text{-}meas}$) will increase as a function of doping concentration. Utilizing different doping concentrations $C_{min\text{-}meas}$ at high frequency can be compared with $C_{min\text{-}theor}$ as calculated by assuming the semiconductor surface is inverted. In the case of devices where the D_{it} is high, Fermi level movement will be restricted such that it will not be possible to reach the minimum capacitance. Where substrates with variable doping levels are available this provides a means to investigate if the oxide-semiconductor interface state concentration has been reduced to levels which allow surface inversion to be achieved. This approach was used previously for GaAs MOS structures to investigate improvements in the CV characteristics of plasma deposited Ga oxide films on GaAs substrates.[11]

Figure 1(a) plots the 1 MHz CV responses for the *p*-type $In_{0.53}Ga_{0.47}As$ MOS devices with varying dopant concentrations. The 1 MHz curves were chosen in order to minimize any contribution of interface states to the measured CV response. Open symbols represent $C_{min\text{-}theor}$ for each doping concentration and calculated using a C_{ox} value in this case of 0.0075 F/m^2, taken from the measured capacitance at low frequency (20 Hz), and at a gate bias of 1.75V. C_{ox} was chosen at 20Hz as this was the lowest frequency that could be measured with the instrument used, and previous work has shown that the CV at 20Hz provides a very close approximation to the C_{ox} obtained using a quasi-static CV.[18] It is clear that the measured minimum capacitance increases as expected with doping and that there is excellent agreement between the measured and theoretical minimum capacitance values, providing strong evidence that the $In_{0.53}Ga_{0.47}As$ surface is inverted. This is notable considering that the change in doping concentration is over two orders of magnitude. It is also significant that the measured CV curves go flat with increasing positive gate bias, which is further support that D_{it} has been reduced to an extent to allow sufficient Fermi level movement that permits surface inversion. Figure 1(b) shows the 1 MHz CV responses for the *n*-type $In_{0.53}Ga_{0.47}As$ MOS devices with changing epitaxial layer dopant concentrations. As in the case of the *p*-type samples, there is excellent agreement between the measured (open symbols) and theoretical (closed symbols) capacitance values. The theoretical minimum capacitance, $C_{min\text{-}theor}$, for each doping concentration was calculated using a C_{ox} value in this case of 0.0093 F/m^2, taken from the capacitance measured at low frequency (20Hz), and at a gate bias of -3.75V. When plotting the measured capacitance versus the theoretical value, (@1.75 V_{gate} for *p*-type and at @-3.75V_{gate} for *n*-type), Figure 2 demonstrates that there is close to a linear relationship in both cases. The inversion of the *n*-type $In_{0.53}Ga_{0.47}As$ MOS is of particular note, as for the Al_2O_3/ $In_{0.53}Ga_{0.47}As$ MOS system the interface state density is generally reported to rise steeply towards the valence band edge,[19,20,21] and the ability to invert the Al_2O_3/*n*-InGaAs surface indicates that the surface preparation and ALD growth conditions have not only reduced D_{it} near the mid gap energy, but also results in D_{it} reduction from mid-gap to the valence band edge.

For all samples the multi-frequency CV and GV responses (20 Hz to 1 MHz) also exhibited the characteristic signatures of inversion behavior for $In_{0.53}Ga_{0.47}As$ MOS devices.[7] As an example illustration the CVs in Figure 3(a) and (b) are plotted for the devices in this study ($1.8x10^{17}$ *p*-type and $6.0x10^{17}$ *n*-type) having doping levels similar to those used in previous reports on inverted $In_{0.53}Ga_{0.47}As$ MOS devices, in order to show the behavior is consistent.[7,22] Space limitations preclude showing the multi-frequency CV for all samples. One of the signatures for an inverted surface is that in strong inversion the measured conductance normalized by frequency, G/ω, peaks at the transition frequency, ω_m.[7,12,23] This relationship is observed for all samples in the study (not shown).

For an inverted surface the multi-frequency C-V and G-V responses can also be used to investigate the minority carrier lifetime in the $In_{0.53}Ga_{0.47}As$ layer and the capacitance of the gate oxide.[12,22] For the case of surface inversion, the transition frequency, ω_m, is inversely related to the minority carrier generation lifetime, τ_g, in the $In_{0.53}Ga_{0.47}As$, and the peak value of G/ω is related to the oxide capacitance, C_{ox}. Considering firstly the case of the minority carrier lifetime, the G/ω recorded at a gate bias of 1.75 V_{gate} for *p*-type and at -3.75V_{gate} for *n*-type are plotted in Figure 4. One observation of note over both *n* and *p*-type samples in Figure 4 is that the transition frequency at which G/ω peaks in inversion increases as the semiconductor doping concentration is increased. Figure 5(a) plots this change for *p*-type and *n*-type devices. For a minority carrier supply provided through mid-gap state generation, this behavior is expected as the minority carrier lifetime τ_g values generally decrease with increasing doping concentration. These observations are therefore consistent with previous work on similar device structures indicating that at room temperature the dominant mechanism for the supply of minority carriers is a generation-recombination process through mid-gap bulk defects in the $In_{0.53}Ga_{0.47}As$ depletion region.[7] These results are not consistent with a border trap[24] contribution to the observed minority carrier response. The results in Figure 5(a) also indicate that at similar doping levels the transition frequency for the *n*-type samples is generally one order of magnitude higher than for the corresponding *p*-type samples.

A Synopsis Sentaurus device simulator was employed to perform physics based ac simulations, where the value of τ_g in the simulations is altered to achieve a match between the transition frequency of the physics based ac simulations and the experimental transition frequency values in Figure 5(a). The resulting τ_g are plotted in Figure 5(b) demonstrating a marked decrease with increasing doping concentration for both *n* and *p*-type devices. The fact that higher generation lifetimes at similar doping levels are observed for *p*-type compared to *n*-type samples is possibly related to inequalities in the bulk $In_{0.53}Ga_{0.47}As$ properties arising from differences in the epitaxial growth conditions for the *p* and *n*-type $In_{0.53}Ga_{0.47}As$ layers. However, further analysis of this is beyond the scope of the current study. Previous work also demonstrated that it is possible to passivate some of the bulk mid-gap traps in $In_{0.53}Ga_{0.47}As$ through H_2/N_2 annealing, as indicated by an increase in τ_g.[22,25] It is noted that all samples in each doping series in this work were processed simultaneously with the $In_{0.53}Ga_{0.47}As$ surface seeing identical conditions and therefore should have comparable D_{it}. Interface states do not contribute to the observed minority carrier response because in strong inversion interface states are either full (*p*-type) or empty (*n*-type). Therefore changes in surface potential arising from modulation of the small signal a.c. voltage applied to the gate will not significantly affect their occupancy.[22]

C_{ox} is an important parameter in device analysis, for example with regard to D_{it} extraction. These doping series samples can also be utilized with regard to the C_{ox} extraction method we published recently,[12] where it was demonstrated that in strong inversion the maximum value of G/ω at ω_m is equal to $C_{ox}^2/2(C_{ox}+C_D)$. In the current study the oxide thickness is fixed while the doping concentration is varied. Therefore, for a given C_{ox}, as doping concentration increases, C_D will increase and it would be expected using the above relationship that the value of G/ω would decrease. Figure 6 plots the expected theoretical values of G/ω versus doping, for various values of C_{ox}. The measured G/ω values are plotted as open symbols, with the dashed blue lines representing an approximate fitting to those points in each case. It is seen that the experimental values follow the trend of the theoretical values quite closely. In Figure 6 (a) it is evident that the curve calculated using C_{ox} of 0.0075 F/m^2 is in very good agreement with the experimental G/ω data. In the case of the *n*-type devices the 0.0093 F/m^2 for C_{ox} provides a good approximation over most of the doping range, although some deviation is observed in the experimental data for the two highest doping concentrations. These observations are important also in validating the calculations of the theoretical minimum capacitances described earlier in regard to Figure 1 and 2, where the C_{ox} values used to extract the theoretical minimum capacitances were 0.0075 F/m^2 and 0.0093 F/m^2 for *p*-type and *n*-type samples respectively, determined from the measured capacitance at 20Hz. Therefore the C_{ox} values that provide the best fit in both *n* and *p*-type cases in Figure 6 are in agreement with the C_{ox} measured at low frequency (20Hz).

In summary, *p*-type and *n*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitors with semiconductor doping concentrations ranging from $10^{16}cm^{-3}$ to $10^{18}cm^{-3}$ exhibited behavior consistent with surface inversion. The measured minimum capacitance at 1 MHz scales correctly with the $In_{0.53}Ga_{0.47}As$ doping concentration based on a maximum depletion width calculated assuming the surface is inverted, providing evidence that the interface state concentration was reduced to a level which allows inversion of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface for both *n* and *p* type doped $In_{0.53}Ga_{0.47}As$. The minority carrier generation lifetime in the $In_{0.53}Ga_{0.47}As$, τ_g, was found to decrease with increasing doping concentration. C_{ox} values extracted using a method based on the relationship between the capacitance and conductance in strong inversion exhibited excellent agreement with the C_{ox} measured at low frequency (20 Hz). It is notable that this was illustrated previously using an Al_2O_3 thickness series on both *n* and *p*-type $In_{0.53}Ga_{0.47}As$ in which case the doping was fixed and C_{ox} varied with dielectric thickness[22], and also that results from physics based a.c simulations show the relationship to be generally true.[12] Those results, combined with the results of this variable doping study, indicate that the equality of the maximum value of G/ω at ω_m being equal to $C_{ox}^2/2(C_{ox}+C_D)$ in inversion, is a reliable tool to obtain an accurate estimate of C_{ox}, and most significantly that this method can be applied for any MOS system in inversion, regardless of the oxide or semiconductor material.

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Figure 1. 1MHz CV responses at 295K for (a) Au/Ni/7nm-Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$ and (b) Au/Ni/5nm-Al_2O_3/*n*-$In_{0.53}Ga_{0.47}As$ MOS devices with dopant concentrations ranging from ~ 10^{16} cm^{-3} to 10^{18} cm^{-3}. The theoretical values (open symbols) were estimated using a C_{ox} value of 0.0075 F/m^2, and 0.0093 F/m^2 for the *p*- and *n*-type devices respectively.

Figure 2. Plot of measured versus theoretical minimum capacitance for: (a) different *p*-type doping concentrations, with the measured values being those at a gate bias of 1.75 V in Fig. 1(a); and (b) different *n*-type doping concentrations, with the measured values being those at a gate bias of -3.75 V in Figure 1(b).

Figure 3: Multi-frequency CV responses at 295K of (a) *p*-type and (b) *n*-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$, devices, with $In_{0.53}Ga_{0.47}As$ doping concentrations of $2.7x10^{17}$ cm^{-3} and $6.0x10^{17}$ cm^{-3}, and Al_2O_3 thicknesses of ~ 7 nm and 5 nm, respectively. The CV responses with increasing positive gate bias for the *p*-type devices, and with increasing negative gate bias for the *n*-type devices, are consistent with the CV behavior arising from a minority carrier response in inversion.

Figure 4. G_m/ω plotted versus ω in strong inversion for (a) Au/Ni/7nm Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$, and (b) Au/Ni/5nm Al_2O_3/*n*-$In_{0.53}Ga_{0.47}As$ devices. The values of G/ω were taken at a gate bias of 1.75 V for *p*-$In_{0.53}Ga_{0.47}As$ devices and at a gate bias of -3.75 V for *n*-$In_{0.53}Ga_{0.47}As$ devices, utilizing the multi-frequency GV data. Note, the frequency scaled conductance, G/ω, can also be expressed in units of F/m^2.

Figure 5. (a) Increase in transition frequency, ω_m, as a function of $In_{0.53}Ga_{0.47}As$ doping concentration for *p*-type (star) and *n*-type (circle) MOS devices. (b) Decrease in the minority

carrier generation lifetime, τ_g, with increasing doping for *p*-type (star) and *n*-type (circle) MOS devices.

Figure 6. Peak G/ω in inversion as a function of doping concentration for (a) *p*-type and (b) *n*-type Au/Ni/Al_2O_3/$In_{0.53}Ga_{0.47}As$ devices. Different C_{ox} values were used to compute the corresponding theoretical G/ω values at each doping level according to the $(G/\omega)_{max}=C_{ox}^2/2(C_{ox}+C_D)$ relationship. The measured peak G/ω values in strong inversion are plotted as open symbols, and fitted with the dashed line. Note, the frequency scaled conductance, G/ω, can also be expressed in units of F/m^2.

Figure 1

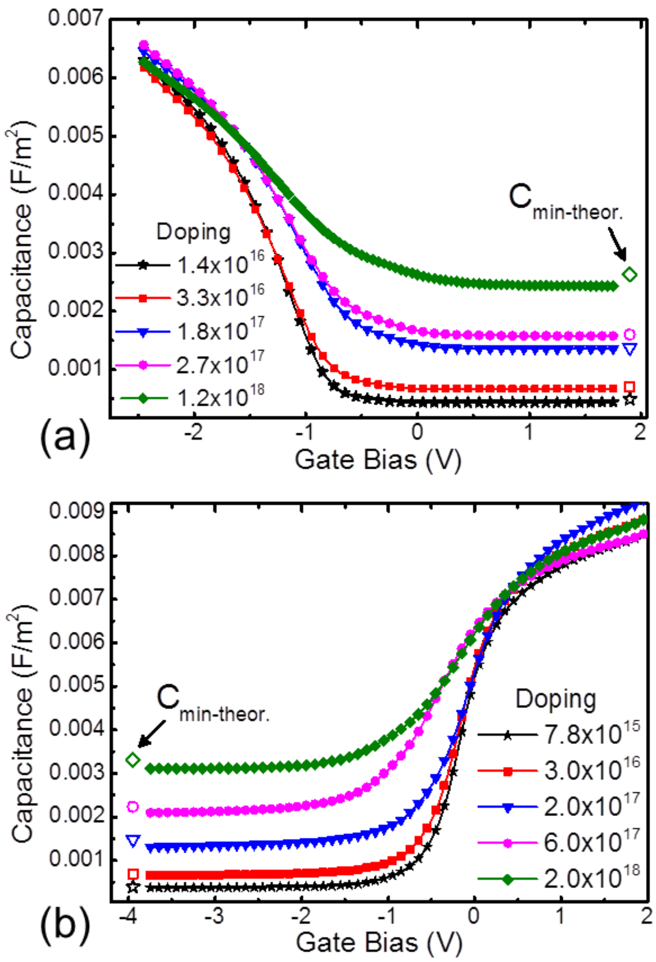


Figure 2

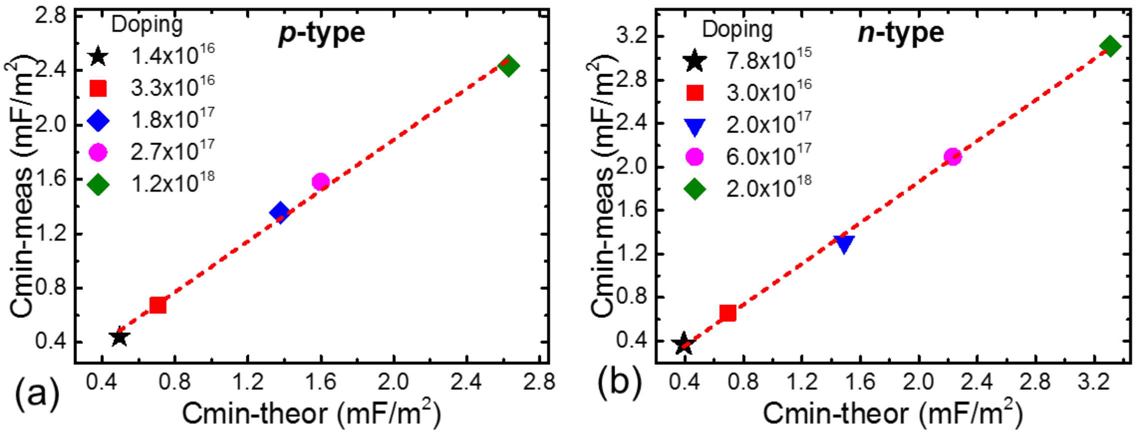


Figure 3

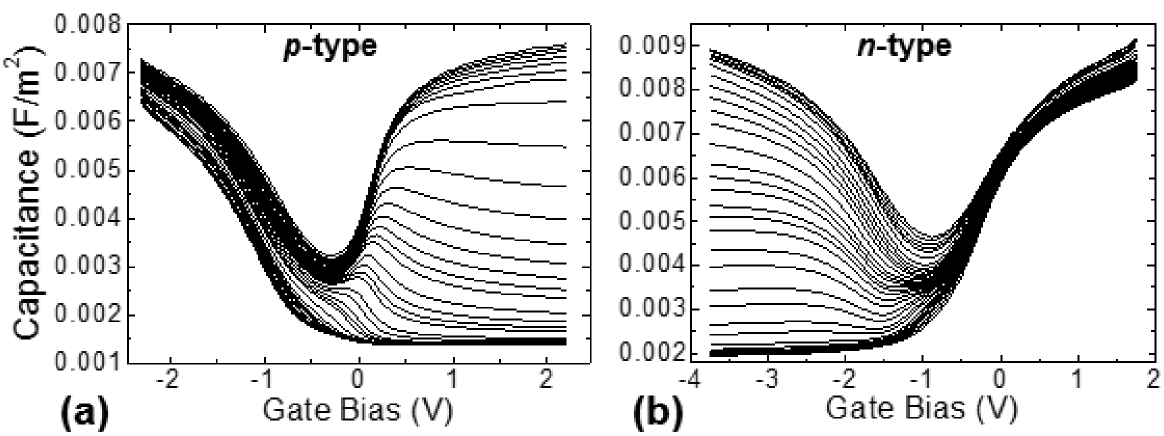


Figure 4

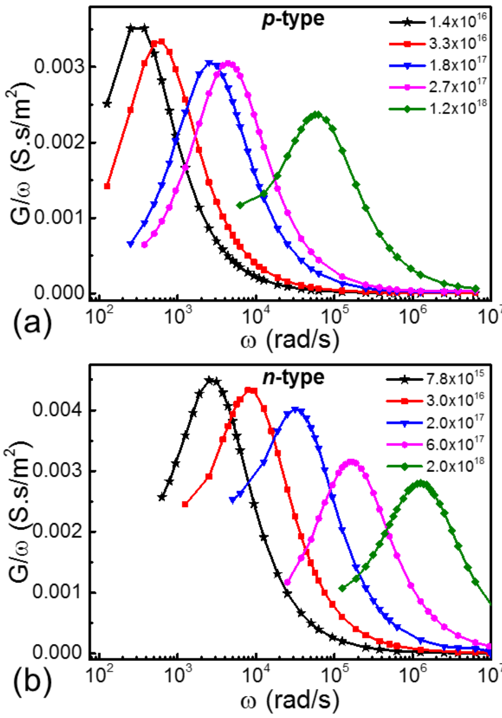


Figure 5

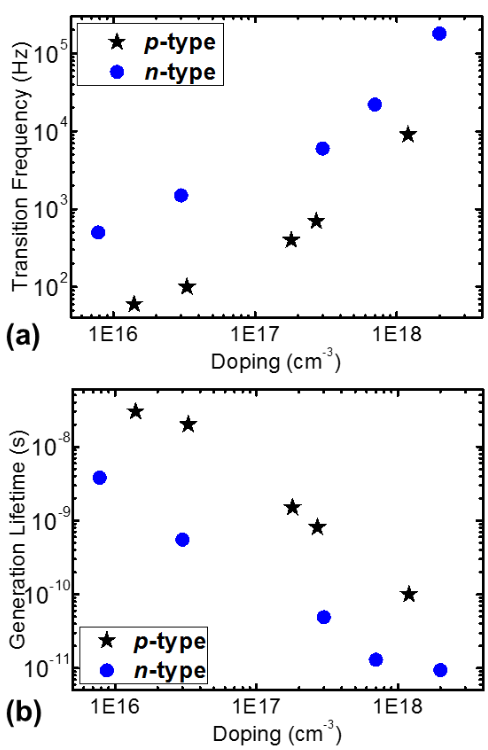
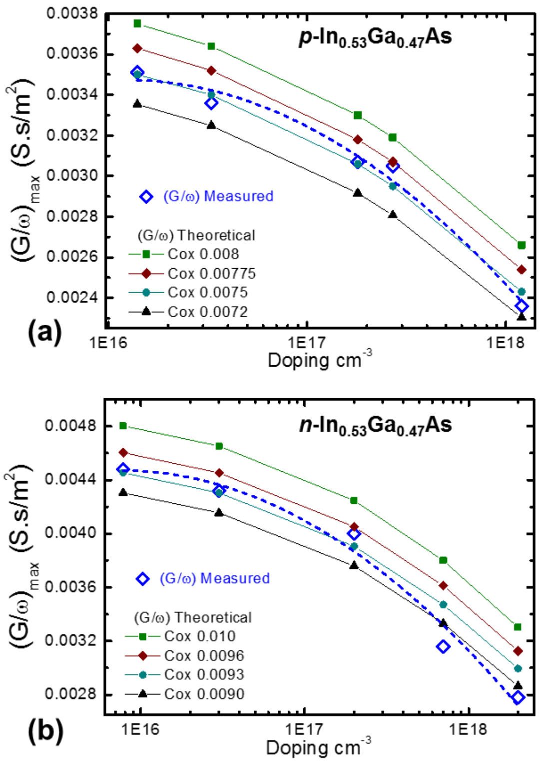


Figure 6



p-In0.53Ga0.47As
(G/ω)max (S.s/m2)
(G/ω) Measured
(G/ω) Theoretical
Cox 0.008
Cox 0.00775
Cox 0.0075
Cox 0.0072
0.0038
0.0036
0.0034
0.0032
0.0030
0.0028
0.0026
0.0024
1E16
1E17
1E18
Doping cm-3
(a)
n-In0.53Ga0.47As
(G/ω)max (S.s/m2)
(G/ω) Measured
(G/ω) Theoretical
Cox 0.010
Cox 0.0096
Cox 0.0093
Cox 0.0090
0.0048
0.0044
0.0040
0.0036
0.0032
0.0028
1E16
1E17
1E18
Doping cm-3
(b)

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