A 40-Gb/s 1.5-µm VCSEL Link with a Low-Power SiGe VCSEL Driver and TIA Operated at 2.5 V

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Abstract: VCSEL links typically require multiple supply voltages for high-speed and low-power operation. We report a 40-Gb/s 1.5-µm VCSEL link achieving 8.7 pJ/bit of energy efficiency with a 0.13-µm SiGe VCSEL driver and TIA operated at 2.5 V.

OCIS codes: (250.3140) Integrated optoelectronic circuits; (250.7260) Vertical-cavity surface-emitting lasers

1. Introduction

High-speed vertical-cavity surface-emitting laser (VCSEL) drivers that directly modulate the laser current are available in two configurations: anode drive and cathode drive. Anode drive has the potential to lower the supply voltage of the VCSEL driver, whereas cathode drive avoids the use of the slower p-type transistors in the high-speed path. Both still have one thing in common though, namely that the VCSEL driver is operated from multiple supply voltages to lower power consumption [1–4], with laser supply voltages ranging from 3.3 V to 5.8 V. In this paper, we will further focus on cathode drive and propose a solution to get rid of the multiple supply voltages.

Cathode drive VCSEL transmitters can be implemented with a back-termination resistor at the output to improve the transition times. Unfortunately, this introduces a current path between the supply voltage of the driver V_{driver} and the supply voltage of the common-anode laser V_{anode}. This can only be nulled by choosing V_{anode} equal to the sum of V_{driver} and the laser forward threshold voltage V_l, enforcing the vendor to provide multiple supply voltages.

We present a 0.13 µm SiGe BiCMOS driver and transimpedance amplifier (TIA) integrated circuit (IC) that can operate a single-mode 1.5 µm VCSEL link up to 40 Gb/s using a single supply voltage of 2.5 V. Although the driver is equipped with a back-termination resistor R_t of 100 Ω, aforementioned problems are eliminated by the balanced regulated output stage shown in Fig. 1. The output stage tracks the anode voltage V_{anode} on-chip and adjusts the common node voltage V_z, through a voltage replica of the laser and a local voltage converter, to stabilize the VCSEL current I_v. A balancing circuit draws a dummy current I_{vd} equal to I_v at low frequencies in order to isolate the voltage converter dynamics from the high-speed output current. The output stage is preceded with a 2-tap feed-forward equalization (FFE) driver of which the magnitude, sign and delay difference of taps A1 and A0 can be modified.

The 0.13 µm SiGe receiver used in the experiments is composed of a common-emitter shunt feedback TIA followed by a cascade of amplifiers. This design is a modified version of [5] in which the resistive shunt feedback is replaced with an active feedback circuit. The gain of the TIA and amplifier stages can be adapted for linear or limiting operation.

2. Experiments

The transmitter die measures 2.5 mm x 1.3 mm and is designed as a 4-channel driver with a channel pitch of 300 µm. The driver outputs are wire bonded to two different 2x1 single-mode VCSEL arrays developed by Technische Universität München, see Fig. 1. Only the rightmost VCSEL is used for the experiments of this paper. The double-mesa short-cavity 1543 nm device is characterized by a buried tunnel junction diameter of 5 µm, a bottom-mesa diameter of 18 µm and a small-signal bandwidth in excess of 19 GHz [6]. The maximum output power of 4.5 mW occurs at a rollover current of 18 mA. The receiver is a 2-channel TIA with a channel pitch of 750 µm. The TIA measures 3.6 mm x 0.98 mm and is wire bonded to two separate photodiodes (PDs) . The PD has an active area of 12 µm and a responsivity of 0.63 A/W. The PD bandwidth is above 35 GHz for bias voltages between 2.5 V and 3 V.

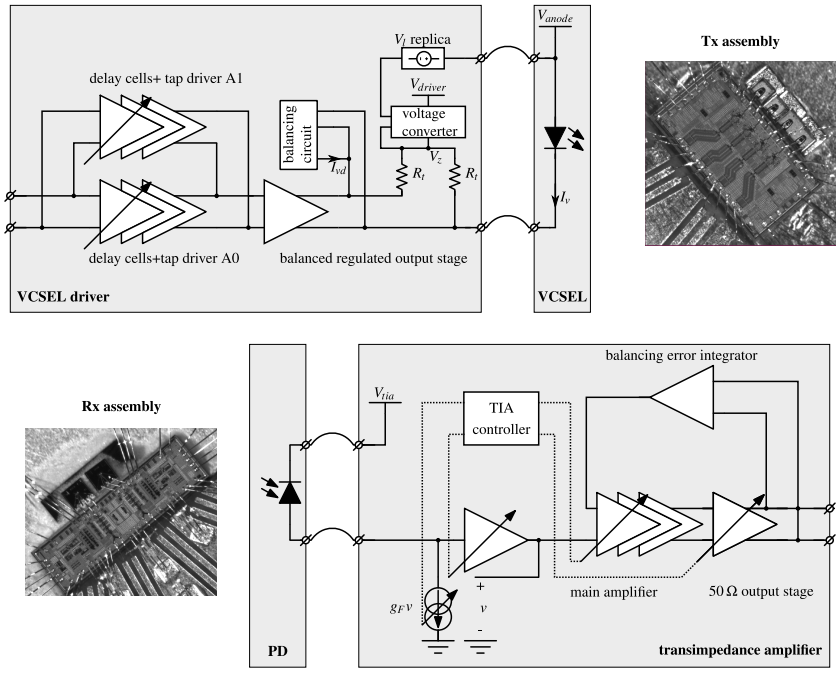

Fig. 1. Block diagram of the 0.13 µm SiGe BiCMOS VCSEL driver and receiver together with a micrograph of the wire bond assembly. Supply voltages V_{driver}, V_{anode} and V_{tia} are all equal to 2.5 V.

The performance of the VCSEL link is tested at 28 and 40 Gb/s using a differential 600 mV pseudorandom bit sequence (PRBS) of 2^7-1 as input signal for the driver. Light is coupled in and out of the optical devices using lensed fibers. Sensitivity curves are measured back-to-back (BTB) and over 100 m and 500 m of single-mode fiber (SMF). The concept of the balanced regulated output stage inside the transmitter will also be verified.

3. Results and discussion

The VCSEL is biased at an average current of 12 mA for all experiments. An extinction ratio (ER) of 5.3 dB is achieved before equalization and reduces to 3.6 dB after equalization. The received eye diagrams at 28 Gb/s and 40 Gb/s are shown in Fig. 2 together with the bit-error ratio (BER) curves. The TIA is pushed to the limiting region to maximize the eye opening, resulting in a differential swing of 400 mVpp. Applying FFE improves the eye height at 40 Gb/s, although the performance improvement is more clear in the BER curves, revealing a gain in sensitivity of 2.3 dB optical modulation amplitude (OMA) at a BER below 10^{-11}. Increasing the data rate from 28 Gb/s to 40 Gb/s induces a power penalty of 2 dB OMA. The VCSEL link is able to operate error-free, i.e. a BER of 10^{-13} is maintained for at least 60 s, over 500 m at 28 Gb/s and 100 m at 40 Gb/s . At 500 m, the maximum optical power coupled into the PD is limited by the setup preventing to go below a BER of 10^{-9}. The power consumed by the receiver amounts 175 mW while the transmitter dissipates 132 mW at 28 Gb/s and 172 mW at 40 Gb/s , leading to 8.7 pJ/bit at 40 Gb/s. Although the link is around 5 dB less sensitive than [3, 4], our link is almost three times more energy efficient while operating at 2.5 V compared to the 4, 5 and 5.8 V used in [3]. With respect to a 25 Gb/s common-cathode VCSEL link operating at 1 and 3.3 V [1], our common-anode link is 3 dB more sensitive at 28 Gb/s with similar power consumption.

Figure 3 clearly shows that the transmitter can preserve a constant current through the laser over a wide range of anode voltages. The BER curves prove that high-speed performance is only marginally affected when changing the anode voltage, i.e. when the switching transistors are not pushed into saturation as is the case at 2.3 V.

4. Conclusion

We have successfully demonstrated a 0.13 µm SiGe driver and TIA operating a 1.5 µm VCSEL link at 40 Gb/s error-free over 100 m of SMF. Most notably, these results are obtained running the ICs of a single supply voltage of 2.5 V while achieving an energy efficiency of 8.7 pJ/bit.

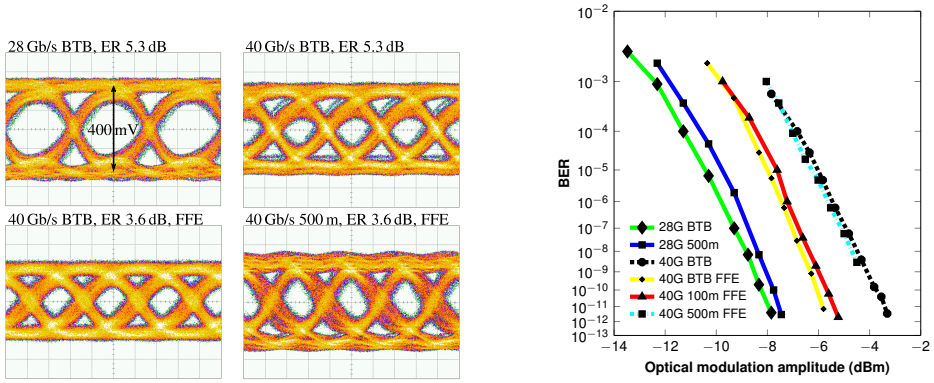

Fig. 2. Received eye diagrams and BER curves at 28 Gb/s and 40 Gb/s for various transmission distances. Remark that the eye diagram at 500 m was recorded at a higher input power.

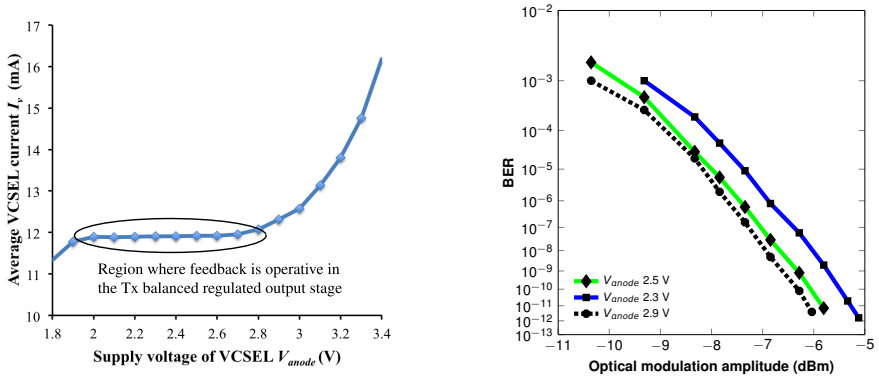

Fig. 3. Impact of the VCSELs anode voltage at DC and at 40 Gb/s

5. Acknowledgments

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