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Carbon-Related Defects in Si:C/Silicon Heterostructures Assessed by Deep-Level Transient Spectroscopy

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This paper reports on a Deep-Level Transient Spectroscopy (DLTS) study of the electrically active defects in ~100 nm Si:C stressors, formed by chemical vapor deposition on p-type Czochralski silicon substrates. In addition, the impact of a post-deposition Rapid Thermal Annealing (RTA) at 850°C on the DLT-spectra is investigated. It is shown that close to the surface at least two types of hole traps are present: one kind exhibiting slow hole capture, which may have a partial extended defect nature and a second type of hole trap behaving like a point defect. RTA increases the concentration of both hole traps and, in addition, introduces a point defect at $E_V + 0.35$ eV in the depletion region of the silicon substrate at some distance from the Si:C epi layer. This level most likely corresponds with C_iO_i-related centers. Finally, a negative feature is found systematically for larger reverse bias pulses, which could point to a response of trap states at the Si:C/silicon hetero-interface.

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Further scaling of CMOS transistors goes hand in hand with higher straining of the channel, in order to boost the device performance. For nMOSFETs, this can be achieved by applying tensile stress in the channel direction for enhancing the electron mobility.[1–8] Channel strain can be implemented by replacing the silicon source/drain (S/D) regions by so-called stressors, deposited by selective epitaxy. In a bulk FinFET architecture several of the standard strain techniques, like, e.g., the application of a Contact-Etch Stop Layer (CESL), lose their effectiveness, so that stress engineering becomes more and more difficult.[9] It has been shown that for n-channel bulk FinFETs, Si:C source/drain stressors are very efficient,[9] explaining recent research interest.[7–10] Highly in situ phosphorous-doped Si:C hetero-epitaxial layers with about 1% C can for example be grown by selective Chemical Vapor Deposition (CVD), using a cyclic deposition and etching process.[11] It is important that both C and P are incorporated in substitutional positions in order to reduce the in-plane lattice parameter of the S/D stressors and to introduce maximum stress in the adjacent channel. However, keeping in mind that the equilibrium solid solubility of C in Si is much lower than 1%, there will be a large driving force for carbon precipitation upon subsequent thermal processing. The formation of interstitial or clustered carbon will reduce the strain and also the favorable effect of the stressors on the device performance. At the same time, keeping an as high as possible active P concentration is essential to reduce the contact resistance.[6,12]

It has been observed in the past that the application of a post-deposition laser anneal (LA) increases the active P doping level[13] but at the same time results in lower layer stress,[12] suggesting the loss of substitutional carbon. This can happen through the formation of interstitial carbon (C_i) which is highly mobile even at room temperature (RT). C_i can diffuse from the Si:C epi layer into the silicon substrate, where it becomes trapped by intrinsic point defects or impurities to form complex, more stable point defects, which may be electrically active.[14–17] These defect pairs can act as nuclei for further carbon clustering by trapping more C atoms, according to the reaction schemes proposed in the literature.[18–21]

In this paper, a Deep-Level Transient Spectroscopy (DLTS) analysis is performed to address this issue, since some of the C-related defects correspond with levels in the bandgap of silicon. Monitoring these levels provides more insight into the microscopic processes going on in the Si:C epi layer and in the substrate depletion region underneath.

Experimental

Undoped $Si_{0.984}:C_{0.016}$ layers with a thickness of ~100 nm have been deposited on p-type Czochralski (CZ) silicon substrates by a CVD process as described previously.[12,22] In addition, post-deposition Rapid Thermal Annealing (RTA) was performed at 850°C for 15 min. under N_2 atmosphere. No in situ P doping was applied in order to avoid the formation of an n^+p junction, which makes the assessment of electrically active defects in the highly doped Si:C layer difficult if not impossible. Instead, Al Schottky barriers (SBs) with different diameters have been thermally evaporated on an undoped Si:C epitaxial layer. Typical current-voltage (I-V) and 1 MHz capacitance-voltage (C-V) curves are represented in Fig. 1 for a 3.1 mm diameter SB on an annealed sample, showing decent C-V and forward current. The rather high reverse current indicates the presence of a large density of generation-recombination centers in the silicon depletion region. From the reverse capacitance, a uniform p-type doping density N_{dop} of 2.0×10^{15} cm^{-3} has been derived at room temperature. A similar doping density is found in the p-type substrates, for the as-grown and RTA samples. The depletion width in Fig. 2, corresponding with a reverse bias V_R, is calculated from $W(V_R) = \varepsilon_{Si}\varepsilon_0 A/C(V_R)$, with A the area of the SB, ε_{Si} the dielectric constant of silicon and ε_0 the permittivity of vacuum.

Fourier-transform (FT) DLTS has been performed from 75 K to room temperature, using the sine coefficient b1 to calculate the DLT-spectrum from the capacitance transients. Different bias pulses have been applied during the same temperature scan, from V_R to V_P, as indicated schematically in Fig. 2, showing the depth probed by the measurements. This should give an idea about the concentration profile of the observed hole traps in the p-type depletion region in the silicon substrate. As can be derived from Fig. 2, when applying a V_R of 0 V and pulsing till approximately the flatband condition ($V_P = 0.7$ V) should enable the detection of deep hole traps close to the surface, i.e., in the Si:C epi layer. In all cases, a sufficiently long pulse duration t_p has been adopted in order to saturate the deep levels in the probed region. The period of the pulse corresponds with the sampling period t_w, which is typically 51.2 ms.

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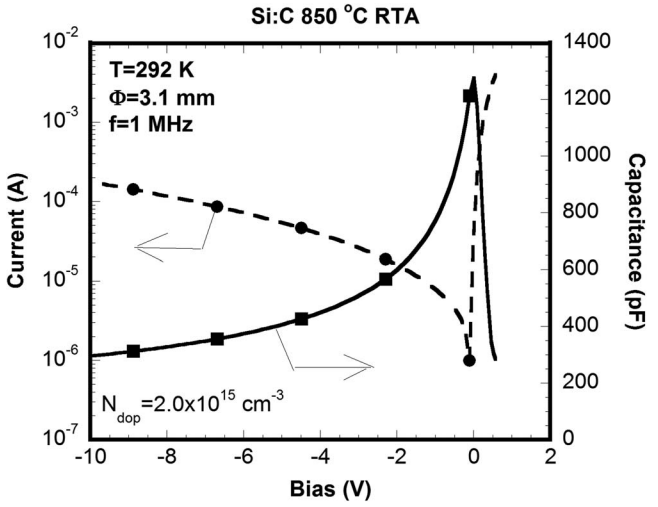

Figure 1. I-V (●) and C-V (■) (f = 1 MHz) characteristics at room temperature of an Al Schottky barrier on a 100 nm $Si_{0.984}$:$C_{0.016}$ epi layer on a p-type CZ silicon substrate.

Results

Deep levels in the silicon substrate.—Figure 3 compares the I-V characteristics of a 3.1 mm Al SB on an as-grown and annealed sample, demonstrating a pronounced, more than one order of magnitude increase of the reverse current after RTA. On the other hand, the forward current overlaps for both SBs. This indicates that the barrier height is not modified, but rather an additional Shockley-Read-Hall (SRH) leakage component is present for the RTA sample. This suggests the creation of active generation-recombination centers in the silicon depletion region. This is also supported by the reduction of the activation energy (E_A) of the reverse current I_R at a reverse bias V_R = –10 V, shown in the inset of Fig. 3. For the as-deposited sample, the E_A = 0.66 eV corresponds with the Schottky barrier height of Al on the Si:C epi layer. After RTA, it is difficult to derive a unique E_A, as the slope is increasing for increasing T. Around room temperature, a value of about 0.24 eV is found, which is much smaller than the expected SB height. This indicates that an additional generation-recombination (GR) current contributes to the leakage current on top of thermionic

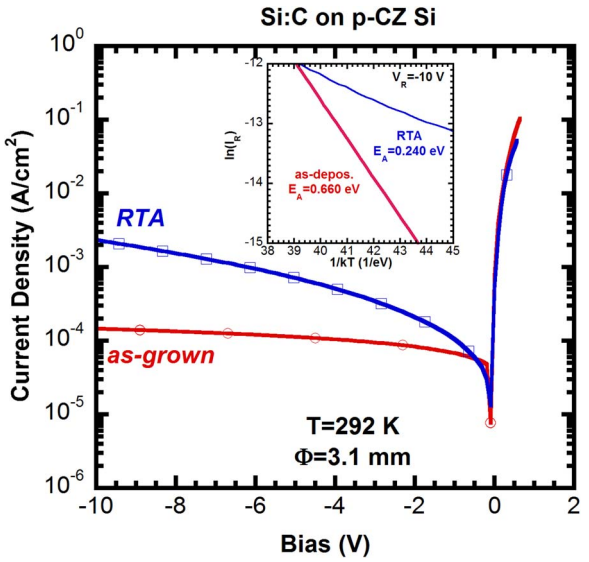

Figure 3. Current density versus bias at room temperature, for an Al SB on an as-deposited and an annealed Si:C layer on a p-type CZ Si substrate. The inset shows the Arrhenius plot of the reverse current I_R at a reverse bias V_R = –10 V for both SBs.

emission across the barrier. The activation energy found in the inset of Fig. 3 should correspond with the energy level of the GR center in the depletion region.

The DLT-spectra of Fig. 4 confirm the idea of a higher trap density in the depletion region: while the as-grown sample exhibits no positive peaks (no hole traps) above the detection limit of the method (on the order of ~10^{11} cm^{-3}), a hole trap is observed after RTA at about 160 K. The corresponding activation energy is 0.35 eV with respect to the valence band E_V, as shown in Fig. 5. This is in reasonable agreement with the deep level position which can be expected from the activation energy of the generation current in the inset of Fig. 3.

A final observation is the presence of a small and asymmetric negative peak at about 200 K in the sample after RTA in Fig. 4. In fact, a similar broad negative peak is found in some of the as-grown samples as well, as demonstrated by Fig. 6. The presence of a peak with opposite sign in DLTS usually points to the presence of minority carrier traps, i.e., electron traps in p-type silicon. However, it is rather

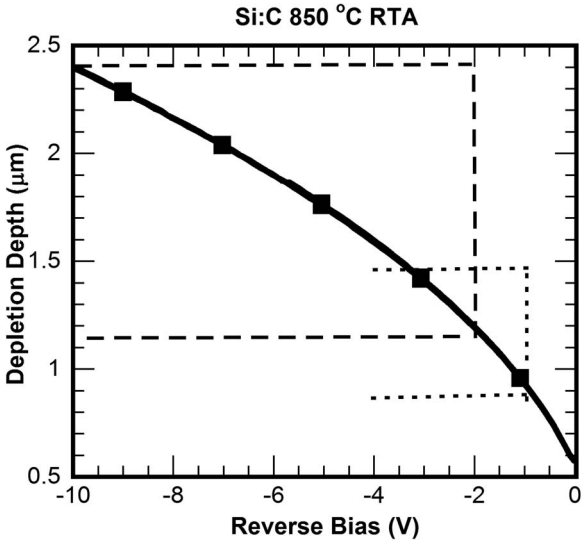

Figure 2. Depletion region width versus reverse bias for the SB diode of Fig. 1. Also indicated are different bias pulses in DLTS and the corresponding depletion depths.

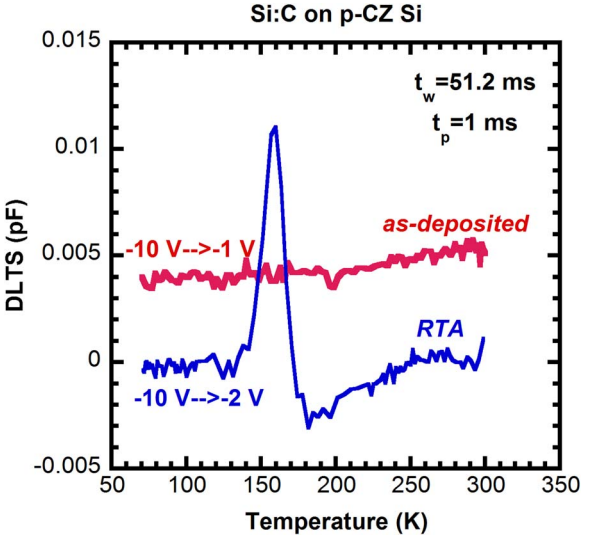

Figure 4. DLT-spectra for an as-deposited and an 850°C RTA treated SB. The bias pulse is from –10 V to –2 (–1) V probing the silicon substrate.

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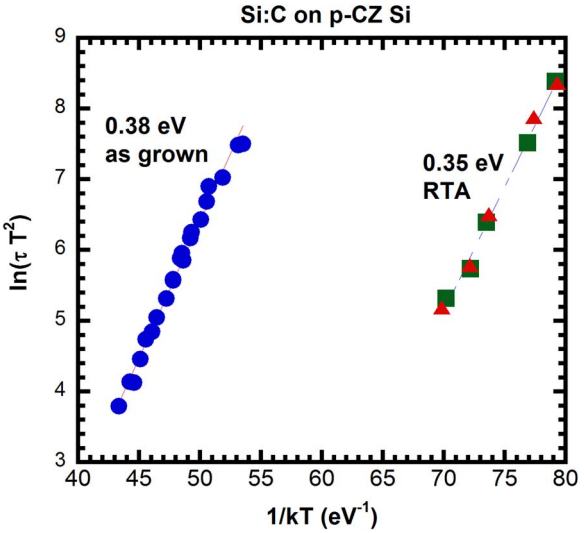

Figure 5. Arrhenius plot for the dominant hole trap in the Si:C epi layer (as grown; 0.38 eV) and for the hole trap in the silicon depletion layer (RTA; 0.35 eV).

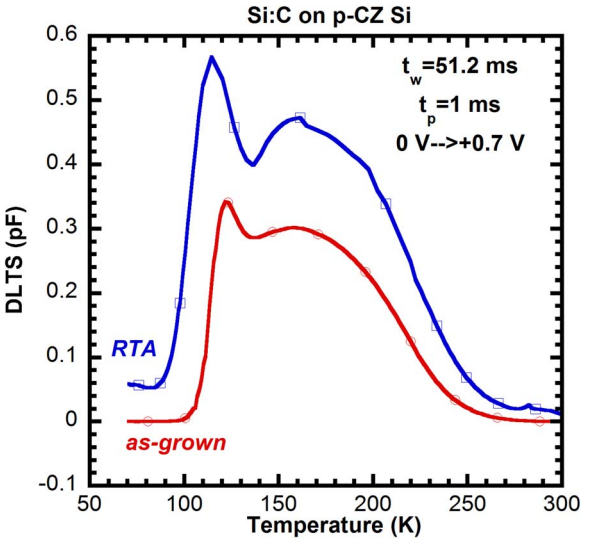

Figure 7. DLT-spectra for an as-deposited and an 850°C RTA treated SB. The bias pulse is from 0 V→+0.7 V probing the epi layer.

exceptional to detect minority carrier peaks in a SB,[23,24] especially for large reverse biases, since the density of minority carriers is negligible. The fact that the negative feature is found in most of the spectra indicates that it is specific for this type of devices, which will be discussed in the following.

Deep levels near the Si:C epi layer.—In order to assess the deep levels in proximity of the Si:C epi layer, i.e., close to the Schottky barrier contact, according to Fig. 2 a bias pulse in forward operation, e.g., from 0 V to +0.7 V has to be applied. The results in Fig. 7 reveal the presence of a broad peak with two maxima both before and after RTA. The DLTS amplitude increases after RTA, indicating an increase in the hole trap concentration in the Si:C layer. The activation energy corresponding with the maximum at higher temperatures (~160 K) is 0.38 eV (Fig. 5). From the spectra in Fig. 8, derived for bias pulses probing the depletion region adjacent to the Si:C layer, a shoulder develops to the high-temperature side of the $E_V + 0.35$ eV peak in the spectrum of an RTA SB, indicating that in the region close to the epi layer, another type of defect(s) is formed, possibly related to small C-related clusters.

Discussion

The "profile" of the hole traps found in a Si:C sample after RTA is summarized by the spectra of Fig. 9. At a depth of about 1 to 2 μm, a hole trap at 160 K is observed with activation energy of 0.35 eV. To the high-T side, also a negative feature is typically found. The spectra broaden significantly when moving closer to the surface for more positive V_R (–1 V and 0 V) and the Si:C layer, resulting in a double-peaked shape in/at the Si:C epi layer.

From the Arrhenius plot in Fig. 5, an activation energy of 0.35 eV is derived and a hole capture cross section of 8×10^{-14} cm^2 for the DLTS peak observed in the samples after RTA, at large negative V_R (Fig. 4). Comparing with literature data,[14,15,25–30] it is concluded that the hole trap found in the p-type silicon substrate after RTA most likely corresponds with C_iO_i-related centers, although the σ_p

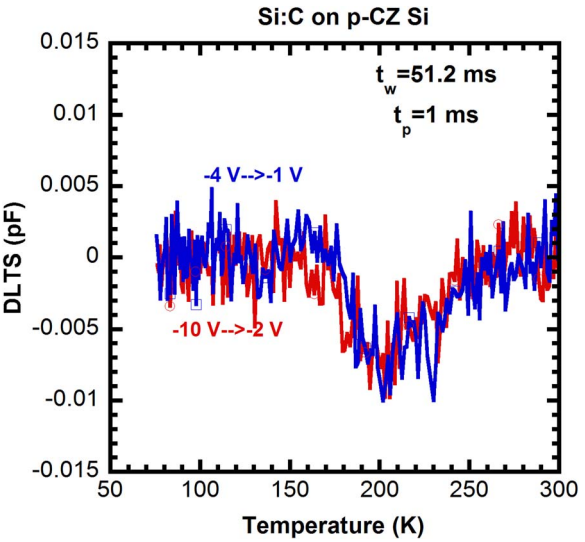

Figure 6. DLTS spectra for a 3.1 mm Al SB on an as-grown sample at a bias pulse from –10 V→–2 V and –4 V→–1 V.

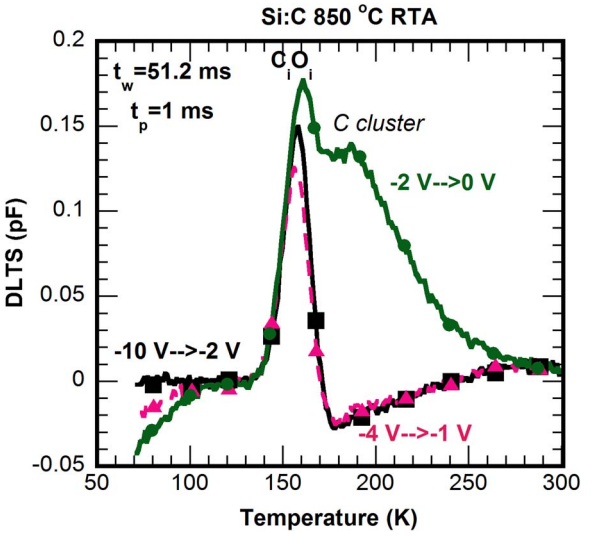

Figure 8. DLT-spectra for an RTA sample (3.1 mm Al SB) corresponding with different bias pulses. A filling pulse of 1 ms and a sampling period of 51.2 ms have been employed.

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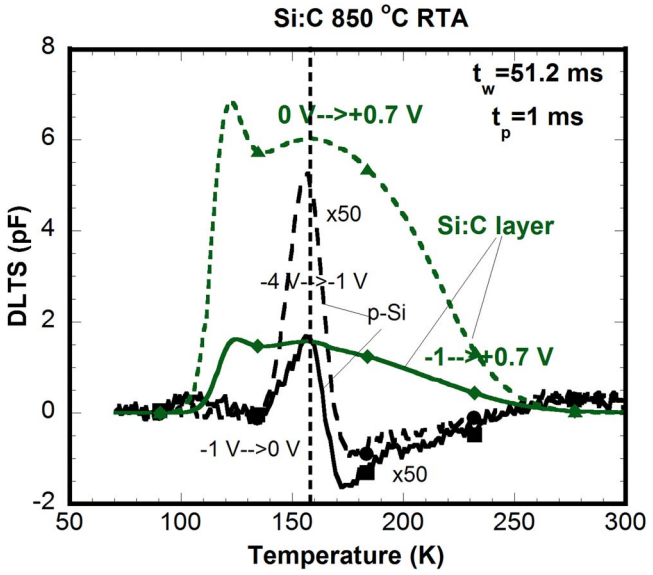

Figure 9. DLT-spectra for an RTA sample (3.1 mm Al SB) corresponding with different bias pulses. A filling pulse of 1 ms and a sampling period of 51.2 ms have been employed.

is about one decade higher than the typically reported values. This could be due to the effect of the negative feature observed in Fig. 4, distorting to some extent the positive peak at about 160 K and the derived Arrhenius plot. In fact, comparing with the data of Ref. 30, one can conclude that the experimental points in Fig. 10 are closer to the Arrhenius plot for the C_iO_i* precursor center than to the C_iO_i data. Also shown in Fig. 10 is the Arrhenius plot for the C_i hole trap in p-type silicon, showing reasonable agreement with the measurement data. However, as interstitial carbon is highly mobile even at 300 K, its energy level is unstable and disappears after a couple of days, transforming into higher-order C-related complexes, like C_iO_i (or C_iO_i*). The fact that a CZ silicon substrate is used, makes it very likely that C_i becomes trapped by O_i in the bulk of the wafer.[14,15,25–30] Another potential source of oxygen could be traces of moisture in the RTA annealing ambient, where oxygen diffuses in from the surface.

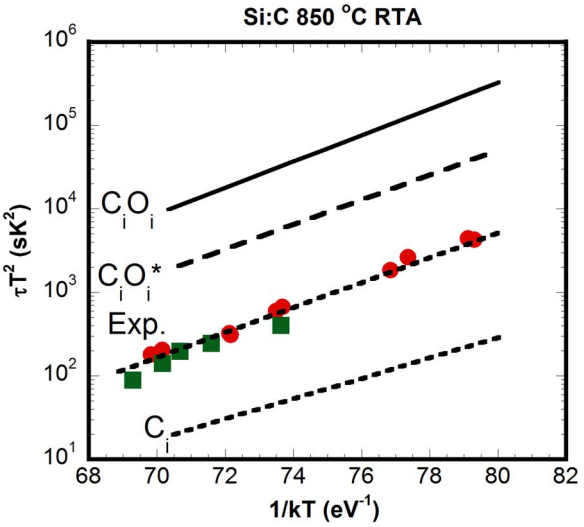

Figure 10. Experimental Arrhenius plot (■;●) for an RTA sample at -4 V→-1 V. The data has been derived from the maximum position in a temperature scan (●) and from frequency scans at different temperatures (■). A comparison is made with literature data for the C_iO_i, the C_iO_i* and the C_i hole trap levels in p-type silicon.[28]

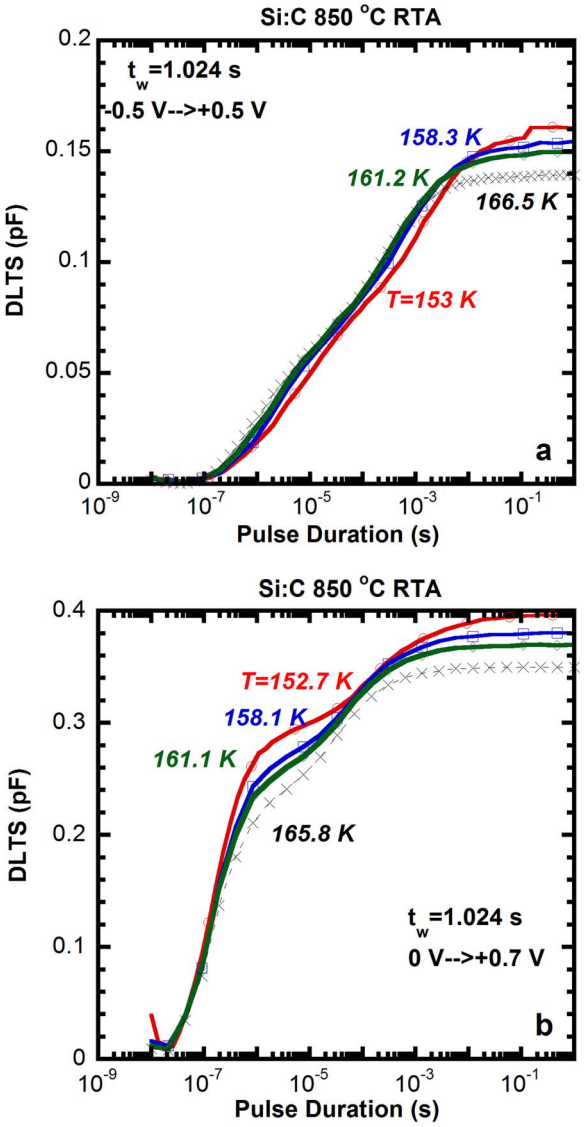

Figure 11. DLTS amplitude in function of the pulse duration at different temperatures for a Si:C epi layer after 850°C RTA. The bias was from –0.5 V→+0.5 V (a) and from 0 V →+0.7 V (b). The sampling period is 1.024 s.

It is also concluded from the DLTS results reported here that during RTA additional carbon atoms are transformed from substitutional into interstitial positions,[31] explaining at least part of the loss of stress after high-temperature annealing.

Inside the epi-layer, Fig. 9 indicates the presence of at least two types of hole traps: one kind, corresponding with a sharp peak at 110–120 K and a second much broader peak occurring at higher temperatures. The large width of the second peak suggests the presence of a distribution of deep levels, which could exist in an extended defect or at the hetero-interface between the silicon substrate and the Si:C epi layer. In order to gain further insight in this matter, the capture kinetics of these hole traps has been studied in function of the bias pulse time t_p. Again, two different types of behavior have been found, pointing toward the existence of at least two kinds of hole traps in the epi layer. The first kind is illustrated by Fig. 11a, corresponding with a bias pulse from –0.5 V to +0.5 V. A logarithmic type of trap filling is observed, followed by a saturation of the DLTS amplitude. This could point to a partial extended defect nature,[32] as has been observed in the past for silicon-interstitial clusters, like the {311} defects.[33] The threshold time noted in Fig. 11a before the start of the trap filling may

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be the result of a slow filling phenomenon at the edge of the depletion region (so-called λ region).[34]

The second behavior is illustrated by Fig. 11b at a bias pulse from 0 V to +0.7 V and showing an initial fast trap filling, saturating at about 1 μs, followed by a second slow-filling component. Comparing the DLTS amplitude, it is clear that the second part at large t_p agrees with the result shown in Fig. 11a and having an amplitude of about 0.15 pF. The filling kinetics of this "faster" trap is more point-defect-like and appears to occur closer to the surface, i.e., closer to the Si:C epi layer, since it is not found in the –0.5 V to +0.5 V spectrum of Fig. 11a. A tentative interpretation is that the extended-type of defects corresponds to a C-related cluster or precipitate, while the point defects could be smaller aggregates or single non-substitutional C atoms, giving rise to hole traps.

The observation of these two types of hole traps in the epi layer (or in its close vicinity) suggests a second pathway for C "de-activation", which is associated with the formation of small C-related clusters (precipitates), already present in the as-grown state and further enhanced by the RTA treatment. A similar conclusion was reached before in the study of pulsed excimer laser-annealed silicon implanted with carbon, demonstrating the formation of silicon carbide precipitates in the near surface region.[35,36] The band of hole traps could then correspond with states at the Si:C/silicon interface.

It should be remarked that it is not straightforward to quantify the concentration corresponding with the hole traps close to the Si:C layer from the DLTS peak amplitude for a bias pulse into forward operation. This can be explained by considering their concentration profile, where it is expected that the traps mainly occur close to or even inside the epi layer of thickness 100 nm. According to Fig. 2, this is only about 20% of the depletion region corresponding with $V_R = 0$ V. This means that the so-called "pulse correction factor" required to account for the fact that only a part of the depletion region is probed by the pulse from V_R to V_P amounts to roughly 5 in this case. One possible way to solve this issue is to deposit the Si:C stressors on a highly doped p-type substrate, in order to reduce the thickness of the depletion layer corresponding with the built-in potential of the Schottky barrier. The drawback is that this will automatically reduce the detection limit, as it is proportional to the doping density. Alternatively, one can deposit a further silicon layer on the Si:C stressor, resulting in a layer which is buried in the built-in depletion region. Of course, it has to be shown whether the top Si epi layer can be grown with sufficient crystalline quality in order not to introduce additional deep levels.

A further complication stems from the observation that the spectrum of the deeper hole trap at $E_V + 0.38$ eV is broader than a simple point defect peak. This means that the Density-of-States has to be considered in order to calculate the corresponding trap concentration. In addition, according to Fig. 11, the slow peak occurs over a wider spatial region than the fast hole trap. It implies that for this slow trap no saturation of the peak height with the pulse duration occurs for typical values, i.e., 1 ms, so that this will contribute to an underestimation of the true trap concentration. Another important consideration is that during a forward bias pulse, employed here to access the near-surface deep levels, a significant majority carrier current flows, which can affect the trap occupation during the pulse. On the other hand, it is expected that the emission transient itself is not compromised as at $V_R = 0$ V in principle minimum current flows through the structure.

For these reasons, it is difficult to quantify the exact amount of substitutional carbon lost by the RTA treatment. Moreover, not all non-substitutional carbon atoms may exist in an electrically active form, rendering them 'invisible' for DLTS observation. A more quantitative assessment of the carbon loss requires other techniques like High-Resolution X-Ray Diffraction and Raman analysis, results which will be published elsewhere.[31]

A final word should be spent on the interpretation of the negative feature found in the spectra for large depletion depths (Figs 4 and 6). As shown in Fig. 12, the negative peak becomes larger for larger pulse durations (100 ms) and its position shifts to higher T for a smaller sampling period t_w. At the same time, the position of the C_iO_i-related hole trap remains the same, as long as the negative feature is not too

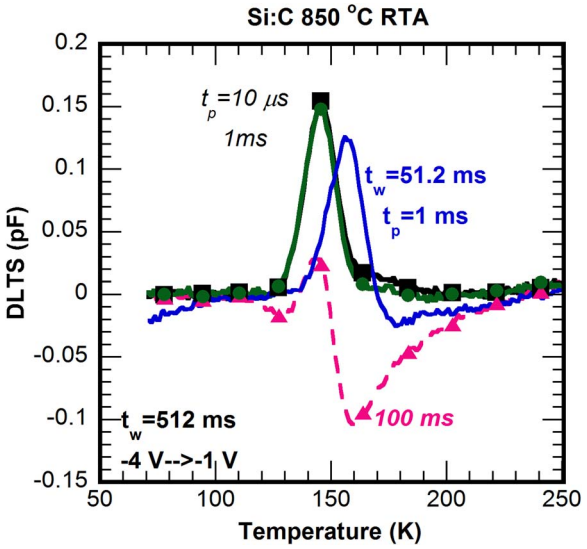

Figure 12. DLTS spectra for a Si:C epi layer after RTA, corresponding with a bias pulse from -4 V→-1 V and with different pulse durations: 10 μs (●); 1 ms (■) or 100 ms (▲). The sampling time is 512 ms. For comparison, a spectrum at the reference condition of $t_p = 1$ ms and $t_w = 51.2$ ms is included (blue line).

pronounced. Also the corresponding peak amplitude for 10 μs and 1 ms remains the same, indicating that at 10 μs the trap concentration is already saturated. While the origin of the "electron trap" in Fig. 12 is unclear for the moment, similar negative peaks have been found before in Molecular Beam homo-Epitaxial (MBE) silicon layers on a p-type silicon substrate, using DLTS on Al Schottky barriers.[37] The broad distribution of electron traps was associated with the epitaxial interface and could be related with the presence of residual oxygen and/or carbon contamination. Observation of the peak was shown to be very sensitive to the pulse duration. In fact, the negative peak resulted from reverse DLTS measurements,[38] where the SB was pulsed from less negative to a more negative value, corresponding with enlarging the depletion region during the pulse. The capacitance transient results then from hole capture or electron emission by the deep levels or both. Alternatively, the negative DLTS peak could originate from the response to the applied bias pulse of a Schottky barrier present at the back substrate contact.[39,40] However, there is no evidence in the I-V and C-V characteristics of Fig. 1 that this is the case. Further in-depth studies are required to identify the origin of the negative peak.

Conclusions

DLTS on Al/Si:C/p-Si Schottky barriers has shown the presence of at least three types of hole traps. In the as-deposited samples and in the vicinity of the Si:C epi layer two hole traps have been observed: a broad band at higher activation energy (peak position at $E_V + 0.38$ eV) and a narrow peak at lower temperatures. Based on the capture kinetics, one trap behaves like a point defect, while the second peak exhibits partial extended-defect behavior. The concentration of the deep levels was found to increase after RTA at 850°C. In addition, a single-level peak at $E_V + 0.35$ eV most likely corresponding with a C_iO_i-related trap has been found in the silicon depletion region after RTA. It provides evidence for two substitutional carbon "deactivation" mechanisms in the epi layer, namely, for the transfer of carbon from substitutional to interstitial sites, resulting in deeply diffusing C_i and the formation of C_iO_i by oxygen trapping in the silicon substrate and, secondly, by the formation of less mobile carbon clusters, closer to the surface.

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