Passive component embedding in printed circuit boards for space applications

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Maarten Cauwe[(1)], Johan De Baets[(1)], Gerhard Schmid[(2)], Christian Galler[(2)], Johan De Hert[(3)], Steven De Cuyper[(3)], Denis Lacombe[(4)]

[(1)] Centre for Microsystems Technology (CMST), imec and Ghent University
Technologiepark 15
9052 Zwijnaarde, Belgium
Email: Maarten.Cauwe@imec.be

[(2)] AT&S AG
Fabriksgasse 13
8700 Leoben, Austria
Email: G.Schmid@ats.net

[(3)]QinetiQ Space
Hogenakkerhoekstraat 9
9150 Kruibeke, Belgium
Email: Steven.DeCuyper@qinetiq.be

[(4)]TEC-QTC, ESTEC
Keplerlaan 1
NL 2200 AG Noordwijk ZH, The Netherlands
Email: Denis.Lacombe@esa.int

ABSTRACT

The objective of this activity was to investigate the suitability of embedding passive components in printed circuit boards for space applications. To achieve this goal, an overview of available technologies for component embedding was provided along with their strongpoints and challenges with respect to space projects. The direct embedding of passive components in printed circuit boards was evaluated in depth to determine its performance and reliability. Characterization and reliability investigation were performed using a dedicated test board containing embedded resistors and capacitors. A Spacecraft Interface Module (SIM) board, part of the Advanced Data and Power Management System developed by QinetiQ Space, was redesigned using embedded passive components to demonstrate the capabilities of the technology. Procurement of components for embedding and other logistic aspects were evaluated in this exercise. The outcome of this study aids ESA in determining which projects can benefit from this technology and what procedures for procurement and validation need to be followed.

INTRODUCTION

Embedded components in printed circuit boards (PCBs) have been around for decades, but broad acceptance and implementation in real-world products only happened in the last five years. Reduced volume and weight, increased electrical performance, larger design freedom and the elimination of solder joints are benefits that are also appealing for space applications. This study aims at closing the gap between quality requirements for space products and the status of the passive component embedding technology.
Embedding of passive components inside a printed circuit board can be realized in two ways. A first approach is to mount stand-alone passive components on one of the inner layers of the PCB. The competing technology creates the passive components in-situ, as an extra layer inside the printed circuit board. While both direct embedding and formed components are theoretically possible for a broad range of passive components, the majority of the technical solutions focus on resistors and capacitors. Due to the limitations in sheet resistivity and capacitor density, the additional design effort needed and the manufacturing issues, forming components inside a PCB remains limited to dedicated functions as power-ground decoupling or integrated heating elements. Direct embedding of placed components is a much more

flexible and powerful alternative to surface-mount technology. The technologies for direct embedding are differentiated by the method for realizing the interconnection to the component (microvia, solder, conductive adhesive) and by the position in the process flow where the embedding actually occurs.
The Embedded Component Packaging (ECP®) technology from AT&S was selected for use in this study. The technology can be used for the embedding of both active and passive components. In this project, only the latter option was evaluated. The main characteristics of the technology are the use of openings in the prepreg layers matching the location of the components and the Cu microvia interconnections to the contact pads of the embedded component. The plated Cu microvia interconnection eliminates the need for solder or conductive adhesives, thus avoiding the associated failure modes. The thickness of the components (150 – 330 µm) and their pad metallization (copper) need to be compatible with the lamination and metallization process steps, respectively. Murata, AVX and Panasonic offer a broad range of embeddable passive components and are continuously improving their product range with respect to available values, tolerances, and temperature and power ratings.
In principle, a standard PCB process flow starts with a double sided core, which is structured in the subsequent process steps and built up to a multilayer construction. In the case of embedding components, a so called "embedded core" is produced first (Fig. 1). The main process steps for embedding components are printing of adhesive, assembly of components, pressing and drilling of vias and plated through holes. After realizing the embedded core, two different ways of further processing are possible. The embedded core can be further processed into a multilayer board construction, or the product can be finalized to a chip package. Depending on what kind of product application is targeted, the process flow will differ in the final processing.

TEST BOARD DEFINITION

Within the frame of this project, two different boards with embedded passive component were specified, designed, manufactured and tested. Board Type I (BTI) is used for the evaluation of the performance and reliability of the embedding technology. Board Type II (BTII) is based on an existing design of QinetiQ Space (SIM-FUMO) and is redesigned for the use of embedded passives by AT&S.
Board Type I is a rigid, four-layer printed circuit board in a 1+2+1 construction (Fig. 2). The components are embedded between layer 2 and 3 and connected to layer 3. The selection of components for Board Type I is guided by the commercial offerings from the component suppliers and the selection of components for Board Type II. For the resistors (Panasonic), a high end (1 MΩ) and low end value (33 Ω, also included in BTII) are selected, combined with a 0201, 1% and 0402, 5 % version of the 10 kΩ resistor. Continuity and interconnection resistance is measured using 0201 and 0402 0-ohm resistors. Two type-I capacitors from Murata are chosen (10 pF and 100 pF), next to four variations of the 10 nF capacitor from AVX (300 µm thickness, 16 V to 50 V and 150 µm thickness, 6.3 V) and a 100 nF capacitor from Murata (150 µm thickness, 6.3 V).
Board Type I includes the following test structures.

- Probe pad test structure for electrical measurement of each individual component, including possibility of stress testing of component (voltage, power).
- Disk, comb and tree test pattern for insulation resistance and dielectric breakdown between layers, within layers, and between component terminal and neighbouring conductive structures (PTH, trace).
- Daisy chain test pattern for continuity and interconnect resistance, including connections to embedded components by using 0-ohm resistors.
- Interconnect stress test (IST) patterns for the evaluation of the interconnection to the components and plated through-holes near the components.

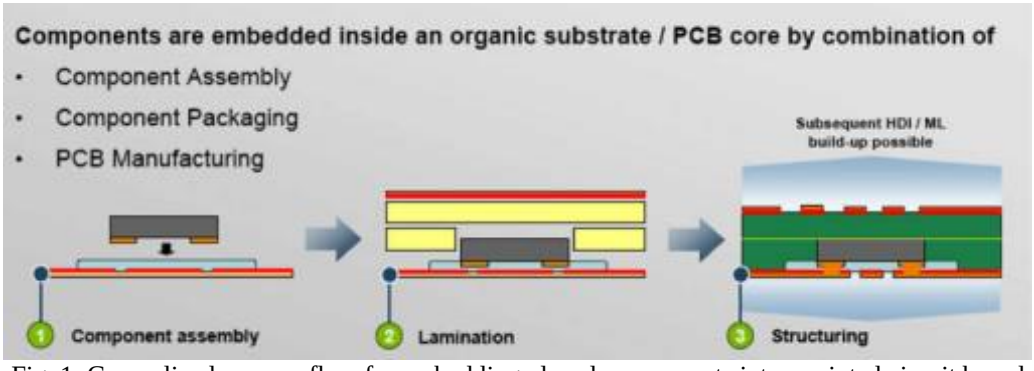

Fig. 1. Generalized process flow for embedding placed components into a printed circuit board

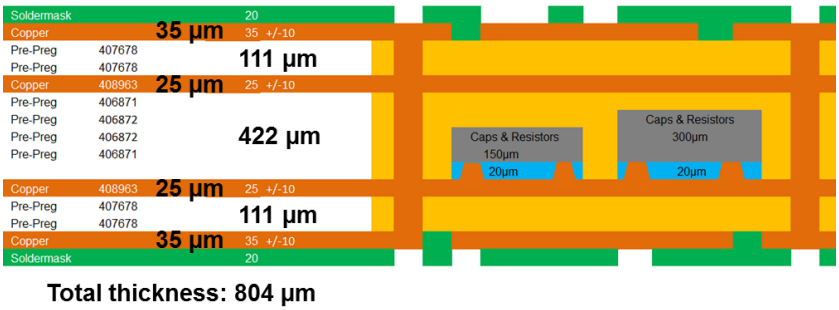

Fig. 2. Build-up and cross sectional drawing for Board Type I

While the design of the probe pad and daisy chain test structures is straightforward, evaluating the influence of embedded components on the interlayer and intralayer insulation requires a dedicated approach. Three different test structures are included in BTI: a disk test structure to verify the interlayer insulation, a comb test structure to test the intralayer insulation and a special tree test structure to evaluate the insulation between the component and a nearby plated-through hole (Fig. 3). For tests at component level (operating life) and interconnect level (vibration, mechanical shock, bending), a comparison of embedded components to surface-mount components is made. The surface-mounted components are exactly the same as the components for embedding, including the copper termination, and the test boards use the same layout.

The proposed Spacecraft Interface Module (SIM) board contains in total 624 components of which 540 are passives (resistors and capacitors) of various values and is therefore a good candidate for the study of embedding passive components. Starting from the full capacitor and resistor list, several iteration cycles were performed to obtain a condensed list of components suited for embedding in the present design. The original design was compliant with the ECSS derating rules but using this standard for the embedding components would be too restrictive in component availability. It was therefore opted not to apply derating on the embedding components and check only compatibility of the actual operating values with the maximum values of the replacement components. To minimize the risk during redesign, the build-up of the board is chosen in such a way that the design of the internal layers does not need to change. The board is a rigid-flex, twelve-layer printed circuit board with two flex cores. The components are embedded between layer 1 and 2 (connected to layer 1) and between layer 11 and 12 (connected to layer 12). In total 293 components are embedded into Board Type II of which 84 in the top embedded core and 209 in the bottom embedded core.

TEST PLAN

The Evaluation Test Plan for Board Type I is based on the test specifications of ESCC generic specification 3009 and 4001 (component level), ECSS-Q-ST-70-10C and 11C (board level), and ECSS-Q-ST-70-38C (assembly level). After manufacturing, the board with embedded components were subjected to the following incoming inspection tests:

- Visual inspection,
- Dimensional check of board and components,
- Micro sectioning with optical inspection and SEM/EDS analysis (2 boards),
- Electrical measurements of components,
- Board-level insulation resistance and dielectric withstanding voltage testing,
- Continuity and interconnection resistance.

Visual inspection, dimensional check and micro sectioning are based on the ECSS-Q-ST-70-11C PCB procurement specifications, complemented with inspection criteria related to passive components in general and component embedding in particular. Electrical measurements of resistors and capacitors are performed in accordance with ESCC generic specification 4001 and 3009, respectively. Interconnection resistance, continuity, board-level insulation resistance and dielectric withstanding voltage are modified to include the possible influence of embedded components.

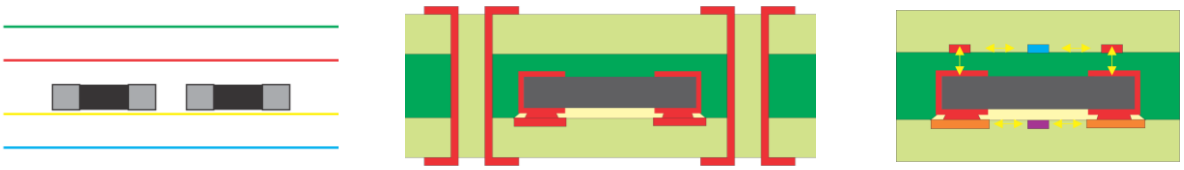

Fig. 3. Test structures for board-level insulation: disc (left), tree (middle) and comb (right)

Following the initial measurements, stress testing at board and component level was performed, including:

- Mechanical testing (vibration, shock and bending),
- Thermal cycling (-70 °C to 130 °C, 10 °/min, 500 cycles),
- Thermal stress (3x SnPb solder float at 288 °C),
- Damp heat (40 °C, 93 % RH, 240 hours),
- Interconnection stress testing (on separate coupons),
- Operating life testing (2000 h),
- Power (resistor) and voltage (capacitor) step-stress testing.

Test specifications for thermal cycling, thermal stress and damp heat are in accordance with ECSS-Q-ST-70-10C, while the IST test procedure is based on the ESA draft specification QT/2014/030/SHv2. Specifications for vibration and mechanical shock were defined in the SoW (TEC-QCT/2012SoW01/DL), while bending is performed according to the automotive test method AEC-Q200-005.
Operating life testing consists of aging the components for 2000 hours at elevated temperatures with power cycling (resistors) or at twice the rated voltage (capacitors). Step-stress testing for power (resistors) or voltage (capacitors) was included to determine the method of failure under extreme stress.
The Board Test Plan consists of the complete functional testing of BTII, including a comparison of the power and signal integrity performance with an existing SIM-FUMO board.

TEST RESULTS

From manufacturing, 24 boards with embedded components, 10 boards for surface-mount components and 10 IST coupons were available for the Evaluation Test Plan (780 resistors, 1190 capacitors and 4300 0-ohm resistors in total). Table. 1 provides an overview of the test results for the electrical measurements during incoming inspection, after stress testing and after component-level testing. Pass/fail criteria for components are the specification limits stated by the component supplier. The change in resistance after testing for interconnection resistance and continuity measurement of 0-ohm resistors should be less than 10 %. Board-level insulation is evaluated by insulation resistance measurements and dielectric withstanding voltage testing.
A resistance tolerance of 1% is difficult to achieve with embedded components. In addition, the 0201-sized embedded resistors exhibit a downward tail in their resistance distribution for which no root cause could be determined. This effect was also visible for their surface-mount equivalent, albeit to a lesser extent.
Type II capacitance and loss factor are within specification for both embedded as surface-mount components. Type I capacitance and loss factor measurements are outside of specification due to the influence of the traces connected to probe pads. Measured insulation resistance is often below specification for both embedded as surface-mount capacitors, whereas embedded type I capacitors reveal multiple outliers below 1 GΩ. No failures (I_L > 100 µA) were observed during voltage proof testing.
Embedded components have no detrimental effect on interlayer and intralayer insulation resistance nor on dielectric withstanding voltage. Loss of insulation between the component and a neighboring PTH was, however, observed and traced back to carbonized epoxy at the edge of the prepreg cavity, resulting in a conductive path between the component and the PTH.
For vibration, mechanical shock, bending and thermal cycling, no significant change in interconnection and daisy-chain resistance was observed and resistor and capacitor measurements were within specification after testing. Failures after thermal stress and damp heat testing are related to the above mentioned loss of insulation between component and neighboring PTH.
Ten test coupons with embedded 0402 and 0201 0-ohm resistors were subjected to interconnection stress testing at PWB interconnect solution in Canada. Assembly operations were simulated by six times preconditioning up to 230 °C. Cycling was performed up to 150 °C for 1000 cycles with sensing of the PTH daisy chain and the daisy chain with 0402 resistors (largest component). As no failures were observed, an additional 100 cycles up to 190 °C was performed to stress the microvia interconnection to the embedded components. Two daisy chains with 0201 resistors failed during cycling up to 190 °C when the microvia lifted from the pad at high temperature (thermal expansion due to high CTE_z of the adhesive above T_g). No failures were detected in the PTH daisy chain and the daisy chain with 0402 resistors.
The 0402-sized resistors show little effect of operating life testing. Embedded components exhibit a slight increase (<1 %) in resistance, while their surface-mount equivalents remain almost constant. Both the embedded as the surface-mounted 10 kΩ, 0201 resistors, however, started failing after 512 hours (10 % increase in total current).
Type II capacitors exhibit a significant drop in capacitance after 1000 hours of testing, while the type I capacitors show little sign of aging over the complete test duration. No clear trend can be discerned for the loss factor and insulation resistance.

Table. 1. Overview of test results for the Evaluation Test Plan for Board Type I

Test	Mounting	Resistor	Capacitor	Daisy chain	Board-level
Initial measurements	Embedded	OUT-OF-SPEC	PASS	PASS	n.a.
	SM	OUT-OF-SPEC	PASS	PASS	n.a.
Overload	Embedded	PASS	n.a.	n.a.	n.a.
	SM	PASS	n.a.	n.a.	n.a.
Board insulation resistance	Embedded	n.a.	n.a.	n.a.	BELOW SPEC
Board diel. withstanding voltage	Embedded	n.a.	n.a.	n.a.	BELOW SPEC
Vibration	Embedded	PASS	PASS	PASS	n.a.
	SM	PASS	PASS	PASS	n.a.
Mechanical shock	Embedded	PASS	PASS	PASS	n.a.
	SM	PASS	PASS	PASS	n.a.
Bending	Embedded	PASS	PASS	PASS	n.a.
Thermal cycling	Embedded	PASS	PASS	PASS	n.a.
Thermal stress	Embedded	PASS	PASS	n.a.	FAIL
Damp heat	Embedded	PASS	PASS	n.a.	FAIL
IST	Embedded	n.a.	n.a.	FAIL	n.a.
Operating life	Embedded	FAIL	FAIL	n.a.	n.a.
	SM	FAIL	FAIL	n.a.	n.a.

The SIM-BTII board passed all initial electrical tests, all field programmable gate array (FPGA) related tests and all functional tests without issues. The performance of the redesigned board with embedded passive components is on par with the standard SIM-FUMO board. No significant difference in signal, power and data integrity were observed. Important to note here is that the design was not optimized for the use of embedded components to minimize the risk of design errors impacting the functionality.
To verify the performance of the embedded capacitors, a direct comparison of the ripple on the power rail with the original SIM-FUMO board was made. No notable differences were observed with the noise levels nearly identical and the peak-to-peak values within the same order of magnitude. Line termination performance for embedded resistors was, within the measurement tolerance, identical to their surface-mounted counterparts.

RESULT ANALYSIS

Overall, it can be concluded that interconnections to embedded components are as robust as their surface-mount equivalent, if not more robust. While the embedding has some impact on the passive components itself, further improvement of the components will resolve this minor issue.
Based on a failure mode, effect and criticality analysis (FMECA), recommended actions to improve the technology are proposed. The highest risks identified in the FMECA are related to the loss of insulation at board level and at component level. The introduction of insulation testing at both board and component level during final inspection is a must. The updated guidelines for high resistance electrical test for PCBs (QT/2013/681/SH) need to be reconciled with the practicalities of boards with embedded components (e.g. insulation testing of nets connected by embedded resistors or nets with multiple parallel capacitors). A test matrix for both component value and insulation resistance measurements at end of line was proposed within the project.
A classical issue for embedded components is supply chain management. For a traditional printed circuit board assembly, the components and printed circuit board are qualified and procured separately. In the case of embedded components, PCB production becomes a three-step process: qualification of the components following current ESCC specifications, including lot acceptance testing and incoming inspection at AT&S; manufacturing of the embedded core

by AT&S as a qualified half product; and finally integration of the embedded core into a final build-up by an ESA qualified PCB manufacturer.
The most important aspects of the procurement specification are the final inspection criteria, electrical test at the PCB manufacturer and test coupon design and quantity. Test coupons with one or more representatives of the embedded components included in the board can be used to test for interconnection failures, change in component values, loss of insulation within the component or between component and a neighboring PTH.
Build-up, materials and design rules for space qualified PCBs differ significantly from current PCBs with embedded components. Other concerns that arose during the project are the lack of automated design flow for space PCBs with dedicated design rule checks and the fact that component repair is not possible. The latter can have a large impact in the final stages of a space projects, but is unfortunately inherent to the technology.

CONCLUSION

Overall, the performance of the component embedding technology is at a high level. Board Type II was fully functional and performed on par with its SMT sibling. Apart from the extreme IST test, no failures in the microvia interconnection to the component were observed on Board Type I. The most important deficiencies were related to the loss of insulation between the component and a nearby conductive surface.
The main hindrance for the use of passive component embedding in space projects is not the performance of the components, but rather the specifications of the components. The range of available component values is still limited and there is at this moment no European supply chain, except for the capacitors from AVX. A further limitation are the voltage, power and temperature ratings of the available components. Derating rules could not be uphold during the component selection for BTII. Qualification testing and lot screening of components need to be upgraded to ESCC requirements and better matched with the embedding concept.

AUTHOR

Dr. Maarten Cauwe (M) received a Degree in electronics engineering from Ghent University, Ghent, Belgium, and a Ph.D. degree from the Center for Microsystems Technology (CMST), imec and Ghent University. He is currently leading the Advanced Packaging Team at CMST, and is involved in several projects concerning substrate technologies, chip assembly, advanced interconnection, and chip embedding. His previous research work was focused on component embedding in printed circuit boards, where he was involved from the first exploratory projects (Hiding Dies, 2004-2006) until the commercial industrialization of this technology in the frame of the HERMES project (2008-2011). He recently coordinated a project on this topic in cooperation with the European Space Agency. The Advanced Packaging team, which he is leading, is composed of four highly skilled engineers in the field of packaging, pcb manufacturing, first and second level assembly, testing and failure analysis.