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ADE Assembler Flow for Rapid Design of High-Speed Low-Power Circuits

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Abstract

High-speed low-power analog circuit design typically requires multiple iterations between schematic and layout before all the specifications are met. Moreover, the overall performance of such a circuit depends on many factors, leading in many cases to a sub-optimal design. By using a combination of tools and work flows provided by Virtuoso ADE Assembler, it becomes possible to rapidly hand-off a circuit which is both cutting-edge and high-yield. To accomplish this, we propose a parasitic and variation aware design flow optimized over all corners. The effectiveness of this flow is demonstrated on a 40 Gb/s flip-flop cascade implemented in a 130 nm SiGe BiCMOS technology. In the end, we can achieve a 25 % reduction in power consumption compared to a previous taped-out design. The strong interoperation of the CAD tools in the Virtuoso suite allows to optimize the performance and yield, while reducing the number of design iterations.

Keywords: Custom IC design, Virtuoso ADE Assembler, Parasitic Aware Design, Variation Aware Design, Size over Corners

Introduction

Because of the increasing internet traffic and cloud services, the performance limits of data center interconnects are pursued. These circuits need to be state of the art in terms of low-power and high-speed operation, which constitute a challenging task for the designer. To facilitate the design problem, we propose a parasitic and variation aware work flow based on [1] using multiple features of Virtuoso ADE Assembler, see Figure 1 for a flow chart.

The first part of the flow is actually the most difficult one and determines the rest of the work flow, i.e. setting up the design specifications and creating an initial sizing of the circuit. As electrical parasitics greatly impact the performance of the high-speed circuit, cumbersome iterations between schematic and layout can be avoided or minimized by following a parasitic aware design (PAD) flow from the start. These parasitic estimates are either based on experience and/or on the Electrically Aware Design (EAD) tool that extracts parasitic elements while layouting the circuit.

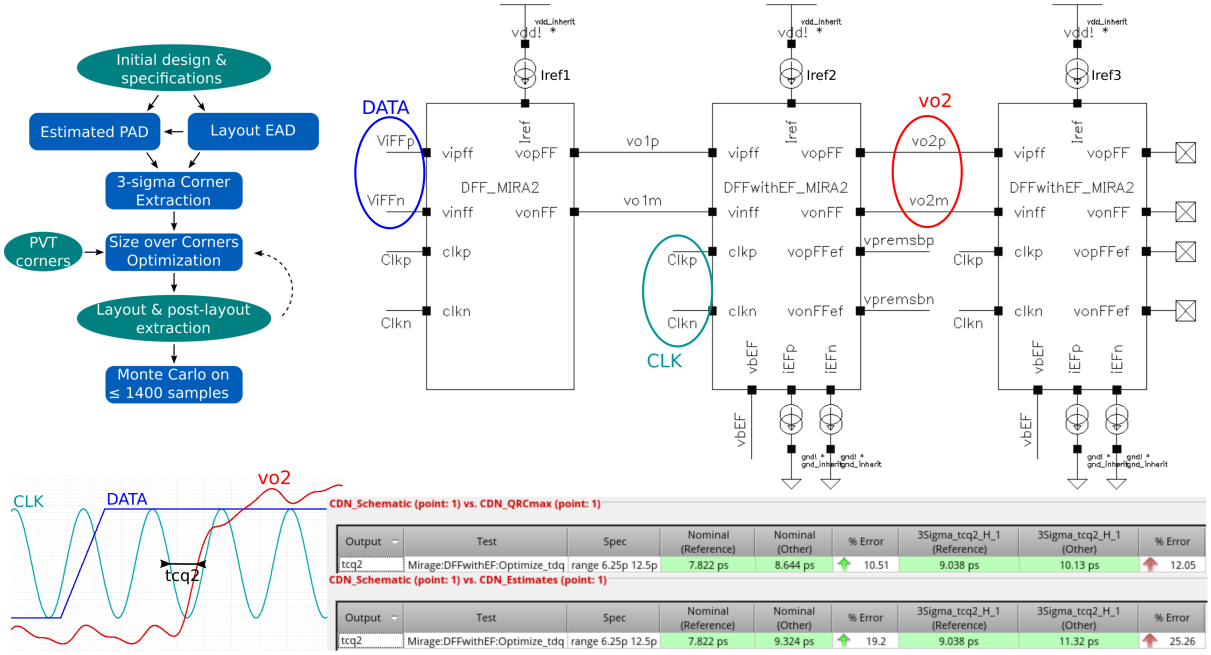
The second part of our flow comprises variation aware design and starts with a Fast K-sigma Corner Extraction of the most relevant specifications. A 3-sigma corner should result in a yield big enough for high-speed circuits, otherwise performance could be sacrificed. Simulation time is restricted to a minimum as this step requires a Monte Carlo run of only ~200 samples. Optimization across the 3-sigma corners together with additional PVT corners can be efficiently carried out using the Virtuoso Size over Corners global optimizer. The design flow continues with the circuit layout and post-layout verification and can lead to a design iteration if not all goals are met. Finally, a full Monte Carlo

analysis is executed on the worst case PVT corners. Approximately 1400 samples are sufficient to reliably extract the yield of the circuit unless the autostop option is used [1].

Following this work flow attempts to reduce the time-to-tapeout while maximizing the performance of the design. It's effectiveness will be demonstrated below on a flip-flop cascade implemented in a 130 nm SiGe BiCMOS technology.

Results

The flip-flop under test was originally part of a PAM-4 laser driver incorporating a 4-tap equalizer, totalling at two rows of five flip-flops [2]. For this paper, we will apply the described flow to significantly improve the energy efficiency. The test bench is shown in Figure 1 and consists of a cascade of 3 flip-flops in which the second flip flop drives the first equalizer tap. A data transition and a sinusoidal clock compose the stimuli to verify the crucial clock-to-output delay (tcq2) among several other parameters. The optimizer adjusts the transistor sizes until all the specifications are met while minimizing Iref2-3 independently from Iref1. The tcq2 parameter obtained from the parasitic estimated view and the post-layout extracted view are compared with the schematic view for the nominal and the 3-sigma corner in Figure 1. It can be concluded that the parasitics were over estimated. The outcome of the work flow has led to a circuit that consumes 25 % less than the flip-flop cascade from [2].



Output	Test	Spec	Nominal (Reference)	Nominal (Other)	% Error	3Sigma_tcq2_H_1 (Reference)	3Sigma_tcq2_H_1 (Other)	% Error
tcq2	Mirage:DFFwithEF:Optimize_tdq	range 6.25p 12.5p	7.822 ps	8.644 ps	10.51	9.038 ps	10.13 ps	12.05

Output	Test	Spec	Nominal (Reference)	Nominal (Other)	% Error	3Sigma_tcq2_H_1 (Reference)	3Sigma_tcq2_H_1 (Other)	% Error
tcq2	Mirage:DFFwithEF:Optimize_tdq	range 6.25p 12.5p	7.822 ps	9.324 ps	19.2	9.038 ps	11.32 ps	25.26

Figure 1: Left: Flow chart of the parasitic and variation aware design flow. Right and bottom: Part of an ADE Assembler test bench including a timing diagram and a spec comparison versus the schematic view.

Conclusions

The proposed parasitic and variation aware design flow assisted by the Virtuoso ADE suite is capable of optimizing and yield-verifying high-speed low-power circuits in a minimum amount of time.

Acknowledgments

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References

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