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Advances in Steep-Slope Tunnel FETs

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Abstract—Tunnel FETs (TFETs) with steep subthreshold slope have been attracting much attention as building blocks for future low-power integrated circuits and CMOS technology devices. Here we report on recent advances in vertical TFETs using III-V/Si heterojunctions. These heterojunctions, which are formed by direct integration of III-V nanowires (NWs) on Si, are promising tunnel junction for achieving steep subthreshold slope (SS). The III-V/Si heterojunction inherently forms abrupt junctions regardless of precise doping technique because the band discontinuity is determined by only the offset of III-V and Si, and depletion region can be controlled by the III-V MOS structure. Thus, good gate-electrostatic control with a large internal electrical field for modulation of tunnel transport can be achieved. Here we report on recent advances in the vertical TFETs using the III-V NW/Si heterojunction with surrounding-gate architecture and demonstrate steep-SS behavior and very low parasitic leakage current.

Keywords—Tunneling FET; III-V compound semiconductors; nanowires; heterojunction

I. INTRODUCTION

The main goal for future electronics is that power consumption of integrated circuits and IoT devices should be reduced to ultralow level and the performance of these devices should be enhanced. A simple but difficult approach to decreasing the power consumption of MOSFETs is to lower the supply voltage (V_{dd}), since the active power of integrated circuits is proportional to the square of the V_{dd} and stand-by power is proportional to the V_{dd} and off-state leakage current (I_{off}). The V_{dd} is determined by the subthreshold slope (SS) and the difference in on-state current (I_{on}) with I_{off} . Therefore, The V_{dd} is expected to be decreased effectively by enhancing the I_{on} under the low bias, reducing I_{off} by suppressing the short-channel effect, and minimizing the SS. In this regard, Si-based CMOS technologies with multi-gate structure [1,2], new channel materials [3], and non-classical switching mechanism [4] reducing power dissipation are expected to be utilized as extended complementary MOS (CMOS) technologies. These distinct features should be mutually addressed in extended CMOS technologies and then these technologies should eventually be integrated as a vertically stacked chip (Fig. 1).

The I_{off} will be decreased by changing the multi-gate structure to a gate-all-around or surrounding-gate structures [2], in which the gate-metal is wrapped around the channel in order to provide the best electrostatic control of the gate possible. Especially, the vertical surrounding-gate architecture would

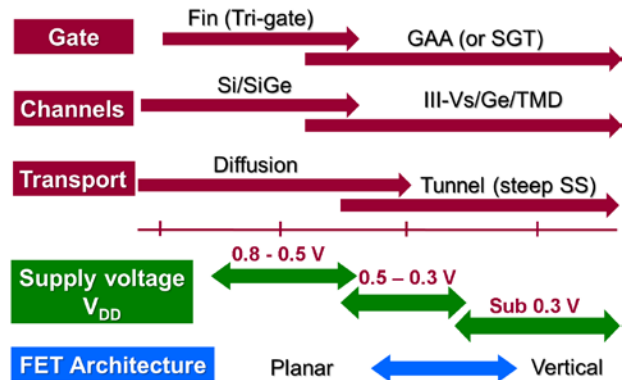


Fig. 1. Evolution scenario of state-of-the-art CMOS technologies

exhibit geometrical and performance advantages in 7-nm-node devices [5].

Changing the channel material from strained SiGe to a III-V, Ge, or two-dimensional transition metal dichalcogenide (2D TMD) is expected result in a higher ON-state current under lower bias because these materials have a higher carrier mobility and lower electron/hole effective mass. Since these materials tend to exhibit slightly high leakage current due to tunneling leakage, a multi-gate architecture would necessary for decreasing leakage current. Furthermore, the inherent mobility mismatch between the n/p-channels will be a bottleneck in future device-integration schemes to match current density. In the near future, the only way to avoid this bottleneck will be to use a vertical channel architecture. In this regard, technique integrating a vertical III-V channel with p-channel Ge will be needed for making Si-CMOS devices. We have already reported that the bottleneck has been avoided by integrating vertical III-V NWs directly on Ge substrates [6].

The switching mechanism in conventional FETs involves carrier thermal diffusion and drift limiting the SS at room temperature (RT) to $2.3 k_B T/q \sim 60$ mV/decade. This physical limitation will stop further scaling of power consumption in integrated circuits. Steep-SS transistors with SS < 60 mV/decade are, therefore, required for further reductions in V_{dd} and power dissipation. Steep-SS transistors such as tunnel FETs (TFETs) [4], impact ionization FETs [7], and mechanical switches [8] have thus attracted a great deal of attention. Of these steep-SS transistors, TFETs whose switching mechanism involves band-to-band tunneling [9] or Zener tunneling [10] are promising steep-SS switches for the building-blocks for future LSIs because their configurations are compatible with those of

conventional Si-based FETs and tunneling is induced under an internal electric field than those of other switches

Using TFETs with an SS <30 mV/decade would reduce the total power consumption of integrated circuits by over 90% because reducing SS decreases V_{dd} . Therefore, various TFETs using Si [11,12], III-V materials [13 – 15], and graphene [16,17] have been investigated, and semiconductor nanowires (NWs) have also been investigated. These TFETs, however, all had difficulties in attaining sufficient steepness (SS <30 mV/decade) owing to significant challenges, such as those associated with the precise doping techniques needed to form abrupt p-n junctions. In this regard, combining Si and III-V materials in one-dimensional (1D) nanostructures could provide a decisive solution to the problem because III-V/Si interfaces formed by integrating III-V NWs on Si have inherently abrupt junctions with band discontinuity [18, 19]. And atomically flat junction utilizing 2D-TMD/p-Ge heterojunction have been demonstrated as tunnel junctions [20].

In this paper, we report on recent advances in vertical TFETs using III-V/Si heterojunctions. We used selective-area metal-organic vapor phase epitaxy (MOVPE) for the direct integration of III-V NWs on a Si(111) substrate. Reducing the opening diameter of the masked substrate decreased the numbers of misfit dislocations. The TFETs made by using III-V NW/Si heterojunctions demonstrated steep-SS properties at room temperature. One of the key issues in the vertical TFETs is the formation of intrinsic channels inside the tiny NW-body and another is the reduction of NW-diameter. We also discuss several current-boosting technologies for the TFETs.

II. III-V NWs AND III-V/SI HETEROJUNCTION

A. Direct integration of III-V NWs on Si/Ge

Selective-area MOVPE was used to form vertical III-V NW-channels. This method is a template method combining bottom-up (crystal growth) and top-down (lithography) approaches, and does not need any metal catalysts. This

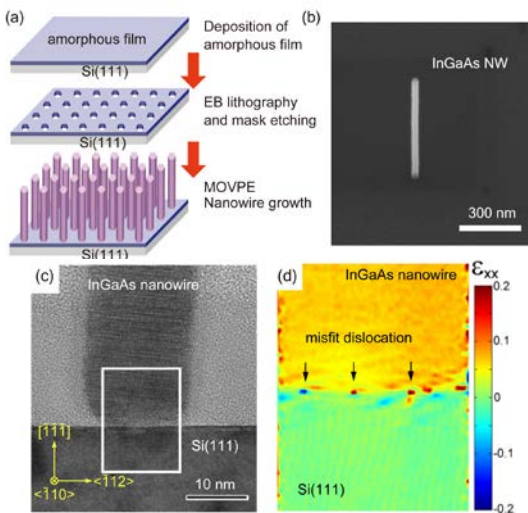


Fig. 2. (a) Growth process for selective-area growth, (b) representative SEM image of InGaAs NW on Si, and (c) TEM image (d) Strain analysis of the area outlined in white in panel (c). The xx direction indicates $<112>$ direction.

method utilizes a faceting mechanism in which the grown structure is surrounded by the low-index planes whose growth rate is slow. In this mechanism, $\{-110\}$ vertical facets can appear on a (111)B-oriented surface under specific growth conditions. Fukui *et al.* demonstrated the formation of rectangular-shaped GaAs wire surrounded by the $\{-110\}$ vertical facets on a GaAs(111)B substrate [21].

A hexagonal pillar shape surrounded by six $\{-110\}$ facets can also be formed by the growth mechanism. The use of (111)B- or (111)A-oriented substrates enables vertically aligned hexagonal pillars to be formed. Thus, the direction of preferential growth is $<111>$ B or $<111>$ A normal to the (111)B or A substrates. However, Si has such polarity, and Si(111) surface has both (111)A and (111)B oriented surfaces. As a result, the growth direction of III-V NWs becomes vertical and inclined. Thus, we have to control these growth directions to form the vertical $<111>$ direction to create a rational design for NW applications to take advantage of the geometries. We have recently reported the formation of a (111)B-oriented surface on the Si(111) surfaces and demonstrated the integration of vertical III-V NWs on Si(111) and Ge (111) substrates by selective-area MOVPE [00-00]. Representative results for growth of InGaAs NW with a 20-nm diameter can be seen in Fig. 1(c). The NW had no defects originating from the anti-phase domain; rather, strain analysis showed misfit dislocations at the InGaAs NW/Si interface. The periodicity of the dislocation became greater than the value calculated from the lattice mismatch.

B. Misfit dislocations at III-V NW/Si junctions

The number of misfit dislocations at the III-V NW/Si heterojunction can be controlled by adjusting the NW-diameter (or opening diameter) [22]. Fig. 3 shows the number of misfit dislocations as a function of III-V NWs/Si heterojunction diameter, which indicating that the number of misfit dislocations falls below the number calculated from the lattice mismatch. InAs NW/Si and InGaAs NW/Si had lattice mismatches of 11.6 and 8.1%, but the numbers of misfit dislocations decreased with the heterojunction diameter. As for GaAs NW on Si, misfit dislocation was virtually suppressed with a NW diameter of 19 nm, which is due to coherent growth. This coherently grown III-V/Si heterojunction is the ideal

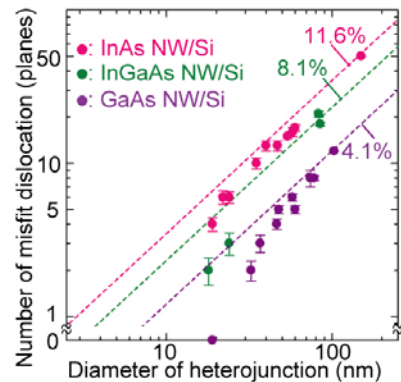


Fig. 3. Misfit dislocation with a variation of diameter of heterojunction. Dashed lines represent calculated number from lattice mismatch.

tunnel junction to induce only band-to-band-tunneling with high heterojunction-resistance. Note that the misfit dislocation forms defect level across the III-V/Si junction, resulting in the trap-assisted tunneling process [23]. When trap-assisted tunneling transport is the dominant process in a TFET, the heterojunction resistance decreases with increasing SS because of the internal electrical field.

C. Diode properties for the III-V NW/Si junctions

As shown in Fig. 4(a), two-terminal device for diode characterization was first fabricated on *p*-Si substrate with various carrier concentrations. In this case, the diameter of InGaAs NW was 70 nm. The device process has been previously reported [18,24]. The current density (J_D)-voltage (V) curve (the Si substrate was grounded) is shown in Fig. 3(b). The measured current was divided by the number of NWs and normalized by the surface contact area. In this case, positive voltage is in the reversed bias direction against p-i-n junction. The J_D -V curve shows typical rectification properties under forward bias ($-1.0 < V < 0$), with an ideality factor of 1.9. The J_D under reverse bias ($0 < V < 1.0$) increases with the carrier concentration of *p*-Si.

Figure 4(d) shows a band diagram calculated by a one-dimensional Poisson-Schrödinger equation [22, 25], and in that figure the band diagram is staggered Type-II band discontinuity. In this calculation, we set the carrier concentration of *p*-Si to $1 \times 10^{18} \text{ cm}^{-3}$. The current in the reverse direction is found to be Zener tunneling transport across the InGaAs NW/Si heterojunction similar to the current in the InAs NW/Si heterojunction [Fig. 4(b)], and the current is increased as carrier concentration increases. In the case of a heavily doped *p*-Si substrate ($n = 1 \times 10^{20} \text{ cm}^{-3}$), Esaki tunneling transport is also observed under the forward bias direction ($V = -0.3 \text{ V}$). This is because the position of the Fermi level lies underneath the valence band in *p*-Si for $n = 1 \times 10^{20} \text{ cm}^{-3}$. These behaviors suggest that controlling the position of the

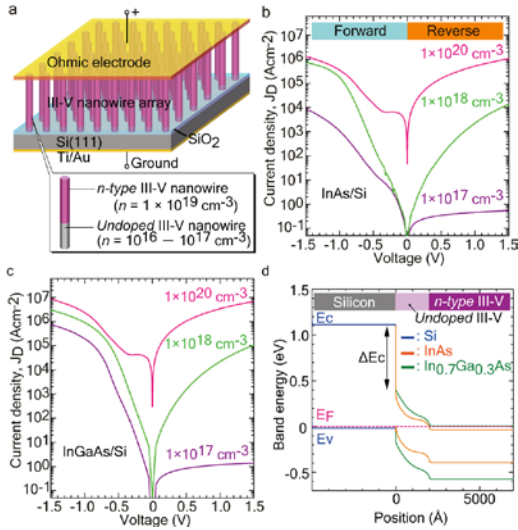


Fig. 4. (a) Illustration of diode structure consisting of 250 III-V NWs on *p*-Si substrate. Diode characteristics for InAs NW/*p*-Si (b), InGaAs NW/*p*-Si (c). The inset numbers denote the carrier concentration of *p*-Si. (d) Band structure calculated by one-dimensional Poisson-Schrödinger equation.

Fermi level by using various electrical fields modulates the tunneling transports induced at the III-V NW/Si heterojunction

III. VERTICAL TUNNEL FETs USING III-V/Si JUNCTION

A. Quality of MOS interface in vertical III-V NW-FETs

Before demonstrating a vertical TFET using III-V NWs/Si heterojunctions, we show the quality of MOS structure for the vertical III-V NW architecture because the vertical TFET has surrounding-gate architecture and formation of a high-quality MOS interface is a precondition for achieving a steep SS in the TFETs. The idea and the demonstration of surrounding-gate transistors (SGTs) were first reported by Takato *et al.* [2]. The main advantage of the vertical surrounding-gate structure was to induce the best electrostatic gate-bias control in the channel due to the wrapped gate metal, and this enabled the occupied area to be reduced to allow denser integration.

The SGT structure of a single InGaAs NW on Si is outlined in Fig. 5(a) [26, 27]. The In composition was 70%. We used a gate-first process and etch-back procedures to make the SGT device [26 – 30]. Fig. 5 show electrical properties of the InGaAs NW-SGT with an effective-oxide thickness (EOT) of 0.75 nm. The NW was 80 nm in diameter. The gate leakage current (I_G) with an EOT = 0.75 nm was moderately lower than that previously reported [29]. I_D was reasonably modulated by V_G with an SS of 68 mV/dec. The drain-induced-barrier-lowering (DIBL) was 33 mV/V. The small SS close to the ideal SS ($\sim 60 \text{ mV/dec}$) and the small DIBL reflect the geometrical advantage of the electrostatic gate bias for the surrounding-gate structure. The SS was almost completely constant with the variation of EOT in Fig. 5(c). According to a simple approximation from the SS, the interface state density (D_{it}) was estimated to be from $1.8 - 3.9 \text{ cm}^{-2}\text{eV}^{-1}$. The extraordinarily low D_{it} for the InGaAs{-110} surface/HfAlO interface is thought to be due to formation of (111)A/B microfacets on the sidewalls of the nanowire-channel. However, the I_{ON} is lower than those of conventional CMOS transistors.

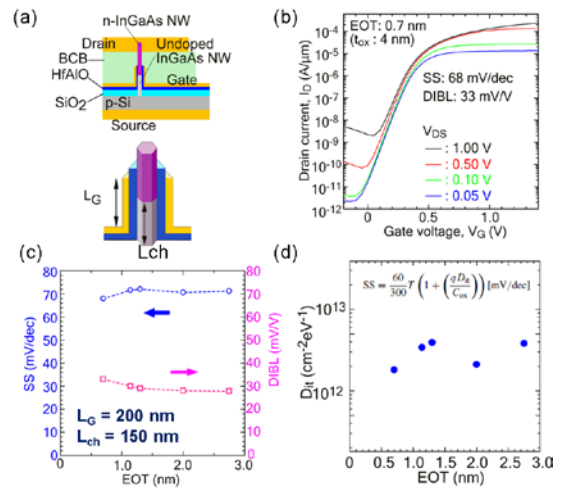


Fig. 5. (a) Illustration of SGT structure. The actual device in this case has 10 NWs in parallel with drain contact. (b) Transfer characteristics for InGaAs NW-SGTs on Si with a gate-oxide 4-nm-thick (EOT = 0.75 nm). (c) SS and DIBL with a variation of EOT, (d) D_{it} estimated from panel (c).

B. Primitive performances for TFET using In(Ga)As NW/Si

Figure 6(c) shows representative transfer characteristics of the fabricated In(Ga)As NW/Si TFET at drain-source voltages (V_{DS}) of 0.05 – 1.00 V. The curves were measured using a parameter analyzer (Agilent 4156C) at room temperature in the dark. The gate voltage (V_G) ranged from – 1.50 to +1.50 V. The current values were normalized using a cross-section of the gate length. Switching properties with a SS of 260 mV/dec were observed in the reverse bias direction (V_G is positive for the n-i-p junction). The SS for an InAs NW/Si vertical TFET was 120 mV/dec at RT.

Almost all reports regarding TFETs mention performance degradation due to degradations in device architecture and the tunnel junctions. This is because the device structure is somewhat degraded, so it cannot induce a large internal field at the heterojunction, in our case III-V NW-channels, under low V_{DS} and V_G . Since the SS is a function of V_G and V_{DS} , the series resistance of the device must be adjusted to minimize the SS. This device thus requires a large internal field induced under lower V_G and V_{DS} . We discuss two approaches to achieve steep SS in vertical TFET with new tunnel junctions.

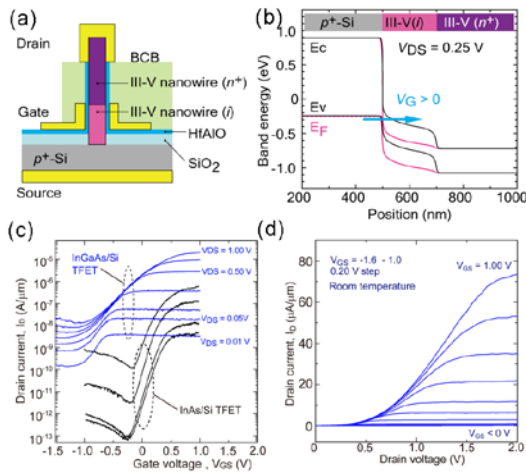


Fig. 6. (a) Illustration of vertical TFET using III-V/Si junction. (b) Simulation of TFET. (c) Transfer curve of vertical TFET using a single In(Ga)As NW/Si heterojunction. The InGaAs NW was 70 nm in diameter. Inset shows the InAs NW/Si heterojunction TFET reported in REF.18. (d) Output property.

C. Effect on NW-diameter scaling

To achieve steep SS in the case of InAs NW/Si heterojunctions, InAs NW diameters must be reduced while reducing the number of misfit dislocations and increasing the contact area to reduce effective the contact resistance [19]. Achieving coherent growth without misfit dislocations that suppress trap-assisted tunneling was predicted to result in steep SS [22, 23], but such a small opening pattern is difficult to form. A device using an InAs nanowire (30 nm in diameter)/Si heterojunction demonstrated a steep-SS (minimum SS = 12 mV/dec) at room temperature (Fig. 7) [19]. There are two SS regions in this device's properties. The SS is very steep in the early stage of gate modulation, but at higher V_G becomes ~ 110 mV/dec. The physical origin of these SS regions remains under

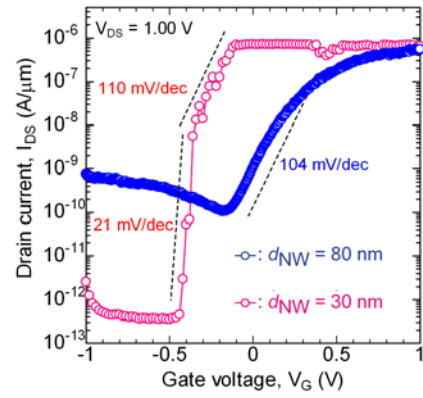


Fig. 7. Transfer curve for vertical TFETs using InAs NW/Si heterojunctions. $V_{DS} = 1.00$ V.

investigation, but two mechanisms (BTBT and TAT) are assumed to be contributed.

D. Doping effect in channel region

Forming an intrinsic layer by using the compensation effect is discussed as an alternative approach to improving the SS of an InGaAs NW/Si heterojunction TFET. Key issues are the carrier density in undoped parts of the III-V NW, modulation of surface accumulation for the III-V NW, and reducing the diameter of III-V NW/Si heterojunction. Ideally, the pure intrinsic III-V NW channel is required to induce a large internal field at the III-V NW/Si heterojunction under small bias. In our device, however, undoped InGaAs NWs have slightly high carrier density owing to unintentional n-type doping ($10^{16} - 10^{17}$ cm^{-3}) during MOVPE [31], which is probably caused by MO precursors. This unintentional doping in the InGaAs NW-channel lowers the internal fields due to V_G and V_{DS} because it lowers the channel resistance. This means large bias is required for inducing tunnel transport, resulting in a SS of 60 mV/decade. Accordingly, a compensation doping with a p-type dopant was used during the growth of the nominally undoped InGaAs NW-channel. In this case, Zn atoms from diethylzinc (DEZn) were used to compensate for the unintentional doping in the InGaAs NW. The carrier concentration due to only a single Zn atom, however, is estimated to be about 2×10^{17} cm^{-3} in such a small NW-channel. Then we implemented a pulse-doping technique [22,25] to obtain the compensation effect. In the case of the Zn pulse-doped InGaAs NW-channel, the threshold voltage (V_T) for the SGT shifted to 0.389 V and the carrier concentration was estimated to be 7.8×10^{15} cm^{-3} . The N_D was decreased by using a Zn-pulse doping technique.

Figure 8 shows the transfer curves of a TFET using the InGaAs NW/Si heterojunction with the Zn pulse-doped InGaAs NW-channel [22,25]. The NW was 30 nm in diameter. The channel length corresponds to that of Zn-pulsed region, 200 nm in this case. By using the pulsed doping technique, we were able to improve the SS compared to an undeoprd InGaAs NW-channel in Fig. 7(a). The advantage of the III-V/Si junction for steep-SS switches is its suppression of parasitic leakage current due to band discontinuities across the III-V/Si heterojunction. In this InGaAs nanowire/Si heterojunction switch, the parasitic leakage current was suppressed effectively

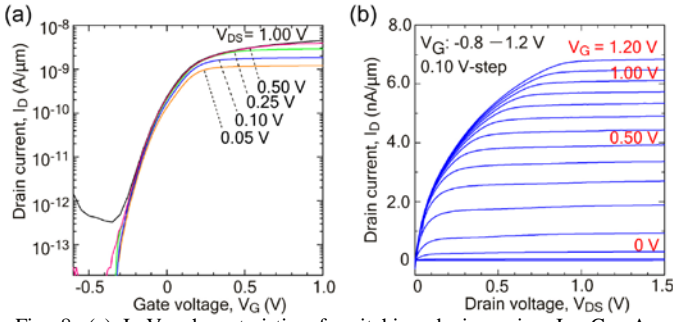


Fig. 8. (a) I_D - V_G characteristic of switching device using $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ NW/Si heterojunctions with an EOT of 1.91 nm. L_G was 150 nm. The d_{NW} of InGaAs NW was 30 nm. A minimum SS was 23 mV/dec, and the ON/OFF ratio was about 10^5 . (b) The output characteristic of a switching device using a single $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ NW/Si heterojunction with an EOT of 1.91 nm. The ON-state current was 3.8 nA/ μm with $V_{\text{DS}}=V_G = 0.50$ V and was 6.0 nA/ μm with $V_{\text{DS}}=V_G = 1.00$ V [32].

and the minimum SS became < 60 mV/dec under lower V_G . The minimum SS was 23 mV/dec and the average SS over two decades ($10^{-13} - 10^{-11}$ A/ μm) was 40 mV/dec at $V_{\text{DS}} = 0.25$ V. However, the SS becomes larger as V_G increases. This is because the tunneling transport involves pure band-to-band tunneling and trap-assisted tunneling since the InGaAs NW/Si heterojunction has misfit dislocation as shown in Fig. 2. Therefore, reducing the InGaAs nanowire-diameter and achieving coherent growth without misfit dislocations would enlarge the steep-SS region. An additional technique to boost I_{ON} is required for InGaAs NW/Si heterojunction tunnel FETs.

IV. CURRENT-BOOSTING TECHNOLOGIES FOR VERTICAL TFETs

A. Effect of channel-length scaling

Next, we investigated the scaling effect of channel length (L_{ch}) [25]. Fig. 9(a) shows the L_{ch} dependence of the transfer curve at a V_{DS} of 0.10 V. The L_G was fixed to 150 nm. And the growth condition and Zn pulse-doping sequence were the same for the different L_{ch} . We chose a low V_{DS} to characterize steep turn-on behavior. Fig. 9(b) shows SS as a function of drain current. The steep-SS region (< 60 mV/decade) in Fig. 9(b) tends to widen with decreasing L_{ch} . The current at the boundary from sub- to super-60 mV/decade (I_{60}) [33] also increases for shorter L_{ch} . The I_{60} was 10^{-12} A/ μm for $L_{\text{ch}} = 50$ nm. Thus, an internal electrical field with short L_{ch} was effectively induced as compared to the longer L_{ch} . Another effect of scaling in L_{ch} is enhanced I_D . The I_D in Fig. 3(a) achieved with short L_{ch} reached 10^{-7} A/ μm , which is 100 times that obtained with the longer L_{ch} . This indicates that a source edge would be better close to the tunnel junction to enhance I_D since tunneling carriers are subject to influence from scattering processes in longer channels. In addition, the device structure in this case had no ideal well-gated structure at the heterojunction. The scaling on L_{ch} to increasing I_D expected to be predictably-effective for $L_{\text{ch}} < 10$ nm because the tunnel distance is usually several nanometers. Thus, scaling L_{ch} has a synergetic effect increasing both I_{60} and I_D .

B. Effect of strain

The benefit of the nanowire-based vertical TFET is that it can utilize both a passivation effect and strain effect induced by

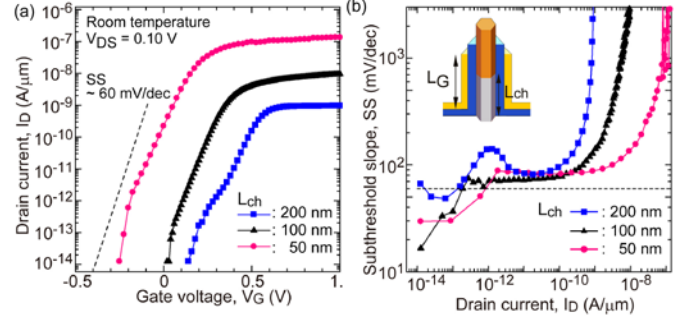


Fig. 9. (a) Transfer characteristics with variation of L_{ch} . V_{DS} is 0.10 V at RT in the dark. Dashed line shows theoretical limitation of carrier thermal diffusion (SS ~ 60 mV/decade). (b) Subthreshold slope as a function of I_D . Dashed line is SS 60 mV/dec. Inset illustrates NW-channel. Note that the device (made with pulse doping) was different with characterization in Fig. 8.

core-shell structure. The direct integration can be used to make various types of core-shell NW structure. Here we characterize the InGaAs NW/Si heterojunction TFET with surrounding-gate structure and the effect of an InP shell layer on the TFET's properties.

Figure 10(b) shows representative transfer properties of the InGaAs-InP core-shell NW/Si TFET at drain-source voltages (V_{DS}) of 0.05 – 1.00 V. The measured current was normalized using gate-perimeter. Switching behavior with a SS of 42 mV/dec was obtained under reverse bias (V_{DS} is positive against the n - i - p junction). This switching characterization appeared at V_{DS} as low as 10 mV. The SS of the TFET exhibits steeper SS behavior under various V_{DS} . The $I_{\text{ON}}/I_{\text{OFF}}$ current ratio was approximately 2.5×10^4 at a V_{DS} of 0.50 V. The on- and off-state currents were about 2.5×10^{-8} and 1.0×10^{-12} A/ μm , respectively. The V_T of the I_{DS} was -0.10 V. This device indicated the dark Zener current of the diode structure was modulated by the V_G . The I_{ON} was ~ 27 nA/ μm at $V_{\text{DS}} = V_G - V_T = 0.50$ V. The DIBL was 3 mV/V, which is much smaller than that of a conventional MOSFET. This indicates that the internal electrical field is applied at the tunneling junction regardless of surface potential lowering due to V_{DS} . Instead, I_{OFF} due to tunneling leakage was increased at $V_{\text{DS}} = 1.00$ V.

The pink dashed curve in Fig. 10(b) shows the transfer property of a InGaAs NW/Si TFET at $V_{\text{DS}} = 0.50$ V. The TFET using the bare InGaAs NW had a SS of 80 – 90 mV/dec and the I_{ON} was 2.7 nA/ μm . The I_{ON} of the InGaAs-InP core-shell NW/Si TFET was 10 times higher than that of the bare InGaAs NW/Si TFET. The benefit of using an InP shell layer is that it improves the SS and increases the I_{ON} . The InP shell layer has a passivation effect on the semiconductor/oxide interface [34], one that decreases interface-state density and thus results in electrostatic improvement of the SS below 60 mV/dec. The strain effect of the InP shell layer also contributes to the improvement of SS and I_{ON} . The outer InP shell induces biaxial tensile strain in the whole core-InGaAs NW because of the lattice mismatch (-1.16%), and this is ascribed to the uniaxial compressive strain, localized near the tunneling junction (InGaAs/Si junction), along the axial direction. The compressive strain is assumed to lower the conduction band.

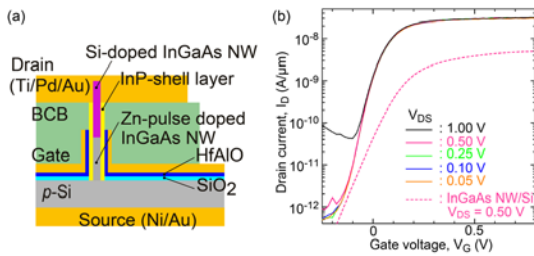


Fig. 10. (a) Illustration of vertical TFET structure. Gate length (L_G) was 200 nm. Thickness of HfAlO was 10 nm. The d_{cs} and d_c were 70 and 50 nm, respectively. The NW length was 1.8 μm . The length of Zn pulse-doped segment was 200 nm. (b) Experimental transfer properties of the vertical TFET using InGaAs-InP core-shell NW/Si. The dashed curve is the transfer curve of a TFET using InGaAs NW/Si heterojunction.

minimum of the core InGaAs NW and thus decreases the effective energy-gap across the Si and InGaAs junction. In Fig. 4(d), the conduction band of such strained InGaAs NW-channel is close to that of InAs NW. Thus, the lowered energy-gap increases tunneling probability and I_{ON} . Further characterization is required for clarify the actual local strain.

V. SUMMARY

We have reported on recent advances in vertical TFETs using III-V/Si heterojunctions formed by the hetero-integration of III-V nanowires on Si. Recent challenges with steep-SS switches using III-V NW/Si heterojunction were also discussed. We investigated the effect of increasing current by using a core-shell structure. Using the shell layer to enlarged collection area for the tunneling carrier was found to be an effective approach to increasing the tunnel current under low drive voltages. In addition, we identified the optimum device structure for attaining steeper-SS switching in III-V nanowire/Si heterojunction TFET structures. Our next target is to integrate these high-performance III-V NW SGTs and TFETs based on III-V nanowire/Si junctions into a Si-LSI platform on which we can build fundamental circuits.

VI. ACKNOWLEDGEMENT

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