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Analytical Comparison of Dual-Input Isolated dc-dc Converter with an ac or dc Inductor for Renewable Energy Systems

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***Abstract*—This paper presents two configurations of dual-input (DI) or three-port (TPC) isolated dc-dc converters for hybrid renewable energy systems such as photovoltaics and batteries. These two converters are derived by integrating an interleaved boost converter and a single-active bridge converter with an ac inductor as a power interfacing element or phase-shift soft-switching converter with an output dc inductor. Both converters are controlled by a pulse-width modulation and phase-shift hybrid modulation scheme. The two converter topologies are, even though quite similar from the topological and control perspective, distinct in operation principles, voltage/power transfer functions, loss distributions, soft-switching constraints, and power efficiency under the same operating conditions. Moreover, the inductor design differs greatly between these two cases. In this paper, a comprehensive comparison is given for the first time and thereby the corresponding design tradeoffs are discussed. Finally, a laboratory 1 kW prototype is constructed and tested to verify the theoretical analysis.**

Keywords*—Converter; dc-dc; multiple inputs; renewable energies; soft swtiching.

I. INTRODUCTION

Applying clean and renewable energies, such as wind energy, solar and hydrogen, has become a research focus in academia and industry over the last decades [1]-[3]. Due to the intermittent feature of renewable energy sources, energy storage units are needed to fill up the gap between electricity generation and consumption. Moreover, hybridizing energy sources can distinctly improve system performance in terms of decreasing cost, isolating energy sources from load fluctuations and enhancing dynamics. Hence, hybrid energy conversion systems are well suited for the applications in which the average power demand is low, whereas the load dynamics are relatively high [4]-[6]. For instance, [3] presented and compared different power electronic interfacing solutions for a reversible fuel cell with auxiliary power sources (APS) to overcome the drawbacks of fuel cell systems such as slow dynamics. Moreover, in order to efficiently regulate output voltage, which normally has large voltage difference from input ports, as well as to provide galvanic isolation, many fully or partially isolated three-port dc-dc converters with high frequency transformers have been proposed and studied in recent years [7]-[14]. An example of forming a partially isolated converter with two input voltage sources is illustrated in Fig. 1. The topology proposed in [8] and

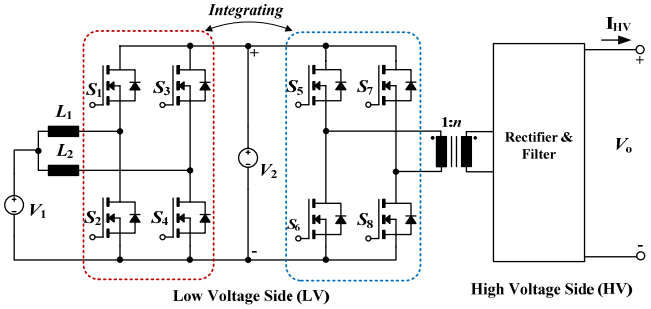

Fig. 1. Derivation of partially isolated three-port converter (TPC).

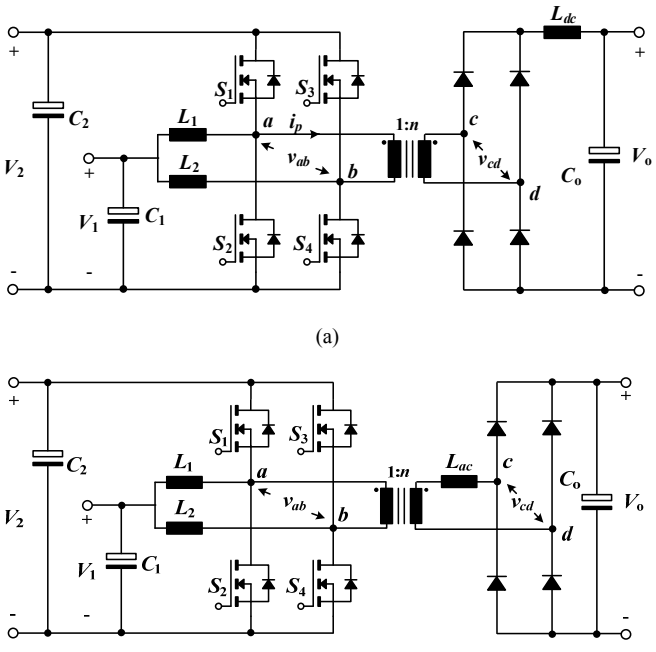

Fig. 2. Topologies of two dual-input (DI) converters. (a) dc-inductor based topology, and (b) ac-inductor based topology.

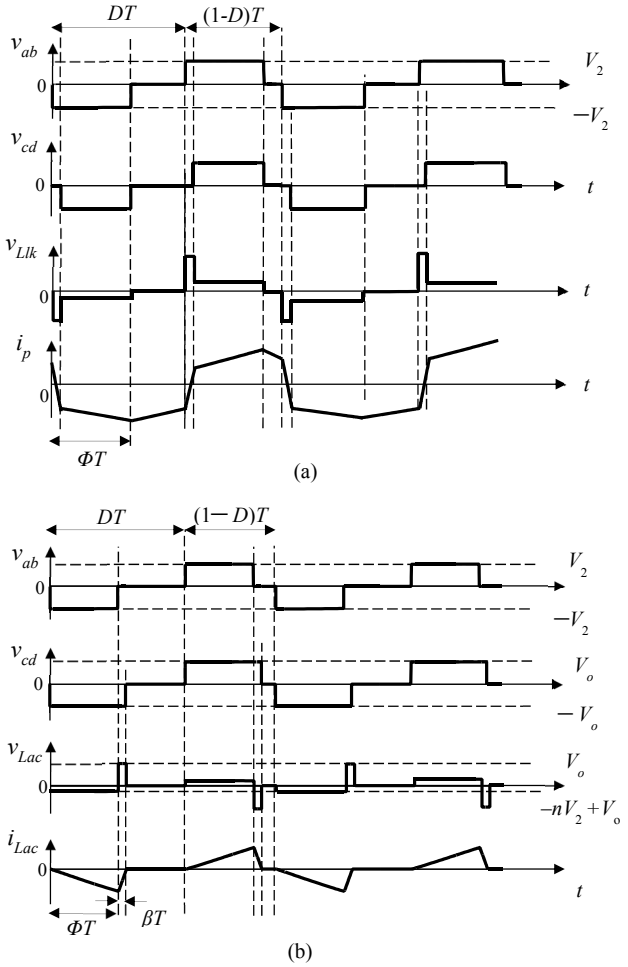

Fig. 3. Typical waveforms of the studied topologies: (a) dc-inductor based topology, and (b) ac-inductor based topology.

[9] and its derivations were obtained by integrating a two-phase interleaved boost converter into a phase-shift full-bridge (PSFB) converter, as shown in Fig. 2 (a), where an LC filter is implemented at the output port. The major drawbacks for PSFB converters, such as duty cycle losses due to leakage inductance, large circulating current during freewheeling periods and limited zero-voltage switching (ZVS) for the lagging-leg switches have been studied in the last decade. Moreover, in buck-type topologies the rectifier diodes must be able to block a voltage higher than the dc output, thereby, leading to high losses in applications such as single-phase or three-phase grid-connected systems where 400 V or 800 V dc-link voltages, respectively, are required. An alternative topology, shown in Fig. 2 (b), based on an ac inductor was studied in [14] and [15]. Since the ac-inductor based converter is derived from the dual-active-bridge (DAB) converters, the operating waveforms, loss distribution, and soft-switching operation are different from that of the dc-inductor configuration in Fig. 2 (a). In this paper, the two topologies with either dc or ac inductor are investigated and compared comprehensively based on the same specifications.

II. Operation Principles

Comparing Fig. 2 (a) with Fig. 2 (b), it can be seen that the only difference is the location of the inductor employed on the secondary side. In these two converters, even though the switches are controlled by the same method, i.e. pulse-width-modulation (PWM) plus duty cycle control, the operating waveforms are different as illustrated in Fig. 3.

From the key waveforms shown in Fig. 3 it can be observed that if the phase-shift angle, Φ, is kept smaller than the duty cycle (D) and its complement ($1-D$), i.e. $\Phi < \min[D, (1-D)]$, the two control parameters, duty cycle D and phase-shift angle Φ, are completely decoupled. Therefore, in this operation mode the energy transferred to the output port is not directly regulated by the duty cycle. Instead, the power between V_1 and V_2 is controlled by D and the power flow delivered to the output port is regulated by Φ as shown in (1)-(5).

The relationship between V_1 and V_2 is governed by the voltage gain of a boost converter as:

$$V_2 = \frac{V_1}{1-D}. \tag{1}$$

Correspondingly, the output voltage (V_o) for the dc-inductor and the ac-inductor based topologies can be derived from the typical operating waveforms in Fig. 3 as shown in (2) and (4), respectively, where n is the transformer turn ratio defined as $N_s : N_p$.

$$V_{o\_dc\_ind\_based} = \frac{2 \cdot n \cdot V_2}{1+m} \cdot \Phi. \tag{2}$$

$$m = 4 \cdot n^2 \cdot L_{lk} \cdot R_L \cdot T << 1 \tag{3}$$

where L_{lk}, R_L and T represent the leakage inductance, the equivalent load resistance, and the switching period, respectively.

$$V_{o\_ac\_ind\_based} = \frac{n \cdot V_2}{k} \cdot \Phi \cdot \left(\sqrt{\Phi^2 + 2k} - \Phi \right) \tag{4}$$

$$k = \frac{2 \cdot L_{ac}}{R_L \cdot T} \tag{5}$$

III. Component Stress Factor (CSF) Analysis

To compare different topologies under certain conditions, component stress factors (CSFs) can be used to indicate the converter stresses and thereby show a quantitative measure of converter performance [17]. CSF analysis is based in the assumption that the studied topologies must have the same amount silicon, magnetic material and capacitor volume. Therefore, three separate components i.e. the semiconductor component stress factor (SCSF), the winding component stress factor (WCSF) as well as the capacitor component stress factor (CCSF) can be defined in (6)-(11), respectively.

$$SCSF_i = \frac{\sum_i W_i}{W_i} \cdot \frac{V_{\max}^{\ 2} \cdot I_{rms}^{\ 2}}{P_{out}^{\ 2}} \tag{6}$$

$$WCSF_i = \frac{\sum_i W_i}{W_i} \cdot \frac{V_{\max\_avg}^{\ 2} \cdot I_{rms}^{\ 2}}{P_{out}^{\ 2}} \tag{7}$$

$$CCSF_i = \frac{\sum_i W_i}{W_i} \cdot \frac{V_{\max}^{\ 2} \cdot I_{rms}^{\ 2}}{P_{out}^{\ 2}} \tag{8}$$

$$SCSF = \sum_i SCSF_i \tag{9}$$

$$WCSF = \sum_i WCSF_i \tag{10}$$

$$CCSF = \sum_i SCSF_i \tag{11}$$

where W_i is the amount of resources assigned to the specific component, which represent a weighting factor. For instance, to optimize the converter in terms of different CSF values, the weighting factors can accordingly be distributed differently. However, in this paper the resources are distributed equally to simplify the analysis.

Since the two-phase interleaved boost structure in both topologies is the same in terms of configuration and operation principle, regardless of whether a dc or an ac inductor is used, the CSF analysis will be performed on the circuit configuration from the input V_2 to the output port V_o.

For CSF analysis it is assumed that converter is ideal and lossless, and the inductor and the capacitors are large enough so that all the ripples are negligible. For the dc-inductor based topology, the root mean square (rms) current of the low voltage side switches can be calculated as in (12).

$$I_{rms\_S1,S3} = n \cdot \frac{P_{out}}{V_o} \cdot \sqrt{1-D}; \quad I_{rms\_S2,S4} = n \cdot \frac{P_{out}}{V_o} \cdot \sqrt{D} \tag{12}$$

The voltage stress in the windings is calculated as

$$V_{\max\_avg} = \frac{\int_0^T \left| V_{winding} \right| dt}{T} \tag{13}$$

where $V_{winding}$ represents the voltage across the windings.

Based on the waveforms in Fig. 3 (a), V_{max_avg} for the dc inductor, and the transformer windings are expressed as in (14) and (15).

$$V_{\max\_avg\_Ldc} = 2 \cdot \Phi \cdot \left(nV_2 - V_o \right) + \left(1 - 2\Phi \right) \cdot V_o \tag{14}$$

$$V_{\max\_avg\_Wprim} = 2 \cdot \Phi \cdot V_2; \quad V_{\max\_avg\_W\sec} = 2 \cdot \Phi \cdot n \cdot V_2 \tag{15}$$

Similarly, the rms current and peak voltage values for the input and output capacitors can be also calculated.

For the ac-inductor based topology, the inductor ripple cannot be neglected. To perform a fair comparison, the ac inductance value is taken as the maximum value that fulfills the condition $\Phi < \min [D, (1-D)]$ for the maximum output voltage and output power. The rms current of the ac inductance and the primary switches is calculated as in (16)-(17).

$$I_{Lac,rms} = I_{Lac_{pk}} \sqrt{\frac{2}{3}\left(\Phi + \beta \right)} \tag{16}$$

$$I_{rms\_S1,S2,S3,S4} = I_{Lac_{pk}} \sqrt{\frac{1}{3}\left(\Phi + \beta \right)} \tag{17}$$

where the inductance peak value as well as the phase-shift and the discharge parameter are defined as in (18)-(20).

$$I_{Lac_{pk}} = \frac{-nV_2 + V_o}{L_{ac}} \cdot \Phi T \tag{18}$$

$$\Phi = \frac{V_o}{\sqrt{2}} \sqrt{\frac{-k}{nV_2\left(V_o - nV_2 \right)}} \tag{19}$$

$$\beta = \frac{nV_2 - V_o}{V_o} \cdot \Phi \tag{20}$$

The voltage stress in the inductor and transformer windings, as well as the capacitors rms current and peak voltages are calculated in the same way as in the dc-inductor counterpart.

Figure 4 presents the SCSF, WCSF and CCSF for the dc-inductor based and ac-inductor based, respectively, for an output power varying from P_{out} = 100 W to P_{out} =1 kW and an output voltage range from V_o = 300 V to V_o = 380 V @ V_2 = 100 V, D = 0.5 and n = 4.

From the CSF analysis of Fig. 4 it can observed a large difference between the dc and ac-inductor based topologies. The CSF in the dc-inductor based topology present small variations over the whole range of output voltage and output power, while in the ac-inductor the worst condition occurs at the lower output voltage. In the ac-inductor based topology, the inductance value is adjusted for maximum output voltage and output power; therefore, as the output voltage decreases, the required phase shift value decreases and the inductance peak current increases, resulting in high rms currents, which gives the worst CSF case scenario. In the dc-inductor based topology, for a certain output voltage the values are independent of the operating power.

Figure 5 shows a comparison of the SCSF, WCSF and CCSF of the dc and ac-inductor based topologies as a function of the output power for a fixed output voltage of V_o = 380 V. As previously discussed, the major difference between CSF analysis of the two studied topologies is that in the dc-inductor based converter, for a certain output voltage, the CSF values remain constant with respect to the output power; however in the ac-inductor based converter varies as a function of the processed power. This is due to the fact that the output voltage is kept fixed and, therefore, in the dc-inductor based converter the phase shift value is constant (in ideal conditions where the leakage inductance is neglected). However, the phase shift value in the ac-inductor based converter is load dependent; in this case the inductance is designed for the maximum output power, which degrades the CSF at low output power.

The dc-inductor based topology presents lower SCSF and CCSF over the entire operating range even due to the large rms currents in the ac-inductor based topology for the same output power. However, the ac-inductor based converter shows lower WCSF at low power operation due to lower voltage stress on its windings compared to the dc-inductor based converter. At maximum output power, the dc-inductor based topology presents lower total CSF than the ac-inductor based converter.

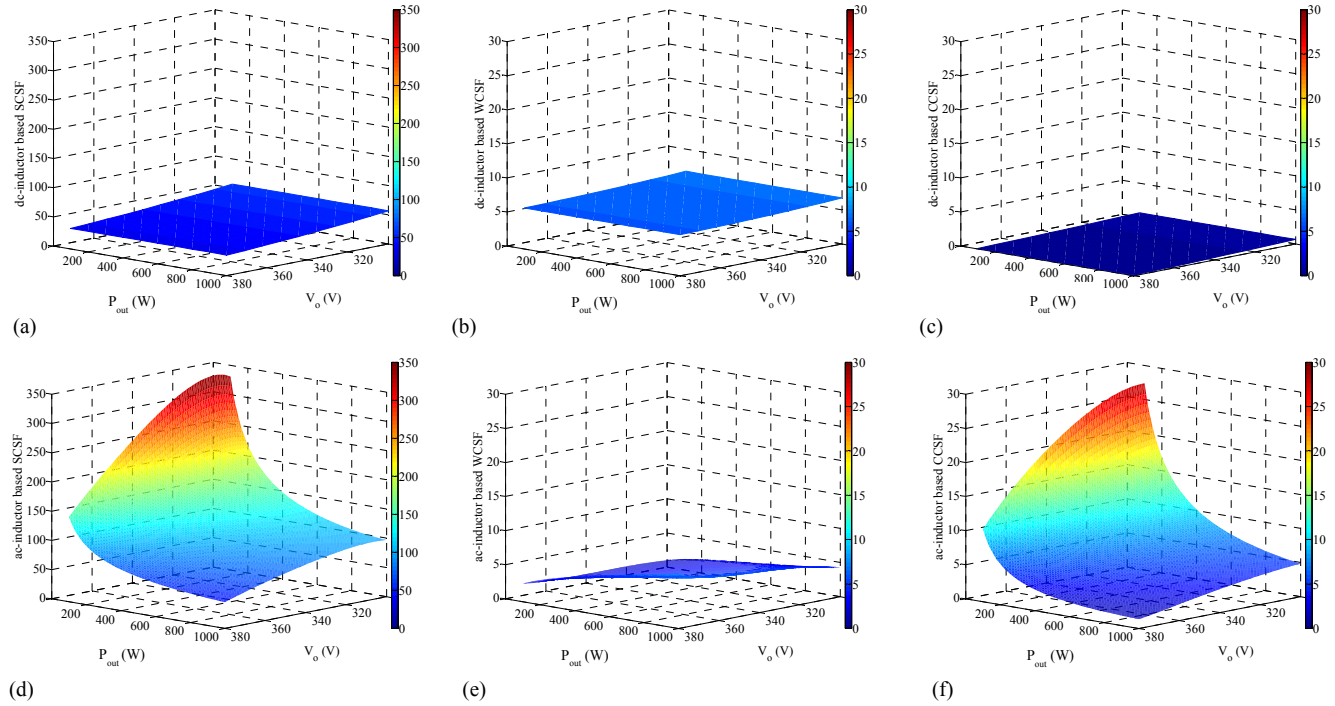

Fig. 4. Component stress factor of dc-inductor based converter: (a) SCSF, (b) WCSF and (c) CCSF and ac-inductor based converter (d) SCSF, (e) WCSF and (f) CCSF as a function of the output power P_{out} and output voltage V_o.

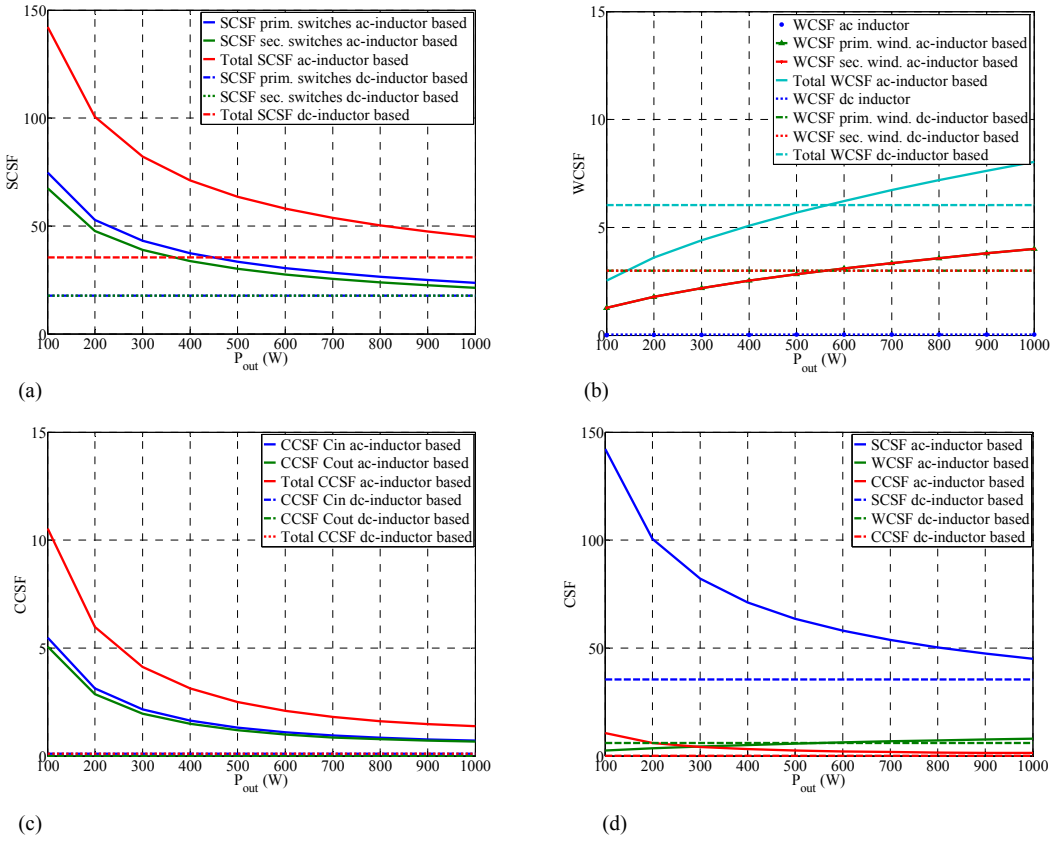

Fig. 5. Comparison of CSFs of dc and ac-inductor based topologies: (a) SCSF, (b) WCSF, (c) CCSF and (d) Total CSF for different P_{out} @ V_o = 380 V.

IV. SOFT-SWITCHING PERFORMANCES

The zero-voltage switching (ZVS) operation for the low-voltage side switches can be deduced on the precondition that the body diode of the MOSFET conducts before it is triggered.

For the dc-inductor based topology, ZVS operation is similar to the conventional PSFB converter. The addition of the two input inductor currents from the two-phase interleaved boost structure complicates the ZVS operation. However, the conclusion for the PSFB converter still holds, i.e. ZVS is load dependent and the ZVS range can be extended by an additional leakage inductance, which, on the other hand, will cause severe voltage overshoot and oscillation across the diodes located on the secondary side. Assuming L_1=L_2=L and L_{dc} is large enough, all the MOSFET can have the ZVS condition once (21) is satisfied.

$$\begin{cases} P_1 > 2V_2 \cdot \left(-n \cdot \dfrac{P_{out}}{V_o} - \dfrac{V_1(1-D)T}{2L} + \dfrac{V_2}{L_{lk}} \cdot t_d \right) \\ P_1 < 2V_2 \cdot \left(n \cdot \dfrac{P_{out}}{V_o} + \dfrac{V_1(1-D)T}{2L} - \dfrac{V_2}{L_{lk}} \cdot t_d \right) \end{cases} \tag{21}$$

where t_d and P_{out} represent the deadtime between high-side and low-side switches and the output power, respectively.

Even though the switch output capacitance is not considered in (21), as explained in [12], the larger the output capacitance, the longer the critical dead time leading to a reduced ZVS range.

For the ac-inductor topology, as discussed in [16], taking into account the amount of stored energy in the MOSFETs' output capacitance (C_{oss}), all MOSFETs can obtain ZVS operation, if (22) is satisfied; in other words, during the deadtime there is significant energy stored in the ac inductor to charge/discharge the output capacitance of the MOSFETs triggered off.

$$\begin{cases} I_{L1,\min} = \dfrac{P_1}{2V_1} - \dfrac{V_1(1-D)T}{2L} < 0 \\ \left| I_{L1,\min} \right| > \sqrt{\dfrac{(2 \cdot C_{oss}) \cdot V_2^2}{L_{ac}}} \end{cases} \tag{22}$$

The ZVS range is reduced when the allowed current ripple is small. However, the high-side switches S_1 and S_3 can inherently achieve ZVS independent of the converter operating conditions. When $I_{L1,\min} > 0$, S_2 in the leading leg loses ZVS, but S_4 in the lagging leg can have ZVS if the constraints in (23) are satisfied.

$$\frac{V_o - nV_2}{L_{ac}} \Phi T - \frac{P_1}{2V_1} + \frac{V_1(1-D)T}{2L} > \sqrt{\frac{(2 \cdot C_{oss}) \cdot V_2^2}{L_{ac}}} \tag{23}$$

Based on the analysis above, accordingly, the ZVS performance of the two topologies can be compared under the same operating conditions, as an example depicted in Fig. 9, where V_1 = 50 V, V_2 = 100 V, V_o = 380 V, L_1 = L_2 = 150 μH, t_d = 50 ns and C_{oss} = 490 pF.

The diodes on the high voltage side can achieve zero-current switching (ZCS) in either dc or ac inductor based topologies. However, in the dc-based, as FBPS, when the current in the diodes decrease to zero, they become reverse-biased and thereby start to block voltage $n \cdot V_2$; however, the resonant circuit formed by the leakage inductance and the diode output capacitance begins to ring, which leads to a considerably high peak voltage in excess of $n \cdot V_2$ over the diodes. Therefore, voltage snubbers are necessarily added to protect the diodes from over-voltage breakdown. On the other hand, for the ac-inductor based, the diodes are fully clamped by the output capacitor, so that no voltage spikes exist, thus extra snubbers are not required.

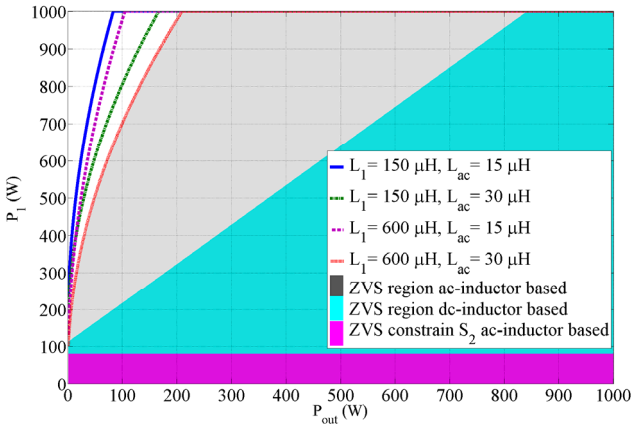

Fig. 9. Comparison of the ZVS ranges.

V. EXPERIMENTAL RESULTS

The ac-inductor based topology is constructed with a fast prototyping technique. The specifications and the components used in the prototype are given in Table I. A digital signal processor (DSP) is employed to generate the PWM gate driving signals as well as to implement closed-loop control algorithms.

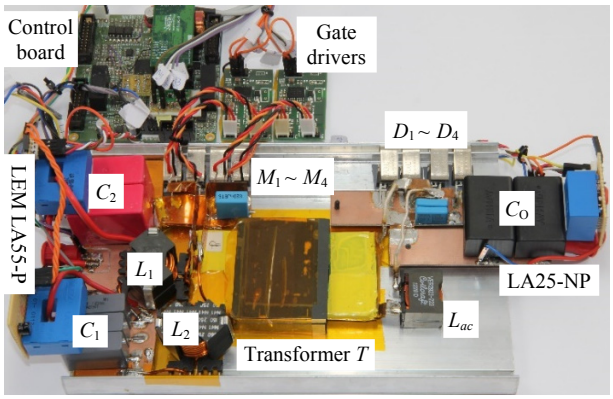

Fig. 10. Propotype of the ac-inductor based DI converter.

TABLE I. SPECIFICATIONS AND COMPONENTS

Input voltage	V_1 = 25 ~ 60 V V_{2_max} = 120 V
Output voltage	V_o = 350 ~ 380 V
Maximum output power	P_{out_max} = 1000 W
Switching frequency	60 kHz
Transformer	4:16, ELP64/10/50, N87
ac inductor	28 μH, VER2923-223
Inductor L_1 and L_2	155 μH, gapped RM12, N41
Semiconductor devices	IRFB4115, HFA08TB60

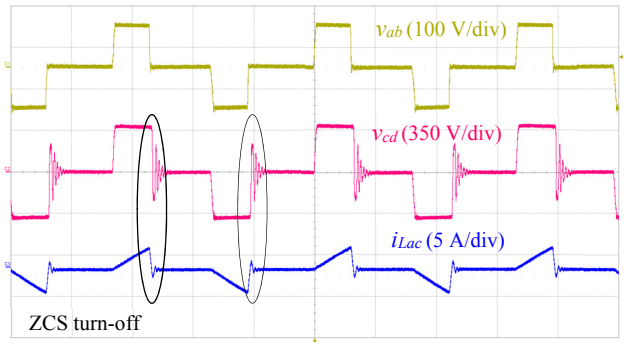

Fig. 11. Experimental results of the high frequency ac voltages v_{ab}, v_{cd} and inductor current i_{Lac} operating in dual input mode at V_1 = 50 V, V_2 = 100 V, V_o = 370 V and P_{out} = 200 W. Time scale: 5 µs/div.

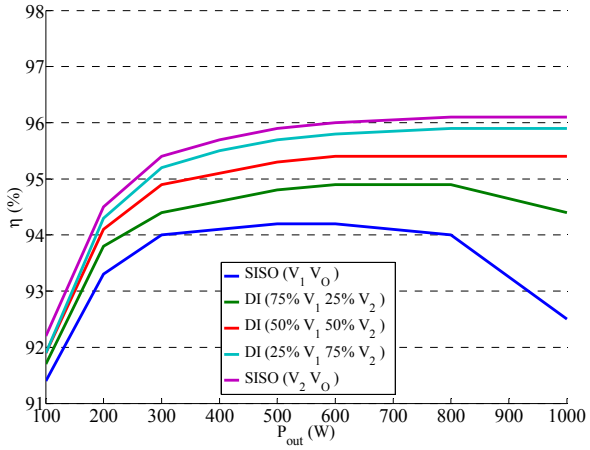

Fig. 12. Measured efficiency of the ac-inductor based dual input converter.

Typical experimental waveforms are measured and shown in Fig. 11, which can match with Fig. 3 (b) well, and therefore verifies the theoretical analysis.

The measured efficiency of the converter operating in dual-input mode (DI) and single-input single-output modes (SISO), for various power sharing between input ports V_1 and V_2, is plotted in Fig. 12, at V_1 = 50, V_2 = 100 V, and V_o = 370 V. A peak efficiency of 97.5% is achieved. More detailed analysis about the experimental test on the ac-inductor based converter have been reported in [16].

VI. Conclusion

In this paper, the dc-inductor and ac-inductor based DI or TPC, are compared in terms of component stress and soft-switching performance. It can be seen that, due to the large output inductor, dc-inductor based topology has lower rms current than its ac-inductor based counterpart. However, the ac-inductor based switching performance is better than the dc-inductor based due to larger ZVS range and lower voltage stress over the output rectifier. In fact, both dc and ac inductor based topologies are the very promising candidates for renewable energy applications. Furthermore, the dc-inductor based topology is favorable for high power application with a low output voltage below 100 V; whereas the ac-inductor based converter would be a better choice for applications requiring a high switching frequency as well as a high output voltage above 400 V, for instance, a compact grid-connected power conversion system.

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