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Graphene antidot lattice transport measurements

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Abstract: We investigate graphene that has been patterned with a short nanomesh – a small number of rows of antidots perpendicular to the current flow. Theoretical reports have suggested that a short antidot lattice in graphene can generate an energy gap with a relatively small reduction of the transmission compared to what is typically associated with nanoribbon and nanomesh devices. Exfoliated graphene flakes were electrically contacted allowing for four-terminal electrical measurements. Antidot lattices were then defined using 100 keV electron beam lithography. Electrical measurements showed that a few rows (1 or 5) had comparable mobilities (>100 cm^2/Vs), while a large number of rows, around 40, led to a strong reduction of apparent carrier mobility (<5 cm^2/Vs). The carrier mobility was measured as a function of temperature, with the low-temperature behaviour being well described by variable range hopping. This work produced the highest pattern density (30 nm hole diameter and neckwidth) reported for graphene using electron beam lithography.

Keywords: Graphene, Antidot Lattice, Nanomesh, Electron Beam Lithography, Variable Range Hoping, Nanopatterning

Biographical notes: David Michael Angus Mackenzie graduated from the University of Canterbury in 2010 with a PhD in physics based on nanoscale cluster devices. He joined the Micro-and-Nanotechnology department at the Technical University of Denmark in 2012 as a postdoctoral researcher where he now works with graphene devices including nanopatterned transistors, nanopatterned gas sensors and large-area graphene devices.

Dr. Alberto Cagliani graduated from the Technical University of Denmark in 2012 with a PhD in nanotechnology based on silicon micromechanical resonator for bio and chemical detection. He stayed with the Micro-and-Nanotechnology department at the Technical University of Denmark as a postdoctoral researcher where he now works with graphene devices including nanopatterned transistors, nanopatterned gas sensors.

Lene Gammelgaard graduated from the Technical University of Denmark in 2013 with a Master's in physics and nanotechnology based on graphene

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Bjarke Jessen graduated from the Technical University of Denmark in 2012 with a Master's in nanotechnology based on graphene devices. He was subsequently hired as a PhD student at the Center for Nanostructured Graphene, also at the Technical University of Denmark, where he now works with graphene and other 2D-material. His current work includes devices of nanopatterned graphene transistors and maintenance of the "Flake Finder", used for automated identification of single-layer 2D materials.

Dirch Hjorth Petersen obtained a Ph.D. degree in applied physics from the Technical University of Denmark in 2010. He is currently a Senior Researcher focus on development of methods for electrical characterization of ultrathin materials.

Peter Bøggild graduated from Copenhagen University in 1998 with a PhD in physics based on low-temperature ballistic transport in 2D electron gases. He moved to DTU Nanotech at the Technical University of Denmark and is now professor, leading a research group which explores graphene and other 2D-materials, devices and applications.

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1   Introduction

Graphene has been predicted to become widely integrated into future electronics, including high-speed transistor-based devices due to the reports of extreme mobilities, and the possibility of very high operating frequencies [1]. While the lack of a transport gap prevents the necessary on/off ratios and drain current saturation [2] for such applications [3], several strategies have proven successful in inducing an energy gap like behaviour, commonly involving nanopatterning of graphene. Nanopatterning invariably introduces additional scattering and subsequent decreases in carrier mobility. Transport gaps in graphene devices have been previously reported [4,5], for nanoribbons and nanomesh structures where in order to achieve the required narrow critical features, samples are often patterned using an etch-mask fabricated from a block co-polymer (BCP) [6,7,8] or by HSQ negative resist [9]. While BCP lithography has poor control over the position and ordering of the nanopatterning, especially when compared to electron-beam lithography (EBL), EBL based on HSQ negative resist has been observed to limit the mobility due to line edge roughness as widths of order tens of nanometers are approached [9]. For HSQ and BCP resist residues remaining after the removal of the etch mask may impede the electrical properties [10].

However, it has been predicted that just a few rows of antidots can lead to a transport gap similar to that of a semi-infinite array, while maintaining acceptable carrier mobility [11]. EBL provides the precision required for highly controlled position and number of rows, while using PMMA as the etch mask, reduces electrical degradation [12]. This study presents gate-controlled transport measurements on such devices.

2   Methods

The fabrication of devices is outlined in Figure 1. Single-layer graphene is produced via the exfoliation method [1] on highly-doped silicon wafers with a 300 nm silicon dioxide (Figure 1(a)). Graphene is identified via optical microscopy and Raman spectroscopy. Electrical contacts were patterned (JEOL JBX-9500 EBL system) and 3 nm Cr/30 nm Au was deposited via electron-beam deposition (Wordentec QCL 800) (Figure 1(b)). The wafer was then spin-coated with 40 nm of PMMA (with a molecular weight of 995k in solution of 2% in anisole) and a 17 nm of aluminum was used as a charge-dissipation layer. EBL was again performed to define an etch mask for the antidot lattice as well as the overall Hall bar geometry. After removal of the aluminum, patterns were developed in IPA:water 7:3 for 30 seconds. The pattern was then transferred to the underlying graphene using a SPTS RIE system (10W, oxygen/argon 40 sccm/5 sccm, 12 seconds) (Figure 1 (d+e)). PMMA was then removed in warm acetone and devices were ready for electrical characterization.

Figure 1   Process flow and schematic of devices. A: Graphene is exfoliated onto a silicon substrate with upper layer of 300 nm of silicon dioxide. B: Electrodes of Cr/Au are fabricated via standard electron-beam lithography. C: An etch mask is created in PMMA using electron-beam lithography and etching in an oxygen plasma. D/E: Device showing individual sections of antidots: 1 row, 5 rows and a large mesh (42 rows).
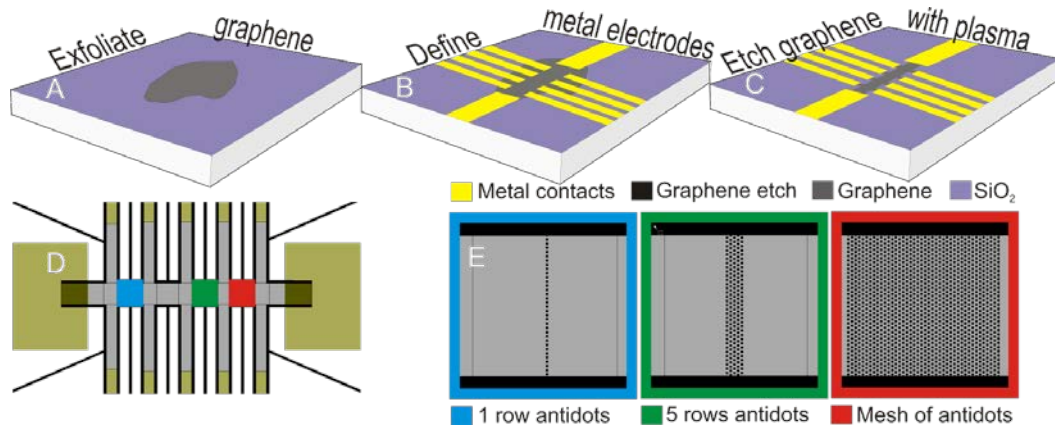
Devices were electrically characterized in a Linkam LTS600P probe station with possibility of a temperature and gas controlled environment, with LabView controlled Keithley 2400 Source Meter SMUs and Keithley 2000 Digital Multimeters. Tylan flow controllers enabled a 100 sccm flow of nitrogen into the chamber at all times. Before measuring, devices were annealed at 225°C for 30 minutes in a nitrogen atmosphere in order to remove surface water and other surface contaminants. Thanks to the device design, all devices sections were measured simultaneously (Figure 2).

Figure 2   Circuit diagram with simultaneous four-point measurements of each antidot section.

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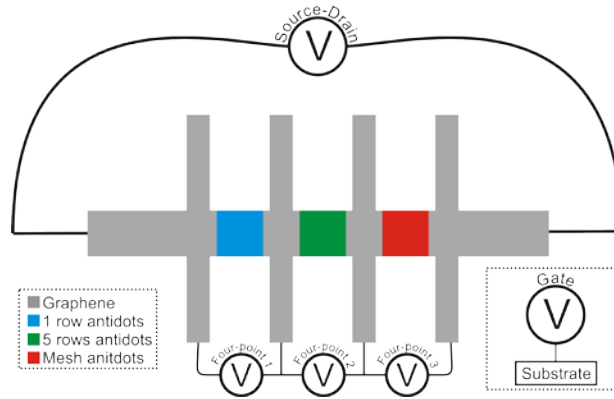
3 Results and Discussion

A completed device is shown in Figure 3. The scanning-electron microscope image shows that the antidots were successfully manufactured, with hole diameters of 30 nm and neckwidths of 30 nm. This is to our knowledge the smallest features of any antidot lattice written in graphene via EBL. Although the mesh section is visibly damaged in Figure 3, the measurements on this structure were consistent with the other sections, suggesting that the current could flow normally in the healthy region. In the following we include these data.

Figure 3 Top: Scanning-electron-micrograph of fabricated devices after measurements including close-up of (blue) 1 row antidots, (green) 5 rows antidots and (red) mesh antidots. Bottom: Temperature-dependent gate characteristics (V_{SD} = 10 mV) in the range of -195°C to 105°C, for (blue) 1 row antidots, (green) 5 rows antidots and (red) mesh antidots. Shown are raw data of five sweeps of the gate voltage.
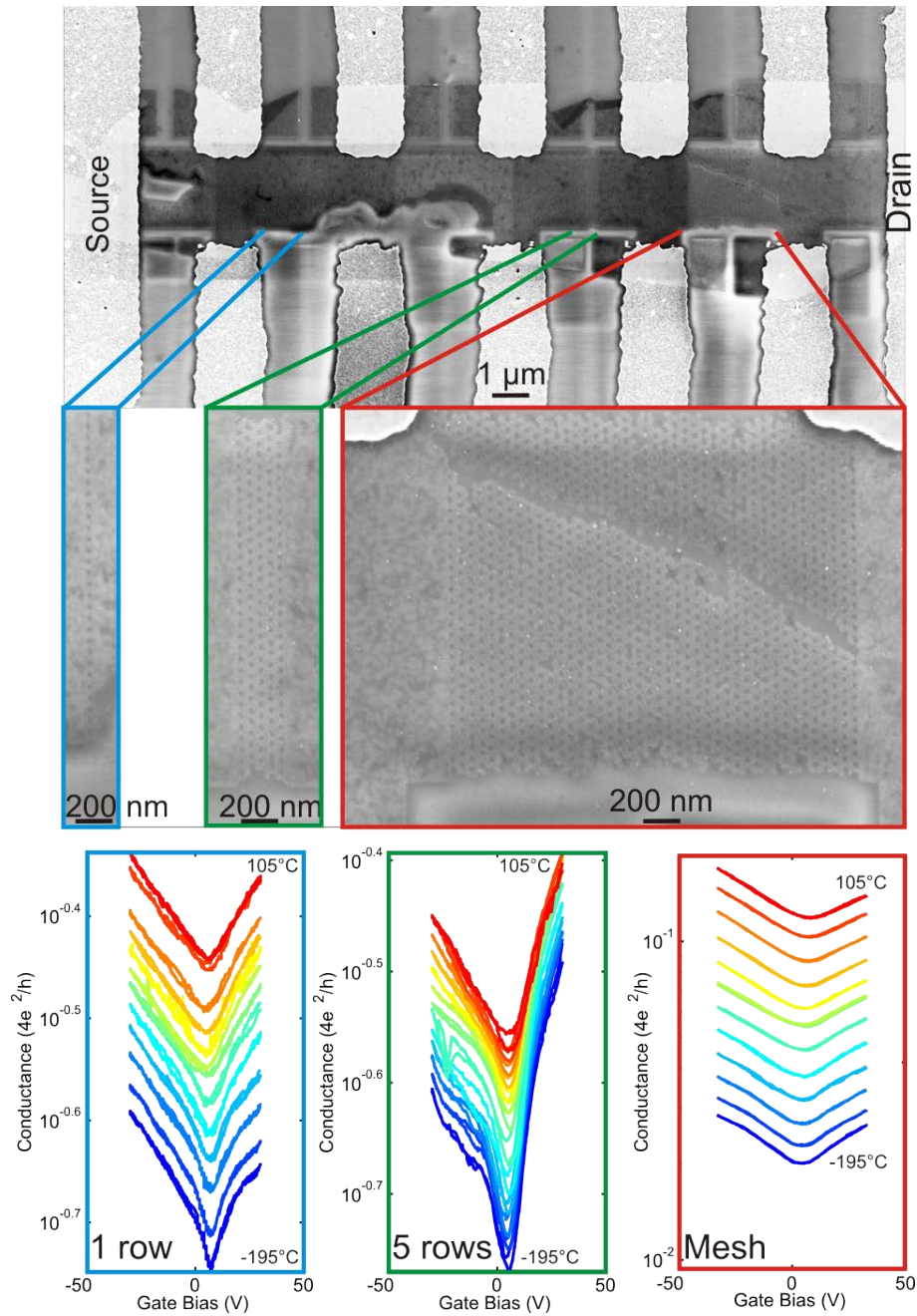
The devices were fabricated on highly-doped silicon wafers with a 300 nm silicon dioxide layer, which allowed field-effect measurements to be carried out. The electron and hole field-effect carrier mobilities as well as the gate bias required to observe a charge-neutrality point (CNP) were determined as a function of temperature (-195°C to 150°C in steps of 25°C); this data is shown in Figure 3 (bottom). The data for each

temperature was fitted using a least-squared method [10] to determine the position of the charge-neutrality point and to extract the mobility. All sections of the devices show a low level of doping with all CNPs at a gate-bias of <10 V. The sections with 1 and 5 rows show conductance levels of the same order. Curiously, the nanomesh does not exhibit any significant increase of the on-off ratio as the temperature is reduced, while the single- and few row mesh structures both show such a tendency, with the on-off ratio increasing from 1:1.25 to 1:1.4, and 1:1.5 to 1:1.9, respectively.

The carrier mobility discussed in the following is the *apparent carrier mobility*, extracted like in Ref [3], but as if the graphene was not patterned and with the intended Hall bar geometry. It should be remarked, however, that even in the extreme case that the holes do not lead to an increased scattering rate, they will certainly leave less graphene available for transport, and effectively correspond to a narrower channel. A narrower channel will have a smaller conductance, and thus appear to have smaller carrier mobility.

When the electron and hole mobilities of the 1 and 5 row sections are compared (Figure 4(left) and 4(right)) the hole mobilites are comparable. Surprisingly, despite a greater amount of nanopatterning, the 5 rows section has larger electron mobility. However, compared to the 1 and 5 row sections, the mesh section shows large reduction in conduction and mobility of more than an order of magnitude.

The temperature dependent conduction for 1 row, 5 rows and mesh structures shown in Figure 3 (bottom) suggests that all sections have a thermally activated component to their conduction mechanism. The temperature-dependent conduction does not correspond to an Arrhenius relationship, and in addition, any significant increase in on-off ratio is not observed, which in combination suggests that the nanopatterning has not opened a gap. However, as shown in Figure 4(right), the temperature-dependent behavior does show $T^{1/3}$ behavior, which is associated with two-dimensional variable range hopping (VRH) [13]. A linear fit is applied to the data analysis from Figure 4(right) and the R^2 values for each device section are show in Table 1. For VRH, the data fits convincingly for the mesh, with a reasonable fit also obtained for the 5-row sections. In comparison, the 1-row section, as well as the Arrhenius data is not linear and hence it is likely that the behavior of these devices is dominated by VRH.

Table 1 R^2 values from linear fits of temperature dependent behaviour for variable-range hoping and Arrhenius-style (transport gap).

	Variable Range Hopping	*Arrhenius*
1 row	0.83	0.74
5 rows	0.92	0.78
Mesh	0.98	0.82

The nanopatterning in our graphene devices has produced a neckwidth of 30 nm, and based on previous reports [1,3] a transport gap of 10-30 meV would be expected. It is proposed that VRH dominates for this neckwidth size and is due to the disorder as a result of our etching process as similar devices with large disorder have previously shown no transport gap [14,15]. As suggested in literature [16], a transport gap is likely to become dominant for smaller antidot lattice feature sizes.

Figure 4 Analysis of temperature-dependent gate data from Figure 3. Left: Hole mobility as a function of temperature. Middle: Electron mobility as a function of temperature. Right: Variable-range hopping analysis of the conductance minimum including linear fit R^2 values.
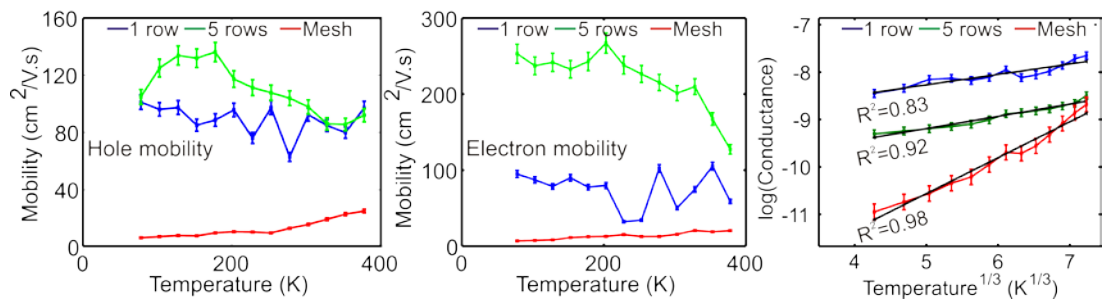
4 Conclusion

Exfoliated graphene was nanopatterned with the smallest-feature antidot lattice or nanoribbon array in graphene via EBL reported. The electron and hole field-effect carrier mobilities determined as a function of temperature are consistent with the prediction that a few rows of antidots leads to a minimal reduction of carrier mobility. The temperature dependence of the antidots sections seems to be well described by variable range hoping for the case of 5 rows of antidots and above. This suggests that future work could investigate a higher variation in the number of rows to investigate the onset of VRH and to discover if further constriction of the anti-dot lattice neckwidth induces a transport gap. It also clearly underlines the necessity to develop more gentle and protective approaches if the high convenience in terms of EBL's patterning flexibility and cleanroom process compatibility is ever to be exploited for high performance graphene devices.

Acknowledgements

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