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Efficiency of Switch-Mode Power Audio Amplifiers - Test Signals and Measurement Techniques

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ABSTRACT

Switch-mode technology is greatly used for audio amplification. This is mainly due to the great efficiency this technology offers. Normally the efficiency of a switch-mode audio amplifier is measured using a sine wave input. However this paper shows that sine waves represent real audio very poorly. An alternative signal is proposed for test purposes. The efficiency of a switch-mode power audio amplifier is modelled and measured with both sine wave and the proposed test signal as inputs. The results show that the choice of switching devices with low on resistances are unfairly favoured when measuring the efficiency with sine waves. A 10% efficiency improvement was found for low power outputs. It is therefore of great importance to use proper test signals when measuring the efficiency.

1 Introduction

Switch-mode technology has during the last decade become the conventional choice in audio where they are known as Class-D amplifiers. This is due to the superior efficiency this technology offers, which theoretically can reach 100%, and the good performance with very low distortion as shown in [1] and [2]. The theoretcally 100% efficiency is not possible but efficiencies ranging well above 90% have been presented in previous work for a wide range of applications, for example in renewable energy systems [3]. Also in audio applications efficiencies in the vicinity of 90% have been achieved [4], [5]. High efficiency is crucial for especially battery driven sound systems. When specifying the performance of the amplifier the complexity of the audio system is often simplified for test purposes. For example the loudspeaker impedance is often simplified as a pure ohmic resistance as discussed in [6]. Also for amplifier efficiency specification conventional measurement techniques involves driving the amplifier with a sine signal. However sine waves are not a good representation of real music signals. Real music signals has great dynamics as described in [7], [8] and [9]. This has the consequence that the effective RMS output power of the amplifier is much lower when playing real music signals compared when playing sine waves as discussed in [10] and [11]. For this reason the amplifier efficiency obtained in previous work, [4], [5], is not representative for the intended amplifier operation, i.e. when it is playing real music signals. In addition to this the choice of the switching devices, e.g. MOSFETs, could easily be mismatched to favour sine wave efficiency instead of real audio efficiency.

This paper describes the fundamental operation of switch-mode power audio amplifiers and examine the losses generated in the power stage and output filter of the amplifier. Moreover this paper investigates the dynamics of audio signals and use this information to make a more representative test signal than sine waves. Finally experimental examples illustrates how the choice of the switching devices is dependent on the used test signal.

2 Switch-mode power audio amplifiers

Switch-mode power technology is well describe in literature [12]. However this section will present the basic operation principles. Moreover an elaborated description of the power stage will be presented. This includes an analysis of the switching voltages and currents in the power stage and the inherent loss mechanisms of the power stage.

2.1 Basic operation

A switch-mode power audio amplifier can be split into three essential blocks. They are:

- Modulator
- Power stage
- Output filter

Figure 1 shows a simplified block diagram. Conventional modulators uses Pulse Width Modulation

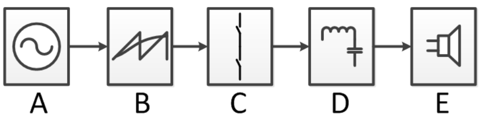


Fig. 1: Block diagram of switch-mode power audio amplifier. A) is audio input, B) is modulator, C) is power stage, D) is output filter and E) is loudspeaker.

(PWM) where the audio signal is modulated with a high frequency carrier waveform. Typically this waveform will have a triangle or sawtooth shape. Normally the modulation is performed by comparing the audio input with the carrier which generates a pulse train at a given frequency, the switching frequency f_{sw}, with varying pulse lengths as shown in figure 2. The length or on-time of the pulses are also known as the duty cycle, D, of the PWM signal. The power stage is where the amplification takes place and it consists of

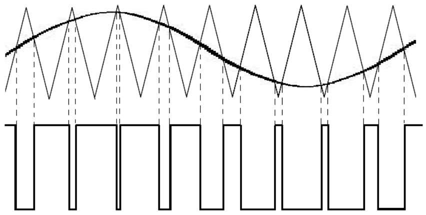


Fig. 2: Modulation of audio signal using triangular carrier resulting in a Pulse Width Modulated (PWM) representation of the audio signal.

switching devices which are switched on and off using the PWM signal. This means that the power stage actually amplifies the PWM signal. The most common switching device for switch-mode power applications is the Metal Oxide Field Effect Transistor (MOSFET). The power stage are typically using a buck topology described in [12]. This topology can be realized either in a half- or full-bridge configuration. The half bridge requires a dual voltage supply while the full bridge only requires a single supply. The component count in the full bridge is twice the component count in the half bridge. This topology is very attractive for audio applications due to an ideally linear transfer function which minimizes the distortion:

$$V_{out} = (2D-1)\,V_{DD} \tag{1}$$

Where V_{out} is the output voltage, D is the duty cycle and V_{DD} is the rail to rail voltage, i.e. V_+ to V_- in half bridge configuration and V_+ to ground in full bridge configurations. In battery driven systems the full bridge configuration is the conventional choice. Figure 3 shows the half bridge buck which includes the output filter formed by the inductor, L_f, and the capacitor, C_f. The switching devices are driven by the PWM signals, V_{gs1} and V_{gs2}, which are 180° out of phase. The output filter is a low pass filter which removes the high frequency PWM representation and restores the audio audio signal which is fed to the load, i.e. the loudspeaker.

2.2 Power stage waveforms

In this section the switching voltages and currents in the half bridge buck power stage will be examined under different switching conditions. In order to do that a more detailed representation of the switching device is necessary. Figure 4 shows the switching device, e.g.

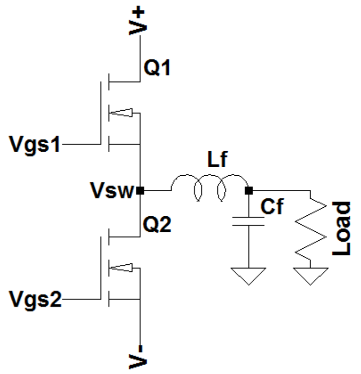


Fig. 3: Half bridge buck topology.

a MOSFET, including its' parasitic components. That is the parasitic capacitances, C_{oss}, C_{gs} and C_{gd}, the on resistance $R_{ds(ON)}$ and the drain to source body diode which will have a given forward voltage drop. As men-

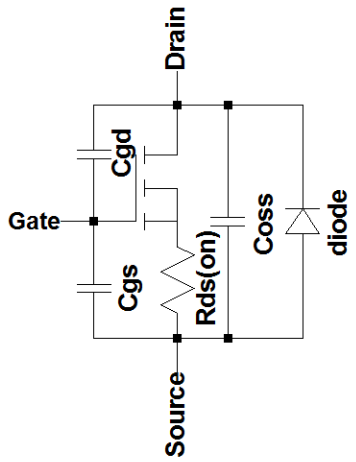


Fig. 4: Switching device, e.g. MOSFET, including the parasitic on resistance, $R_{ds(ON)}$, the drain source capacitance, C_{oss}, the gate capacitances, C_{gs} and C_{gd} and the drain to source body diode.

tioned the gates of the switching devices will be driven 180° out of phase with the PWM signal. To prevent an undesired short circuit through the half bridge some dead time, t_{dt}, between the gate signals should be implemented. Too much dead time can however generate distortion as shown in [13]. This should be taken into account when investigating the switching voltages and currents of the power stage. There exists four different switching conditions which are relevant in order to estimate the losses in the power stage.

1. Hard switching occurs when the parasitic drain source capacitance, C_{oss}, of the switching device can not be charged or discharged by the inductor current, I_L, during the dead time period. This can either be due to a very small dead time period, a large parasitic capacitance or an insufficient inductor current. The switching node voltage, V_{sw}, will ramp up and down together with the drain current, I_D, in the switching device, causing some switching losses. Moreover the parasitic capacitances will be charged or discharged very fast during turn on/off and this energy is dissipated as an additional loss.

2. Soft switching, or Zero Voltage Switching (ZVS), on the other hand occurs when the parasitic drain source capacitance of the switching device can be completely charged or discharged by the inductor current during the dead time period. This eliminates the switching losses in theory.

3. When the ripple in the inductor current is larger than the output current, $\Delta i_L > |I_{out}|$, a situation can occur where the parasitic drain source capacitance is charged or discharged beyond the rail to rail voltage, V_{DD}. In this situation the body diode of the switching device start conducting which causes some losses in the switching device due to the forward voltage drop of the body diode.

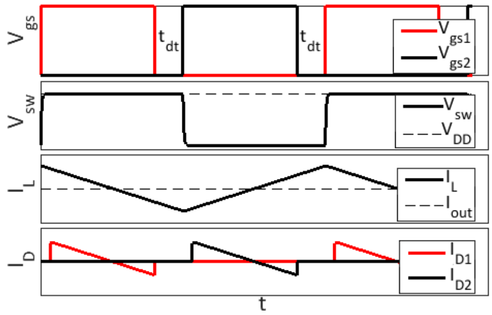
4. Finally when the output current is larger than the ripple in the current, $|I_{out}| > \Delta i_L$, the body diode of the switching device will continue conducting after turn off causing additional losses.

Figure 5 a) to d) shows the waveforms for the four described switching condition.

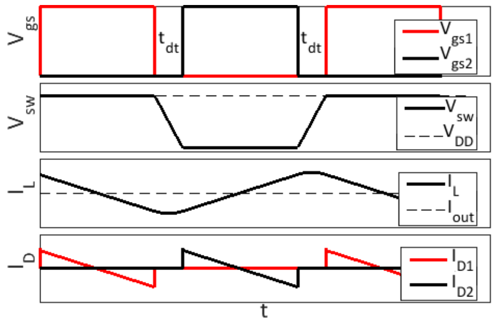
Since the power stage is intended for audio use the duty cycle of the PWM signal driving the switching devices will vary according to the audio input. This means that power stage most likely will undergo all four switching conditions.

2.3 Loss mechanisms

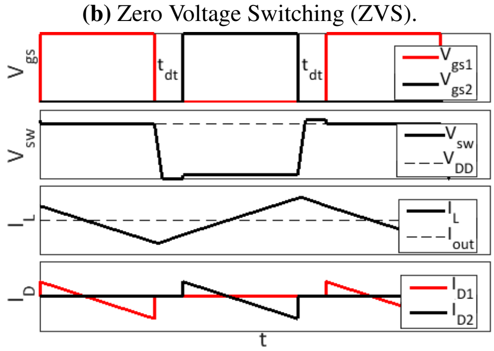
This section will focus on the losses in the power stage and the output filter. The main loss mechanisms will



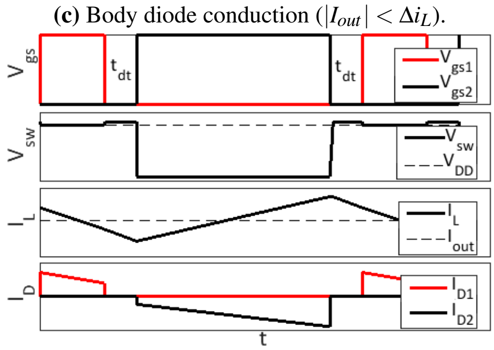
(a) Hard switching



(b) Zero Voltage Switching (ZVS).



(c) Body diode conduction ($|I_{out}| < \Delta i_L$).



(d) Body diode conduction ($|I_{out}| > \Delta i_L$).

Fig. 5: Waveforms in the Buck power stage for different switching conditions

be described and equations for estimating the losses presented. The equations listed throughout this section is for the half bridge buck shown in figure 3.

1. Gate losses are generated by charging and discharging the gate capacitances, C_{gd} and C_{gs}, of the switching device, e.g. transistor. The needed charge is normally specified in transistor data sheet as the total gate charge, Q_g. The gate losses can be determined knowing the gate source voltage of the switching device, V_{gs}, and the switching frequency.

$$P_{gate} = 2 \cdot Q_g \cdot V_{gs} \cdot f_{sw} \tag{2}$$

2. Conduction losses are generated when the switching transistor is in its' on state. During its' on state a current, I_D, is running causing some power to be dissipated in the on resistance of the transitor.

$$P_{cond} = I_D^2 \cdot R_{ds(ON)} \tag{3}$$

3. Switching losses occur during the switching events between the transistors on and off states. As mentioned a current is running in its' on state while no current runs in the off state. This current will ramp up and down together with the fast voltage transients from rail to rail, causing some power to be dissipated. Moreover the parasitic capacitance, C_{oss}, will be charged and discharged by these transients causing additional losses. However these losses can be minimized if the parasitic capacitances of the transistor is charged/discharged by the inductor current, I_L, in the dead time period.

$$P_{sw} = I_D \cdot \left(V_{DD} - \frac{t_{dt} \cdot I_L}{2C_{oss}}\right) \cdot \frac{t_{rise} + t_{fall}}{2} \cdot f_{sw} \tag{4}$$

$$P_{oss} = C_{oss} \cdot f_{sw} \cdot \left(V_{DD} - \frac{t_{dt} \cdot I_L}{2C_{oss}}\right) \tag{5}$$

where t_{rise} and t_{fall} are the transistor rise- and fall-time, typically available from data sheets.

4. Reverse conduction losses occur in the situation where the body diode in the transistor starts or continue conducting the current, I_D. Due to a small forward voltage drop in the diode some power will be dissipated.

$$P_{reverse} = t_{cond} \cdot f_{sw} \cdot I_D \cdot V_f \tag{6}$$

5. The loss in the output filter are related to the inductor current, I_L, and the resistance of the inductor wire. For low frequency signals, e.g. 0 to 20 kHz, the resistance can be assumed to be negligible. However at higher frequencies, around the switching frequency, losses are expected due to the fact that the resistance increases with the frequency in the inductor. The AC resistance is often denoted the Equivalent Series Resistance (ESR) and can typically be found in data sheet for the inductor or measured with an impedance analyser. The losses can be estimated to be:

$$P_f = I_L^2 \cdot \text{ESR} \quad (7)$$

Finally the total losses can be expressed as the sum of the different loss components:

$$P_{tot} = P_{gate} + P_{cond} + P_{sw} + P_{oss} + P_{reverse} + P_f \quad (8)$$

Normally the conduction losses, P_{cond}, the switching losses, P_{sw}, and the filter losses, P_f, will be the dominant losses. However in idle operation, or close to idle operation, where the output power is small, the losses related to the parasitic capacitances becomes significant, i.e. P_{gate} and P_{oss}. The reverse conduction losses are normally quite small, due to the fact that the forward voltage drop of the body diode in many cases is rather small.

2.4 Efficiency

The efficiency is simply the ratio between the output- and input-power.

$$\eta = \frac{P_{out}}{P_{in}} \quad (9)$$

In order to secure good efficiency one must choose the switching devices carefully. Looking at the equations for the losses presented above it seems obvious that to ensure good efficiency one should choose switching devices with tiny parasitic capacitances and a small on resistance. However this is not possible due to the fundamentals of transistor design [15]. If a transistor is to be designed with a low on resistance, this would require a highly conductive path between the drain and source terminals of the transistor when in its' on state. A highly conductive path is made by making the conductive channel between the drain and source terminals wider, thus increasing the overall conductive area. An increment of the area will equally increase the parasitic capacitances. Therefore transistors with tiny on resistances would normally have large parasitic capacitances and vice versa. Figure 6 shows the modelled efficiency vs. the output power for a 12 V switch-mode power audio amplifier driven with a sine wave input for two types of transistors with different specifications. The figure shows that a low on resistance makes it possible to achieve an efficiency above 80% for a large range of output powers, reaching the vicinity of 90% just before clipping, while low parasitic capacitances improves the idle losses on the cost of a poor peak efficiency.

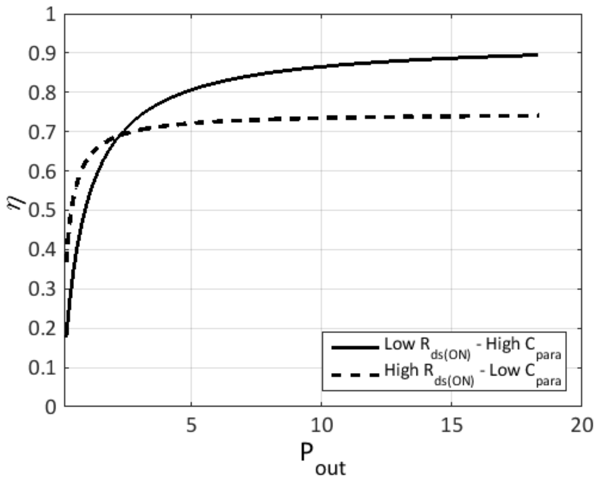


Fig. 6: Modelled efficiency of 12 V switch-mode power audio amplifier driven with a sine wave input for two types of transistors.

3 Audio Dynamics

From the loss analysis performed above and efficiency curves showed in figure 6 it seems obvious to choose transistors with low on resistances to ensure good amplifier efficiency. However a consumer will rarely listen to sine waves and therefore it is relevant to investigate the dynamics of real audio signals.

A music library consisting of 183 audio tracks from a vast selection of genres have been analysed in terms of amplitude distribution and crest factor. The crest factor is the ratio between the peak- and the RMS-value of the signal and is normally given in decibels. Figure 8 a) shows the amplitude distribution of a sine wave and the audio tracks from the music library. The figure shows that there exists a fundamental difference between real audio signals and sine waves. The amplitude distribution of real audio is centred around an amplitude close to zero. For higher amplitudes the distribution decreases. The amplitude distribution for sine waves is almost the opposite of the audio signals with peaks at the maximum amplitudes and a minima around zero. Moreover the crest factor of sine wave is 3 dB where it ranges from approximately 7 to 25 dB for the audio tracks with a mean value of 15 dB. Keeping this in mind it seems futile that sine waves are among the preferred test signals for audio amplifier applications.

The IEC-268 standard [9] presents a test signal which basically is filtered pink noise. Figure 8 b) shows the amplitude distribution including the IEC-268 filtered pink noise and this signal is found to represent the audio tracks much better and has a crest factor of 12 dB. However this signal is not like a sine wave due to the fact that it is a noise signal and thereby does not have a fundamental frequency. Since many test procedures for specifying amplifier performances, such as frequency responses and THD measurements, uses a frequency sweep with constant amplitude, it is relevant to construct an alternative test signal which represent audio tracks but also have a fundamental frequency like sine waves. This is also relevant when measuring efficiency, making it easier to tell when the signal starts to distort just by looking at the waveform with an oscilloscope. An alternative test signal has been constructed by distorting a normal sine wave and it can be expressed mathematically as:

$$f(t) = \left(\frac{0.5+K \cdot sin(\omega t) - (1-(0.5+K \cdot sin(\omega t)))}{(0.5+K \cdot sin(\omega t)) \cdot (1-(0.5+K \cdot sin(\omega t)))} \right)^{\frac{1}{4}} \quad (10)$$

Where $K = 0.49995$ is a constant and $\omega = 2\pi f$. Figure 7 shows the proposed test signal peak normalized to 1, and figure 8 c) shows the amplitude distribution. It is seen that the proposed test signal represents audio signals well. Its' crest factor is approximately 14 dB.

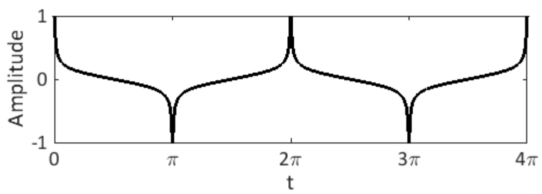
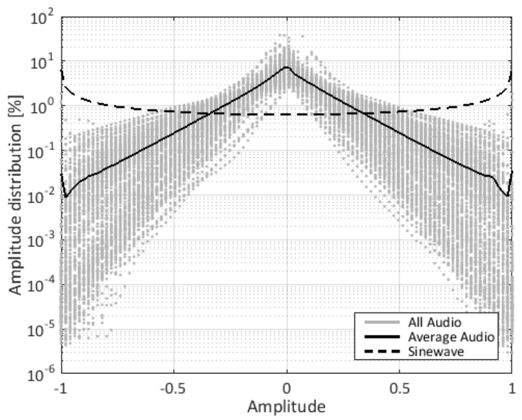
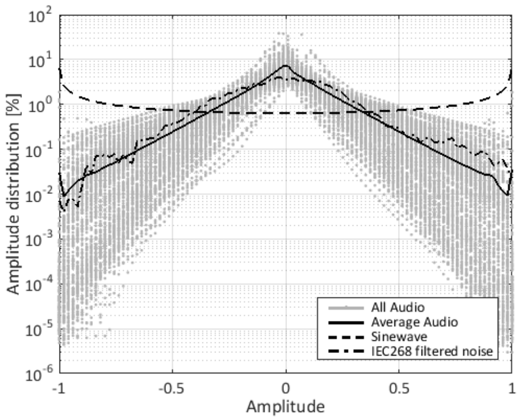


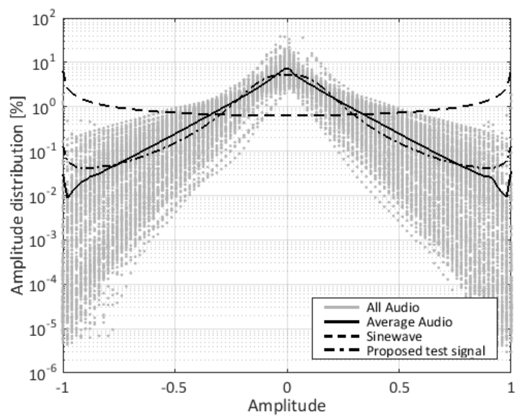
Fig. 7: Proposed test signal peak normalized to 1.



(a) Amplitude distribution of audio and sine.



(b) Amplitude distribution of audio, sine and IEC-268 filtered noise.



(c) Amplitude distribution of audio, sine and proposed test signal.

Fig. 8: Amplitude distribution of signals.

3.1 Revised efficiency

As mentioned above the average crest factor for the audio signals is approximately 15 dB causing the maximum RMS output power of the switch-mode power audio amplifier to be significantly smaller when playing real audio signals instead of sine waves. This actually means that the duty cycle distribution is significantly different when playing audio compared to sine waves. Since the Buck topology has a linear transfer function as shown in eq. 1 the duty cycle distribution will be directly proportional with the amplitude distribution. Figure 9 shows the duty cycle distribution for the audio tracks, the sine wave and the proposed test signal. Knowing the duty cycle distribution of real audio signals enables modelling of the efficiency for the switch-mode power audio amplifier when playing an audio representing signal, e.g. the proposed test signal. As in section 2.4 the efficiency is modelled for a 12 V switch-mode power audio amplifier for the two types of transistors used in the previous examples. Figure 10 shows the results. First of all the figure shows that the maximum RMS output power of the amplifier is significantly lower compared to the sine wave operation from figure 6. Moreover the figure shows that the amplifier efficiency benefits more from low parasitic capacitances than from a small on resistance when using an actual audio representing signal. When looking at figure 6, which shows the efficiency for the sine wave operation, one could easily be led to believe that a low on resistance would be preferable for good amplifier efficiency however this is not the case.

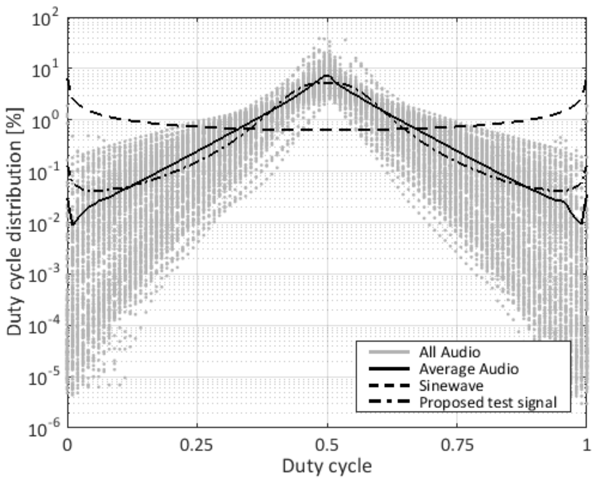


Fig. 9: Duty cycle distribution of audio, sine and proposed test signal.

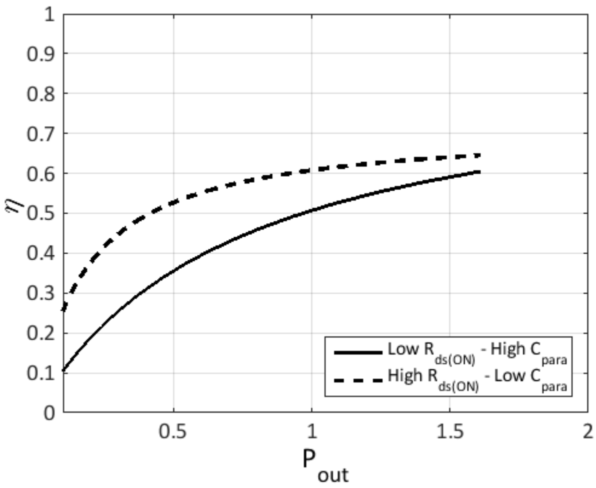


Fig. 10: Modelled efficiency of 12 V switch-mode power audio amplifier driven with an audio representing input signal for two types of transistors.

4 Measurements and results

A series of efficiency measurements have been performed on a 12 V switch-mode power audio amplifier. The implemented test-amplifier uses a full bridge buck topology which enables it to operate from a single voltage supply, e.g. a battery. This also means that it has four switching devices, implemented as MOSFETs in its' power stage. Figure 11 shows the implemented test amplifier. The efficiency has been measured with

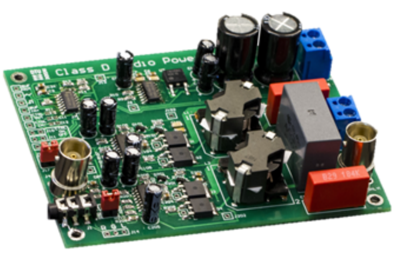


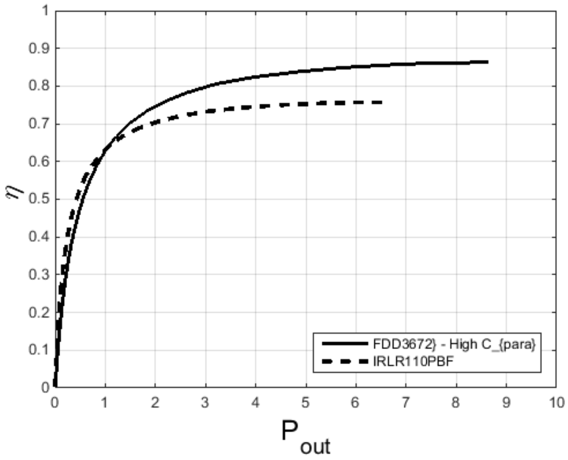
Fig. 11: Implemented 12 V test amplifier.

the amplifier driven by a sine wave and the proposed test signal as input. Moreover the efficiency has been measured for two types of MOSFETs, one with low on resistance and high parasitic capacitances and one with high on resistance and low parasitic capacitances. The used MOSFETs are the FDD3672 from Fairchild Semiconductors and the IRLR110PbF from International Rectifier and their key parameters are listed in table 1. It should be mentioned that both MOSFETs are in the same kind of package (D-PAK). The efficiency was

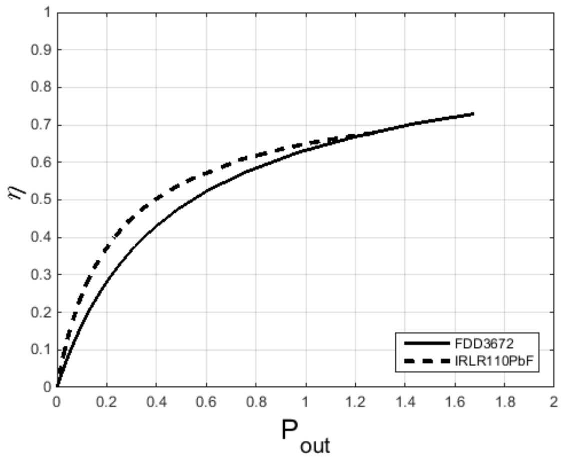
Name	Q_g	$R_{ds(ON)}$	C_{oss}
FDD3672	24 nC	24 mΩ	247 pF
IRLR110PbF	6.1 nC	540 mΩ	80 pF

Table 1: Key parameters for MOSFETs used in power stage

measured by measuring the input and output voltages and currents with a digital multimeter, similar to the Agilent 34401A models [16], for a range of increasing input signals. The measurements continued until the amplified signal was clearly distorted. Figure 12 shows the measured results. Figure 12 a) shows the measured efficiency when the amplifier is driven with a sine wave input while b) shows the measured efficiency when driven with the proposed test signal. The efficiency measurements shows that the FDD3672 MOSFET is preferable for sine wave amplification while the IRLR110PbF is preferable for audio amplification. It is seen that the low power efficiency is approved approximately 10% when using the IRLR110PbF power MOSFET. In this way the results shows the same tendency as shown in the theoretically analysis above. That is that the efficiency of the amplifier benefits more from low parasitic capacitances than from a low on resistance when used for audio. This is due to the fact that the power drawn from the amplifier when playing audio is significantly lower than when playing sine waves and at low power the switching losses are dominating. In addition to this it can be mentioned that the end user will listen to music at background levels most of the time according to [17], lowering the power drawn even more. However no general conclusion or rule on which kind of MOSFETs to choose can be made from this study due to the fact that the presented results only are valid for the 12 V test amplifier. However the importance of using proper test signals when specifying the amplifier efficiency is clearly shown.



(a) Efficiency measured with sine wave as input signal.



(b) Efficiency measured with alternative test signal as input.

Fig. 12: Measured efficiencies for the amplifier using different input signals.

5 Conclusion

This paper has presented the fundamental principles of switch-mode power audio amplification. This include an overview of the different switching conditions the amplifier can undergo when used for audio amplification. A detailed analysis of the inherent loss mechanisms of the amplifier has been presented in order to model the efficiency. It was found that the properties of the switching devices have great impact on what kind of losses there can be expected. Switching devices with low on resistances and high parasitic capacitances will have higher idle losses but can achieve higher efficiencies at high output powers than switching devices with high on resistances and low capacitances. It has been shown that high output powers are easily reached when the amplifier is driven with a sine wave input thus favouring switching devices with low on resistances. However a thorough investigation of the amplitude distribution of 183 audio tracks has shown that sine waves are a very poor representation of real audio signals. A better audio representing signal is the IEC-268 filtered noise signal however this signal does not have a fundamental frequency like sine waves. Therefore an alternative test signal has been constructed which also represents audio signals very well. It was found that the crest factor of audio signals are much greater than that of sine waves thus lowering the RMS output power requirements of the amplifier significantly. This increases the importance of the losses related to the parasitic capacitances of the switching device. A series of efficiency measurements were conducted on a 12 V test amplifier equipped with two types of switching devices. The efficiency was measured when the amplifier was driven by a sine wave and when it was driven with the proposed test signal. The results correlated well with the expectations from the theoretical analysis meaning that measuring the efficiency with a sine wave input signal favours switching devices with low on resistances unfairly. Therefore it is of great importance to measure amplifier efficiency with a proper test signal. In addition to this it was shown that the low power efficiency could be improved approximately 10%.

6 Acknowledgements

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