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System-level Design of an Integrated Receiver Front-end for a Wireless Ultrasound Probe

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Abstract—In this paper a system-level design is presented for an integrated receive circuit for a wireless ultrasound probe, which includes analog front-ends and beamformation modules. The study focuses on the investigation of the effects of architectural design choices on the image quality. The point spread function is simulated in Field II from 10 to 160 mm using a convex array transducer. A noise analysis is performed, and the minimum signal-to-noise ratio (SNR) requirements are derived for the low-noise amplifiers (LNA's) and A/D converters (ADC's) to fulfil the design specifications of a dynamic range of 60 dB and a penetration depth of 160 mm in the B-mode image. Six front-end implementations are compared using Nyquist-rate and $\Sigma\Delta$ modulator ADC's. The image quality is evaluated as a function of the depth in terms of lateral full-width at half maximum (FWHM) and −12 dB cystic resolution (CR). The designs that minimally satisfy the specifications are based on a 8-bit 30 MSPS Nyquist converter and a single-bit 3rd order 240 MSPS $\Sigma\Delta$ modulator, with a SNR for the LNA in both cases equal to 64 dB. The mean lateral FWHM and CR are 2.4% and 7.1% lower for the $\Sigma\Delta$ architecture compared to the Nyquist-rate one. However, the results generally show minimal differences between equivalent architectures. Advantages and drawbacks are finally discussed for the two families of converters.

Index Terms—Portable ultrasound, wireless probe, receiver front-end, Synthetic Aperture Sequential Beamforming.

I. INTRODUCTION

In recent years, the benefits of point-of-care ultrasound imaging performed using hand-held scanners were identified as a game-changer in a large variety of clinical situations. These include austere medical departments such as ambulances and emergency rooms, and remote areas of developing countries [1], [2]. Several studies demonstrated that portable ultrasound devices are able to provide good image quality compared to high-end scanners, and allow a more accurate diagnosis than the stethoscope-based physical examination for patients suspected of cardiovascular abnormalities and referred for echocardiography [3], [4].

For such devices to undergo a widespread distribution, severe restrictions must be considered in terms of cost, size and power consumption, while the image quality must be preserved. Fuller *et al.* [5], [6] developed a low-cost, pocket-sized device for medical ultrasound imaging that integrates a fully sampled 2D array transducer, transmit/receive circuitry, a LCD display and a battery in a very compact enclosure.

However, the device is a C-scan imaging system conceived for needle-tracking and catheter insertion purposes, while the system object of this study is a general-purpose probe, and is therefore a more complex architecture. Comparable devices are present on the market, but very limited technical information is publicly available.

Poland *et al.* [7] proposed a battery-powered wireless probe integrating an array of transducer elements, a microbeam-former [8], and transmit/receive circuits and antennas in a compact enclosure. The sampled partially beamformed signals are sent to an external host system for further beamforming, image processing and displaying. The cable-free solution has the twofold advantage of effectively improving the manoeuvrability while reducing the cost of the probe, as the bulky cable has a significant impact on the market price of the system.

Recently, Siemens Medical Solutions USA, Inc., developed and commercialized a wireless scanner (ACUSON Freestyle™) using proprietary ultra-wideband radio communication protocols and high speed antennas [9]. However, taking advantage of general purpose mobile devices would significantly benefit the cost effectiveness and help supply ultrasound imaging to non-conventional markets.

Hemmsen *et al.* [10], [11] demonstrated the feasibility of a wireless ultrasound system using consumer level mobile devices, such as smartphones and tablets. The overall objective is to use the mobile devices as system hosts for the data processing and visualization, interfaced to an external probe for the acquisition of the ultrasound field. The system is based on Synthetic Aperture Sequential Beamforming (SASB) [12], [13]. The received field is beamformed within the probe handle using a fixed-focus, and further processing is performed in the mobile device after the wireless transmission of the ultrasound data. The idea enables the possibility to critically lower the price of the imaging system, taking ultrasound devices closer to the mobile health (mHealth) concept emerged in the past decade.

Having demonstrated that the wireless transmission of the ultrasound data is possible, a suitable hardware implementation must be found that suits the power consumption limitations while satisfying the image quality requirements. The low noise amplifier (LNA) and A/D converter (ADC) have in particular a significant influence on the power dissipation,
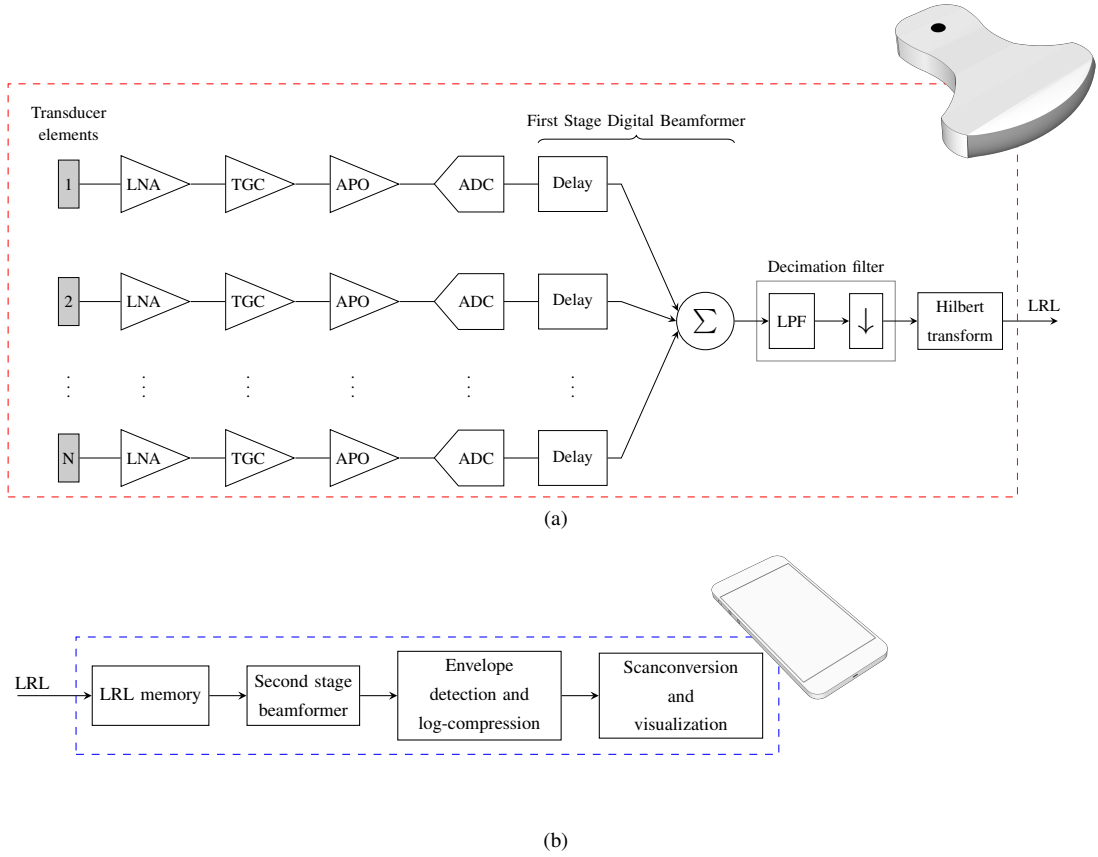
Fig. 1. Schematic overview of the wireless ultrasound system: receiving front-end and beamformation modules are integrated in the probe handle (a); and a post-processing unit is software-implemented in the mobile device (b).

circuit area, and cost of the system. State-of-the-art commercial integrated circuits are overdesigned for the imaging performance of a portable system, at the expenses of the power dissipation, which makes it difficult to integrate the circuitry in a compact form factor. This is discussed in Section III-A, where it is shown that the power consumption of current, commercial chipsets exceeds the power budget for a hand-held scanner. A dedicated chip is therefore required to minimally fulfil the performance requirements and prevent avoidable power usage.

A system-level investigation is presented in this paper for the design of a dedicated integrated circuit (IC) that includes analog front-end (AFE) and beamforming modules. The minimum noise requirements for the LNA and ADC are derived to fulfil the specifications of a 60 dB dynamic range and a penetration depth of 160 mm in the B-mode image. The resolution and contrast are evaluated considering Nyquist-rate and oversampling $\Sigma\Delta$ converters to investigate the effects of architectural design choices on the image quality.

The remainder of the paper is organized as follows: the SASB focusing technique is introduced in Section II; in Section III, the architecture is presented and the design using commercial integrated devices is considered; the details on the critical components are introduced and discussed in Section IV; Section V describes the simulation setup for the preliminary noise study and the system-level comparison; the results are presented in Section VI, and system-level considerations are finally discussed in Section VII.

II. SYNTHETIC APERTURE SEQUENTIAL BEAMFORMING

In conventional ultrasound imaging, a sector is scanned by sweeping a set of narrow beams in a number of directions. For a given depth of field, tradeoffs between image quality and frame rate are imposed by the speed of sound and the number of acquired lines. In addition, the image is optimally focused only at one depth, if a single focused transmission is used per direction. Synthetic Aperture (SA) [14]–[17] techniques overcome these limitations by collecting the information from the entire imaged sector at once using defocused spherical waves, dynamically focused in receive to obtain low-resolution frames. A fully-focused image with spatially independent resolution is therefore synthesized by coherently combining a number of low-resolution frames.

The heavy data handling demand imposed by the need to compute and store several frames for creating a high-resolution image, makes the implementation of a full SA beamformer challenging in a real system. The sequential beamforming idea was introduced to loosen the system requirements combining the monostatic SA focusing technique [14] with the concept of virtual source (VS) created by means of a focused emission [18]–[20]. A dual-stage beamformer is used in receive to reduce the data throughput and storage demand, taking advantage of the SA approach in a downscaled setup. The first stage is a fixed-focus beamformer with the focal point coincident

TABLE I
POWER DISSIPATION FOR THE DESIGN BASED ON COMMERCIAL INTEGRATED CIRCUITS

Model	# of bits ADC	Sampling frequency [MSPS]	ADC SNR [dB]	Variable gain range [dB]	Power dissipation/ch. [mW/ch]	Total power dissipation (64 ch.) [W]
AD9273-25	12	25	70	42	102	6.53
AD9278	12	40	70	45	88	5.63
AFE5816	12	40	70	39	55	3.53
AFE5807	12	40	72	40	97	6.21

with the VS position. A number of beamformed RF-lines - referred to as low-resolution lines (LRL's) in the remainder of the paper - from a number of emissions is then stored and sent to the second stage beamformer for re-focusing. For a thorough understanding of the sequential beamforming implementation, readers are referred to the cited articles.

The performance of the SASB approach was first investigated by Kortbek *et al.* [12], [13] with a linear array transducer, demonstrating that the lateral resolution is globally improved compared to conventional dynamic receive focusing and less depth dependent. Hemmsen *et al.* [21] showed the feasibility with a convex array through wires and tissue mimicking phantoms. Finally, the clinical evaluation of the method was performed in [22] by Hemmsen *et al.*, and SASB was proven to provide an image quality comparable to that of conventional imaging. In [22] the VS's were positioned at a depth of 70 mm using 64 active elements in transmit and receive. The same setup is maintained here and used as a starting point for the design of the probe with the intention of keeping consistency with the imaging setup evaluated in the clinic.

III. ARCHITECTURE OVERVIEW

A block diagram of the wireless ultrasound system is schematically outlined in Fig. 1. In particular, Figure 1a shows the receiver front-end addressed in this study. $N = 64$ channels consisting of analog pre-amplifiers, ADC's, and delay-and-sum modules process the signals received by a sub-array of transducer elements. The beamformation is performed in the digital domain although the first fixed-focus beamformer can be realized using simple analog circuitry [23]. Flexibility and robustness considerations make the digital implementation a more attractive option, and the possibility for the focal point to be moved along the depth and the beam steered across different directions opens the way for the integration of a wide spectrum of imaging modalities in a very versatile system.

The beamformed low-resolution lines are first downsampled to the Nyquist rate f_N and Hilbert transformed to obtain the in-phase and quadrature components. These are sent via wireless link to the external processing unit (Fig. 1b), where a set of lines is stored. In [10], a setup similar to the one investigated here was implemented, and a data throughput of 25.3 MB/s was demonstrated to be sufficient for achieving real-time performance. A high-resolution image is finally created by the second stage beamformer, and envelope detection, log-compression, and scan-conversion are performed before the image is displayed.

A. Design using commercial integrated circuits

Particular conditions are imposed on the power consumption of a portable system compared to that of a cart-based scanner due to the integration of the front-end into the handle. The heating of the transducer surface in contact with the patient's skin must be kept below the limits of the Food and Drug Administration (FDA) [24] and the International Electrotechnical Commission (IEC) [25]. Furthermore, the IEC limits to 75 °C the temperature for continuously held plastic components. In addition, the battery capacity is limited by size and weight constraints. Referring for comparison to a consumer level smartphone, it is frequent during a phone call to experience the heating of the device, which causes discomfort for the user. For such use-case, the average power is reported in [26] to be between 747 and 1135 mW.

A wireless probe encounters the same thermal design challenges of mobile devices. Due to manoeuvrability requirements, active cooling strategies can not be used, therefore the heat is conveyed by conduction to the casing, and then partially transferred to the user's hand. Taking into account an external surface of the wireless probe approximately doubled compared to the one of a conventional smartphone, the ideal power consumption is about 2.2 W, and should not exceed 3 W for comfortable use.

As a first step, the feasibility of the wireless probe was investigated using the four least power consuming commercial AFE's from Analog Devices, Inc., and Texas Instruments, Inc. The IC's include a LNA, a variable gain amplifier (VGA), and an ADC for each channel. The total power dissipation for a 64-channel system is shown in Table I, and results for all the cases greater than 3 W. Furthermore, additional power usage must be considered for the beamformation, in particular for the multi-bit interpolation needed to achieve the suitable delay resolution (see Section IV-C), and for chip-to-chip communication. Therefore, the power consumption of current, commercial circuits exceeds the power budget of a hand-held scanner.

Owing to the considerations discussed above, a dedicated integrated circuit is required to minimally fit the design specifications while fulfilling the power demands. Integrating beamformer and front-end on the same chip offers the advantage of minimized connector pin count, resulting in a lower power consumption. A system-level design for such device is presented in the remainder of the paper.

IV. PROBE DESIGN

In this section the models considered for the design of the analog front-end are introduced. Time and depth are used
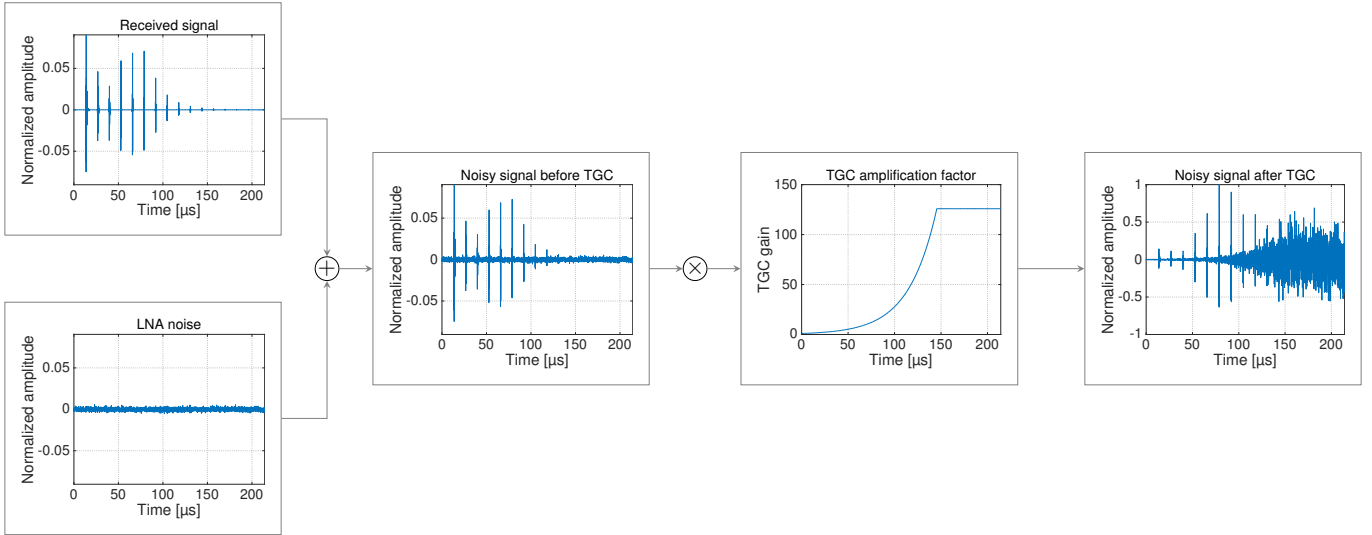
Fig. 2. Noise model for the LNA: the received signals are attenuated due to the propagation in the tissue, and a depth-independent noise is added in the LNA stage giving a depth-dependent SNR. A variable gain is then applied as a function of the depth for the time-gain compensation. The amplitudes are normalized to the input voltage range of the ADC.
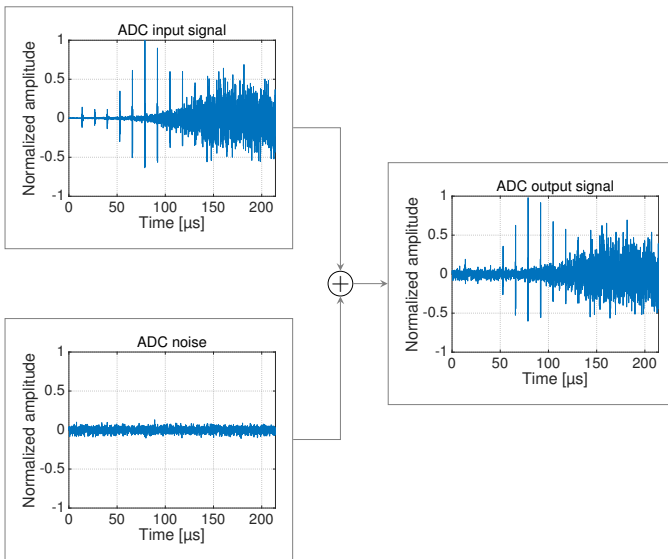

Fig. 3. Noise model for the ADC: quantization and thermal noise are considered as a depth-independent, white Gaussian noise source, and a depth-dependent SNR degradation is introduced where the saturation of the TGC amplifier occurs.

here interchangeably, being the quantities related by a direct proportionality in case of constant speed of sound.

A. Analog front-end

In the AFE in Fig. 1a, the received echoes are first amplified by LNA's located close to the transducer elements, and a depth-dependent gain factor is introduced by VGA's for the time-gain compensation (TGC) of the attenuation caused by the propagation in the tissue. Finally, an apodization function is used to suppress the sidelobes in the low-resolution lines.

In Fig. 2, the model for the noise of the LNA is displayed. The received signals are attenuated by a factor α - equal to $0.5\,\mathrm{dB\,cm^{-1}\,MHz^{-1}}$ in the figure - to take into account the propagation losses, and a depth-independent noise is added in the LNA stage. As a consequence, the Signal-to-Noise Ratio (SNR) of the noisy signal is decreasing as a function of the depth. A TGC amplification factor is applied to compensate for the attenuation. In the figure, the TGC amplification is limited to a range 0–42 dB and saturation occurs at about $146\,\mu\mathrm{s}$, corresponding to a depth of $11.2\,\mathrm{cm}$. The amplitudes in the figure are normalized to the input voltage range of the ADC. The model is used for the simulations described in Section V.

The noise model for the ADC is shown in Fig. 3. Quantization and thermal noise contributions are thought of as an additive depth-independent white Gaussian noise source. The TGC in Fig. 2 provides a way of using the entire input dynamic range of the ADC at all the depths, and does not alter the SNR in this model. However, the amplitude of the received signal is lower than the input range of the ADC at the depths where the saturation of the TGC amplifier occurs. This introduces a further depth-dependent SNR degradation, being the noise of the ADC at a constant level throughout the depth.

The performance of the LNA is critical for achieving the design specifications, in particular for what concerns the depth of penetration. Nonlinearities and distortions introduced at this stage are unlikely to be removed in subsequent steps, and a high SNR is required to limit the amount of noise introduced in the signal processing chain. High-performance, however, is directly translated into increased power consumption, and has an important impact on the power budget.

B. Analog-to-Digital converter

A number of parameters can be used for the characterization of A/D conversion performance, including stated resolution, SNR, spurious-free dynamic range, two-tone intermodulation distortion, and power dissipation [27]. The following discussion is based on SNR considerations, due to the fact that
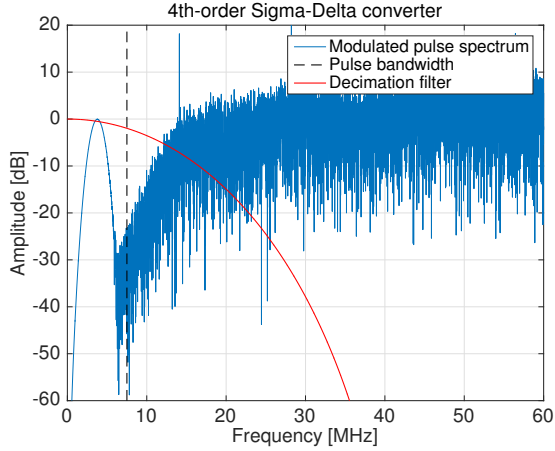
Fig. 4. Spectrum of a 3.75 MHz pulse modulated with a single-bit 4th-order $\Sigma\Delta$ converter with 360 MSPS sampling frequency. Most of the quantization noise is out of signal bandwidth (black dashed line) and can be filtered in the digital domain. The transfer function of the decimation filter is plotted in red.

the design specifications are highly influenced by the noise level. In an ideal ADC, the quantization is the only process introducing noise in the digital signal. The quantization error can be considered to be a uniformly distributed, zero-mean, white noise, if the quantizer is not overloaded and under the assumption of uncorrelated successive quantization error samples [28]. The assumption is valid, if the quantization step is small compared to the signal amplitude, and the signal is sufficiently complex. For a conventional Nyquist-rate converter with sampling rate f_s and L bits of resolution, the theoretical Signal-to-Quantization Noise Ratio (SQNR) in dB is defined as:

$$SQNR = 10\log\left(\frac{\sigma_s^2}{\sigma_e^2}\right) = 6.02L + 10\log_{10} m + 1.76, \quad (1)$$

where σ_s^2 and σ_e^2 identify the power for the signal and the in-band quantization noise, and $m = f_s/f_N$ is the oversampling ratio. In a real ADC, however, the noise spectrum contains contributions from other sources such as thermal noise from the circuitry, aperture uncertainty, and comparator ambiguity. These result in a lower SNR compared to the SQNR, and the effective number of bits (ENOB), defined as:

$$ENOB = \frac{SNR - 1.76}{6.02}, \quad (2)$$

is used, which takes into account all the noise contributions. In [27], the average difference between stated resolution and ENOB for state-of-the-art ADC's was reported to be approximately 1.5 bits. Only quantization and thermal noise are considered in this study.

It can be noted in (1) that the SQNR is increased by approximately 6 dB for every additional bit of resolution and 3 dB for every doubling of the oversampling ratio. Hence, it is possible to trade speed with resolution [28], and this opens the way to the realization of low-complexity, high-speed processing systems. $\Sigma\Delta$ A/D converters [29]–[31] combine oversampling with noise shaping to modify the power spectral density of the quantization noise such that most of the noise

is out of the signal bandwidth and can be filtered in the digital domain before the signal is downsampled.

The spectrum of a 3.75 MHz pulse modulated with a single-bit 4th-order $\Sigma\Delta$ converter with a sampling frequency of 360 MSPS is shown as an example in Fig. 4. For such converters, the calculation of the SQNR must take into account the noise-shaping transfer function as well as the digital decimation filters to account for the residual out-of-band noise that partially aliases in the signal bandwidth when decimation occurs. For the $\Sigma\Delta$ modulators used in Section V-B, the SQNR was found by simulating a full-scale sinusoid.

If the thermal noise generated by the ADC's circuitry is taken into account, the total SNR in dB can be defined as:

$$SNR = 10\log\left(\frac{\sigma_s^2}{\sigma_e^2 + \sigma_{th}^2}\right) = 10\log\left(\frac{\sigma_s^2}{\sigma_n^2}\right), \quad (3)$$

where σ_{th}^2 is the thermal noise power and σ_n^2 the total noise power. It is common practice to design the ADC with a SQNR greater than the target SNR [32]. The overall performance is therefore limited by the thermal noise rather than the quantization noise. For all the ADC's considered in the following sections, the SQNR was designed to be 6 dB greater than the target SNR.

C. First-stage beamformer

In the digital fixed-focus beamformer actual delay values are quantized to the sampling period, and a phase error is introduced in the beamformed line, which contributes to the sidelobes amplitude [33]. Different approaches can be used to achieve the adequate delay resolution needed for the sidelobes level to drop below the system's dynamic range.

A first method oversamples with a ratio $m > 1$. Typical ratios are in the range from five to ten [34], and this introduces an additional overhead. However, the delay line can be easily realized by means of a simple first-in-first-out (FIFO) shift register.

As an alternative, digital delay interpolation can be used to obtain the required delay resolution saving ADC and memory resources [34]. The received signals are in this case sampled at the Nyquist rate and $K - 1$ intra-sample values are calculated for each pair of successive samples giving an effective oversampling ratio of K. A finite impulse response (FIR) filter with approximately $5K$ coefficients is required in each channel for this purpose [34], with increased computational cost.

The delay interpolation is typically preferred with multi-bit ADC's, as this provides in this case a less expensive solution. Conversely, oversampling converters, such as $\Sigma\Delta$ modulators, yield an inherently high sampling frequency, and better suit the oversampling beamforming approach without any additional cost.

V. Methods

A simulation study was performed to investigate the effects of design choices on the image quality. The minimum noise requirements were derived for the LNA and ADC to satisfy the specifications of a 60 dB dynamic range and 160 mm penetration depth in the B-mode image. Several front-end

TABLE II
SIMULATION PARAMETERS

Speed of sound	$1540\,\mathrm{m\,s^{-1}}$
Attenuation factor - α	$0.5\,\mathrm{dB\,cm^{-1}\,MHz^{-1}}$
Transducer parameters	
Transducer	Convex array
Center frequency	3.75 MHz
Number of elements	192
Transducer element pitch	0.33 mm
Transducer element height	13 mm
Convex curvature radius	61 mm
Elevation focus	65 mm
Transmit parameters	
Center frequency - f_0	3.75 MHz
Signal bandwidth	7 MHz
Excitation	2-cycle weighted sinusoid
Apodization function	Rect function
Active aperture size	64 elements
Focus axial position	70 mm
$f\#$	3.3
Number of emissions	269
Receive parameters	
Apodization function	Hamming
Active aperture size	64 elements
Focus axial position	70 mm
$f\#$	3.3
TGC range	0–42 dB
Second stage parameters	
Apodization function	Hamming

implementations using equivalent Nyquist-rate and $\Sigma\Delta$ converters were examined to evaluate the influence of system-level considerations on the imaging resolution and contrast.

A model of the system was built in MATLAB (The MathWorks Inc., Natick, MA), and the analytic signals were obtained through a Hilbert transform. The second stage beamformer was implemented with the BFT3 toolbox [35], and the high-resolution images showed with a dynamic range of 60 dB.

The simulation parameters are shown in Table II. A 192-element convex array transducer with center frequency $f_0 = 3.75$ MHz was used and focused in transmit/receive at a depth $z_f = 70$ mm. The active aperture was limited to $N = 64$ elements and gives a transmit f-number $f\# = 3.3$, where $f\# = z_f/L_A$ and L_A is the aperture length. A Hamming function was used for weighting the received echoes in the first stage as well as the beamformed low-resolution lines in the second stage, while no apodization was applied on the emitting aperture. The point spread function (PSF) was simulated in Field II [36], [37] from 10 to 160 mm in steps of 10 mm. Absorption and scattering losses were included by means of an attenuation factor $\alpha = 0.5\,\mathrm{dB\,cm^{-1}\,MHz^{-1}}$. The TGC was introduced as an amplification curve with a slope equal to αf_0 in the range 0–42 dB. For this setup, the maximum gain of the amplifier is attained at a depth of 11.2 cm.

The study focused on the analysis of the LNA and ADC modules as these components are expected to significantly contribute to the final power consumption, owing to the considerations discussed in Section III-A. The TGC and apodization amplifiers were therefore considered ideal throughout all the simulations.

A. SNR study

The noise introduced by the analog circuitry and by the ADC has a direct influence on the dynamic range and depth of penetration, as illustrated in Section IV-A. An ideal ADC was first considered with a sampling frequency of $f_N = 15$ MSPS and infinite resolution. The beamformation was performed assuming non-quantized delay values. The same model as shown in Fig. 2 was used for the LNA, consisting of a depth-independent white Gaussian noise source $e(t)$. The power of $e(t)$ in the 7 MHz signal bandwidth was calculated to obtain the desired SNR relative to the power of a full-scale sinusoid. The SNR of the LNA was swept from 0 to 80 dB in steps of 5 dB, and $M = 50$ independent simulations were performed at each step to find the output SNR at the 16 points where the PSF was simulated. A noiseless signal $\bar{y}$ was also simulated and, denoting by $y(n, i)$ the complex sample at the n-th point for the i-th noisy simulation, with $n = 1, ..., 16$, the noise power was calculated as:

$$\sigma_n^2(n) = \left| \frac{1}{M} \sum_{i=1}^{M} (y(n, i) - \bar{y}(n))^2 \right|. \tag{4}$$

The SNR was found as:

$$SNR(n) = 10 \log \left(\frac{\sigma_s^2(n)}{\sigma_n^2(n)} \right), \tag{5}$$

with $\sigma_s^2 = |\bar{y}|^2$ the power of the noiseless signal.

A minimum requirement of 42 dB for the LNA results from the preceding simulations. This corresponds to a noise voltage of $3\,\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ at the output of the LNA. The input noise voltage for an actual amplifier depends on the gain, and is therefore a function of the amplitude of the received signals. The SNR of the LNA was then fixed to 48 dB and 64 dB to analyze the system behaviour in two different cases, and the same procedure was repeated to find the minimum requirement for the ADC to fulfil the design specifications. The signals were sampled at $f_N = 15$ MSPS and a second white Gaussian noise source was added to model the ADC quantization and thermal noise contributions. The assumption of a uniformly distributed white quantization noise is valid, if the conditions stated in Section IV-B are satisfied. The SNR of the ADC was swept from 0 to 80 dB in steps of 5 dB and $M = 50$ simulations were performed to find the SNR in the output image as indicated by (4) and (5).

B. System-level comparison

Six AFE implementations were simulated to investigate the effect of architectural design choices on the image quality. Three conventional Nyquist-rate converters were compared along with three single-bit $\Sigma\Delta$ ADC's. The parameters of the simulated ADC's are reported in Table III. The SNR of the LNA was set equal to 64 dB in all the simulations.

For the Nyquist-rate converters, a sampling frequency of $f_s = 30$ MSPS ($m = 2$) was used, with a resolution of 5, 8, and 10 bits. The three architectures are referred to as Nyq5, Nyq8, and Nyq10 in the remainder of the paper. The SQNR calculated according to (1) is equal to 35 dB, 53 dB, and 65 dB, respectively. White Gaussian noise was added to mimic the

TABLE III
PARAMETERS OF THE A/D CONVERTERS USED IN THE SYSTEM-LEVEL
SIMULATION STUDY

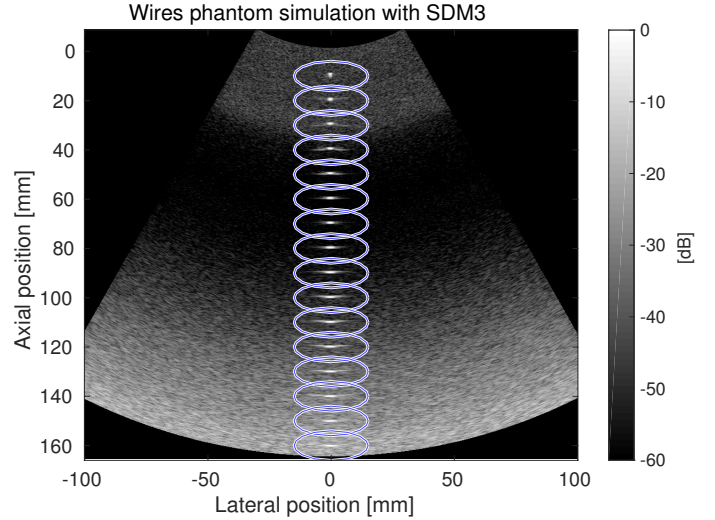|	Resolution	f_s	Decimation	SQNR	SNR
	[bit]	[MSPS]	-	[dB]	[dB]
Nyquist	5	30	2	35	29
	8	30	2	53	47
	10	30	2	65	59
	Order	f_s	Decimation	SQNR	SNR
	-	[MSPS]	-	[dB]	[dB]
$\Sigma\Delta$	2	120	2 and 4	35	29
	3	240	4 and 4	55	49
	4	300	5 and 4	65	59

Fig. 5. B-mode image of the wire phantom simulated with the SDM3 architecture. The highlighted regions surrounding each point target were used for the calculation of the cystic resolution as stated in Eq. (8). The SNR was estimated from 50 simulations (see Fig. 7), and it is assumed constant in each region.

thermal noise, with a final SNR 6 dB lower than the SQNR. The actual delay values were quantized with a resolution of $T_0/24$, with $T_0 = 1/f_0$ the pulse period. If $f_N = 4f_0$, the required oversampling ratio is 6, and a FIR interpolation filter with at least 15 coefficients and 30 MHz clock frequency is needed for each channel, as discussed in Section IV-C. A matched FIR decimation filter was used before downsampling the beamformed lines to the Nyquist rate.

Three single-bit $\Sigma\Delta$ ADC's were used: 2nd order with $f_s = 120$ MSPS ($m = 8$), 3rd order with $f_s = 240$ MSPS ($m = 16$), and 4th order with $f_s = 300$ MSPS ($m = 20$). The architectures are referred to as SDM2, SDM3, and SDM4. A MATLAB model was developed for the modulators following the procedure in [38]. The noise transfer functions were determined by designing 2nd, 3rd, and 4th order high-pass Butterworth filters. The downsampling of the beamformed lines was performed in two steps: a first *sinc* cascaded-integrator-comb (CIC) stage [39] was used before downsampling with a decimation ratio of 2, 4, and 5 for the three architectures. Finally, the Nyquist rate was restored after matched filtering and decimation with a ratio of 4.

The SQNR for the oversampling converters was estimated from $M = 50$ simulations of each modulator cascaded with the relative decimation filters to take into account the out-of-band quantization noise aliased in the signal bandwidth when decimation occurs. A sinusoid $\bar{x}(k)$ with center frequency of 3.75 MHz was modulated, and the resulting single-bit signal filtered and downsampled. The SQNR was calculated as:

$$SQNR = 10\log\left(\frac{\sigma_{\bar{x}}^2}{\sigma_{qn}^2}\right), \qquad (6)$$

where $\sigma_{\bar{x}}^2$ is the power of the sinusoid and:

$$\sigma_{qn}^2 = \frac{1}{M}\frac{1}{K}\sum_{i=1}^{M}\sum_{k=1}^{K}(x_i(k) - \bar{x}(k))^2 \qquad (7)$$

is the estimated quantization noise. In (7), x_i is the decimated signal from the $i-$th simulation and K the number of temporal samples. The resulting SQNR is equal to 35 dB, 55 dB, and 65 dB for the three architectures. White Gaussian noise was added for a final SNR 6 dB lower than the estimated SQNR. For the three oversampling architectures, the beamformation

was performed by merely shifting the single-bit signals, and the delay resolution is equal to $T_0/32$, $T_0/64$, and $T_0/80$, respectively, with no need for temporal interpolation.

A 1-D gain compensation was applied after the second stage beamformer to the envelope detected signals for equalizing the peak amplitudes of the point targets. The PSF was evaluated in terms of lateral Full-Width at Half Maximum (FWHM) and -12 dB cystic resolution (CR) to investigate the effects on the image quality of architectural choices in presence of noise, in particular concerning the delay quantization. The latter metric is defined as the radius ρ of a void centred on the maximum of the PSF providing a contrast $C(\rho)$ equal to -12 dB [40], calculated by:

$$C(\rho) = 10\log\left(\frac{1 + SNR^2\left(1 - \frac{E_{in}(\rho)}{E_{tot}}\right)}{1 + SNR^2}\right), \qquad (8)$$

where $E_{in}(\rho)$ is the PSF energy inside the void and E_{tot} the total PSF energy.

A B-mode image of the wire phantom simulated with the architecture SDM3 is shown in Fig. 5. The ellipses highlight the regions in which the total PSF energy E_{tot} was calculated. In each region, the SNR was assumed constant. This was estimated from $M = 50$ independent simulations as stated in Eq. (4) and (5) for each of the six architectures considered. The mean and standard deviation of the FWHM and CR showed in Section VI were also estimated from the 50 simulations.
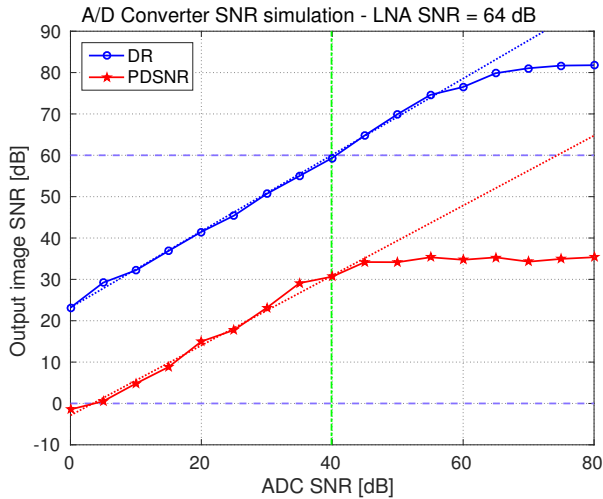
VI. RESULTS

In this section the results of the simulation studies introduced above are shown, and the effects of design choices on the image quality are discussed.

Low-Noise Amplifier SNR simulation

(a)

A/D Converter SNR simulation - LNA SNR = 48 dB

(b)
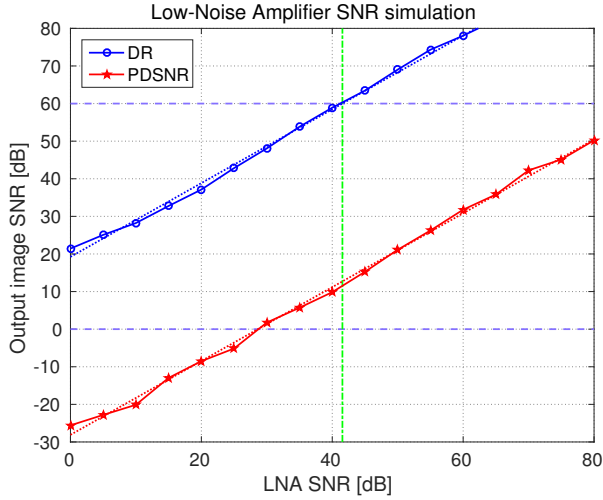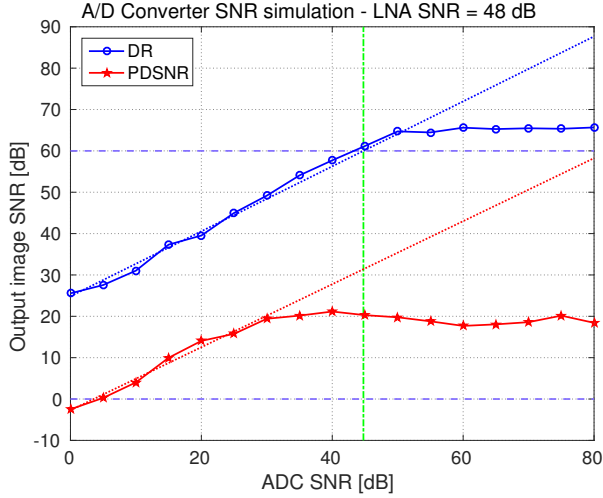
A/D Converter SNR simulation - LNA SNR = 64 dB

(c)

Fig. 6. Result of the preliminary noise study for the LNA and ADC: (a) the blue curve shows the dynamic range (DR) and the red curve shows the SNR at a depth of 160 mm (PDSNR) in the B-mode image as a function of the SNR of the LNA; (b) DR and PDSNR as a function of the SNR of the ADC for LNA SNR = 48 dB; (c) DR and PDSNR as a function of the SNR of the ADC for LNA SNR = 64 dB. The green dashed lines indicate the minimum SNR requirements to fulfil the design specifications.
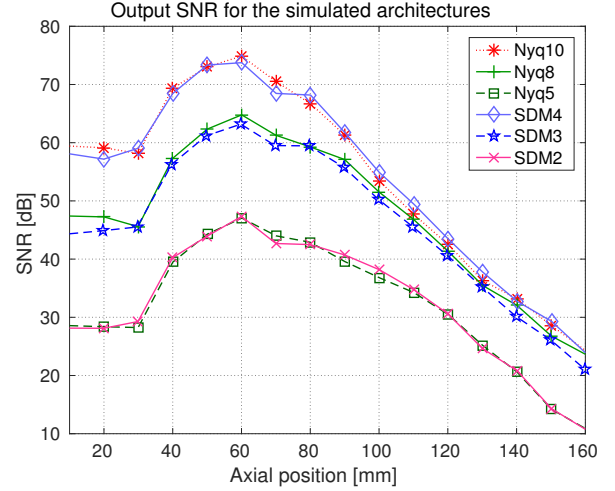
Output SNR for the simulated architectures

Fig. 7. Signal-to-noise ratio of the output image as a function of the axial position for the six simulated architectures in Table III.

A. SNR study

The result of the noise study for the LNA is shown in Fig. 6a. The top curve shows in blue the dynamic range (DR) and the bottom curve shows in red the SNR at a depth of 160 mm (PDSNR) in the B-mode image as a function of the LNA SNR. A linear regression is fitted to both the curves, and the minimum SNR requirement is highlighted by the green dashed line. The output SNR shows, as expected, a linear trend, and the minimum SNR requirement is equal to 42 dB. For this value, PDSNR is equal to 12.7 dB, and therefore the tightest constraint for this setup is set by the dynamic range specification.

The results of the noise study for the ADC are plotted in Fig. 6b for LNA SNR = 48 dB. The curves initially follow a linear trend, up to the point where DR and PDSNR equal the respective values for LNA SNR = 48 dB in Fig. 6a, i.e. 66 dB and 19 dB. Beyond this point, improvements in the ADC SNR no longer translate in better image quality, and the noise is dominated by the noise level of the LNA. The minimum ADC SNR requirement for this configuration is equal to 45 dB. A similar trend is shown in Fig. 6c for LNA SNR = 64 dB. The curves saturate at DR = 82 dB and PDSNR = 35 dB, and the minimum SNR requirement is 40 dB.

It is important to notice here that the noise requirements for the two components are strictly related, and increasing the SNR of the LNA loosens the requirement on the ADC. However, how this factor translates in terms of circuitry depends on the actual design and implementation of both the components. The SNR at 160 mm is everywhere greater than 0 dB in Fig. 6b and 6c; this suggests the possibility of decreasing the range of the variable gain for the TGC amplifier.

Different factors contribute to the dynamic range and to the SNR at the penetration depth. The noise introduced by the LNA and ADC propagates to the output image through a cascade of two beamformers. In the first stage, a fixed-focus is used with a static apodization. The SNR of the LRL is therefore improved compared to the received signals, and the improvement depends on the apodization window. In the
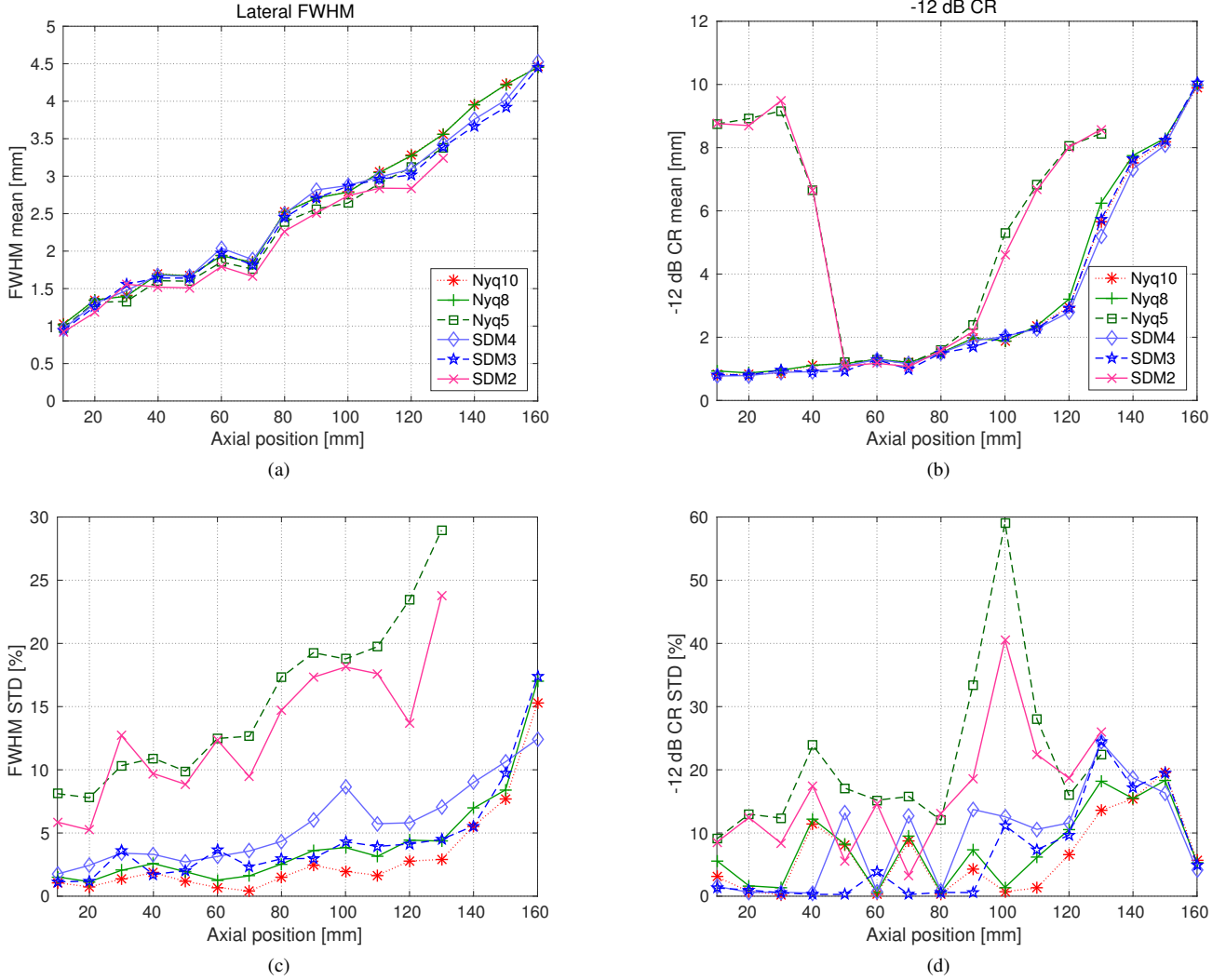
Fig. 8. The figures on the left side show the mean (a) and relative standard deviation (c) of the FWHM from 50 PSF simulations at 16 axial positions using the six architectures in Table III; on the right side, the mean (b) and relative standard deviation (d) are shown for the -12 dB cystic resolution.

second stage, the focus and apodization are dynamic, and the SNR of the high-resolution line increases as a function of the apodization window and the number of LRL's coherently added. The SNR is improved at all the depths except at the VS position, where one single LRL is considered. As shown in Fig. 7, the maximum SNR (dynamic range) occurs in proximity of the VS position, and is for this reason only partially influenced by the second-stage beamformer. On the other hand, the SNR at 160 mm is largely determined by the dynamic apodization of the second stage.

B. System-level comparison

According to the results of the preliminary SNR study, the architectures Nyq10, Nyq8, SDM4, and SDM3, satisfy the minimum SNR requirement to fulfil the design specifications, while Nyq5 and SDM2 provide a SNR 11 dB below the minimum requirement. The latter were chosen to investigate the image quality in case of under-designed configurations.

In Fig. 7 the SNR in the output image is shown as a function of the depth for the six architectures in Table III. As previously

mentioned, the SNR shows a peak in proximity of the focal position, and this is the value determining the output dynamic range. As expected, architectures similar in terms of SNR provide comparable results in the output image. Nyq8 and SDM3 are the ones which minimally fit the design specifications of a dynamic range equal to 60 dB and a penetration depth of 160 mm. Nyq10 and SDM4 show a different slope beyond the VS position compared to the other architectures; this is caused by the noise of the LNA dominating the overall performance in case of high SNR ADC's. The values in Fig. 7 were used for the calculation of the CR in (8), assuming a constant SNR throughout each elliptical region in Fig. 5.

The results for the lateral FWHM and CR are displayed in Fig. 8 for the six architectures. On the left side, the mean FWHM calculated from 50 independent simulations is plotted on the top figure (a), and the relative standard deviation is shown on the bottom (c). The mean FWHM shows as expected an increasing trend, and small differences are noticeable between the simulated architectures. The calculation for Nyq5 and SDM2 failed in the points from 140 to 160 mm for several

simulations, and the values for these points were therefore discarded. This was due to the high noise in the output image that made it difficult to identify the PSF. The relative standard deviation also shows an increasing trend due to the decreasing SNR as a function of the depth. Particularly high values were obtained for Nyq5 and SDM2 due to the lower SNR of these architectures.

On the right side in Fig. 8, the mean CR is plotted on the top (b) and the relative standard deviation on the bottom (d). The CR gives a measure of the contrast, and is influenced by the delay resolution. The results were expected to show significant differences among the simulated systems due to the better delay resolution of all the oversampling architectures compared to the Nyquist-rate ones. However, the results from pairs of similar architectures are comparable. This suggests that the contrast is actually dominated here by the noise rather than the delay resolution, i.e. errors in the beamformation introduced by the delay quantization yield a degradation in the output image, which is negligible compared to the noise where this is at a relatively high level. This is an important consideration that should be taken into account in further steps of the design process. The relative standard deviation is also comparable between the simulated architectures.

For Nyq8, the mean lateral FWHM is between 1.02 and 4.45 mm, and between 0.94 and 4.45 mm for SDM3. The FWHM is in average 2.4% lower for SDM3 compared to Nyq8. The mean CR is between 0.93 and 9.97 mm for Nyq8, and between 0.81 and 10.05 mm for SDM3, and results in average 7.1% lower for the latter architecture.

VII. DISCUSSION AND CONCLUSION

In this paper, a system-level design was performed for the receiver front-end circuit for a wireless ultrasound probe. The study focused on the investigation of the effects of architectural design choices on the image quality, with the purpose of determining the systems that minimally fulfil the image quality specifications. As a consequence of the compact form factor required for a portable system, strict limitations are posed in terms of power consumption if enough scanning time is to be ensured and the FDA and IEC limits satisfied. In Section III-A a power dissipation of 3 W was identified as a target for such system.

The minimum SNR requirements for critical components were derived by simulating the PSF using a convex array transducer, and the details of the noise propagation from the circuitry to the output image were introduced and discussed. Architectural design choices were argued and evaluated through the simulation of six different implementations based on Nyquist-rate converters and oversampling single-bit $\Sigma\Delta$ modulators. The results showed no considerable differences in terms of lateral resolution and contrast between equivalent Nyquist-rate and oversampling ADC's.

In [41], trends are shown for the performance and power efficiency of A/D converter designs as a function of time. The average power dissipation is reduced by a factor two approximately every two years, and this demonstrates that ADC's are constantly object of optimization. The gain is due to technology scaling and simplified architectures. However, it is difficult to characterize this trend as a function of the ADC architecture; the performance and power efficiency also depend upon the target application and the semiconductor technology. The same conclusion can be deduced from [27], where the most power-efficient converters are pointed out from different families such as flash, folded-flash, pipelined, and $\Sigma\Delta$ modulators. For these reasons, it is a great challenge at this proof-of-concept phase to make any assumptions on the power consumption and circuit area of the systems, and a worthwhile analysis would require their full development and characterization. Some considerations are summarized here from [29]–[31].

Conventional Nyquist-rate converters need precise analog circuits for their filters and comparators, and can be very sensitive to noise and interference [29]. Furthermore, a high-order analog antialiasing filter is required at the input of the converter to smooth the out-of-band components before they alias in the signal band as a consequence of the sampling process. Finely matched capacitors need to be used to achieve high precision conversion, which leads to large capacitive loads and, in turn, increased power dissipation, circuit area and cost.

Extraordinary efforts have been put in optimizing the power efficiency of these converters, using simplified analog circuits and digitally assisted A/D architectures [41]. However, they are often difficult to integrate in fine-line very-large-scale integration (VLSI) technologies [29], focused on providing high-speed digital processing rather than accurate analog circuits. Oversampling conversion, on the other hand, can be implemented using relatively high-tolerance analog components, and moves the resource requirement towards the digital domain. The technology scaling continuously experienced by CMOS processes makes it convenient from a power dissipation and circuit area perspectives to concentrate the challenging hardware requirements in the digital section. Furthermore, the high-speed conversion removes the need for the sharp antialiasing analog filter, and noise and interference are attenuated in the digital domain before the signal is downsampled to the Nyquist rate. The interconnection complexity between the ADC and the following processing modules is also reduced as the signals are converted in single-bit strings. For these reasons, $\Sigma\Delta$ converters well suit applications that require high-integration, low-cost, and densely packed circuit designs by taking advantage of fine-line VLSI technologies [29]. Finally, the use of oversampling converters also simplifies the beamformer architecture due to the inherently high sampling frequency that avoids temporal interpolation on the RF data.

This study demonstrated that single-bit $\Sigma\Delta$ converters can be employed in a hand-held setup maintaining the image quality. Further studies will investigate whether a power dissipation below 3 W can be attained for this system.

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