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Capacitive Substrate Coupling of Row–Column-Addressed 2-D CMUT Arrays

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***Abstract*—Row–column-addressed CMUT arrays suffer from low receive sensitivity of the bottom elements due to a capacitive coupling to the substrate. The capacitive coupling increases the parasitic capacitance. A simple approach to reduce the parasitic capacitance is presented, which is based on depleting the semiconductor substrate. To reduce the parasitic capacitance by 80% the bulk doping concentration should be at most $10^{12}\,\mathrm{cm}^{-3}$. Experimental results show that the parasitic capacitance can be reduced by 87% by applying a substrate potential of $6\,\mathrm{V}$ relative to the bottom electrodes. The depletion of the semiconductor substrate can be sustained for at least 10 minutes making it applicable for row–column-addressed CMUT arrays for ultrasonic imaging. Theoretically the reduced parasitic capacitance indicates that the receive sensitivity of the bottom elements can be increased by a factor of 2.1.**

I. Introduction

Row–column-addressed (RCA) 2-D arrays for ultrasonic imaging has recently attracted some attention, as they offer volumetric imaging with a greatly reduced channel count compared to fully addressed matrix arrays. The idea is to select the elements in the 2-D array either by the row or column index. Each row or column thereby acts as one large element. This effectively turns the array into two 1-D arrays, which are oriented perpendicular to each other. A corner of a capacitive micromachined ultrasonic transducer (CMUT) RCA array is shown in Fig. 1, with four row/top (orange) and four column/bottom (blue) elements and part of the top elements are removed to reveal the underlying CMUT cells.

Several groups have presented RCA CMUT arrays based on different fabrication processes [1]–[4]. They are all fabricated on a silicon substrate with an insulator separating the bottom electrodes from the substrate. The drawback is that the bottom electrodes will couple capacitively to the substrate, which appears to be grounded. This coupling introduces an increased parasitic capacitance of the bottom elements, which lowers the receive sensitivity [1], [3], [4]. A decrease of sensitivity lowers the signal-to-noise ratio of the received signal, and especially flow estimations are effected, as they rely on detecting echoes from the blood where the signal strength lies 30 to $40\,\mathrm{dB}$ below the signal from the surrounding tissue [5].

The objective of this paper is to experimentally demonstrate that by depleting the silicon substrate, the parasitic capacitance can be reduced significantly, and it can be sustained for a longer period of time making it applicable for RCA arrays for ultrasonic imaging.

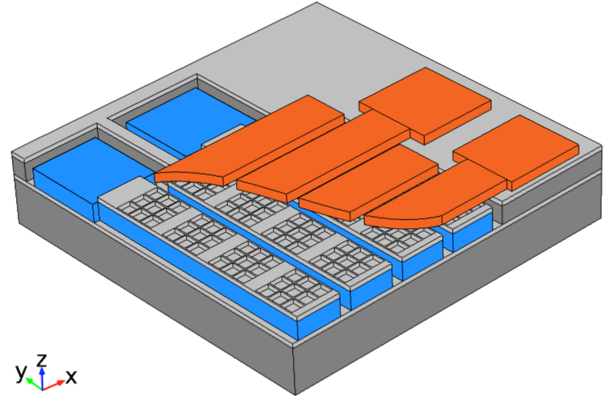

Fig. 1: 3-D illustration of an RCA transducer array showing a corner with four top and four bottom electrodes. The top electrode is colored orange and the bottom electrode blue. The light gray part between the electrodes is the insulator defining the cavities and the dark gray is the silicon substrate.

This paper is organized as follows: Section II explains the capacitive substrate coupling and possible solutions. Section III describes the fabricated devices. Section IV introduces the measurement setup. Section V comments and discusses the results and finally section VI concludes the paper.

II. Capacitive Substrate Coupling

The measured element capacitances of a 62+62 RCA CMUT probe (described in [4]) is shown in Fig. 2. Elements numbered 1-62 are colored blue and correspond to the bottom electrodes, and elements numbered 63-124 are colored orange and correspond to the top electrodes. The element capacitance of the bottom electrodes are roughly three times higher than the capacitance of the top electrodes, as a result of the capacitive coupling to the substrate. Fig. 3 illustrates two cross sections of a CMUT RCA array, (a) shows a cut perpendicular to the top electrodes and (b) shows a cut rotated 90°, perpendicular to the bottom electrodes. When a top electrode is probed (Fig. 3(a)) all bottom electrodes are grounded, hence only C_{CMUT} is measured. When a bottom electrode is probed (Fig. 3(b)) the substrate will appear grounded, since the signal may follow a path through the substrate and couple to ground via the neighboring bottom electrodes. Although the substrate has a non-negligible impedance, Z_{s}, the parallel coupling of

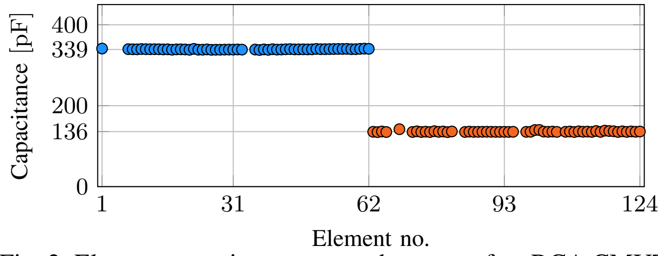

Fig. 2: Element capacitance across the array of an RCA CMUT probe [4]. Element number from 1-62 corresponds to the bottom electrodes and 63-124 to the top electrodes.

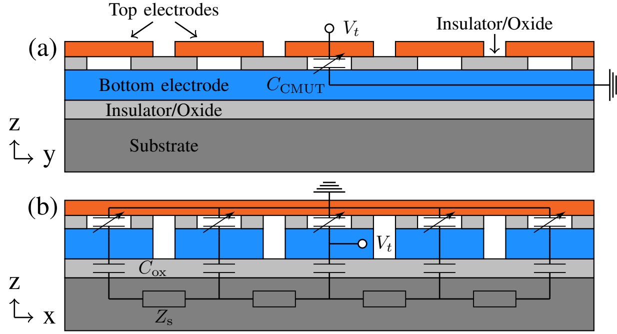

Fig. 3: Illustration of the electrical circuit seen when probing a top electrode (a) and a bottom electrode (b). The figures show a cross-section, such that the top electrodes are oriented perpendicular to the cut in (a), while the array is rotated 90° in (b).

the bottom electrodes results in a relatively low-impedance path to ground. Therefore, the capacitance measured when probing a bottom electrode will have a contribution from both C_{CMUT} and C_{ox}. The effect of the parasitic capacitance on the receive sensitivity, can be estimated by the electro-mechanical coupling factor [6]

$$k^2 = \frac{1}{1 + C_0/C_m}, \tag{1}$$

where C_0 is the total element capacitance and C_m is the lumped mechanical capacitance from the equivalent circuit model, which take the spring softening effect into account [7]. The parallel coupling of the parasitic capacitance, C_{ox}, will increase the total element capacitance, resulting in a lower electro-mechanical coupling coefficient.

To eliminate or reduce the substrate coupling different methods can be employed. The path through the substrate can be removed, hence the signal cannot couple to the neighboring elements. This can be realized by fabricating devices on an insulating substrate e.g. a quartz or fused silica substrate. However, the heat and electrical insulating substrate might introduce problems, both with concern to the fabrication and the operation of the final array. Another approach could be to increase the thickness of the insulator separating the bottom elements from the substrate. Growing several microns of silicon oxide will however require an extremely long oxidation time, which is not desirable. The intrinsic stress in the silicon oxide can also lead to a large wafer bow, further complicating the fabrication. A third approach, which can be directly implemented in the current fabrication processes [1]–[3], is to deplete the silicon substrate. The bottom electrode, insulator, and substrate are essentially a two-terminal MOS (Metal-Oxide-Semiconductor) capacitor. A MOS capacitor can be in three different modes, accumulation, depletion, and inversion. For an n-type substrate, accumulation occurs, when a positive bias is applied to the gate (bottom electrode). The positive charge on the gate will attract electrons from the substrate to the oxide-semiconductor interface. The capacitance measured in this mode will solely have a contribution from the oxide. When applying a negative voltage to the gate, the mobile electrons are pushed into the substrate leaving behind the ionized donor atoms. The surface region is depleted of mobile carriers and consist only of stationary charges from the donor atoms, hence the region is non-conducting. The capacitance measured in this mode has a contribution from both the oxide and the depletion region. When decreasing the gate voltage beyond the threshold voltage, inversion can occur. In inversion, a negatively charged layer is generated at the oxide-semiconductor interface as a result of minority carriers (holes) being generated in the depletion region and attracted to the interface. The capacitance measured will therefore only have a contribution from the oxide. Therefore, to reduce the parasitic capacitance, one has to operate the device in the depletion mode.

The parasitic capacitance, when depleting the substrate, can be modeled as two capacitors in series, the oxide capacitance, C_{ox}, and the depletion capacitance, C_{d}. The parasitic capacitance, C_{para}, normalized to the oxide capacitance is given by

$$\frac{C_{\text{para}}}{C_{\text{ox}}} = \frac{C_{\text{d}}}{C_{\text{d}} + C_{\text{ox}}} = \frac{t_{\text{ox}}\epsilon_{\text{si}}}{x_d\epsilon_{\text{ox}} + t_{\text{ox}}\epsilon_{\text{si}}}, \tag{2}$$

where t_{ox} is the oxide thickness, x_d is the depletion width, and ϵ_{ox} and ϵ_{si} is the permittivity of the silicon oxide and silicon, respectively.

The maximum depletion width, x_{dt}, of an n-type substrate is calculated as [8]

$$x_{dt} = \sqrt{\frac{4V_t\epsilon_{\text{si}}\ln\left(N_d/n_i\right)}{qN_d}}, \tag{3}$$

where V_t is the thermal voltage, q is the elementary electric charge, n_i is the intrinsic carrier concentration, and N_d is the bulk doping concentration. The maximum depletion width will depend on the bulk doping concentration and likewise the parasitic capacitance. Fig. 4 shows the normalized parasitic capacitance when the substrate is depleted, (2), for a device having a silicon oxide (insulator) thickness of $1\,\mu\text{m}$. To reduce the parasitic capacitance with 80% the bulk doping concentration should be $\sim 10^{12}\,\text{cm}^{-3}$. Such low bulk doping concentration can be obtained by manufacturing the wafers using the Float-zone technique.

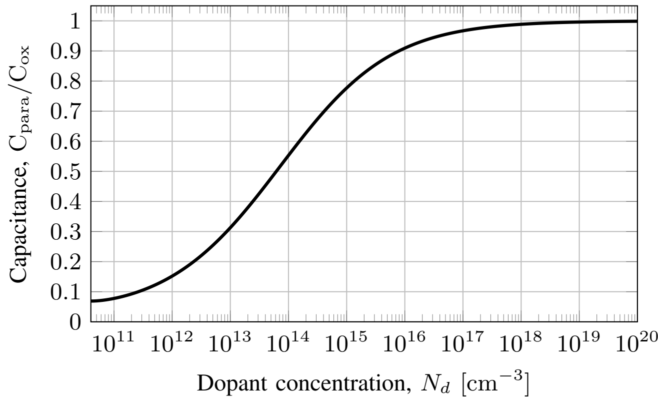

Fig. 4: The parasitic capacitance, C_{para}, when the substrate is fully depleted normalized to the oxide capacitance, C_{ox}, as a function of bulk doping concentration, N_d. The values are calculated by combining (2) and (3) where $t_{\mathrm{ox}} = 1\,\mu\mathrm{m}$.

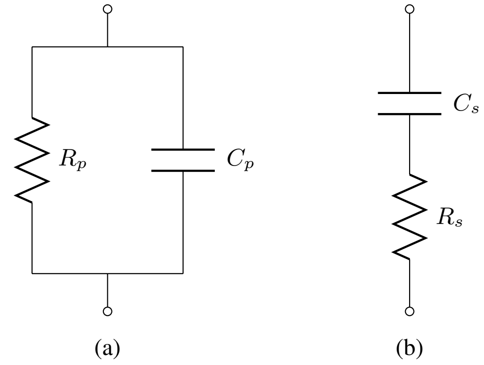

Fig. 5: Models for extracting the capacitance from the measured complex impedances. (a): Parallel resistance model (b): Series resistance model.

III. Design and Fabrication

In this study two wafers were fabricated to mimic the bottom electrodes of a 62+62 RCA CMUT array described in [4] with the exact same dimensions. Two SOI wafers were utilized both with a $2\,\mu\mathrm{m}$ low resistivity ($0.01 - 0.001\,\Omega\mathrm{cm}$) p-type device layer and a $1\,\mu\mathrm{m}$ thick buried oxide. The substrate of the first wafer is manufactured using the Czochralski process, is n-type having a bulk doping concentration of $N_d \approx 10^{15}\,\mathrm{cm}^{-3}$ and is referred to as CZ. The substrate of the second wafer is manufactured using the Float-zone process and is also n-type having a bulk doping concentration of $N_d \approx 10^{12}\,\mathrm{cm}^{-3}$ and is referred to as FZ.

A $200\,\mathrm{nm}$ aluminum layer is deposited on top of the device layer and an etch mask was defined on top of the aluminum using UV lithography to create the bottom electrodes. The aluminum was etched in a heated wet etch based on phosphoric acid and with the same mask the silicon was etched using a deep reactive ion etch (DRIE).

A gallium-indium eutectic was applied on the backside of the wafers to form an ohmic contact to the substrate to be able to control the substrate potential.

IV. Measurement Setup

The capacitance between the bottom electrode and the substrate was measured using an Agilent B1500A semiconductor Device Parameter Analyzer. The complex impedance is measured at $100\,\mathrm{kHz}$ and the capacitance is extracted using a series resistance model (Fig. 5(b)). This is chosen rather than the parallel resistance model (Fig. 5(a)) as the leakage current through the silicon oxide is assumed to be negligible due to its thickness. All measurements are carried out in darkness, to minimize the generation of charge carriers. A final CMUT array would be mounted in a probe and covered with a polymer for electrical insulation, hence no light can reach the CMUT and generate charge carriers.

Two different measurements were performed. 1: The capacitance was extracted as a function of substrate voltage and the voltage was swept from $-25\,\mathrm{V}$ (accumulation) to $25\,\mathrm{V}$ (depletion). 2: The capacitance was measured over time for varying substrate voltages to investigate the effect of depleting the substrate on a long term scale. The substrate potential was held in accumulation ($-25\,\mathrm{V}$) for 100 seconds before starting the measurement with a new substrate voltage. This was done to have a well defined starting condition.

V. Results and Discussion

The parasitic capacitance, C_{para}, normalized to the oxide capacitance, C_{ox}, measured for the two wafer types are shown in Fig. 6. As predicted by (2) the CZ substrate, with a bulk doping concentration of $10^{15}\,\mathrm{cm}^{-3}$, will only reduce the parasitic capacitance by less than 20%. By using the FZ substrate, with a bulk doping concentration of $10^{12}\,\mathrm{cm}^{-3}$, the parasitic capacitance is reduced to almost 10% of the oxide capacitance when depleting the substrate. This verifies that a low bulk doping concentration is required to reduce the coupling to the substrate substantially. The voltage is swept over a couple of seconds, whereas an ultrasound examination takes several minutes or even longer. To investigate the influence of time, the capacitance was measured over time for the FZ wafer. Fig. 7 shows a contour plot of the parasitic capacitance, C_{para}, normalized to the oxide capacitance, C_{ox}, over time for varying substrate voltages. At the time $t = 0\,\mathrm{min}$ the measured capacitance is similar to the CV curve shown in Fig. 6. As time goes, the measured capacitance is seen to increase, and this is most pronounced for higher substrate voltages. This is contrary to the expected, where a constant capacitance is expected when depleting the substrate. At $25\,\mathrm{V}$ after ten minutes the capacitance is increased to 46% of the oxide capacitance.

Further investigation is needed to clarify the mechanism resulting in the increase capacitance over time. A high bias voltage is therefore not advisable, instead a minimum of the capacitance at a substrate voltage of $6\,\mathrm{V}$ is observed. By applying $6\,\mathrm{V}$ to the substrate relative to the bottom electrodes, the parasitic capacitance can be reduced to below 13% of the oxide capacitance for at least 10 minutes. For a specific

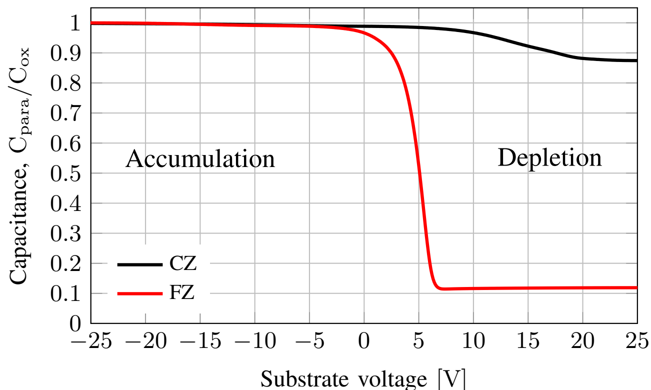

Fig. 6: C-V characteristics of two MOS capacitors with n-type substrates. CZ is manufactured using the Czochralski process with a bulk doping concentration of $N_d \approx 10^{15}\,\mathrm{cm}^{-3}$. FZ is manufactured using the Float-zone process with a bulk doping concentration of $N_d \approx 10^{12}\,\mathrm{cm}^{-3}$

device, as the one described in [4] where $C_m = 12\,\mathrm{pF}$, the electro-mechanical coupling factor will theoretically increase by a factor of 2.1 using (1).

VI. Conclusion

This paper demonstrated the experimental results of a simple method for reducing the capacitive substrate coupling, causing a low receive sensitivity of RCA arrays. The method is based on depletion of the semiconductor substrate by applying a potential to the substrate relative to the bottom electrodes. This method can be directly implemented into existing fabrication processes where the only requirements are that the bulk doping concentration of the substrate is low ($< 10^{12}\,\mathrm{cm}^{-3}$) and a contact is made for controlling the substrate potential. Experimental results show that the parasitic capacitance can be reduced by 87% by applying a substrate potential of 6 V relative to the bottom electrodes. The depletion of the semiconductor substrate can be sustained for at least 10 minutes making it applicable for RCA CMUT arrays for ultrasonic imaging. Theoretically the reduced parasitic capacitance indicates that the receive sensitivity of the bottom elements can be increased by a factor of 2.1.

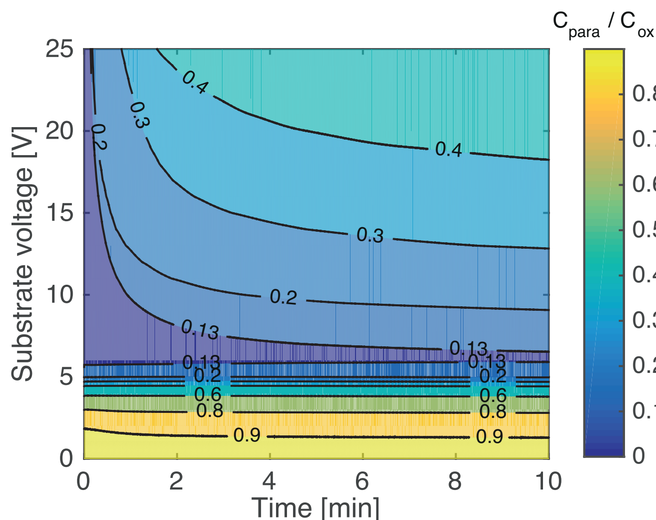

Fig. 7: The parasitic capacitance, C_{para}, of the FZ wafer normalized to the oxide capacitance, C_{ox}, for varying substrate voltages over time. A minimum in the capacitance is observed at a substrate voltage of 6 V.

Acknowledgement

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