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Abstract—Electric power distribution grids increasingly use higher levels of monitoring and automation, both dependent on grid topology. However, the total amount of information to adequately describe power grids is vast and needs to be reduced when used locally.

This work presents an approach for reducing and assembling power grid topologies in a decentralized way, such that full details of the local grid neighborhood are preserved, while remote areas get reduced in detail. Full connectivity information is retained.

Practical evaluation is performed on a modified version of the 906-bus IEEE European low-voltage test feeder, augmented with additional lines which introduce loops. The resulting size is 0.067 % of the full matrix for a subarea size of 66 buses.

Index Terms—Common Information Model, Information Management, Power System Operation, Smart grids, Topology

I. INTRODUCTION

A variety of factors are driving the transformation of electricity grids towards decentralization of production, increased levels of renewable generation and the inclusion of controllable demand side resources into the operation of the grid. This creates an increasingly complex power system together with the need to coordinate a large number of energy resources; raising the level of automation in the grid is seen as key to meeting this challenge. Various concepts for a more decentralized approach to grid control have been proposed, e.g. [1], [2], [3], [4], deviating from the traditional concept of centralized energy management by delegating some control tasks to embedded controllers in the field. One of the technical challenges common to these approaches is the need to provide the decentralized controllers with relevant grid state information, including information about the current grid topology and connectivity.

However, the total amount of information required to represent the detailed topology of an entire power system is vast; significant bandwidth and processing capacity would be required to replicate and synchronize the complete information for each decentralized controller in real time. It would be desirable for a practical implementation to reduce the information such that certain features of interest are retained in full detail while the rest of the topology is being simplified.

Reduction techniques are generally employed whenever the complexity of a model is either too high for its intended purpose, or would render the targeted problem infeasible.

In [5], the dynamic model of power system components is reduced while retaining the dynamic response and number of inputs and outputs. Topological reduction for printed ciruit boards is performed in [6], where only the low frequency response is of interest. Common approaches for reducing topological complexity in the field of power engineering are Kron reduction, Ward external equivalents, Dimo's method, and Zhukov's method [7], [8], [9]. They are widely applied for various types of power system analyses of large, interconnected areas. While each of these methods serves a different purpose, they all focus on the electrical aspects of grids but do not take logical grouping into account.

In this work we present an approach for reducing and assembling topology and binary connectivity information for a power grid. The reduction algorithm retains the logical grouping of buses into pre-defined areas and preserves information about the overall hierarchy of the grid, such that the reduced topology of each area contains complete information of the grid layout inside the area but progressively decreases the level of detail of grid sections at other levels of the hierarchy. Physical connectivity information between areas remains intact. By using a global naming scheme, the computation of reduced area representations as well as the assembly of the reduced global topology can be performed in a decentralized manner.

This work is structured as follows: Section II elaborates on the applications which motivate the presented approach. Section III describes the grid model and the topology reduction and assembly algorithm. In Section IV numerical performance evaluations of the algorithm are performed. Section V tests the algorithm against the IEEE European low-voltage feeder. Section VI discusses the question of information modelling, and finally, Section VII concludes the findings and gives an outlook on future developments.

II. NEW USES OF TOPOLOGY DATA

Topological data is extensively used in modern power grid operation and management systems, for example for monitoring, planning, and decision support [10]. However, these current use cases all assume a single point at which topology data is collected and consumed, such as the central topology database of a SCADA/EMS system. This architecture works well if all operational and management functions which

require topology data are centralized as well and physically colocated with the database. In recent years, many types of control architectures have been proposed which deviate from the classical, centralized model in order to enable a higher level of automation in the grid and in order to handle the resulting increase in complexity. These approaches include hierarchical systems - for example for coordinating ancillary service provision from DERs between voltage levels [2] or between individual DER units [1] - as well as control systems based on a peer-to-peer architecture, for example for voltage stabilization [3] or loss minimization [4]. Common to all of these approaches is that they require topology and connectivity information across the whole architecture, i.e. at multiple points of the system, in order to maintain coordinated operation of the distributed resources: If topology changes, be it due to a fault or due to system optimization, connects two DER units to the same electrical feeder, the coordination of their actions must reflect this fact. As an example, it must be known whether a PV inverter, whose reactive power injection is used to provide voltage stabilization in a distribution feeder, is actually connected to the feeder in question at the time of service delivery, instead of to a neighbouring one. On the other hand, many local controllers would primarily require the detailed topology of the grid in their immediate vicinity; details in remote parts of the grid could be lumped together by an adequate reduction algorithm such as the method proposed in this paper. This would drastically reduce the amount of data to be exchanged and the processing time required locally.

A. ELECTRA Web-of-Cells

In the ELECTRA project, innovative control schemes are being investigated in order to assess whether conventional frequency and voltage control approaches are suitable, or which aspects need to be revised for scenarios with massive amounts of small-scale DER [11]. The ELECTRA approach is based on a web of subsystems called cells which are operated autonomously and similarly to present control areas. A cell can be defined as a group of interconnected generation, load and storage, all within well-defined grid boundaries corresponding to a physical section of the grid. Neighboring cells are connected via tie-lines [12].

The proposed method can be used to detect undesired loop flows between cells due to differences between commercial schedules and physical power flows. Power flows along unexpected paths could occur due to open links within certain cells. Utilizing reduced topology data enables local reasoning over all flows in the grid to detect undesired loop flows.

III. METHOD

This section provides the mathematical background for the proposed approach. Starting from a general grid model which introduces the topological elements, the reduction process and assembly of the reduced topology are elaborated subsequently.

A. Grid Modeling

We consider a generic distribution grid topology as shown in Fig. 1a with buses, lines/cables, breakers/switches, areas, and

a unique naming scheme for all topological elements. This model holds the complete static physical structure. The effective topology is shown in Fig. 1b, which considers dynamic breaker states and is described in a graph structure [8].

Starting point for all further considerations is the oriented graph $G = (V, E)$, with V being vertices/nodes and E edges, and $n = \aleph(V)$, $m = \aleph(E)$ as their respective cardinalities. The incidence matrix of G is an $n \times m$ matrix defined as

$$
I_{i,j} = \begin{cases} -1: & v_i \text{ is the source of } e_j \\ 1: & v_i \text{ is the sink of } e_j \\ 0: & v_i, e_j \text{ are not incident,} \end{cases} \tag{1}
$$

with $v_i \in V$ and $e_j \in E$.

The graph $T_{\text{full}} = (B_{\text{full}}, L_{\text{full}})$ represents our global distribution grid topology, where B_{full} is the set of vertices representing buses, L_{full} is the set of edges representing closed lines between buses, and $n_{\text{full}} = \aleph(B_{\text{full}})$, $m_{\text{full}} = \aleph(L_{\text{full}})$ are the respective element numbers. The dimension of the incidence matrix calculates to:

$$
\text{Dim}(I_{\text{full}}) = n_{\text{full}} \times m_{\text{full}}. \tag{2}
$$

While an undirected graph would be sufficient to describe the connectivity state of an electric power system, we need the orientation of lines in order to properly attribute RDF information to the two terminals (see Section VI).

In order to give a reference frame in which the topology reduction and assembly process is conducted, a hierarchical ordering of the grid topology into defined areas A is assumed. The hierarchical level l is determined by the number of subindices. For example, A is the set of areas on the topmost level $l = 0$, A_i is the set of areas on the first level $l = 1$ for one area i, and so on. We call A_i a subarea of $A = \{A_1, A_2, \ldots\}$, $A_{i,j}$ a subarea of $A_i = \{A_{i,1}, A_{i,2}, \ldots\}$, i.e. $A \supseteq A_i \supseteq A_{i,j}$. For the sake of simplicity, we focus only on two levels and assume that each of the $r = \aleph(A)$ areas A_i has $r_i = \aleph(A_i)$ areas $A_{i,j}$, and $r_{i,j} = \aleph(A_{i,j}) = \emptyset$.
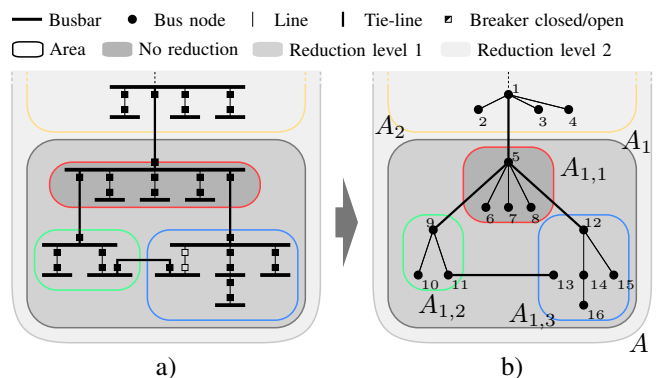

Fig. 1. Considered grid model and its components in an exemplary topology. The node/breaker model in (a) shows the complete physical model. The bus/branch model in (b) features the effective electric topology as a set of nodes and edges. Buses are hierarchically grouped into areas (colored), and the desired reduction levels are marked for area $A_{i,j}$ (shades of gray).

To the hierarchy level of $A_{i,j}$ belongs the subset $B_{i,j}$ of the complete set of buses B_{full}, and the smallest possible area corresponds to a single bus node. Each bus $b \in B_{\text{full}}$ belongs to one and only one area $A_{i,j}$, hence $B_{i,j} \cap B_{i,k} = \emptyset$ and $\bigcup_{i,j} B_{i,j} = B_{\text{full}}$ for $\forall i \in \{1 \ldots r\}$ and $\forall j, k \in \{1 \ldots r_i\}$, $j \neq k$. The hierarchy level of $A_{i,j}$ also contains domestic lines $L_{i,j}$, which connect the buses $B_{i,j}$, and the tie-lines $L_{\text{tie},i,j}$ each belonging to just one bus in $B_{i,j}$ because their respective other ends cross the area boundaries. Concordantly, A_i has the domestic lines L_i connecting the areas $A_{i,j}$ and the tie-lines $L_{\text{tie},i}$, and A features the domestic lines L and tie-lines L_{tie}. The last set contains all tie-lines that leave the observed grid and is empty for a closed topology. The corresponding graphs of each area on all levels contains the according buses/subareas and domestic lines, e.g., $T_{i,j} = (B_{i,j}, L_{i,j})$.

B. Topology Reduction

Using the grid model given in the previous section, the reduction is performed locally and entirely decentralized by all areas. The reduction process starts at the lowest level, where the set of connected topology segments $C_{i,j}$ of area $A_{i,j}$, $\forall i,j$ is determined. Each connected segment $c \in C_{i,j}$ is disjoint with the other segments within the area, i.e. there are no connecting lines between them, hence $c_a \cap c_b = \{\}$, $\forall a, b \in \{1 \ldots r_{i,j}^c\}$, $a \neq b$, and $r_{i,j}^c = \aleph(C_{i,j})$. The reduced area $A_{i,j}^{\text{red}}$ is formed by a new set of equivalent buses $B_{i,j}^{\text{equ}}$ each corresponding to one $c \in C_{i,j}$, and the tie-lines $L_{\text{tie},i,j}$. Thus, $A_{i,j}^{\text{red}}$ maintains the full connectivity information between its tie-lines $L_{\text{tie},i,j}$ without exposing its inner structure. The reduced topologies of all areas $\bigcup_j A_{i,j}^{\text{red}}$ are subsequently propagated upwards in the hierarchy to A_i, which are then reduced to A_i^{red} with B_i^{equ} and $L_{\text{tie},i}$ accordingly. The process finishes on the topmost level after reducing $\bigcup_i A_i^{\text{red}}$ into A^{red} with B^{equ} and L_{tie}.

C. Reduced Topology Assembly

The reduced global graph $T_{i,j}^{\text{red}} = (B_{i,j}^{\text{red}}, L_{i,j}^{\text{red}})$ as viewed from on area $A_{i,j}$ is then obtained by collecting and assembling all the topological information from the different levels across the hierarchy levels:

1) The complete local topology;
2) The reduced topology of the areas $A_{i,k}$, $\forall k \neq j$ within hierarchy level 2;
3) The reduced topology of the areas A_k, $\forall k \neq i$ within hierarchy level 1.

The resulting reduced global topology $A_{i,j}^{\text{glob}}$ for area $A_{i,j}$ consists therefore of

$$
\begin{aligned}
B_{i,j}^{\text{red}} &= B_{i,j} \cup \left(\bigcup_{k \neq j} B_{i,k}^{\text{equ}} \right) \cup \left(\bigcup_{k \neq i} B_k^{\text{equ}} \right), \\
L_{i,j}^{\text{red}} &= L_{i,j} \cup L_{\text{tie},i,j} \cup \left(\bigcup_{k \neq i} (L_k \cup L_{\text{tie},k}) \right) \cup L,
\end{aligned}
\tag{3}
$$

with the cardinalities $n_{i,j}^{\text{red}} = \aleph(B_{i,j}^{\text{red}})$, $n_{i,j} = \aleph(B_{i,j})$, $m_{i,j}^{\text{red}} = \aleph(L_{i,j}^{\text{red}})$, and $m_{i,j} = \aleph(L_{i,j})$. The total number of

equivalent buses and lines is therefore $n_{i,j}^{\text{equ}} = n_{i,j}^{\text{red}} - n_{i,j}$ and $m_{i,j}^{\text{equ}} = m_{i,j}^{\text{red}} - m_{i,j}$. These numbers are finally used to calculate the dimensions of the incidence matrix $I_{\text{red},i,j}$ of the reduced global topology for area $A_{i,j}$:

$$
\text{Dim}(I_{\text{red},i,j}) = (n_{i,j} + n_{i,j}^{\text{equ}}) \times (m_{i,j} + m_{i,j}^{\text{equ}}). \tag{4}
$$

For numerical investigations of the matrix in the following section, rows and columns are split into original and equivalent buses and lines. Assuming $n_{i,j}, n_{i,j}^{\text{equ}} \ll n$ and $m_{i,j}, m_{i,j}^{\text{equ}} \ll m$ for typical power grids, the reduction gain is apparent.

D. Example

Here we demonstrate the application of the algorithm on the exemplary bus/branch model in Fig. 1b. It consists of 16 buses, 15 lines, the top level area A, two areas A_1, A_2 on the first hierarchy level, and three areas $A_{1,1}$, $A_{1,2}$, $A_{1,3}$ on the second hierarchy level within A_1. The incidence matrix size of the complete topology is $16 \cdot 15 = 240$ according to (2).

Table I shows both the full and the reduced incidence matrices for all areas that hold buses. Three of these areas only contain one equivalent bus (labeled with *eq*) which all tie-lines connect to. Area $A_{1,3}$, however, has two electrically disjoint grid segments and just as many equivalent buses.

Using these matrices, the reduced global topology can be constructed for any area as demonstrated on $A_{1,1}^{\text{red}}$ in Table IIa. The size of the reduced incidence matrix is only $8 \cdot 7 = 56$, which is 23 % of the full matrix. Table IIb demonstrates the construction of the reduced incidence matrix A_1^{red} from its subareas. The process is completely decentralized, as the reduced topologies are communicated upwards in the hierarchy where they are assembled and reduced.

TABLE I
FULL AND REDUCED TOPOLOGIES OF THE EXAMPLE GRID IN FIG. 1.

IV. NUMERICAL PERFORMANCE EVALUATION

Numerical evaluations with reasonable assumptions for the number of buses, lines, areas and connected sub-areas from the perspective of one area $A_{i,j}$ are performed in the following.

We introduce the function f_{mesh} that linearly interpolates between a radial graph with $n - 1$ edges and a fully meshed graph with $\frac{1}{2}n(n-1)$ edges using the mesh factor $x \in [0, 1]$, resulting in the total number of edges in a graph with n nodes:

$$
f_{\text{mesh}}(n, x) = (n - 1)\left(\left(\frac{n}{2} - 1\right)x + 1\right). \tag{5}
$$

a)

$A_{1,1}^{\text{glob}}$	1-5	5-6	5-7	5-8	5-9	5-12	11-13
5	1	-1	-1	-1	-1	-1	0
6	0	1	0	0	0	0	0
7	0	0	1	0	0	0	0
8	0	0	0	1	0	0	0
121eq	0	0	0	0	1	0	-1
131eq	0	0	0	0	0	0	1
132eq	0	0	0	0	0	1	0
21eq	-1	0	0	0	0	0	0

b)

$A_{1,1}$	1-5	5-9	5-12	11-13
111eq	1	-1	-1	0
121eq	0	1	0	-1
131eq	0	0	1	0
132eq	0	0	0	1

⇓

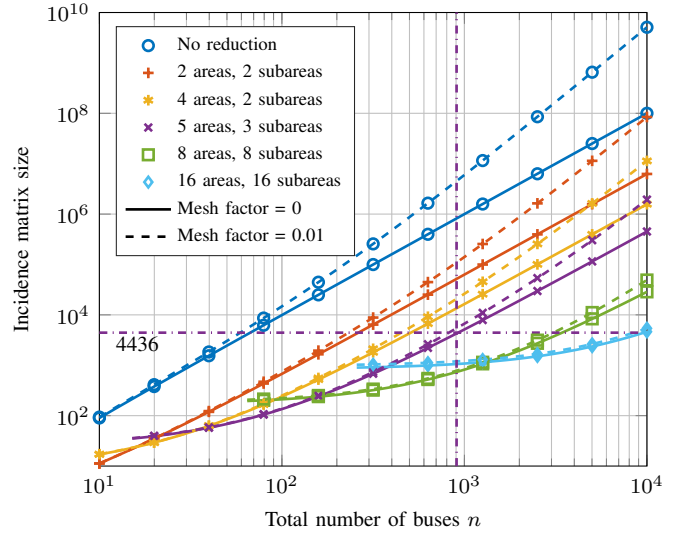| A_1^{red}	1-5
11eq	1

Fig. 2. Numerical performance evaluation of the reduction algorithm different numbers of areas and mesh factors. The vertical and horizontal dash-dotted lines mark the average reduced incidence matrix size per subarea for the total number of buses in the test case discussed in Section V-B.

The next step is to define the variables in (4) based on the arbitrarily chosen total number of buses n, the number of areas r_l in each area level $l \in \{1,2\}$, and the average number of connected grid segments in each area $\bar{r}^c$:

$$n_{i,j} = n \prod_{k=1}^{l} r_k^{-1},$$

$$n_{i,j}^{\text{equ}} = \bar{r}^c \sum_{k=1}^{l} (r_k - 1), \qquad (6)$$

$$m_{i,j} = f_{\text{mesh}}(n_{i,j}, x),$$

$$m_{i,j}^{\text{equ}} = f_{\text{mesh}}(n_{i,j}^{\text{equ}}, x).$$

Here, the number of buses $n_{i,j}$ in the area is the total number of buses divided by the total number areas on the lowest level. For the evaluation of the number of equivalent buses $n_{i,j}^{\text{equ}}$ one area less needs to be taken into account on each hierarchical level (e.g., if an area level has three subareas, only two need to be replaced by equivalent buses because our considerations are performed from the perspective of the third subarea). The number of lines $m_{i,j}$ and $m_{i,j}^{\text{equ}}$ is calculated from (5).

Fig. 2 shows the numerical evaluation results of the incidence matrix dimension $\text{Dim}(I)$ depending on the total number of buses n for variations of the number of areas r and the mesh factor x. Two hierarchy levels l are considered for all areas. The number of connected grid segments per area is uniformly chosen as $\bar{r}^c = 1$, as its influence on the figures is small compared to the other quantities. Only results fulfilling the condition $n_{i,j} \geq 1$ of (6) are plotted.

In the case of the full incidence matrix without reduction and $x = 0$, we observe the expected n^2 growth using (2). Applying a mesh factor of only 1% increases the size remarkably. For $n = 10^4$ the number of matrix entries based on (4) changes from about 10^8 to about $5 \cdot 10^9$, indicating that increased computational demands of potential future meshed grid configurations can be expected.

Dividing the grid into two areas and two subareas each yields a significant size reduction of a factor of around 10 across the range. By increasing the number of areas and subareas in the last case, the gain in size becomes more pronounced and accounts for more than 4 orders of magnitude and 10^4 buses. The dependency between the total and the reduced number of buses is non-linear, because for small n and high r the total amount of areas dominates the result. In the opposite case of high n and low r, however, the incidence matrix size is mostly proportional to the square of the number of buses per subarea $n_{i,j}$. For the case of 5 areas and 3 subareas, the average reduced incidence matrix size per subarea is marked by the vertical and horizontal dash-dotted lines as a reference for the test case discussed in the next section. Here, the evaluation predicts an average incidence matrix size of 4436 entries, which is 0.05% of the full incidence matrix with 819930 entries.

V. PRACTICAL ASSESSMENT

In this section we apply the algorithm on a modified version of the IEEE European low-voltage (LV) test feeder. Starting from the area partitioning process, the topology reduction and assembly process is then exemplified step by step.

A. Random Partitioning

Areas are assigned automatically by applying Algorithm 1 which randomly splits the input topology into an arbitrary number of areas r, where the function $\text{ConnectedAreas}(T)$ determines the sets of connected buses forming these areas. The algorithm terminates when the number of desired areas r is reached. A radial topology must be provided to the algorithm; meshed topologies can be processed by adding the remaining lines after performing the random partitioning on a spanning tree.

The algorithm creates areas with a certain minimal number of buses $n_{\min}$ depending on the total number of buses n and areas r in order to achieve balanced area sizes. The choice of $n_{\min} = \text{ceil}\left(\frac{n}{2r}\right)$ ensures that the algorithm will always terminate for $1 < r < \text{floor}\left(\frac{n}{2}\right)$. Here, $\text{ceil}(\cdot)$ and $\text{floor}(\cdot)$

return the next higher respectively lower integers of the real-valued input arguments. Recursive application on the resulting areas allows for hierarchical splitting of the topology into the desired number of hierarchy levels.

Algorithm 1 Random partitioning algorithm.

Require: Radial topology graph $T = (B, L)$
Require: Desired number of areas $1 < r < \text{floor}\left(\frac{n}{2}\right)$
  function CREATERANDOMAREAS(T, r)
    $n \leftarrow \aleph(B)$
    $n_{\min} \leftarrow \text{ceil}\left(\frac{n}{2r}\right)$
    $L_{\text{sel}} \leftarrow L$
    $L_{\text{tie}} \leftarrow \emptyset$
    $A \leftarrow \emptyset$
    repeat
      repeat
        $l_{\text{cut}} \leftarrow \text{rand}(L_{\text{sel}})$
        $L_{\text{temp}} \leftarrow L_{\text{sel}} \setminus l_{\text{cut}}$
        $T_{\text{temp}} \leftarrow (B, L_{\text{temp}})$
        $C \leftarrow \text{CONNECTEDAREAS}(T_{\text{temp}})$
      until $\aleph(c) \geq n_{\min}, \forall c \in C$
      $L_{\text{sel}} \leftarrow L_{\text{temp}}$
      $L_{\text{tie}} \leftarrow L_{\text{tie}} \cup l_{\text{cut}}$
    until $\aleph(C) = r$
    for all $c \in C$ **do**
      $A \leftarrow A \cup (c, L)$
    end for
    return A
  end function

B. IEEE LV grid

The IEEE European Low-Voltage Test Feeder is a 906 bus radial distribution grid which connects to the medium-voltage system through a substation transformer [13]. For studying the behavior of the reduction algorithm in meshed grids, new lines were added to the original topology. Also, some existing lines were removed in order to break areas into disconnected grid segments. The list of modifications is given in Table III.

TABLE III
LINE MODIFICATIONS TO THE IEEE EUROPEAN LV TEST FEEDER.

Bus 1	Bus 2	Added	Removed
1	70	✓	
196	290	✓	
327	562	✓	
337	406	✓	
469	731	✓	
778	861	✓	
151	158		✓
686	691		✓

TABLE IV
COMPARISON OF THE MODIFIED IEEE EUROPEAN LV TEST FEEDER BEFORE AND AFTER PERFORMING TOPOLOGY REDUCTION FOR SUBAREA 1 OF AREA 1 IN FIG. 3A.

Quantity		Full	Reduced
# nodes	n	906	74
# lines	m	909	75
# Incidence matrix size	$\text{size}(I)$	823554	5550
# nodes in area	$n_{i,j}$	-	66
# lines in area	$m_{i,j}$	-	65

Fig. 3a shows the grid layout and the randomly created areas as described in Section V-A. Two hierarchy levels are generated, with the second level (subarea) only marked in area 1. The reduction levels from the local perspective of subarea 1 are shown in Fig. 3b. The dark gray zone marks the area of full topological resolution. Mid gray indicates the first reduction level which comprises all other subareas within area 1. The light gray zone includes the reduced topologies of all other areas but not subareas.

To generate the reduced global topology for subarea 1, all subareas perform the topology reduction as described in Section III-B. The parent level of each subarea assembles the reduced topologies according to Section III-C (only considering step 2) and performs another reduction. Subarea 1 then collects the reduced topologies of the subareas in area 1 as well as all other reduced topologies and merges them. As tie-lines between areas are kept, the resulting topology features the complete mesh information with gradually decreasing resolution for the areas.

Considering only the top-level areas in Fig. 3a, one could assume that area 1 and 4 form a loop, and areas 1, 3 and 5 form another. The reduced topology in Fig. 3c, however, shows that area 3 and 4 are internally split into separate grid segments. The assumption about area 4 is therefore wrong, and the assumption about the second loop is only true because it closes via area 2. Assembling the incidence matrices as described preserves the internal topology characteristics while keeping the total incidence matrix complexity low. Table IV compares the number of buses and lines along with the resulting matrix size before and after topology reduction for subarea 1 of area 1. The reduced matrix is 0.067% the size of the full matrix for a subarea size of 66 buses, which is the expected order of magnitude with respect to Section IV.

VI. INFORMATION MODELLING

One of the steps towards a practical implementation of the proposed method is the choice of an information model suitable to represent the data to be exchanged between grid areas or nodes. The Common Information Model (CIM) as defined by the IEC 61970 and IEC 61968 series of standards, has been established as the technical standard for the exchange of grid data between various utility systems. It provides a semantically and syntactically sound format for data exchange between SCADA, EMS, DMS, OTS and asset management systems. CIM is one of the most established standards worldwide in the energy domain, as its acceptance in the energy sector and the active standardization work is very high. CIM is an EMS-API standard containing a large data and information model for the energy domain which provides an integration framework including several technology mappings, interface specifications, as well as the data model [14].

CIM standardizes the exchange of messages among different stakeholders and provides the basis for modeling topologies of the power grid for both transmission and distribution grids. These topologies can then be serialized in the Resource Description Format (RDF) in order to facilitate data exchange.
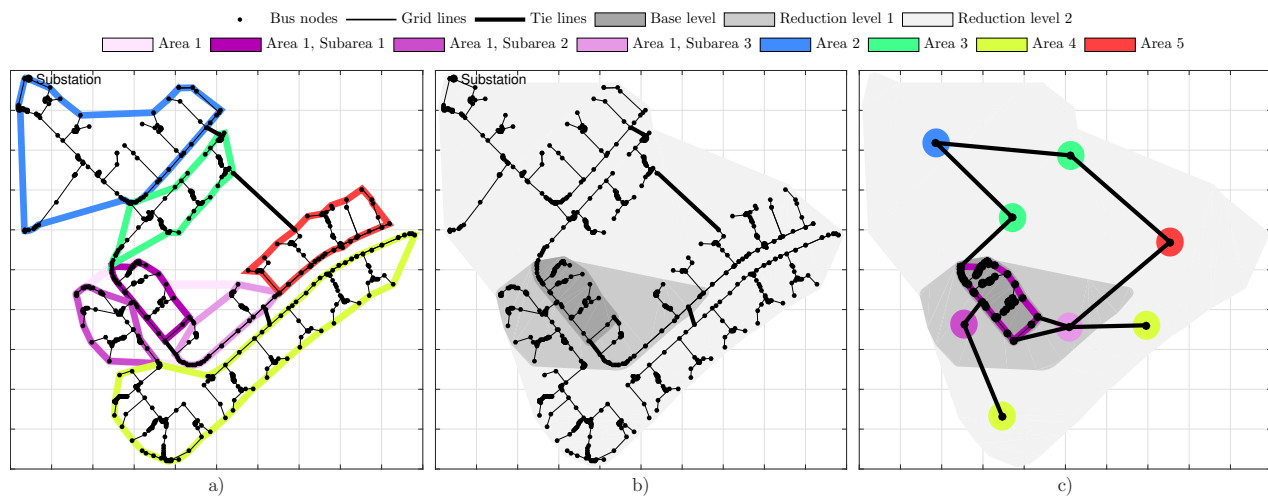
Fig. 3. Exemplary reduction of the modified IEEE European low voltage test feeder. The topology with its pre-defined areas and subareas is shown in (a). The desired reduction levels for subarea 1 of area 1 are marked in (b). The reduced global topology as seen from the subarea is shown in (c).

The use of RDF as a serialization format for CIM is of interest to the proposed method, since it allows the representation of arbitrary topology graphs, including cyclic graphs. This enables CIM/RDF to represent the reduced topologies within the same framework as the full topology.

An additional question concerns the representation of reduced topologies by CIM classes, ideally without having to extend the existing class hierarchy. One interesting possibility is to use the *equivalentLoad* class which can be used to represent the reduced grids. Based on the CIM UUID mechanism, complete global topologies could be resolved as well.

VII. Conclusions & Outlook

The approach presented in this work enables significant reduction of the binary connectivity information of electric distribution grid topologies. The reduction is sufficient for the targeted applications in the ELECTRA project, where global topology representations are desirable but not feasible to implement without reduction. Numerical investigations of the algorithm performance show that optimal reduction is achieved by the right choice of numbers of areas with respect to the total number of buses. This knowledge may provide a starting point for grid partitioning.

Future work will focus on decreasing the communication overhead of the reduced incidence matrices in order to facilitate practical applicability, possibly using difference/delta updates. Secondly, the algorithm will be extended by augmenting the binary connectivity with equivalent electrical impedances. Using existing electric reduction approaches such as Kron's Reduction or Dimo's Method, the combined approach will allow for the deduction of a reduced global electrical topology that is generated and assembled in a decentralized way.

Acknowledgement

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