Analysis of Drain-Induced Barrier Rising in Short-Channel Negative Capacitance FETs and Its Applications

Junbeom Seo, Jaehyun Lee, and Mincheol Shin

***Abstract*—We investigate the performance of hysteresis-free short-channel negative-capacitance field-effect transistors (NCFETs) by combining quantum mechanical calculations with the Landau-Khalatnikov equation. When the subthreshold swing (SS) becomes smaller than 60 mV/dec, a negative value of drain-induced barrier lowering (DIBL) is obtained. This behavior, drain-induced barrier rising (DIBR), causes negative differential resistance (NDR) in the output characteristics of NCFETs. We also examine the performance of an inverter composed of hysteresis-free NCFETs to assess the effects of DIBR at the circuit level. Contrary to our expectation, although hysteresis-free NCFETs are used, hysteresis behavior is observed in the transfer properties of the inverter. Furthermore, it is expected that the NCFET inverter with hysteresis behavior can be used as a Schmitt trigger inverter.**

***Index Terms*—Subthreshold swing, ferroelectric, negative capacitance FET, hysteresis behavior, drain-induced barrier lowering, Schmitt trigger inverter**

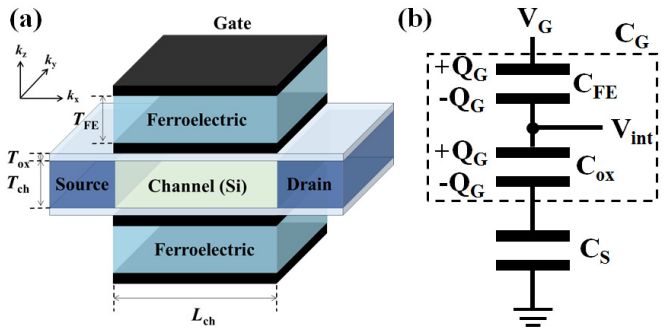

Fig. 1. (a) Schematic structure of the UTB NCFET and (b) a series of ferroelectric (C_{FE}), dielectric (C_{ox}), and semiconductor capacitors (C_s). The gate capacitance (C_G) is modeled as a series capacitance of C_{FE} and C_{ox}.

I. Introduction

As conventional metal-oxide-semiconductor field-effect-transistors (MOSFETs) are reduced to a nanometer scale, the subthreshold swing (SS) reaches the fundamental thermal limit of 60 mV/dec [1]. It is well-known that this limitation is an obstacle to achieving high-performance and low-power consumption devices. To solve this issue, new device concepts, such as impact ionization MOS (I-MOS) [2] and tunneling FETs (TFETs) [3] have been suggested. Despite their outstanding features, I-MOS suffers from reliability issues and is not suitable for low-power consumption devices because of their high applied voltages. In the case of TFETs, ON-state current (I_{ON}) is restricted due to tunneling probability, even though sub-60 mV/dec switching behavior occurs [3]-[6].

In recent years, negative capacitance FETs (NCFETs), proposed by Salahuddin *et al.* [7], have received much attention as a new type of steep switching device. NCFETs are capable of achieving steep SS and high I_{ON} by amplification of the gate voltage (V_{GS}) through the ferroelectric material. Unlike I-MOS and TFETs, the I_{ON} of NCFETs strongly depends on the thermionic currents. According to recent experimental studies on NCFETs, they have successfully achieved very steep SS values of 18 and 11.3 mV/dec as well as a high ON/OFF current ratio with low drain volgate (V_{DS}) [8]-[10].

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There has been growing interest in the evaluation and optimization of NCFETs. Kobayashi *et al.* [11] suggested exploiting the ferroelectric properties to design low-power NCFETs. The dependences of NCFET performances on ferroelectric thickness (T_{FE}) have been studied extensively [12]-[16]. Khan *et al.* [17] provided guidelines for parameters to develop low-power NCFETs. Since NCFETs are based on conventional MOSFETs, they may be vulnerable to short-channel effects (SCEs). Recently, Li *et al.* [18] pointed out the coupling effects between gate and drain on the device performance of short-channel bulk NCFETs. Except for Li's work, SCEs on NCFETs have never been reported.

In this work, we investigated the performance of short-channel NCFETs through quantum mechanical simulations with the Landau-Khalatnikov (LK) equation. We especially focused our attention on the SCEs associated with V_{DS} and drain-induced barrier lowering (DIBL). Furthermore, we explored the influence of SCEs on the inverter to verify the viability of NCFETs at the circuit level.

The remainder of this paper is organized as follows. Section II describes our simulation approach based on the LK theory and quantum transport. In Section III, the basic properties of NCFETs are presented focusing on the SCEs. We discuss the characteristics of the NCFET inverter and propose a new application in Section IV, followed by a summary and conclusions in Section V.

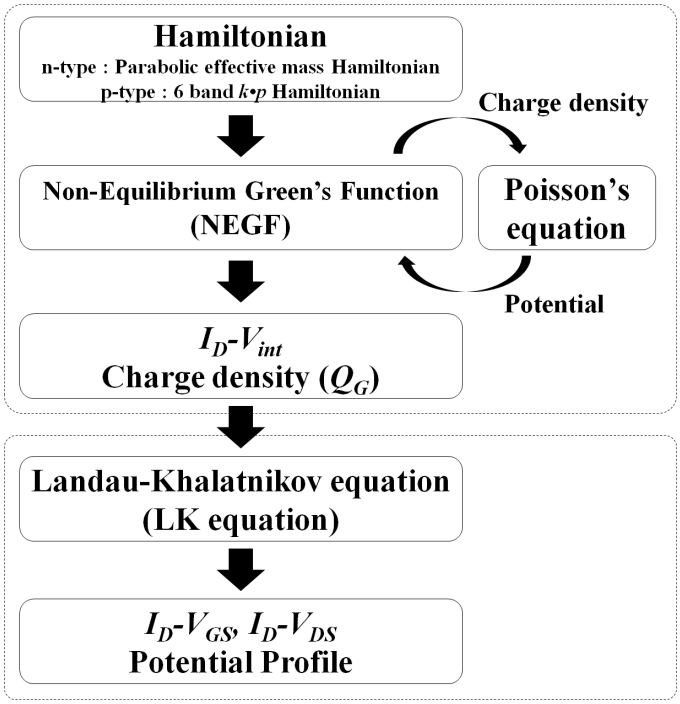

Fig. 2. Flowchart of the NCFET simulation.

II. Simulation approach

A schematic diagram of the ultra-thin body (UTB) double-gate (DG) NCFETs simulated in this work is shown in Fig. 1(a). The key difference between the structure of NCFETs and conventional MOSFETs is the presence of a ferroelectric material in the gate stack. As in the case of recent experiments [8][9], the ferroelectric and baseline MOSFET in our work are supposed to be spatially separated, but connected by a metal layer with the same contact area, which provides the same gate charge density (Q_G) to both the internal gate and ferroelectric surfaces. The channel length (L_{ch}) and T_{FE} are subject to variation, whereas the channel thickness (T_{Si}) and equivalent oxide thickness (EOT) are assumed to be 5 and 2 nm, respectively.

Fig. 1(b) describes the equivalent capacitance model. An NCFET can be depicted with three capacitances, including ferroelectric, dielectric, and semiconductor capacitors. The total gate capacitance (C_G) consists of a series combination of oxide (C_{ox}) and ferroelectric (C_{FE}) capacitances. The internal voltage (V_{int}) indicates the voltage amplified by the ferroelectric, and it acts as V_{GS} in the conventional MOSFET.

The overall simulation procedure shown in Fig. 2 consists of two parts: electronic calculation and ferroelectric capacitor modeling.

First, we solve the non-equilibrium Greens function (NEGF) and Poisson equation self-consistently in the ballistic transport regime for the conventional MOSFET with the same dimensions as those of NCFETs [19]. In the channel region, the effective mass Hamiltonian and 6 bands $k \cdot p$ Hamiltonian for n-type and p-type devices are used to describe the conduction and valence bands, respectively. The effective masses are calibrated from the $sp^3d^5s^*$ tight-binding method [20]. The Luttinger parameters are adjusted from the sp^3s^* tight-binding method [21]. From the self-consistent calculation, we obtain Q_G and drain current (I_D) as a function of V_{GS}.

Next, the ferroelectric capacitor is modeled as follows. The LK equation [22][23] which describes the dynamics of polarization in response to time is given as

$$\rho \frac{dP}{dt} + \nabla_{\vec{P}} U = 0, \tag{1}$$

where ρ, P, and t are resistivity, polarization, and time, respectively. Here, U represents the free energy of the ferroelectric material and is defined by the Landau-Devonshire (LD) theory [24] as

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - \vec{E} \cdot \vec{P}, \tag{2}$$

where E is an external electric field and α, β, and γ are the order parameters. In the case of the ferroelectric material, α is always negative. In this work, the ferroelectric material is assumed to be $SrTiO_3$ with the parameters of $\alpha = -6.5 \times 10^7$ m/F , $\beta = 3.75 \times 10^9$ m^5/F/C^2, and γ = 0 m^9/F/C^4 [25]. We note that the use of bulk order parameters in this work may be justified considering the supposed spatial separation between the ferroelectric and baseline MOSFET. However, in an ultimate integration of ferroelectric into the gate stack, the size of ferroelectric should affect the ferroelectricity [26]-[28] and thus leads to different order parameters than the bulk ones. We nevertheless believe that the overall trend as predicted from the results of this work might not change in nature.

We assume that the ferroelectric is in steady-state polarization ($dP/dt = 0$). Substituting Eq. (2) into Eq. (1), the electric field is given as

$$E = 2\alpha P + 4\beta P^3, \tag{3}$$

which can be further derived as

$$V_{int} = V_{GS} - [2\alpha P + 4\beta P^3] T_{FE}, \tag{4}$$

where V_{int}, V_{GS}, and T_{FE} are the internal voltage, gate bias, and ferroelectric thickness, respectively. Since Q_G can be expressed as $Q_G = P + \epsilon_0 E \approx P$ because P of the ferroelectric is larger than $\epsilon_0 E$, Eq. (4) is approximated as

$$V_{int} = V_{GS} - [2\alpha Q_G + 4\beta Q_G^3] T_{FE}. \tag{5}$$

Finally, the drain current at a particular gate voltage (V_{GS}^{NCFET}) in NCFETs, $I_D^{NCFET}(V_{GS}^{NCFET})$, is obtained by looking up the drain current in the conventional MOSFET which was precalculated in the previous step, $I_D^{MOSFET}(V_{GS})$, as follows:

$$I_D^{NCFET}(V_{GS}^{NCFET}) = I_D^{MOSFET}(V_{GS}),$$

where $V_{GS} = V_{int}(V_{GS}^{NCFET})$ as given by Eq. (5).

III. Characteristics of NCFET

A. Dependence on T_{FE}

Fig. 3 presents the transfer characteristics of conventional MOSFETs and NCFETs with L_{ch} = 20 nm, respectively. As T_{FE} increases, I_{ON} increases and SS decreases. For instance, NCFETs with T_{FE} = 270 nm provide larger I_{ON} (12.9 mA/μm) and lower SS (43.5 mV/dec) than conventional

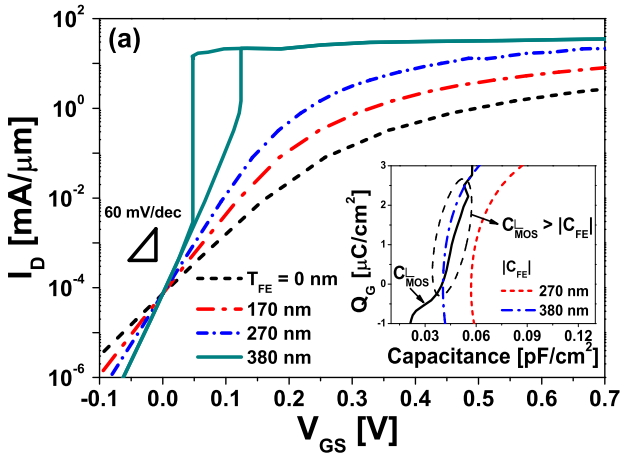

Fig. 3. Transfer characteristics of the conventional MOSFET (T_{FE} = 0 nm) and NCFETs with T_{FE} = 170, 270 and 380 nm. Inset shows Q_G versus the capacitance of NCFETs with T_{FE} = 270 and 380 nm.

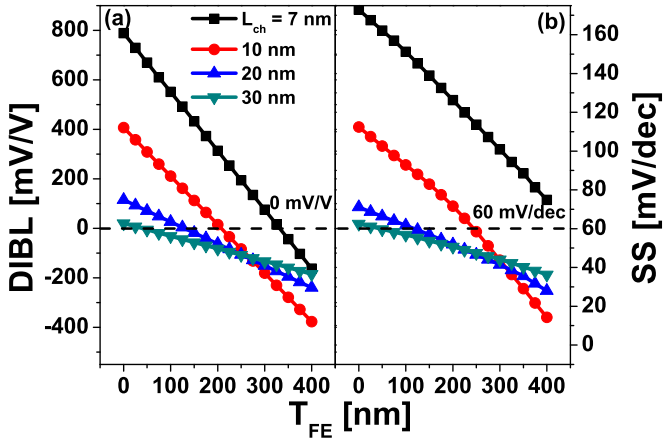

Fig. 4. (a) DIBL and (b) SS as a function of T_{FE} for L_{ch} = 7, 10, 20, and 30 nm.

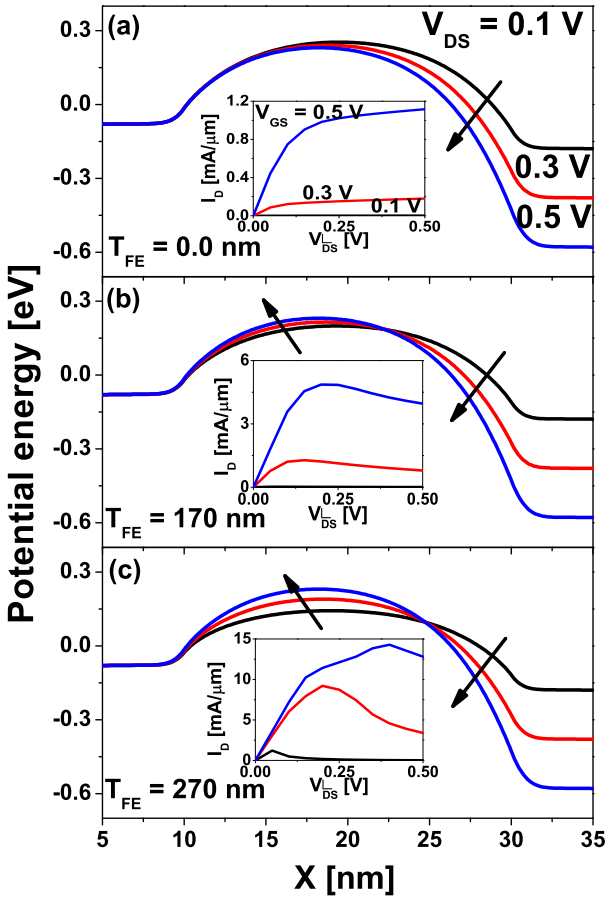

Fig. 5. Potential profile at V_{GS} = 0.0 V for (a) the conventional MOSFET and NCFETs with (b) T_{FE} = 170 and (c) 270 nm. Insets show the output characteristics of each device.

MOSFETs (1.1 mA/μm and 71.5 mV/dec). However, in the case of NCFETs with T_{FE} = 380 nm, the hysteresis behavior is observed. Inset of Fig. 3 shows the MOS capacitance (C_{MOS}) and C_{FE} as a function of Q_G for NCFETs with T_{FE} = 270 and 380 nm. For T_{FE} = 270 nm, C_G is positive in the all range of Q_G, because $|C_{FE}|$ is larger than C_{MOS}. For T_{FE} = 380 nm, on the other hand, $|C_{FE}| > C_{MOS}$ in a certain range of Q_G and so C_G becomes negative in the range only. In this condition, NCFETs become unstable, resulting in the hysteresis behavior [17]. Such a trade-off between high performance and hysteresis agrees well with previous results [12][17]. Since hysteresis behavior is not desirable, we consider only hysteresis-free NCFETs hereafter.

The dependence of DIBL and SS on T_{FE} is shown in Fig. 4. Regardless of the hysteresis behavior, we can extract SS and DIBL for the forward sweep. SS is defined as the minimum inverse slope near threshold voltage (V_{th}), which is defined as the gate voltage at which I_D = 0.1 μA/μm for the forward sweep. It is interesting to note that in the cases of devices with L_{ch} = 20 and 30 nm, DIBL has a value of 0 mV/V when SS becomes 60 mV/dec. This behavior can be explained by the fundamental semiconductor theory as follows. First, SS is defined as

$$SS = \frac{dV_{GS}}{dlog_{10}I_D} = \frac{dV_{GS}}{d\phi_s}\frac{d\phi_s}{dlog_{10}I_D} = (1+\frac{C_s}{C_G})\times\frac{k_BT}{q}ln10, \quad (6)$$

where ϕ_s, k_B, T, and q are the surface potential, Boltzmann constant, temperature, and electronic charge, respectively. Secondly, DIBL is expressed as

$$DIBL = \frac{V_{th}^{high} - V_{th}^{low}}{V_{DS}^{high} - V_{DS}^{low}}, \quad (7)$$

where $V_{th}^{low(high)}$is the threshold voltage at low (high) $V_{DS}^{low(high)}$. From the fundamental theory of bulk transistors, V_{th} is written as

$$V_{th} = \phi_{MS} + 2\phi_{bi} + \frac{Q_G}{C_G}, \quad (8)$$

where ϕ_{MS} is the work function difference between the gate metal and semiconductor and ϕ_{bi} is the built-in potential [29]. Assuming that ϕ_{MS} and ϕ_{bi} are not affected by the ferroelectric, V_{th} only depends on Q_G/C_G. That is, if the value

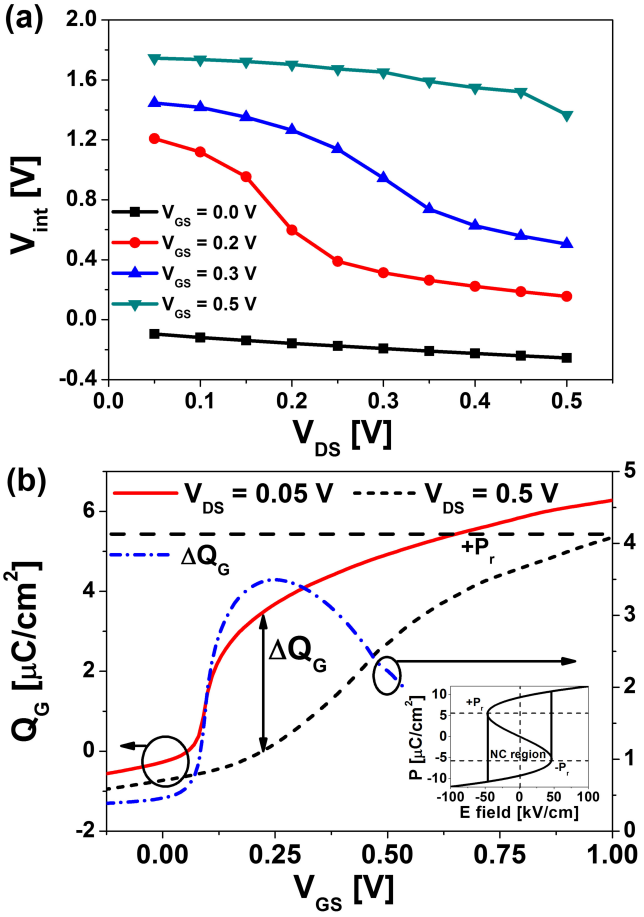

Fig. 6. (a) V_{int} versus V_{DS} for the n-type NCFETs with T_{FE} = 270 nm and (b) Q_G versus V_{GS}. Inset of (b) shows the polarization versus electric field for $SrTiO_3$, where the remanent polarization (P_r) and coercive electric field (E_c) are 5.2 μC/cm^2 and 46.6 kV/cm, respectively.

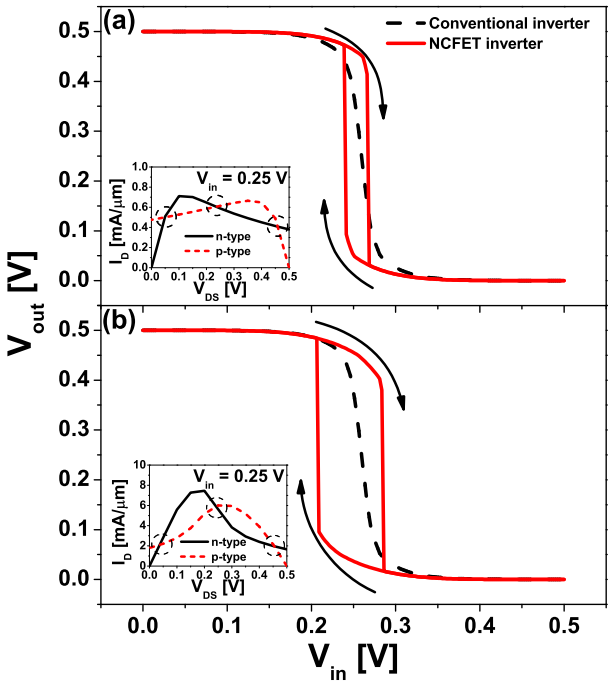

Fig. 7. Voltage transfer characteristics of the NCFET inverters with (a) T_{FE} = 170 (n-type) and 140 (p-type) nm and (b) T_{FE} = 270 (n-type) and 280 (p-type) nm. Dashed lines represent the voltage transfer characteristics of the conventional MOSFET. Insets show the road line of the n-type and p-type NCFETs at V_{in} = 0.25 V.

of C_G is very large (it can be infinite when $C_{ox} = -C_{FE}$ for NCFETs), DIBL becomes 0 mV/V. At the same time, the first term of SS, called the body factor, becomes 1, thus, SS becomes 60 mV/dec at room temperature.

When L_{ch} = 7 and 10 nm, we cannot find the specific T_{FE} to satisfy DIBL = 0 mV/V and SS = 60 mV/dec simultaneously. This is because, as L_{ch} decreases, the direct source-to-drain tunneling current increases. Thus, SS no longer can be described by Eq. 6. Therefore, when DIBL = 0 mV/V, SS $\neq$ 60 mV/dec in short-channel devices.

B. Drain-Induced Barrier Raising (DIBR)

In the previous subsection, we showed that when SS becomes less than 60mV/dec, DIBL has a negative value. This behavior is in good agreement with Li's work [18]. To investigate it in details, we first compare the potential profile in the channel region of conventional MOSFETs and NCFETs with T_{FE} = 170 and 270 nm, respectively, as shown in Fig. 5. Here, L_{ch} is assumed to be 20 nm for these devices. In the case of the conventional MOSFET, the potential barrier is lowered with increasing V_{DS}, which indicates a typical DIBL. However, NCFETs show the opposite trend, which we call drain-induced barrier rising (DIBR).

The V_{int} values of NCFETs are plotted as a function of V_{DS} with various V_{GS} values in Fig. 6(a). To exhibit DIBR clearly, T_{FE} and L_{ch} of NCFETs are assumed to be 270 and 20 nm, respectively. From Fig. 6(a), we can see that, as V_{DS} increases, V_{int} decreases. In particular, when V_{GS} = 0.2 V, V_{int} undergoes a steep variation. This behavior can be elucidated by Fig. 6(b) and Eq. (6). In this case, the NCFET is operated in the NC region because Q_G is less than remanent polarization (P_r) of 5.2 μC/cm^2, as seen in Fig. 6(b) and its inset. Due to the small Q_G in the NC region, the second term in Eq. (5) is more dominant than the third term. Moreover, Fig. 6(b) shows that Q_G for V_{DS} = 0.05 V is higher than that for V_{DS} = 0.5 V. As a consequence, Q_G reduction with increasing V_{DS} leads to a decrease in V_{int}, resulting in DIBR as seen in Fig. 5(b). In addition, variation in V_{int} with respect to V_{DS} is well in accordance with the change in Q_G, $\triangle Q_G (Q_G(V_{DS} = 0.05\ \text{V}) - Q_G(V_{DS} = 0.5\ \text{V})$.

As seen in the insets of Fig. 5(b) and (c), NCFETs show negative differential resistance (NDR) [16][30], which is a distinctive feature that is not seen in the conventional MOSFET. In a Gunn diode, known as a transferred-electron device, NDR is induced by the transition of electrons from a high-mobility valley to a low-mobility valley [31]. In the case of NCFETs, however, it occurs due to the reduction of current caused by DIBR. For instance, when T_{FE} = 270 nm, V_{int} is reduced from 1.45 to 0.5 V with increasing V_{DS} from 0.05 to 0.5 V as shown in Fig. 6(a), and NDR is induced as a consequence. Moreover, since DIBR is associated with C_{FE}, NDR can be controlled

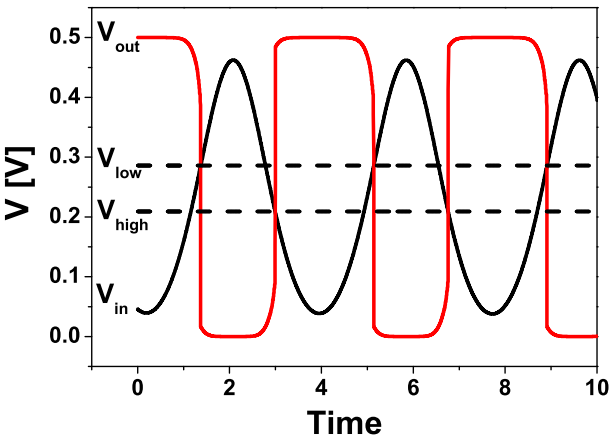

Fig. 8. Transient response of NCFET inverters with T_{FE} = 270 (n-type) and 280 (p-type) nm. $V_{in(out)}$ and $V_{low(high)}$ are input (output) signal and low (high) threshold voltage, respectively.

by T_{FE}. Despite NDR, NCFETs still deliver a larger current than the conventional MOSFET.

In recent experimental works where SS less than 60 mV/dec was achieved [9][32], DIBR and NDR behaviors were not observed. In [9], Q_G shows only a weak dependence on V_{DS} which makes DIBL more predominant than DIBR. In a different setting where Q_G becomes a stronger function of V_{DS}, we may expect appearance of both NDR and DIBR.

IV. NCFET INVERTERS

A. Voltage transfer characteristics of NCFET inverters

Fig. 7 shows the voltage transfer characteristic (VTC) of NCFET inverters. The VTC of NCFET inverters is extracted from cross points of n-type and p-type NCFET load curves at each V_{in}. Insets of Fig. 7 show the load lines of n-type and p-type NCFETs at V_{in} = 0.25 V. The T_{FE} values of n-type and p-type NCFETs without hystresis behavior are adjusted to have similar I_{ON}. As seen in this figure, however, unexpected hysteresis loops are observed. In common load lines of the conventional MOSFETs, there is a cross point for one input voltage, but in the case of NCFETs with NDR, two or three cross points are observed as shown in the insets. This induces the hysteresis behavior in VTC of NCFET inverters. The hysteresis loop can be modified by adjusting T_{FE}. In the case of NCFET inverters with T_{FE} = 170 (n-type) and 140 (p-type) nm as shown in Fig. 7, the hysteresis window (V_{hys}), low threshold (V_{low}), and high threshold (V_{high}) are 0.0198, 0.243, and 0.262 V, respectively. As the T_{FE} values of NCFETs become thicker, the hysteresis loop becomes more apparent due to stronger NDR; for example, in the NCFET inverter with T_{FE} = 270 (n-type) and 280 (p-type) nm, V_{hys}, V_{low}, and V_{high} become 0.0743, 0.272, and 0.332 V, respectively (See Fig. 7).

B. Schmitt trigger inverter

The transient response of NCFET inverters is shown in Fig. 8. The transient response of NCFET inverters is the same as that of the Schmitt trigger inverter described in [33] and [34]. The Schmitt trigger inverter, which consists of 4 to 6 MOSFETs, acts as a filter of noise and disturbance in an analog circuit, which exhibits hysteretic characteristics [33]-[35], while the NCFET Schmitt trigger inverters requires just two transistors. Further, since NCFETs outperform the conventional MOSFETs with regard to I_{ON} and SS, it is concluded that NCFET inverters are superior to conventional Schmitt trigger inverters. If one makes use of the hysteresis behavior of NCFETs as suggested in this work, it is expected that the application of NCFETs can be extended to functional circuits.

V. CONCLUSION

In this paper, we assessed the performance of UTB short-channel NCFETs by combining quantum-mechanical transport calculations with LD theory. Since C_G increases with T_{FE}, both SS and DIBL decrease due to strong gate controllability. When SS becomes less than 60 mV/dec, unexpected behaviors, such as DIBR and NDR, emerge in NCFETs, whose origin was analyzed by investigating the potential profile and the dependence of Q_G on V_{DS} and V_{GS}.

We found that, even if both the n-type and p-type NCFETs are hysteresis-free, the inverter shows hysteresis behavior due to NDR. Together with the fact that NDR accompanies hysteresis behavior in the inverters, it is difficult for the inverter composed of steep SS devices to avoid the hysteresis behavior. However, NCFET inverters with hysteresis behavior can be used as a noise filter, such as the Schmitt trigger inverter, which suggests an expansion of the application area of NCFETs.

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