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Test Structures for Nano-Gap Fabrication Process Development for Nano-Electromechanical Systems

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Abstract—**Nanometre scale pores, gaps or trenches are of significant interest for a number of applications in nano and microsystems, including biosensors, nanofluidic devices and mechanical resonators. This paper presents the design of two test structure chips for the development of a process capable of the fabrication of controllable nanoscale trenches or gaps. This process uses uses standard microfabrication technologies, without the need for nano-scale lithography. Initial results from the first test chip have suggested design rules for pattern density and feature size for the process, which relies on chemical mechanical planarisation of polysilicon. These results have been used to inform the design of a second test chip which includes mechanical and electrical test structures. Initial results show that HF etch rate of a nanoscale silicon oxide used as a sacrificial layer can be very high, even for the very high aspect ratio features in this process.**

I. Introduction

Nanometre scale gaps, trenches or pores have a range of interesting applications including DNA sequencing [1], nanofluidics [2], and MEMS resonators [3]. The purpose of the current study is to use test structures to explore relatively low cost methods to fabricate such features using standard micro-fabrication techniques, including micrometre scale lithography. Of particular interest is the investigation of the development of processes that can fabricate structures with narrow ($\leq$10 nm) trenches. The process involves the use of thermal oxidation to create highly controllable, nanometre scale sacrificial layers between silicon and polysilicon features. Subsequent processing can then be performed to create conducting electrodes on either side of the feature or to create larger micromechanical structures using more standard techniques. The nanogap can be created by etching the sacrificial oxide using a vapour phase etch with hydrofluoric acid (HF).

In this paper test structures have first been designed to determine the ideal pattern density for a nanogap process which uses chemical mechanical planarisation (CMP) of polysilicon. The results have informed the design of a second test chip layout which includes both electrical and mechanical test structures as well as etch release test structure to study the HF process. In order to create conducting electrodes on either side of the nanogaps a platinum silicide process could be used. The second test chip design includes electrical test structures to investigate the resistivity of the poly/Pt silicide material. In addition micromechanical strain test structures [4]–[6] have been included to study the effects of silicide formation on the intrinsic stress of the material.

II. Fabrication Process

The process for the fabrication of nano-scale gaps using micro-scale lithography is illustrated in Fig. 1. The key to this process is dry thermal oxidation, which can produce well controlled, uniform thin films with nanometre thicknesses. Bare silicon wafers are patterned with standard optical or electron-beam photolithography with micron-scale features (Fig. 1a) and etched using anisotropic reactive ion etching (Fig. 1b). The patterned wafers are oxidised to form a sacrificial SiO_2 layer of 10 nm or less (Fig. 1c). These oxidised wafers are coated with low pressure chemical vapour deposited (LPCVD) polysilicon with a thickness greater or equal to the silicon etch depth (Fig. 1d). The wafers are then polished, typically after dicing into single chips, using CMP with a silicate polishing slurry. The polishing is performed until the polysilicon and silicon oxide is completely removed from the unpatterned areas of the silicon substrate (Fig. 1e). This exposes silicon oxide insulation on the sidewalls of silicon and polysilicon structures. The final step is to etch the oxide using a vapour phase HF process to create nanometre scale trenches/gaps (Fig. 1f). Careful design of the polysilicon patterns makes it possible to release them from the silicon substrate in a similar manner to standard surface micromachined MEMS devices.

III. Test Structure Designs

Two test chips were designed. The first consists of an array of test features, including lines, squares, crosses, serpentines and waffle patterns, with varying dimensions, spacing, offsets and pattern densities. The objective of this layout was to assess polysilicon polishing using single chip processing on a Logitech CMP tool and to determine ground rules for designing more complex structures. The polysilicon feature critical

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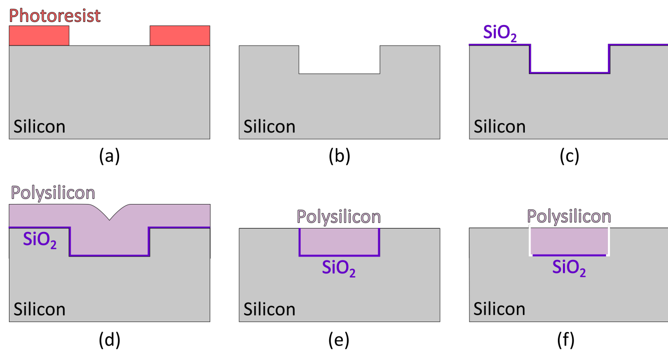


Fig. 1. Schematic representation of process flow for sacrificial nanogap fabrication.

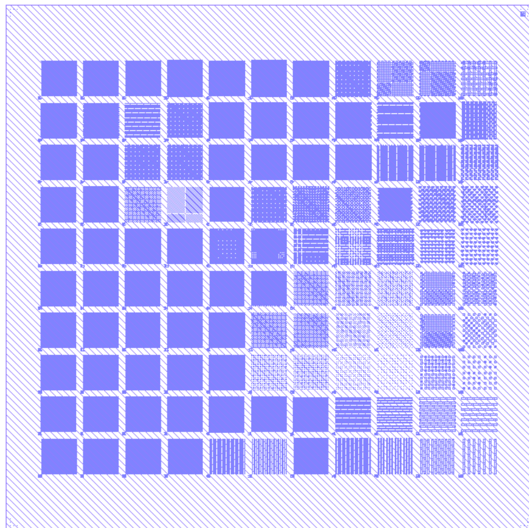
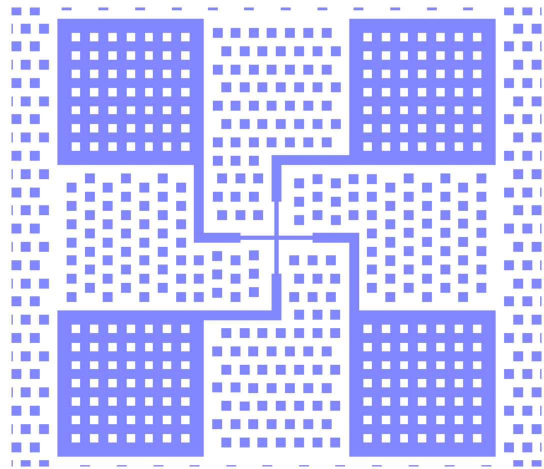
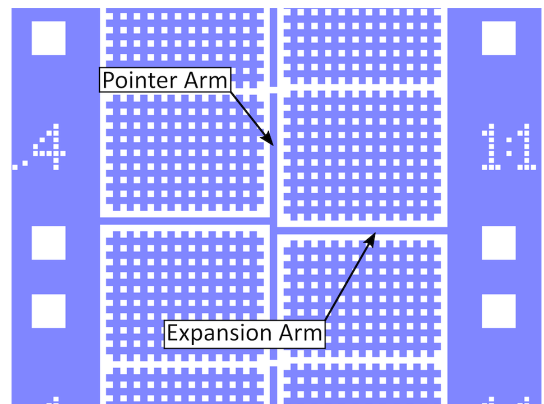


Fig. 2. Layout of test chip 1



(a)



(b)

Fig. 3. (a) Part of test chip 2 layout showing a Greek cross with arm width of 2 µm. (b) Part of test chip 2 layout showing a microrotating MEMS test structure. Both designs include dummy features to improve the uniformity of the polishing process.

dimensions ranged from 5 µm to 50 µm with pattern density ratios starting at approximately 4:1 between polysilicon and unetched silicon with increasing ratios of unetched silicon up to 1:15. The areas between the different patterns in the array have no etched silicon, and this was designed to provide the requirement for dummy fill patterns in future designs. Fig. 2 shows the layout of test chip 1, in general the polysilicon feature size increases from left to right across the chip while the pattern density reduces.

Initial results (see section IV-A) indicate that the most even planarisation requires relatively small features and a high ratio of polysilicon (etched trenches) to unetched silicon. Based on this a second test chip was designed which includes Greek cross sheet resistance test structures (Fig. 3(a)) to investigate the conductive properties of polysilicon after silicidation as well as micromechanical stress test structures. The design of one stress test structure with a critical dimension of 1µm is shown in figure 3(b). This is based on well understood test structures for measurement of stress/strain in patterned thin films as detailed in previous publications [4]–[6]. The operating principal is that when the test structure is partly released from the substrate by a sacrificial etch, the expansion arms will expand or contract due to intrinsic stress in the material and cause the pointer arm to rotate. Unusually, in this application the nano-scale scale gap surrounding the released structure will limit the rotation making it realistically only possible to determine whether the force is tensile or compressive, assuming there is no stiction resulting from surface tension effects. The design includes a range of different pointer arm lengths and different expansion arm separations, with the aim of investigating whether these structures could be used for determining whether stress was tensile or compressive. These structures could potentially also be used to observe any intrinsic stress in the deposited polysilicon as well as to detect any change in stress due to silicidation. Both tensile and compressive stresses in platinum silicides have been previously observed [7], [8].

IV. Results

A. Test Chip 1

Fig. 4 shows a low resolution microscope image of test chip 1 after CMP processing. This chip has been polished

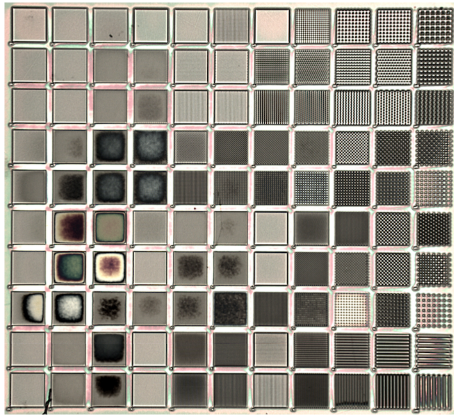


Fig. 4. Microscope image of test chip 1 after CMP.

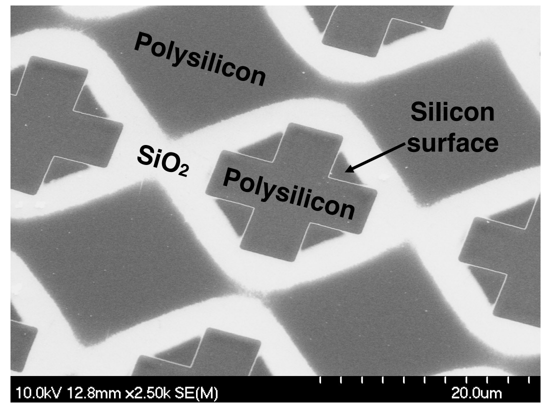
for 5 minutes with a silicate based polishing slurry which will mechanically remove both polysilicon and silicon dioxide. The chip was processed until it was clear that at least some of the patterns had been correctly planarised. Designs with small feature sizes and good CMP results show as a uniform grey colour while remaining polysilicon can be seen in some test patterns as an uneven darker colour, or as a brighter reflective material covering larger areas of unetched silicon.

SEM images of two different patterns are presented in Fig. 5. In Fig. 5(a) the polysilicon and SiO_2 is not completely removed due to the relatively low pattern density. This pattern has cross shaped etched trenches with a feature width of 5 μm and a spacing of 10 μm. The average polysilicon:silicon density of this pattern is 1:4. Meanwhile, in Fig. 5(b) the removal is complete. This design has etched trenches in a waffle pattern with 5 μm features and 10 μm square gaps, giving an average polysilicon:silicon density of 5:4. Waffle patterns such as this gave the best results for the polishing process.

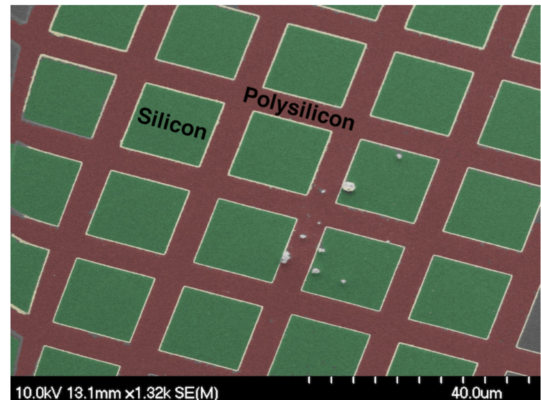
The results from test chip 1 suggest that pattern density ratios of less than ∼1:2 (etched: unetched) resulted in incomplete removal of both the polysilicon and silicon dioxide from the unetched silicon areas. This can be seen in Fig. 6, which shows part of an array of 20 μm squares (etched) with a 40 μm space. The pattern density here is 1:8 and it is obvious that there is remaining polysilicon and SiO_2 between the etched structures. It is clear that there is also significant remaining polysilicon in the space around the edge of the test pattern.

In addition, polysilicon filled trenches with critical dimensions larger than 20μm showed significant "dishing" where the material is lower in the middle of the feature than at the edges. This is illustrated in figure 7 which shows a checkerboard pattern (pattern density 1:1) with 50 μm squares where the variation of the polysilicon thickness is clearly visible.

One sample of test chip 1 was used in an initial trial of HF vapour etching. Figure 8 is an SEM image of a portion of a serpentine pattern from a chip with was etched for 5 minutes using an IDONUS vapour phase etch system with an etch temperature of 40C. The etching of the oxide is clear in this image though no etch rate was determined on this sample.



(a)



(b)

Fig. 5. SEM Images of cross and waffle patterns from test chip 1 after polishing. Figure (a) shows a cross pattern with incomplete removal of polysilicon. Figure (b) has false colour added to highlight the different materials in the structure. Red is polysilicon, green is the unetched silicon, and yellow is the thin silicon oxide which has charged up in the SEM.

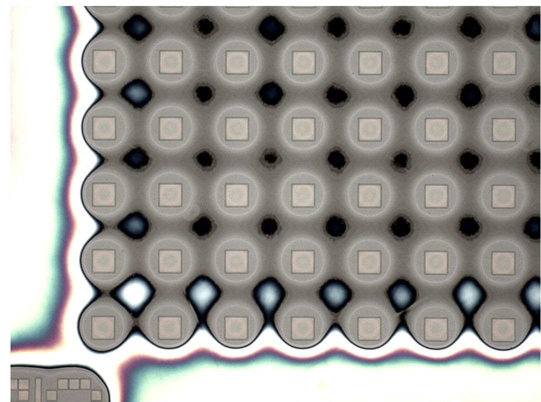


Fig. 6. Microscope image of part of an array test pattern with 20 μm squares (etched) with a 40 μm space.

B. Test Chip 2

A sample of test chip 2 was etched using a Memsstar Orbis Alpha HF vapour etch system with the intention of investigating how well the process released the structures;

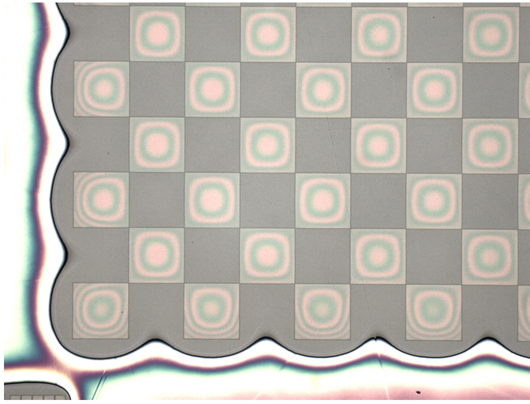


Fig. 7. Microscope image of part of a checkerboard test pattern with 50 µm squares

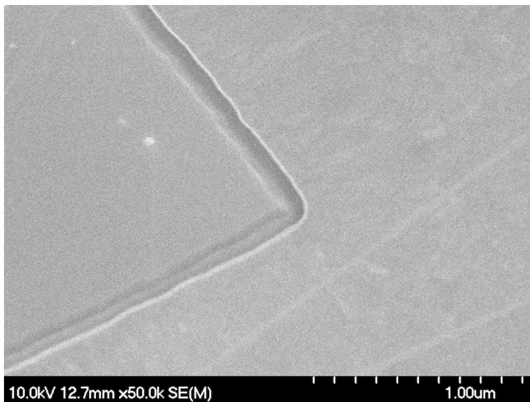
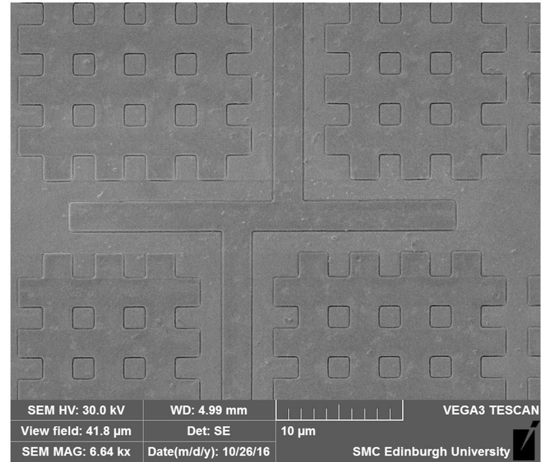
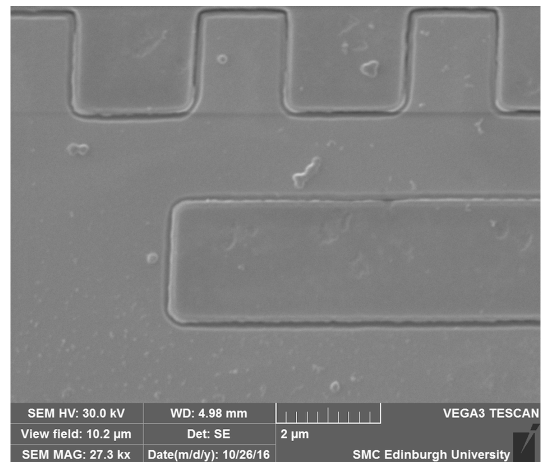


Fig. 8. SEM image of a structure on test chip 1 which has been HF etched to partially remove sacrificial oxide.



(a)



(b)

Fig. 9. (a) SEM image of a micromechanical test structure from test chip 2. (b) is a close up of the left hand end of the pointer arm of the structure.

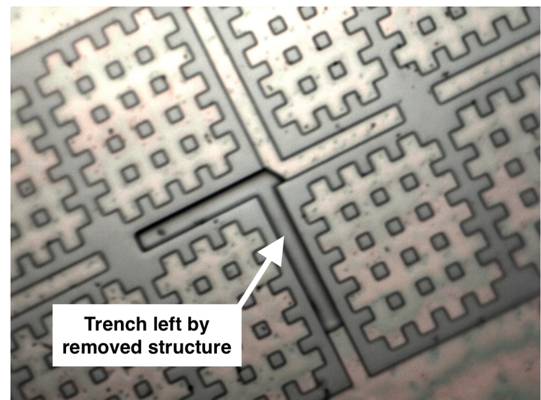


Fig. 10. Released structure removed with Kapton tape.

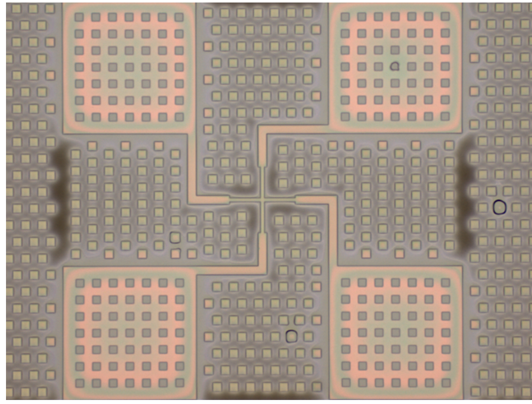
i.e. how far underneath the structure the underlying sacrificial oxide would be removed. Fig. 9(a) and (b) shows SEM images of a strain test structure on test chip 2. These images suggest that there is no visible rotation of the pointer arm on the micromechanical structure. There are a number of possible conclusions from this:

1) the structure has not been completely released,
2) the structure is stuck to the substrate by stiction forces,
3) the level of intrinsic stress is too low to cause significant movement,
4) the nanoscale gap means any rotation is not visible, or
5) the oxide has been completely removed, releasing the anchors for the expansion arms and relieving the stress.

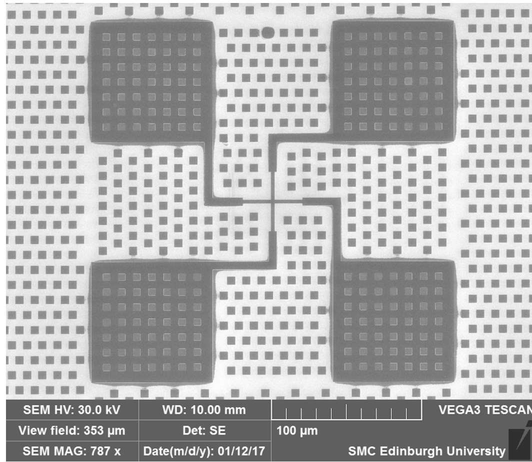
The etch process applied here was relatively aggressive as it was thought that the etch rate in the high aspect nano-trench would be slow. Operating in such a regime involves the generation of water which could result in stiction of the structures. With such a thin sacrificial layer minimising water generation is very important for successful release. Fig. 10 shows where part of the structure has been removed by performing a standard layer adhesion test using Kapton tape. This suggests that complete release has been achieved as no SiO_2 was visible in the trench. This result also suggests that the adjacent dummy fill waffles have also been "released".

C. Full Wafer Processing

Full wafers of both test chip designs have subsequently been CMP processed using a PRESI polishing system with a slurry

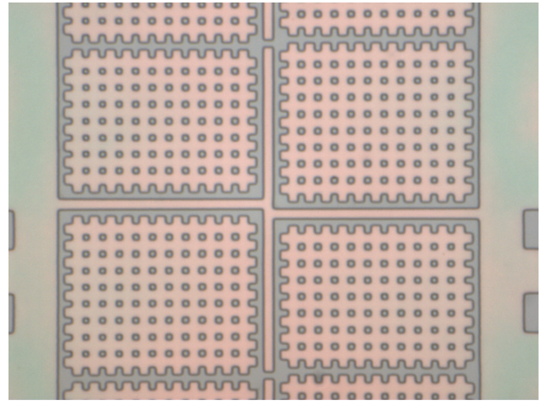


(a)

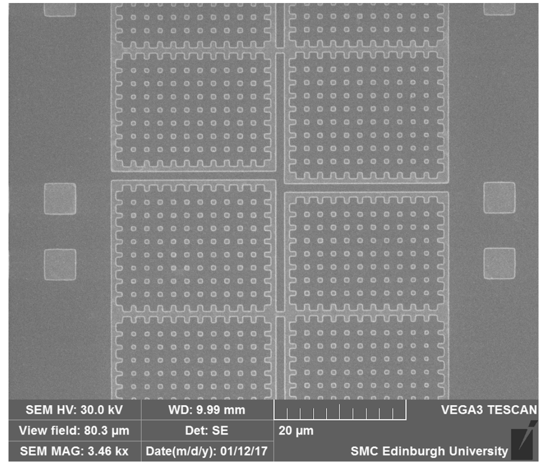


(b)

Fig. 11. (a) Microscope image of a Greek cross test structure with a 2 µm arm width. (b) SEM image of a Greek cross test structure with a 2 µm arm width.



(a)



(b)

Fig. 12. (a) Microscope image of a 1 µm wide stress release test structure. (b) SEM image of a 1 µm wide stress release test structure.

designed for silicon and polysilicon processing. This showed increased polysilicon removal rates and better uniformity than previous single chip processing. Figure 11 shows Greek cross test structures from a test chip 2 wafer, which has been polished for a total of 90 seconds in 30 second steps. In the optical microscope image darker material is visible around the dummy fill areas and the SEM image clearly indicates that this is silicon dioxide as it is brighter than the conducting silicon and polysilicon due to charging. This suggests that the dummy fill pattern density is too low but it would not prevent further HF etch release processing as this material would be quickly removed.

Figure 12 shows stress test structures with a 1 µm wide arm width from the same wafer. The higher polysilicon pattern density in these structures means that there is no remaining SiO_2 over the silicon surface. The thin oxide surrounding the recessed polysilicon features is clearly visible and the next step will be to attempt HF sacrifical etching. These results are very promising for future fabrication of nano-gap structures using this process and will lead to further optimisation of dummy fill features and sacrificial etch processes.

V. Conclusions and Future Work

This paper has detailed the design of test structures to support the development of processes to create nanometre scale gaps or trenches using standard microfabrication processes to create sacrificial layers with nm dimensions. The first test chip has been used to study CMP of polysilicon and determine design rules for feature size and pattern density in this process. A second test chip design based on these results has been fabricated and initial results demonstrate that the release process has been successful. These results are very encouraging as they indicate that structure release can be achieved with very narrow trenches ($\sim$10 nm). Further work will involve the release of structures with the Memsstar Orbis Alpha system programmed with a much slower etch process to minimise the formation of water vapour. This investigation will also involve characterising the ability of HF vapour to release structures and to develop design rules for nanoscale trench spacings required for the release of such structures. In addition, the wafer level processed structures will be used to investigate platinum silicidation and the effects on electrical and mechanical properties.

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