Test structures for the characterisation of sensor packaging technology

Test Structures for the Characterisation of Sensor Packaging Technology

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Abstract – This paper presents three test structures targeted at characterising sensor packaging materials for liquid environments. The test structures enable the evaluation of: 1) the successful removal of packaging material on sensing areas, 2) the permeability of the packaging material to its environment, 3) electrical continuity through the packaging process, and 4) the ingress of the liquid environment between the packaging material and the chip surface. The paper presents an example of the evaluation of a UV curable resin as packaging process for a biomedical sensor.

I. Introduction

Microsystems packaging is a key technology, focused on interfacing MEMS and sensor systems to the world in a low-cost and reliable manner. A particularly challenging area is the packaging of sensor systems which require some area(s) of the electronics to be in direct contact with the surrounding environment [1], [2]. This is especially the case when liquids are involved, which requires the encapsulation material to be patterned [3]. Numerous materials have been reported for this purpose, but are typically not available in a standardised way, such as is the case for microelectronic integrated circuits [1], [4]–[6].

Generally, the key parameters of the encapsulation material are:

- The permeability or barrier properties to the surrounding environment;
- physical durability;
- adhesion of the encapsulation material to the surface of the chip;
- ability to be patterned to expose sensing areas; and
- compatibility with standard microfabrication or post-CMOS processing techniques.

In any process development, it is important to be able to quantify parameters that characterise the performance of the overall packaging technology. This paper presents three test structures that can be used to characterise these parameters, facilitating quantifiable comparisons between packaging materials and techniques, thereby enabling systematic optimisation of selected encapsulation technologies. The capability of these test structures is then assessed by characterising an example sensor packaging process, according to the parameters outlined above. A biocompatible, UV-curable epoxy-resin (Epo-Tek ETOG116-31/1LB) was chosen, as a relevant material for biomedical sensors. In this area of research, stringent biocompatibility and miniaturisation considerations present challenges [2], [7], [8]. It is therefore especially important to be able to thoroughly characterise packaging materials and processes for biomedical applications.

II. test Structure Philosophy and Design

The three test chip layouts have been designed with the purpose of characterising specific aspects of the packaging material and process:

1. The layout of test structure one (TS1) is presented in figure 1(a). It consists of a chip with four rows of connected aluminium bond pads, used for checking electrical continuity throughout the packaging process. Optical inspection of the blank central area can be used to confirm that no residue has been left behind by the patterning process.
2. The second test structure layout (TS2) is shown in figure 1(b). This uses a 2 mm square electrode in the centre to quantify pinhole density and/or permeability of the packaging material to its environment.
3. The final layout (TS3) is shown in figure 1(c) and comprises 6 parallel interconnects of differing lengths. This enables the ingress of the liquid environment between the package material/chip interface to be monitored, informing both the lifetime of the package and the adhesion of the package material to the chip.

TS2 and 3 use electrodes to measure leakage current/ion permeation through the material of choice and ingress of liquid solution respectively. This is achieved by applying a potential difference between the electrode under the packaging material and the liquid environment, and monitoring any current. A more detailed explanation and analysis of electrochemical techniques, applied to measure barrier material properties are reported here [9].

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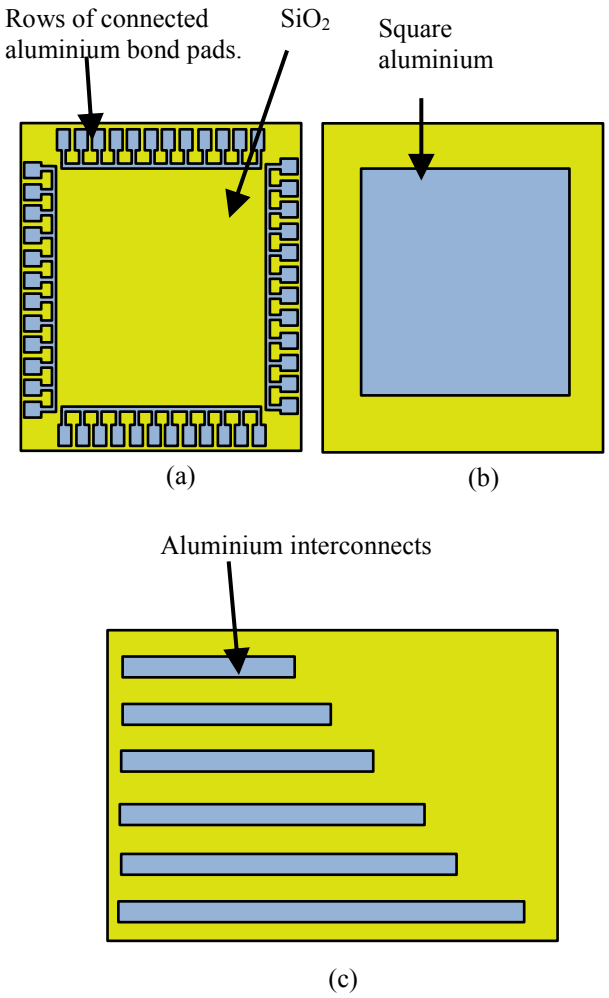

Figure 1: Schematic layout of (a) test structure one (TS1), (b) test structure two (TS2), and (c) test structure three (TS3). Not to scale.

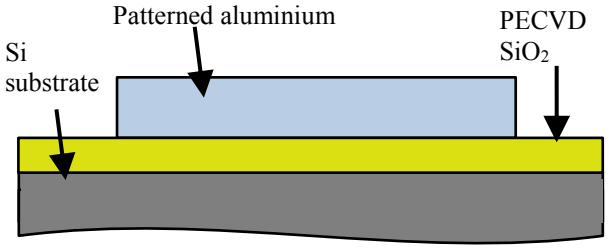

Figure 2: Schematic cross-section through a test structure, showing the layers. Not to scale.

III. Fabrication of Test Structures

It is essential that the processes used to fabricate the test structures replicate those used in typical sensor technology. Therefore, for this work, a 500 nm thick insulating layer of SiO_2 is deposited using Plasma Enhanced Chemical Vapour Deposition (PECVD) on a silicon wafer, followed by 1 µm of sputtered aluminium. The aluminium is then patterned to form one of the test structure shown in figure 1. The wafer is then diced into individual chips, ready for characterisation. Figure 2 presents a schematic cross section of the layers forming the test structures.

A. *Package Preparation*

For characterising the example encapsulation material, the test structures were glued into ceramic chip packages and wire bonded as in figure 3 (a). The UV sensitive epoxy resin (encapsulation) being evaluated was manually dispensed over the chip to fill the cavity. TS1 and 3 were then exposed to UV light through a photomask which shielded areas of the epoxy. As the epoxy resin is a negative type material, the areas shielded from the UV light remained uncured and could easily be removed. These became windows in the resin, exposing the chip underneath. For TS1, a 2 mm square area in the centre was masked from the UV light and for TS3, the area chosen was a large rectangle which overlapped the die but not enough to expose the metal electrodes. The rest of the epoxy was exposed for 14 minutes; the relatively long exposure time was due to the low power of the UV source used. After exposure, the uncured epoxy was removed by first rinsing in acetone, then isopropanol alcohol, and finally deionised water before drying in N_2. The next section details the characterisation of the resin for encapsulating a device exposed to an aqueous solution

IV. Measurement Results

A. *Process Characterisation*

Photographs of TS1 before and after dispensing and patterning of the resin are shown in figure 3(a) and (b) respectively. Optical inspection confirmed the epoxy had been completely removed, as evidenced by a microscope image of the cleared surface of a TS1 in figure 4. In order to further check that no residue remained, a reflectometer was used to measure the thickness of the exposed SiO_2 before and after packaging the chip. Any residue would alter the reflective properties of the SiO_2 surface and result in a change in the measured thickness. The measured values are presented in table 1 and suggest there has been no appreciable change to the SiO_2 surface, hence suggesting that the uncured epoxy has been successfully removed.

Table 1: Average thickness of the SiO_2 insulation layer measured before and after packaging. Five measurements were taken across each chip surface. Standard deviations are presented to ± 3σ.

	Average thickness of SiO_2 layer (nm)		
	Chip 1	Chip 2	Chip 3
Before dispensing resin	473 ± 3	473 ± 2	475 ± 3
After removing uncured resin	478 ± 9	475 ± 5	475 ± 2

B. *Electrical Continuity*

The connectivity of the electrical connections and wire bonds was established on TS1 both before dispensing the resin and after removing the uncured material. The electrical path measured is shown schematically in figure 5. Since only

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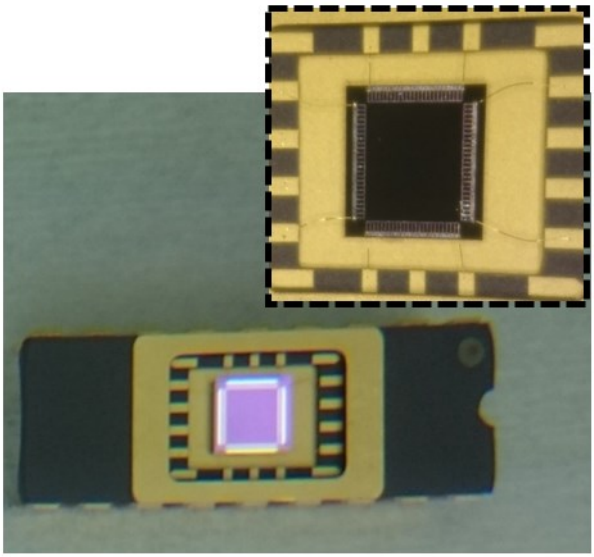
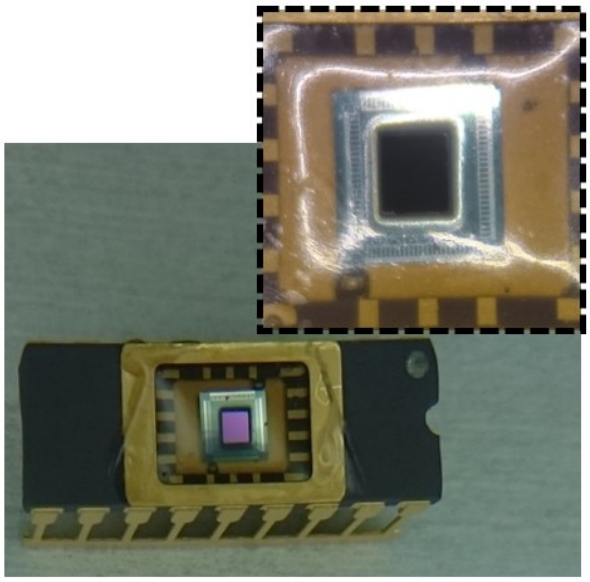


(a)



(b)

Figure 3: Photograph of a TS1 (a) before dispensing of epoxy resin and (b) after patterning.

Figure 4: A 10× microscope image of the exposed SiO_2 surface of a TS1 after removal of uncured epoxy.

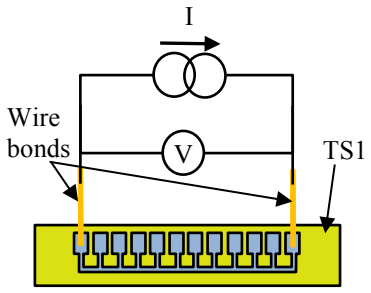


Figure 5: Schematic diagram of the two-terminal measurement employed to monitor connectivity of the wire bonds.

the presence of an electrical path through the circuit was of interest, a two-terminal measurement was deemed sufficient. If a Kelvin measurement is desired, another pair of bond wires could be added enabling a 4 terminal resistance measurements to be made. All test structures were additionally subject to 20 minutes of ultrasonic agitation in deionised water to test the physical durability of the package. Table 2 presents the measured resistances before dispensing the resin, after removing the uncured material, and after ultrasonic agitation.

Table 2: Average electrical resistance measured through the wire bonds and contact pads before and after packaging. Four measurements were taken from each chip, one for each row of contact pads. Standard deviations are presented to ± 3σ.

	Average electrical resistance of wire bonds (Ω)		
	Chip 1	Chip 2	Chip 3
Before dispensing resin	12.1 ± 1.1	11.4 ± 0.6	11.5 ± 0.6
After removing uncured resin	12.3 ± 1.4	11.8 ± 0.8	11.6 ± 0.4
After US agitation	12.2 ± 1.4	9 ± 9.9	11.7 ± 0.3

The results indicate that the dispensing, curing, and clearing processes have not damaged the wire bonds. Additionally, the bonds survived the 20 minute ultrasonic agitation test, which demonstrates the mechanical robustness of the encapsulation material

C. Leakage Current Test

Leakage current measurements of the example system were made on TS2. Photographs of TS2 before and after packaging are presented in figure 6 (a) and (b). UV glue was then used to create walls to confine a 500 mM KCl solution over the resin. A range of voltages were applied between the metal areas on the test structures and a secondary electrode (a silicon strip coated in a 50 nm film of platinum) immersed in the solution. Any pinholes or permeability of the resin would be indicated by an increase in current. Measurements were performed in a Faraday cage and a photograph of this set up is shown in figure 7. A range of voltages between –5 V and

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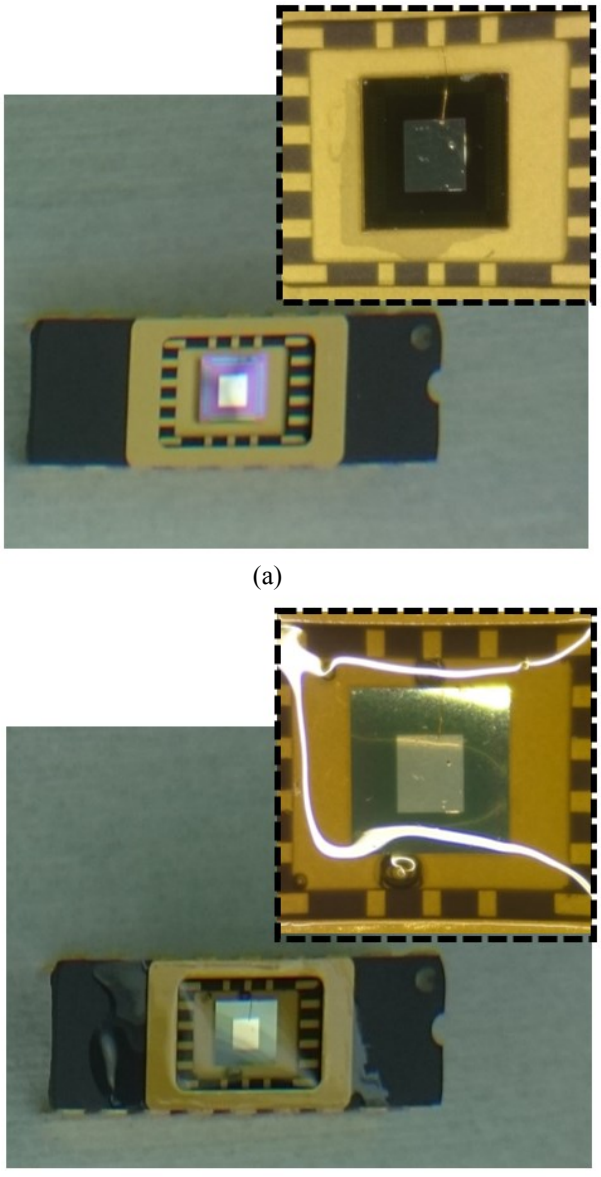
+5 V were applied, each for 5 minutes. Although applying a potential is a more destructive method of assessment than techniques which do not (such as monitoring open circuit potential), it would be expected to accelerate the appearance of any corrosion [9], [10].



(a)

(b)

Figure 6: Photograph of a TS2 (a) before dispensing of epoxy resin and (b) after curing.

Figure 8 presents the average current measured against applied potential. It is encouraging to see that the currents are on the order of 10 pA, typically on the levels of electrical noise. The recorded currents also do not change with applied potential, lending confidence to the conclusion the recorded current stems from background electrical noise and not pinholes or permeability of the resin.

D. Resin Adhesion

The adhesion of the resin to the chip surface was investigated using TS3. An example of a TS3 before and after dispensing and patterning of the resin is shown in figure 9 (a) and (b) respectively. The window patterned into the resin

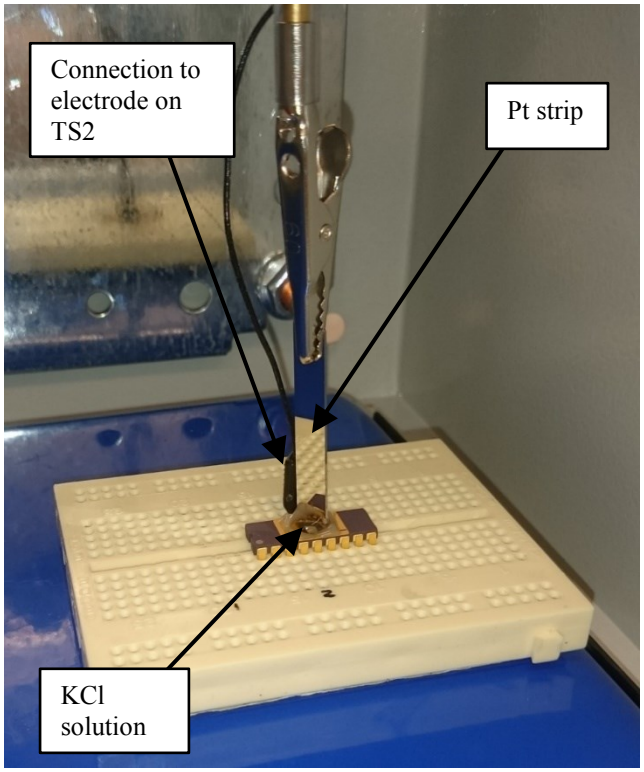


Figure 7: Photograph of the electrochemical set up used to measure the leakage current with TS2.

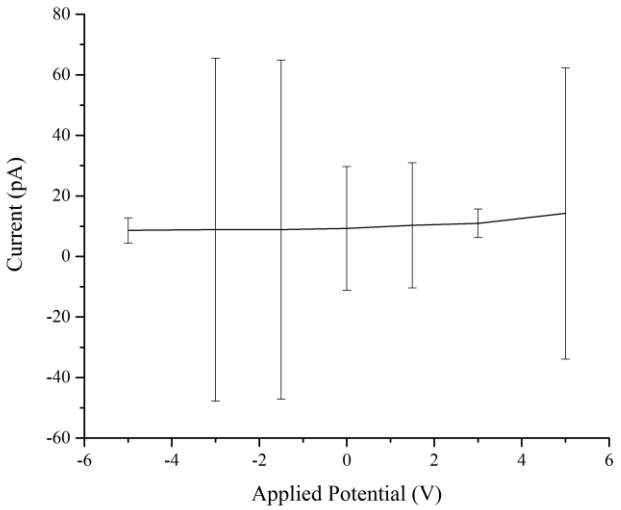
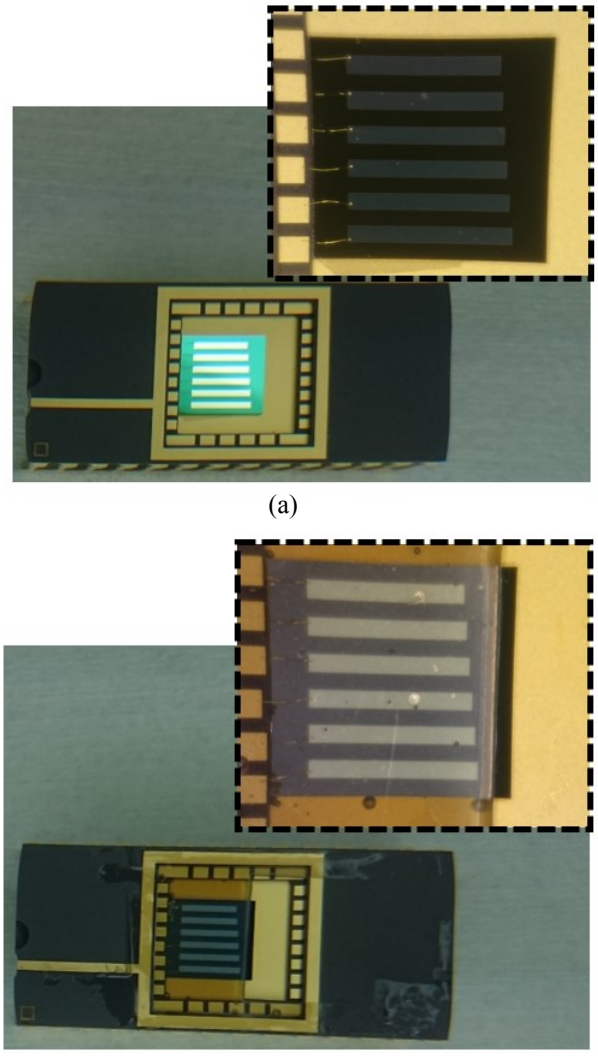


Figure 8: Plot of average current against applied potential. Each point is an average current measured across 5 minutes over 3 test structures, resulting in 1800 measurements per potential. Standard deviations are presented to ± 3σ.

overlapped the die, exposing the resin/chip interface. Should the liquid environment encroach between the chip and resin, it will be measured at the electrodes. Three packages were dipped vertically into 500 mM KCl until the window patterned in the resin was submerged. The electrical connections to the electrodes were therefore above the solution, but were still covered with epoxy to prevent any possible shorting. 5 V DC was applied between a Pt counter electrode, also in the solution, and each electrode sequentially for ten days. The experiment too large for the available Faraday cages, hence the background noise was larger than that measured in figure 8. For this reason, the KCl was deemed to have made contact with the aluminium electrode

when the current measured between it and the Pt strip increased to above 10 nA. The time between this occurring at each electrode was divided by the distance between each electrode, giving the rate at which the KCl progressed between the resin and chip surface.



(a)

(b)

Figure 9: Photograph of a TS1 (a) before dispensing of epoxy resin and (b) after patterning.

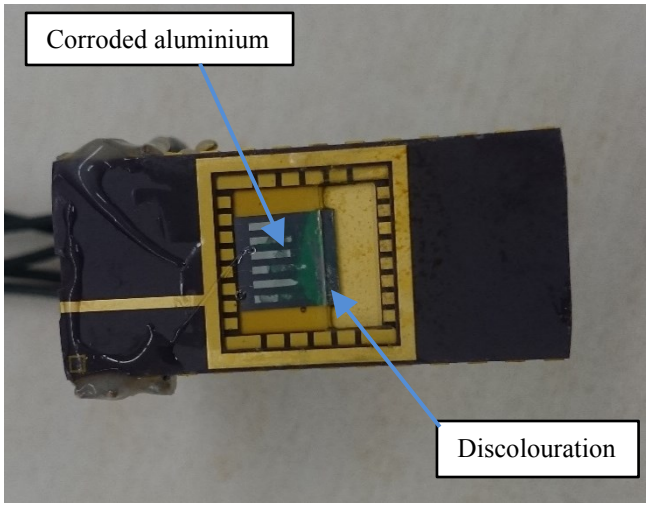


Figure 10: Photograph of a TS3 sample after immersion in KCl for ten days.

Unfortunately, the difference in time between the electrodes making contact with the solution varied greatly, resulting in ingress rates ranging from 2 to 48 μm/hour. However, the KCl has certainly ingressed under resin over the time-course of the experiment. This is further confirmed by the photograph in figure 10 which presents a TS3 after ten days of immersion in KCl. The aluminium electrodes have clearly been corroded and the area where the KCl was present has become discoloured.

V. Discussion

The optical measurements of TS1 indicate that the open areas patterned into the resin were free of significant residue. If this had not been the case, and more thorough cleaning was required, then the results from the electrical measurements demonstrate that the resin is physically robust enough to withstand ultrasonic agitation. This means harsher cleaning methods may be applied if required. The electrical measurements also demonstrate that TS1 can be used to assess how wire bonds and packaging materials will cope when employed in physically stressful environments.

The leakage currents measured on TS2 suggest that the resin insulates effectively in KCl. These measurements could be performed using a number of more application-specific aqueous solutions or temperatures. Other electrochemical measurement techniques could be employed, such as electrochemical impedance spectroscopy or, the previously mentioned, open circuit potential.

TS3 enabled a rough rate of ingress to be determined, although this was variable, as values ranged between 2 and 48 μm/hour. This could be due to the epoxy not being outgassed, trapping air bubbles in the resin. Pinholes may also be present in the resin, and could contribute towards the high variability. Another possibility stems from KCl encroaching between the package and the chip around the perimeter of the cavity. Though this seems unlikely, as the distance to the electrodes is much greater via this route. The results obtained from TS3 indicate that, in this instance, the adhesion of the epoxy resin requires optimisation before being employed in applications lasting longer than several hours.

The EPO-TEK resin demonstrated good insulation properties from the KCl solution, was physical durable, and easily patterned. However, the adhesion of the resin to the chip surface presented a weak point and allowed ingress of the solution over several days. Methods of improving adhesion, such as pre-treating or roughening the surface of the chip, could be employed; with the test structures presented here enabling a systematic comparison of these techniques.

IV. Conclusion

Sensor packaging materials are typically required to insulate effectively in liquid environments and can be patterned. This paper has presented three test structures capable of characterising packaging materials. These test structures were

then employed in characterising a bio-compatible, UV curable resin. They enabled:

- The successful monitoring of the gold wire bond stability through the packaging process and a further physical durability test;
- confirmation that the uncured resin had been removed from the desired areas during patterning;
- quantification of the resin's permeability to a KCl solution, mimicking a typical liquid environment; and
- assessment of the adhesion of the resin to the chip surface and monitoring the rate of ingress of the liquid environment between the chip and resin.

The combination of these tests results in a comprehensive understanding of the strengths and weaknesses of various packaging materials. These test structures can then be further used to systematically optimise key parameters of packaging processes and materials. They are therefore, already being implemented in other projects involving chip packaging. Further work is required to be able to batch test many test structures at once, and for longer durations in order to assess insulation layer lifetimes. This would enable large scale, statistically significant comparisons of numerous materials

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