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Title: Trap Healing for High-Performance Low-Voltage Polymer Transistors and Solution-Based Analogue Amplifiers on Foil

Vincenzo Pecunia†, Mark Nikolka†, Antony Sou, Iyad Nasrallah, Atefeh Y. Amin, Iain McCulloch, Henning Sirringhaus**

Dr. V. Pecunia, Dr. M. Nikolka, Dr. A. Sou, Dr. I. Nasrallah, Dr. A. Y. Amin., Prof. H. Sirringhaus
Optoelectronics Group, Cavendish Laboratory, J J Thomson Avenue, Cambridge CB3 0HE, United Kingdom.
E-mail: vp293@cam.ac.uk, hs220@cam.ac.uk

Dr. V. Pecunia
Institute of Functional Nano & Soft Materials (FUNSOM), Jiangsu Key Laboratory for Carbon-Based Functional Materials & Devices, Soochow University, 199 Ren'ai Road, Suzhou, 215123, Jiangsu, PR China.

Dr. A. Sou
Currently at: Pragmatic Printing Ltd., Unit 322, Cambridge Science Park, Milton Road, Cambridge, CB4 0WG, United Kingdom.

Prof. I. McCulloch
Department of Chemistry, Imperial College London, South Kensington Campus, London SW7 2AZ, United Kingdom.

† Equal contribution

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Abstract

Solution-processed semiconductors such as conjugated polymers have great potential in large-area electronics. While extremely appealing due to their low-temperature and high-throughput deposition methods, their integration in high-performance circuits has been difficult. An important remaining challenge is the achievement of low-voltage circuit operation. The present study focuses on state-of-the-art polymer TFTs based on IDT-BT and shows that the general paradigm for low-voltage operation via an enhanced gate-to-channel capacitive coupling is unable to deliver high-performance device behaviour. The order-of-magnitude longitudinal-field reduction demanded by low-voltage operation plays a fundamental role, enabling bulk trapping and leading to compromised contact properties. A trap-reduction technique based on small molecule additives, however, is capable of overcoming this effect, allowing low-voltage high-mobility operation. This approach is readily applicable to low-voltage circuit integration, as this work exemplifies by demonstrating high-performance analogue differential amplifiers operating at a battery-compatible power supply voltage of 5 V with power dissipation of 11 μW, and attaining a voltage gain above 60 dB at a power supply voltage below 8 V. These findings constitute an important milestone in realising low-voltage polymer transistors for solution-based analogue electronics that meets performance and power-dissipation requirements for a range of battery-powered smart-sensing applications.

Solution-processed semiconductors such as conjugated polymers have recently received significant attention for their potential in large-area electronics. Their great appeal arises from the compatibility with low-temperature and high-throughput deposition (e.g., by printing and coating) on plastic substrates, and their excellent mechanical properties that will enable electronic circuits to be deployed in non-traditional environments and form factors, e.g., for applications in wearable electronics, the Internet of Things, sensing, and bioelectronics. Several groups have already achieved impressive demonstrations of complex circuits, including active matrix sensor arrays,[1,2] an organic-based microprocessor,[3] and RFID tags on PEN substrates.[4] These demonstrations were based either on vacuum-sublimed p-type organic thin-film transistors (TFTs);[1,2] or on the combination of vacuum-sublimed p-type organic and n-type oxide TFTs.[3–5]

With solution-processible materials, integration of high-performance circuits has been more difficult. An important remaining challenge is the achievement of low-voltage operation. Most of the solution-based circuit demonstrations made to date operate at above 10 V, and are thus not compatible with the limited supply voltage and power available from compact energy harvesters and low-cost printed batteries.[6,7] This is especially true for analogue electronic applications, which represent particularly demanding requirements: they require all transistors to operate in saturation, each one taking up a finite share of the power supply voltage; they are highly sensitive to the detailed shape and non-idealities of the transistor characteristics; and they place stringent requirements on variations of the threshold voltage.[8]

The main approach to low-voltage operation in organic TFTs has been along the same lines as in conventional silicon technology, namely to increase the gate-to-channel capacitive coupling via thinner and higher-*k* dielectrics.[9–14] Operation at around 1 V has been successfully demonstrated in a number of systems, most notably using evaporated small molecule semiconductors with SAM nanodielectrics.[14] However, with solution-processed polymer transistors, specific challenges are encountered, as dictated by their electronic

structure and charge-transport properties. Here and in the following, low-voltage operation refers to transistors capable of switching between their OFF and ON regions for a maximum terminal bias of about 3 V.[14–18] For a transistor channel length in the micrometre range, as allowed by conventional microfabrication methods, low-voltage operation corresponds to typical longitudinal electric fields down to 1 kV cm^{-1} or less; at the same time, for gate dielectric thicknesses in the submicron range, the transverse field is reduced to tens of kV cm^{-1}. This is to be contrasted with the operational window of conventional organic transistors, driven by an order of magnitude higher fields. The relatively high bulk trap density of polymer semiconductors tends to give large threshold voltages and shallow subthreshold slopes when the transverse field is reduced to such small values. In addition, the dramatic reduction of the longitudinal field requires to take into account its impact on transport and injection. As a result, no approach to low-voltage polymer TFTs reported to date meets the requirements for analogue integration. For instance, there is currently no successful demonstration of differential amplifiers—the prototypical embodiment of an analogue circuit—using solution-processed materials that operate below 15 V.

Here we argue that the mere enhancement of the gate-to-channel capacitance via high-k gate dielectrics may not be sufficient for low-voltage operation of polymer transistors. We studied state-of-the-art high-performance polymer TFTs based on poly(indacenodithiophene-benzothiadiazole) (IDT-BT), a high-mobility ($\mu \approx 1\ cm^2\ V^{-1}\ s^{-1}$) conjugated polymer with nearly "disorder-free" charge transport properties,[19] combined with solution-processible relaxor ferroelectric polymer P(VDF-TRFE-CFE), a high-k dielectric ($k \approx 40$) previously demonstrated in low-voltage organic and amorphous-metal-oxide transistors,[11,20] and we found that their performance is rather poor and well below their high-voltage counterpart, in spite of the strong gate-to-channel capacitive coupling. We show that this is triggered by the order-of-magnitude reduction of the longitudinal field inherent in low-voltage operation, which enables bulk trapping to emerge, and leads to compromised contact properties. Hence

we show that techniques to reduce trap density in polymer semiconductors are needed to achieve low-voltage transistor operation suitable for battery-compatible analogue circuit integration.

We fabricated top-gate bottom-contact IDT-BT TFTs with a 210-nm thick film of P(VDF-TRFE-CFE). In order to avoid interfacial dipolar disorder due to the high-k polymer gate dielectric leading to a reduction of the field-effect mobility and transistor performance,[21] we inserted a 25 nm-thin low-k fluoropolymer dielectric layer of CYTOP® between the semiconductor and the relaxor ferroelectric film. In the following, transistors with such gate dielectric stack will be referred to as low-voltage. A cross-sectional view of these transistors and the materials used are shown in **Figure 1**a-c. For the sake of comparison, we shall also discuss devices with a thick low-k gate dielectric (a 500 nm-thick CYTOP® film), which constitute the high-voltage counterpart.

Low-voltage transistors with pristine IDT-BT layers are characterised by rather poor performance. As illustrated in **Figure 2**a,b, their characteristics denote an anomalous behaviour: the drain current increases superlinearly with drain voltage, is approximately invariant of the gate voltage V_G in the linear region, and exhibits a super-quadratic dependence on V_G in saturation. The poor performance is confirmed by the extremely low apparent linear and saturation mobility (extracted as detailed in the Experimental Section). The saturation mobility has a pronounced dependence on V_G, and is as low as $1.6 \cdot 10^{-1}$ cm^2 V^{-1} s^{-1} at its maximum. This is approximately an order of magnitude lower than corresponding high-voltage devices, even at equal induced carrier concentration (i.e., $C_d \cdot V_G$, C_d being the gate dielectric capacitance) (Figure 2c). The sizeable discrepancy between apparent saturation and linear mobility further confirms the substantial deviation from ideal TFT models. Finally, while always giving poor performance, low-voltage IDT-BT transistors present a significant batch-to-batch and device-to-device variability (see SI 1). All this shows that a strong gate-to-

channel capacitive coupling (and a non-polar semiconductor-dielectric interface) is not sufficient to achieve low-voltage operation in IDT-BT transistors. In regard to their use in flexible electronics, they would offer a poor match to state-of-the-art n-type transistors, thus impairing complementary circuit integration.

The highly non-linear output characteristics at small drain-to source bias V_{DS} may result from the convolution of contact and transport effects. Transmission-line method (TLM) analysis of low-voltage pristine IDT-BT devices with variable channel length gives a contact resistance of approximately 3 MΩ cm (**Figure 3**a). As conventional TLM assumes that contact and transport properties are independent of longitudinal field, we also carried out gated four-point-probe (gFPP) measurements, which allow the direct evaluation of contact resistance and carrier mobility at varying fields (SI 2).[22] gFPP measurements on low-voltage pristine IDT-BT devices give a contact resistance exponentially decreasing with contact potential, with values in the region of 1-10 MΩ cm (SI 2). They also reveal that the actual field-effect mobility (i.e., purged of contact effects) is approximately 1.0 $cm^2 V^{-1} s^{-1}$ and invariant of the longitudinal field E_l (Figure 3c). This is nearly an order of magnitude greater than the apparent mobility extracted from transistor transfer characteristics (Figure 2a). The independence of IDT-BT charge transport from longitudinal field is in contrast to early literature on organic semiconductors,[23–25] which reported an exponential dependence of mobility on longitudinal field attributed to structural and energetic disorder. This feature of IDT-BT is likely to arise from its nearly disorder-free transport.[19]

Mobility being independent from longitudinal field, the nonlinearity of the transistor output characteristics arises solely from longitudinal-field-dependent contact effects. Therefore, it is possible to extract the contact resistance of a given low-voltage pristine IDT-BT transistor directly from its output characteristics (SI 2). The contact resistance as a function of V_{DS} obtained from such analysis (Figure 3b) is an exponentially decreasing function of V_{DS} (consistently with gFPP measurements), its value being halved as V_{DS}

approaches $-0.4\ V$. To extend the range of this analysis to higher longitudinal field strength, high-voltage devices are to be considered (SI 2). Interestingly, contact resistance extracted from the latter follows a similar exponential trend, with nearly overlapping values at intermediate field. Remarkably, at $V_{DS} = -5\ V$ (i.e., the maximum V_{DS} applied to the devices in Figure 2b), contact resistance has dropped by two orders of magnitude.

The analysis above shows that the poor performance of low-voltage pristine IDT-BT transistors can be traced to the longitudinal-field dependence of their contact resistance. In fact, their charge transport behaviour is unaffected by the reduced longitudinal field characteristic of low-voltage operation. Their contact resistance, instead, increases by orders of magnitude, resulting in extremely low apparent mobility. While the high-voltage counterpart shares the same contact issues, it can rely on a much higher longitudinal field to overcome them, allowing its excellent charge transport properties to emerge.

The loss of performance of low-voltage pristine IDT-BT devices can be overcome by incorporating small molecule additives, such as F4-TCNQ and TCNQ (Figure 1b), into the IDT-BT film. The resulting devices are referred to as IDT-BT/additive transistors in the following. The incorporation of F4-TCNQ gives high-performance low-voltage devices capable of operating at below 3 V (Figure 2d,e). Similar results are obtained for IDT-BT/TCNQ (SI 3), hence the effect is not related to residual p-type charge-transfer doping, which does occur only with F4-TCNQ but not with TCNQ.[26] The transfer characteristics of IDT-BT/additive devices exhibit near-ideal behaviour: mobility is nearly invariant of V_G and comparable to the high-voltage counterpart (Figure 2d,f); the linear and saturation mobilities are nearly overlapping (Figure 2d); the drain current is approximately linear at small V_{DS} (Figure 2e). TLM analysis shows that low-voltage IDT-BT/additive devices have three orders of magnitude lower contact resistance than pristine ones (Figure 3a). Furthermore, contact resistance is now independent of longitudinal field and well aligned with that of high-voltage IDT-BT/additive TFTs (Figure 3b).

These findings are consistent with the picture recently proposed by Nikolka, Nasrallah et al. regarding the improvement of operational device stability of high-mobility polymer semiconductors by additive incorporation: The additives fill nanometre size voids within the polymer film and prevent residual water molecules in the polymer film from creating trap states.[26] This picture is consistent with the improved low-voltage operation reported here: By reducing the water-related trap density in the bulk of the polymer film and at the active interface, the additives improve the charge transport through the polymer bulk that determines the contact resistance in our staggered devices. The level of trap reduction achieved via additive incorporation in the low-voltage devices can be estimated by considering the difference in threshold voltage between IDT-BT and IDT-BT/additive TFTs, i.e., $\Delta Q_{tr} \cong C_d \, \Delta V_T / t_S$. Here, Q_{tr} is the trapped charge density, V_T is the transistor threshold voltage, and t_S is the thickness of the semiconductor film. Referring to low-voltage devices at $V_{DS} = -0.5\,V$ (i.e., at a bias point where the impact is minimal of the longitudinal field on trapping and on charge density inhomogeneity in the active region), we estimate a reduction in trap density on the order of $5 \cdot 10^{17}\ cm^{-3}$ due to the incorporation of the additive. Finally, the more dramatic manifestation of trap reduction emerging from low-voltage IDT-BT/additive devices is clearly associated with the reduced longitudinal-field range they cover. In relation to this picture, our findings indicate the presence of field-assisted detrapping, which allows the exponential reduction of contact resistance with increasing longitudinal field.

In order to assess the suitability of low-voltage p-type IDT-BT/additive transistors for flexible electronics, we pursued their integration with solution-processed n-type Indium-Zinc Oxide (IZO) transistors on plastic foil (as depicted in SI 4 and detailed in the Experimental Section). This choice of technologies reflects the generally superior performance of complementary circuits over unipolar ones and the demonstrated strength of hybrid organic/metal-oxide technologies.[27,28] In fact, our route to low-voltage IDT-BT transistors by additive incorporation proves suitable for circuit integration on foil, as evidenced by the

characteristics in **Figure 4**b measured from 10 integrated devices. They are hardly distinguishable from one another, denoting an extremely small spread. This is further confirmed by the histograms of their mobility and threshold voltage (Figure 4c): μ_{sat} is narrowly distributed at 0.5-0.6 $cm^2 V^{-1} s^{-1}$ and V_T is at around $-0.6\ V$. Being within a factor of 2 from the IZO counterpart (SI 4), this performance level is suitable for complementary hybrid integration.

We used our complementary integration platform to realise two-stage differential amplifiers, namely analogue circuit blocks capable of amplifying differential signals while suppressing common-mode noise and interference. These are relevant to a host of signal-conditioning applications, e.g. smart-sensor systems. The circuit topology is illustrated in **Figure 5**b and includes two stages: the first comprises a p-channel differential pair with n-channel current-mirror load; the second is an active-load common-source stage (SI 5).

Voltage transfer characteristics (VTCs) of the two-stage differential amplifier at various supply voltages are shown in Figure 5d. The VTCs reflect the amplifier's capability to operate at a power supply voltage as low as 5 V. Our differential amplifiers can be powered with a battery, as, in fact, we were successful in demonstrating using a single PP3 battery (Figure 5c). Moreover, the amplifiers possess a near rail-to-rail output voltage swing, always saturating at less than 1 V from the supply rails. This is fundamental to ensure the applicability of the amplifiers to battery-powered applications. Below 5 V the amplifier fails to operate. This is easily understood by considering that the longest path between the power rails contains three transistors, and that each of them takes up 1.5-2 V across. To the best of our knowledge, this work achieves the lowest supply voltage (i.e., 5 V) ever reported for a complementary differential amplifier realised with solution-processed organic semiconductors (SI 6). In fact, previous reports feature power supply voltages greater than 20 V.[29–32] In particular, the challenge of realising low-voltage complementary differential amplifiers with solution-processed organic semiconductors has been due to the performance limitations of n-

type organic materials, which involve threshold voltages of 18 V even in their best realization within a solution-processed differential amplifier circuit.[30,31] Moreover, while metal-oxide-only differential amplifiers reported to date are capable of operating down to power supply values in the 5–10 V range, they rely on unipolar architectures, which generally afford lower circuit performance.[33–36]

The differential gain of the two-stage differential amplifier, shown in Figure 5e is as high as 233 V/V with a 5 V power supply value, reaching values in excess of 1000 V / V (i.e., in excess of 60 dB) for $V_{DD} \geq 8\,V$. To the best of our knowledge, these differential gain values are the highest reported for two-stage organic or metal-oxide differential amplifiers (SI 6).[30–32,34,35,37,38] High voltage gain values are indeed essential for a differential amplifier to be used as a quasi-ideal gain block in a negative feedback circuit (e.g., as an operational amplifier), namely to obtain minimal input error voltage and closed-loop gain error.[39]

In view of their potential relevance to portable electronics, we analysed of the power consumption of our two-stage differential amplifiers. The quiescent power consumption at maximum gain is an increasing function of the power supply voltage (Figure 5f). This holds both for the overall amplifiers and their component stages, and evidences that higher power supply values allow greater gain at the price of increased power dissipation. The two-stage differential amplifiers are capable of a voltage gain over 40 dB while consuming 11 μW (at $V_{DD} = 5\,V$). A comparison with literature values for similar circuits (two-stage solution-based differential amplifiers) shows that, to the best of our knowledge, the power dissipation of our amplifiers is at least a factor of 3 lower (see SI 6).[30–32,38] This is a direct result of their dramatic reduction in power supply voltage.

The amplifiers provide a differential input resistance in the range of 0.5–1.0 · 10^8 Ω (SI 7). Such values are higher than those of many general-purpose silicon BJT operation amplifiers,[39] and confirm that our amplifiers can be coupled to a host of signal sources without signal loss. In actuality, the excellent insulating properties of our polymer gate

dielectric stack could allow much higher input resistance values, in the range of silicon FET operational amplifiers, with further optimisation of the gate electrode geometry (SI 7).

Finally, the operational stability of the amplifiers was evaluated in two configurations: a) after a 24h-long period inclusive of stress, and b) under continuous cycling of its input voltage. A first assessment of the amplifier's stability was conducted by monitoring its VTCs and the total current consumption at maximum gain over a period of 24 h. During an extensive portion of this time (7 h), the circuit was subjected to DC testing, namely its input voltage was swept for VTC characterisation (along similar lines as in the inset of **Figure 6**c), with power supply voltages in the 5-10 V range. For the remainder of this experiment, the amplifier was left unpowered. This stress condition is relevant to operation in real-world applications, which often involve alternating ON and OFF times. The VTCs in Figure 6a were obtained from one such experiment. The characteristics acquired at the end of the experiment are nearly overlapping with the initial ones, denoting satisfactory stability. Moreover, the total current consumption (sum of I_{BIAS1}, I_{BIAS2}, and of the current through the auxiliary circuits, as detailed in SI 5) in the steep segment of the amplifier's VTCs was also monitored in this stress configuration (Figure 6b). The total current here is primarily set by the IDT-BT transistors, which serve as current sources in the circuit. Over this stress experiment, the total current at all power supply voltages is stable within approximately 1% of its value. This is consistent with the exceptional stability reported for high-voltage IDT-BT/additive TFTs.[26]

Additionally, the bias stress behaviour of our amplifiers was captured dynamically under repeated cycling of its inverting input voltage. Specifically, Figure 6c shows the two-stage amplifier's VTCs acquired at discrete points in time while the amplifier is powered up ($V_{DD} = 7\ V$) and the inverting input terminal is cycled as detailed in the inset. This is a demanding stress condition, as it involves driving the transistors between their ON and OFF regions, and subjecting them to a V_{GS} and a V_{DS} approaching V_{DD}. This is in contrast to the normal region of operation of an amplifier (corresponding to the steep segment of its VTCs),

within which the transistors are driven at much smaller V_{GS} ($\approx V_{DD}/3$). The amplifier's VTCs measured during the stress conditions of Figure 6c are hardly distinguishable from one another. A closer look indicates the occurrence of a minor ($\approx$ 1% of V_{DD}) reduction of the output swing and a small shift of the input voltage at maximum gain. These shifts all saturate within the duration of the stress experiment, indicating promising operational stability. We note that these measurements were carried out on unencapsulated circuits in nitrogen atmosphere, hence more rigorous stability assessment will be needed to characterise the behaviour under ambient conditions and to determine the level of encapsulation required for particular applications. However, the performance and stability results reported here are encouraging and suggest that solution-processed differential amplifiers are approaching the requirements for smart-sensor applications.

Our work provides experimental evidence that the combination of high-k gate dielectrics with an additive-based trap-reduction technique enables the fabrication of low-voltage high-mobility polymer TFTs suitable for flexible electronics. The order-of-magnitude longitudinal-field reduction entailed by low-voltage operation leads to compromised performance in pristine IDT-BT devices. In fact, we show that a mere enhancement of the gate-to-channel capacitive coupling may not be sufficient for low-voltage operation, particularly when bulk trapping compromises contact properties, such as in IDT-BT. The incorporation of a suitable small molecule additive into the polymer semiconductor film reduces bulk trapping and leads to dramatically improved contact properties, enabling high-performance low-voltage polymer transistors. This approach allows us to achieve p-type polymer TFTs with sufficiently ideal and robust device characteristics for circuit integration. We exemplify this capability by demonstrating two-stage analogue differential amplifiers on foil also comprising solution-processed amorphous oxide TFTs. This prototypical circuit block is capable of operating down to a battery-compatible power supply voltage of 5 V with power dissipation of 11 μW, and attains a voltage gain above 60 dB at a power supply voltage

below 8 V. To the best of our knowledge, these figures constitute the highest gain,[29–32,38,40–43] the lowest operating voltage, [29–32,38,40–43] and the lowest power dissipation[29–32,38] for such type of circuit realised with solution-processed semiconductors, giving a further powerful demonstration of the excellent low-voltage performance of additive-treated polymer semiconductors. Our work constitutes an important milestone in realising low-voltage polymer transistors, and is readily applicable to demanding solution-processed analogue circuits that meet performance and power-dissipation requirements for a range of battery-powered smart-sensing applications in healthcare, environmental monitoring, smart packaging, and wearable electronics.

Experimental Section

Plastic Substrates: Plastic substrates were spun (1500 rpm) from a polyimide resin (PI-2555 HD Microsystems) to a thickness of 3.8 μm on a rigid carrier (glass slide or silicon chip). After curing (280 ^{0}C in N_2 atmosphere), they were passivated with 25 nm-thick sputtered SiN_x.

Source and Drain Electrodes: Source and drain electrodes—Cr(2nm)/Au(12nm)–were thermally evaporated and photolithographically patterned (bilayer lift-off processing via MicroChem LOR 5B and Shipley S1813 resists) to a channel length of 10 μm.

IZO Films: 42 mg of Indium(III) nitrate hydrate (Sigma-Aldrich, 99.999 % metals basis) and 18 mg of Zinc nitrate hexahydrate (Alfa Aesar, 99.998 % metals basis) were mixed in 1 mL of deionised water. After spin coating (5000 rpm), the samples underwent a 2 h annealing step at 275 ^{0}C in air, and were subsequently patterned as described in Ref. 26. A 1h annealing step at 180 ^{0}C in N_2 followed.

IDT-BT Films: IDT-BT was dissolved in 1,2-dichlorobenzene:chloroform (3 : 1) to a concentration of 10 g L^{-1}. When F4-TCNQ or TCNQ was added, it amounted to 10 % (by

weight) of the dissolved IDT-BT. Spin coating was carried out at 3000 rpm, followed by an annealing step at 90 ^{0}C for as long as 1 h. All steps were carried out in N_2.

Gate Dielectric: The gate dielectric stack of low-voltage devices comprises a 25 nm-thick CYTOP® film and a 210 nm-thick P(VDF-TrFE-CFE) film. The CYTOP® film was deposited by spin coating a dilute CYTOP® solution (1 : 5 in proprietary solvent, 5000rpm), followed by a 5 min annealing step at 90 ^{0}C. Subsequently, a 1 nm-thick AlOx wetting layer was deposited by thermal evaporation, followed by the spin coating of the P(VDF-TrFE-CFE) solution (40 g L^{-1} in n-butyl acetate, 1500rpm). Then the sample was kept on a hotplate at 60^{0}C for 2 h. The high-voltage devices have a gate dielectric consisting of a 500 nm-thick CYTOP® film, spun from a dilute CYTOP® solution (3 : 1 in proprietary solvent, 2000 rpm), followed by a 20 min annealing step at 90 ^{0}C.

Gate Metallisation and Interconnects: Gate electrodes (Al (30 nm)) and interconnects (Al (130 nm)) were fabricated by shadow mask evaporation.

Via-Hole Fabrication: Via holes were realised by mechanical hole punching through the gate dielectric stack with SE-20TB tungsten needles (Signatone Inc.).

IDT-BT Transistors and gFPP Devices: After patterning source and drain electrodes, an IDT-BT film was deposited, followed by the gate dielectric stack. Finally, the gate metal was evaporated. gFPP devices were fabricated similarly. They differ only in the following: a) they comprise two voltage probes in contact with the channel, each $L/4$ away from the nearest injecting electrodes (i.e., source and drain); their source-to-drain distance L amounted to $240\ \mu m$ and the channel width was $W = 80\ \mu m$; their semiconductor was patterned by O_2 plasma, according to the physical delamination procedure developed by Chang et al.[44]

Integrated Transistors and Circuits: After depositing the plastic substrate on a rigid carrier, source and drain electrodes were patterned. Prior to IZO deposition, the plastic substrate

underwent O_2-plasma treatment (180 W for 10 min). Following IZO patterning, the sample was subjected to a hydrophobic surface treatment (CYTOP® 1 : 20 in its proprietary solvent, spun at 8000 rpm to a thickness of 7 nm). Afterwards, the sample underwent O_2-plasma (300 W for 30 s) through a suitable shadow mask, allowing the removal of the hydrophobic treatment from the substrate regions intended for p-type transistors. Subsequently, IDT-BT was deposited by spin coating and patterned by dewetting. Finally, the gate dielectric stack and the gate metal were deposited, the necessary via holes fabricated, and the interconnects deposited.

Electrical Characterisation: Current-voltage characterisation of TFTs, gFPP devices, and circuits was performed at room temperature in an N_2 glovebox (via an HP4155C Semiconductor Parameter Analyser or an Agilent B1500A Semiconductor Device Analyser). Apparent mobility values were extracted from TFT characteristics as $\mu_{sat} = 2\left(\partial\sqrt{I_D}/\partial V_{GS}\right)^2/(C_d\ W/L)$ and $\mu_{lin} = (\partial I_D/\partial V_{GS})/(C_d\, W/L\ V_{DS})$.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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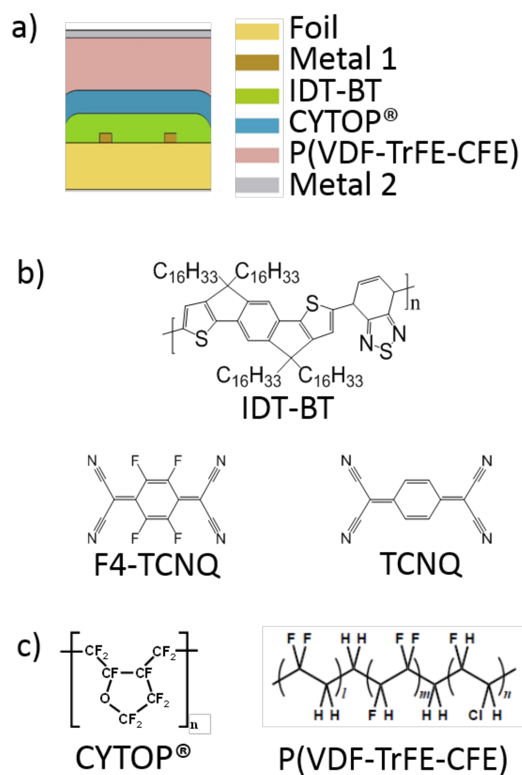

Figure 1. Low-voltage IDT-BT transistors: g) cross-sectional view; h) chemical structures of the materials used as semiconductor and additives; i) materials in the gate dielectric stack.

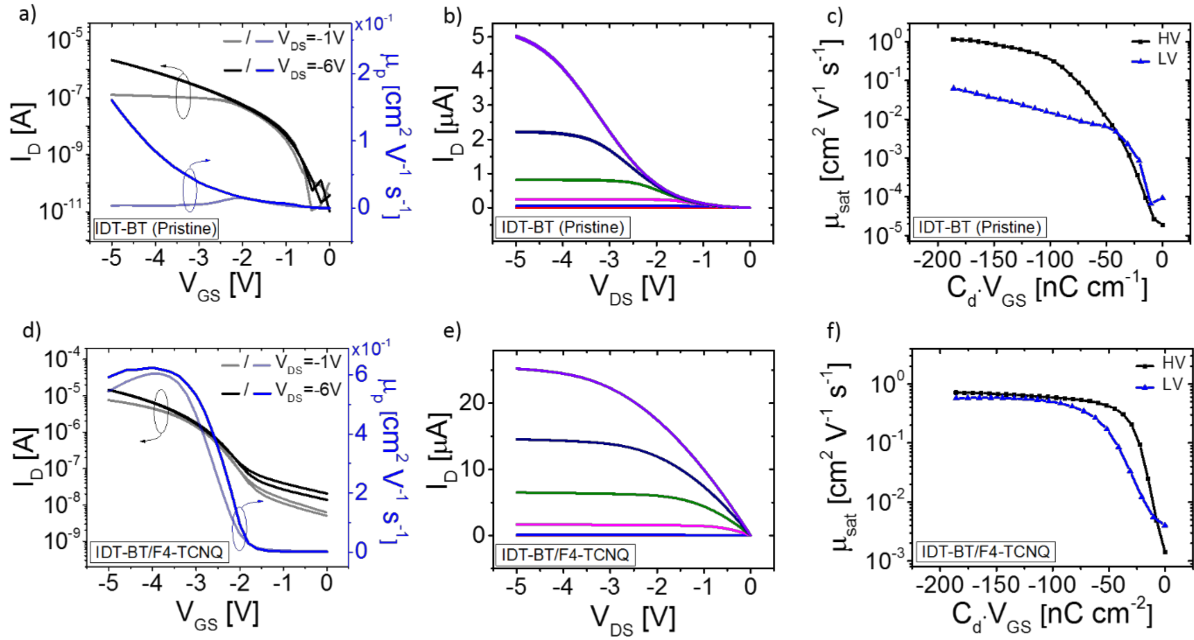

Figure 2. Low-voltage IDT-BT transistors: pristine IDT-BT versus IDT-BT/additive. a) Transfer and b) output characteristics of a pristine IDT-BT low-voltage transistor and the equivalent d) transfer and e) output characteristics of an IDT-BT/F4-TCNQ transistor. Apparent saturation mobility extracted from $\partial\sqrt{I_{DS}}/\partial V_{GS}$ of c) pristine IDT-BT and f) IDT-BT/F4-TCNQ transistors, both low-voltage (LV) and high-voltage (HV). Operation in saturation for the high-voltage devices is ensured by $V_{SD} = 50\ V$, while $V_{SD} = 5\ V$ suffices for the low-voltage devices.

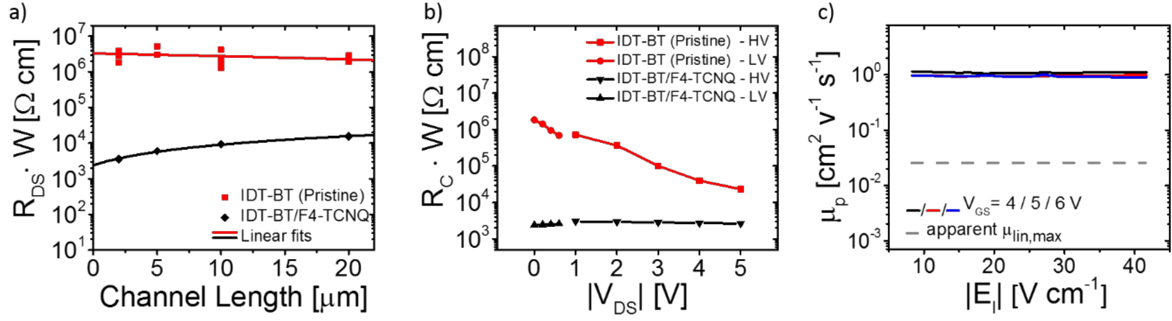

Figure 3. Contact resistance and actual mobility in IDT-BT devices. a) Drain-to-source resistance for $V_{DS} \to 0\ V$ as a function of channel length, obtained from pristine IDT-BT and IDT-BT/F4-TCNQ devices at $V_{GS} = -6\ V$ and plotted in semi-logarithmic scale (TLM analysis). b) Contact resistance of pristine IDT-BT and IDT-BT/F4-TCNQ low-voltage (LV) devices as a function of V_{DS} (calculated as in SI 2). Data points obtained from high-voltage (HV) devices are also shown (conventional TLM was used in this case). c) Actual (gFPP-derived) channel mobility as a function of longitudinal field (maximum apparent linear mobility extracted from $\partial I_D / \partial V_{GS}$ is also shown for the sake of comparison).

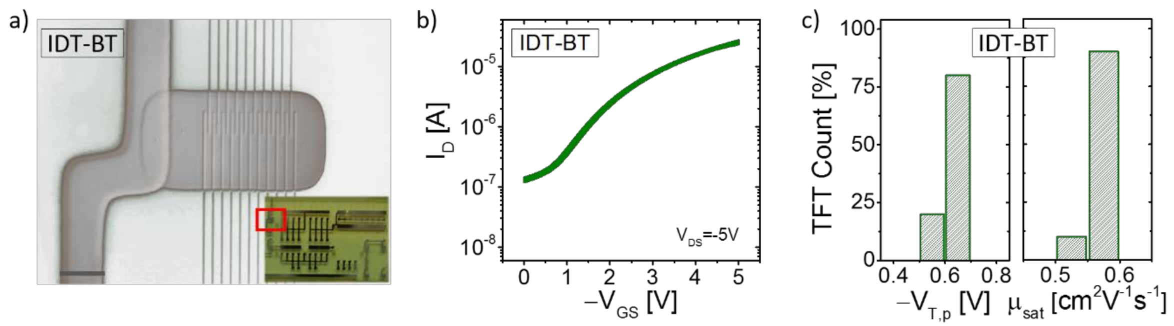

Figure 4. Integrated IDT-BT/F4-TCNQ transistors. a) Top view of an integrated IDT-BT transistor, fabricated as in SI 4. The scale bar corresponds to 200 μm, and the inset shows the device location on a two-stage amplifier foil. b) Transfer characteristics of 10 integrated low-voltage IDT-BT/F4-TCNQ TFTs ($W/L = 1mm/10\mu m$), and c) histograms of their threshold voltage and saturation mobility (left and right, respectively).

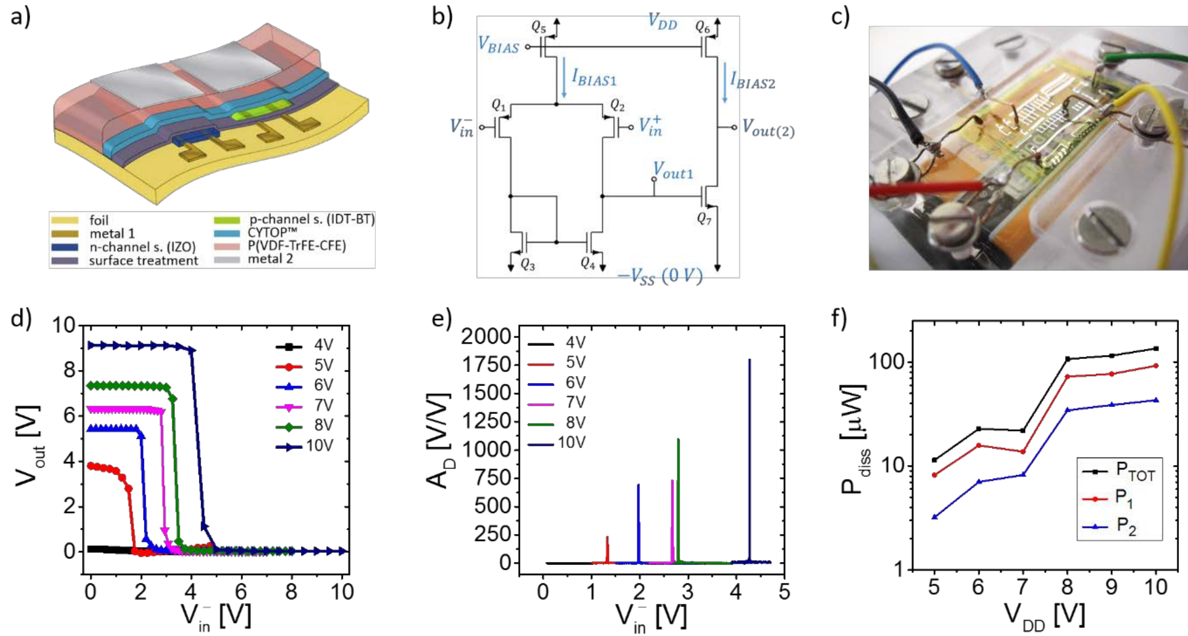

Figure 5. Hybrid solution-based two-stage complementary differential amplifier. a) Cross-sectional view of the integration platform. b) Basic circuit topology of differential amplifier. c) Amplifier biased by a PP3 battery. d) VTCs of an amplifier at variable V_{DD}, determined experimentally by sweeping the voltage of the inverting input terminal, the noninverting one being kept constant and at approximately $V_{DD}/2$. e) Differential gain at variable V_{DD}, extracted as $\partial V_{out(2)}/\partial V_{in}^-$. f) Power dissipation of a two-stage amplifier, P_{TOT}, and of its component stages, P_1 and P_2 (obtained from experimental values of I_{BIAS1} and I_{BIAS2}).

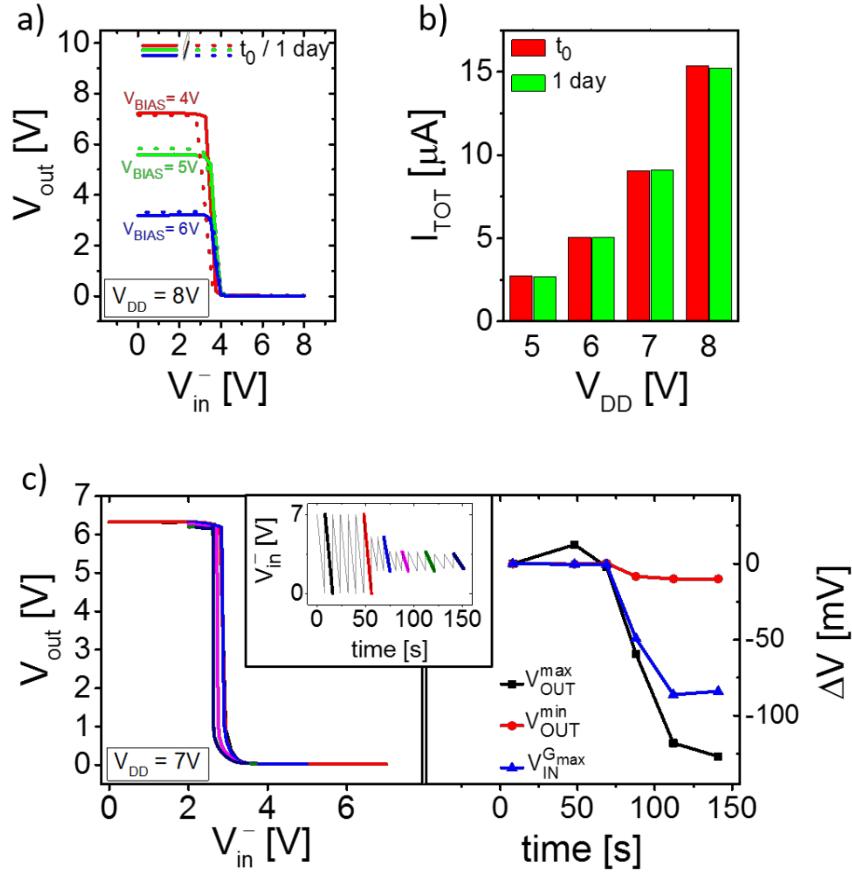

Figure 6. Stability of a solution-processed two-stage differential amplifier. a) and b) present the amplifier's behaviour over a 1 day experiment, comprising a period of 7 h of stress, during which the input voltage was repeatedly swept along similar lines as in the inset of c): a) amplifier's VTCs at V_{DD} = 8 V and at different values of V_{BIAS}, the solid traces referring to the start of the stability experiment and the dashed traces being acquired after 1 day; b) total bias current (sum of I_{BIAS1}, I_{BIAS2}, and the current through the auxiliary circuits) over the same experiment. c) VTCs at V_{DD} = 7 V (left) and under consecutive sweeps of V_{in}^{-} (as in the inset), and evolution of key parameters (right). The parameters are defined as follows: V_{OUT}^{min} and V_{OUT}^{max} are the minimum and maximum output voltage, respectively, and $V_{IN}^{G_{max}}$ is the input voltage at maximum gain.