An Efficient SSHI Interface with Increased Input Range for Piezoelectric Energy Harvesting Under Variable Conditions

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***Abstract*—Piezoelectric vibration energy harvesters have been widely researched and are increasingly employed for powering wireless sensor nodes. The Synchronized Switch Harvesting on Inductor (SSHI) circuit is one of the most efficient interfaces for piezoelectric vibration energy harvesters. However, the traditional incarnation of this circuit suffers from a significant start-up issue that limits operation in low and variable amplitude vibration environments. This paper addresses this start-up issue for the SSHI rectifier by proposing a new architecture with SSHI startup circuitry. The startup circuitry monitors if the SSHI circuit is operating correctly and re-starts the SSHI interface if required. The proposed circuit is comprehensively analyzed and experimentally validated through tests conducted by integrating a commercial piezoelectric vibration energy harvester with the new interface circuit designed in a $0.35\,\mu\mathrm{m}$ HV CMOS process. Compared to conventional SSHI rectifiers, the proposed circuit significantly decreases the required minimum input excitation amplitude before energy can be harvested, making it possible to extract energy over an increased excitation range.**

***Index Terms*—Energy harvesting, piezoelectric transducer, synchronized switch harvesting on inductor (SSHI), rectifier.**

I. Introduction

Along with the development of Internet of Everything, wireless sensing networks (WSN) are being developed to interconnect between the physical world and the Internet. In order to make these low-power devices fully self-sustained, there has been an emerging research interest on harvesting ambient vibration energy [1]–[3]. Piezoelectric transducers (PT) are widely used in vibration energy harvesters (VEH) as mechanical-to-electrical transducers due to their relatively high power density [4], scalability and compatibility with conventional integrated circuit technologies [5], [6]. A typical piezoelectric VEH can provide an power density of around 10 - 500 $\mu\mathrm{W}\cdot\mathrm{cm}^{-2}$, which sets a significant constraint on designing the associated power conditioning interface circuit [7], [8]. Full-bridge rectifiers are widely used in commercially available harvesters due to their simplicity and stability; however, they set high threshold voltages for the generated energy to be extracted by the circuit. While vibrating at or close to its resonance, a piezoelectric VEH can be modeled as a current source I_P connected in parallel with a plate capacitor C_P and a resistor R_P. Fig. 1 shows the full-bridge rectifier connected with a PT and the associated waveforms. From the figure, it can be seen that a significant amount of charge is wasted due to discharging and charging the internal capacitor C_P so that only a small fraction of charge can be transferred to C_S [9].

In order to improve the power efficiency and minimize the charge waste due to charging C_P, many active interface circuits have been reported [8], [10], including MPPT (maximum power point tracking) [11], [12], synchronous electric charge extraction (SECE) [13]–[16], etc. Among all interface circuits for piezoelectric VEH, the SSHI (Synchronized Switch Harvesting on Inductor) rectifier [17] is one of the most energy-efficient circuits with ideally no charge wastage. The SSHI circuit performs charge inversion on C_P through an RLC system controlled by synchronized switches. Successful on-chip implementations of SSHI (bias-flip) interface circuits has been previously described and demonstrated by Ramadass [18] and by Aktakka [19]. Fig. 2 shows the SSHI interface circuit and its associated waveforms. At each zero-crossing point of I_P, the switches are synchronously closed for a short period of time to invert the charge on C_P from $-(V_S + 2V_D)$ to $(V_S+2V_D)-V_{TH}$, where V_{TH} represents the energy loss due to the resistance of the RLC network and $V_{piezo} = V_P - V_N$ is the voltage across the PT. Despite the performance of the SSHI rectifier, a startup issue exists which may prevent the system from commencing operation and no energy can be extracted as a result. In Section II, the conventional SSHI rectifier is modeled and the startup issue is addressed with theoretical calculations and simulations. Section III presents an overall view of the proposed SSHI rectifier. The detailed circuit implementations are presented in Section IV and the simulation results in Section V. Section VI shows the measured results and a conclusion is given in the last section.

II. Modeling

In a conventional SSHI circuit, the switches controlling the inductor (see Fig. 2) are synchronously turned ON to invert the voltage on C_P while I_P crosses zero. When I_P is close to zero, the diodes of the full-bridge rectifier are just about to turn OFF. At this instant, one of V_P and V_N is close to $-V_D$ and the other one is close to $V_S + V_D$. One method to detect the zero-crossing of I_P is to compare either V_P or V_N (depending on the sign of V_{piezo}) with a reference voltage V_{ref} using continuous-time comparators [20]. The reference

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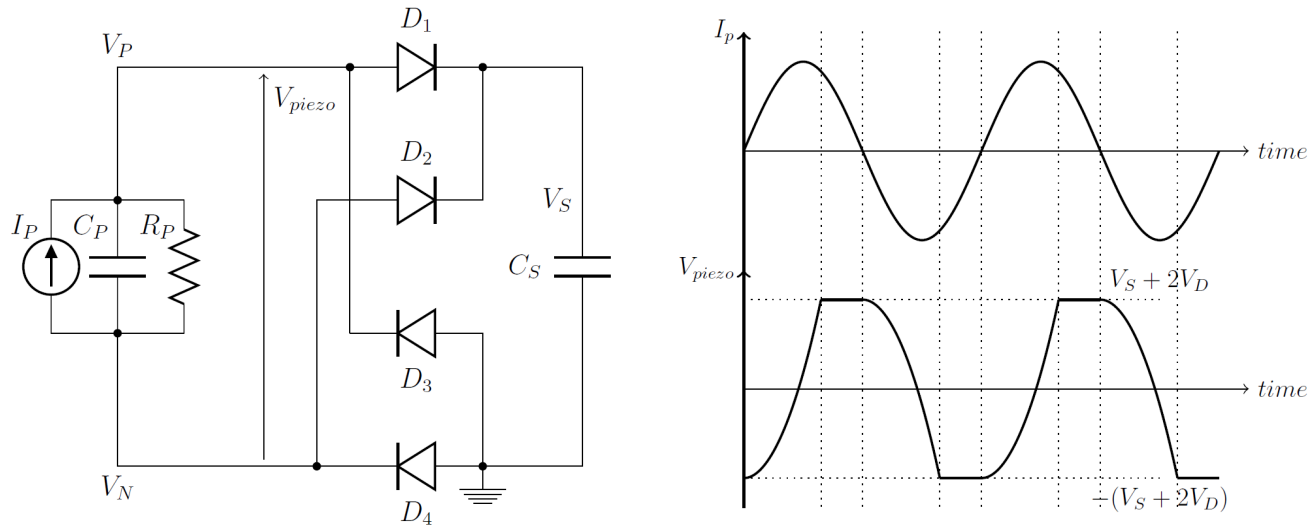
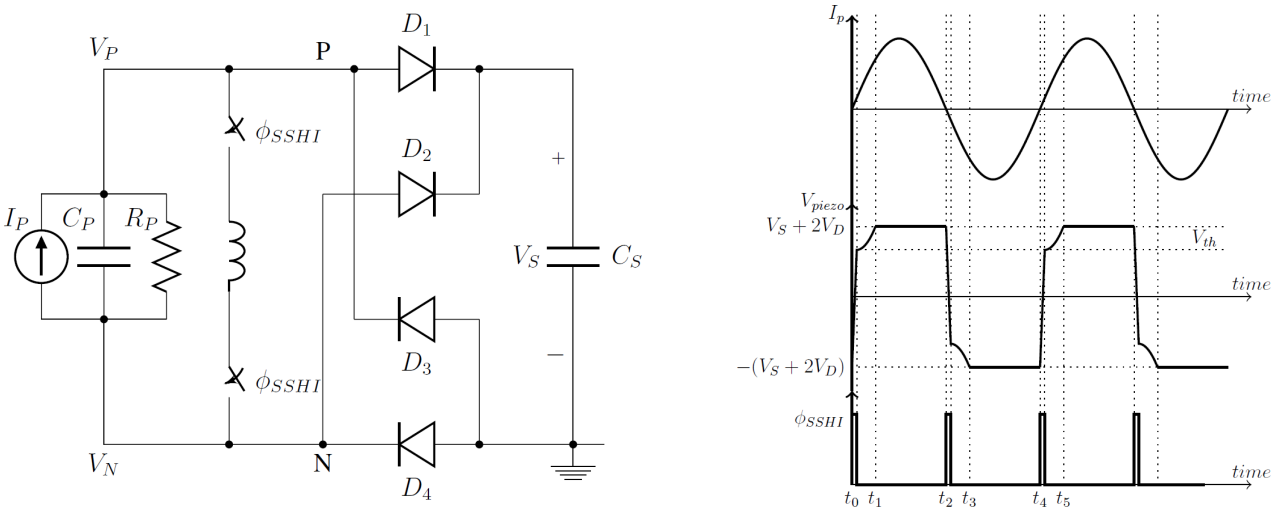


(a) The equivalent circuit of a piezoelectric VEH connected to a full-bridge rectifier.

(b) Representative waveforms for the current (I_P) and voltage (V_{piezo}).

Fig. 1: Full-bridge rectifier for piezoelectric VEH and the associated waveforms.



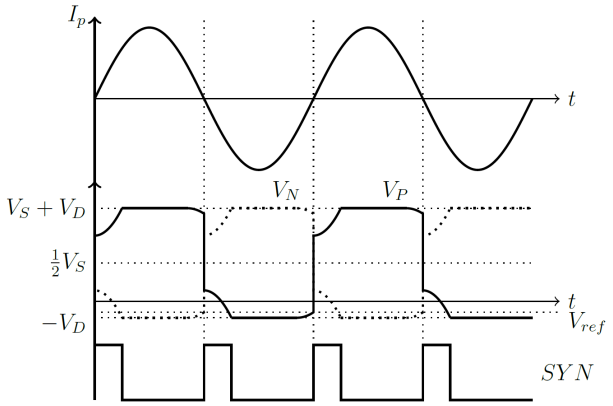
(a) SSHI interface circuit.

(b) Associated waveform.

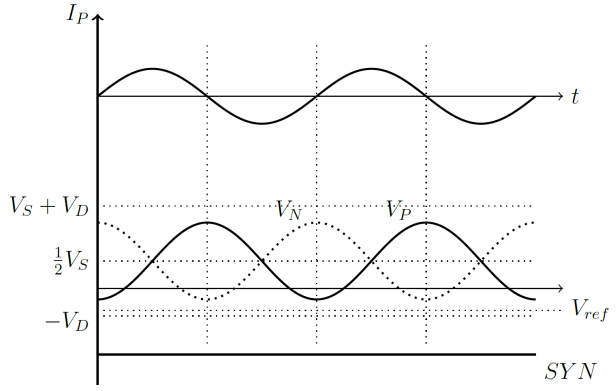
Fig. 2: SSHI interface and the associated waveforms.

voltage V_{ref} is set slightly higher than the negative value of the voltage drop of the diodes ($-V_D$). Fig. 3a shows the waveforms while the SSHI circuit is operating properly, where SYN is the synchronous signal used to generate the switching signal ϕ_{SSHI}. For each I_P zero-current point, a rising edge is generated in SYN. The condition for generating the rising edge is that either V_P or V_N should go below V_{ref} attaining $-V_D$. If the excitation input is too small to make V_P or V_N attain $-V_D$, SYN will stay high and no synchronous rising edge can be generated, as illustrated in Fig. 3b. In this case, the switches in the SSHI circuit are kept open and no energy can be extracted.

For no or very weak input excitation, both of V_P and V_N are equal to $\frac{1}{2}V_S$ or oscillate around this voltage. This is because the high and low limits of these two voltages are $V_S + V_D$ and $-V_D$. If the four diodes match with same voltage drop, the value of V_P and V_N will approximate the middle balance voltage $\frac{(V_S+V_D)+(-V_D)}{2} = \frac{1}{2}V_S$. If there is a mismatch for the diodes, this balance voltage may be shifted a bit but this effect can be partially absorbed by the mismatch of other diodes. As a result, some, or even most, of effect contributing to shift the balance voltage is canceled. In this implementation, the diodes are carefully selected and experimentally measured for minimal mismatch. Hence the balance voltage for V_P and V_N should be very close to $\frac{1}{2}V_S$. Noting $V_{pp(open)}$ is the peak-to-peak voltage of V_{piezo} ($V_{piezo} = V_P - V_N$) while the piezoelectric transducer (PT) is in open-circuit , so $V_{pp(open)}$ needs to be greater than $2(V_S + 2V_D)$ in order to make V_P (or V_N) attain $-V_D$ to trigger the comparators and to start generating the synchronous signal SYN. Therefore, the condition to start SSHI circuits is:



(a) Waveforms while SSHI is operating properly.



(b) Waveforms while SSHI is not operating.

Fig. 3: Associated waveforms of SSHI interface while the circuit is operating properly and not operating.

$$V_{pp(open)} > 2(V_S + 2V_D) \tag{1}$$

This is also the condition for a full-bridge rectifier to start transferring energy. While flipping the voltage V_{piezo} at each zero-crossing moment, there is an electrical damping in the RLC loop due to the resistance. Assuming the voltage V_{piezo} is flip from $V_S + 2V_D$ towards $-(V_S + 2V_D)$, the damped expression of V_{piezo} is: $V_{piezo} = (V_S + 2V_D)e^{\frac{t}{\tau}} \sin(2\pi f_0 t)$, where $\tau = 2L/R$ and $f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{\tau^2}}$. After a half pseudo-period where $t = \frac{1}{2f_0}$, the resulting V_{piezo} equals to $-(V_S+2V_D)e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}}$. Hence the voltage loss V_{TH} due to flipping (illustrated in Fig. 2b) can be expressed as:

$$V_{TH} = (V_S + 2V_D)(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}}) \tag{2}$$

Besides the electrical damping calculated above, synchronized current generated to flip V_{piezo} in the SSHI circuit produces an electrical actuation that opposes the vibration, which increases the effective damping of the mechanical system. This effect is known as Synchronized Switch Damping (SSD) [21], [22]. SSD can significantly affect the mechanical vibration for strongly-coupled piezoelectric transducers; however this effect is limited or negligible for weakly-coupled PTs. Hence, the SSD effect has not been considered here and is assumed to be negligible. According to the voltage loss in (2), in order to make V_P (or V_N) attain $-V_D$ to keep the SSHI circuit operating after the charge inversion, the open-circuit peak-to-peak voltage of V_{piezo} should be greater than V_{TH}. Therefore, the condition to maintain operation is:

$$V_{pp(open)} > V_{TH} \tag{3}$$

After comparing the two threshold voltages in (1) and (3), the condition for starting the SSHI circuit is usually much more difficult to be satisfied than the condition for keeping it working while it is already operating. In real-world implementations, the ambient vibration is unpredictable and periods corresponding to no input vibration (or very small vibrations that cannot satisfy the condition in (3)) are very likely to occur. Therefore, once an SSHI circuit stops operating, the minimal excitation requirement for the circuit to extract energy is increased from (3) to (1), which means the input excitation needs to overcome a much higher threshold to start the circuit.

Fig. 4 shows the simulated waveforms to illustrate how the SSHI circuit fails to restart after a period of weak excitation. The signal I_P (top) represents the input excitation amplitude and it is expressed as $I_P = I_0 \sin \omega t$, where the I_0 values corresponding to different periods of time are shown above the signal. V_{piezo} ($V_{piezo} = V_P - V_N$) is the voltage across the PT and V_P and V_N are the voltage at the two electrodes of the PT. SYN is the synchronous signal to invert the voltage across the PT and ϕ_{SSHI} is the synchronous switch signal generated from SYN to flip V_{piezo}. Before t_1 in the figure, an excitation level at $I_0 = 230\,\mu\text{A}$ makes the SSHI operate properly with the signal SYN generated correctly. Between t_1 and t_2, the excitation is decreased to a value such that the condition in (3) is marginally satisfied. During this time, SYN can still be generated and V_{piezo} can be properly inverted. After t_2, the excitation input is further decreased to a near-zero value to simulate the condition for very week excitation, so that the SSHI circuit cannot maintain operation. In this case, the synchronous signal SYN maintains a high level. As the charge on the internal capacitor C_P of the PT cannot be inverted, the remaining charge on C_P diminishes due to the internal leakage. As a result, V_P and V_N tend towards $\frac{1}{2}V_S$ and V_{piezo} tend towards zero, where V_S is set to 3 V in the simulation. From t_3 the excitation input is gradually increased to $I_0 = 100\,\mu\text{A}$, $150\,\mu\text{A}$, $200\,\mu\text{A}$ and $250\,\mu\text{A}$. When the excitation is increased to a level much higher than $90\,\mu\text{A}$, the SSHI circuit cannot be restarted while both V_P and V_N are oscillating around $\frac{1}{2}V_S$ and they cannot attain $-V_D$. Although the excitation level of $I_0 = 90\,\mu\text{A}$ is sufficient to maintain the SSHI circuit (between t_1 and t_2), it cannot restart the SSHI, even at a higher value of $I_0 = 250\,\mu\text{A}$.

The simulation results show that the operational range of this SSHI rectifier implementation is limited as it requires high input excitation to be restarted. In the following sections of this paper, a new SSHI architecture is introduced, which is able restart the SSHI circuit when required to increase the

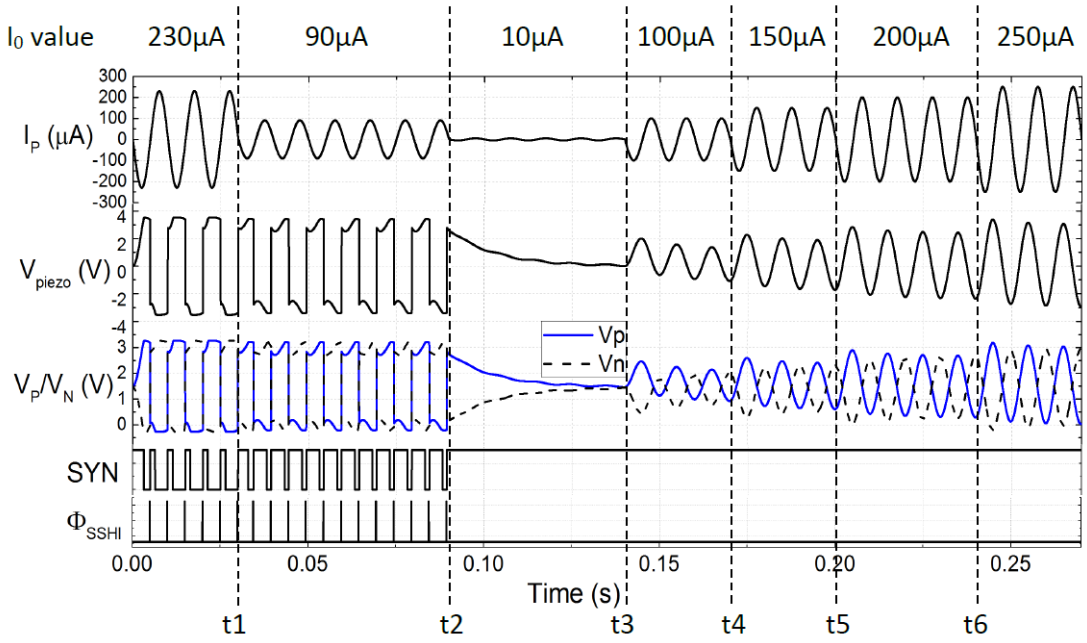


Fig. 4: Simulation waveforms showing the SSHI circuit fails to restart.

effective operational range.

III. Proposed Architecture

This section proposes an improved SSHI rectifier able to automatically restart the SSHI circuit while it is not working. Fig. 5 shows the block architecture of the proposed system containing a conventional SSHI rectifier and an SSHI startup circuitry. The synchronous signal SYN is generated from the "zero-crossing detector" block while a zero-crossing moment of I_P is detected. This signal is used in the conventional SSHI rectifier to flip the voltage across the PT and it is also used by the "SSHI working monitor" block to monitor if the SSHI interface is operating correctly. Once the SSHI circuit stops generating the SYN signal, the signal $WORKING$ goes low indicating that the SSHI is not operating now. A low $WORKING$ signal turns ON the power supply for the following "Excitation evaluation" block. This block aims to evaluate the input excitation because restarting the SSHI circuit is only needed if the input excitation is stable (not an instant shock) and the amplitude is high (the condition $V_{pp(open)} > V_{TH}$ is satisfied for the SSHI circuit being able to maintaining operating once started). If either of these two conditions are not met, the "excitation evaluation" block will not restart the SSHI circuit as it will stop working again after being restarted and the energy "invested" to restart is wasted. If this block determines that the SSHI circuit can be restarted under the given excitation, a signal $PRECHARGE$ will be generated to allow the "pre-charging" block to charge the PT to a voltage value sufficient to generate the SYN signal. Once SYN is generated, "SSHI working monitor" block reads this signal and send a high $WORKING$ signal to indicate that the SSHI circuitry is operating. Therefore, the following two blocks "excitation evaluation" and "pre-charging" are powered OFF to minimize power loss.

Using the proposed circuit, the threshold of starting an SSHI circuit is lowered from (1) to (3) and both thresholds depend on V_S. If the diodes are with zero voltage drop and V_S is high, say $4\,\mathrm{V}$, the threshold for conventional SSHI circuits ($V_{pp(open)} > 8\,\mathrm{V}$) is relatively hard to attain for some PTs implemented in low excitation environments. If a load device is present and continuously consumes the energy in C_S, weak excitation prevents the system from harvesting any energy and V_S keeps decreasing. Assuming V_S is decreased to $0.5\,\mathrm{V}$ after a long period of time without any input excitation, the threshold in (1) is lowered to $2V_S = 1\,\mathrm{V}$ and a conventional SSHI circuit can be started from a much lower threshold $V_{pp(open)} > 1\,\mathrm{V}$ (a stable power supply generated from this low V_S with a boost converter is assumed to be available). While conventional SSHI circuits becomes easier to be started, the same principle also applies to the proposed SSHI rectifier with startup circuitry, where the threshold in (3) is also significantly decreased to $V_{pp(open)} > V_S(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}})$, which can be around $0.2\,\mathrm{V} \sim 0.5\,\mathrm{V}$. Hence, the proposed circuit always shows an increased operational range for different V_S values although this improvement becomes less obvious for low V_S.

Besides giving a "kick" with the invested energy from the battery to start the SSHI circuit as proposed in this paper, another method is also possible by using a different means to detect zero-crossing points and flipping V_{piezo} until it exceeds $V_S + 2V_D$. For this method, detecting if the SSHI circuit can extract any energy from the PT is also useful (equivalent to "working" and "non-working" phases in this paper). This is because if the excitation is too small to meet the condition in (3), neither V_P nor V_N can attain $V_S + V_D$ or $-V_D$; hence repeatedly flipping V_{piezo} in this case will waste the energy used to drive the large W/L CMOS switches without any

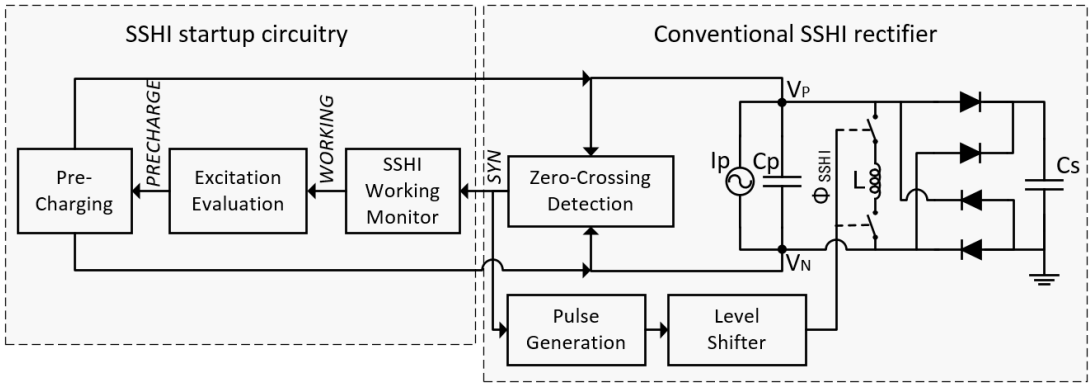


Fig. 5: System architecture of the proposed SSHI interface with self-startup circuitry.

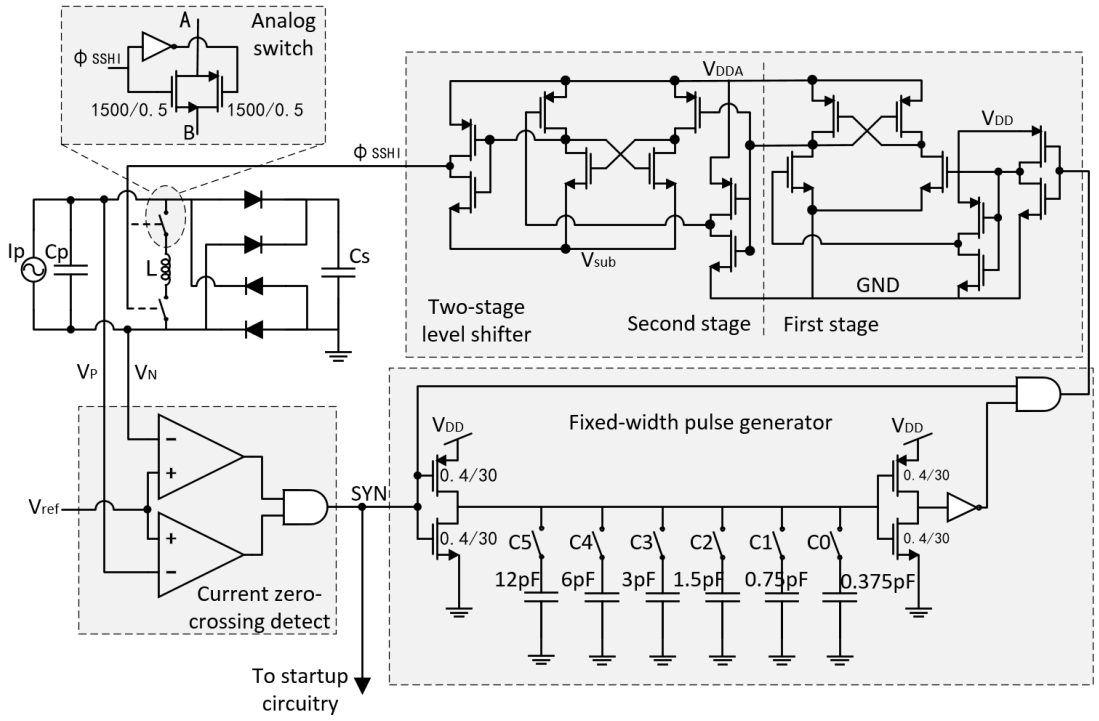


Fig. 6: Conventional SSHI rectifier.

energy harvested. In order to distinguish these two phases, additional blocks need to be designed, which add extra power consumption and complexity, while the proposed SSHI startup circuit can just use the SYN signal to do the same job. Distinguishing between "working" and "non-working" phases can not only decrease the chip power consumption in this case, but it also provides an important signal for the load electronics, such as a wireless sensor node, to indicate if any energy is being harvested. Therefore, the load electronics can dynamically manage the power consumption in the case of very low environmental vibration or no vibration.

Fig. 5 presents a block level diagram to describe the working principle of the entire system and the detailed transistor-level circuits for different blocks will be presented in the next section.

IV. Circuit implementation of the proposed SSHI circuit

This section describes the implementation of the self-startup SSHI rectifier as a CMOS circuit. As shown in the block diagram of Fig. 5, there are four main blocks in the proposed circuit: a conventional SSHI circuit, a working monitoring block, an excitation evaluation block and a pre-charging block. These blocks and the internal transistor-level circuit diagrams will be presented and explained in this section.

A. Conventional SSHI circuit

Fig. 6 shows the circuit diagram of the conventional SSHI rectifier. In order to find the current zero-crossing point of I_P, two continuous-time comparators are employed to compare V_P and V_N with a reference voltage V_{ref}, which is set slightly

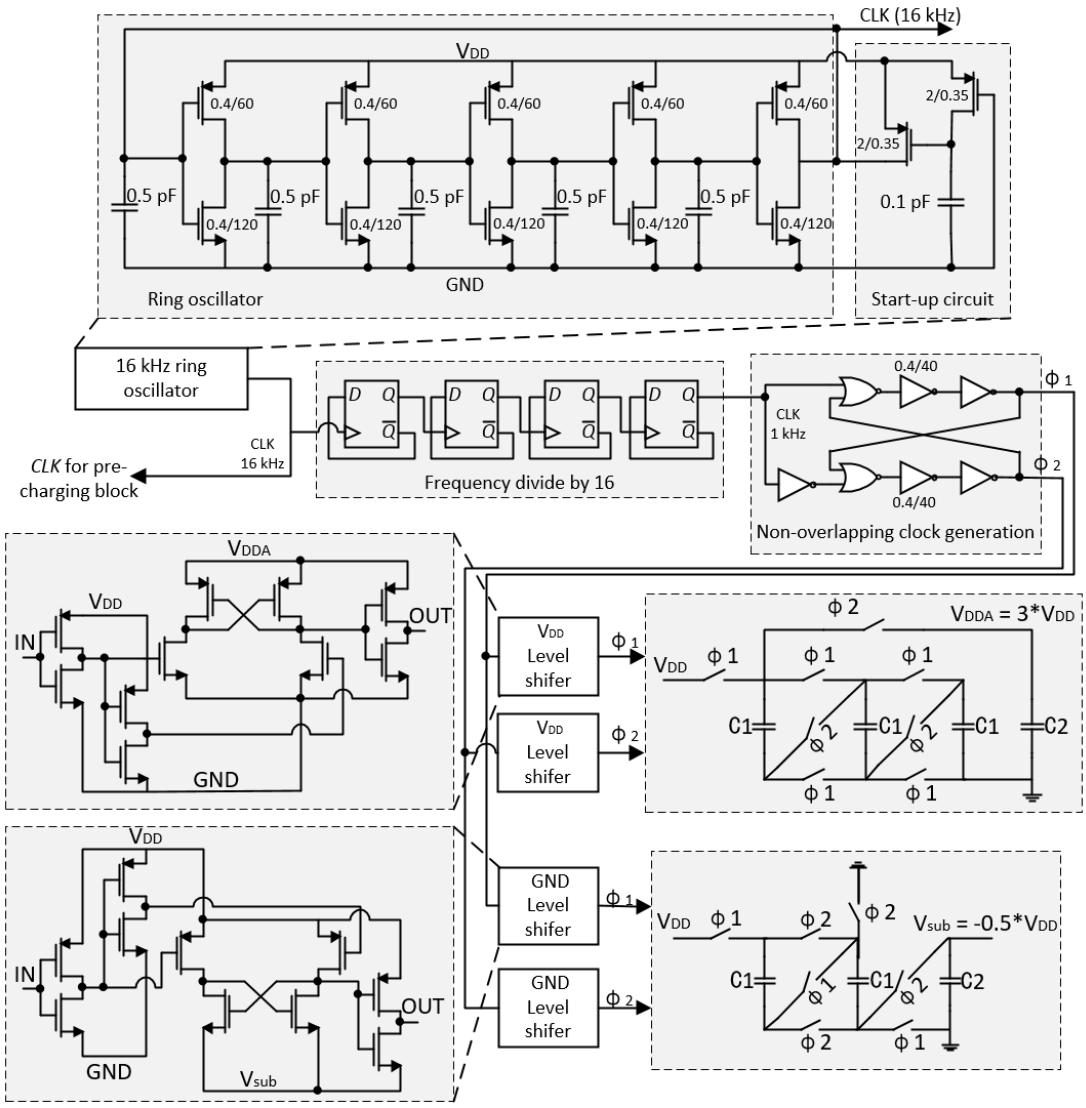


Fig. 7: Ring oscillator and DC-DC converters to generate gate over-driving voltage levels.

higher than $-V_D$. Details of this method to detect the zero-crossing point is explained in Section II. As $V_{ref} < 0\,\mathrm{V}$, the negative power supply of the comparators is connected to a negative voltage level in order to keep V_{ref} in the operational range of the comparators. In this paper, the comparators are powered with supplies of $-0.75\,\mathrm{V}$ and $1.5\,\mathrm{V}$. The signal SYN from the outputs of these two comparators is the synchronous clock signal having a rising edge at each I_P zero-crossing point. Each rising edge of SYN is used to generate a fixed-width pulse in the following delay block. The pulse width is adjusted to control the ON-time of the two switches of the inductor.

The fixed-width pulse generator aims to generate the fixed-width pulse signal from SYN. This pulse generator is a simple AND gate where the synchronous signal SYN is ANDed with the delayed and inverted version of SYN. The delay is performed using two weak inverters charging up capacitors, where the total capacitance is controlled by a 6-bit signal C[0:5]. The pulse width is adjustable over a wide range from $2\,\mu\mathrm{s}$ to $70\,\mu\mathrm{s}$ with resolution of $1.1\,\mu\mathrm{s}$, which is able to accommodate large inductors up to $2\,\mathrm{mH}$. The 6-bit delay control signal C[0:5] statically controls the width of the generated pulse equal to a half pseudo-period of the RLC oscillation system. In this implementation of the proposed SSHI rectifier, the 6-bit signal C[0:5] is set externally. For a given inductor (with inductance L) and a given PT (with internal capacitance C_P), the duration of putting the switches ON is fixed. Hence, before implementation, it is necessary to do a one-time calibration for the 6-bit signal C[0:5]. Although this static settling of flipping phase can be precisely tuned, possible unpredictable variation of the parameters of the PT due to fatigue (e.g. internal micro-cracks) during operation may change the internal capacitance C_P and make the static settling method invalid. Alternative auto-timing solutions presented in [19], [23] can be considered in future designs to dynamically settle the flipping phase.

The switch-controlling signal obtained from the delay block cannot be directly used for driving the two switches because different voltage levels are needed. The voltages of the two

sides of the switches are V_P and V_N, which vary over a wide range between $-V_D$ and V_S+V_D; however, the voltage levels of the pulse signal obtained from the delay block are $0\,\mathrm{V}$ and $1.5\,\mathrm{V}$ (the V_{DD} used in this implementation is $1.5\,\mathrm{V}$). In order to fully switch ON and OFF the two switches, the driving signal on the switches should have an ON voltage higher than $V_S + V_D$ and OFF voltage lower than $-V_D$. Assuming the voltage V_S does not go higher than $4\,\mathrm{V}$ and the energy stored on C_S will be transferred to a battery capacitor when V_S attains this threshold, so voltage levels of $-0.75\,\mathrm{V}$ and $4.5\,\mathrm{V}$ are suitable to fully drive the switches. For this reason, a level-up shifter is needed to shift the voltage level $0\,\mathrm{V}$ to $-0.75\,\mathrm{V}$ and $1.5\,\mathrm{V}$ to $4.5\,\mathrm{V}$. A two-stage level-up shifter is shown in the figure, which is able to shift the high level of the input signal to a higher voltage and the low level to a lower voltage. The different voltage levels shown in the figure are $GND = 0\,\mathrm{V}$, $V_{DD} = 1.5\,\mathrm{V}$, $V_{DDA} = 4.5\,\mathrm{V}$ and $V_{sub} = -0.75\,\mathrm{V}$. The first stage employs a cross-coupled PMOS load aims to shift logic voltage levels from [0 V, 1.5 V] to [0 V, 4.5 V]. The second stage employs a cross-coupled NMOS load to further shift logic levels from [0 V, 4.5 V] to [−0.75 V, 4.5 V].

In order to provide gate overdriving voltages V_{DDA} and V_{sub}, switched capacitor (SC) DC-DC converters are employed, which are driven by an internally generated clock signal. Fig. 7 shows the circuit diagrams to provide gate overdriving voltage levels and a clock signal for the other blocks. A $16\,\mathrm{kHz}$ clock is generated from a ring oscillator and its frequency is reduced to $1\,\mathrm{kHz}$ to drive the converters. The $1\,\mathrm{kHz}$ is then cross-coupled with its delayed inverted version with two NAND gates to generate two non-overlapping signals ϕ_1 and ϕ_2. These two clock signals are shifted with two different level shifters to drive the DC converters. Besides employing SC DC-DC converters, a higher supply (HS) circuit for V_{DDA} and a negative voltage converter (NVC) for V_{sub} are also good options as presented in [9]. As ring oscillators are normally power hungry and the one in this implementation consumes $260\,\mathrm{nW}$ power (other circuits in Fig. 7 consume additional $13\,\mathrm{nW}$), using HS and NVC circuits can decrease the power consumption to $96\,\mathrm{nW}$. However, the circuit in this work requires a clock signal to drive the counters in other blocks. Due to this reason, SC DC-DC converters only consumes $13\,\mathrm{nW}$ additional power while the HS and NVC circuits would consume more.

B. SSHI working monitoring block

In order to monitor the conventional SSHI circuit, the synchronous signal SYN is used in the "SSHI working monitoring" block, which is shown in Fig. 8. This block employs a 8-bit digital counter (two MSBs can be set externally and other bits are connected to V_{DD}) driven by an internally generated $1\,\mathrm{kHz}$ clock signal. The counting-down time of the counter is set several times longer than the longest period of the current source I_P. For this implementation, the PT has a natural frequency of $82\,\mathrm{Hz}$, hence the count is set to 128, which is approximately 10 times of the period of the PT. The counter can be reset by a low SYN, which represents one of the voltages V_P and V_N attains $-V_D$. Hence, while the SSHI

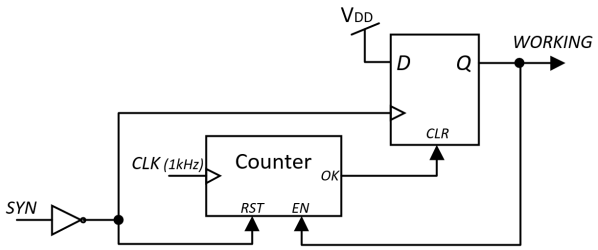


Fig. 8: Circuit diagram of SSHI working monitoring block.

circuit is working and the signal SYN is generated correctly, the counter can be reset at each zero-crossing point of I_P. While the SSHI circuit stops working, the signal SYN will keep at high level. As a result, the counter cannot be reset until it finishes counting and sends a reset signal to the D-flip-flop so that the signal $WORKING$ goes to low level indicating that the SSHI circuit is not working. While the SSHI is not working, the $\overline{WORKING}$ also disables and resets the counter to initialize it for the next time when the SSHI restarts operation. During the non-working state, once the signal SYN can be generated correctly, the output of the D-flip-flop takes the value of the input V_{DD} so that $WORKING$ goes to high level. Based on the signal $WORKING$, the following blocks can be cut off from power while the SSHI is working to decrease power loss.

C. Excitation evaluation block

When the signal $WORKING$ is low, the system goes to "non-working" state and it tries to restart the SSHI circuit; however, the system needs first to evaluate whether the startup is rewarding. If the excitation is just a weak impulse (producing a weak vibration attenuating to zero) or it is stable (not an impulse) but not high enough to maintain the operation of the SSHI circuit, restarting is not rewarding because the circuit will stop operating shortly after it is restarted and the invested energy is completely wasted. It should be mentioned that if the excitation levels in these two cases satisfy $V_{pp(open)} > 2(V_S + 2V_D)$, the SSHI startup circuitry will not be used and the SSHI circuit will be automatically started. Hence, for restarting the circuit in low excitation levels, an "excitation evaluation" block is necessary to provide the decision as to whether to restart the SSHI circuit. There are two things that the "excitation evaluation" block needs to evaluate before making a decision: the excitation amplitude and its duration. Fig. 9 shows the circuit diagram of this block which consists of three stages. The stage 1 aims to evaluate the excitation amplitude, stage 2 aims to evaluate the duration of the excitation satisfying the previous stage and stage 3 provides the signal to the next block to restart the SSHI circuit.

In the stage 1, the excitation amplitude is evaluated by comparing a fraction of V_S with a fraction of V_P. The rule of evaluating the excitation amplitude is that the SSHI circuit can at least maintain operation and generation of the SYN signal once it is restarted. (3) gives the condition for maintaining the SSHI in operational mode. Hence, the peak-to-peak voltage of $V_P - V_N$ (or V_{piezo}) should be greater than V_{TH}. If only V_P

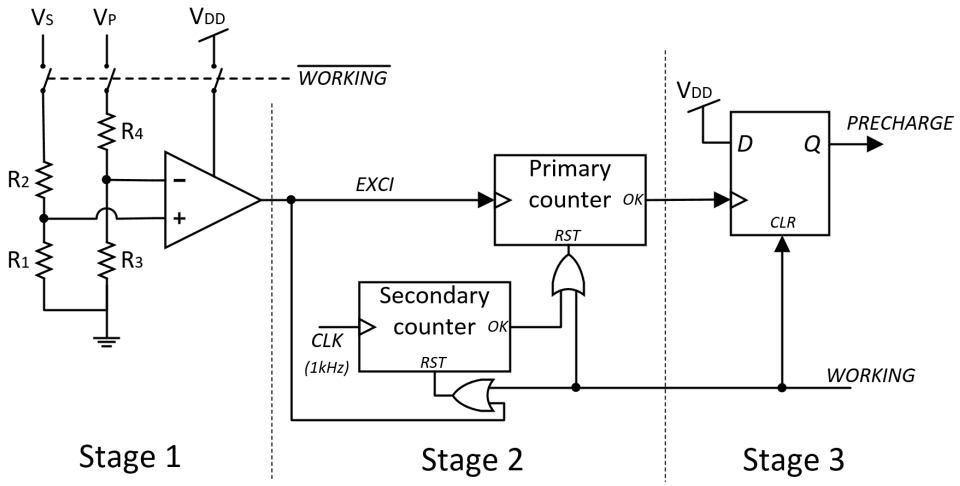


Fig. 9: Circuit diagram of excitation evaluation block.

is monitored instead of considering $(V_P - V_N)$, this condition is equivalent to that the zero-to-peak amplitude of V_P should be greater than $\frac{1}{4}V_{TH}$.

While the SSHI circuit is not working, both V_P and V_N are around a balance voltage $\frac{1}{2}V_S$. So a comparison can be performed between voltages V_P and $(\frac{1}{2}V_S - \frac{1}{4}V_{TH})$. If V_P goes lower than $(\frac{1}{2}V_S - \frac{1}{4}V_{TH})$, it means the excitation amplitude is high enough to satisfy the condition in (3) to maintain the SSHI circuit in the "working" state. From the expression of V_{TH} in (2), the condition above can be written as:

$$V_P < \frac{1}{2}V_S - \frac{1}{4}V_{TH} \Rightarrow V_P < \frac{1}{2}V_S - \frac{V_S + 2V_D}{4}\left(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C} - 1}}}\right) \tag{4}$$

In this implementation, off-chip diodes are used in the rectifier because the CMOS process accessed for this implementation does not support Schottky diodes. The forward voltage drop V_D of the diodes is measured at around $0.2\,\mathrm{V}$. Assuming $V_S \gg 2V_D$, the inductor is $L = 1\,\mathrm{mH}$, the internal capacitance of the PT is $C_P = 115\,\mathrm{nF}$ and the total ON resistance of the two switches is $R = 20\,\Omega$, so $\frac{4L}{R^2C} \gg 1$. Hence, (4) can be approximately written as:

$$V_P < \frac{1}{2}V_S - \frac{V_S}{4}\left(1 - e^{-\frac{\pi R}{2}\sqrt{\frac{C}{L}}}\right) \Rightarrow V_P < \frac{1}{4}V_S\left(1 + e^{-\frac{\pi R}{2}\sqrt{\frac{C}{L}}}\right) \tag{5}$$

With the L, R and C chosen above, $e^{-\frac{\pi R}{2}\sqrt{\frac{C}{L}}} \approx 0.72$. Hence (5) can be expressed as $V_P < \frac{1.72}{4}V_S$. Considering the shift of the balance voltage $\frac{1}{2}V_S$ due to diode mismatch and the fabrication tolerances of the CMOS process, a suitable condition is chosen as $\frac{1}{2}V_P < \frac{3}{16}V_S$, where the fractions on the both sides are to make sure the voltages in the operational range of the comparator. Hence the resistance ratios in Fig. 9 are: $\frac{R_2}{R_1} = \frac{13}{3}$ and $R_3 = R_4$. In this implementation, the resistors are chosen as $R_1 = 60\,\mathrm{M\Omega}$, $R_2 = 260\,\mathrm{M\Omega}$, $R_3 = R_4 = 50\,\mathrm{M\Omega}$ and these resistors are implemented off-chip. While the SSHI circuit is operating and the $WORKING$ signal is high, the two resistive branches and power supply of the comparator are cut off to decrease unnecessary power loss, which totally consume around $151\,\mathrm{nW}$ static power. Once the condition $\frac{1}{2}V_P < \frac{3}{16}V_S$ is met, $EXCI$ goes high, which means the excitation amplitude is high enough.

The stage 2 of this "excitation evaluation" block aims to filter any vibration impulses by employing two digital counters. The primary (10-bit) counter takes $EXCI$ as the clock signal and counts the number of pulses in $EXCI$ in order to determine if the excitation is stable. The 7 LSBs of the primary counter are set to 7'b1111111 internally and its 3 MSBs can be set externally, which enables a counting number varying from 127 to 1023. As the startup circuitry aims to restart the SSHI circuit under excitation levels between $V_{TH} < V_{pp(open)} < 2(V_S + 2V_D)$, the counting number set for this counter is determined by the vibration cycles of a PT attenuating from $V_{pp(open} = 2(V_S + 2V_D)$ to $V_{pp(open} = V_{TH}$ without applying any stable excitation, which depends on the mechanical characteristics of the PT. After experimentally measuring the PT that is used in the measurements, it takes around 45 vibration cycles while it attenuates between these two excitation levels. That takes $0.55\,\mathrm{s}$ as its natural frequency is $82\,\mathrm{Hz}$. Hence the counting number for the primary counter is set to 127 (around $1.6\,\mathrm{s}$ for this PT) in order to fully cover 45 attenuation cycles. For different PTs, the attenuation cycles are different but the maximum value 1023 is believed to be compatible with most of low frequency and high Q PTs.

The secondary counter (8-bit) in this stage is employed to reset the primary counter after a period of time while no $EXCI$ pulse is present. This counter is reset by the pulses of the signal $EXCI$ and it is driven by a $1\,\mathrm{kHz}$ CLK signal, which is internally generated. While an impulse excitation is present, a number of pulses of $EXCI$ will be generated to clock the primary counter. If the counting number is set sufficiently large, no $EXCI$ will be generated and the reset input of the secondary counter is released to start counting. After a period of time without $EXCI$ pulses, the secondary counter resets the primary counter and the input excitation is determined as an impulse. The counting time for this counter should ideally be set to a value much higher than $2/f_P$, where f_P is the natural frequency of the PT. In the case that the

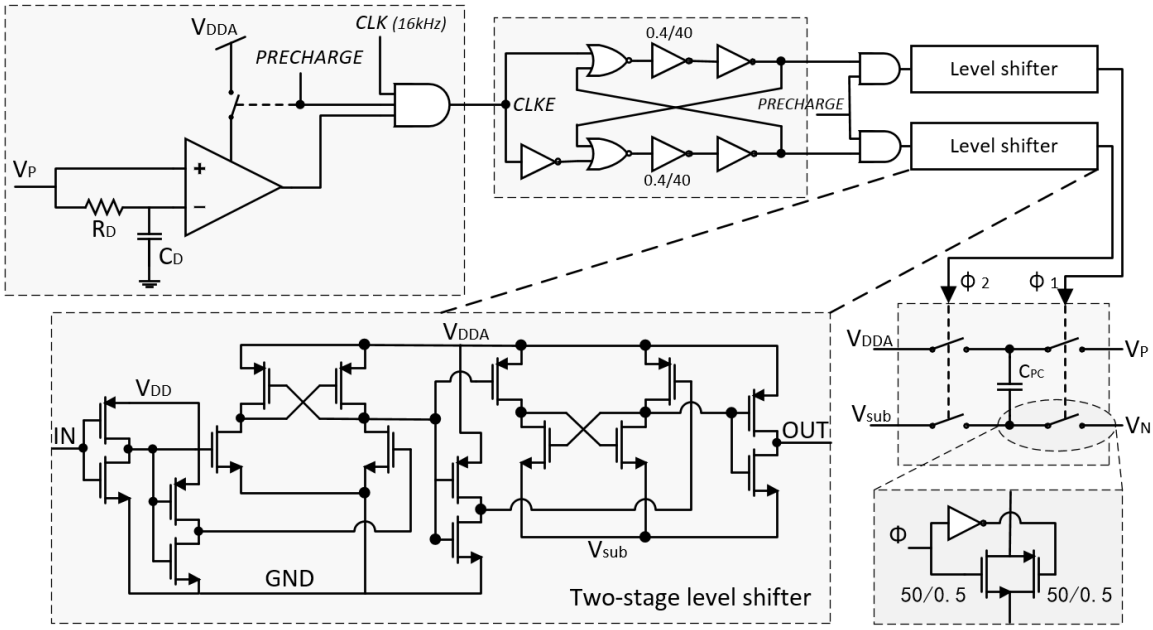


Fig. 10: Circuit diagram of the pre-charging block with on-chip $R_D = 7.5\,\mathrm{M\Omega}$ and $C_D = 30\,\mathrm{pF}$.

input excitation is stable, a pulse $EXCI$ will be generated for each vibration cycle to reset the secondary counter before it counts out, and this finally allows the primary counter to finish counting. The finishing OK signal from the primary counter is generated and sent to the next Stage. The stage 3 simply employs a D-flip-flop to give the decision of this block. Once it receives a pulse from the primary counter, the output $PRECHARGE$ goes to high level to the next block to pre-charge the piezoelectric device until the SSHI circuit goes back to work. When the SSHI circuit is restarted, the $WORKING$ signal resets this flip-flop.

In this implementation, the power supply of the comparator and the two resistive paths in the stage 1 are cut off with the signal $WORKING$ while the SSHI circuit is operating properly to minimize the power consumption. The following two digital counters and the flip-flop is not powered OFF as they consumes very little static power; instead, they keep being reset by a high level $WORKING$ signal until $WORKING$ goes low to enable the excitation evaluation block.

D. Pre-charging block

Another important block in the proposed SSHI rectifier is the pre-charging block, which performs the function of restarting the SSHI circuit while it receives an $PRECHARGE$ signal from the excitation evaluation block. Fig. 10 shows the circuit diagram of this block. This whole block is controlled by a key signal $PRECHARGE$, which indicates if pre-charging is needed and it also cuts the power supply to this block when it is at a low level to minimize power loss. Once a high $PRECHARGE$ signal is present, the comparator is powered ON and some digital signals in the following sub-blocks are enabled. While the comparator finds the right time to perform pre-charging, its high output enables the 16 kHz CLK and the enabled clock signal $CLKE$ copies CLK. Two

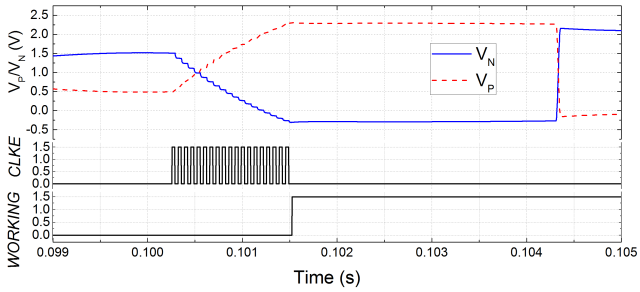


Fig. 11: Simulation waveforms of pre-charging block.

non-overlapping signals ϕ_1 and ϕ_2 are generated and shifted to higher voltage levels in the following two sub-blocks. The shifted signals ϕ_1 and ϕ_2 are then used to drive a charge pump circuit to pre-charge the PT to $V_{DDA} - V_{sub}$, which has a 5.25 V voltage difference. The flying capacitor used in the charge pump is implemented off-chip with $C_{PC} = 50\,\mathrm{nF}$. Theoretically, $V_{piezo} = V_P - V_N$ can attain a maximum value of 5.25 V after several cycles of $CLKE$; however, this value is limited by $V_S + 2V_D$ due to the diodes of the bridge rectifier. While V_{piezo} is charged to $V_S + 2V_D$, V_P equals to $V_S + V_D$ and V_N equals to $-V_D$. As V_N attains $-V_D$, SYN goes low due to the comparator in the current zero-crossing detection block in Fig. 6. A low level SYN then puts $WORKING$ signal high in the "SSHI working monitoring block" in Fig. 8 and, a high level $WORKING$ resets the $PRECHARGE$ signal to low level in the stage 3 of the "excitation evaluation block" in Fig. 10. As $PRECHARGE$ in this "pre-charging block" goes low, this whole block is powered OFF and the signals ϕ_1 and ϕ_2 are disabled to low, which turn the switches OFF in the charge pump shown in Fig. 10. Therefore, the pre-charging finishes automatically when $V_P - V_N$ is charged to $V_S + 2V_D$ and the SSHI circuit starts operating again.

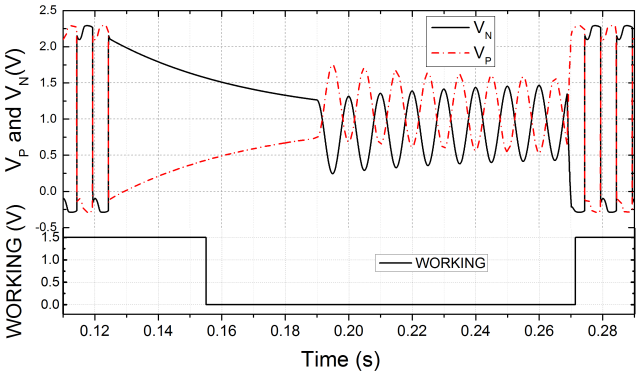


Fig. 12: Chip-level simulation waveforms.

Fig. 11 shows the simulated waveforms of the pre-charging block. It can be seen that the pre-charging starts while V_P is about to increase from its minimum. When the pre-charging starts, the signal $CLKE$ copies CLK to drive the charge pump to charge C_P. Once V_N attains $-V_D$, the $WORKING$ signal goes back to high level and the pre-charging state finishes. During the pre-charging period while $CLKE$ signal is present, the power consumption is as high as $1.4\,\mathrm{mW}$ for a time period lasting less than $1\,\mathrm{ms}$. Hence, a certain amount of energy (less than $1.4\,\mu\mathrm{J}$) is "invested" for restarting the SSHI circuit.

V. Simulation Results

The simulations in this paper were performed using licensed Virtuoso, Cadence version IC6.1.5. The waveforms of the chip-level simulation are shown in Fig. 12. From the figure, it can be seen that the SSHI works to specification and the voltages V_P and V_N are correctly inverted before $0.125\,\mathrm{s}$. Between $0.125\,\mathrm{s}$ and $0.19\,\mathrm{s}$, there is no excitation so both the V_P and V_N go towards $\frac{1}{2}V_S$ due to the leakage (which is $1\,\mathrm{V}$ as $V_S = 2\,\mathrm{V}$ in the simulation). After a period of time from $0.125\,\mathrm{s}$, the "SSHI working monitoring" block finds that the SSHI is not working and makes $WORKING$ signal go to a logic low level. From $0.19\,\mathrm{s}$, a weak excitation is present. The amplitude of this excitation satisfies the condition $V_{pp(open)} > V_{TH}$ but it cannot satisfy $V_{pp(open)} > 2(V_S + 2V_D)$. Hence, the conventional SSHI circuit will not work in this case and will not extract any energy. But in the proposed SSHI rectifier with self-startup circuitry, the SSHI circuit is restarted after several periods of excitation evaluation. The pre-charging occurs at the time $0.27\,\mathrm{s}$. When V_N approaches $-V_D$, the $WORKING$ signal goes back to high level so the SSHI circuit is now restarted.

VI. Measurement Results and Discussion

The proposed SSHI rectifier with self-startup circuitry was experimentally evaluated using a commercially available piezoelectric transducer (PT) of dimension $47\,\mathrm{mm} \times 36\,\mathrm{mm}$ (Mide Technology Corporation V20W). A shaker (LDS V406 M4-CE) was excited at the natural frequency of the PT at $82\,\mathrm{Hz}$ and driven by a sine wave from a function generator (Agilent Technologies 33250A $80\,\mathrm{MHz}$ waveform generator)

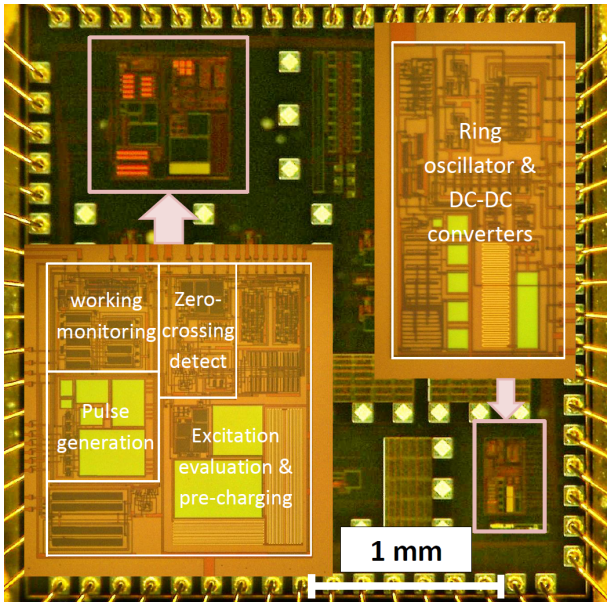


Fig. 13: Micrograph of the test chip fabricated in a $0.35\,\mu\mathrm{m}$ CMOS foundry process. The overall die size is $2.8\,\mathrm{mm} \times 3.2\,\mathrm{mm}$. The active area for the proposed circuit is around $0.6\,\mathrm{mm}^2$.

amplified by a power amplifier (LDS PA100E Power Amplifier). An off-chip voltage regulator (ON Semiconductor NCP4681DSQ15T1G) with ultra-low ground leakage current ($I_{GND} \approx 1.5\,\mu\mathrm{A}$) was employed to provide a stable $1.5\,\mathrm{V}$ if $V_S \geq 1.5\,\mathrm{V}$. When the system is self-sustained and at a fully-discharged state, the system simply works as a full-bridge rectifier (threshold is very low due to low V_S) and V_S needs to be charged to $1.5\,\mathrm{V}$ before the proposed circuit starts working. Hence, an external power supply at $1.5\,\mathrm{V}$ was also used for some cases. A super capacitor is employed as the energy storage capacitor (AVX BestCap BZ05CA103ZSB, measured capacitance $C_S \approx 5.2\,\mathrm{mF}$) and four off-chip diodes (DIODES INC. DFLS130L-7, measured voltage drop when working in a bridge rectifier is $V_D \approx 0.2\,\mathrm{V}$) are employed to build a full-bridge rectifier. The voltage drop of the diodes can be measured by employing a full-bridge rectifier (refer to Fig. 1a) and measuring the higher and lower limits of V_P and V_N to obtain the effective voltage drop of the four diodes. The proposed chip was implemented in a $0.35\,\mu\mathrm{m}$ HV CMOS process. Fig. 13 shows the die photo of the test chip. The active area of the proposed SSHI rectifier together with the DC-DC converters and clock generator is $0.6\,\mathrm{mm}^2$. Off-chip capacitors are used for the SC converters due to limited design area and the rest of the chip is occupied by other circuits for other projects.

Table I lists the power loss due to different blocks of the interface circuit. While the SSHI circuit is operating, the level shifters consumes high dynamic power due to driving switches, especially the big W/L CMOS switches controlling the inductor. As these two switches have very large transistor width for low ON-resistance purpose, the parasitic capacitance associated with the gate is extremely large, which increases

TABLE I: Breakdown of the chip power consumption.

	Power loss	
Loss mechanism	SSHI working	SSHI not working
Ring oscillator	260 nW	260 nW
DC converters	13 nW	13 nW
Level shifters	286 nW	19 nW
Zero-crossing detect	211 nW	198 nW
Pulse generator	6 nW	0.1 nW
Work monitoring	0.4 nW	0.4 nW
Excitation evaluation	0.2 nW	152.4 nW
Total	776.6 nW	642.9 nW

the energy consumption per switch. When the SSHI circuit is not working, the driving signal ϕ_{SSHI} of the big W/L switches is kept at low level, hence the power loss due to level shifters is significantly decreased. As the comparator in the zero-crossing detection block constantly outputs a high SYN signal while SSHI is not working, there is no dynamic power loss for this comparator. But the excitation evaluation block is powered ON which consumes extra power while SSHI is not working. From the table, the power consumption while the SSHI circuit is not working is found to be less than when the SSHI circuit is working. Another power-consuming block not listed in the table is the pre-charging block, which consumes 1.4 µJ for one startup. The average power loss due to this 1.4 µJ startup energy is difficult to be calculated as it depends on the environmental vibration and how frequently the SSHI rectifier needs to be restarted. Assuming the SSHI circuit needs to be restarted for every 100 s, the duty ratio for this block is around 0.001% and the average power loss is around 14 nW.

Fig. 14 shows waveforms of V_N, ϕ_{SSHI}, $WORKING$ and $PRECHARGE$ from an oscilloscope. The signals were measured in a period of 20 s by changing the input excitation amplitude when necessary and $C_S = 2$ V. Before the time t_1, the SSHI circuit is working and the input excitation is high enough to maintain operation of the SSHI interface. Pulses ϕ_{SSHI} are generated correctly to invert V_{piezo} and the signal $WORKING$ is at high level. Between t_1 and t_2, the excitation is decreased to a very low level. As a result, ϕ_{SSHI} cannot be generated and $WORKING$ goes to a low level indicating that the SSHI is not working. Between t_2 and t_3, the excitation is slightly increased but the condition for maintaining the SSHI operational is still not satisfied. This weak excitation is evaluated by the "excitation evaluation" block, which decides not to restart the SSHI circuit. From t_3, the excitation is further increased. After evaluating the input excitation for 1.6 s to make sure that it is not a shock, a $PRECHARGE$ pulse is generated to restart the SSHI circuit at time t_4. From this instant, $WORKING$ goes back to a high level until the input excitation is decreased to a very low level at time t_5.

The waveforms in a short period of time while restarting the SSHI circuit is shown in Fig. 15. After the excitation evaluation block decides to restart the SSHI circuit, a $PRECHARGE$ pulse is generated to pre-charge the PT. During the pulse of $PRECHARGE$, $CLKE$ copies the

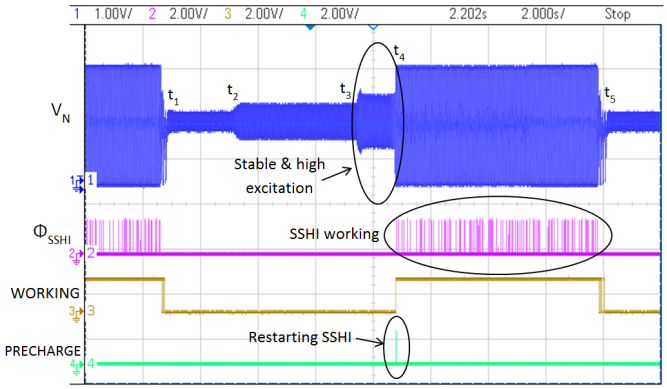


Fig. 14: Measured waveforms of signal V_N, ϕ_{SSHI}, $WORKING$ and $PRECHARGE$ in a period of 20 s.

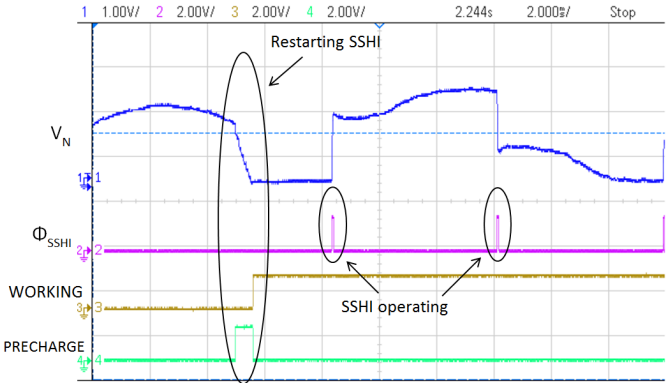


Fig. 15: Measured waveforms in a short period of time while restarting the SSHI circuit.

16 kHz clock and V_N is charged to $-V_D$. Once V_N attains $-V_D$, $WORKING$ goes high, which clears the signal $PRECHARGE$ and the pre-charging state terminates. As the SSHI circuit is now working, the signal ϕ_{SSHI} can be correctly generated to invert the voltage across the PT at each I_P zero-crossing point. The waveforms obtained are consistent with the operation as described in Sections IV and V.

Fig. 16 shows the measured power obtained at the output capacitor C_S of the rectifier for different V_S. The PT was excited at 82 Hz with an open-circuit voltage $V_{pp(open)} = 2.8$ V (equivalent to 2.0 g) for the measurements. The experiments were performed with a full-bridge rectifier and the proposed SSHI rectifier with self-startup circuitry while the value of the inductor is changed. With the fabricated chip, the full-bridge rectifier can be achieved by forcing the voltage-inverting signal ϕ_{SSHI} being at low level and disabling the SSHI circuit. According to the figure, the full-bridge rectifier was able to provide a maximum output power of 13.5 µW with an optimal V_S voltage of 0.6 V. As expressed in (1), the condition for starting the SSHI circuit is $V_{pp(open)} > 2(V_S + 2V_D)$; hence, the theoretical condition for that the SSHI circuit can be started is $V_S < \frac{V_{pp(open)}}{2} - 2V_D$, or $V_S < 1.2$ V. As shown in the figure, region 1 and region 2 represent the allowed region and the forbidden region for the conventional SSHI rectifier, respectively. Compared to the conventional SSHI rectifier, the

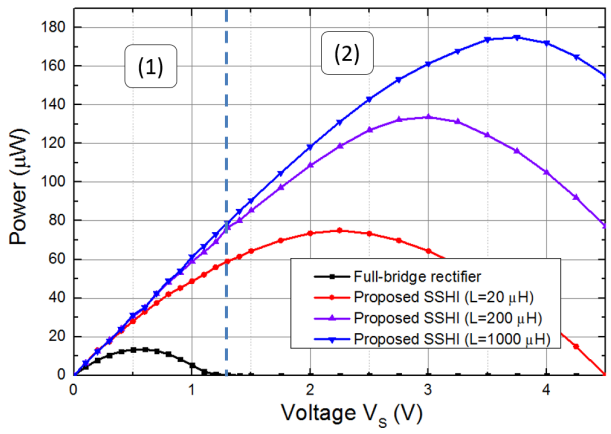


Fig. 16: Measured electrical power output of full-bridge rectifier and the proposed SSHI rectifier with off-chip diodes ($V_D = 0.2\,\mathrm{V}$), where the horizontal axis V_S represents the voltage across the storage capacitor C_S and $V_{pp(open)} = 2.8\,\mathrm{V}$.

improved SSHI rectifier with self-startup circuitry is able to start the SSHI circuit at a lower excitation amplitude (or at a higher V_S for a given $V_{pp(open)}$), as expressed in (3). Considering the startup issues of conventional SSHI rectifiers, the proposed circuit can easily achieve theoretical maximum power points while the conventional SSHI circuit cannot work at these points if not previously re-started. Hence, the proposed SSHI is allowed to work in both regions 1 and 2.

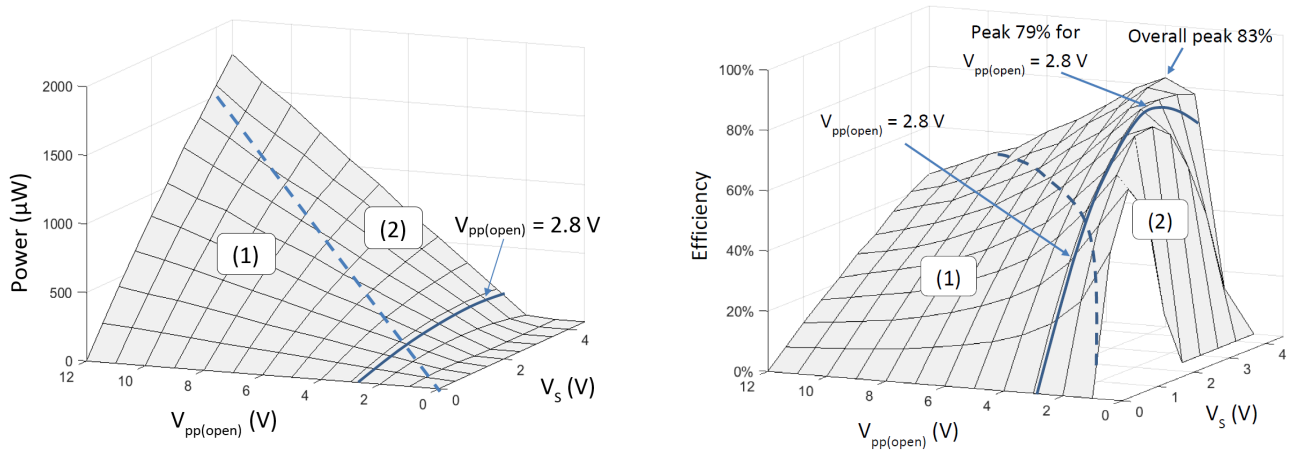
Similar experiments and output power plots for conventional SSHI rectifiers have been presented in [18], [23], [24], in which the SSHI startup issue was not addressed. Although some of the implementations use other methods to detect the voltage peak and are able to flip V_{piezo} until it attains V_S+2V_D (or $-(V_S + 2V_D)$) to start the SSHI circuits, employing "working monitor" and "excitation evaluation" blocks can be considered as useful and significant additions to determine when to start the SSHI circuit in order to avoid energy loss due to flipping V_{piezo} at weak excitation levels. According to the theoretical calculation and experimental results in Fig. 16 in this paper, if an SSHI rectifier is not started, a high V_S voltage prevents the rectifier from harvesting energy while the SSHI circuit is not working. In real-world implementations, it is impractical to perform manual startup (such as shaking the harvester) after each period of time, where the excitation level is extremely low, when the SSHI circuits stop working. Hence, adding a startup circuitry in an SSHI rectifier is practically essential to increase the average output power so that energy can still be extracted at moderate or low excitation levels.

Fig. 17 shows the measured electrical output power and efficiency in a surface plot while $V_{pp(open)}$ is varied from $0\,\mathrm{V}$ to $12\,\mathrm{V}$ with steps of $1\,\mathrm{V}$ and V_S is varied from $0\,\mathrm{V}$ to $4.5\,\mathrm{V}$ with steps of $0.5\,\mathrm{V}$ representing 130 independent measurements. The regions 1 and 2 separated by dotted curves represent the allowed and forbidden regions, respectively, for conventional SSHI circuits. The inductor used in these measurements was chosen at $1\,\mathrm{mH}$ and the $V_{pp(open)} = 2.8\,\mathrm{V}$ plane (corresponding to Fig. 16) is highlighted. It can be seen that while the excitation level $V_{pp(open)}$ is small (less than $3\,\mathrm{V}$), the maximum power point in function of V_S can be attained over the measured V_S range ($0\,\mathrm{V} \rightarrow 4.5\,\mathrm{V}$). However, when the excitation goes higher, the maximum power point is shifted to higher V_S. As the peak power points under higher excitation levels cannot be achieved as $V_{pp(open)}$ goes higher, the power efficiency decreases although the output power increases. From Fig. 17b, it can also be found that the startup circuitry allows the proposed SSHI rectifier to achieve efficiency peaks in region 2 while the conventional SSHI rectifier can only work in the region 1.

Fig. 18a shows the measured power efficiency from the PT to the storage capacitor C_S for the proposed SSHI with startup circuitry and the conventional SSHI without startup circuitry while the circuit is externally powered and self-powered. The voltage across the storage capacitor is $V_S = 2\,\mathrm{V}$, the inductor is chosen at $1\,\mathrm{mH}$ and the excitation level is swept for $V_{pp(open)} = 0\,\mathrm{V} \rightarrow 12\,\mathrm{V}$. For conventional SSHI circuits, if the SSHI circuit is not manually started, the circuit does not harvest any energy until $V_{pp(open)}$ goes higher than $2(V_S + 2V_D) = 4.8\,\mathrm{V}$. However, for the proposed SSHI circuit, $V_{pp(open)}$ just needs to overcome V_{TH}, which is around $1\,\mathrm{V}$. This allows the proposed circuit to achieve the theoretical peak efficiency point and it can harvest energy over an increased input range. Fig. 18b shows the efficiency variation while the excitation level is swept from low to high and from high to low. The conventional SSHI circuit is only able to achieve the theoretical peak performance when the excitation moves from high to low because the SSHI circuit has been started by high excitation before; but from low to high, the conventional SSHI cannot work as expected until it overcomes the $2(V_S+2V_D)$ threshold. However, the proposed SSHI circuit is able to achieve the expected performance in both excitation sweeping directions.

VII. Conclusion

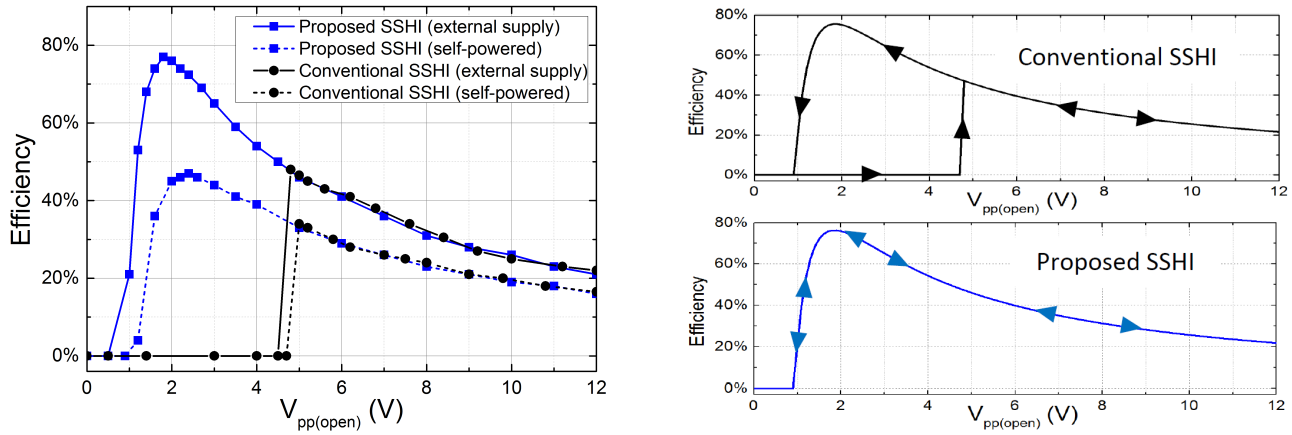
This paper identified a startup problem that exists with the conventional SSHI interface circuits that are commonly used in piezoelectric energy harvesters due to the high power efficiencies. This startup issue limits the operational range of conventional SSHI rectifiers making it difficult to extract any energy under low excitation input. An improved SSHI architecture is introduced in this paper to dynamically detect the operation of the SSHI circuit and automatically restart the circuit when it is not operational and the excitation input meets startup conditions. Theoretical calculations and measured results show that the proposed SSHI interface circuit is able to extract energy in an increased input range starting from a much lower excitation amplitude. With an increased input range, the proposed SSHI circuit can achieve the theoretical maximum power point and the maximum efficiency point while the conventional SSHI circuit can only attain these points if it has been previously started off at a higher excitation amplitude. This approach thus provides the ability to re-start the SSHI circuit and increase the operational range under practical excitation conditions without consuming additional power. This work also sets the stage for future designs that can tune the configuration of the interface power conditioning circuit



(a) Power.

(b) Efficiency.

Fig. 17: 3-D surface plot of measured output electrical power and efficiency in function of $V_{pp(open)}$ and V_S while the inductor is chosen at $L = 1\,\mathrm{mH}$ (with external stable $1.5\,\mathrm{V}$ power supply and the conversion efficiency of voltage regulator is not considered).



(a)

(b)

Fig. 18: (a) Measured power efficiency for the proposed SSHI with startup circuitry and the conventional SSHI without startup circuitry while the circuit is externally powered and self-powered using an off-chip voltage regulator. (b) Efficiency variation while excitation level is swept in two directions.

for energy harvesters with a view towards maximizing output power by dynamically evaluating the operating environmental conditions.

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