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Impact of silicon nitride stoichiometry on the effectiveness of AlGaN/GaN HEMT fieldplates

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Abstract— **Fieldplate control of current collapse and channel electric field distribution in AlGaN/GaN HEMTs is investigated as a function of LPCVD silicon-nitride stoichiometry. Dependence of current collapse is seen, however this also leads to enhanced fieldplate pinch-off voltages and higher leakage. Electric field concentration at the gate edge is indicated by measuring off-state 2DEG position with a sense contact technique. A model explaining the fieldplate threshold variation due to barrier leakage is proposed.**

Index Terms— **AlGaN/GaN HEMT, field plate, passivation.**

I. INTRODUCTION

THERE has been much interest in AlGaN/GaN based transistors for high power applications, in part due to GaN's superior critical breakdown field of 3.3 MV/cm [1]. However strong electric fields, which exist in devices during operation can be the cause of reliability problems such as leakage, charge trapping and device degradation [2-4]. Some of these problems can be reduced by building devices with well optimized field plates (FPs) [5,6], together with a SiN_x passivation/encapsulation deposition process. Previous work on the silicon nitride deposition process has measured DC characteristics and current collapse [7-12]. Here, in addition to this we demonstrate the impact of SiN_x changes to the channel electric field profile which is critical to device reliability. Importantly, this work shows that modifying the silicon nitride process can change the FP pinch-off voltages.

Introduction of FPs into devices has been shown to dramatically increase breakdown voltage by spreading the region where potential is dropped away from the edge of the gate. Models usually assume a purely capacitive effect, given by electrostatics, where the difference in potential between the FP and the channel defines the depletion of electrons in the 2DEG. The drain voltage when the channel pinches off under the FP, V_{FP} is given by

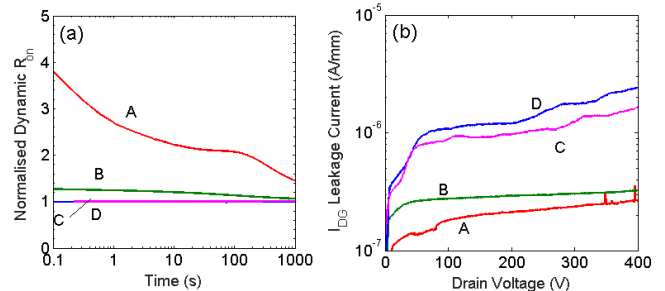$$V_{FP} = \frac{en_s}{C_{FP}}, \qquad (1)$$

Fig. 1. (a) Normalized dynamic R_{on} of HEMTs fabricated on wafers with low leakage, A, and high leakage, D, LPCVD nitride. Stress conditions V_{GS}=-5V, V_D= 100V for 1000s. Measurement conditions V_{GS}=0V, V_D= 1V. (b) Drain-gate leakage current of the same devices.

where $-en_s$ is the electron charge density of the channel and C_{FP} is the channel to FP capacitance per unit area. C_{FP} is calculated by the in-series addition of capacitance of each layer. Capacitance of each layer is given by $\frac{\varepsilon}{d}$ where d is the thickness of the layer and ε is the dielectric constant of the layer. In this paper, we demonstrate a fieldplate pinch off voltage different from Eq. 1 that is dependent on the stoichiometry of the silicon nitride deposited onto the AlGaN surface.

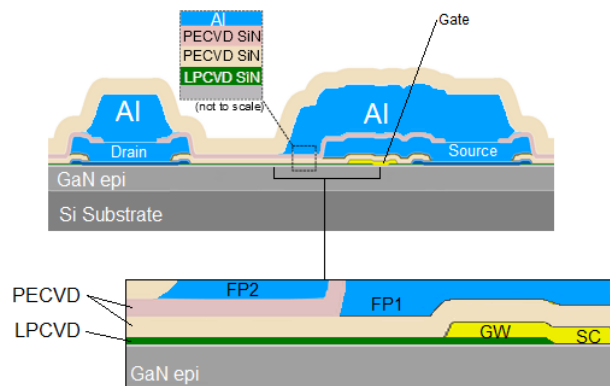In this study, we investigate the consequence of the leaky

Fig. 2. Cross-section of normal HEMT device. Expansion of device regions; Schottky contact (SC), gate wing (GW), fieldplate1 (FP1) and fieldplate2 (FP2).
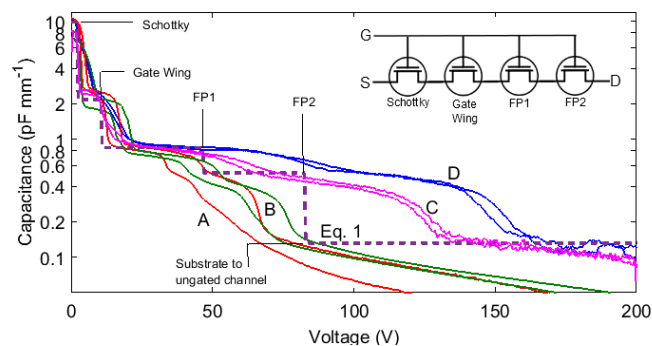
Fig. 3. Capacitance measured on Schottky diode devices with FP geometry matching Schottky HEMTs. High Si-content LPCVD nitride, devices C&D, have an increased V_{FP} for both FP1 and FP2.
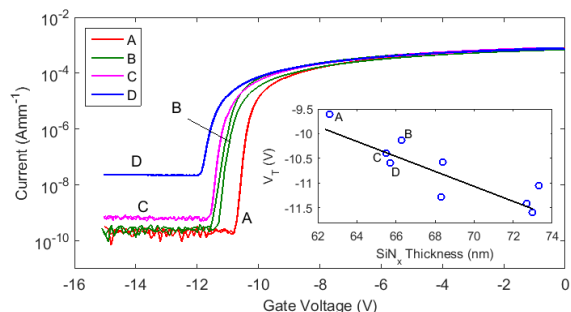

Fig. 4. Drain current vs gate voltage for fatFET structures with gate stack corresponding to gate wing. $V_D = 50mV$. Small V_T variation is seen which can be explained by manufacturing differences in the thickness, inset is V_T plotted against SiN_x thickness for all wafers in the batch showing a clear trend along the capacitive line.

dielectric on the effectiveness of the FPs and show that the voltages at which they become effective are strongly influenced by passivation nitride stoichiometry with consequences for device reliability. Effectiveness in this context is the ability of the FP to reduce the lateral electric field at edge of the gate metal, increased FP threshold voltages seen here lead to a doubling of this electric field. This effect is linked to changes in current collapse and leakage through the device.

II. GROWTH AND FABRICATION

Measurements were made on 4 wafers which were grown with identical epitaxy. These were 150mm diameter GaN-on-Si wafers grown by metal organic chemical vapor deposition with a strain relief layer, a carbon doped buffer and uid-GaN layer, followed by a 20 nm AlGaN layer and a 3 nm GaN cap, giving a total epitaxial thickness of ∼5µm; 2DEG carrier density was $5.87\times 10^{12} cm^{-2}$. Subsequently a 70 nm low-pressure chemical vapor deposition (LPCVD) silicon nitride was deposited using a horizontal LPCVD furnace at 850°C, with an approximate pressure of 100mTorr. The wafers were soaked in NH_3 before introduction of the dichlorosilane (DCS). The stoichiometry of this silicon nitride was varied between the wafers and was the only difference between the wafers. The stoichiometry was controlled by varying the DCS/NH_3 precursor ratio while keeping a constant gas flow rate. Wafer A received the stoichiometric Si_3N_4 ratio and the DCS fraction was increased systematically up to wafer D with the highest Si content, given in Table 1. Devices and test structures were fabricated using a
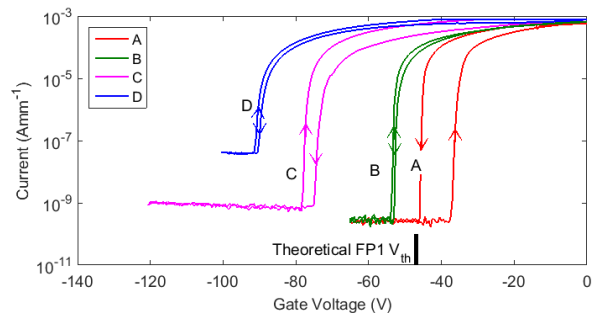

Fig. 5. Drain current vs gate voltage for fatFET structures with gate stack corresponding to FP1. Large variation is seen between the wafers. $V_D = 50mV$. Capacitive model predicts V_{th}= -47V. Ramp rate of 2.3V/s
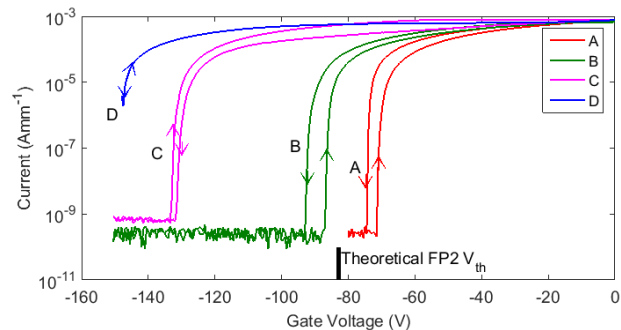

Fig. 6. Drain current vs gate voltage for fatFET structures with gate stack corresponding to FP2. Large variation is seen across the wafers. $V_D = 50mV$. Capacitive model predicts V_{th}= -83V. Ramp rate of 2.3V/s

650V GaN-on-Si depletion mode process [13]. All measurements were made with the substrate at 0V [14].

TABLE I
LPCVD SiN_x PROPERTIES BY WAFER

	A	**B**	**C**	**D**
DCS/NH₃	0.33	2.49	3.30	4.38
Stress (MPa)	1132	428	275	117
Refractive Index	2.01	2.10	2.14	2.21

III. EXPERIMENTS AND RESULTS

Dynamic resistance measurements were made on HEMTs after a stress condition of V_{GS}=-5V, V_D= 100V had been applied for 1000s, these are shown in Fig. 1(a). A trade-off between leakage and current collapse is seen as DCS/NH_3 ratio is varied. The high current collapse in wafer A is reduced in D by increasing the DCS/NH_3 ratio, however this is also seen to increase the off-state drain current seen in Fig. 1(b). Details of the exact mechanism will be investigated in future work.

Capacitance was measured in large anode-width Schottky diodes (30mm) and is shown in Fig. 3. These had two anode FPs which extended along the channel, the first (FP1) was deposited after a PECVD Si_3N_4 of 300 nm, the second (FP2) was after another 300nm of Si_3N_4, giving a total thickness of
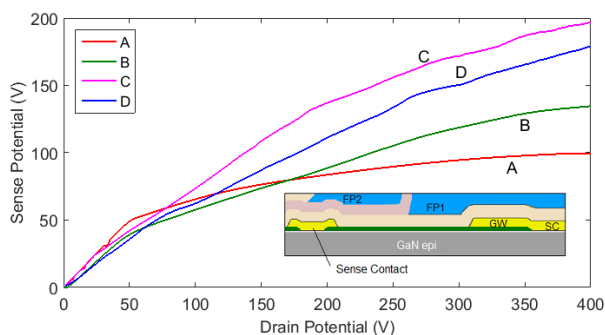
Fig. 7. Voltage measured on sense potential devices. Knee voltage indicates that the 2DEG has retracted past the sense finger. Devices with higher Si content in LPCVD nitride have slower 2DEG retraction. Inset is cross section of sense node device, as in Fig 2, but with sense contact indicated. Sweep rate 4.9V/s.

693nm from FP2 to the 2DEG. FP geometry is that of the HEMT in Fig. 2 but here the gate and fieldplates are in electrical contact, which allows easy capacitance measurements in a structure that is electrically very similar to the HEMT in off state operation. Also plotted is the theoretical capacitance in the case of zero leakage or charge trapping based on Eq. 1 using the dimensions of the field plates. The value of each theoretical capacitance step fits the measured values well, however there is strong positive and negative deviation in the FP pinch-off voltages in each of the devices from this theoretical curve. Wafers C&D show a large increase in the threshold voltage of FP1 and FP2 indicating a temporary positive charge storage, whereas wafers A, B show a small negative shift.

Measurements of 100μm×100μm fatFET devices with gate stacks equivalent to the HEMT gate wing, FP1 and FP2 are shown in figures 4, 5 & 6 respectively. The negative threshold voltage of these transistors corresponds to the required positive voltage applied to the drain in a HEMT to induce retraction of the 2DEG from under that FP. For the gate wing devices there is no significant threshold change, any change can be explained by manufacturing differences in the thickness, displayed in the inset. A lack of threshold hysteresis or shift here strongly indicates no charge trapping at the AlGaN /LPCVD SiN_x interface and that any interface charge here was kept constant between the wafers. In the case of the FP devices there are both positive and negative shifts in the expected threshold voltages with respect to a purely capacitive model, suggesting multiple mechanisms altering the threshold voltage. Wafers A&B have a threshold close to the purely capacitive case, and show hysteresis indicating negative charge storage, with the possible exception of wafer B FP1. Whereas wafers C&D (with high DCS/NH_3 ratio) have a much larger threshold voltage, and show a small hysteresis, indicating positive charge storage. The smaller hysteresis in wafer B FP1 may indicate the trapping process is field dependent and has more contributions than just at the surface.

In order to monitor this retraction of the 2DEG in a working device, special Schottky gate HEMTs were fabricated. These are HEMTs with an extra Schottky sense-contact positioned under FP2, shown inset in Fig. 7. This device design has been used in a previous study [15]. Here, this extra contact is biased in current mode such that a small current (10^{-7}A in this case)
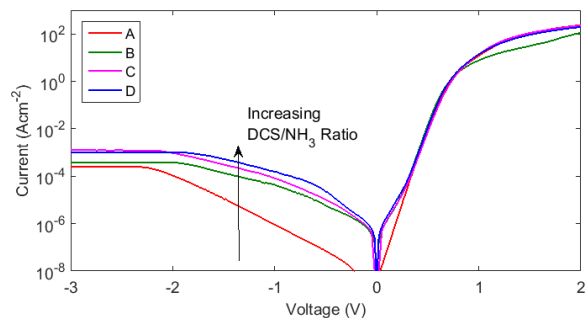

Fig. 8. Schottky Gate leakage measured on 100 μm×100 μm gate area fatFET device. Shows large change in conductivity in reverse bias that follows DCS/NH_3 fraction.
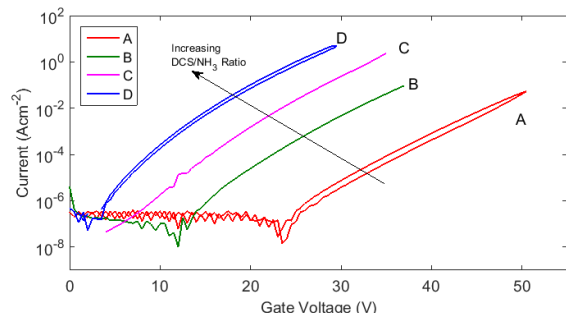

Fig. 9. Leakage through 70nm LPCVD SiN_x. High DCS/NH_3 ratio wafers have low threshold for leakage.

flows from the channel across the forward biased Schottky barrier. The potential measured, V_{sense}, is then within 1V of the channel potential under this sense-contact. The gate is biased at -7V to pinch off the channel, source is at 0V and the drain voltage is swept to 400V, with V_{sense} shown in Fig. 7. Before the 2DEG has retracted past the sense finger the potential measured at that contact should be almost equal to the drain potential (i.e. $V_{sense} = V_D$). At the point where the 2DEG retracts past this sense contact the potential will show a reduction in gradient. This knee indicates that the channel potential at the sense contact is no longer in good electrical connection to the drain, thus the potential V_{sense} rises more slowly than the drain potential. It can be seen clearly from Fig. 7 that the wafers with low DCS/NH_3 ratio, A&B, have a sharp knee at around 60V, whereas high DCS/NH_3 wafers, C&D, have a less well defined knee indicating slower 2DEG retraction and a resultant stronger electric field at the gate edge, broadly consistent with the data of Fig. 6.

The Schottky leakages are displayed in Fig. 8. These were measured on 100μm×100μm fatFET devices. There is clear ranking in Schottky reverse bias leakage between the wafers, with leakage increasing from A to D.

As the LPCVD SiN_x was the only step which varied between these wafers the difference in its leakage was measured. Due to the processing sequence this leakage was measured in series with the AlGaN barrier and the results are shown in Fig. 9. This MIS junction was forward biased to reduce the contribution to resistance from the AlGaN barrier. The AlGaN barrier has a much lower resistance than the SiN_x, for example by comparing Figs 8 and 9 at a current of $1Acm^{-2}$ less than 1V is dropped across the AlGaN. The highest DCS/NH_3 ratio wafer D has ~six orders of magnitude more LPCVD SiN_x leakage current than the lowest ratio, A. There is significant leakage through this
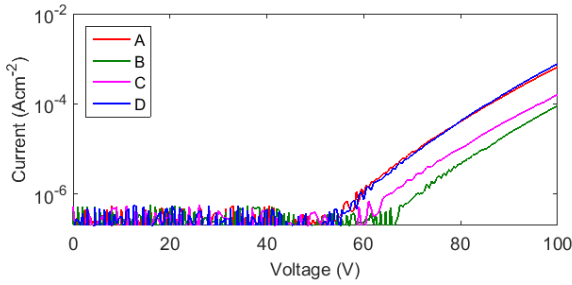
Fig. 10. Leakage through 300nm PECVD SiN_x layers measured on metal-insulator-metal structures. The leakage level through the LPCVD layers is indicated for wafers C and D at the point of pinch-off, this would be the current through the entire stack in the steady state. This current is broadly consistent with the FP1 V_{TH} measured which has been indicated.

layer for wafers C and D at the point the channel would retract (~11.5V), contributing to the higher off-state leakage seen in Fig. 1(b).

The leakage through the 300nm PECVD layer present in FP1 was measured on a metal-insulator-metal structure and is presented in Fig. 10. The resistance is higher than for the LPCVD layer due to increased thickness. The minor variation seen here is due to small manufacturing differences. This layer is shown to be very resistive until a voltage of 60V or more is dropped across it.

IV. DISCUSSION

The key observation is that FP threshold voltages for the highest DCS/NH_3 ratio wafers, C&D, shift to higher voltages with respect to the purely capacitive value implying temporary positive charge storage. This shift can be seen in capacitance and fatFET measurements in Figures 3, 5 and 6 but is not seen in the gate wing devices plotted in Fig.4. We note that the different SiN_x layers between the FP and the 2DEG will have different conductivity, so when biased, charge can accumulate within the dielectric stack and this can cause an increase in V_{FP}. A circuit model is shown in Fig. 11(c). When the charge stored across the combined capacitor of the AlGaN and LPCVD SiN_x layers, $C_{GW}V_{GW}$, is equal to the initial channel electron density, qn_s, the 2DEG is depleted and will retract from under the FP towards the drain. For a leaky device dielectric this new threshold voltage is calculated by considering the potential
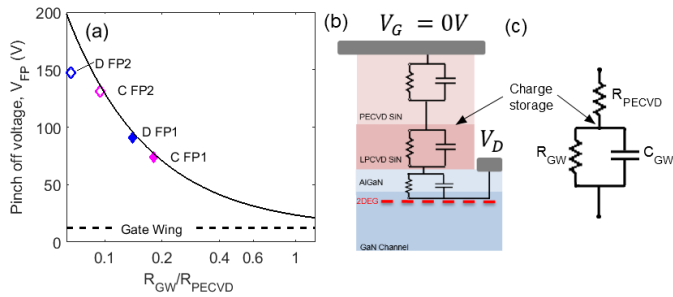

Fig. 11. (a) Equation 3 plotted as a function of the ratio of resistances of the barrier layers. Measured values for FP pinch off voltages on wafers C and D are also plotted. (b) A circuit model of a leaky barrier between the channel and the FP, the resistances of the different layers act as potential dividers and modify the FP pinch-off voltage. (c) Simplified circuit showing important parameters for V_{FP}. Where $C_{GW} = C_{AlGaN}C_{LPCVD}/(C_{AlGaN} + C_{LPCVD})$ and $R_{GW} = R_{AlGaN} + R_{LPCVD}$

across the lower part of the stack, V_{GW}, when the conducting stack acts as a potential divider.

$$V_{GW} = \frac{R_{GW}}{R_{PECVD} + R_{GW}} V_D \qquad (2)$$

This leads to a modified expression of Eq. 1 valid in the steady state:

$$V_{FP} = \left(1 + \frac{R_{PECVD}}{R_{GW}}\right) \frac{en_s}{C_{GW}}. \qquad (3)$$

where

$$R_{GW} = R_{AlGaN} + R_{LPCVD}; \text{ and } C_{GW} = \frac{C_{AlGaN}C_{LPCVD}}{(C_{AlGaN} + C_{LPCVD})}.$$

R_{label} and C_{label} are the resistances and capacitances of each of the layers labelled in Fig. 11(b). Eq. 3 applies when the RC time constant of each of the layers is shorter than the time held at each measurement voltage. Whereas Eq. 1 applies instantaneously after switching. An increase in the leakage through the AlGaN and LPCVD SiN_x barriers results in $R_{PECVD} \gg R_{GW}$ and so, from Eq. 3, V_{th} increases. Each of the layer resistances are field dependent and lead to field-dependent time constants that have been plotted in Fig. 12, calculated from measured resistances and known thicknesses of the layers. The FP stack will either be described (i) by Eq. 1 if each layer is highly resistive, (ii) by Eq. 3 if it has reached a steady state or (iii) it will be in a transient state where the charges and fields in the stack are changing. The RC time constants marked by diamonds in Fig. 12 for each LPCVD SiN_x layer indicate the response-time at the electric field required to pinch-off the channel, this is very high for wafers A and B, on the order of a minute and above, explaining why Eq. 3 applies to wafers C and D only.

Fig. 11(a) is a plot of Eq. 3 as the ratio of resistances in the dielectric stack, $\frac{R_{PECVD}}{R_{GW}}$, is varied. This agrees reasonably well with the measured V_{TH} values for wafers C and D. For the highest DCS/NH_3 ratio wafers the lower part of the barrier is leaky (AlGaN and LPCVD SiN_x) and the potential is mainly dropped over the PECVD nitride layer, away from the channel, resulting in positive charge accumulating at the PECVD/LPCVD SiN_x interface and thus requiring a much larger voltage to deplete the channel. Whereas for low DCS/NH_3 ratio wafers A&B the AlGaN barrier and LPCVD nitride are more resistive and the stack responds closer to the purely capacitive model. It can be seen from Fig. 9 that wafers A and B do not have significant leakage across the nitride before the channel in a device is pinched-off, at a potential difference of ~ 11.5 V, once pinched-off any increase in drain potential is dropped elsewhere in the device. Fig. 12 also indicates that the time constants for charge to accumulate across the LPCVD SiN_x layer are very long for these wafers at pinch-off. These observations explain the absence of increased FP threshold in wafers A and B; without leakage across this LPCVD SiN_x layer positive charge cannot be stored at the LPCVD/PECVD SiN_x interface.

This difference in conductivity through the different layers provides an explanation for the hysteresis observed in Figs 3, 5
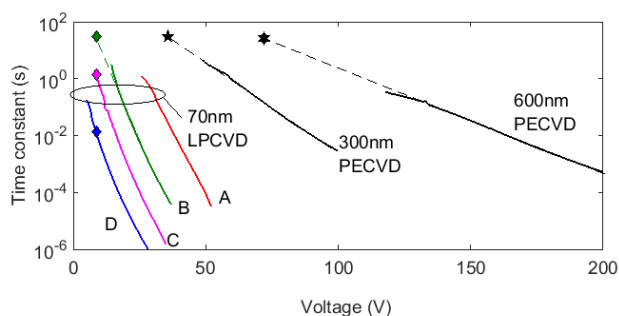
Fig. 12. Voltage dependent RC time constants of the layers in fieldplate structures. From measured resistance and calculated geometric capacitance. Markers indicate each layer time-constant immediately after switching off, where the stack is behaving purely capacitively, these have been extrapolated from measured values where necessary. Dashed lines indicate extrapolated trends.

and 6 i.e. transport to traps rather than the trapping kinetics is the rate-limiting step, in contrast to systems where the de-trapping process is dominant [16]. This model is supported by the lack of shift in the gate wing threshold in Fig. 4. The positive charge is presumably caused by electrons vacating traps at the SiN_x/SiN_x interface. For high DCS/NH_3 ratio wafers, C&D, any positive charge stored at the LPCVD/PECVD SiN_x interface leaves the structure quickly after a sweep due to the high leakage of the lower part of the stack even at relatively low fields meaning small positive-charge hysteresis. Conversely, when the AlGaN and LPCVD SiN_x are more resistive than the PECVD SiN_x layer a negative charge can become trapped at the LPCVD/PECVD SiN_x interface due to leakage in the PECVD SiN_x under high electric fields, this charge cannot quickly escape the structure as the time constants when in this state are much longer, layers only conduct under high electric field via a Poole-Frenkel mechanism. The negative-charge hysteresis and V_{th} shift seen in Figures 3, 5 and 6 can be explained by this mechanism. In this paper we have considered charge storage above the channel, charge storage in the GaN:C buffer can cause a dynamic on-resistance [17].

Methods for controlling current collapse and leakage in AlGaN/GaN HEMTs include gate edge shaping [18], optimization of the buffer [19], and optimizing epitaxial thickness [20]. Modifying the stoichiometry of the LPCVD SiN_x provides an additional parameter which should be considered when optimizing devices for current collapse and leakage. However, this SiN_x can change the off-state lateral and vertical electric field profile due to enhancement of FP pinch-off voltages, this effect should be considered when maximizing reliability with FP structures.

V. Conclusion

The LPCVD silicon nitride's DCS/NH_3 ratio has a strong effect on fieldplate pinch-off and has an influence on the current-collapse and leakage tradeoff in GaN HEMTs. Changing the nitride stoichiometry changes the dielectric leakage, and in a multilayer dielectric stack this will modify the FP threshold voltages, introduce an unwanted time dependence and alter electric field control in the channel, modifying FP optimization.

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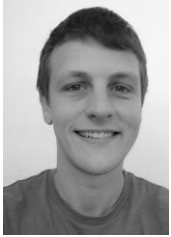
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