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Neutral Points Voltage Balancing Control of a Four-level π -type Converter

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Abstract—In this paper, a carrier-based modulation method with optimal zero-sequence signal injection has been introduced to modulate a four-level π -type converter as well as regulate its DC-link neutral points' voltages. The two neutral points' voltages can be well controlled with a back-to-back configuration even under high modulation index and high power factor. A back-to-back experimental system has been built and tests under 300V have validated this control strategy.

Keywords—energy efficiency and industrial applications; power converters, control, and modeling

I. INTRODUCTION

Multilevel converters provide an effective way to process voltages higher than the individual switching device rating through various topologies. In industry, they are commonly used in medium voltage (3~33kV) high power applications. They are also recently considered in low-voltage (200~460V) applications as an alternative to the conventional two-level converter [1]. Compared with a two-level converter, to achieve equivalent output harmonics, the switching frequency of multilevel converters can be kept low, thus reducing the switching losses and shrinking the heatsink size. On the other hand, if operated at the same switching frequency, the filter size of multilevel converters can be smaller. Either way will improve the system power density, which is favoured in more electric aircrafts, electric/hybrid vehicles, solar or wind power generation, where converter power density is an important factor. In addition, the switching loss of multilevel converters is generally lower than the two-level converter due to the use of lower voltage-rating devices and lower switching voltage [2]. This means the efficiency drops insignificantly with the increase of the switching frequency [3], which provides the possibility to further increase the switching frequency and achieve a higher power density system.

The main concern of multilevel converters is the increased complexity regarding the circuit and control. Converter topologies that generate output voltages of more than three levels have been studied [4, 5]. An alternative four-level π -type converter was introduced with only six switching devices per phase leg [6]. This topology does not need the clamping diodes or flying capacitors as required in the diode neutral-point-clamped (NPC) converter or flying capacitor (FC) converter,

which simplifies the circuitry. The advantages of this topologies have been detailed in [3, 6]. Similar to other multilevel converter topologies, the four-level π -type converter also has the unbalanced neutral points' voltages problem [7-9], and this issue will cause system instability and affect the output harmonics. Space vector modulation (SVM) for normal four-level converters have been researched [4, 7, 10]. The advantage of SVM is it has the ability to regulate the neutral points' voltages through the selection of redundant vectors. However, when SVM is used for a converter which has more than four voltage levels, the selection of voltage vectors, calculation of the time duration of each vector and the arrangement of the sequence of each vector become very complicated and computationally intensive. Thus, the carrier-based modulation can be seen as a better option for multilevel converters. With the injection of an appropriate zero-sequence component into the fundamental signals, the effect of the carrier-based modulation will not only be equivalent to SVM [11, 12] but simpler. Previous papers regarding neutral points' voltages balancing agree that the DC-link capacitors' voltages can only be balanced with a back-to-back configuration (rectifier + inverter) if the modulation index and power factor is high [9, 10, 13, 14] for four-level or five-level NPC converters. The neutral points' voltage balancing control and experiments based on coordination between rectifier and inverter switching angles have been presented [15, 16]. However, in a real case, the grid and load conditions can vary independently and it may not be practical to set a fixed relationship between the rectifier and inverter, e.g. similar modulation indexes at both sides. In [9], an independent neutral point voltage balancing control of the inverter and rectifier for a five-level back-to-back converter has been proposed without experimental validation. This paper continues the work in [6], and proposes a carrier-based modulation control strategy, which has the ability to balance the neutral points' voltage regardless the conditions of the rectifier or inverter, e.g. with different modulation index and power factor, and simplifies the control complexity at the same time. A back-to-back converter with 300V DC-link voltage experiment has validated this control strategy.

II. CONVERTER STRUCTURE AND MODULATION

Fig.1 shows the phase-leg structure of a four-level π -type converter. T1 and T6 need to withstand the whole DC-link

voltage ($3E$). T3 and T4 are required to hold $2/3$ of the DC-link voltage ($2E$), and T2, T5 will have to hold $1/3$ of the DC-link voltage (E). A carrier-based modulation scheme concept for this topology is shown in Fig.2. The intersection of the modulation wave and each carrier wave determines the switching states of one pair of the switching devices in a complementary manner. In practical implementation, the comparison and modulation can be simplified by using a single carrier wave and dividing the modulation wave into three parts.

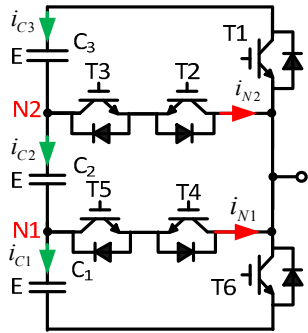


Fig.1. Four-level π -type converter phase-leg structure

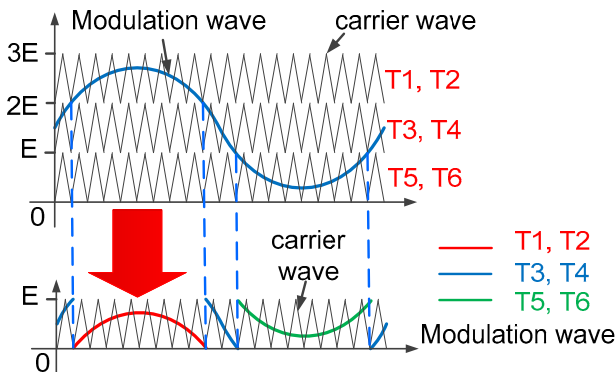


Fig.2. Carrier-based modulation scheme for a four-level π -type converter

Table I summarizes the switching states at different voltage levels.

TABLE I. SWITCHING STATES AND OUTPUT VOLTAGE LEVEL

| Device | T1 | T2 | T3 | T4 | T5 | T6 |
|--------|-----|-----|-----|-----|-----|-----|
| 3E | ON | OFF | ON | OFF | ON | OFF |
| 2E | OFF | ON | ON | OFF | ON | OFF |
| E | OFF | ON | OFF | ON | ON | OFF |
| 0 | OFF | ON | OFF | ON | OFF | ON |

III. NEUTRAL POINTS' VOLTAGES BALANCING CONTROL

As a multilevel converter, the four-level π -type converter has the issue of the neutral points voltage drift at its DC-link side. Fig.3 shows the condition of the currents flowing through neutral points during different commutation periods. For a four-level π -type converter, the neutral points' voltages are affected by the charge and discharge situation of the middle capacitor ($C2$). When load power factor equals to 1, in one fundamental period, $C2$ keeps discharging. Thus, the voltage across $C2$ will decrease to zero gradually and causes the converter neutral points' voltages unbalancing. On the other hand, when load power factor equals to 0, in one fundamental

period, there're two parts relating to the charging process and two other parts relating to the discharging process for $C2$. In this situation, the converter can automatically balance its neutral points' voltages. Fig.4 shows this phenomenon, and indicates that the higher the power factor, the harder the neutral points' voltages can be balanced.

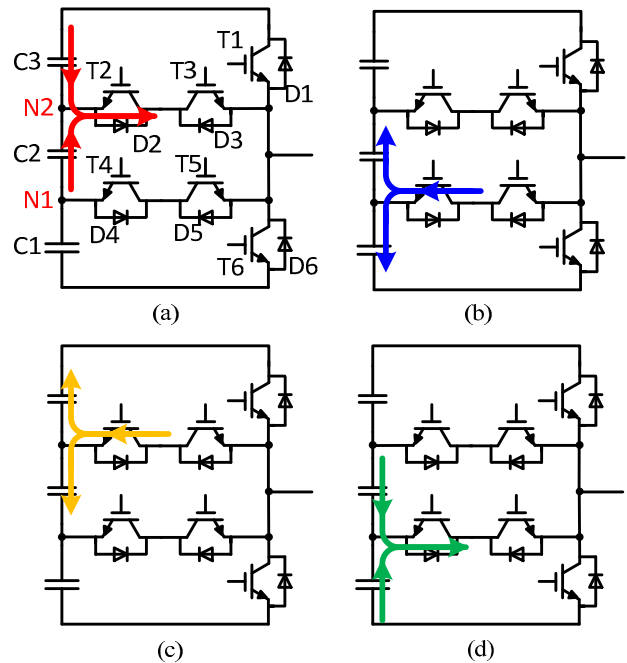


Fig.3. Currents flow through neutral points during different commutation periods (a) N2 to inverter (b) inverter to N1 (c) inverter to N2 (d) N1 to inverter

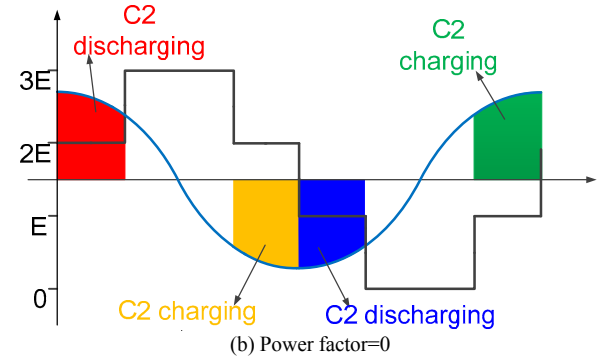
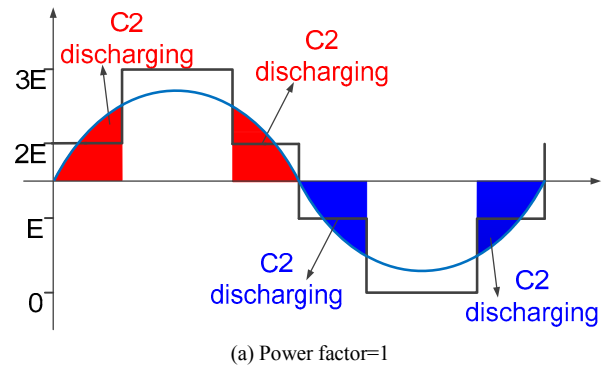


Fig.4. Charge and discharge condition of $C2$

Thus, a control method needs to be identified to adjust the currents flowing through the DC-link capacitors especially the

ones flow through C2, which can help to achieve the neutral points' voltages balancing even at a high power factor condition. As the carrier-based modulation is employed here to simplify the modulation process. With an appropriate zero-sequence signal injection, the four-level π -type converter can be well modulated and the DC-link neutral points' voltages can be balanced at the same time.

The reference voltage (modulation signal) for the converter is composed of two parts: fundamental components (three-phase sinusoidal waveforms) and a zero-sequence component as given in (1).

$$u_i(t) = u_i^*(t) + c(t) \quad i = a, b, c \quad (1)$$

Where, $u_i(t)$ is the reference voltage; $u_i^*(t)$ is the fundamental component; $c(t)$ is the zero-sequence component. The fundamental components are obtained from the output of the current control loop, which are used to control the fundamental current of the converter to track the reference. The zero-sequence component can be adjusted and added to the three-phase fundamental components simultaneously to achieve neutral points' voltages balancing. For the computational convenience, set the phase reference voltage normalized with 1/3 of the total DC-link voltage (e.g. E in Fig.1), then the per unit value of the phase reference voltage with regard to the negative DC-bus will be in the range of 0~3. Therefore, the maximum as well as the minimum zero-sequence component $c(t)$ which can be injected to the three-phase fundamental signals can be expressed as

$$-u_{\min}^*(t) \leq c(t) \leq 3 - u_{\max}^*(t) \quad (2)$$

Where, u_{\max}^* and u_{\min}^* are the maximum and minimum value of the three-phase fundamental components and are given by

$$\begin{cases} u_{\min}^*(t) = \min(u_a^*(t), u_b^*(t), u_c^*(t)) \\ u_{\max}^*(t) = \max(u_a^*(t), u_b^*(t), u_c^*(t)) \end{cases} \quad (3)$$

After the available range of zero-sequence signal is derived by (2), the optimized zero-sequence signal can be selected from it. Although the optimized zero-sequence signal for neutral points' voltages balancing target may be derived analytically, sampling several values within the given range could be a simpler way. For example, ten values can be selected equally within the range in (2) and evaluated against the control objective. The one which leads to the optimized value of the control objective will be selected. In order to balance the DC-link capacitors' voltages, the control objective can be set to minimize the capacitor's energy as given in (4) [9, 10, 14, 18].

$$J = \frac{1}{2} C \sum_{j=1}^3 \Delta v_{Cj}^2 = \frac{1}{2} C \sum_{j=1}^3 (v_{Cj} - \frac{V_{dc}}{3})^2 \quad (4)$$

Where Δv_{Cj} is the voltage deviation of capacitor C_j in Fig.1 from 1/3 of the total DC-link voltage. v_{Cj} is the individual

capacitor voltage. V_{dc} is the DC-link voltage. C is the capacitor value. Once an optimized zero-sequence signal is selected, J can be minimized (ideally reduced to zero) when the capacitors' voltages are regulated at the reference value of 1/3 of the total DC-link voltage. To simplify control implementation, it is better to calculate the derivative of (4) as shown in (5). When capacitor energy is minimized, the value of (5) becomes negative.

$$\frac{dJ}{dt} = C \sum_{j=1}^3 \Delta v_{Cj} \frac{dv_{Cj}}{dt} = \sum_{j=1}^3 \Delta v_{Cj} i_{Cj} \leq 0 \quad (5)$$

Where, i_{Cj} is the current flowing through the capacitor C_j as shown in Fig.1. Therefore, the control objective can be set as in (6) and the control variable is the zero-sequence component with the defined range in (2).

$$\begin{cases} \min J = \sum_{j=1}^3 \Delta v_{Cj} i_{Cj} = \sum_{j=1}^3 (v_{Cj} - \frac{V_{dc}}{3}) \cdot i_{Cj} \\ \text{Constraint: } -u_{\min}^*(t) \leq c(t) \leq 3 - u_{\max}^*(t) \end{cases} \quad (6)$$

The next step is to find out the relationship between the control objective and zero-sequence signal so that each zero-sequence signal can be evaluated against the control objective. The relationship between capacitor current i_{Cj} in (6) and the neutral point currents i_{N1} , i_{N2} can be derived according to Fig.5.

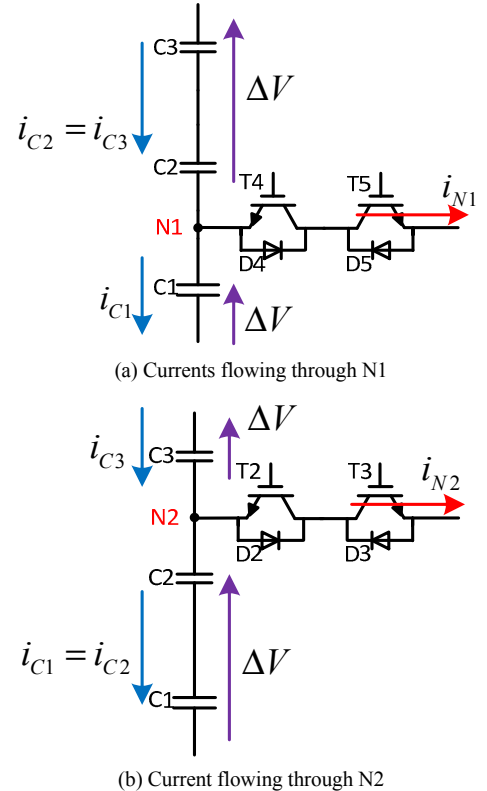


Fig.5. Transients during currents flowing through neutral points

For the transient state in Fig.5 (a), when the current flows through N1, assume the voltage change on C1 is equal to the

voltage change on C2 and C3. While for the transient state in Fig.5 (b), when the current flows through N2, assume the voltage change on C3 is equal to the voltage change on C1 and C2. Therefore, the relationship can be derived as

$$\text{inverter} \begin{cases} i_{C1} = -\frac{1}{3}i_{N2} - \frac{2}{3}i_{N1} \\ i_{C2} = -\frac{1}{3}i_{N2} + \frac{1}{3}i_{N1} \\ i_{C3} = \frac{2}{3}i_{N2} + \frac{1}{3}i_{N1} \end{cases} \quad \text{rectifier} \begin{cases} i_{C1} = \frac{1}{3}i_{N2} + \frac{2}{3}i_{N1} \\ i_{C2} = \frac{1}{3}i_{N2} - \frac{1}{3}i_{N1} \\ i_{C3} = -\frac{2}{3}i_{N2} - \frac{1}{3}i_{N1} \end{cases} \quad (7)$$

Since the reference voltage has been normalized within the range of 0~3, the integer part of the voltage reference (u_i) represents the voltage level and the fractional part determines the duty cycle. This significantly simplifies the calculation to find out the relationship between neutral points currents, modulation signal and phase current. For example, if the reference voltage is 1.2, it means the voltage level is 1 and duty cycle is 0.2. Therefore, the output voltage will switch between E and 2E. Specifically, the output voltage will be E for 80% of the switching period with switches T4 and T5 ON, where the phase output current flows through i_{N1} . The output voltage will be 2E for 20% of the switching period with switches T2 and T3 ON, where the phase current flows through i_{N2} . Therefore, the neutral currents (i_{N1} , i_{N2}) can be determined by the reference voltage level (integer part of the reference voltage) and the duty cycle (fractional part of the reference voltage). The illustration of the voltage level and duty cycle with regards to the integer and fractional part of the reference voltage is shown in Fig.6.

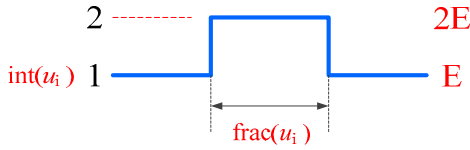


Fig.6. Illustration of the reference voltage level and duty cycle

The reference voltage u_i can be adjusted by the zero-sequence component, which gives the reason the zero-sequence component can affect the neutral paths currents, the corresponding capacitor currents and the control objective in (6). The relationship between the neutral point current and the reference voltage (including zero-sequence voltage) can be formulated as in (8) [12, 19, 20].

$$\begin{cases} \bar{i}_{N1} = \sum_{i=a,b,c} i_i \times [(\text{int}(u_i) = 0) \times \text{frac}(u_i) + (\text{int}(u_i) = 1) \times (1 - \text{frac}(u_i))] \\ \bar{i}_{N2} = \sum_{i=a,b,c} i_i \times [(\text{int}(u_i) = 1) \times \text{frac}(u_i) + (\text{int}(u_i) = 2) \times (1 - \text{frac}(u_i))] \end{cases} \quad (8)$$

Where, $\text{int}(u_i)$ represents the integer part (voltage level) of the reference voltage and $\text{frac}(u_i)$ represents the fractional part (duty cycle) of the reference voltage. i_a , i_b , i_c are the converter phase currents. $\text{int}(u_i) = 0$ is used to check whether the reference voltage level is 0 or not. If it is zero, then $(\text{int}(u_i) = 0)$ equals to 1, otherwise 0. It can be seen that only when the voltage level is 0 or 1, the phase current may flow through i_{N1} . When the voltage level is 1 or 2, the phase current

may flow through i_{N2} . And the amount of current flows through the neutral points will be determined by duty cycle.

With (1)-(8), the relationship between the control objective and the zero-sequence signal can be established. In summary, the modulation and neutral points' voltages balancing algorithm can be implemented as follows. First, the three-phase fundamental components are obtained from the current control loop. Second, using (2), the range of zero-sequence component can be derived. Third, equally sample several values within the range of the zero-sequence component, and add to the fundamental component to obtain the reference voltage. Fourth, using (8), (7) to check which zero-sequence component leads to the minimum value of the objective function in (6). That zero-sequence component will be selected to form the final reference voltage. After the reference voltage is obtained, it will be compared with three triangle carrier-signals to generate the appropriate PWM signals to the devices gate drivers. The algorithm flow chart in Fig.7 is able to present this control strategy intuitively.

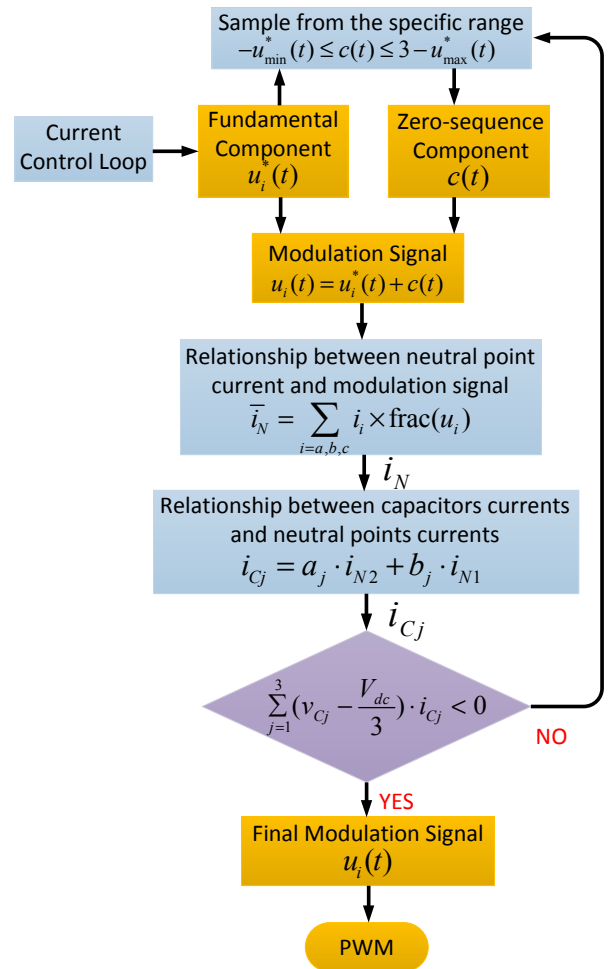


Fig.7. Neutral points' voltages balancing algorithm

It should be noted that although the above algorithm attempts balance the voltage on each DC-link capacitor, the neutral points' voltages balancing can only be achievable if the modulation index is limited to about 0.6 with the load power factor is limited to 0.8 [8]. From the point of view of SVM, the

best DC-link capacitors voltages balancing quality can be achieved when there's no restriction for the selection of the redundant vectors. When the modulation indices are of high values, fewer redundant switching vectors are available for the neutral points' voltages balancing activities [7, 10]. Meanwhile, from the carrier based modulation point of view, higher modulation indices signifies a smaller range of the zero-sequence components can be selected. If the high modulation index and high power factor are required, a back-to-back configuration should be established as in Fig.8. With a back-to-back configuration, the unbalance tendencies of both sides have a potential to compensate each other because of the symmetry of the system. With proper control strategy, the net current flowing into each neutral point during each fundamental period can be controlled as closed to zero as possible, the current and power flowing through the neutral points (N1 and N2) can be coordinated, therefore achieve the neutral points' voltages balancing [8].

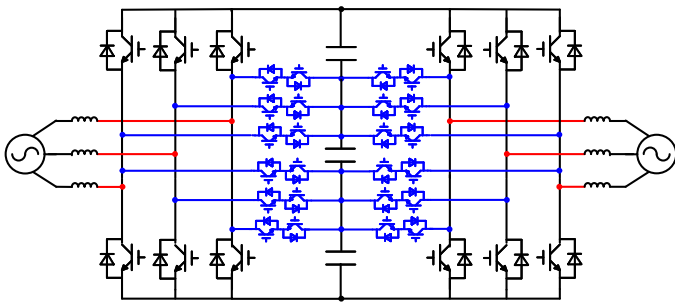


Fig.8. Schematic of a back-to-back four-level π -type converter

IV. SIMULATION RESULTS

A simulation system has been established in MATLAB/Simulink according to the configuration in Fig.8. In order to present the capacitors' voltages balancing ability of this control strategy, the different modulation indices situation has been presented here. The input grid side RMS line voltage is 342V. The DC-link voltage is controlled to be 650V. This gives modulation index of 0.9 at the rectifier side. The load side RMS line voltage is 187V, which means the inverter side modulation index is 0.55. The rectifier side choke set is $R=0.1\Omega$, $L=5\text{mH}$, and the inverter side load is $R=25\Omega$, $L=1\text{mH}$, which means the power factors on both sides are close to 1. The switching frequency is 10 kHz.

Fig.9 (a) shows the rectifier AC-side line voltage and phase voltage. The line voltage has seven levels and phase voltage has four levels as expected. There are some distinct pulses appearing in the phase voltage, which is due to the injection of the optimized zero-sequence signals for the DC-link neutral points' voltages balancing. These pulses do not affect the line voltage as they can cancel out between phases. Fig.9 (b) shows the inverter output line voltage and phase voltage. The line voltage has five levels and phase voltage has three levels as expected. Fig.9 (c) shows the voltage distributions of the three DC-link capacitors. They have been well regulated around 216V which is a third of the total DC-link voltage of 650V.

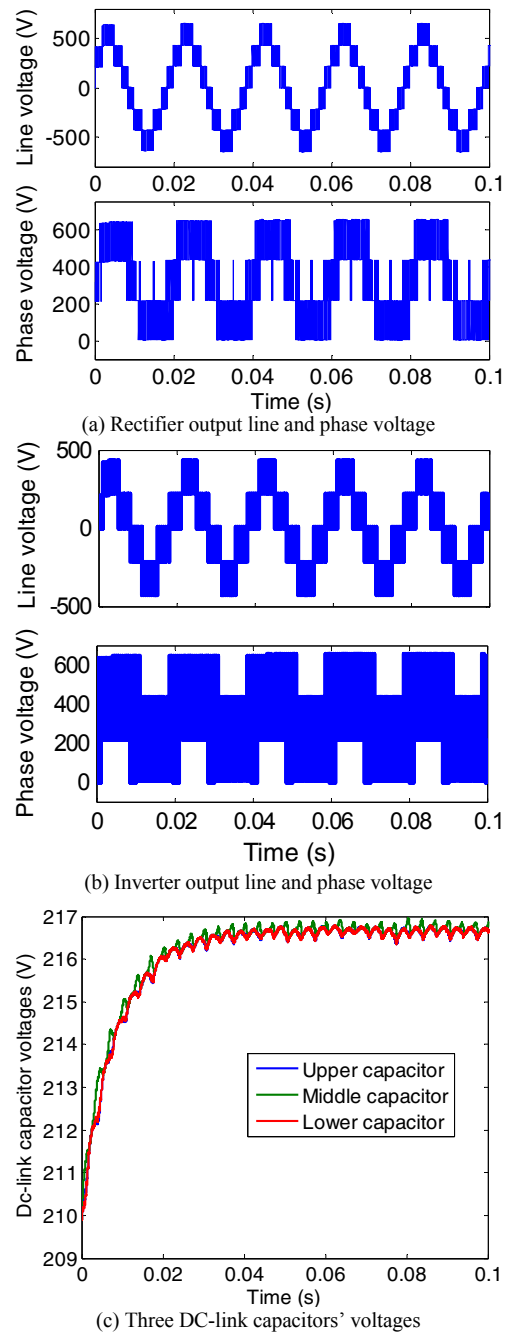


Fig.9. Simulation results with a back-to-back four π -type converter

V. EXPERIMENTAL RESULTS

The devices in Table II are used to establish the prototype for the test as shown in Fig.10. The converter prototype is designed for an output of 5kW maximum and allows the switching frequency to be set in a range from 5 kHz to 50 kHz with a maximum 900V DC-link voltage. It has been tested with a 600V DC-link voltage and 3kW output power from 10 kHz to 50 kHz switching frequency for an inverter open loop test in [3]. For a back-to-back closed-loop neutral points' voltages balancing test, two converter boards are required and stacked. They are both controlled by a XC3S400 FPGA with TMS320F28335 DSP control board.

TABLE II. SELECTED IGBT FOR THE CONVERTER PROTOTYPE

| Switch | Device |
|----------------|-------------|
| T1, T6 | FGW15N120VD |
| T2, T3, T4, T5 | IKW30N60H3 |

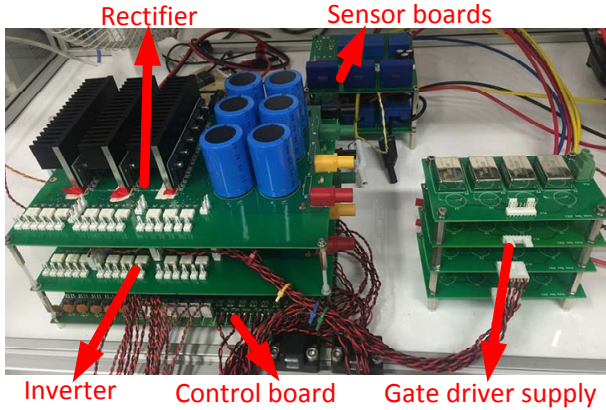


Fig.10. Experimental setup

The test setup also included a three phase 5mH inductive choke (equivalent resistance 0.2Ω) at the input of the rectifier, a three-phase star-connected resistance-inductance load ($R=44\Omega$, $L=6.32mH$) for the output of the inverter side. This means the power factor on both sides is close to 1. The DC-link voltage is set as 300V. Each DC-link capacitor $C=1000\mu F$, thus the total equivalent DC-link capacitance is $1333.33\mu F$. The fundamental frequencies and switching frequencies on both sides are 50 Hz and 10 kHz, respectively. Due to the rectifier side is grid-connected, a Proportional-Integral (PI) control based DC-link voltage loop and current loop are applied to the rectifier side. An open loop voltage control is applied to the inverter side. The proposed DC-link neutral points' voltage balancing control is employed on both sides. Set the modulation index of rectifier $m_{rec}=0.9$, and the modulation index of inverter is $m_{inv}=0.9$ as well.

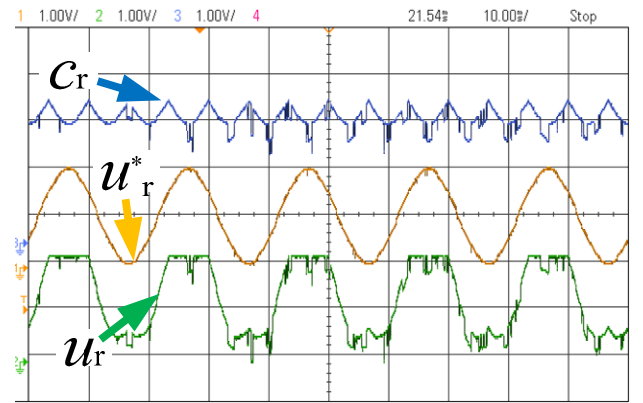
Using an AD5725 DAC chip, the internal variables in the code can be monitored. The modulation waveforms as well as the injected zero-sequence signal waveforms on both sides can be monitored through DAC and are shown in Fig.11 (a) (b). In order to get rid of the noise, the acquisition mode used here is high resolution mode. The yellow waveforms represent the fundamental components which are sinusoidal. The blue waveforms are the selected the zero-sequence components through the method in Section III, and their frequencies are triple of the ones of the fundamental components. The green waveforms are the final modulation signals by adding previous two waveforms together.

Given the complexity of the control algorithm, the control program processing is not instant and requires the time consumption. To execute the code for one time the actual period is evaluated as $140\mu s$. It has been shown in Fig.11 (c) by zooming in the waveform in Fig.11 (a). This period is still larger than the actual switching period which is $100\mu s$. This time difference will reduce the rectifier side voltage loop and current loop control bandwidth, and cause the control delay as it is grid connected. This will cause the rectifier side currents distortion to some extent.

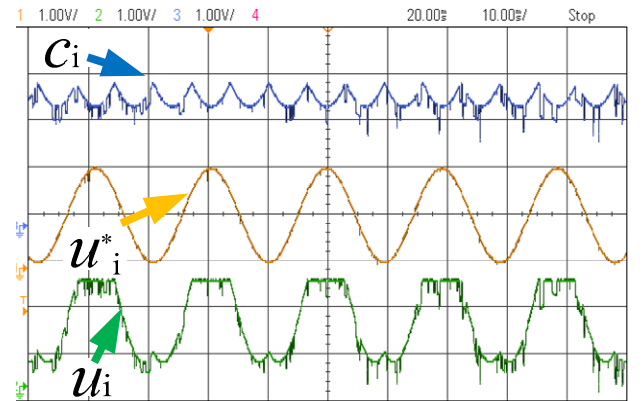
Fig.11 (d) shows the rectifier output phase voltage as well as line voltage. The phase voltage has four levels and the line voltage has seven levels as expected. The inverter voltage waveforms in Fig.11 (f) have the same features as the rectifier side ones have. Fig.11 (e) shows the three-phase rectifier AC side currents. Because of the delay problem mentioned before, there is a bit low frequency distortion in the rectifier currents waveforms. Fig. 11 (g) presents the inverter AC side three phase sinusoidal currents.

Fig.11 (h) shows the grid side phase voltage as well as the grid side current. As the rectifier power factor is close to 1, thus these two waveforms are in phase with each other.

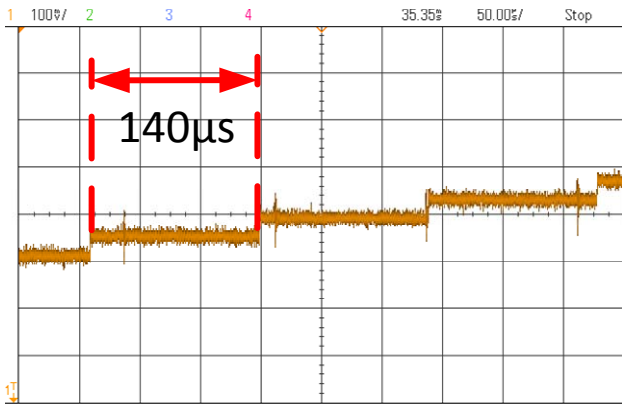
Fig.11 (i) shows three DC-link capacitors' voltages. They are well balanced through this control method. Due to the three voltage probes used are three different types, the noise on the waveforms are different. Fig.11 (j) presents these three DC-link capacitors' voltages more clearly by setting the offset in different values.



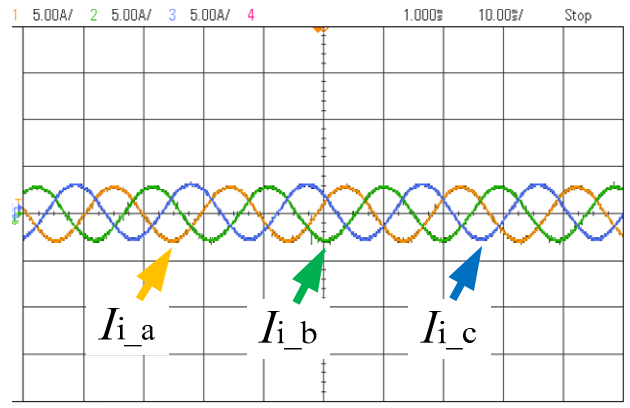
(a) Rectifier modulation and zero-sequence signals



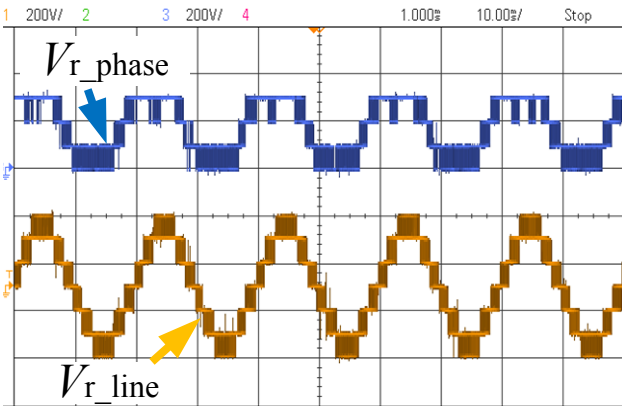
(b) Inverter modulation and zero-sequence signals



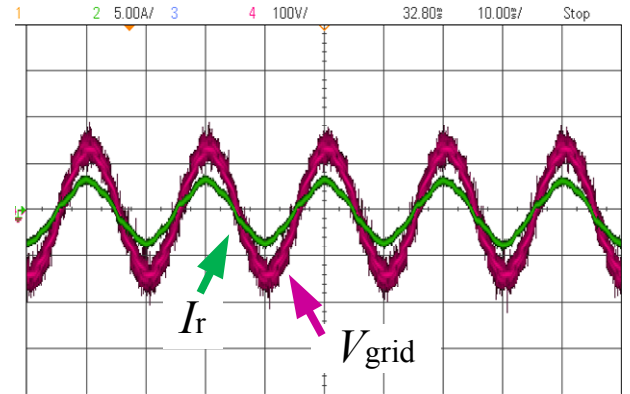
(c) Actual time period of each AD sampling interrupt



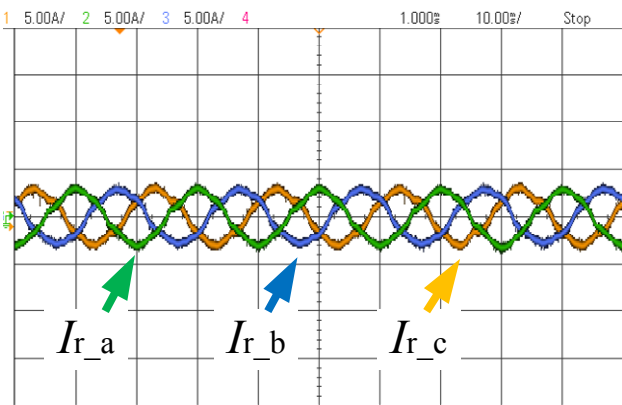
(g) Inverter AC side three-phase currents



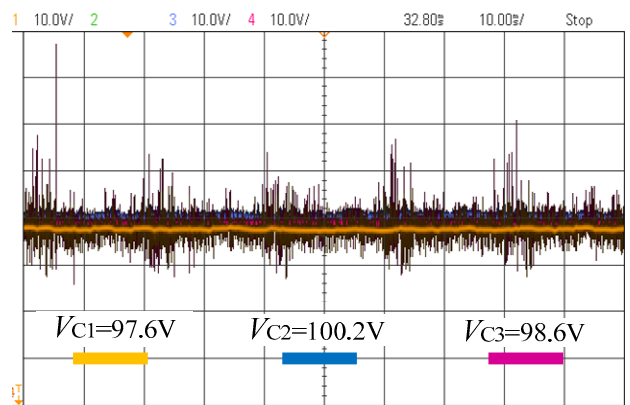
(d) Rectifier output phase and line voltages



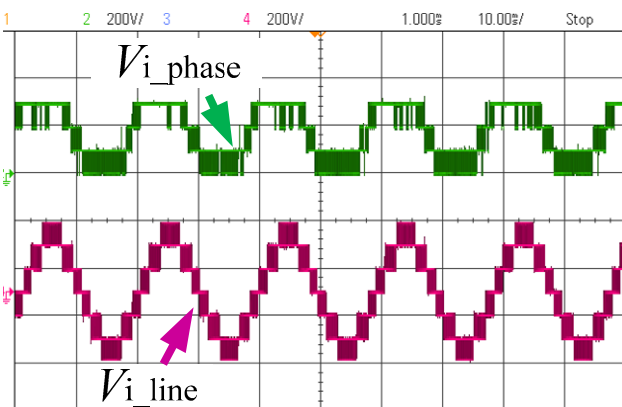
(h) Grid voltage and current



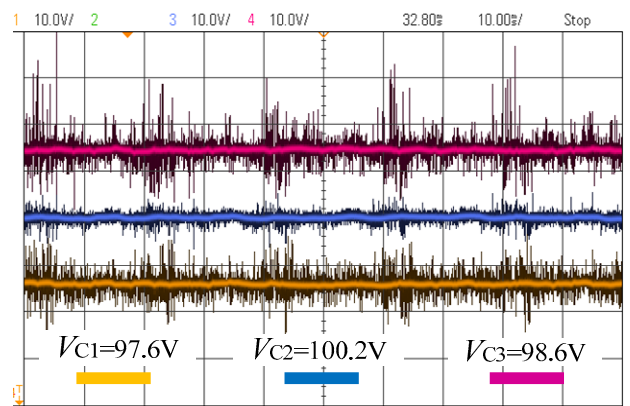
(e) Rectifier AC side three-phase currents



(i) Three DC-link capacitors voltages



(f) Inverter output phase and line voltages

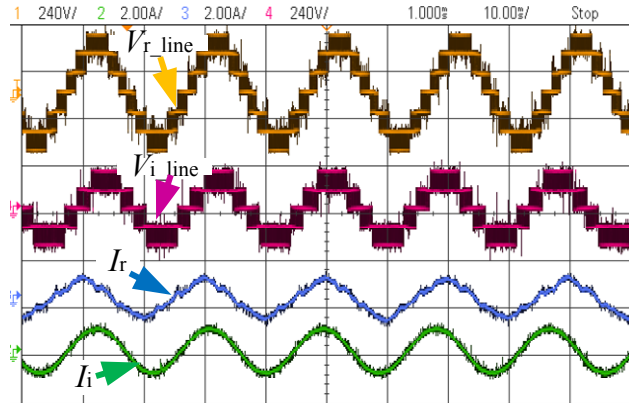


(j) Three DC-link capacitors voltages when offset values are different

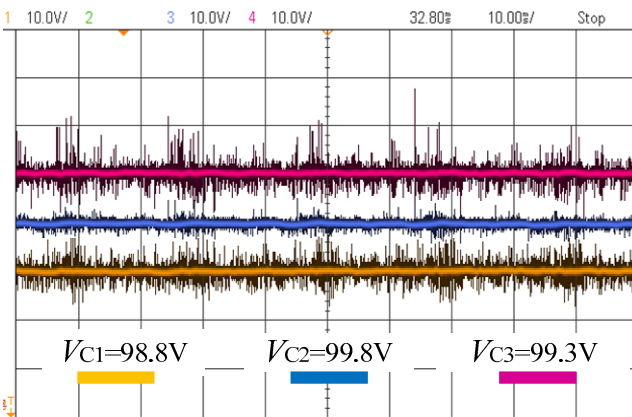
Fig.11. Experimental results of the equal modulation indices on both sides

The condition of the different modulation indices on each side has been tested as well. Set the modulation index of rectifier $m_{rec}=0.9$, and modulation index of inverter is $m_{inv}=0.6$. In this case, the rectifier side line voltage has seven levels while the inverter side line voltage only has five levels as shown in Fig.12 (a). Due to the inverter side modulation index is low, it can be deemed as a load shedding condition. Therefore the total power is reduced. The power transfer on both sides is equal, however the rectifier side voltage is higher than the inverter side voltage, thus the rectifier current is lower than the inverter current in this situation.

Fig.12 (b) shows the three DC-link capacitors' voltages. They are also well regulated at 1/3 of the total DC-link voltage when the modulation indices on both sides are different.



(a) Line voltage and current waveforms on both sides



(b) DC-link capacitors' voltages

Fig.12. Experimental results of the different modulation indices on both sides

VI. CONCLUSION

This paper introduced a carrier-based neutral points' voltages balancing control strategy for the four-level π -type converter. This control method has the ability to control DC-link capacitors' voltages independently on either rectifier or inverter side. It can also greatly simplify the modulation process compared with the SVM. A 300V DC-link voltage back-to-back experiment has validated this control strategy. The DC-link neutral points' voltages are well balanced with high power factor and different modulation indices at the rectifier and inverter sides.

REFERENCES

- [1] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electronics*, vol. 28, no. 2, Feb. 2013, pp. 899 - 907.
- [2] X. Yuan, "Analytical averaged loss model of a three-level T-type converter" in *Proc. IET PEMD'14 Conf.*, Apr. 2014, pp. 1 - 6.
- [3] B. Jin and X. Yuan, "Power loss and efficiency analysis of a four-level π -type converter," in *Proc. IEEE EPE'15 Conf.*, Sept. 2015, pp. 1 - 10.
- [4] G. Sinha and T. A. Lipo, "A four-level inverter based drive with a passive front end," *IEEE Trans. Power Electronics*, vol. 15, no. 2, Mar. 2000, pp. 285 - 294.
- [5] G.S. Perantzakis, F.H. Xepapas, and S. N. Manias, "A novel four-level voltage source inverter—influence of switching strategies on the distribution of power losses," *IEEE Trans. Power Electronics*, vol. 22, no. 1, Jan. 2007, pp. 149 - 159.
- [6] X. Yuan, "A four-level π -type converter for low-voltage applications," in *Proc. IEEE EPE'15 Conf.*, Sept. 2015, pp. 1-9.
- [7] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Industrial Electronics*, vol. 52, no. 1, Feb. 2005, pp. 190 - 196.
- [8] Z. Pan and F. Z. Peng, "Harmonics optimization of the voltage balancing control for multilevel converter/inverter systems," *IEEE Trans. Power Electronics*, vol. 21, no. 1, Jan. 2006, pp. 211 - 218.
- [9] M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters a practicable way to balance DC-link voltages," *IEEE Trans. Industrial Electronics*, vol. 49, no. 4, Aug. 2002, pp. 752 - 765.
- [10] M. Saeedifard, R. Iravani, and J. Pou, "A Space Vector Modulation approach for a back-to-back connected four-level converter," in *Proc. IEEE PESC'07 Conf.*, Jun. 2007, pp. 2043 - 2049.
- [11] F. Wang, "Sine-triangle versus Space-vector Modulation for three-level PWM voltage-source inverters," *IEEE Trans. Industry Applications*, vol. 38, no. 2, Mar./Apr. 2002, pp. 500 - 506.
- [12] X. Yuan, Y. Li, and C. Wang, "Objective optimisation for multilevel neutral-point-clamped converters with zero-sequence signal control," *IET Power Electronics*, vol. 3, no. 5, Sept. 2010, pp. 755 - 763.
- [13] I. Hasegawa, T. Kondo, and T. Kodama, "Voltage control of common flying capacitors in 5-level converter with capacitor current estimation," in *Proc. IEEE EPE'15 Conf.*, Sept. 2015, pp. 1-10.
- [14] M. Marchesoni, M. Mazzucchelli, and P. Tenca, "An optimal controller for voltage balance and power losses reduction in MPC AC/DC/AC converters," in *Proc. IEEE PESC'00 Conf.*, Jun. 2000, pp. 662 - 667.
- [15] F. Peng, J. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage-source converter system with balanced DC voltages," in *Proc. IEEE PESC'95 Conf.*, Jun. 1995, pp. 1144 - 1150.
- [16] Z. Pan, F.Z. Peng, K.A. Corzine, and V. R. Stefanovic, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," *IEEE Trans. Industry Application*, vol. 41, no. 6, Nov. 2005, pp. 1698 - 1706.
- [17] K. Tian, B. Wu, M. Narimani, and D. Xu, "A capacitor voltage-balancing method for Nested Neutral Point Clamped (NNPC) inverter," *IEEE Trans. Power Electronics*, vol. 31, no. 3, Nov. 2016, pp. 2575 - 2583.
- [18] M. Marchesoni, M. Mazzucchelli, F. V. P. Robinson, and P. Tenca, "A minimum-energy-based capacitor voltage balancing control strategy for MPC conversion systems," in *Proc. IEEE ISIE'99 Conf.*, Jul. 1999, pp. 20 - 25.
- [19] J. K. Steinke, "Switching frequency optimal PWM control of a three-level inverter," *IEEE Trans. Power Electronics*, vol. 7, no. 3, Jul. 1992, pp. 487 - 496.
- [20] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Proc. IEEE IAS'93 Conf.*, Oct. 1993, pp. 965 - 970.