The 5th International Conference on Through-life Engineering Services (TESConf 2016)

Experiment Results of Failure Progression from Low Power Wires

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Abstract

Despite various studies that have been conducted so far on the failure of high power cables, failure progression in low power cables, wires and interconnections have not been well understood yet. In general, it is hypothesised that failures of wires are progressed from random intermittent failures that are gradually developed as hard faults. This paper aims to present a test rig and possible test techniques that can be used for testing the failure progression of wires and interconnections. Research presented in this paper is based on tools, equipment and techniques that facilitate various ageing mechanisms needed to capture proper and right failure patterns from low power cables, wires and interconnections.

1. Introduction

Industrial applications such as aviation systems widely suffer from a specific type of fault that can't be duplicated by evaluating technicians due to their random nature. Hence, the potential failure can't be fixed using conventional techniques. They highly add to the maintenance cost because they remain hidden during the troubleshooting. These types of faults are known as No-fault-fault (NFF) [1-3]. In the literature, they have been also called as Fault-No-Found (FNF), No-Fault-Apparent (NFA), Fault-Cleared-During-Investigation (FCDI), and etc.

The cause of NFF is attributed to various mechanical, chemical, environmental and human issues including oxidation, mechanical stresses (vibration) electromagnetic fields, poor design and bad/wrong operation. They cause various intermittency issues in; for instance, chassis, PCBs, connectors, cables and wires as the system is gradually aged.

Intermittent fault [4] is a malfunction of a device or system that occurs at intervals, usually irregular, in a device or system that functions normally at other times. In many industrial applications such as in-line replaceable unit (LRU) of aviation systems, intermittent faults found in the power chain of a system can be cascaded into other electronic circuitry,

processors, microcontrollers, and memories causing random intermittent failures [5]. Various strategies and efforts in detecting and isolating intermittent fault have been presented in [6-8]. Wakil [9] also discuss that intermittency can be detected by injecting a fixed frequency sinusoidal signal into electronics interconnection system.

It can be hypothesised that the property of a failure sign such as amplitude, duration and repetition of failure signal is increased as the system is gradually aged. At an earlier stage of fault progression (stage 1 in Fig. 1), random low-level noises are seen in the failure signal; however, the system would be subject to intermittency and NFF if duration and amplitude of spikes get to certain levels (stage 2). System degradation mechanisms further develop semi-hard faults and permanent hard faults, stage 3 in Fig. 1. Testing such a hypothesis requires the development of proper test rigs that facilitate various accelerated gaining mechanisms conducted on wires, cables, interconnections, and etc. In this regards, number of challenges that should be taking into account are:

- *Lack of knowledge:* Fault detection technology from low power wires is not well understood.
- *Sampling speed:* At an earlier stage of degradation, spike-like variations in the failure signal look like as noises that

contain higher frequency contents. Hence, a high-speed sampling is required for capturing tools to avoid missing important intermittency signs.

- *Resolution:* As the system develops degradation gradually, a high resolution capturing tools would be needed to record changes at higher possible accuracy.
- *The size of degradation profile:* Sampling at higher speed and resolution causes recording a huge degradation data be created even just from a single thin wire as it may take hours or days to fail the wire gradually.
- *Development of test rig:* Development of the test rig to age low power wires needs additional care to avoid noise while providing better-capturing facilities.
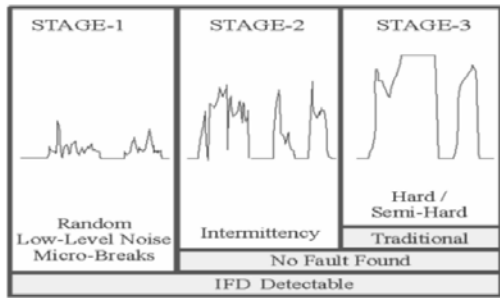

Fig. 1. Three-stage fault progression [4].

In order to contribute to knowledge for providing a better understanding of failure progression mechanisms in low power wires and connections, this paper presents a simple capturing technique that supports reasoning needs where small changes in the failure patterns are almost missed out due to spike like changes at an earlier stage. In this regard, a test rig that assists us to age single and multi-strand thin wires is developed, too. Then results are presented; however, testing the earlier mentioned hypothesis in regards to fault progression is left for future work along with signal analysis steps needed for interpreting failure patterns and characterising property of intermittency.

The rest of the paper will be as follow; section 2 will consist of the test platform, where it shall be further explained the created test rig, its mechanisms and limitations in accelerating ageing mechanisms of single/multi-strand wires including concepts and principles of possible test techniques that can be conducted using the developed test rig. Section 3 shall cover a model for the test rig describing changes in the resistance of the wires under tests. Results are presented in section 4. Lastly, section 5 shall cover the conclusion.

2. Test Rig

A test rig that facilitates three different ageing mechanisms on low power multi-strand wires has been created, Fig. 2. Concepts of tests are summarised in the Fig. 3, 4, and 5. First test facilities cutting strands of wire one by one, gradually, Fig. 3. Next test ages wire by twisting them using a motor, Fig. 4. Finally, ends of a broken wire are twisted to one another to regenerate their contact again; and then, recreated contact is stressed under pressure in test 3, Fig. 5. Each test is

repeated under four different scenarios. Two scenarios for each test are operated using a switch (SW in Fig. 3, 4 and 5) to manage either a dead or live circuit. Live circuit is fed up using a DC power supply (PS) that powers load of the test circuit (LD) up. The other two testing scenarios vary as:

- *First test:* cutting strands of wire one by one, or cutting the wire under test, gradually, while its strands remain together.
- *Second Test:* twisting a wire under test in one continues direction, or in two frequent directions.
- *Third test:* applying pressure/force on twisted contact of a wire while either pressure is just increased, or increased-released repeatedly in a sequence of present and absence of force.
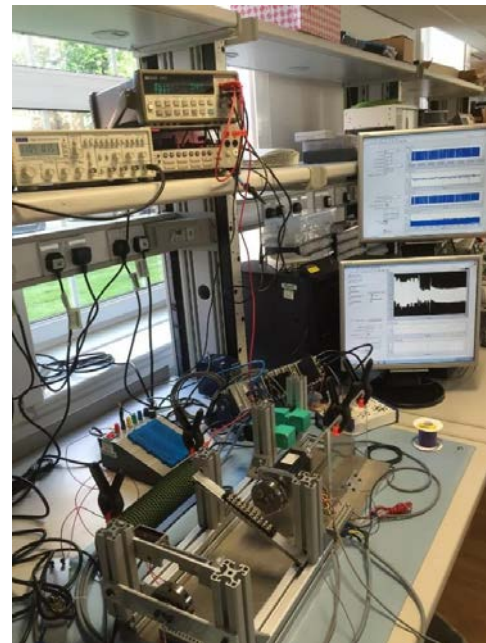

Fig. 2. Created test rig used to age wires and connections at Through Life Engineering Centre, Cranfield University.
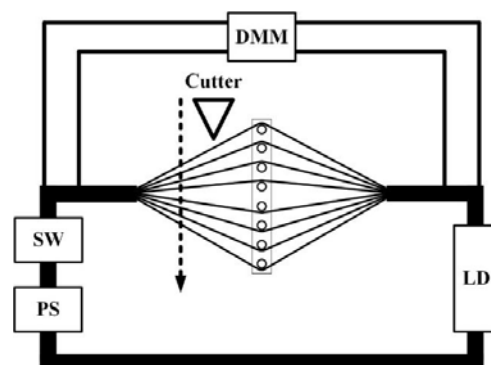

Fig. 3. Test 1, cutting strands of wire one by one. Digital multi-meter presents step changes in the resistance of wire as strands are broken by the cutter.
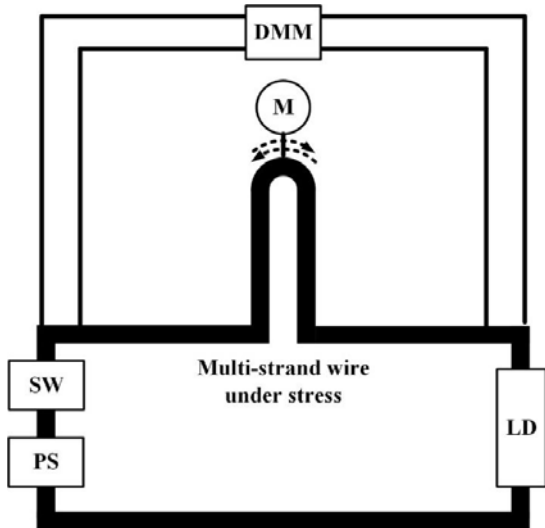
Fig. 4. Test 2, twisting a multi-strand wire. The wire is gradually aged as motor twists wire under test forward and backward.
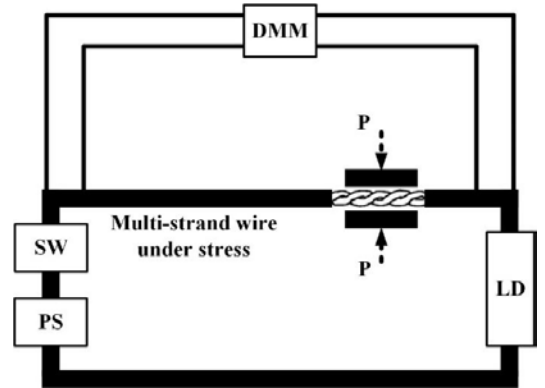

Fig. 5. Test 3, to examine changes in the resistance of wire as the connection is stressed by pressure (P).

All the various testing scenarios are listed in Table 1. In any case, a Digital Multi-Meter (DMM) [10] is used to capture changes in the resistance of wire. The power supply has a 12 volt DC with a maximum current of 1 A. It is not intended to test wires under the condition of AC power supply.

Table 1. List of testing scenarios.

Test type	Mechanical Action	Electrical Action	
		Dead Circuit	Live Circuit
Test 1	Cutting a wire gradually	$S_{1,1}$	$S_{1,3}$
	Cutting the strands one by one	$S_{1,2}$	$S_{1,4}$
Test 2	Twisting (one direction)	$S_{2,1}$	$S_{2,3}$
	Twisting (two directions)	$S_{2,2}$	$S_{2,4}$
Test 3	Pressure is increased, gradually	$S_{3,1}$	$S_{3,3}$
	Pressure is increased and released frequently	$S_{3,2}$	$S_{3,4}$

3. Model of Test Scenarios

Regardless of what ageing mechanism is employed to degrade the wire, the proposed test rig can be modelled by a circuit shown in Fig. 6 from the capturing point of view. In this figure, V_{DMM} and I_{DMM} are voltage was seen and currently produced by DMM, respectively. V_{PS} is a voltage of power supply. R_{Lead}s are the resistance of probes that connect 4-wired DMM to the wire under test. R_{wire} is the resistance of the wire under test that is changed due to degradation; and finally, R_{SW} and R_L are resistances of the switch and the load. R_{SW} can be ignored when the switch is on as its value is too small in comparison with the resistance of the load, R_L. The same, as internal resistance of multi-meter V_{DMM} is too high; hence I_{sense} is ignored so that digital multi-meter senses voltage across the wire under test, V_{Rwire}:

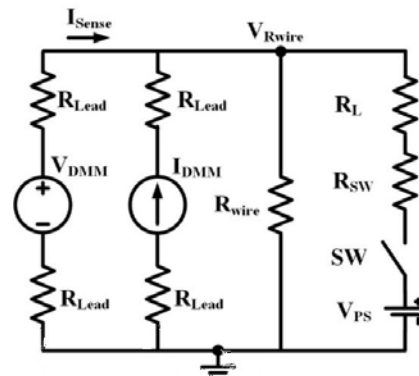$$V_{DMM} = V_{Rwire} \qquad (1)$$

Fig. 6. Model of test rig from the capturing point of view for both the live and dead circuit. R_{wire} is the wire under test.

For a dead circuit, when the switch is off, the circuit of Fig. 6 can be simplified as the circuit in Fig. 7-a. Fig. 7-b is a simplified circuit for when the switch is on considering Norton theorem applied to the power supply and load while ignoring resistance of the switch.
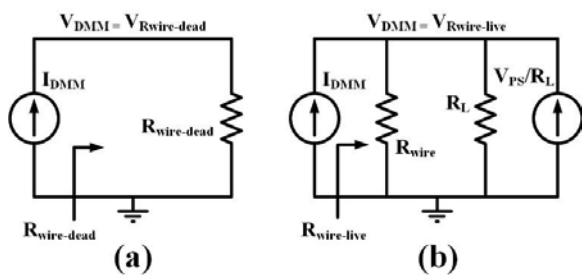

Fig. 7. A simplified model of test rig: a) dead circuit, b) live circuit.

The resistance of wire under test for a dead circuit, $R_{wire-dead}$, is obviously calculated from equation 2, Fig. 7-a:

$$R_{wire-dead} = R_{wire} = V_{Rwire-dead}/I_{DMM} \qquad (2)$$

In the case of a live circuit, $R_{wire-live}$ is amplified in compare with a dead circuit because DMM assumes that wire under test is derived only by I_{DMM}; however, external power supply PS also contributes in the voltage across the R_{wire}. Using KCL of Kirchhoff's law, the voltage across the wire under test is obtained from equation 3 for a live circuit.

$$\frac{V_{Rwire-live}}{R_{wire} \parallel R_L} = I_{DMM} + \frac{V_{PS}}{R_L} \qquad (3)$$

In this experiment, resistance of the wire under test is over 100 times smaller than R_L, hence equation 3 can be rewritten as equation 4:

$$\frac{V_{Rwire-live}}{R_{wire}} = I_{DMM} + \frac{V_{PS}}{R_L} \qquad (4)$$

Equation 4 can be also rewritten as equation 5 and 6:

$$\frac{V_{Rwire-live}}{R_{wire}} = I_{DMM}\left(1 + \frac{1}{I_{DMM}}\frac{V_{PS}}{R_L}\right) \qquad (5)$$

$$\frac{V_{Rwire-live}}{I_{DMM}} = R_{wire}\left(1 + \frac{1}{I_{DMM}}\frac{V_{PS}}{R_L}\right) \qquad (6)$$

V_{PS}/R_L is the current of external power supply, I_{PS}; and from equation 2 it is known that $R_{wire-dead}$ is equal to R_{wire}. Hence, by substituting them in the equation 6:

$$R_{wire-live} = R_{wire-dead}(1 + A_I) \qquad (7)$$

where A_I is amplification gain for the resistance of the wire under test in a live circuit accounted for I_{PS}/I_{DMM}. This amplification helps us to capture changes in the resistance of the wire under test accurately in compare with a dead circuit.

4. Test Results

Results for different test scenarios listed in Table 1 are shown in Fig. 7 to 11. Regardless, when a test is conducted using a dead circuit, captured values of resistance looks so noisy that hardly any clear meaning can be distinguished. In contrast, tests using live circuit provide us much better degradation profile with distinct steps in the pattern of resistance. Steps obviously refer to the moments that strands of a wire are broken, Fig. 9. In fact, each strand is broken in a form of sudden failure. Hence, steps are created in the failure pattern of the wire as strands are broken one by one over time.

Whenever a strand of wire is broken, effective cross-sectional area of whole wire that contribute to the resistance of the wire is reduced, equation 8 [11]:

$$R = \rho \frac{l}{A} \qquad (8)$$

where ρ is resistivity, l is length, and A is cross-sectional area of the wire that is almost equal to the summation of strands' cross-sectional areas, a_i where n is a number of strands.

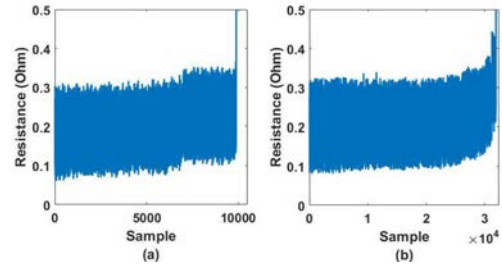$$A = \sum_{i=1}^{n} a_i \qquad (9)$$

Fig. 8. Results for a wire under test 1 when a dead circuit is utilised, a) test scenario $S_{1,2}$, b) test scenario $S_{1,1}$.
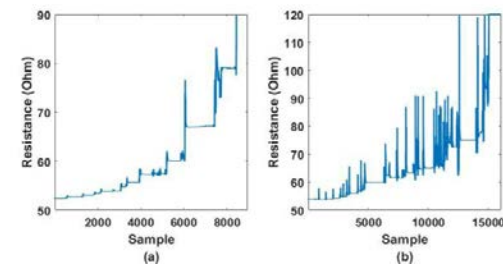

Fig. 9. Results for a wire under test 1 when a live circuit is utilised, a) test scenario $S_{1,4}$, b) test scenario $S_{1,3}$.

Degrading a wire using the twisting mechanism shown in Fig. 3 causes strands to gradually stress and ultimately break. However resistance is increased whenever a strand is broken, but twisting process causes some of the broken strands to get in touch and move across one another for a short period of time. This generates many noises in the pattern of resistance as shown in Fig. 10 and 11. Still steps in the patterns captured from a live circuit, Fig. 11, can be distinguished in contrast with patterns from a dead circuit, Fig. 10. An example of aged wire through twisting test process is shown in Fig. 12.

Similarly, it can be seen in the Fig. 13 that resistance is reduced when the ends of a broken wire are simply twisted and connected under pressure; however, resistance is reduced when pressure is released. In fact, twisting ends of a broken wire to one another provides connection nevertheless the twisted contact of the wire is under pressure or not. Pressure/force just increases contact area; and so, provides a higher cross-sectional area that reduces the contact resistance, equation 9.
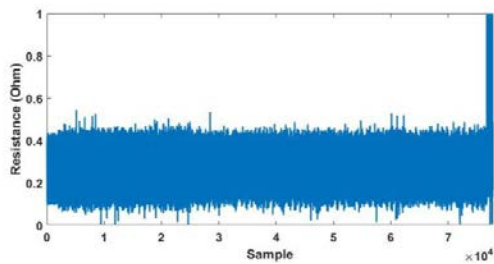
Fig. 10. Twisting the wire under test in a dead circuit, $S_{2,2}$. Meaningful changes in the resistance hardly can be detected.
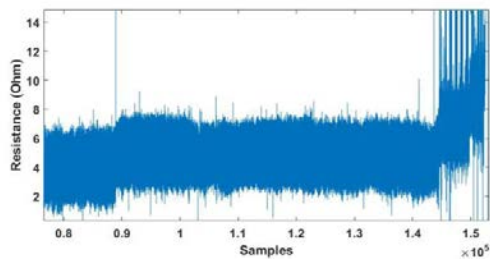

Fig. 11. Twisting the wire under test in a live circuit, $S_{2,4}$.

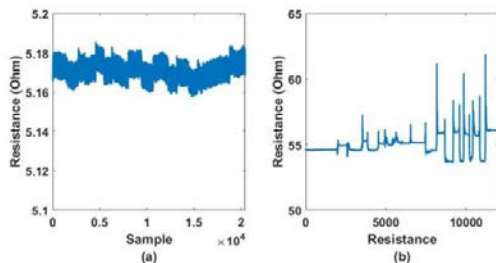Fig. 12. An example of aged wire through twisting test process.

Fig. 13. Results from wire under pressure: a) test 3, $S_{3,2}$, b) test 3, $S_{3,4}$.

5. Conclusion

A test rig that utilises various ageing mechanisms; including cutting and twisting wires as well as pressing twisted broken wires have been presented. The created test rig enabled us to measure the resistances of wires under tests within a dead and live circuit. Results show that the live test provides us with a better capturing facility to track small changes in the resistance as the wire is gradually degraded. In fact, a live circuit amplifies resistance of the wire so that minimal capturing noise won't affect the result. Such a technique satisfies reasoning needs to get distinct meaning while interpreting degradation profile. It is a technique to improve even 4-wire resistance measurement facility of conventional DMMs. Authors of this paper aim to continue their experiments and research toward investigating fault progression mechanism in low power wires and interconnections in their future research while utilising the created test rig and capturing techniques.

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