Design and analysis of compact MMIC switches utilising GaAs pHEMTs in 3D multilayer technology

DOI:
10.1088/1361-6641/aa681b

Document Version
Accepted author manuscript

Published in:
Semiconductor Science and Technology

Design and Analysis of Compact MMIC Switches Utilising GaAs pHEMTs in 3D Multilayer Technology

Norshakila Haris[1,2], Peter B K Kyabaggu[1], Mohammad A Alim[3] and Ali A Rezazadeh[1]

[1] School of Electrical and Electronic Engineering, The University of Manchester, Sackville Street Building, M13 9PL Manchester, UK
[2] Marine Electrical & Electronic Engineering Technology Section, Universiti Kuala Lumpur – Malaysian Institute of Marine Engineering Technology, Lumut, Perak, Malaysia.
[3] Department of Applied Physics, Electronics and Communication Engineering, University of Chittagong, Bangladesh

E-mail: norshakila.haris@manchester.ac.uk

Abstract
In this paper, we demonstrate for the first time the implementation of 3-Dimensional (3D) multilayer technology on GaAs-based pseudomorphic high electron mobility transistor (pHEMT) switches. Two types of pHEMT switches are considered, namely single-pole single-throw (SPST) and single-pole double-throw (SPDT). The design and analysis of the devices are demonstrated first through a simulation of the industry-recognised standard model, TriQuint's Own Model - Level 3 (TOM3), developed by TriQuint Semiconductor, Inc. From the simulation analysis, three optimised SPST and SPDT pHEMT switches which can address applications ranging from L to X bands, are fabricated and tested. The performance of the pHEMT switches using multilayer technology are comparable to those of the current state-of-the-art pHEMT switches, while simultaneously offering compact circuits with the advantages of integration with other MMIC components.

Keywords: GaAs, MMIC, pHEMT, SPDT, SPST, switch.

---

1. Introduction

Semiconductor chips for cutting-edge electronic devices such as smartphones and tablets are becoming increasingly sophisticated with the integration of components and circuits such as transmit-receive (T/R) circuitry, antennas, and global positioning systems (GPS). In spite of their superior performances, the costs involved in realising this technology are still excessively high. Over the years, there has been a continuous drive to reduce the manufacturing cost. 3-Dimensional (3D) multilayer technology has good prospects of being adopted for this purpose, as all the components and circuits are arranged in vertically staggered component layers, which offers significant chip size reduction [1]–[3]. Reducing the chip size is important as compact chips improve the economics of manufacturing by allowing more components to be placed on a single chip reducing the area used. The performance of the chips can be improved further by monolithic integration of the devices with high performance GaAs monolithic microwave integrated circuits (MMICs)-based active device technology [3], [4]. Figure 1 illustrates the implementation of multilayer MMICs on semi-insulating GaAs substrate using pseudomorphic High Electron Mobility Transistors (pHEMTs) which are pre-fabricated on top of the substrate. The integration of active and passive components can be realised by opening the silicon nitride (Si_3N_4) windows of the pre-fabricated pHEMTs which is labelled as committed pHEMT. This procedure allows sandwiched layers of metal

and dielectric layers to be deposited on the top of the committed pHEMT to create multilayer MMICs.

MMIC switches have been used for many years, particularly for regulating signals in wireless communication. For instance, modern smartphones have many functions such as GPS, Bluetooth, radio, and antennas which operate on several frequency bands. To enable this multiband within one small device, multiple switching circuits are used. Many conventional switches employ p-i-n diodes which have demonstrated high quality performance [5], [6]. The process of traditional p-i-n diodes, however, is incompatible with the existing MMICs process technology [7], [8]. It also yields high DC power dissipation in the control bias circuitry [9]. Therefore, pHEMT switches are an attractive alternative, since they offer significant design flexibility, which is well-matched with the MMIC process, and have faster switching speed. Several studies on pHEMT switches have been conducted recently in MMIC [10]–[12]; however none of them have utilised 3D multilayer technology in the design. This paper describes for the first time the implementation of single-pole single-throw (SPST) and single-pole double-throw (SPDT) switches using pHEMTs, which are developed using 3D multilayer technology. The switches are fabricated and their performances analysed by means of microwave characterisations based on s-parameters.

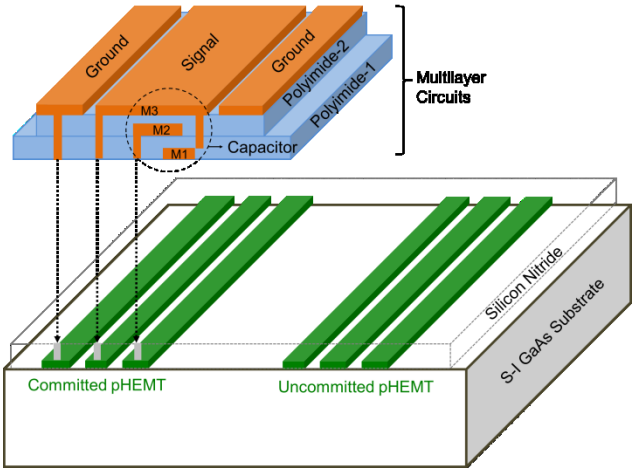

Figure 1. Conceptual illustration of 3D multilayer GaAs MMICs with three metal and two dielectric layers combining the multilayer circuits and the pre-fabricated pHEMT (commited pHEMT).

2. Basics of pHEMT Switches

This section firstly describes the characteristics of multilayer pHEMT that demonstrates the usefulness of the device in designing switching circuit. Next, the principle operations of two types of pHEMT switches are discussed, in order to provide a basic explanation of the switching mechanism.

2.1 Characteristics of Multilayer AlGaAs/InGaAs pHEMT

Multilayer AlGaAs/InGaAs pHEMTs operate as voltage-controlled resistor where the resistance between the source and drain contacts in the channel is controlled by the gate bias. They therefore consume far less current than current controlled p-i-n switches. This property is useful in applications requiring low power consumption, such as mobile communications. In a typical switching mode, the device is in its low-impedance state when zero bias is applied to the gate. A high-impedance state is achieved by applying a negative voltage of greater than the pinch-off voltage to the gate.

Measurements of the DC and RF characteristics of uncommitted and committed pHEMTs under bias suggested insignificant differences between these two configurations. Figure 2 shows the maximum attainable transconductance, g_m for both uncommitted and committed pHEMTs of 58.5 mS and 54.1 mS, respectively. The current gain, h_{21} and the maximum stable gain / maximum available gain (MSG/MAG) of devices are derived from measured S-parameters as functions of frequency. The extrapolations of current gain, h_{21} and MSG/MAG with -20 dB per slope give a cut-off frequency, f_t and a maximum oscillation frequency, f_{max}, respectively. Figure 3 demonstrates the measured cut-off frequencies, f_t of 30.7 GHz and 27 GHz as well as the maximum frequencies, f_{max} of 94.8 GHz and 117 GHz for the uncommitted and committed pHEMTs, correspondingly. Furthermore, the measured insertion loss, S_{21} of the committed pHEMT is shown to be comparable to the uncommitted pHEMT as depicted in Figure 4 confirming the feasibility of integration of these devices in producing compact MMICs.

Additional layers of polyimide and metal on top of the active region have generated extra heat in the committed pHEMT [13]. This can be seen from the source resistance, R_s values of uncommitted and committed pHEMTs, which are 2.2 Ω and 3.4 Ω, respectively. Further studies on this thermal influence on committed pHEMT has been reported in the literature [14]. Since g_m varies with R_s, a slightly degraded characteristic can be observed in their g_m, as well as in the f_t and f_{max}. The uncommitted and committed pHEMTs in this work are double heterostructure types which are shown in their g_m characteristics as double peaks. Due to greater sensitivity of these channels at the 2DEG depth, these differences are more pronounced than the other depths of the channel especially as V_{gs} approaching zero volt. The multilayer processing also introduces additional parasitics such as resistances, inductances and capacitances. However, because these two devices have similar epilayers and gate width, the difference is insignificant.

2.2 Principle Operation of pHEMT Switches

Various switching configurations are available when designing a switching device, each with its own advantages and disadvantages. Figure 5 illustrates two fundamental switch configurations, namely series and shunt, which are

connected with quarter wavelength (λ/4) transmission lines at the input and output ports. The switches are controlled by two complementary gate signals, 0.2 V and -2 V, respectively. A series resistor, R, is normally added to the gate driver of the pHEMT to prevent RF signal leakage, and also to provide isolation between the RF signal path and DC control path. The series SPST switch is "ON" when the pHEMT is in the low-impedance state and "OFF" when the pHEMT is in the high-impedance state. In contrast, the shunt SPST is "ON" when the pHEMT is in the high-impedance state and "OFF" when the pHEMT is in the low-impedance state. In both cases, no biases are applied to the source and drain terminals, thus the pHEMT switches can be considered as passive devices.

The pHEMT switches are characterised by a number of parameters including insertion loss and isolation. Insertion loss is defined as the transmission loss through the physical structure of a closed ("ON") pHEMT switch. Isolation is a measure of how effectively a pHEMT switch can be turned "OFF". These parameters are closely related to the DC characteristics of pHEMTs and are the most important factors, because high frequency signals leak through parasitic capacitances [15].

To investigate the switching performance, all SPST and SPDT pHEMT switches in this study are simulated using Keysight Advanced Digital System (ADS) software based on the industry-recognised standard model, TriQuint's Own Model - Level 3 (TOM3), developed by TriQuint Semiconductor, Inc. The simulated insertion losses and isolations of series and shunt pHEMT switches are shown in Figure 6. The data suggests that series pHEMT switch has higher insertion loss than shunt pHEMT switch over the whole frequency range. This is due to the higher ohmic contact resistance of the pHEMT. Hence, the shunt pHEMT switch is considered more lenient to high "ON" state resistance and is suitable to be used in a low-loss switch design. On the other hand, the isolation of series pHEMT switch is better than the shunt one at low-frequency range. However, its isolation was found to decrease at higher frequencies due to higher drain-source capacitance of the pHEMTs. All the information obtained from these basic series and shunt pHEMT switches is necessary, and will be taken into account when designing the optimal configurations of SPST and SPDT pHEMT switches using multilayer technology.

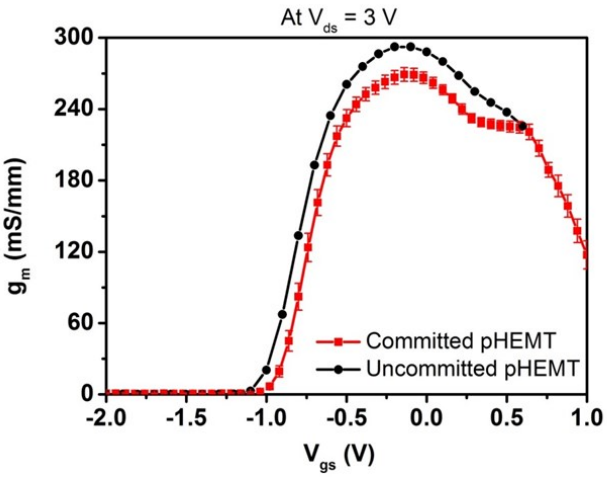

Figure 2. Measured transfer and transconductance characteristics of the uncommitted and committed pHEMTs.

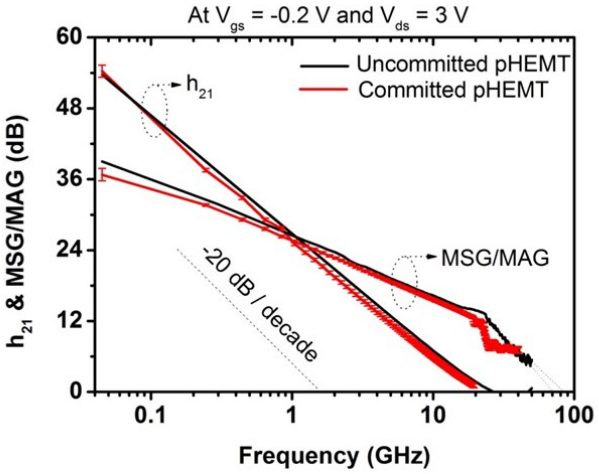

Figure 3. The current gain, h_{21} and the maximum stable/available gain (MSG/MAG) of uncommitted and committed pHEMTs as a function of frequency response.

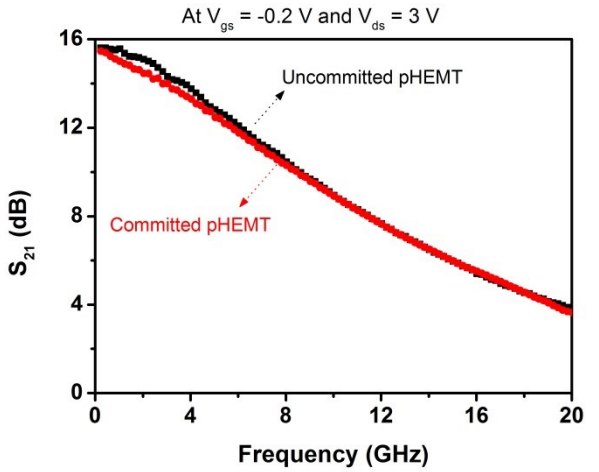

Figure 4. Comparison of measured insertion loss, S_{21} of uncommitted and committed pHEMTs.

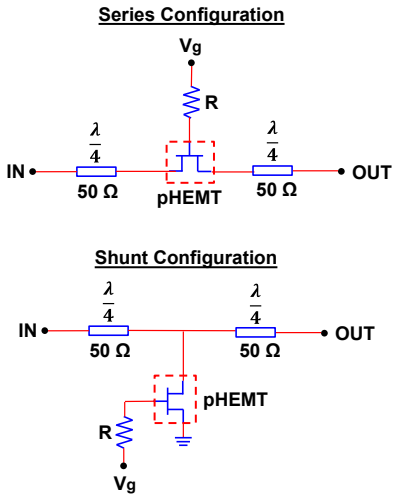

Figure 5. Series and shunt configurations of SPST pHEMT switches.

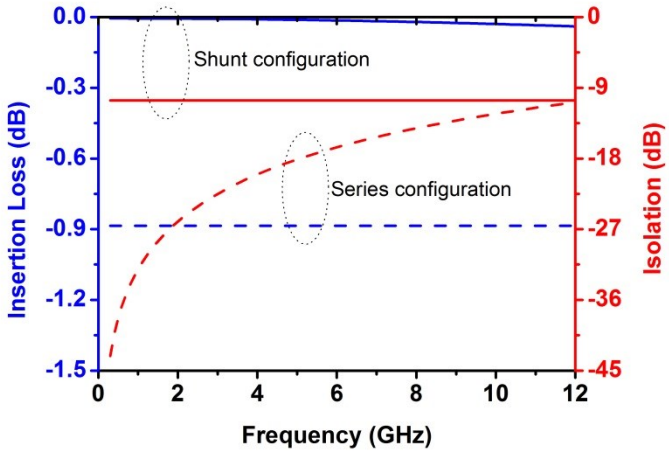

Figure 6. Simulated insertion loss and isolation of series and shunt SPST configurations.

3. Multilayer MMIC Fabrication Process

In this study, the investigated SPST and SPDT pHEMT switches are fabricated from Filtronic's 0.5 µm mushroom-shaped gate pHEMT using coplanar waveguide (CPW) MMIC technology. CPW structures are used on both sides of the input and output ports of the device, which employ ground-signal-ground (G-S-G) pad structures for RF probe measurement purposes. The gate width is 100 µm with two fingers and the spacing between gate-source and gate-drain are 0.5 µm and 2.5 µm, respectively. The process is based on an AlGaAs/InGaAs/GaAs epitaxial layer structure grown on 600 µm thick GaAs semi-insulating (S-I) substrates by molecular-beam-epitaxy (MBE) technique. The multilayer fabrication consists of seven processing levels of mask design. These include a deposition of three Titanium/Gold (Ti/Au) metal layers and two polyimide dielectric layers with thicknesses of 0.8 µm and 2.5 µm, respectively. A wafer with pre-fabricated pHEMTs is passivated with a standard silicon nitride (Si_3N_4) layer. The integration of the pre-fabricated pHEMTs with other passive components in a vertically stacked arrangement is made possible by opening the Si_3N_4 windows using a buffered oxide etch (HF) and lithography process. Si_3N_4 layer is very thin and the devices' geometry is very relaxed. Therefore, a simple wet etching using buffered HF is the simpler process to use rather than dry etching in this technology. It is found that for that particular thickness, the Si_3N_4 can be etched for 120 second [16]. The Ti/Au contacts are formed by evaporation and lift-off processes. Figure 7 shows the layout of fabricated pHEMT using a multilayer process and its micrograph. A conductor layer is applied on top of the pre-fabricated pHEMT to allow other passive MMIC components to be integrated with the device, as well as providing a path for probing. The total number of cells on a typical GaAs multilayer wafer is 12. All the multilayer pHEMT switches from these cells are measured. On the average, 67% of the cells have been successfully analysed and produced good results. The remaining cells have shown relatively poor performances due to the positions of these cells close to the edge of the sample.

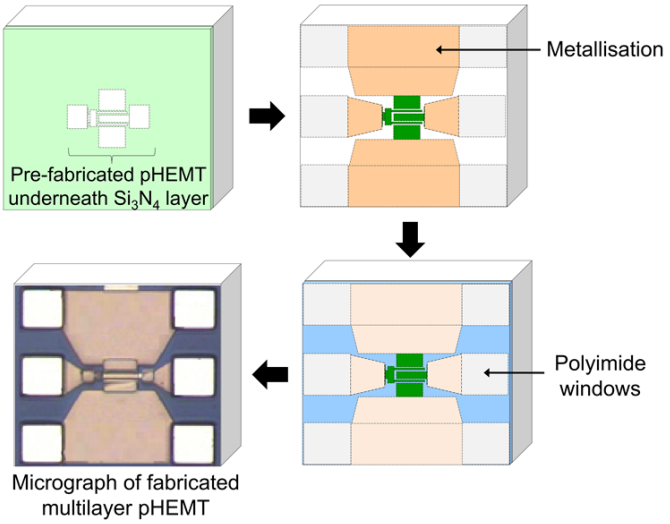

Figure 7. Layout and micrograph of fabricated pHEMT in 3D multilayer process

4. Design of SPST pHEMT Switches

Many factors may influence the design and application of pHEMT switches. A well-performing switch has low insertion loss with excellent isolation. In this study, three specific design considerations are taken into account to achieve such performance criteria and are discussed in the following.

4.1 Multistage Switch

One of the renowned practices to improve the performances of pHEMT switches is to cascade multiple series or shunt configurations, separated by λ/4 transmission line as shown in Figure 8 and Figure 9. Simulated results in Figure 10 and Figure 11 show that multistage series pHEMT switches improve isolation, but degrade insertion loss proportionately.

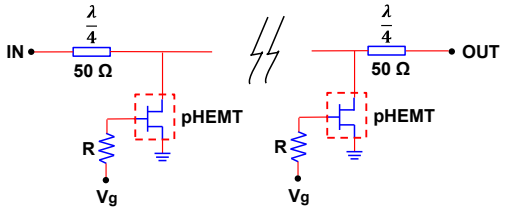

Figure 8. Cascaded configuration of shunt pHEMT switches.

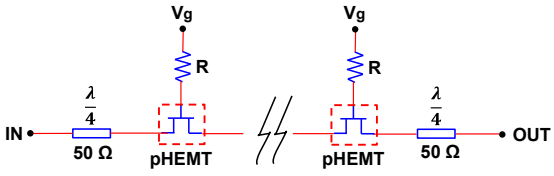

Figure 9. Cascaded configuration of series pHEMT switches.

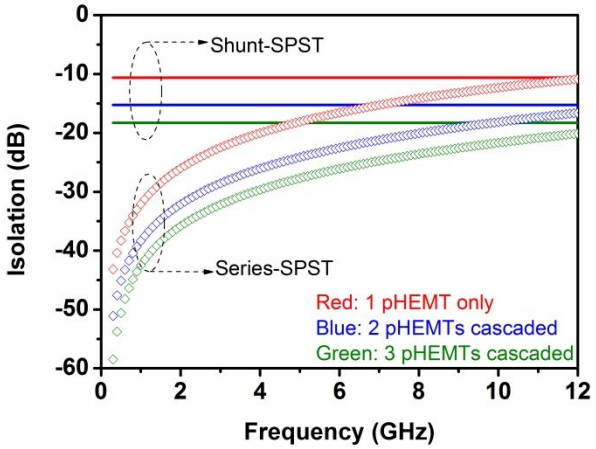

Figure 10. Simulated isolation of cascaded series and shunt SPST configurations.

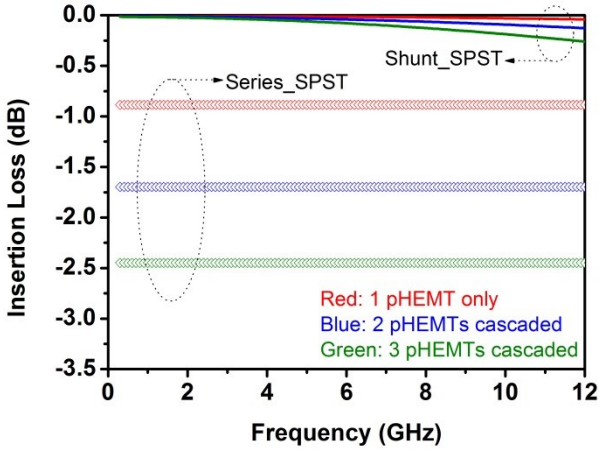

Figure 11. Simulated insertion loss of cascaded series and shunt SPST configurations.

4.2 Combination of Series-Shunt Configurations

At high frequencies, series pHEMT switch designs may not be able to meet the requirements for insertion loss and isolation; therefore many commercially available pHEMT switches make use of both series and shunt devices in combination. Figure 12 demonstrates the schematic diagrams of series-shunt combinations of pHEMT switches. As shown in Figure 13 and Figure 14, adding a shunt pHEMT switch considerably improves isolation at a high-frequency range, at the cost of a slightly higher insertion loss.

4.3 Varying Gate Width (Wg)

Gate width is one of the key parameters that needs to be chosen sensibly when designing a switching circuit using a pHEMT device. An optimisation of the gate width is required to compromise their isolation and insertion loss. When the pHEMT is in the "ON" state, the resistance will decrease as the gate width increases, which results in the insertion loss decreases. This is clearly demonstrated in Figure 15 where the gate width of 200 µm of series-shunt SPST switch produces the lowest insertion loss among them all. Increasing the gate width also increases the capacitance, resulting in the decrease in isolation in the "OFF" state. Figure 16 shows the isolation of series-shunt SPST demonstrating better performance as the gate width increases. In this study, a 200 µm gate width has been chosen for all the design and analysis of multilayer pHEMT switches.

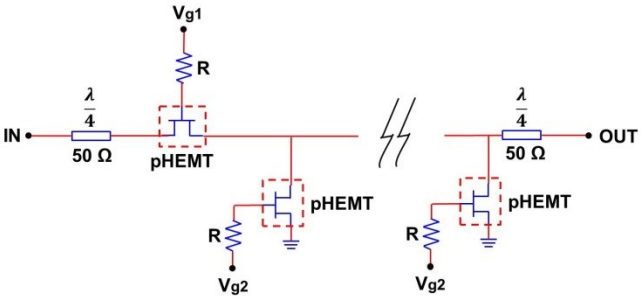

Figure 12. Schematic diagram of series-shunt combination SPST pHEMT switches.

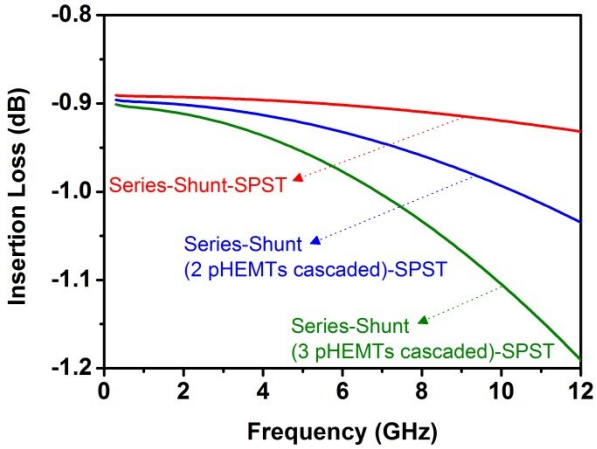

Figure 13. Simulated insertion loss of series-shunt combination SPST configurations.

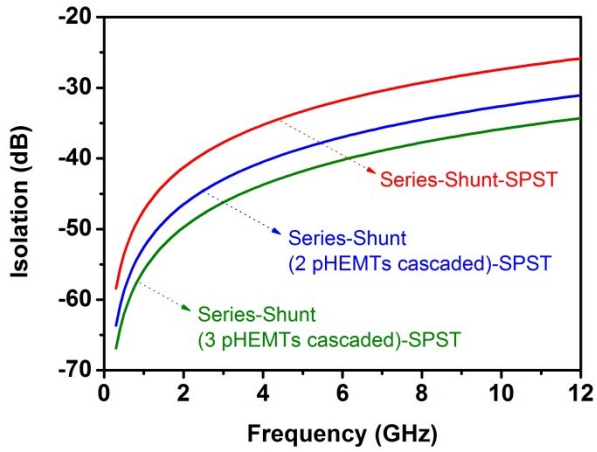

Figure 14. Simulated isolation of series-shunt combination SPST configurations.

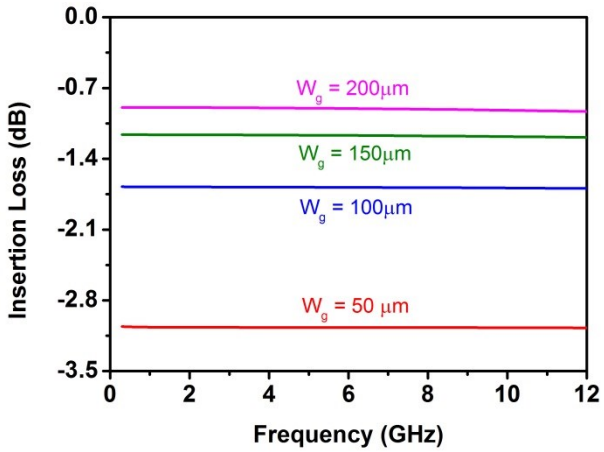

Figure 15. Simulated insertion loss of series-shunt SPST configuration with various gate widths.

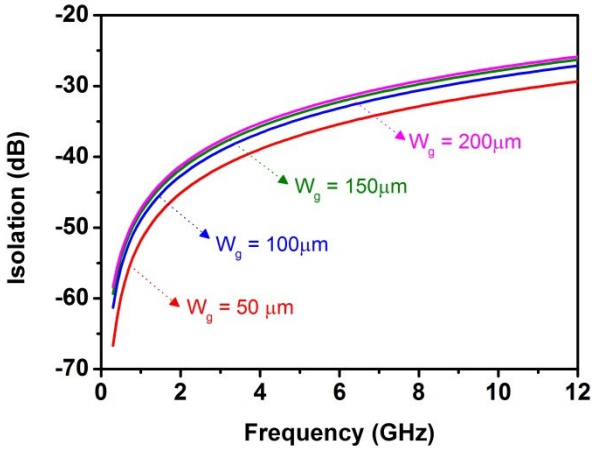

Figure 16. Simulated isolation of series-shunt SPST configuration with various gate widths.

5. SPDT pHEMT Switches Design

Switches may vary in the number of both poles and throws. The SPDT pHEMT switches under consideration have one input and two output arms. Ideally, when both arms are matched to 50 Ω, a 50% voltage split is expected between them. This switches power into either of the arms depending on the DC bias applied to the pHEMTs. SPDT switches in this study use SPST configuration as their basic building block. Figure 17 shows the schematic diagrams of the series and shunt SPDT pHEMT switches. Multiport S-parameters are used in ADS in conjunction with the TOM3 models of the active devices to simulate the pHEMT switches' performance. Series SPDT pHEMT switch shows better insertion loss and isolation than shunt SPDT pHEMT switch as shown in Figure 18 and Figure 19. Its insertion loss is higher than 1 dB and isolation of more than 16 dB is obtained on the entire frequency bands.

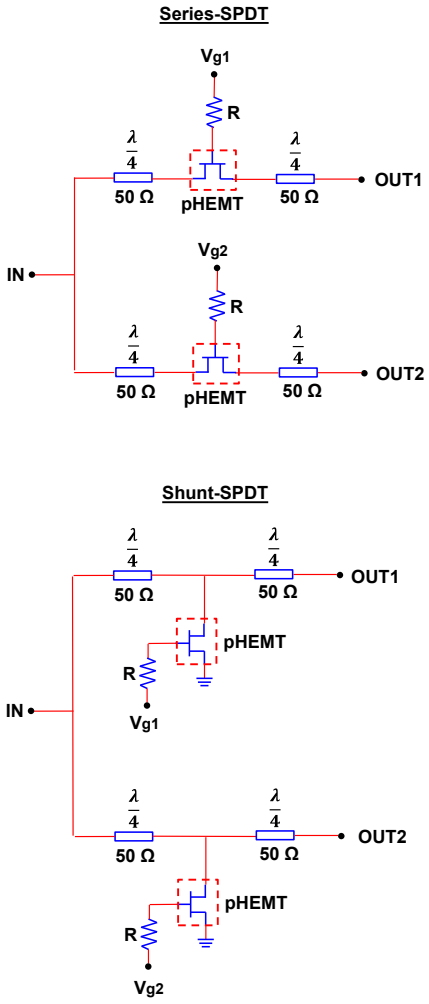

Figure 17. Schematic diagrams of series SPDT and shunt SPDT pHEMT switches.

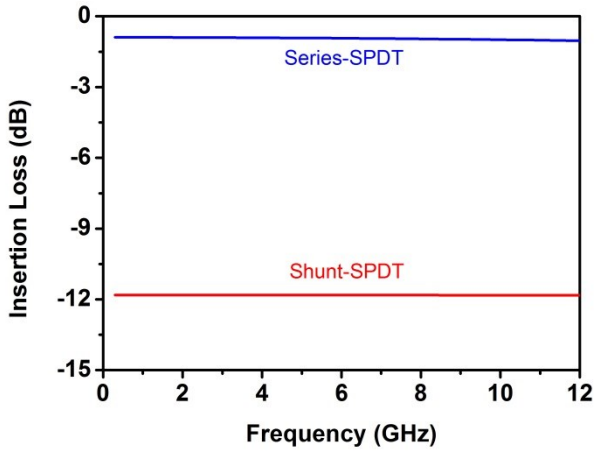

Figure 18. Simulated insertion loss of series SPDT and shunt SPDT pHEMT switches.

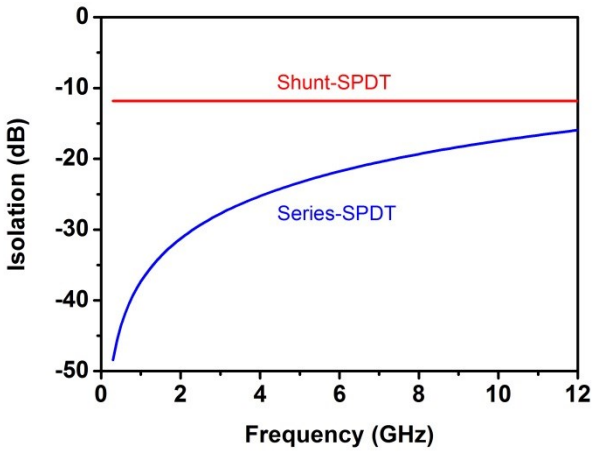

Figure 19. Simulated isolation of series SPDT and shunt SPDT pHEMT switches.

6. Measurement Results and Discussion

In this work, all the pHEMT switches are designed based on pHEMTs that are exclusively operated in a common-source configuration [10]–[12]. On-wafer S-parameter measurements are carried out based on four different frequency ranges from L, S, C, and X bands using HP8510C network analyser that is connected to Cascade Microtech 9000 analytical probe station at room temperature using coaxial cables. The network analyser uses 150 µm G-S-G probe pitch and is calibrated using a standard LRRM calibration substrate. A DC power supply is used to provide gate bias to the pHEMTs. Figure 20 illustrates the setup for measuring the pHEMT switches.

Micrographs of fabricated SPST and SPDT pHEMT switches are shown in Figure 21. Their measured and simulated results are compared in Figure 22 and Figure 23 where similar patterns of behaviour can be observed from the S-parameters' performance. The accuracy in design and simulation of SPST and SPDT pHEMT switches is ensured by comparing the simulated and measured data with the extracted data obtained from the small-signal model. Our investigations in several multilayer devices utilising pHEMT have shown that the differences between the simulated and measured results are due to the use of standard TOM3 model in ADS simulation tool, which does not consider the effect of multilayer processing as discussed in Section 2 [17]. Besides that, the measurements do not reflect the actual results since the effects of the internal VNA features and the test fixtures are not considered due to calibration reference plane used. Hence, the error percentage between the measured and the simulated S-parameters of the devices is shown to be high (around 40%-55%). The insertion loss is quite high due to inductive and capacitive losses introduced by the 50 Ω CPW transmission lines. The measured data are raw data without de-embedding; hence the losses can be reduced by subtracting the contribution of these unwanted portions of the structure.

Insertion loss error in simulated and measured results is increasing at higher frequencies as shown in Figure 22 due to high losses of the thin film conventional CPW transmission lines used in the design [18]. The insertion loss can be improved in an optimised process by increasing the conductor thickness of the transmission line and replacing the gold conductor to copper which has a higher conductivity [18].

The performance of the measured SPST and SPDT pHEMT switches are summarised and compared with commercially available and published pHEMT switches in Table I. The table suggests that better performances and smaller chip sizes can be obtained using multilayer technology. They are comparable with the current state-of-the-art pHEMT switches, and provide the advantage of possible integration with other MMIC components in vertical arrangement.

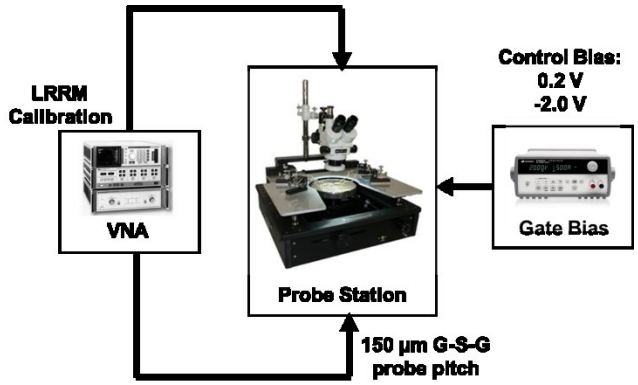

Figure 20. Measurement setup for pHEMT switches.

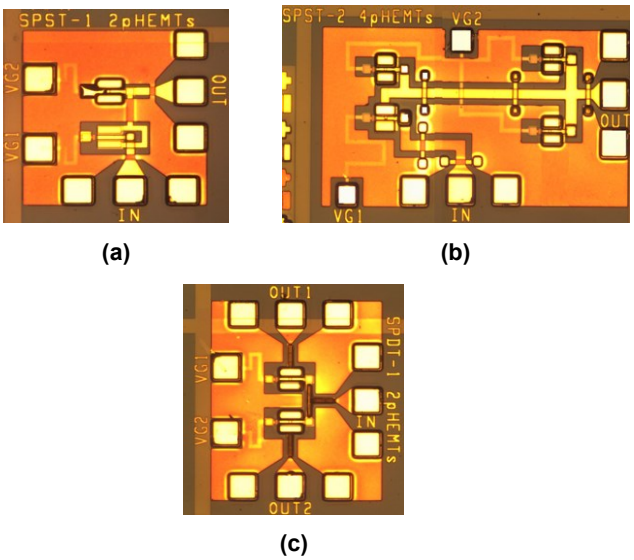

Figure 21. Micrographs of fabricated pHEMT switches (a) Series-Shunt SPST, (b) Series-Shunt (3pHEMTs) SPST, and (c) Series SPDT.

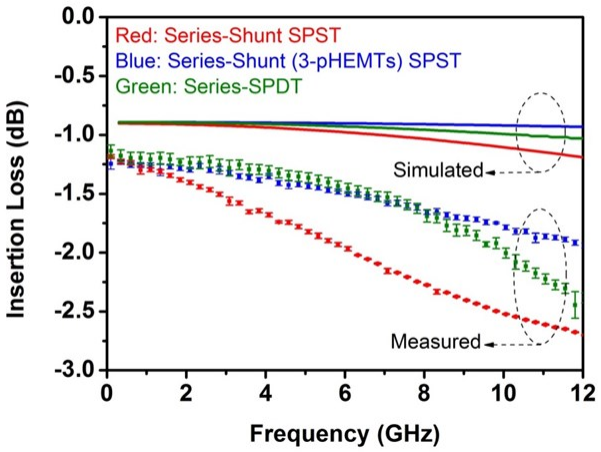

Figure 22. Comparison of measured and simulated insertion losses of fabricated SPST and SPDT pHEMT switches.

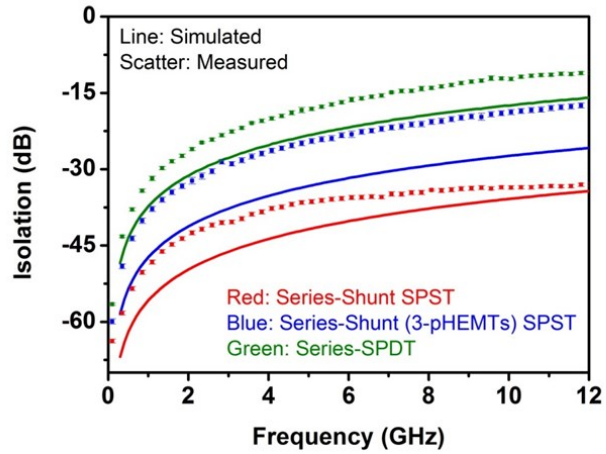

Figure 23. Comparison of measured and simulated isolations of fabricated SPST and SPDT pHEMT switches.

7. Conclusion

GaAs multilayer technology has been successfully used for the first time to realise compact SPST and SPDT pHEMT switches, on pre-fabricated GaAs pHEMT wafers. In spite of early stage of multilayer processing technology, TOM3 model showed good agreement with the measured data providing a valuable tool in the design of MMICs. The developed pHEMT switches demonstrated 1.39 dB maximum insertion loss and 26.5 dB minimum isolation at 2.4 GHz. Although the insertion loss can be improved through proper de-embedding of the data, the results are encouraging and significant, not only because of their novelty but also because they offer potential integration with other MMIC components in a compact single chip. The investigation of uncommitted and committed pHEMTs suggested that multilayer fabrication processing does not introduce any significant effects on the performance of the pHEMTs. Hence, to achieve a miniature overall chip size, it is possible to integrate active and passive components by implementing this technology.

References

[1] Q. H. Wang, T. Gokdemir, D. Budimir, U. Karacaoglu, A. A. Rezazadeh, and I. D. Robertson, "Fabrication and Microwave Characterisation of Multilayer Circuits for MMIC Applications," *IEEE Proceedings - Microwaves, Antennas and Propagation*, vol. 143, no. 3, p. 225, 1996.

[2] M. Geen, G. Green, R. Arnold, and R. Jansen, "Miniature multilayer spiral inductors for GaAs MMICs," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1989. Technical Digest 1989., 11th Annual*, 1989, pp. 303–306.

[3] Q. Sun, V. T. Vo, R. A. Davies, J. Tan, and A. A. Rezazadeh, "Miniaturized Multilayer CPW pHEMT Amplifiers," in *European Microwave Integrated Circuit Conference*, 2008, pp. 44–47.

[4] L. Krishnamurthy, Q. Sun, V. Vo, G. Parkinson, D. Paul, K. Williams, and A. Rezazadeh, "A comparative study of active and passive GaAs microwave couplers," in *European Gallium Arsenide and Other Semiconductor Application Symposium, GAAS*, 2005, pp. 353–356.

[5] E. Alekseev, D. Pavlidis, V. Ziegler, M. Berg, and J. Dickmann, "77 GHz high-isolation coplanar transmit-receive switch using InGaAs/InP PIN diodes," in *GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 20th Annual. Technical Digest 1998 (Cat. No.98CH36260)*, 1998, pp. 177–180.

[6] J.-L. Jar-Lon Lee, D. Zych, E. Reese, and D. M. Drury, "Monolithic 2-18 GHz low loss, on-chip biased PIN diode switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 2, pp. 250–256, 1995.

[7] H. Takasu, F. Sasaki, H. Kawasaki, H. Tokuda, and S. Kamihashi, "W-band SPST Transistor Switches," *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 9, pp. 315–316, 1996.

[8] D. C. W. Lo, Huei Wang, B. R. Allen, G. S. Dow, Kwo Wei Chang, M. Biedenbender, R. Lai, Sian Chen, and D. Yang, "Novel monolithic multifunctional balanced switching low-noise amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 12, pp. 2629–2634, 1994.

[9] J. V. Bellantoni, D. C. Bartle, D. Payne, G. McDermott, S. Bandla, R. Tayrani, and L. Raffaelli, "A monolithic high power Ka-band PIN switch," in *Digest of Papers.,Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp. 47–50.

[10] A. Freeston, C. Varmazis, and T. Boles, "Nanosecond pHEMT switches," in *Microwave Integrated Circuits Conference, 2009. EuMIC 2009. European*, 2009, pp. 13–16.

[11] J. Mun, H. Ji, H. Ahn, H. Kim, and C.-O. Park, "Design and Fabrication of pHEMT MMIC Switches for IEEE 802.11.a/b/g WLAN Applications," *Semiconductor Science and Technology*, vol. 20, no. 8, pp. 677–684, Aug. 2005.

[12] Q. Xiao, T. Samiotes, GGalluccio, and B. Rizzi, "A High Performance DC-20 GHz SPDT Switch in a Low Cost Plastic QFN Package," in *European Microwave Integrated Circuits Conference (EuMIC)*, 2009, pp. 320–323.

[13] Jimmy P.H. Tan, "Thermal and Small-Signal Characterisation of AlGaAs/InGaAs pHEMTs in 3D Multilayer CPW MMIC," The University of Manchester, UK, 2011.

[14] M. A. Alim and A. A. Rezazadeh, "Thermal Influence on Multibias Small- and Large-Signal Parameters of GaAs pHEMT Fabricated in Multilayer 3-D MMIC," *IEEE Transactions on Electron Devices*, pp. 1–8, 2017.

[15] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, USA: McGraw-Hill, Inc., 2001.

[16] A. Witvrouw, B. Du Bois, P. De Moor, A. Verbist, C. A. Van Hoof, H. Bender, and C. Baert, "Comparison between wet HF etching and vapor HF etching for sacrificial oxide removal," 2000, pp. 130–141.

[17] E. P. Sinulingga, A. A. Rezazadeh, and P. B. Kyabaggu, "3D momentum modeling technique and measurements of CPW compact GaAs multilayer MMICs," in *2015 Asia-Pacific Microwave Conference (APMC)*, 2015, pp. 1–3.

[18] V. T. Vo, L. Krishnamurthy, Q. Sun, and A. A. Rezazadeh, "3-D Low-loss Coplanar Waveguide Transmission Lines in Multilayer MMICs," *IEEE Transaction on Microwave Theory and Techniques*, vol. 54, no. 6, pp. 2864–2871, 2006.

[19] "Datasheet: RFSW2040 - DC to 20 GHz SPST pHEMT GaAs Switch," *RF Micro Devices, Inc. (RFMD)*. [Online]. Available: https://www.rfmw.com/ProductDetail/RFSW2040/416360. [Accessed: 17-Feb-2017].

TABLE I
COMPARATIVE TABLE WITH COMMERCIAL AND PUBLISHED SPST AND SPDT PHEMT SWITCHES

Type	Reference	No. of pHEMT	Chip Size (mm^2)	Insertion Loss (dB) @				Isolation (dB) @			
				1-2 GHz	2-4 GHz	4-8 GHz	8-12 GHz	1-2 GHz	2-4 GHz	4-8 GHz	8-12 GHz
SPST	[11]	4	0.9 x 0.5	0.2	0.4	0.5	0.8	28	31	39	43
SPDT	[11]	4	0.7 x 0.7	0.5	0.8	1.0	1.8	41	35	29	23
SPST	[19]	2	1.5 x 1.5	1.8				40			
SPDT	[12]	6	1.4 x 1.7	1.7				40			
SPST	This Work	2	0.7 x 0.7	1.39	1.67	2.26	2.60	43.16	38.14	34.60	32.98
SPST	This Work	4	0.7 x 1.3	1.27	1.37	1.62	1.90	32.86	27.05	21.13	17.66
SPDT	This Work	2	0.9 x 0.7	1.22	1.31	1.66	2.40	26.52	19.91	14.00	11.05