Reducing neutral point voltage fluctuation in NPC three-level active power filters

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Abstract: Shunt active power filters (SAPFs) have been widely used to improve power quality of the grid by mitigating harmonics injected from nonlinear loads. This paper presents a new method for improving the performance of SAPFs using neutral point clamped (NPC) three-level inverters. NPC three-level inverters often suffer excessive voltage fluctuations at the neutral-point of DC-link capacitors, which may damage switching devices and cause additional high harmonic distortion of the output voltage. In order to solve the problem, two compensating schemes are proposed to restrict voltage fluctuation in the inverters. The first is voltage dependent, adopting a voltage compensation method, while the second is current dependent, using a current compensation method. The paper describes the respective circuit architectures and principles of operation. Corresponding models are mathematically formulated and evaluated under typical balanced and unbalanced working load conditions. The results show that both schemes are able to alleviate considerably voltage oscillations and hence harmonic distortions, and the current compensated NPC inverter outperforms the voltage compensated NPC inverter**.** Consequently, it is shown that the proposed approaches are effective and feasible for improving power quality of the grid when connected to nonlinear loads.

Keywords: shunt active power filter (SAPF), three-level inverter, neutral point clamped (NPC), DC-link, voltage compensation, current compensation

Symbols and abbreviations

SAPF	Shunt active power filters
NPC	Neutral point clamped
DG	Distributed generation
PV	Photovoltaics
THD	Total harmonic distortion
SVPWM	Space voltage vector pulse-width modulation
VNPCI	Voltage dependent NPC three-level inverter
CNPCI	Current controlled NPC three-level inverter
IGBT	Insulated gate bipolar transistor
u_{sa}, u_{sb}, u_{sc}	Three-phase alternating-current supply
i_{sa}, i_{sb}, i_{sc}	Grid currents
i_{La}, i_{Lb}, i_{Lc}	Load currents
i_{ca}, i_{cb}, i_{cc}	Compensation currents provided by the SAPF
u_o	Neutral point voltage of the three-phase bridge arm
u_N	Neutral point voltage of the DC-link capacitors
u_c	Voltage of the primary side of the transformer
u_b	Compensating voltage
u_s	DC-link voltage applied across the capacitors
S_1, S_2, S_3, S_4	IGBT power switches
T	Coupling transformer
L, C_f	LC filter
u_{dc}	DC voltage applied to the single-phase full-bridge inverter
u_i	Voltage output of the single-phase inverter
i_1	Current through the filter inductor
i_2	Transformer primary side current
i_{cf}	Current through the filter capacitor
D_1	Diode used to prevent reverse current flow
L_2, C_3	LC filter
u_{dc1}	Voltage input of the boost DC/DC converter
u_{dc2}	Voltage output of the boost DC/DC convertor

56	$i_{c3(off)}$	Current in capacitor C_3 when switching device S_5 is turned off
57	i_3	Current in the inductor L_1
58	i_4	Compensating current
59	$u_{L1(off)}$	Voltage across the inductor L_1 when switching device S_5 is turned off
60	$u_{L1(on)}$	Voltage across inductor L_1 when switch S_5 is turned on
61	D	Duty cycle of the switching device S_5
62	K_p, K_i	Parameters of the PI controller

63

1. Introduction

Recently, distributed generation (DG) installation has been significantly increased, due to the deregulation of utilities, environmental constraints, and concerns regarding climate change [1]. This type of power generation system, as shown in Fig. 1, can provide electric power at or on a site closer to end users. However, harmonic-related problems have become a key concern because DG generators, such as wind and photovoltaics (PV), are coupled to power electronic converters and nonlinear loads [2]. In this regard, shunt active power filters (SAPFs) are widely used to mitigate these harmonic distortion problems in the grid. Compared to traditional two-level voltage-source inverters used in SAPFs, three-level voltage-source inverters are able to bear higher voltage classes and operate with lower harmonic distortion and at lower switching frequencies. Three-level inverters therefore offer better performance, in particular for medium-voltage applications [3]. In terms of topological structure, three-level inverters can be classified as one of three distinct types, namely diode clamped multilevel inverters, clamping capacitor multilevel inverters, and isolated H-bridge multilevel inverters [4-5]. The neutral point clamped (NPC) three-level inverter [6] is classified as type of diode clamped multilevel inverters. The most commonly used NPC three-level inverter circuit [7-9] is shown in Fig. 2, where it is incorporated into a SAPF. A full description of the circuit will be given in subsequent sections.
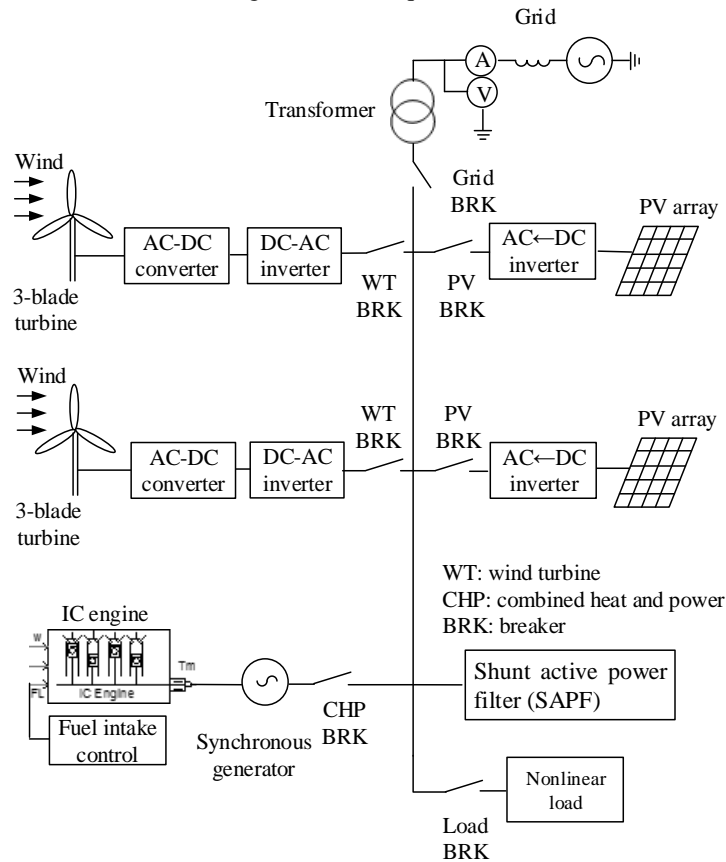
Figure 1. Schematic diagram of a distributed generation system

In a NPC three-level inverter, the neutral point of the DC-link capacitors and the neutral point of the three-phase bridge circuit are linked together directly. The neutral-point voltage of the three-phase bridge arm will vary because of the oscillation of the neutral-point voltage in the DC-link. The problem is inherent because

85 there is a neutral-point current flowing into or out of the neutral points in the circuit [10-11]. The varying current
86 causes a charge-discharge phenomenon associated with the capacitors through the neutral-points in the circuit,
87 thus resulting in a fluctuation in the neutral-point voltage. Consequently, the voltage ripples produced will affect
88 the capability of the NPC three-level inverter to work efficiently [12]. Furthermore, excessive fluctuations of
89 the DC-link voltage increase voltage stresses on the switching devices and hence the total harmonic distortion
90 (THD) of the output current, which may limit potential engineering applications of this type of inverter.
91   There are three main factors that may cause oscillations in the neutral-point voltage in the DC-link branch.
92 Firstly, the capacitance associated with the DC-link capacitors may become unbalanced after use for extended
93 periods of time. DC link capacitors are required to endure high ripple currents leading to self-heating, which,
94 in addition to high ambient operating temperatures, can result in the deterioration of the electrolyte material and
95 the loss of electrolyte by vapour diffusion. Secondly, a critical factor for the inverter to work is delivery of the
96 gate drive signals to the switching devices, as controlled by the switching frequency. Any switching delay will
97 cause load current imbalance. Thirdly, nonlinear loads also cause harmonics to appear in the load current, which
98 may in turn inject harmonics back to the inverter. Mathematical descriptions regarding the causes of voltage
99 oscillations can be found in [13].
100   In order to solve these problems, three main methods have been investigated to alleviate voltage
101 oscillations. The first is through the use of two independent DC sources to ensure a stable and constant DC
102 voltage across the inverter. The method is expensive [14], because two independent DC sources require two
103 isolation transformers. The second involves the design of improved control strategies, which are arguably the
104 most widely used techniques at present [15-17]. Among the control strategies, the best known is the space
105 voltage vector pulse-width modulation (SVPWM) method [18-22]. The control strategy proposed in [18]
106 replaces the P-type or N-type small switching states with other switching states that do not affect the neutral-
107 point voltage. Reference [23] demonstrates the ability of the SVPWM method to balance the neutral point
108 voltage for different regions of the space vector plane, while a new general model was introduced in [24] to
109 investigate the theoretical and practical limitations of the balancing problems caused by space vector
110 modulation. A control scheme based on a virtual space vector PWM method is proposed in [25] to control the
111 neutral-point voltage fluctuation over the full range of the modulation index and load power factor, subject to
112 the condition that the sum of the three-phase output currents equals zero. The third method reduces voltage
113 oscillations through a change in circuit topology, as the solution by hardware circuit has its own advantages.
114 This method incorporates auxiliary components in the traditional NPC three-level inverter circuit and has
115 proved to be able to achieve good performance to suppress excessive neutral-point voltage fluctuation
116 effectively at low cost [26].
117   In this paper, two new NPC three-level inverter topologies are proposed. The first is a voltage dependent
118 NPC three-level inverter (VNPCI), which adopts a voltage compensation method to restrain the neutral point
119 voltage fluctuation of the DC-link. The second method is a current controlled NPC three-level inverter (CNPCI)
120 and uses a current compensation method. Both two new inverter topologies are incorporated in a SAPF. The
121 remainder of this paper is organised as follows. The principle of the SAPF is described in Section 2. The circuit
122 architectures, their principles of operation and mathematical models describing voltage and current dependent
123 inverters are outlined in Section 3 and Section 4, respectively. Simulation results of the inverter models and the
124 performance of the SAPF under typical balanced and unbalanced working load conditions are shown and
125 discussed in Section 5. Conclusions and suggestions for future work are given in Section 6.
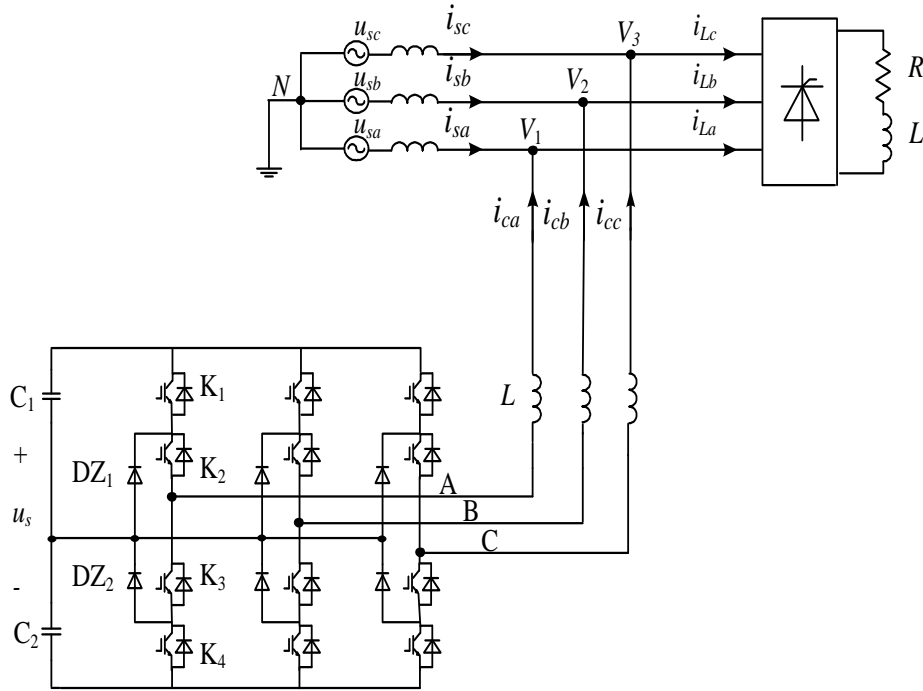126

127 **2. Shunt active power filter (SAPF)**

**Figure 2.** A SAPF based on the neutral point clamped (NPC) three-level inverter

Figure 2 shows a SAPF based on the NPC three-level inverter. In this figure, u_{sa}, u_{sb}, u_{sc} are the three-phase alternating-current supplies; the load is nonlinear, generating harmonic currents; i_{sa}, i_{sb}, i_{sc} and i_{La}, i_{Lb}, i_{Lc} are grid currents and load currents, respectively; i_{ca}, i_{cb}, i_{cc} are compensation currents provided by the SAPF, which are used to eliminate harmonic currents in the grid. The SAPF is essentially composed of two major components, namely a conventional NPC three-level inverter and an associated control scheme. In the inverter circuit, K_1, K_2, K_3, K_4 are IGBT (insulated gate bipolar transistor) power switches, while DZ_1, DZ_2 are clamp diodes; note that only the components of one inverter arm are labeled for simplicity. The DC bus voltage is split in half using two DC capacitors, C_1 and C_2, and into three voltage levels, u_s, 0, and $-u_s$, via clamping diodes. The control scheme detects the load currents in real time, which are used to calculate command signals for the IGBT switches. The inverter then works as a signal amplification circuit, producing appropriate compensation currents. This compensation current is equal but opposite to the harmonic currents, which can be overlaid to the load currents, thus eliminating the harmonic currents generated by the nonlinear load.

3. Voltage compensated NPC inverter (VNPCI)

3.1. Inverter circuit

The schematic diagram of the VNPCI circuit is shown in Fig. 3. Essentially, the circuit consists of two parts. Power unit 1 is associated with the conventional NPC three-level inverter, as described in the preceding section. In order to reduce excessive neutral-point voltage fluctuations across the DC-link capacitors, this paper considers the application of an active voltage compensation method in which the controllable voltage source is used in series between the neutral point of the DC-link and the neutral point of the three-phase bridge circuit. This voltage source is used in order to compensate for voltage fluctuations across the three-phase bridge arm of the inverter. The voltage at the neutral-point of the three-phase bridge arm is detected in real time and compared with a reference voltage, producing an appropriate value for the compensation voltage. Subsequently, the voltage source generates an equal but opposite voltage, thus reducing the voltage fluctuation across the inverter.
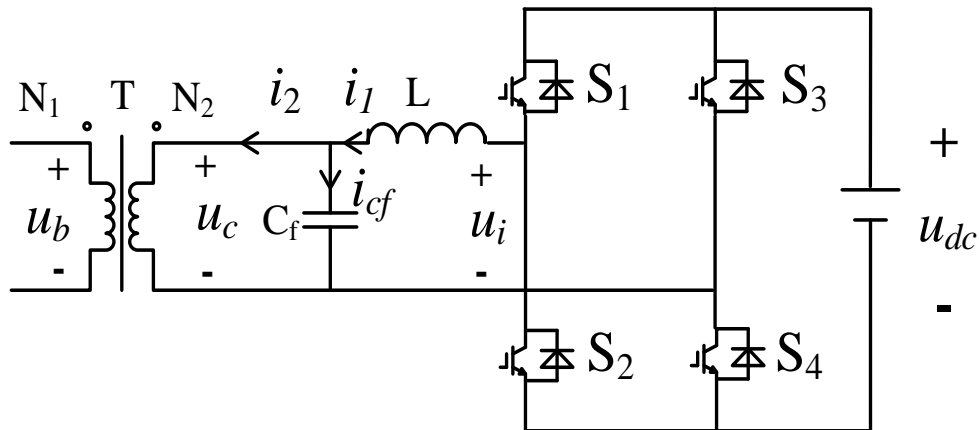
Power unit 2 is an active voltage compensation device, which in essence is a single-phase full-bridge inverter. The device works as a controllable voltage source and is connected in series between the neutral point of the three-phase bridge arm and the neutral point of the DC-link through a coupling transformer. The variables u_o and u_N denote the neutral point voltage across the three-phase bridge arm and the DC-link capacitors, respectively; u_c and u_b are the voltages across the primary and secondary sides of the transformer, respectively, for which u_b is used as the compensating voltage; u_s is the DC-link voltage applied across the capacitors.

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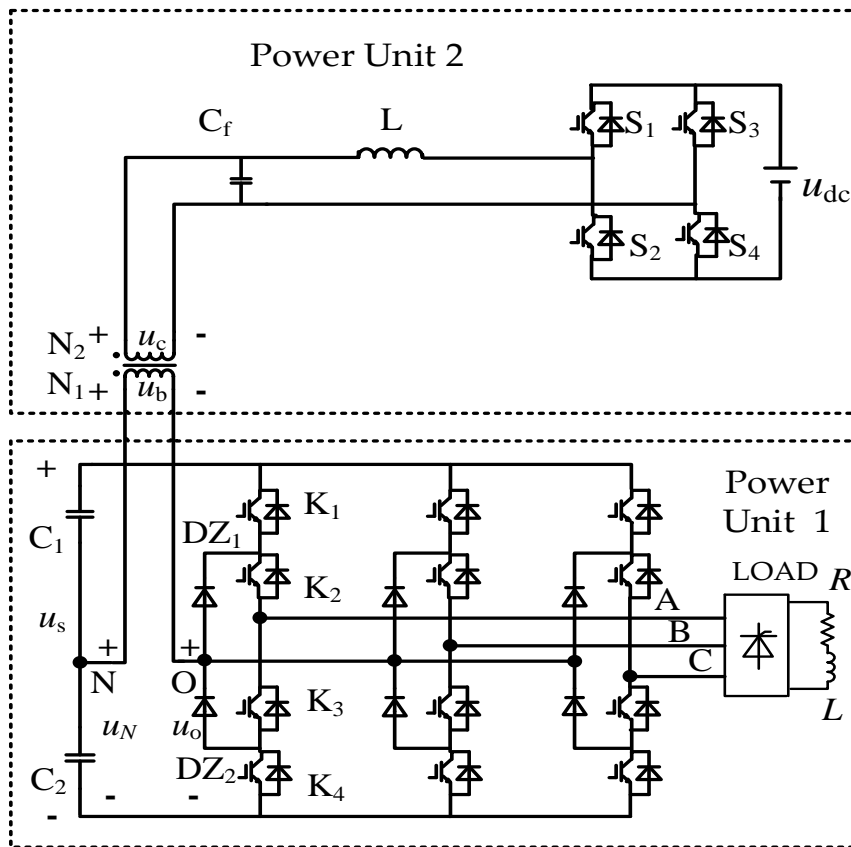
Figure 3. Schematic diagram of the voltage compensated NPC inverter

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164   *3.2. The active voltage compensation device*

165

166   **Figure 4.** Schematic diagram of the active voltage compensation device

167   The voltage compensation device is shown in Fig. 4. It is composed of a single-phase, full-bridge inverter
168   circuit, where S_1, S_2, S_3, S_4 are IGBT power switches; T is the coupling transformer with a transformation ratio
169   of n; the inductor L and the capacitor C_f form a LC filter that removes unwanted switching harmonics from the
170   inverter output.
171   Now consider the mathematical model of the voltage compensation device. In the circuit illustrated in Fig.
172   4, u_{dc} is a DC voltage applied to the single-phase full-bridge inverter; u_i is the voltage output of the single-phase
173   inverter; i_1 is the current through the filter inductor; i_2 is the transformer primary side current; i_{cf} is the current
174   passing through the filter capacitor.
175   For an ideal transformer (i.e., no losses and no leakage flux between the primary and secondary windings),

$$u_b = \mathrm{n}\left(u_i - \mathrm{L}\frac{di_1}{dt}\right)$$

(1)

Hence, for the NPC inverter shown in Fig. 3, the voltage due to the introduction of the compensating voltage u_b can be obtained via the following equations. In the ideal situation, three-phase bridge arm voltage u_o should be equal to the half DC-link voltage, i.e., $0.5\ u_s$.

$$u_N - u_b = u_o$$

(2)

$$u_N - \mathrm{n}(u_i - \mathrm{L}\frac{di_1}{dt}) = 0.5u_s$$

(3)

For the voltage output of the single-phase inverter u_i

$$u_i = S^* u_{dc}$$

(4)

where S^* represents the switching function; if S_1 and S_4 are switched on while S_2 and S_3 are switched off, then $S^*=1$; if S_1 and S_4 are switched off while S_2 and S_3 are switched on, then $S^*=-1$.

Substituting (4) into (3) gives

$$u_N - \mathrm{n}(S^* u_{dc} - \mathrm{L}\frac{di_1}{dt}) = 0.5u_s$$

(5)

Therefore, the state equations of this active voltage compensation device can be described as,

$$\frac{du_c}{dt} = \frac{1}{\mathrm{C_f}}(i_1 - i_2)$$

(6)

$$\frac{di_1}{dt} = \frac{1}{\mathrm{L}}(u_i - u_c)$$

(7)

The resulting control scheme of the active voltage compensation device is shown in Fig. 5. It illustrates the operating principle of active voltage compensation device as controlled by this scheme. In this diagram, the voltage $0.5u_s^*(s)$ refers to half of the DC-link voltage under balanced capacitors; $u_n(s)$ is the DC-link neutral-point voltage measured in real time; $u_c^*(s)$ is the reference compensating voltage; $u_i(s)$ is the output voltage of the single phase full bridge inverter circuit; $u_c(s)$ is the transformer primary side voltage; $i_1(s)$ is the current in the filter inductor; and $i_2(s)$ is the transformer primary side current. The compensating voltage $u_c^*(s)$ is obtained by calculating the difference between the measured neutral-point voltage of DC-link and half of the ideal DC-link voltage. The error voltage between $u_c^*(s)$ and $u_c(s)$ is then used for generating PWM signals based on the triangular wave modulation method, which are then used to control the voltage output of the single-phase inverter at a desired level. A PI controller, represented by K_p+K_i/s, is used because it can provide a compensating voltage output more accurately, thus improving performance further.
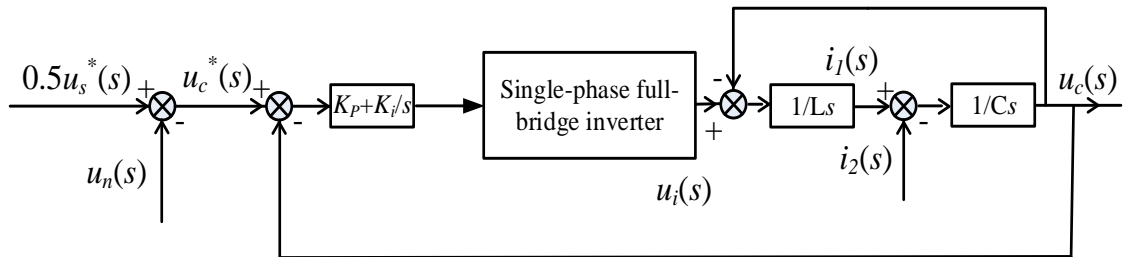
Figure 5. The control scheme for the active voltage compensation device

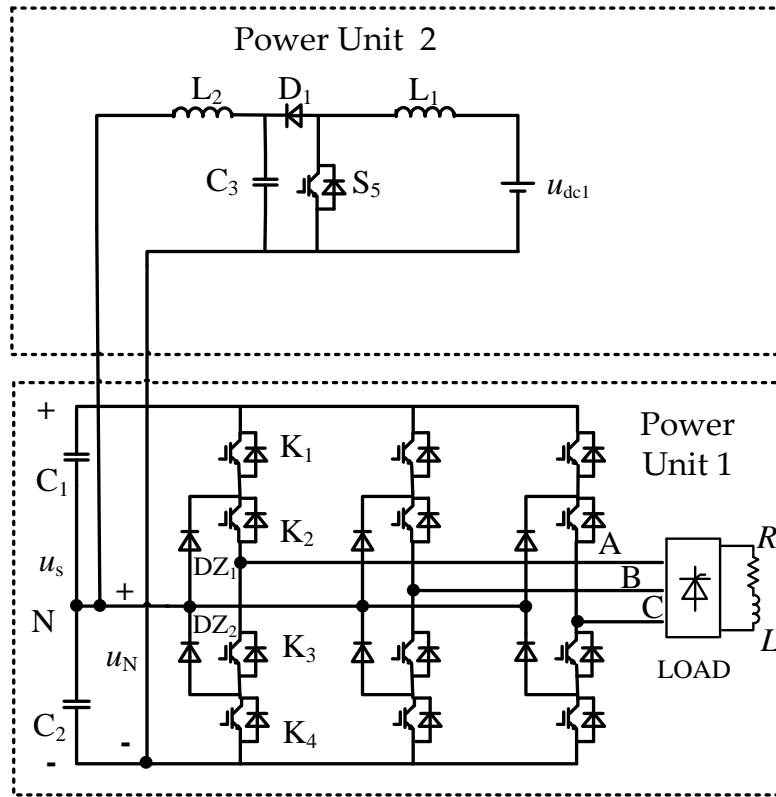## 4. Current compensated NPC inverter (CNPCI)

4.1. Inverter circuit

As described above, the primary reason causing neutral-point voltage fluctuation across the DC-link is the current that flows in to or out of the neutral points in the circuit. The varying current will lead to charge-discharge phenomena associated with the capacitors through the neutral-points in the circuit, resulting in a fluctuation in the neutral-point voltage. The voltage fluctuation can be alleviated naturally through the use of an active current compensation scheme in which a controllable current source is connected in shunt with one of the DC capacitors. This controllable current source is used to compensate for the current flow between the

212 neutral point of DC-link capacitors and the neutral point of three-phase bridge circuit. It can further suppress
213 neutral-point voltage fluctuations because, if this scheme is applied effectively, there is approximately zero
214 current flowing between the neutral points in the inverter.
215
216

218 **Figure 6.** Schematic diagram of the current compensation NPC inverter

219
220   The schematic diagram of CNPCI is shown in Fig. 6. It also consists of two parts: part 1 is the conventional
221 NPC three-level inverter and part 2 is the proposed active current compensation device. The compensation
222 device is essentially a boost DC/DC conversion circuit, which works as a current source. The current flowing
223 between the neutral points of the inverter is detected in real time, and an equal but opposite current is then
224 generated through the current compensation device, offsetting the current flow between the neutral points in the
225 inverter. Thus, the charge-discharge phenomenon of DC capacitors through DC-link neutral-point can be
226 restrained effectively. The effectiveness of the current compensation device relies on the voltage difference
227 between the boost circuit and the DC-link, which is applied to the inductor (L_2 in Fig. 6), thus producing a
228 compensation current for the DC capacitor.
229

230 *4.2. Inverter circuit*

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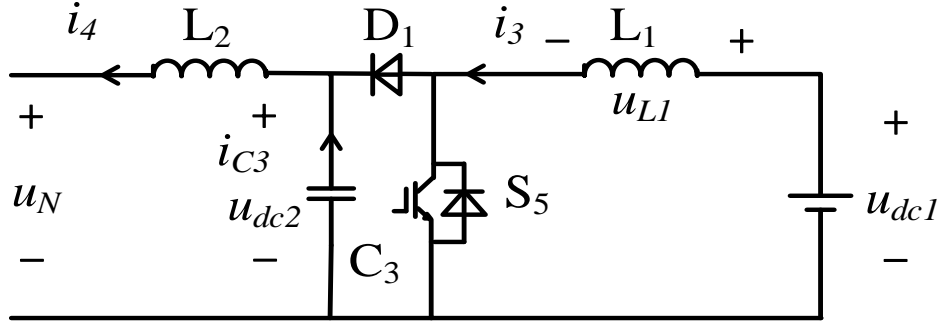
Figure 7. Schematic diagram of the active current compensation device

233

234 Fig. 7 shows the proposed active current compensation device, essentially a boost DC/DC converter
235 circuit, where S_5 is the IGBT power switch; D_1 is a diode preventing reverse current flow; L_1 is a power inductor
236 used for energy storage; L_2 and C_3 form a LC filter for the circuit. Now consider the mathematical model of the
237 active current compensation device. In the circuit, u_{dc1} is the voltage input of the boost DC/DC converter; u_{dc2}
238 is the voltage output of the boost DC/DC convertor; u_N is the DC-link neutral-point voltage; i_{c3} is the current in
239 the capacitor C_3; i_3 is the current in the inductor L_1; i_4 is the compensating current. Suppose $i_{c3(off)}$ and $i_{c3(on)}$ are
240 the current in capacitor C_3 when the switching device S_5 is off and on, respectively; $u_{L1(off)}$ is the voltage across
241 the inductor L_1 when the switching device S_5 is off while $u_{L1(on)}$ is the voltage across the inductor L_1 when the
242 switch S_5 is on.
243 When the switching device S5 is turned on, the state equations of the current compensation device can be
244 described as,

245
$$\begin{cases} L_1 \dfrac{di_3}{dt} = u_{dc1} = u_{L_1(on)} \\ C_3 \dfrac{du_{dc2}}{dt} = i_4 = i_{C_3(on)} \end{cases} \tag{8}$$

246 When the switching device S5 is turned off, the above equation can be writen as

247
$$\begin{cases} L_1 \dfrac{di_3}{dt} = u_{dc1} - u_{dc2} = u_{L_1(off)} \\ C_3 \dfrac{du_{dc2}}{dt} = i_4 - i_3 = i_{C_3(off)} \end{cases} \tag{9}$$

248 During one switching cycle, T_s, the average voltage across the inductor L_1 is,

249
$$\bar{u}_{L_1} = \frac{1}{T_S}\left[\int_t^{t+DT_s} u_{L_1(on)}(\tau)d\tau + \int_{t+DT_s}^{t+T_s} u_{L_1(off)}(\tau)d\tau \right] \tag{10}$$

250
$$\bar{u}_{L_1} = Du_{dc1} + (1-D)(u_{dc1} - u_{dc2}) \tag{11}$$

251 where D represents the duty cycle of the switching device S_5, i.e., the proportion of time during which S_5 is
252 operated.
253 During one switching cycle, the average current in the capacitor C_3 is equal to

254
$$\bar{i}_{C_3} = \frac{1}{T_S}\left[\int_t^{t+DT_s} i_{C_3(on)}(\tau)d\tau + \int_{t+DT_s}^{t+T_s} i_{C_3(off)}(\tau)d\tau \right] \tag{12}$$

255
$$\bar{i}_{C_3} = Di_4 + (1-D)(i_4 - i_3) \tag{13}$$

256 It is well known that the average voltage across an inductor and the average current in a capacitor should
257 be zero during a switching cycle. Hence, under steady state, the current compensation device can be described
258 as follows

259
$$\begin{cases} u_{dc2} = \dfrac{1}{1-D} u_{dc1} \\ i_4 = (1-D) i_3 \end{cases}$$
(14)

260   A control scheme, designed for the active current compensation device, can be derived from this model,
261   as shown in Fig. 8. In this circuit, $u_{dc2}(s)$ is the voltage output of the boost DC/DC converter; $u_N(s)$ is the DC-
262   link neutral-point voltage measured in real time. The reference compensating current $i_c^*(s)$ is obtained by the
263   real-time detection of the current flowing between the neutral points of the inverter. The current $i_c(s)$ is the
264   compensation current generated by the boost circuit. The error current between $i_c^*(s)$ and $i_c(s)$ is then used to
265   generate PWM signals. This signal is based on the triangular wave modulation method, producing a
266   compensating current at the desired level. As with the voltage compensation scheme, a PI controller, represented
267   by $K_p + K_i/s$, is used because it generates a more accurate compensation current.

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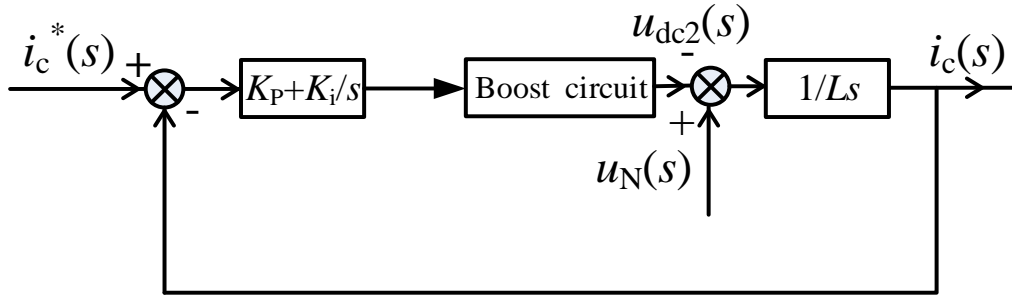
269   **Figure 8.** The control scheme for the active current compensation device

270   **5**. **Results and analysis**

271   *5.1. The inverters*

272   Models of the voltage compensation device and the current compensation device have been built using
273   Simulink SimPowerSystems, as described above and shown in Fig. 3 and Fig. 6, respectively. The parameters
274   used in the models are given in Table 1. The DC-link voltage is 3 kV, a level commonly used in medium voltage
275   power drives; the switching frequency for the NPC three-level inverter is 1 kHz; and the switching frequencies
276   used to control the single-phase inverter for the voltage- and current-compensation device are both set to 10
277   kHz. In order to evaluate the dynamic performance of the proposed inverters, a nonlinear load is used in this
278   study. This load consists of a three-phase rectifier with a resistive (4Ω) and inductive (15mH) load. The use of
279   a nonlinear load increases the neutral-point voltage fluctuation of the DC-link, because the nonlinear load draws
280   a current that is not necessarily sinusoidal, hence generating harmonic currents. The NPC three-level inverter
281   is used with a constant voltage output control strategy, based upon space voltage vector modulation (SVPWM).
282   The error voltage between the NPC three-level inverter output voltage and the reference voltage is processed
283   by a PI controler, which is then used as the input signal for SVPWM to generate appropriate PWM signals. This
284   control scheme has a higher eficiency for controlling the DC-side voltage than the equivalent sine pulse width
285   modulation method.

286   Table 1. Parameters used in the VNPCI and CNPCI inverters

| Parameters of the VNPCI		Parameters of the CNPCI	
Parameters	Value	Parameters	Value
u_{dc}	500 V	u_{dc1}	100 V
C_f	50 μF	L_1	10 mH
L	0.4 mH	L_2	0.5 mH
		C_3	800 μF
Parameters of the NPC three-level inverter			
u_s	3000 V		
C_1, C_2	500 μF		

287
288   In real world applications, the load can be either in a balanced or unbalanced condition. An unbalanced
289   load added to the three phase output voltage of an inverter can result in greater fluctuations in the neutral-point
290   voltage across the DC-link. In the simulation, the inverters are initially connected to a balanced nonlinear load,
291   and resistive (8Ω) and inductive (1.5mH) loads are then applied between phase A and phase B in order to
292   evaluate the dynamic performance of the proposed compensation devices under a unbalanced load condition.
293   The unbalanced load occurs at 10.05 s and lasts for 0.05 s.
294   Firstly, a conventional NPC three-level inverter, under balanced and unbalanced working load conditions,
295   has been modelled and investigated. Fig. 9(a) and (b) show the waveform of the neutral-point voltage u_o, the
296   phase A to phase B voltage u_{AB} of the conventional inverter. The neutral-point voltage fluctuation across the
297   DC-link is severe, even in the balanced load condition; the range of the fluctuation reaches a value of 200V.
298   During the unbalanced load condition, applied from 10.05s to 10.1s, it can be seen the neutral-point voltage
299   fluctuation range increases to 300V. The THD (total harmonic distortion) of the output voltage waveform across
300   the inverter is 45.30%.
301

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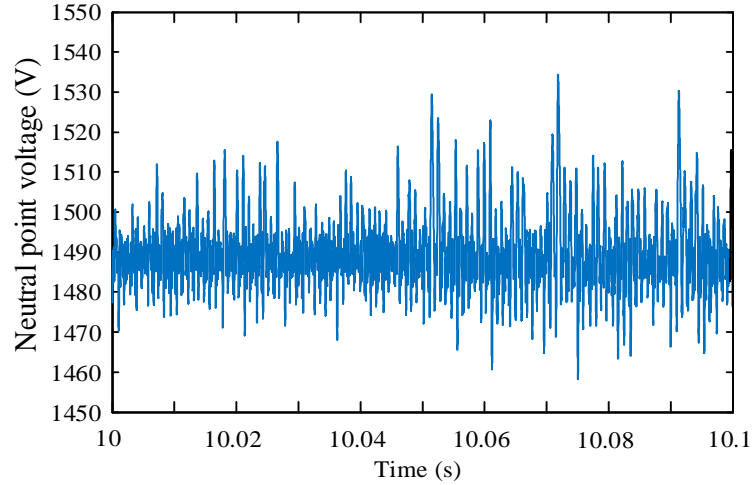303   a.   Voltage waveform of neutral-point voltage u_o
304
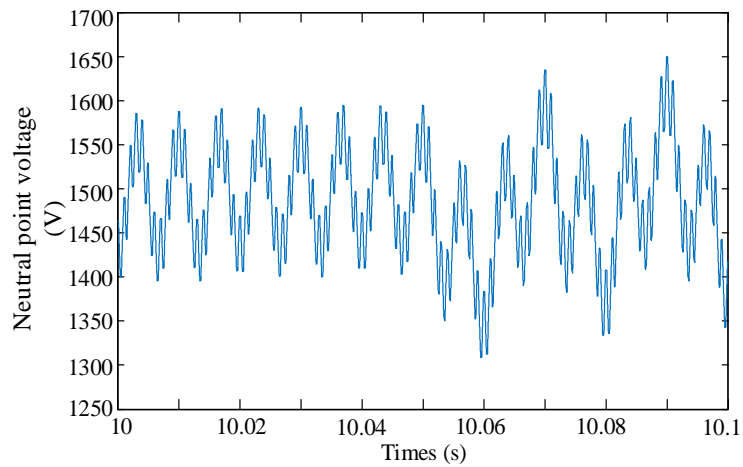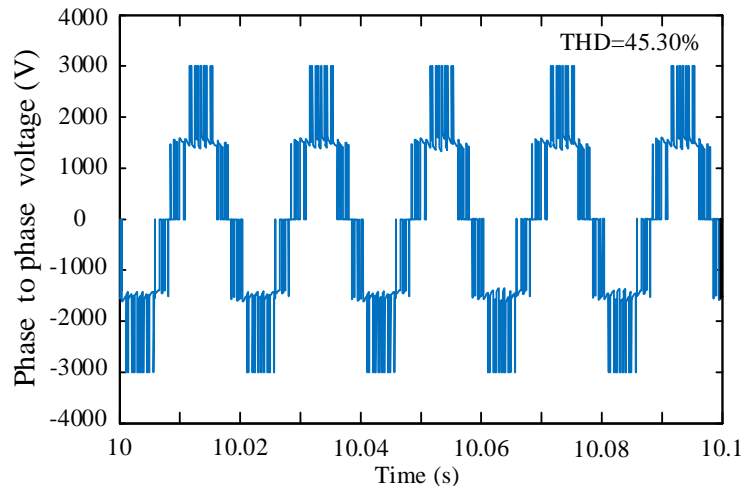
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306   b.   Voltage waveform of phase A to phase B voltage u_{AB}
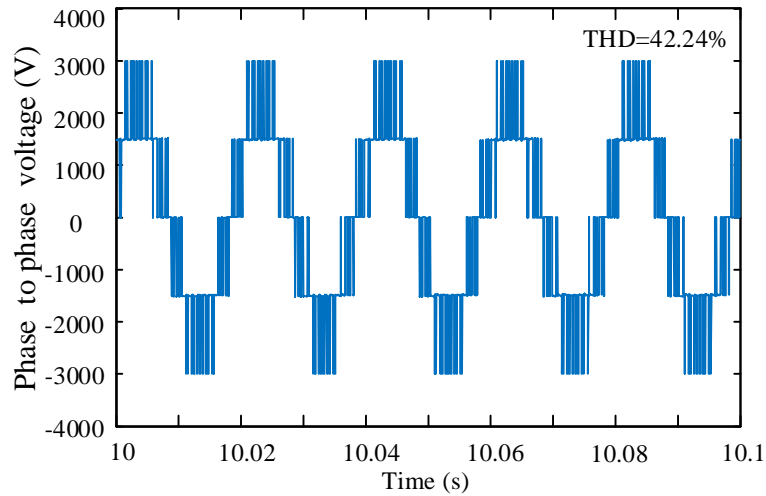
307   **Figure 9.** Voltage waveforms of the conventional NPC in a load swell

308   Fig. 10(a) and (b) show the waveform of the neutral-point voltage u_o, the phase A to phase B voltage u_{AB}
309   of the proposed voltage compensated NPC inverter under the balanced and unbalanced working load conditions.
310   With the voltage compensation device being added, the neutral-point voltage fluctuation of DC-link is
311   suppressed effectively, being reduced to 40V. Similarly, an unbalanced load is applied at 10.05 s, lasting 0.05
312   s. The neutral-point voltage fluctuation of DC-link is reduced to 75V under the unbalanced load condition. The
313   THD of output voltage of the inverter is 42.24%.

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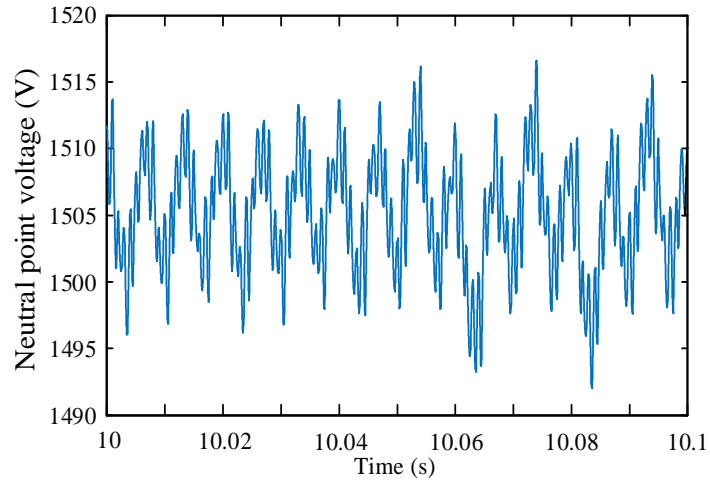315   a.   Voltage waveform of neutral-point voltage u_o

316
317   b.   Voltage waveform of the phase A to phase B voltage u_{AB}
318   **Figure 10.** Voltage waveforms of the proposed VNPCI in a load swell
319

320   Fig. 11(a) and (b) shows the neutral-point voltage u_o, the phase A to phase B voltage u_{AB} of the proposed
321   current compensated NPC inverter under the balanced and unbalanced working load conditions. With the
322   current compensation device being added, the neutral-point voltage fluctuation of DC-link is suppressed further
323   to 18V. Under the unbalanced load condition between 10.05 s and 10.1 s, the neutral-point voltage fluctuation
324   of DC-link is reduced to 25V. The THD of output voltage of the NPC three-level inverter is 42.08%.
325   The results clearly show that the current compensated NPC inverter (CNPCI) has a better performance
326   than the voltage compensated NPC inverter (VNPCI). Fig. 10 and Fig. 11 demonstrate that the CNPCI can
327   restrict the neutral-point voltage fluctuation of the DC-link to 0.6% and 0.83%, respectively, when the CNPCI
328   works under typical balanced and unbalanced working load conditions. However, the VNPCI restrains the
329   neutral-point voltage fluctuation of DC-link to 1.2% and 2.3%, respectively, in the same conditions. The
330   waveform comparison of neutral-point voltage u_o produced in different condition is shown in Fig. 12. The effect
331   of the switching frequency on the output performance was also investigated. It was found a frequency higher
332   than 2 kHz can produce acceptable results but the use of 10 kHz switching frequency produced the best results
333   although it might be too fast for the device to work at such a high voltage level.
334

335

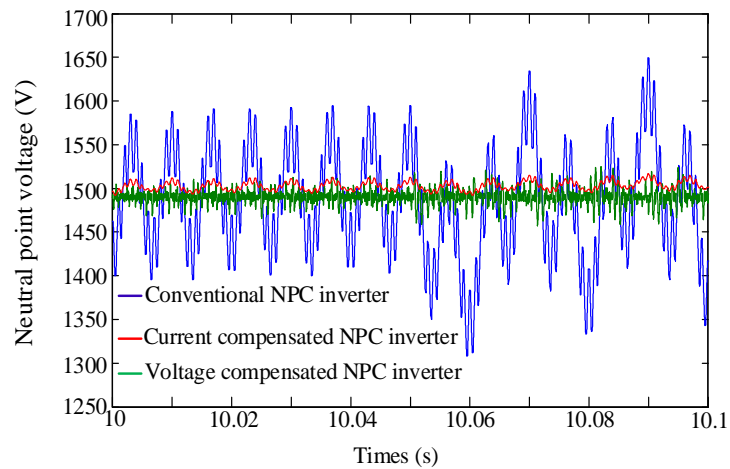a.   Voltage waveform of neutral-point voltage u_o

337
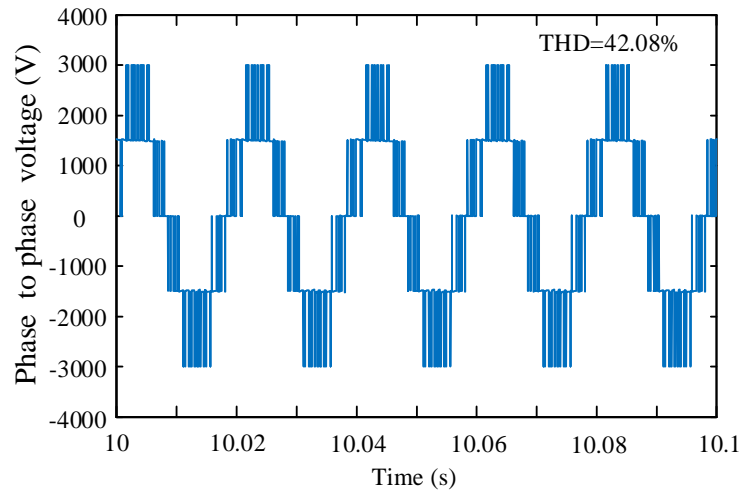
b.   Voltage waveform of the phase A to phase B voltage u_{AB}

Figure 11. Voltage waveforms of the proposed CNPCI in a load swell

341
342   **Figure 12.** Waveform comparison of the neutral-point voltage u_o produced in the three inverter topologies
343

344   The VNPCI only eliminates the voltage fluctuation at the neutral-point of three-phase bridge arm; there is
345   still fluctuation of the neutral-point voltage of the DC-link. This means the fluctuation problem cannot be
346   eliminated thoroughly. However, the CNPCI can eliminate the neutral-point voltage fluctuation of the DC-link
347   more effectively because the CNPCI offsets the current that flows between the neutral point of the DC-link

348 capacitors and the neutral point of the three-phase bridge circuit in the inverter, which is the cause of the voltage
349 fluctuation. In addition, for the VNPCI, an isolated transformer is required, which should be able to handle
350 several harmonic components without entering to the saturation region in the primary side and handle secondary
351 side voltage range quickly to compensate the zero sequence voltage generated at the NPC converter. A
352 complicated control scheme is therefore needed to overcome these problems [27]. On the contrary, the CNPCI
353 avoids using the isolated transformer; the cost to manufacture and assemble the CNPCI is therefore lower than
354 the VNPCI; the CNPCI requires only one IGBT power switching device (the most expensive component in the
355 circuit), while the VNPCI needs four IGBT power switches and a coupling transformer. Thus, the CNPCI offers
356 a more cost-effective performance.

357 The selection of PI control parameters were made by trial and error, aiming to achieve an optimal
358 performance from tests. The proportional response can be adjusted by multiplying the error (i.e., the voltage
359 difference in the case of the VNPCI and the current difference in the case of the CNPCI) by the proportional
360 gain K_p. The integral term in the PI controller is the sum of the instantaneous error over time, thus giving the
361 accumulated offset, which is then multiplied by the integral gain K_i. For the VNPCI, the selected value of K_p
362 and K_i are 5 and 10, respectively, while, for the CNPCI, the selected value of K_p and K_i are 10 and 0.5,
363 respectively. Results have shown that the use of these parameters can provide an improved performance of the
364 controllers.

365 *5.2. The shunt active power filters (SAPF)*

366 The two proposed inverters are now applied in the SAPF that is indispensable part of the grid system. The
367 SAPFs incorporating with the current compensated NPC inverter and the voltage compensated NPC inverter
368 have been built and simulated. One of the typical SAPF applications is in the AC 400V DG system [28]; but
369 unlike the normal inverter, in order to satisfy the working condition in three phase power system, the DC link
370 voltage of SAPF must be over 3 times higher than the phase voltage. Thus, the NPC three-level inverter is very
371 suitable to apply in SAPF due to high DC link voltage. The parameters used in the model are defined as follows:
372 DC link voltage of SAPF is 800V; supply fundamental frequency f = 50Hz; filter line inductance Ls= 2mH;
373 other parameters used for the inverters are referred to Table 1. It is noteworthy that the use of a low DC link
374 voltage, rather than the 3000V previously discussed, was to assess the performance of the proposed inverters
375 for this particular application in SAPF. As mentioned above, nonlinear loads are often connected in the power
376 grid and the load condition will affect the work efficiency of the NPC three-level SAPF. The SAPF is firstly
377 connected to a balanced nonlinear load and then to an unbalanced load emulated by a resistive (8Ω) and
378 inductive (1.5mH) load being applied between phase A and phase B. The unbalanced load also occurs at 10.05
379 s and lasts 0.05 s.

380 Firstly, a SAPF based on the traditional NPC three-level inverter connected with the three phase nonlinear
381 load, as shown in Fig. 2, has been investigated under the balanced and unbalanced working load conditions.
382 Fig. 13 show the waveform of grid current of phase A, as an example. The grid current distorts heavily in both
383 balanced and unbalanced load condition, and the THD of the grid current is 18.52%.

384
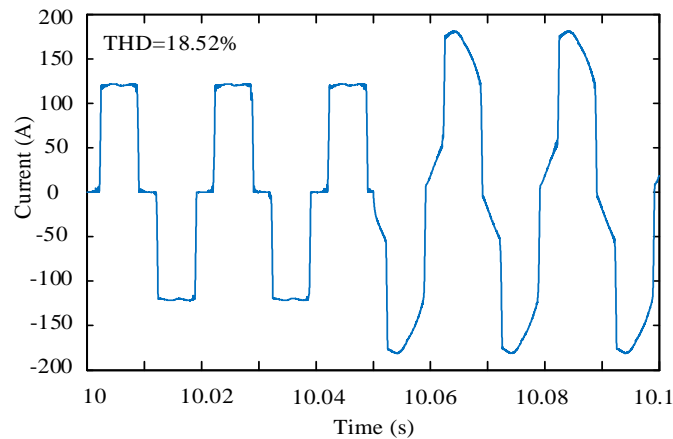
385

386 **Figure 13.** Waveform of phase-A current of the power grid under the nonlinear load

387   Fig. 14 shows the waveform of the filter output of phase A, i.e., the currents i_{ca}, i_{cb} and i_{cc} as shown in Fig.
388   2, and the grid currents of the proposed VNPCI three-level SAPF, i.e., the currents i_{sa}, i_{sb} and i_{sc} as shown in
389   Fig. 2, under the typical balanced and unbalanced working load conditions. Essentially, the filter output currents
390   are effective to compensate the harmonics being injected from nonlinear loads, hence improving the quality of
391   the gird currents. The frequency component is dominant at 50 Hz while other harmonic components in phase-
392   A current are now eliminated effectively. The THD of the grid current is reduced to 2.05%. Fig. 15 shows the
393   waveform of the grid currents of the proposed CNPCI three-level SAPF under typical balanced and unbalanced
394   working load conditions. It can be seen that the harmonic currents in phase A can be eliminated more effectively.
395   The THD of the grid current is reduced further to 1.7%.

396
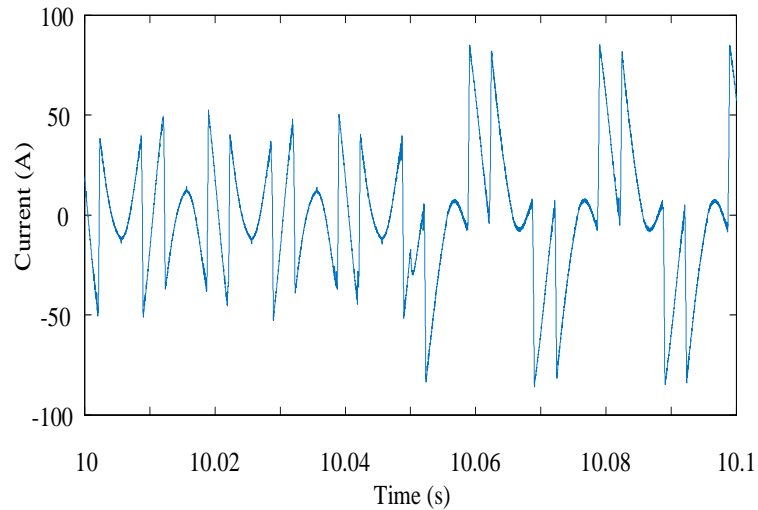
397
398   a.   Waveform of the phase-A current in the filter output
399
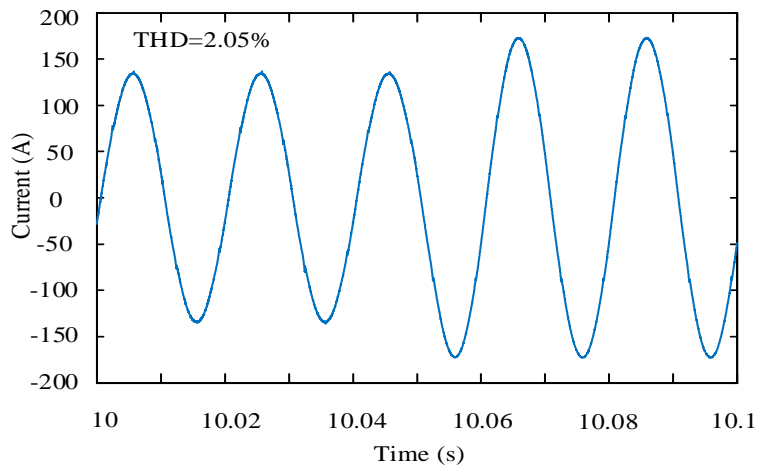
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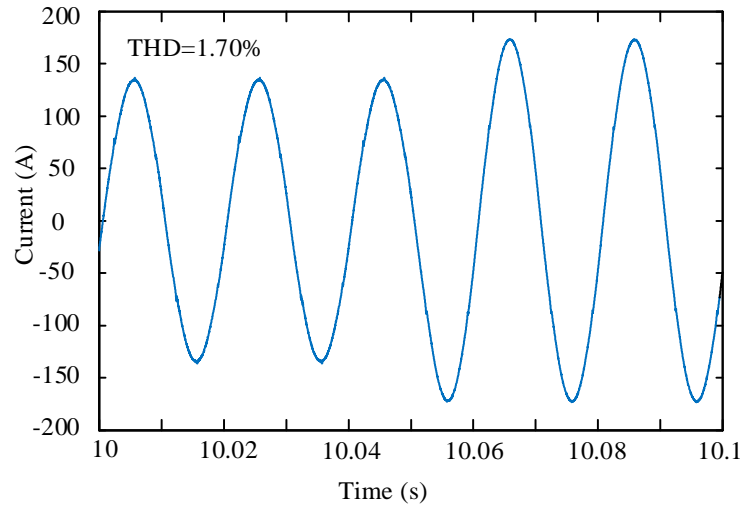401   b.   Waveform of the phase-A current in the power grid

402   **Figure 14.** Waveform of the phase-A currents in the filter output and the power grid empolying the
403   proposed VNPCI three-level SAPF

THD=1.70%

404

405   **Figure 15.** Waveform of the power grid currents employing the proposed CNPCI three-level SAPF

406   **6. Conclusions**

407   The paper presents two new NPC three-level inverter topologies in order to eliminate excessive voltage
408   fluctuation happened at the neutral-point of DC-link capacitors of the inverter. The first is voltage dependent,
409   which adopts a voltage compensation method to restrain the neutral point voltage fluctuation. The second is
410   current dependent, using a current compensation method to restrict the voltage fluctuation. The results show
411   that both topologies can suppress the neutral-point voltage fluctuation of the DC-link effectively under typical
412   balanced and unbalanced working load conditions. The current compensated NPC inverter outperforms the
413   voltage compensated NPC inverter. Furthermore, these compensated NPC three-level inverters are applied to a
414   shunt active power filter in the grid lines. It is shown that the proposed approaches are effective and feasible for
415   eliminating harmonic currents and therefore improving power quality of the grid system when connected with
416   nonlinear loads.
417   Future work will focus on experimental testing of the proposed NPC three-level SAPFs to further verify
418   their performance. Optimal selection of PI control parameters for the inverters will also be investigated in order
419   to further optimize system performance under different load conditions. In addition, the application of the
420   proposed current compensated NPC inverter is being considered in both a wind power generation system and a
421   small grid system in the laboratory in order to address the power quality issues related to inverter-coupled
422   generation and associated loads.
423
424

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