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High Current GaSb/InAs(Sb) Nanowire Tunnel Field-Effect Transistors

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Abstract—We present electrical characterization of GaSb/InAs(Sb) nanowire tunnel field-effect transistors. The broken band alignment of the GaSb/InAs(Sb) heterostructure is exploited to allow for inter-band tunneling without a barrier, leading to high on-current levels. We report a maximum drive current of $310 \mu\text{A}/\mu\text{m}$ at $V_{DS} = 0.5 \text{ V}$. Devices with scaled gate oxides display transconductances up to $g_m = 250 \text{ mS}/\text{mm}$ at $V_{DS} = 300 \text{ mV}$, normalized to the nanowire circumference at the axial heterojunction.

Index Terms—Tunnel field-effect transistors (TFET), broken gap, InAs, GaSb, III-V

I. INTRODUCTION

THE rapid development of semiconductor technology during the last few decades has resulted in high-performance transistors in both Si and III-V semiconductor technologies [1], [2]. However, MOSFETs suffer from a fundamental lower limit of $60 \text{ mV}/\text{decade}$ subthreshold swing (SS) at room temperature, and a corresponding lower limit of the power dissipation at a given threshold voltage and on-current level. There is a demand for devices with very steep inverse subthreshold slopes in order to maintain a high I_{ON}/I_{OFF} ratio while lowering the supply voltage. For this reason, steep-slope devices, such as tunnel field-effect transistors (TFETs), are now being studied in great detail in different material systems. Recent reports on devices with SS below $60 \text{ mV}/\text{decade}$ [3]–[5], however show that the devices suffer from low on-current levels. Furthermore, there are often difficulties in integrating high- κ dielectrics with III-Vs to achieve optimized device electrostatics [6]. Since the current in a p - i - n TFET device relies on charge carriers tunneling through a barrier at a given limited probability, the on-current is invariably lower than for a corresponding MOSFET device [7], [8]. As an alternative to conventional designs, we here focus on the GaSb/InAs(Sb) heterostructure, which forms a broken type II band alignment, and thus allows for inter-band tunneling without a barrier.

Based on highly doped p^+/n^+ junctions of this particular heterostructure, we have recently demonstrated Esaki diodes with reverse-bias current densities up to $I_{reverse} = 3.6 \text{ MA}/\text{cm}^2$ [9]. Here we investigate the TFET properties of such heterostructures, with a p^+/n doping profile and it is found that such devices exhibit correspondingly high on-current levels. Furthermore, we report on the temperature behavior of such devices as well as the effect of various device geometries.

II. MATERIALS AND DEVICE FABRICATION

GaSb/InAs(Sb) nanowires were grown from Au aerosols on a GaAs substrate by means of metalorganic vapor phase epitaxy. A short GaAs stem was first grown in order to facilitate

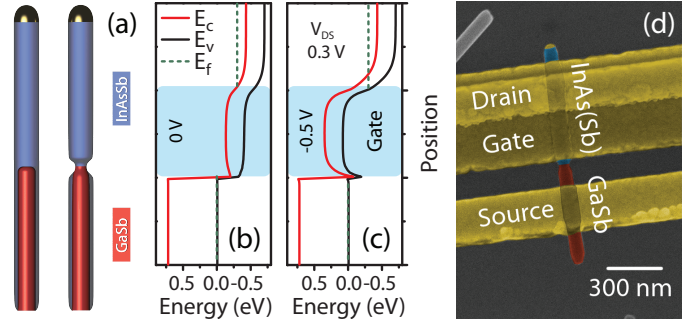


Fig. 1. (a) Schematics of the two types of nanowires used in the study. (b, c) Simulated band structures of an ideal device at 300 K including an exponentially graded Sb composition from 0.4 to 0.1 over 10 nm at the interface at $V_{DS} = 300 \text{ mV}$ and at (b) $V_{GS} = 0 \text{ V}$ and (c) $V_{GS} = -0.5 \text{ V}$. Note that applied gate voltage and semiconductor potential do not follow as 1:1 in the measured devices. (d) A colorized scanning electron microscopy image of a completed device. Note that the apparent nanowire diameter is here increased by the HfO_2 film, and that gate overlap/underlap varies between devices as discussed in the text below.

the nucleation of the GaSb segment [10], into which Zn (Zn/Ga molar flow fraction = 0.56) is also introduced to reduce the series resistance [9]. Subsequently, an unintentionally doped axial InAs(Sb) segment is grown which also forms a thin, $\sim 5 \text{ nm}$, shell around the GaSb segment. This shell aids in reducing the series resistance to the source electrode and allows for a one-step fabrication process for the source and drain electrodes. In order to minimize a potential leakage current in the shell, and to reduce the cross-sectional area of the conducting channel, the nanowires were annealed in H_2 during the final stage of the growth, forming a constriction at the axial GaSb/InAs(Sb) heterointerface [11]. As a reference, nanowires were also grown where the Zn-doping and H_2 annealing were omitted. Assuming a hole mobility between $70 \text{ cm}^2/\text{Vs}$ (calculated from [12]) and $700 \text{ cm}^2/\text{Vs}$ [1], and a measured resistivity of $7.1 \text{ m}\Omega \cdot \text{cm}$ [9], we estimate the carrier concentration in the GaSb segment to be in the range $1.3 \cdot 10^{18} - 1.3 \cdot 10^{19} \text{ cm}^{-3}$. A corresponding estimate for the InAs(Sb) segments yields a carrier concentration of $6 \cdot 10^{17} \text{ cm}^{-3}$ [13].

After the growth, the nanowires were dry-deposited onto prepatterned Si chips with a 100-nm-thick thermally grown SiO_2 . Source and drain electrodes were defined by electron beam lithography (EBL) followed by thermal evaporation of Ni and Au. A lift-off window for the high- κ dielectric was defined by EBL, followed by an atomic layer deposition of an $\text{Al}_2\text{O}_3/\text{HfO}_2$ bi-layer (2/70 cycles) both deposited at $100 \text{ }^\circ\text{C}$ corresponding to an EOT of 2 nm, assuming $\epsilon_r = 15$. As a final step, a Ni/Au top-gate was formed. All room temperature

measurements were carried out in darkness and vacuum.

III. RESULTS AND DISCUSSION

Fig. 2a presents the output characteristic for a reference device without a constriction at the axial heterointerface (as displayed in the schematics in Fig. 1a) and without Zn doping in the GaSb segment. In this device, carrier transport can occur along the InAs(Sb) shell and across the GaSb/InAs(Sb) heterojunction simultaneously due to the ambipolarity of the core-shell system [12]. At negative gate bias, the InAs(Sb) is depleted of electrons and the majority of the current is forced through the heterojunction. At positive gate bias, electrons accumulate at the surface, enabling n-type conduction along the shell with reduced tunneling. It is not possible to turn this device off.

Fig. 2b displays the output characteristic for a device with a Zn-doped GaSb segment and where a constriction has been formed at the axial heterointerface ($d = 35 \text{ nm} \pm 5 \text{ nm}$). We calculate an on-current of $91 \mu\text{A}/\mu\text{m} \pm 13 \mu\text{A}/\mu\text{m}$ at $V_{DS} = V_{GS} - V_T = 0.5 \text{ V}$ (normalized to the nanowire circumference, $\pi \cdot d$), and a maximum on-current of $310 \mu\text{A}/\mu\text{m} \pm 45 \mu\text{A}/\mu\text{m}$ ($V_{DS} = 0.5 \text{ V}$, $V_{GS} - V_T = 2 \text{ V}$), corresponding to $R_{ON} = 1.57 \Omega \cdot \text{mm}$, exceeding the drive currents of e.g. staggered AlGaSb-InAs TFETs [6].

As illustrated, the device in Fig. 2b has a 35 nm gate underlap to the heterojunction. In an ideal case, this would constitute a tunnel junction integrated in series with an InAs(Sb) MOSFET. Such a tunnel junction is normally open for conduction due to the broken gap, and the current is modulated by the gate-action imposed on the InAs(Sb) segment. In the off-state, the device will suffer from the ungated segment, allowing tunneling across the heterostructure. Minority carriers (holes) injected from the drain may also accumulate and become trapped under the gate due to a barrier in the valence band to the GaSb.

The output characteristics of a device where the gate overlaps the heterojunction is included in Fig. 2c & d. The better off-state device performance we attribute to two effects; (i) the improved electrostatics at the heterojunction, gating the constriction rather than the thicker InAs(Sb), in agreement with the results of Tomioka et al. [5] and (ii) the device design layout itself as discussed next. For the device in Fig 2c & d, where the gate overlaps the heterointerface, we argue that in the on-state, the bands in the GaSb and the InAs(Sb) bend downwards. The bands are likely more easily modulated in the InAs(Sb) segment but some modulation of the GaSb is also expected. This may compromise the on-state by forming a barrier in the valence band in the GaSb segment, and reduce the probability of inter-band tunneling. However, Fermi level movement in GaSb-based MOS-structures is typically difficult due to the high number of acceptor-like interface traps (D_{it}) between GaSb and high- κ dielectrics [14]. In addition, the high Zn-doping level of the GaSb should lead to a limited movement of the bands on the GaSb side. For this reason, we argue that a device with a gate overlap better cuts off the tunneling path at the source heterojunction, which is otherwise open for an underlapping device (Fig. 2b). Furthermore, the

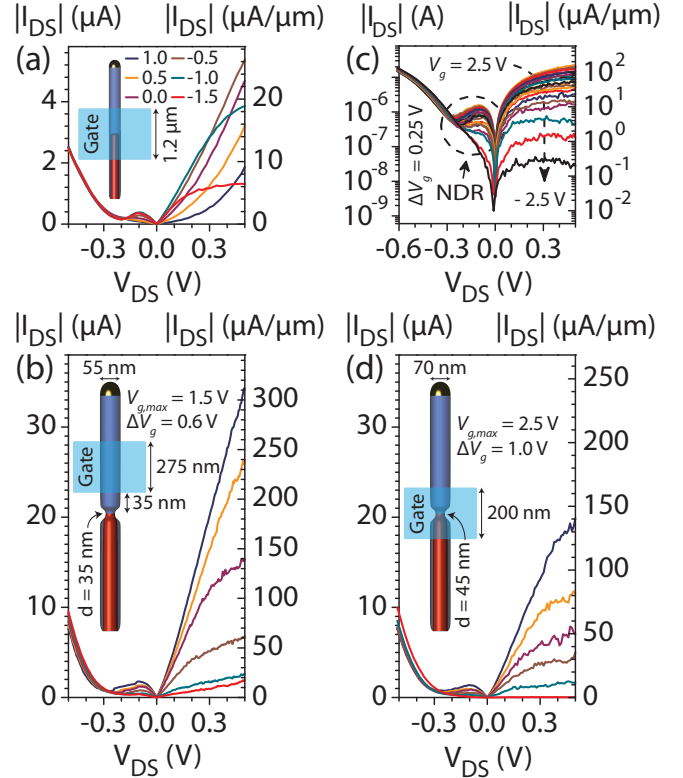


Fig. 2. Room temperature output characteristics of different TFET structures (reverse biased with GaSb grounded) with data normalized with respect to the circumference of the constriction. (a) I_{DS} - V_{DS} sweep for an undoped nanowire without a constriction ($d = 65 \text{ nm}$). (b-d) Output characteristics for TFET structures with a constriction and Zn-doped GaSb segment. (b) 35 nm gate underlap and 35 nm diameter at the GaSb/InAs(Sb) heterointerface. (c-d) 120 nm gate overlap and 45 nm diameter at the heterointerface constriction.

improved electrostatics at the constriction may lead to a better gate response. However, the devices are sensitive to measurement history, charging and hysteresis effects which makes the analysis somewhat challenging, e.g. determining a well-defined threshold voltage. The devices presented above show the extremes of a number of devices studied.

Evaluating the negative differential resistance region in the underlapping device, we calculate a maximum peak-to-valley current ratio of 3 with a maximum peak-current of $240 \text{ kA}/\text{cm}^2$ (forward biased with the InAs(Sb) segment grounded). We observe that V_P remains constant, or moves to *slightly higher* V_{DS} bias with increasing gate bias. In the ideal case of a gated resistance (MOSFET) integrated in series with a passive tunnel junction we expect V_P to move to lower V_{DS} values with increasing gate bias. The lack thereof indicates that the band alignment at the tunnel junction is affected by the gate.

Fig. 3a & b display the transfer characteristic of a device where the EOT is scaled to 1.3 nm and the gate has been aligned to the heterointerface ($\sim 5 \text{ nm}$ overlap), with $L_G = 290 \text{ nm}$. We calculate an on-current of $62 \mu\text{A}/\mu\text{m}$ at $V_{DS} = 0.3 \text{ V}$ and $V_{GS} - V_T = 0.5 \text{ V}$, $V_T = -0.51 \text{ V}$, and a maximum on-current of $130 \mu\text{A}/\mu\text{m}$ ($V_{DS} = 0.3 \text{ V}$, $V_{GS} - V_T = 1.75 \text{ V}$). The drain-induced barrier lowering was determined between $V_{DS} = 0.05$ and 0.3 V to be $280 \text{ mV}/\text{V}$. The maximum I_{ON}/I_{OFF} ratio increases from 143 at RT to 10^4 at 4.2 K and the SS decreases with temperature from $320 \text{ mV}/\text{decade}$ at 295 K

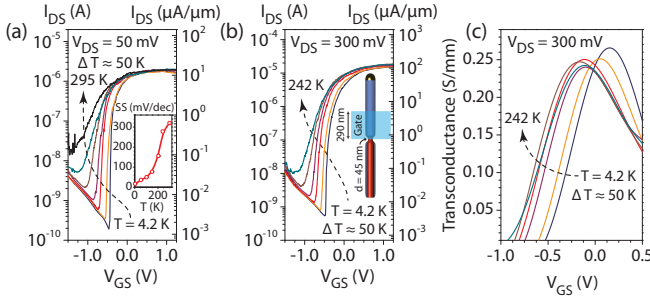


Fig. 3. Electrical data for a nanowire TFET, $d = 45$ nm, where the gate oxide thickness is scaled to 5 cycles of Al_2O_3 and 50 cycles of HfO_2 . The data is normalized to the constriction circumference. (a) Temperature dependent I_{DS} - V_{GS} characteristics at $V_{DS} = 50$ mV from 4.2 K up to 295 K in increments of approximately 50 K. The inset shows the subthreshold swing as a function of temperature. (b) Temperature dependent I_{DS} - V_{GS} characteristics and (c) transconductance at $V_{DS} = 300$ mV from 4.2 K to 242 K, $\Delta T \approx 50$ K.

to 17 mV/decade at 4.2 K as seen in the inset of Fig. 3a. Similar values have been reported in other III-V TFET devices [15]. The temperature dependent SS is likely a result of trap-assisted tunneling via the high D_{it} at the high- κ /semiconductor interface. The determined activation energy, when reverse-biased, in the off-state from Fig. 3a (not shown) corresponds to the band gap of $\text{InAs}_{0.9}\text{Sb}_{0.1}$ (0.27 eV). Furthermore, the onset of a temperature-independent ambipolar current is also evident in Fig. 3a & b, most likely due to band-to-band tunneling at the gate-drain junction related to the narrow band gap of the $\text{InAs}(\text{Sb})$. The temperature dependence of the valley current (forward-biased with $\text{InAs}(\text{Sb})$ grounded, not shown) suggests activation energies well-below $E_g/2$ of $\text{InAs}(\text{Sb})$ indicating that trap-assisted tunneling is limiting the off-state performance.

Fig. 3c displays the temperature dependent transconductance at $V_{DS} = 300$ mV and the maximum extrinsic transconductance is extracted at 250 mS/mm ($V_{GS} - V_T = 0.5$ V). The transconductance is nearly temperature independent, suggesting that the temperature dependent scattering mechanisms are not limiting the on-state of the device. In order to improve the off-state characteristics we propose two approaches; (i) increasing the band gap of the material in the drain by replacing $\text{InAs}(\text{Sb})$ with e.g. InGaAs to decrease the band-to-band tunneling at the gate-drain junction, (ii) reducing trap assisted tunneling by surface pretreatment/passivation and/or further improving the high- κ quality, by e.g. higher deposition temperatures, to lower the SS. To increase the on-current further we suggest a higher doping of Zn in the GaSb to maintain a low-ohmic junction when gating the heterointerface as well as reducing the series resistance.

IV. CONCLUSIONS

In this paper, experimental data for GaSb/ $\text{InAs}(\text{Sb})$ tunnel field-effect transistors are presented, demonstrating high current densities attributed to the broken type II band alignment. These devices show on-currents of $310 \mu\text{A}/\mu\text{m}$ ($R_{ON} = 1.6 \Omega \cdot \text{mm}$). Devices with a scaled gate oxide display a maximum extrinsic transconductance of 250 mS/mm at $V_{DS} = 300$ mV. The inverse subthreshold slope at room temperature is 320 mV/decade at $V_{DS} = 50$ mV and is likely limited by a high D_{it} at the high- κ /semiconductor interface. At this point, the

minimum value of the off-current is limited by the narrow band gap of $\text{InAs}(\text{Sb})$.

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