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LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

Microwave CMOS VCOs and Front-Ends
- using integrated passives on-chip and on-carrier

Markus Törmänen

Lund 2010

LUND INSTITUTE OF TECHNOLOGY
Lund University

Department of Electrical and Information Technology
Lund University
P.O. Box 118
SE-221 00 LUND
SWEDEN

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Abstract

The increasing demand for high data rates in wireless communication systems is increasing the requirements on the transceiver front-ends, as they are pushed to utilize more and wider bands at higher frequencies. The work in this thesis is focused on receiver front-ends composed of Low Noise Amplifiers (LNAs), Mixers, and Voltage Controlled Oscillators (VCOs) operating at microwave frequencies.

Traditionally, microwave electronics has used exclusive and more expensive semiconductor technologies (III-V materials). However, the rapid development of consumer electronics (e.g. video game consoles) the last decade has pushed the silicon CMOS IC technology towards even smaller feature sizes. This has resulted in high speed transistors (high f_T and f_{max}) with low noise figures. However, as the breakdown voltages have decreased, a lower supply voltage must be used, which has had a negative impact on linearity and dynamic range. Nonetheless, todays downscaled CMOS technology is a feasible alternative for many microwave and even millimeter wave applications.

The low quality factor (Q) of passive components on-chip usually limits the high frequency performance. For inductors realized in a standard CMOS process the substrate coupling results in a degraded Q. The quality factor can, however, be improved by moving the passive components off-chip and integrating them on a low loss carrier. This thesis therefore features microwave front-end and VCO designs in CMOS, where some designs have been flip-chip mounted on carriers featuring high Q inductors and low loss baluns. The thesis starts with an introduction to wireless communication, receiver architectures, front-end receiver blocks, and low loss carrier technology, followed by the included papers.

The six included papers show the capability of CMOS and carrier technology at microwave frequencies: Papers II, III, and VI demonstrate fully integrated CMOS circuit designs. An LC-VCO using an accumulation mode varactor is presented in Paper II, a QVCO using 4-bit switched tuning is shown in Paper III, and a quadrature receiver front-end (including QVCO) is demonstrated in paper VI. Papers I and IV demonstrate receiver front-ends using low loss baluns on carrier for the LO and RF signals. Paper IV also includes a front-end using single-ended RF input which is converted to differential form in a novel merged LNA and balun. A VCO demonstrating the benefits of a high Q inductor on carrier is presented in Paper V.

Sammanfattning (in Swedish)

De ökande kraven på högre datahastigheter inom trådlös kommunikation ställer allt högre krav på både radiosändare och mottagare, då dessa behöver utnyttja fler frekvensband med större bandbredd vid högre frekvenser. Fokus i denna avhandling ligger på högfrekvensdelen av radiomottagaren, som består av lågbrusförstärkare, blandare, och oscillatorer vid mikrovågsfrekvenser.

Traditionellt har mikrovågselektronik använt sig av exklusiva och dyra halvledarteknologier (III-V material). Den snabba elektronikutvecklingen för konsumentprodukter (t.ex. TV-spelkonsoler) har det senaste årtiondet påskyndat utvecklingen av den kiselbaserade CMOS teknologin. Detta har lett till små och snabba transistorer (hög f_T och f_{max}) med låg brusfaktor. Samtidigt tål transistorerna inte så höga spänningar och den lägre matningspänningen har tyvärr en negativ effekt på linjäriteten och det dynamiska området. Trots detta är dagens moderna CMOS-teknologi lämplig för många mikrovågs- och även millimetervågstillämpningar.

Ofta begränsar förlusterna (på grund av lågt Q-värde) i de passiva komponenterna kretsens prestanda vid högre frekvenser. Speciellt för induktanser i en standard CMOS process bidrar den elektromagnetiska kopplingen till substratet till ett lägre Q-värde. Genom att flytta de passiva komponenterna från chipet till en bärare med låga förluster kan Q-värdet förbättras avsevärt. I denna avhandling presenteras kretsar med lågbrusförstärkare, blandare och oscillatorer i CMOS-teknologi på mikrovågsfrekvenser. En del av kretsarna har monterats på bärare med induktanser och baluner med låga förluster.

Avhandlingen börjar med en introduktion till trådlös kommunikation, arkitekturer för mottagare, blocken i mottagaren, bärarteknologi med låga förluster, och följs av de sex inkluderade vetenskapliga artiklarna.

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Preface

This thesis summarizes my academic work in the Analog/RF group at the department of Electrical and Information Technology, Lund University, for the Ph.D. degree in Circuit Design. The thesis consists of two parts, where the first part is a general introduction to the research area, and the second part is the included research papers, listed below:

M. Törmänen and H. Sjöland, "A 20-GHz 130-nm CMOS Front-End using Baluns on Glass Carrier," *IEEE Proc. 2nd International Conference on Signals, Circuits & Systems, SCS 2008*, pp. 1-4, Nov. 2008, Hammamet, Tunisia.

M. Törmänen and H. Sjöland, "A 25-GHz Differential LC-VCO in 90-nm CMOS," *IEEE Proc. Asia Pacific Conference on Circuits and Systems, APCCAS 2008*, pp. 554-557, Nov. 30 - Dec. 9, 2008, Macao, China.

M. Törmänen and H. Sjöland, "A 24-GHz LC-QVCO in 130-nm CMOS using 4-bit Switched Tuning," *IEEE Proc. International Conference on Microelectronics, ICM 2008*, pp. 462-465, Dec. 2008, Sharjah, United Arab Emirates.

M. Törmänen and H. Sjöland, "Two 24 GHz Receiver Front-ends in 130-nm CMOS using SOP Technology," *IEEE Proc. Radio Frequency Integrated Circuits Symposium, RFIC 2009*, pp. 559-562, June 2009, Boston, Massachusetts, USA.

M. Törmänen and H. Sjöland, "A 24 GHz VCO with 20 % tuning range in 130-nm CMOS using SOP Technology," *IEEE Proc. Radio Frequency Integrated Circuits Symposium, RFIC 2009*, pp. 473-476, June 2009, Boston, Massachusetts, USA.

M. Törmänen and H. Sjöland, "A 24-GHz Quadrature Receiver Front-end in 90-nm CMOS," *IEEE Proc. Asia Pacific Microwave Conference, APMC 2009*, Dec. 2009, Singapore.

Related publications

The following papers contain overlapping, complementing, and additional material, but are not considered part of this thesis.

M. Törmänen and H. Sjöland, "A 26-GHz LC-QVCO in 0.13-um CMOS," *IEEE Proc. Asia Pacific Microwave Conference, APMC 2007*, pp. 1769-1772, Dec. 2007, Bangkok, Thailand.

M. Törmänen and H. Sjöland, "A 25-GHz Low Phase Noise LC-VCO," Proc. SSoCC 2008, May 2008, Gnesta, Sweden.

K. K. Lee, C. Bryant, M. Törmänen, and H. Sjöland, “A 65-nm CMOS ultra-low-power LC quadrature VCO,” *IEEE Proc. NORCHIP 2009*, Nov. 2009, Trondheim, Norway.

M. Törmänen and H. Sjöland, “A 24 GHz SOP VCO with 20 % tuning range,” GigaHertz Symposium 2010, March 2010, Lund, Sweden.

M. Törmänen and H. Sjöland, “K-band Receiver Front-ends in 0.13μm CMOS using Carrier Technology,” Proc. SSoCC 2010, May 2010, Kolmården, Sweden.

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During my time as a graduate student I have met many people that contributed in one way or another to this thesis, but to mention them all here is impossible and I restrict myself to those that have had substantial impact on this work.

I have been fortunate to be part of the Analog/RF Cicuit Design group at the Dept. of Electrical and Information Technology, Lund University. During this time it has been a privilege working with a highly competent supervisor, Prof. Henrik Sjöland, whos knowledge and experience in the field is extensive. His enthusiasm to attack various problems has been very inspiring.

I would like to thank both current and former colleagues in the Analog/RF group for a productive and relaxed atmosphere, and also their friendship. In particular, my travel companions to different parts of the world: Andreas Axholt, Johan Wernehag, Martin Anderson, and Ellie Cijvat. Peter Sjöblom, Niklas Troedsson, Fredrik Tillman, and Peitro Andreani for all fruitful discussions. A special thanks to Roland Strandberg for sharing my interest in hunting and target shooting. I would also like to thank the people at Ericsson Research in Mölndal, particularly Harald Jacobsson, Lars Aspemyr and Mingquan Bao, for a good collaboration at the start of my Ph.D. studies.

I am very grateful for the help and support from the faculty, the technical staff, and the administration at the department. Especially, Göran Jönsson for introducing me to RF electronics during my undergraduate studies, Bertil Larsson for giving me the opportunity to lecture the Advanced Analog Electronics course, Lars Hedenstjerna for all mechanical assistance, Martin Nilsson for PCB manufacturing, Stefan Molund for CAD support, Erik Jonsson for UNIX/Linux support, and Pia Bruhn for her help with various administrative tasks. A special thanks also to Lars Olsson for proofreading this thesis.

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Markus Törmänen

List of Acronyms

ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
BB	Baseband
BCB	Benso-Cyclobutene
BEOL	Back End of Line
BER	Bit Error Rate
BSF	Band Select Filter
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CPW	Co-Planar Wave Guide
CS	Common Source
CSF	Channel Select Filter
DAC	Digital-to-Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
F	Noise Factor
FET	Field Effect Transistor
FOM	Figure of Merit
FOM_T	Figure of Merit taking tuning range into account
GaAs	Gallium Arsenide
GND	Ground
IC	Integrated Circuit
$\mathrm{ICP}_{1\mathrm{dB}}$	Input referred 1dB Compression Point
IF	Intermediate Frequency
IIP_2	Input referred Second-Order Intercept Point
IIP_3	Input referred Third-Order Intercept Point
IM	Intermodulation
IRF	Image Reject Filter

ISF	Impulse Sensitivity Function
IP_2	Second-Order Intercept Point
IP_3	Third-Order Intercept Point
IRR	Image Rejection Ratio
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LO	Local Oscillator
mHEMT	Metamorphic High Electron Mobility Transistor
MIM	Metal Insulator Metal
MMIC	Monolithic Microwave Integrated Circuit
MOS	Metal Oxide Semiconductor
NF	Noise Figure
NMOS	N-channel Metal Oxide Semiconductor
NR	Noise Ratio
NR_{tot}	The Total Noise Ratio
PA	Power Amplifier
PCB	Printed Circuit Board
PM	Phase Modulation
PMOS	P-channel Metal Oxide Semiconductor
Q	Quality factor
QAM	Quadrature Amplitude Modulation
QVCO	Quadrature Voltage Controlled Oscillator
RF	Radio Frequency
SiO_2	Silicon Dioxide
SMD	Surface Mounted Device
SoC	System on Chip
SOP	System on Package
TCR	Temperature Coefficient of Resistivity
VCO	Voltage Controlled Oscillator
V_{DD}	Supply Voltage
WLP	Wafer Level Package

List of Symbols

C_{gs}	Gate to source parasitic capacitance
C_{gd}	Gate to drain parasitic capacitance
Δf	Offset frequency
$\Delta\omega$	Angular offset frequency
ϵ	Amplitude error in an image reject architecture
f_0	Resonance frequency
f_c	Center frequency
f_{IF}	Intermediate frequency
f_{IM}	Image frequency
f_{LO}	Local oscillator frequency
f_{max}	Maximum oscillation frequency
f_{RF}	Radio frequency
f_T	Transition frequency
γ	Body effect coefficient
g_{ds}	Drain to source conductance
g_{ds0}	Drain to source conductance at $V_{DS} = 0$
G_m	Effective transconductance
g_m	Transconductance
g_{mb}	Body transconductance
I	DC current
I+	In phase positive signal
I-	In phase negative signal
λ	Wavelength
L	Transistor channel length
$\mathcal{L}\left(\Delta\omega\right)$	Phase noise at certain offset frequency
ω	Angular frequency
ω_0	Resonance angular frequency
ω_T	Angular transition frequency

θ	Phase error in an image reject architecture
$\mathrm{P_{DC}}$	DC power consumption
Q+	Quadrature phase positive signal
Q-	Quadrature phase negative signal
q_{max}	Maximum charge in the LC-VCO resonance tank
S	Number of symbols
s	complex angular frequency or Laplace transform variable
S_{ing}	Power spectral density of induced gate noise (input referred)
S_{iw}	Power spectral density of white noise (output referred)
S_{vg}	Power spectral density of input noise voltage ($1/f$ noise)
V_0	Differential peak to peak voltage of an LC-VCO resonator
W	Transistor width
Y	Admittance
Z_{in}	Input impedance

Introduction

Chapter 1

Thesis Outline

1.1 Motivation

The history of wireless communication started in the late 19th century pioneered by men like Heinrich Hertz, Alexander Popov, and Guglielmo Marconi. The technological development has since then been very rapid, specially in the last two decades of cellular communication. Today's increasing demand for higher data rates is pushing wireless communication systems to utilize more and wider bands at higher frequencies. At the same time as the performance must increase, low cost and small size implementations are necessary to be commercially successful.

The III-V technologies, e.g. GaAs, are the obvious technologies of choice for microwave applications as they offer low noise, high speed, and high breakdown voltages. However, they do not meet the low cost requirements for large scale production. Being used for virtually all digital circuits, CMOS is the dominating IC technology today, and the large volumes result in low cost. The evolution of CMOS towards even smaller and faster devices has made it a viable technology for cost sensitive radio systems operating also at microwave and millimeterwave frequencies. This has also opened the possibility to design fully integrated SoCs, where the microwave front-ends, data converters (ADC/DAC), and DSPs can be placed on the same chip. However, as the speed (f_T and f_{max}) of CMOS transistors has increased with technology scaling, the breakdown voltages have decreased, and shorter channel length devices produce more low frequency noise which imposes challenges for the designer. Even with a fast high performance CMOS technology the performance of microwave circuits is usually limited by the losses of on-chip passive components. Moving the passives from the chip to a low loss carrier can help to improve the performance, but it also requires good knowledge of the package transition parasitics.

The focus of this thesis is on the receiver front-end. Different front-ends using differential topologies, consisting of low noise amplifiers (LNAs) and mixers, have been designed in CMOS technology. The dies have been flip-chip mounted to carriers featuring low loss baluns to generate the differential signals needed by the chip. Differential and quadrature voltage controlled oscillators (VCOs) have also been designed in CMOS, where one VCO makes use of a low loss on-carrier inductor to achieve high phase noise performance. A fully integrated CMOS quadrature receiver front-end consisting of LNAs, mixers, and a QVCO is also demonstrated.

This thesis is not meant to be a text book on wireless communication nor RF electronics as very good ones exist in litterature, e.g. [1–3]. However, to put the work in this thesis into perspective, an introduction to wireless communication, receiver architectures, front-end receiver blocks, and low loss (high Q) passive components is presented in the following chapters.

1.2 Organisation of the Thesis

Chapter 1 - Thesis Outline

Starts with a motivation to the work followed by a presentation of how the thesis is organized.

Chapter 2 - Radio Receiver Architectures

Begins with a short introduction to wireless communication and the basic principles and building blocks of a modern radio transceiver. The heterodyne, image reject, and direct conversion receiver architectures are described.

Chapter 3 - Receiver Front-end Considerations

The different blocks of the radio receiver front-end are treated here. Differential topologies of CMOS VCOs, low-loise amplifiers and mixers are treated, as well as the effect on the received information caused by their imperfections.

Chapter 4 - System-on-Package Technology

This chapter describes passive microwave components. As the Q-value for on-chip passives is quite limited it can be benefitial to move them off-chip. Postprocessed inductors are also discussed. Finally, VCOs and front-ends using carrier integrated passives are demonstrated with a few examples.

Chapter 5 - Discussion and Future Work

This chapter discusses the research results and suggests some ideas for future improvements and work with carrier technology.

Included Papers

Microwave front-ends and VCOs are demonstrated in the included papers with some designs using System-on-Package (SOP) technology. All of the circuits in the included papers have been designed, fabricated, and measured.

Papers II, III, and VI demonstrate the capability of fully integrated CMOS circuit designs. An LC-VCO using an accumulation mode varactor is presented in Paper II, a QVCO using 4-bit switched tuning is shown in Paper III, and a quadrature receiver front-end (including QVCO) is demonstrated in paper VI.

Papers I and IV demonstrate SOP receiver front-ends using low loss baluns on carrier for the LO and RF signals. Paper IV also includes a front-end using single-ended RF input, which is converted to differential form in a novel on-chip merged LNA and balun. A SOP VCO demonstrating the benefits of a high Q inductor on carrier is presented in Paper V, where the VCO achieves a 20% tuning range at 24GHz with excellent phase noise performance.

Chapter 2

Radio Receiver Architectures

This chapter presents a brief introduction to wireless communication and the most common radio receiver architectures used today. Some advantages and drawbacks of the different receiver architectures are also discussed.

2.1 Wireless Communication

A basic system for wireless communication is illustrated in Figure 1. It consists of a transmitter, a communication channel, and a receiver. In the transmitter the information to be sent is modulated on a radio frequency (RF) carrier and amplified by a power amplifier (PA) before it is transmitted through the antenna. In the communication channel the signal gets attenuated and subjected to noise and interference. To be able to receive the attenuated signal it is amplified in the receiver front-end, where it is also downconverted to a lower frequency, called intermediate frequency (IF). After reducing interference by filtering, the signal can finally be demodulated. The demodulator is often digital, consisting of an analog to digital converter (ADC) and a digital signal processer (DSP). In order for the demodulator to detect the transmitted information correctly, the front-end must cope with the impaired signal from the channel and convert it to a signal that fits the demodulator. In a digital system, the bandwitdh the system must handle is proportional to the baseband (BB) signal bitrate. With an increasing demand on high data rates, wireless communication systems are therefore pushed to use more and wider frequency bands, which are available at higher frequencies. More details on wireless communication can be found in e.g. [1].

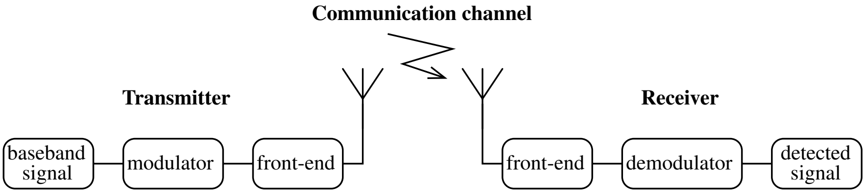

Figure 1: An illustration of radio transmission

2.2 Receiver Achitectures

The task of the receiver front-end is to supply the input of the demodulator, normally the ADC, with an amplified, frequency downconverted and filtered signal from which the transmitted information can be detected. The downconversion is achieved by multiplying the RF signal with a local oscillator (LO) signal in the mixer, which results in first order output signals located at the sum and difference frequencies. The difference frequency, or intermediate frequency (IF), $f_{IF} = |f_{RF} - f_{LO}|$, becomes a new carrier of the downconverted received RF signal. One problem is that an interferer located at the image frequency will also be downconverted to the same IF. For high-side injection ($f_{LO} > f_{RF}$) the image frequency will be located at $f_{IM} = f_{RF} + 2 \cdot f_{IF}$, and for low-side injection ($f_{LO} < f_{RF}$) at $f_{IM} = f_{RF} - 2 \cdot f_{IF}$. This image signal problem has to be dealt with in the receiver.

The three most common receiver architectures are presented briefly in the the following sections; the heterodyne receiver, the image reject receiver, and the direct conversion/homodyne receiver. The main difference between these architectures is the way the image signal is handled. A more detailed description of receiver achitectures can be found in e.g. [2, 3].

2.2.1 The Heterodyne Receiver

The heterodyne receiver architecture [4] is shown in Figure 2. Like all the receiver architectures presented here, it has a band select filter (BSF) that attenuates interferers outside the received band. The BSF precedes the low noise amplifier (LNA), where the RF signal is amplified before it is filtered by the image reject filter (IRF). The RF signal is then downconverted to an IF in the mixer by multiplying with a local oscillator (LO) signal. Due to the image frequency problem described above the IRF has to be placed before the mixer, because after the mixer an interferer at the image frequency can not be separeted from the downconverted RF signal as they will both be at the same IF. The purpose of the channel select filter (CSF) is to then filter out the channel to be demodulated.

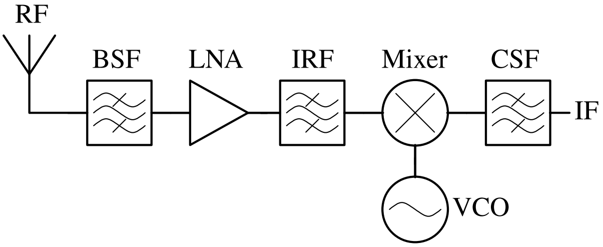

Figure 2: The heterodyne receiver architecture

A trade-off, again due to the image problem, has to made in choosing the IF. The

CSF is a bandpassfilter at the IF, with a Q value proportional to the IF. Thus the lower the IF, the better for the CSF. However, the IF must be chosen larger than half the width of the received band, since otherwise the image signal will be in-band and can not be filtered out. Furthermore, if the minimum IF is chosen (equal to half the width of the received band), the IRF filter has to be very sharp (have high order). Thus, a higher IF has to be chosen, and a compromise has to be made between the IRF and the IF blocks (CSF, amplification, and detector). Due to the stringent filtering required, the filters are usually not possible to implement on-chip, and they are thus quite costly.

A possibility to relax the requirements on the different blocks is to perform the downconversion in two steps. This type of architecture is usually referred to as the double-conversion heterodyne receiver. However, with two IFs the receiver complexity and cost increases as another filter, mixer, and LO signal is needed.

2.2.2 The Image Reject Receiver

The image reject receiver architecture allows the image to be inside the band. This enables a low IF to be used, reducing the requirement for a high Q in the IF filter. The principle of image rejection is to first employ complex downconversion by mixers fed by quadrature LO signals. The down-converted IF outputs from the two mixers are then phase shifted and added. The image signals will then cancel whereas the wanted IF signals from the two branches add in phase.

Two common architectures, the Hartley (1928) [5] and the Weaver (1956) [6], are shown in Figures 3 and 4, respectively. A 90° phase shift is introduced in one of the branches of the Hartley receiver, while the Weaver structure instead utilizes a double complex downconversion.

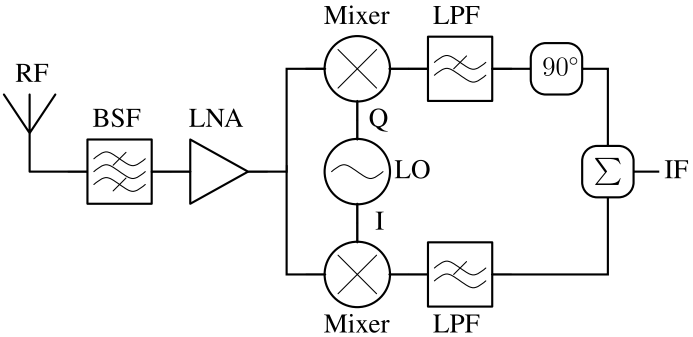

Figure 3: The hartley image reject receiver architecture

Both phase and amplitude mismatch result in reduced image rejection, thus it is important that the two branches are well matched and that the LO signal has a good quadrature accuracy. An equation for the image rejection ratio (IRR) is derived in [2]

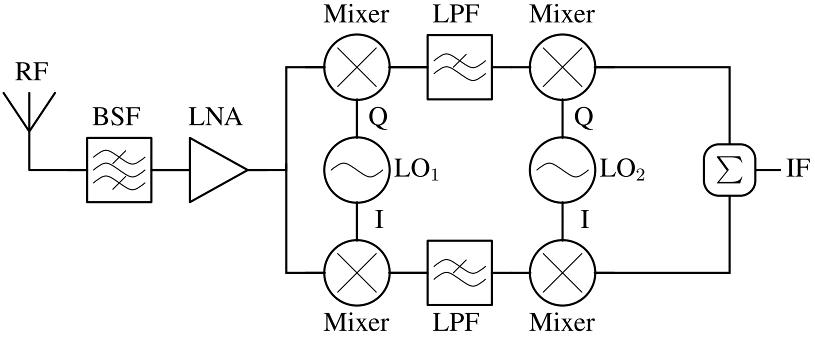

Figure 4: The weaver image reject receiver architecture

and shown in (1),

$$IRR = \frac{1 + 2\left(1+\epsilon\right)\cos\left(\theta\right) + \left(1+\epsilon\right)^2}{1 - 2\left(1+\epsilon\right)\cos\left(\theta\right) + \left(1+\epsilon\right)^2} \approx \left.\frac{4}{\epsilon^2+\theta^2}\right|_{\text{small } \epsilon \text{ and } \theta} \tag{1}$$

where ϵ is the relative amplitude (gain) mismatch and θ the phase imbalance (in radians).

If the I and Q branches are kept separated in the front-end, the image rejection (phase shift and addition) can also be performed in the digital baseband.

2.2.3 The Direct Conversion / Homodyne Receiver

The direct conversion or homodyne receiver [7], sometimes also referred to as the zero-IF receiver, presents yet another way to deal with the image signal problem, see Figure 5. This is accomplished by choosing the LO signal frequency equal to that of

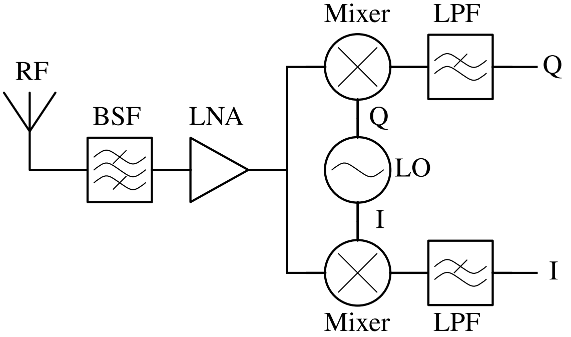

Figure 5: The homodyne receiver architecture

the RF signal, setting the IF equal to zero (DC) and thus making the signal to receive its own image. The channel select filtering becomes easier as the mixer outputs just have to be low pass filtered before the demodulator. Since the image signal is never stronger than the signal to receive, the mismatch of the I and Q branches is not as critical as in the image reject receiver. The drawback, however, is that since the signal after down-conversion is centered at DC, the architecture is sensitive to flicker noise ($1/f$ noise) and DC-offsets. Low frequency disturbance can also be caused by interfering signals through even order non-linearities and self-mixing. The requirements on the second order non-linearity of the mixer are therefore very stringent in homodyne receivers. As the gain is typically quite high before the ADC in the demodulator, even small DC-offsets can saturate the ADC input or the amplifiers preceeding it.

Chapter 3

Receiver Front-end Considerations

The receiver front-end is the first part of the radio receiver. It receives the high frequency signal from the antenna. The front-end's purpose is to amplify, frequency down-convert, and filter the signal while adding as little noise and other impairments as possible to the signal, so that the transmitted information can be retrieved by the succeeding stages. CMOS voltage controlled oscillators (VCOs), low-noise amplifiers (LNAs), and mixers are briefly treated in this chapter, as well as the effects on the received information caused by their imperfections. A more comprehensive treatment can be found in e.g. [2] or [3].

3.1 CMOS Oscillators

Oscillators are circuits that generate an output signal at a certain frequency with a DC power supply as the only source. The frequency can be controlled typically by a voltage, making the oscillator a voltage controlled oscillator (VCO). The output signal is usually used as a local oscillator (LO) signal in mixers to produce a downconverted intermediate frequency (IF) signal from the input radio frequency (RF) signal.

Generally oscillators can be divided into two types, relaxation and harmonic (tuned) oscillators. The relaxation oscillators, e.g. Schmitt trigger using positive feedback and ring oscillators, can be used to produce different periodic waveforms. They do not use large on-chip inductors and are thereby small in size, but unfortunately they are not suitable for RF applications requiring low phase noise. Harmonic oscillators, e.g. differential LC, Clapp, Colpitts, Hartley, and Pierce oscillators have better phase noise performance and sinusoidal output waveform due to the filtering provided by the resonator, and they are suitable for RF applications. The oscillator designs included in this thesis are based on the differential LC oscillator topology, which is the topology covered briefly in the following sections.

3.1.1 Differential LC oscillator

The differential LC oscillator is depicted in Figure 6. The cross-coupled transistors provide a negative resistance to overcome the losses in the resonator composed of the varactor and inductor. A stable oscillation is reached when the integrated losses over one cycle in the resonator are exactly compensated for by the energy supplied by the negative resistance of the differential pair. In theory [3], a minimum net startup loop gain of one is required for the oscillator to start. However, in practice the loop gain must be chosen a few times larger than one to ensure startup, since the gain of the differential pair will be compressed at large signal levels. If the startup loop gain is not sufficiently large, full oscillation amplitude will therefore not be reached. This would result in degraded phase noise and potentially reduced mixer performance due to insufficient LO amplitude. Fortunately, startup loop gain is rarely a problem in the CMOS differential oscillator, where the output signal is connected directly to the transistor gate terminals.

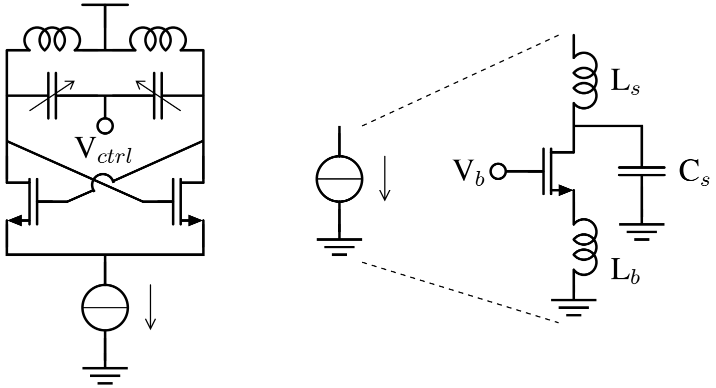

Figure 6: Differential LC oscillator

By using a first order model of the differential pair, it can be shown that the differential admittance provided by the transistors is as shown in (2).

$$Y = \frac{1}{2}\left(-g_m + sC_{gs} + 4sC_{gd}\right) \tag{2}$$

MOS Varactor

The frequency tuning of the oscillator can be accomplished by changing either the inductance or the capacitance of the resonator, as the resonance angular frequency is given by $\omega_0 = \frac{1}{\sqrt{LC}}$. Typically, the capacitance is made tunable. The variable capacitor, called varactor, is often realized as an MOS varactor using either NMOS or PMOS transistors. With the drain and source terminals connected together, and the bulk terminal at GND (NMOS) or V$_{DD}$ (PMOS), the tunable capacitance is achieved through the potential difference between the gate and drain-source terminals. The tuning range is similar for both NMOS and PMOS varactors, but the parasitic resistance is lower for the NMOS device, although it can be more sensitive to substrate-induced noise due to the lack of a separate p-well. This type of devices is often referred to as inversion-mode varactors, since they operate in the inversion (and depletion) region of the MOS transistor.

Another common MOS varactor is the accumulation-mode varactor [8], which operates in the accumulation and depletion regions. Based on the PMOS transistor, with the p^+ doped diffusions of the drain and source replaced by n^+ well contacts, the accumulation-mode varactor offers a low series resistance.

An important parameter for the varactor is the Q-factor, where the MOS varactors typically offer higher quality factors than reverse biased PN junction based varactors. Since the losses are dominated by the series resistance, the quality factor is inversely proportional to the frequency, $Q = 1/\left(\omega_0 CR\right)$. The use of minimum channel length devices maximizes the Q since the channel resistance is then minimized. Short fingers are then necessary to reduce the series gate resistance. However, due to bias independent gate-source and gate-drain overlap capacitances, the maximum to minimum capacitance ratio (C_{max}/C_{min}) is reduced for short channel lengths. A C_{max}/C_{min} ratio of about 3 can be achieved typically by MOS varactors. The Q-factor improves with technology scaling, but at the same time the C_{max}/C_{min} ratio decreases due to parasitic overlap capacitances.

The non-linearity of the varactor is also a problem, because amplitude noise can be converted into phase noise by the varactor [9]. The MOS varactors, with their step-like characteristics, have strong non-linearities. The larger the tuning range and varactor gain, the larger the AM to PM noise conversion. To reduce this effect, a smaller continuously tuned varactor combined with fixed (linear) capacitors that can be switched in and out or the resonator can be used [10]. The small varactor then only has to be large enough to ensure continuous frequency coverage between the different states where different capacitors are switched in.

Source Node Filtering

Noise from several harmonics and DC ($1/f$) contribute to the oscillator phase noise around ω_0, which is further discussed in section 3.1.2. To improve the phase noise performance a possible implementation of the tail current source is also shown in Figure 6. This source node filtering technique is composed of the source node inductor L_s, capacitor C_s, and the FET [11]. The tail current source should have high impedance at $2\omega_0$, thus inductor L_s is to resonate the parasitics of the source node at $2\omega_0$, and capacitor C_s shorts the high frequency noise from the FET to ground. The FET can be used to control the VCO to be in the current-limited region or the voltage-limited region. Usually the best performance is achieved if the VCO is operating in the current limited region, on the border of being in the voltage limited region [12]. This maximizes both the resonator energy and the power efficiency.

The filtering technique described above prevents tail current noise at $2\omega_0$ from creating phase noise, but low frequency tail current noise can cause amplitude noise which is converted to phase noise by the nonlinearities of the varactor. In [13], a large off-chip inductor (L_b in Figure 6) is used to suppress also the low frequency $1/f$ noise.

Noise in the MOS transistor

The different noise sources in the MOS transistor determine the achievable noise performance of the front-end. The main sources of noise in the MOS transistor are: thermal channel noise, $1/f$ noise, gate-induced noise, and noise from parasitic resistances. The thermal noise has a white power spectral density (S_{iw}) and is due to random thermal movement of electrons and holes in the channel.

The low frequency $1/f$ noise (flicker noise) is the dominating noise source at low frequencies. The origin of the noise is still discussed and different theories exist: random fluctuation of the number of charges in the channel due to the trapping and releasing of charges in the Si-Si0$_2$ interface [14], and variations in phonon scattering resulting in mobility variations over time [15]. The equivalent gate voltage spectral density is $S_{vg}\left(f\right) \sim 1/\left(WLf\right)$, where it can be seen that the transistor width (W) and length (L) have a large impact on the $1/f$ noise.

The gate-induced current noise is due to the capacitive coupling of random potential variations in the channel [16], $S_{ing} \sim \left(\omega C_{gs}\right)^2$. The gate-induced current noise increases with the square of frequency, but is typically not a concern in oscillators, even if they operate at high frequencies. In the very common inductively source-degenerated low noise amplifier, on the other hand, this noise is often dominant [17].

A more comprehensive treatment of the MOS transistor and the noise sources in the transistors different regions of operation can be found in e.g. [18].

3.1.2 Phase Noise

In 1966 Leeson presented an empirical phase noise model [19]. The model covers three regions of the phase noise spectrum; $1/f^3$, $1/f^2$, and the thermal noise floor, as illustrated in Figure 7. According to Leeson the phase noise of an oscillator can be modelled by (3),

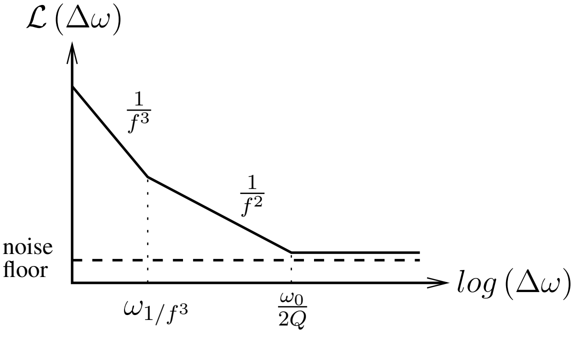

Figure 7: Phase noise versus offset frequency on a log-log axis

$$\mathcal{L}\left(\Delta\omega\right) = 10\,log_{10}\left\{\frac{2FkT}{P_s}\cdot\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \tag{3}$$

where P_s is signal power in the resonance tank, ω_0 the angular resonance frequency (carrier), $\Delta\omega$ the angular frequency offset from the carrier, k the Boltzmann constant, and T the temperature in Kelvin. At a given offset frequency the phase noise can be improved by increasing the carrier power in the resonator or the resonator Q value, which appears squared in the model. Another important parameter is the circuit dependent noise factor, F, which is always larger than 1. For the LC oscillator topology in Figure 6, with the ideal current source replaced by an NMOS transistor, an expression for the noise factor (4) was found by Rael [20],

$$F = 1 + \frac{4\gamma RI}{\pi V_0} + \gamma\frac{4}{9}g_{m,cs}R \tag{4}$$

where V_0 is the differential peak to peak voltage in the resonator, $g_{m,cs}$ the current source transconductance, I the DC current, R the parallel resistance of the resonator at resonance, and γ the transistor channel noise factor which is bias dependent and varies over the oscillation cycle [21]. If we assume that the resonator in Figure 6 is fed with an ideal square wave from the differential pair ($V_0 = \frac{4}{\pi}RI$) and assume an ideal noiseless current source, equation (4) simplifies to:

$$F = 1 + \gamma \tag{5}$$

which is the minimum noise factor for the differential LC oscillator.

In 1998, Hajimiri presented a phase noise formula based on the impulse sensitivity function (ISF) [22]. The ISF, Γ, is a dimensionless, frequency- and amplitude-independent periodic function which describes the sensitivity of the oscillator phase to a unit impulse. Hajimiris phase noise formula is shown is (6)-(7) where the $1/f$ noise is neglected and white noise is assumed.

$$\mathcal{L}\left(\Delta\omega\right) = 10\,log_{10}\left(\frac{\frac{\overline{\mathsf{i}_n^2}}{\Delta f}\sum_{n=0}^{\infty}\mathsf{c}_n^2}{4\mathsf{q}_{max}^2\Delta\omega^2}\right) \tag{6}$$

$$\sum_{n=0}^{\infty}\mathsf{c}_n^2 = \frac{1}{\pi}\int_0^{2\pi}|\Gamma\left(x\right)|^2dx = 2\mathsf{\Gamma}_{rms}^2 \tag{7}$$

The coefficients c_n are real valued coefficients for the different harmonics and q_{max} is the charge of the resonance tank. Combining (6) and (7) yields (8), which represents the phase noise spectrum of an arbitrary oscillator in $1/f^2$ region [22].

$$\mathcal{L}\left(\Delta\omega\right) = 10\,log_{10}\left(\frac{\mathsf{\Gamma}_{rms}^2}{\mathsf{q}_{max}^2}\cdot\frac{\overline{\mathsf{i}_n^2}/\Delta f}{2\Delta\omega^2}\right) \tag{8}$$

3.1.3 Figures of Merit

The performance of oscillators can be compared by calculating the figure of merit (FOM) [23], which describes the phase noise performance versus power consumption as shown in (9),

$$\text{FOM} = 10\, log_{10}\left(\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{10^{\frac{\mathcal{L}(\Delta\omega)}{10}}P}\right) \tag{9}$$

where P is the power consumption of the oscillator in mW. In order also to take the tuning range of the oscillator into account, the expression (9) can be modified to (10), [24].

$$\text{FOM}_T = 10\, log_{10}\left(\left(\frac{\omega_0 \cdot tuning\,(\%)}{10 \cdot \Delta\omega}\right)^2 \frac{1}{10^{\frac{\mathcal{L}(\Delta\omega)}{10}}P}\right) \tag{10}$$

3.1.4 Survey of Oscillators

The advances in CMOS processing during the last decade has improved the performance of RF ciruits in general, and ocillators in particular. A brief overview of some differential and quadrature oscillators at microwave frequencies will be given in this section. However, more state-of-the-art designs exist than are cited here.

Technology scaling has improved the perfomance of VCOs operating at higher frequencies mainly by improvements in f_T and f_{max} resulting in higher transistor switching speed. Thick interconnects also make it possible to design high Q on-chip inductors and baluns, thus the varactors are usually the limiting factor for phase noise performance at microwave frequencies. Some microwave CMOS oscillators achieving a high phase noise figure of merit (FOM) are published in: (186dB) [25], (190dB) [26], and (199dB) [27]. The oscillator in [27] is fabricated in a 90nm CMOS process, but it is also postprocessed using a high-Q inductor on top of insulating Benso-Cyclobutene (BCB) material, which minimizes the substrate losses. A CMOS LC-VCO, using an accumulation mode varactor, achieving a FOM between 185-188dB is demonstrated in Paper II. In Paper V a 24GHz LC-VCO, using a high Q glass carrier inductor and two cascaded frequency doublers, achieves a wide 20% tuning range combined with a FOM of 191dB.

Modern radio receivers with direct conversion or low-IF architectures require quadrature LO signals. The quadrature LO generation can be done in a number of different ways: one is to use quadrature voltage controlled oscillators (QVCOs). The original QVCO topology proposed in [28] is shown in Figure 8(a). The two LC-VCO cores are locked to oscillate in quadrature through coupling transistors in parallell with the switch transistors. This topology is commonly referred to as the P-QVCO. In Figure 8(b) the two LC-VCOs are locked to oscillate in quadrature through the source node coupling capacitor C$_c$, [29]. Another common QVCO topology is the series coupled QVCO, S-QVCO, which was proposed in [30]. The S-QVCO topology has the coupling transistors stacked in series with the switch transistors, with their gates

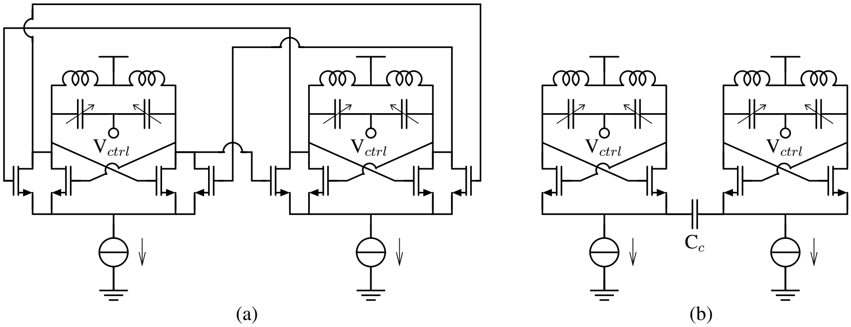

Figure 8: (a) The original QVCO. (b) QVCO coupled to oscillate in quadrature by means of C$_c$

connected to the other LC resonance tank. Other LC-QVCO topologies have also been proposed, however, they are similar to those described since they are all based on the idea of injection locking two LC-VCOs to operate in quadrature. The quadrature signal generation can also be performed by converting the differential output signal from a VCO to a quadrature signal with a passive or active polyphase filter [31–33]. This approach typically occupies less area than a QVCO, but the passive polyphase filter attenuates the signal and may require buffer amplifiers, whereas the active polyphase filter can have a high power consumption. Another approach is to feed the differential VCO output signal to a frequency divider, obtaining a quadrature signal at half the VCO frequency. The double frequency VCO and divider occupy much less area than a QVCO, however, the frequency divider can have a substantial power consumption and be very difficult to realize at microwave frequencies.

QVCOs based on the topologies in Figure 8(a) and (b) are demonstrated in Papers III and VI, respectively.

3.2 LNAs & Mixers

In the receiver front end the signal from the antenna is first passed through a band select filter (BSF) before entering the low noise amplifier (LNA). The purpose of the BSF is to attenuate out-of-band interferers. In-band interference, however, will not be suppressed, and the LNA must thus be able to amplify weak signals in presence of strong in-band interferers. It has to provide sufficient amplification to overcome the noise of subsequent stages, while itself adding as little noise as possible. To meet the requirements of the preceeding filter, the LNA also has to provide a resistive input impedance, often 50Ω. The purpose of the mixer is to frequency downconvert the signal, since at lower frequency it is easier to implement gain, filtering and demodulation. Like the low noise amplifier, the mixer should have a low noise and high linearity. Since the signal is amplified by the LNA before reaching the mixer, the linearity is generally most critical in the mixer.

3.2.1 The CS & CG LNAs

This section describes the common-source (CS) and common-gate (CG) low noise amplifiers. The amplifiers described here use differential topologies, since these are used in the front-ends of the included papers. In general, differential topologies are known to have better linearity and stability than their single-ended counterparts, at the expense of higher power consumption, chip area, and possible need for baluns.

The CS LNA

A differential CS amplifier is shown in Figure 9. The CS amplifier is the topology that provides the best noise performance at frequencies well below the transit frequency, ω_T. The input forms a series resonance circuit composed of L_g, L_s, and C_{gs}. At resonance the input impedance is resistive, given by (11).

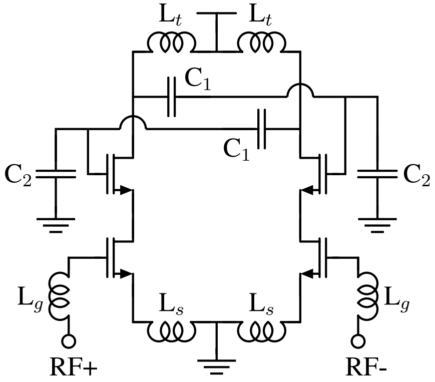

Figure 9: Differential CS LNA using capacitive cross coupling

$$Z_{in,res} = \frac{g_m}{\mathrm{C}_{gs}}\,\mathrm{L}_s = \omega_T \mathrm{L}_s \tag{11}$$

As can be seen the input impedance is proportional to the source inductance L_s. Impedance match can thereby be achieved by choosing L_s properly. The gate inductance L_g is then chosen to resonate with L_s and C_{gs} at the operating frequency ω_0 according to (12).

$$\mathrm{L}_g = \frac{1}{\omega_0^2 \mathrm{C}_{gs}} - \mathrm{L}_s \tag{12}$$

If the Q factor of the input series resonance circuit (13) is high the input is quite narrow band. A high Q will also make the voltage gain Q times higher compared to the CG amplifier and result in reduced input referred thermal noise from the transistor. Unfortuanately it will also degrade the linearity, increase the sensitivity to the input matching, and increase the input referred gate induced noise.

$$Q = \frac{1}{2R_s \omega_0 \mathrm{C}_{gs}} \tag{13}$$

The minimum noise factor for an impedance matched CS LNA is given in (14),

$$F_{min,CS} = 1 + \frac{2\omega_0}{\sqrt{5}\omega_T} \sqrt{\gamma\, \delta\, (1 - |c|^2)} \tag{14}$$

where the parameters for a long channel device are typically: γ equal to 2/3, δ equal to 4/3, and the correlation coefficient for drain and gate induced noise $|c|$ equal to 0.395, [34]. For short channel devices, the parameters for γ [35] and δ [18] can be considerably larger. The noise factor of a source degenerated CS amplifier was also studied in [17]. The expression derived for F_{min}, with a given Q for the series input resonance circuit, is shown in (15). Note that in this work an additional lossless capacitor is inserted between the gate and source. This reduces the contribution of the gate-induced noise, however, at the cost of reduced gain, which makes this technique less attractive at microwave frequencies.

$$F_{min,CS} \approx 1 + \frac{1}{Q} \cdot 4\beta'^{1/4} \left(\frac{\gamma'}{12}\right)^{3/4} \sqrt{\frac{2\omega_0}{3\mu'_{eff} R_s I_{ds}} L} \tag{15}$$

In (15), β' represents the gate induced noise factor, γ' the channel current noise factor, R_s the generator resistance, and L the channel length of the transistor [17].

The effective transconductance for an impedance matched, source inductor degenerated, CS amplifier is given in (16) [3]. As can be seen in the equation a high effective transconductance requires a high ω_T/ω_0 ratio. The transit frequency, and thus the effective transconductance, will improve with technology scaling. This will result in improved high frequency gain.

$$G_{m,CS} = \frac{1}{2R_s} \cdot \frac{g_m}{\mathrm{C}_{gs} \omega_0} = \frac{1}{2R_s} \cdot \frac{\omega_T}{\omega_0} \tag{16}$$

The CS input transistor can be stacked with a cascode CG transistor as shown in Figure 9. The CG transistor increases the isolation between the input and output of the LNA, which results in improved stability and reduced LO leakage. Unfortunately, at microwave frequencies short channel length transistors must be used for high frequency performance, resulting in poor isolation due to an increased drain-source conductance (g_{ds}). Also shown in Figure 9 is a capacitive cross coupling technique using capacitors C$_1$ and C$_2$. This capacitive cross-coupling is used to increase the differential isolation by cancelling the currents due to the drain-source conductance for differential signals. By using the simplified small signal schematic in Figure 10 it can be shown that cancellation is achieved when the capacitance ratio C$_2$/C$_1$ is equal to the cascode transistor intrinsic gain minus one (17).

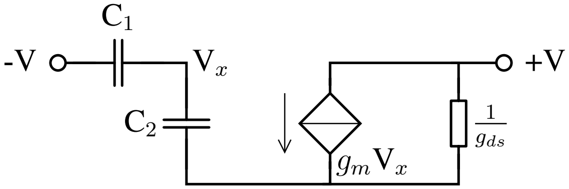

Figure 10: Small signal schematic illustrating capacitive cross coupling

$$\frac{\mathrm{C}_2}{\mathrm{C}_1} = \frac{g_m}{g_{ds}} - 1 \tag{17}$$

There are also some drawbacks with the cascode transistor. It reduces the voltage headroom and adds noise. With increasing frequency the impedance of the node between the CS and CG transistors drops due to parasitic capacitance, which makes the topology more sensitive to noise from the cascode transistor. However, the parasitic capacitance can be minimized by a layout where the CS transistor drain and CG transistor source junctions are shared [36]. The result is a 'double-gate' device with low parasitic capacitance. The topogy in Figure 9, utilizing a 'double-gate' device, is used in the front-end of Paper I.

The CG LNA

The CG amplifier provides a more broadband input matching. A single CG transistor amplifier has a resistive input impedance that equals $1/(g_m + g_{mb}) \approx 1/g_m$ (neglecting the load resistance) when the parasitic capacitance at the source node is resonated by an inductor. The input becomes quite broadband since the Q of the input is fairly low, the parallel resonance circuit being loaded by the input resistance, $1/g_m$. A common-gate amplifier has a minimum noise factor given by (18) [3],

$$F_{min} = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{g_m R_s} = 1 + \frac{\gamma}{\alpha} \tag{18}$$

where input impedance matching is assumed and α is equal to g_m/g_{ds0}, with g_{ds0} being the drain-source conductance at $V_{DS} = 0$. For long channel devices α is equal to one, but it is reduced for short channel devices [18].

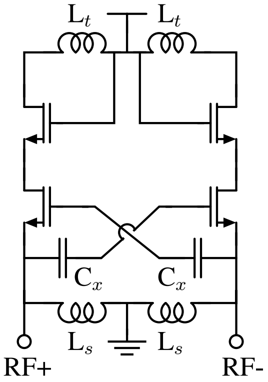

Figure 11: Differential CG LNA using capacitive cross coupling

A differential CG amplifier is shown in Figure 11, where a differential source node inductor is used to resonate the input parasitics. A capacitive cross-coupling technique using capacitors C_x is also employed, where capacitors C_x are larger than C_{gs}. The capacitive cross-coupling has many benefits as it improves the gain and noise performance of the CG amplifier [37, 38]. The effective transconductance is doubled (19), and the noise from the input transistors can thereby be reduced (20). The effective input impedance at resonance is given by (21) [38].

$$G_{m,CG} = 2g_m \tag{19}$$

$$F_{min,CG} = 1 + \frac{\gamma}{2\alpha} \tag{20}$$

$$Z_{in,CG,res} = \frac{1}{2g_m} \tag{21}$$

The expression for the noise factor (20) assumes that the input impedance is matched to the source impedance for maximum power transfer. However, if some mismatch can be accepted, a lower noise factor can be obtained by increasing g_m . This was demonstrated in [39], where a noise figure reduction of 1.4dB was achieved by accepting an S_{11} of -12dB.

The differential CG LNA of Figure 11, also using the capacitive cross-coupling of Figure 9 at the output for increased differential isolation, is demonstrated in the front-ends of Papers IV and VI. The front-end in Paper IV also presents a novel merged LNA and balun using a CG input stage.

3.2.2 The Gilbert Cell & Passive Mixers

The purpose of the mixer in a receiver front-end is to downconvert the RF signal to a lower frequency, where it is easier to apply amplification, filtering and detection. Transistor based mixers dominate in integrated circuits thanks to their high performance. In this section the double-balanced active Gilbert and passive mixers, both MOS transistor based, are briefly treated. The term double-balanced means that the RF, LO, and IF signals are all differential. The undesired LO signal component is then cancelled at the IF output thanks to mixer symmetry.

Gilbert mixer

The double-balanced active Gilbert mixer is depicted in Figure 12. The RF input voltage is first converted to an RF signal current by the input transistors. The mixing action is then achieved by switching the RF current so that it is connected either straight or cross-coupled to the differential load.

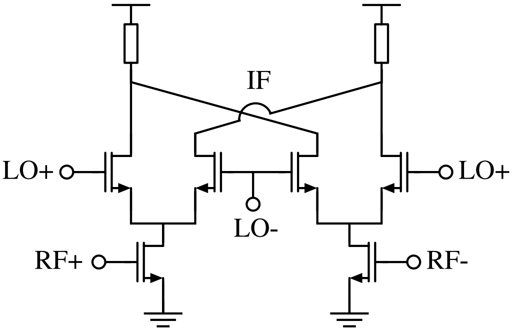

Figure 12: Double-balanced Gilbert mixer

By assuming that the LO-driven transistors behave as perfect switches, the differential output current can be regarded as the multiplication of the current from the transconductor with a unit amplitude square wave at the LO frequency. From a Fourier expansion the fundamental tone amplitude of the square wave can be found and the conversion transconductance calculated (22) [3].

$$G_{conv} = \frac{2}{\pi} g_m \tag{22}$$

The Gilbert mixer is active and therefore it can provide power gain. The drawback is that it consumes DC power, and that it generates $1/f$ noise. The $1/f$ noise is particularly harmful in homodyne receivers, and is generated mainly by the random modulation of the conduction angle of the switches (the time instants of mixer switching) [40]. Other important noise sources are the channel thermal noise of the transistors, and noise of the load itself. The switch transistors produce most noise during switching, when all switches are on simultaneously. A larger LO amplitude shortens the switching time, and thereby reduces the noise. It is difficult to calculate the noise figure of mixers by hand due to the large signal operation involved, so special methods have been developed e.g. [41]. The linearity is also difficult to predict by hand, but it is investigated in [42] by treating the mixer as a periodically time-varying weakly nonlinear circuit.

Passive mixer

The passive double-balanced mixer is shown in Figure 13. Contrary to the current mixing used by the Gilbert mixer, voltage mixing is performed by the passive mixer. Note, however, that by using a low impedance IF load also the passive mixer can be operated in the current mode.

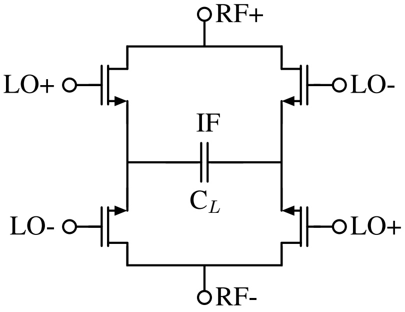

Figure 13: Double-balanced passive mixer

The on-chip load is usually capacitive and the conversion gain (loss) is dependent on the wave form of the LO signal. For a square wave LO signal the conversion gain is given by (23), whereas the voltage gain is higher for a sinusoidal LO drive (24) [3].

$$A_{cv,sq} = \frac{2}{\pi} \tag{23}$$

$$A_{cv,sin} = \frac{\pi}{4} \tag{24}$$

The on-resistance of the switches occurs in series with the load. A certain transistor width is therefore required to meet the noise requirements. Both the noise figure and linearity (IP3) depend on the width of the switches and the LO drive, since the on-resistance must be low and constant [3]. A bootstrapping technique to improve the linearity by making the on-resistance less signal dependent is proposed in [43]. A detailed analysis of the passive mixer is found in [44].

Compared to the Gilbert mixer the passive mixer has better linearity, does not consume DC power, and has no $1/f$ noise. However, the passive mixer does not provide power conversion gain. The choice of which type of mixer to use for a receiver depends on the system requirements. In the front-end designs of Papers I, IV, and VI, low $1/f$ noise was of high importance, therefore a passive mixer topology was used.

3.3 Front-end imperfections

As described earlier the main performance parameters of the front-end are those related to the gain, noise figure, and linearity. The power consumption is, of course, also a very important parameter, especially for battery operated devices. The following sections describe how the front-end noise figure and linearity can be calculated, and which blocks of the front-end have most influence on different performance parameters.

3.3.1 Noise Figure

Noise limits the sensitivity of the receiver front-end, which can be defined as the minimum input signal amplitude required to produce an output signal with the minimum signal-to-noise ratio needed to detect the transmitted information. The noise ratio or noise factor for any system can be described according to (25),

$$NR = \frac{(S/N)_i}{(S/N)_o} \tag{25}$$

where the (S/N)$_i$ and (S/N)$_o$ is the signal-to-noise ratio measured at the input and output, respectively. In [45] Friis presented a formula (26) to calculate the total noise factor for a system consisting of n cascaded blocks,

$$NR_{tot} = NR_1 + \frac{NR_2 - 1}{A_{p,1}} + \frac{NR_3 - 1}{A_{p,1}A_{p,2}} + \cdots + \frac{NR_n - 1}{A_{p,1}A_{p,2}\cdots A_{p,n-1}} \tag{26}$$

where NR_x and $A_{p,x}$ represent the noise factor and available power gain of block x, numbered from the antenna, respectively. As can be seen in (26), a high front-end noise performance requires a high gain and low noise in the first block, the LNA. If the LNA gain is high, noise from subsequent stages will have less influence, and NR_{tot} is dominated by the noise from the LNA. The noise figure (NF) is the decibel equivalent of the noise ratio, $NF = 10\,log\,(NR)$ [46].

3.3.2 Linearity

The linearity of RF front-ends is measured for intermodulation (IM) distorsion, rather than harmonic distorsion like in audio amplifiers, due to the rather low bandwidth to carrier frequency ratio of typical receiver front-ends. The linearity of the front-end puts a limit to how strong in-band interferers can be handled. For differential topologies the distorsion is usually dominated by the third-order IM product. Other odd-order IM producs also exist but third order typically dominates. Two tones at the input with frequencies f_1 and f_2 can produce downconverted third-order IM products in the wanted frequency band at the output with frequencies $f_{LO} - (2f_2 - f_1)$ and $f_{LO} - (2f_1 - f_2)$. The third-order IM products can be plotted in the intercept diagram of Figure 14. The figure shows the power at the output of the first-order (linear) outputs and of the third-order IM product. They are shown on a logarithmic scale versus input power. The 1dB compression point, usually called $\mathrm{ICP_{1dB}}$ when referred to the input, is defined when the first order output power (at $f_{LO} - f_1$ and $f_{LO} - f_2$) deviates by 1dB from the ideal (linear) extrapolated line. The third-order intercept point is defined as where the two extrapolated lines from the first-order output and third-order IM product cross. The input referred third-order intercept point $\mathrm{IIP_3}$ is also shown in Figure 14. Even-order IM products also exist. Typically they cause disturbancies at or near DC due to rectification of amplitude modulated interferers, which is a major concern in direct conversion receivers. Fortunately even-order nonlinearities can be kept small by the use of differential (balanced) topologies, where the $\mathrm{IP_2}$ is usually limited by mismatch between differential paths. To calculate the linearity requirements it is necessary to know what worst case scenarios must be handled, that is what sensitivity level must be maintained for different interference.

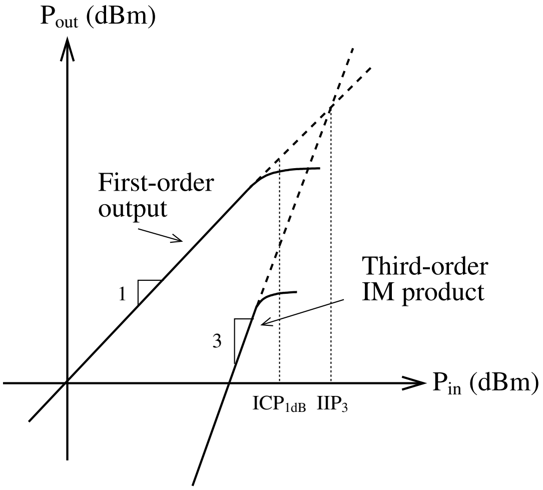

Figure 14: Intercept diagram

The dynamic range of the front-end can be defined as the input power range where the front-end is useful, with the lower limit set by the noise floor and the upper limit by the compression point.

In terms of linearity, a total IIP$_3$ of the front-end can be calculated if the gain and IIP$_3$ is known for all the included blocks (27) [2, 3],

$$\frac{1}{\mathrm{IIP}_{3,tot}^2} = \frac{1}{\mathrm{IIP}_{3,1}^2} + \frac{\mathrm{A}_{v,1}^2}{\mathrm{IIP}_{3,2}^2} + \cdots + \frac{(\mathrm{A}_{v,1}\mathrm{A}_{v,2}\cdots\mathrm{A}_{v,n-1})^2}{\mathrm{IIP}_{3,n}^2} \tag{27}$$

where $\mathrm{A}_{v,x}$ is the voltage gain of block x. The equation shows that, contrary to (26), the gain of the first stage should be low to get a high $\mathrm{IIP}_{3,tot}$. Thus, a trade-off has to be made as simulataneous optimization for low noise and high linearity is not possible. Note that in equation (27) no filtering is assumed between the blocks, whereas in a practical radio receiver progressively sharper filtering is typically applied through the signal chain.

3.3.3 Phase Noise - Reciprocal Mixing

The oscillator should have good spectral purity, i.e. low phase noise. Otherwise a strong in-band interferer, close to the wanted RF signal, can be down-converted and smeared out in frequency. The down-converted interferer could then partly mask or completely overlap the wanted RF signal, resulting in erroneous detection of the transmitted information in the receiver. This is known as reciprocal mixing and is illustrated in Figure 15.

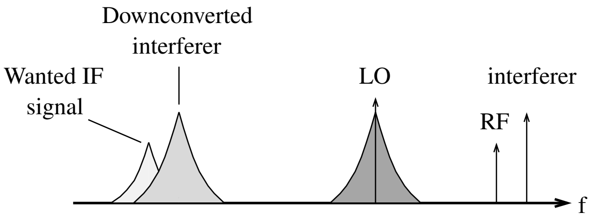

Figure 15: An illustration of reciprocal mixing

3.3.4 Imperfections exposed on the received information

The isolation between different blocks of the front-end is important as leakage can cause DC offsets at the mixer output due to the LO or the RF signal mixing with itself. This is usually referred to as self-mixing and is illustrated in the block diagram of Figure 16. The LO signal can leak to the mixer or LNA input and result in a DC offset after being mixed with itself. Similarly, the RF signal can leak to the LO input and

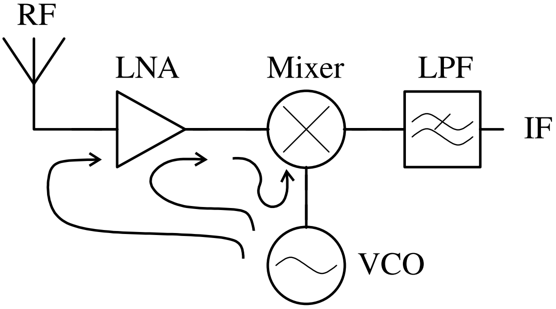

Figure 16: Front-end self-mixing

cause a DC offset. The leakage on-chip is usually through substate coupling, capacitive coupling, or even inductive coupling. The DC offsets can saturate the following low frequency amplifiers and the ADC. It is particularly harmful in direct conversion receivers as was described in section 2.2.3.

Quadrature amplitude modulation (QAM) is a common modulation scheme used in wireless communication systems. An ideal constellation diagram, using 16-QAM, is shown in Figure 17(a). Each dot in the figure is a symbol value. Each symbol represents 4 bits, since it can have 2^4 different values. Also shown, with dashed lines, are the decision boundaries. If noise is added in the front-end, the constellation diagram could look like in Figure 17(b), where the dots in the noise clouds represent different received symbols. The noise makes error free detection hard, especially close to the decision boundaries. Additionally, the constellation diagram is also affected by oscillator phase noise (through random phase variations) and interferers (through front-end non-linearities and limited filter selectivity), making it even harder to detect the transmitted information correctly.

Since the transmitted information typically includes redundant information through coding, the transmisson and the detection do not have to be entirely error free. However, a certain maximum bit error rate (BER) is in general specified for a digital communication system.

3.4 Survey of Front-ends

A short overview of some state-of-the-art microwave and millimeterwave front-ends is given in this section along with a description of the front-ends included in this thesis. More state-of-the-art designs exist than can be cited here.

In 2002 Guan *et al.* [47] presented a 24GHz CMOS receiver front-end achieving 27.5dB conversion gain and 7.7dB NF at 5GHz IF while dissipating 64.5mW. In the following years a lot of research was put into CMOS front-ends, also to push them to higher frequencies [48–51]. The 65nm CMOS front-end in [51], also including an on-

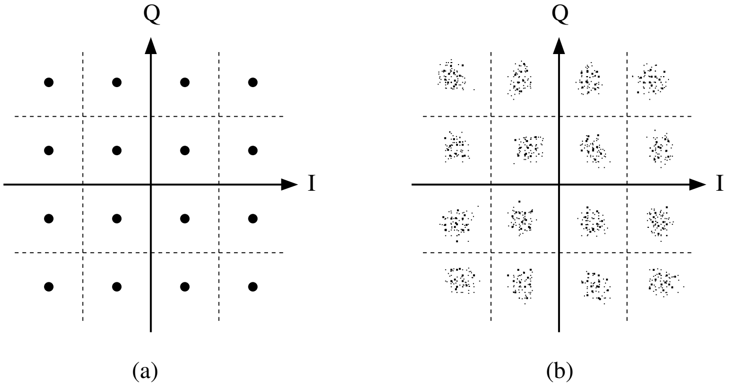

Figure 17: 16-QAM constellation diagrams, (a) ideal and (b) perturbed by noise

chip ADC, achieves a NF of 7dB at 60GHz with 198mW power consumption (P_{DC}). Using GaAs mHEMT technology Gunnarsson *et al.* in [52] demonstrated a 60GHz receiver with a 12.9dB conversion gain and 7.2dB NF at 450mW P_{DC}, and in [53] a 220GHz MMIC receiver achieving 8.4dB NF.

The fully differential front-ends of Papers I and IV use low loss baluns on a glass carrier (covered in Chapter 4) to generate the differential LO and RF input signals. A single-ended RF input front-end is also demonstrated in Paper IV, where only an LO input balun is used on the carrier. The front-end in Paper I uses a common source topology for the input LNA stage and achieves an overall NF of 7dB at 38mW P_{DC}, whereas the more broadband common gate topology is used in Paper IV. The fully differential front-end of Paper IV achieves 21dB conversion gain and 7.8dB NF at 28.6mW P_{DC}, and the one using single-ended RF input achieves 15dB conversion gain and 8.5dB NF at 33.8mW P_{DC}.

An on-chip quadrature receiver front-end at 24GHz in 90nm CMOS (including QVCO) is demonstrated in Paper VI, the front-end die photograph is shown in Figure 18. The RF input is single-ended, but is converted to differential form in the first LNA. The LNAs have two bands of operation within the QVCO tuning range, and the front-end measures 18dB conversion gain and 8.9dB NF at 64mW P_{DC} in the higher band.

The performance of the microwave and millimeter wave receiver front-ends is summarized in Table 1.

Table 1: Some published receiver front-end results

Ref.	Technology	f (GHz)	NF (dB)	Gain (dB)	IIP_3 (dBm)	ICP_{1dB} (dBm)	P_{DC} (mW)
Paper I	0.13μm CMOS SOP	20	7.0	11	-5.2	-16	38
Paper IV	0.13μm CMOS SOP	24	7.8	20.7	-12.6	-23.3	28.6
Paper VI	90nm CMOS	24	8.9	18	-11	-23	64
[47]	0.18μm CMOS	24	7.7	27.5			64.5
[48]	0.13μm CMOS	60	12.5	28*		-22.5	9
[49]	90nm CMOS	60	8.4	22			144
[50]	65nm CMOS	60	9.2	14.5		-24.4	134
[51]	65nm CMOS	60	7.0	45-79*		-38.5	198
[52]	0.15μm GaAs mHEMT	60	7.2	12.9	-10	-17	450
[53]	0.1μm GaAs mHEMT	220	8.4	1.8			

*Voltage gain

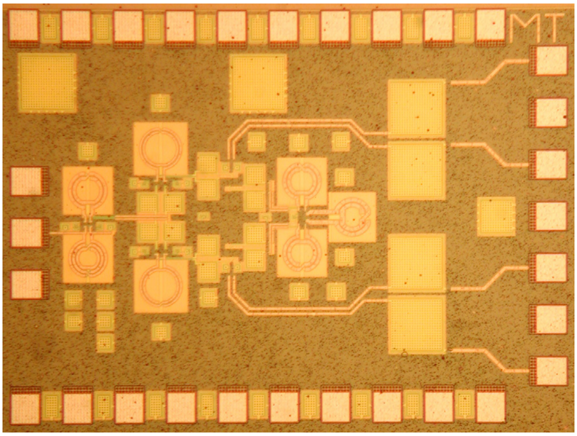

Figure 18: Quadrature receiver front-end in 90nm CMOS

Chapter 4

System-on-Package Technology

The performance of the different building blocks in CMOS front-ends is usually limited by the on-chip passive components. Unfortunately the passive components also have a high cost since they, mainly inductors, occupy a majority of the integrated circuit area. Even with the rapid technology scaling, with Moore's law saying that the number of transistors will double on a given circuit area about every two years, the passive components do not scale much. The following sections therefore discuss on-chip passives, postprocessed inductors, and carrier technology for System-on-Package (SOP) .

4.1 On-Chip Passives

As was mentioned above the on-chip passive components usually limit the performance due to their low Q values. For monolithic inductors the losses are due to the series resistance of the metal trace and resistive losses in the substrate due to capacitive and inductive coupling. The losses of the wire can be lowered by using a top metal with thick copper metallization instead of aluminum, however, this is not always supported by the foundries for standard fabrication processes. By shunting more metal levels the resistance can also be lowered, but this unfortuanately increases the capacitive coupling and lowers the self resonance frequency of the inductor. To reduce the substrate losses a high resistivity, lightly doped, substrate can be used. Furthermore, a patterned ground shield in the poly or metal 1 layer can be used to block the capacitively coupled substrate losses at the expense of a slightly reduced inductor self resonance frequency.

Inductors can be realized with a number of different geometries e.g. spiral, differential, bondwire, or transmission line stubs. Differential geometries are preferred over spriral since they occupy less area for a given inductance, and can have a higher Q value. Bondwire inductors have high Q but the inductance is hard to predict accurately due to uncertainty of the bondwire length, thus they are seldom used at high frequencies. The transmission line stubs also offer fairly high Q and are more common in millimeter-wave circuits, where their length is short enough to be practical. The quality factor of on-chip inductors tends to increase with operating frequency, as the equivalent series resistance increases less with frequency than the reactance.

For MOS varactors on the other hand the Q value is inversely proportional to frequency. The reason is that the losses are dominated by the frequency independent series resistance, and that the reactance of a capacitor is inversely proportional to the frequency. The Q will, however, improve with technology scaling as the channel gets shorter, but the capacitance tuning ratio will also drop since parasitics will then have more impact on the overall capacitance. The varactor Q is usually limiting the phase noise performance for microwave and millimeter wave oscillators. More about MOS varactors can be found in section 3.1.1.

4.2 Postprocessed Inductors

By placing the inductors on top of the back-end-of-line (BEOL) metal layers the distance to the chip substrate is increased, which results in higher Q. It is performed by depositing a thick dielectric, usually BCB, and metal above the BEOL passivation layer. This is also referred to as postprocessing or wafer level packaging (WLP). Due to the lower resolution requirements, the mask cost is lower for WLP than for a standard IC process. In [27] a microwave CMOS VCO achieved a FOM of 199dB using postprocessed inductors. A patterned ground shield can also be used, with great benefit, with a postprocessed inductor as demonstrated in [54], where the Q factor of a 1.4nH inductor at 5GHz was doubled to 40 by the use of a patterned ground shield in the poly layer.

4.3 Carrier Technology

Moving the passives completely off-chip to a low loss carrier is another feasible way to achieve high Q passive components. The general idea of the System-on-Package (SOP) concept [55] is to improve the performance by moving critical passive components from the chip to a low loss carrier. Depending on the carrier technology different components can be realized, e.g. inductors, baluns, capacitors, antennas, and tunable ferroelectric components.

The process stack-up of the glass carrier technology used in the SOP designs of Papers I, IV, V, is shown in Figure 19 [56]. As can be seen in the figure the active die is flip-chip mounted to the glass carrier, which is optimized for high Q RF passive components. The carrier features three metal layers on a non conductive substrate which offers very low losses. Different high Q components can be realized, e.g. metallic resistors (with better than 5% accuracy), MIM capacitors (up to 5nF/mm^2), and high Q thick copper inductors (Q up to 100).

Flip-chip mounting is used extensively in high performance applications and is the method of choice for silicon microwave circuits. Soldering is typically used to join the active die - stud bump - carrier, since it offers high reliability, self-alignment, and a good electrical connection [57]. The chip to carrier assembly can be done with a standard pick and place machine for SMD components before the package is put through the oven. The carriers can also be bumped for flip-chip mounting on a common motherboard (PCB), see Figure 20.

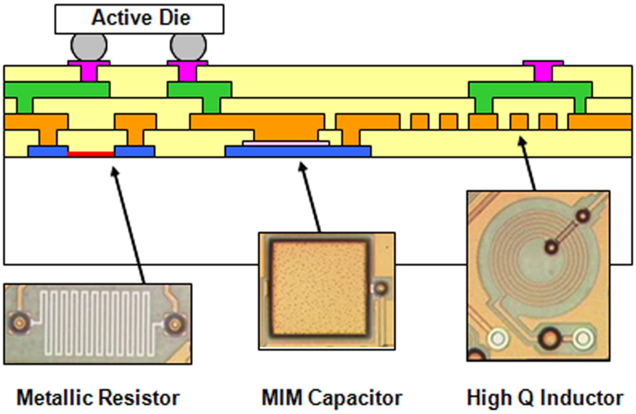
Active Die
Metallic Resistor
MIM Capacitor
High Q Inductor

Figure 19: Process stack-up (STMicroelectronics)

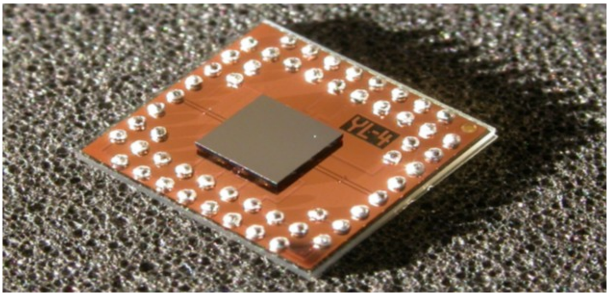

Figure 20: Bumped carrier for flip-chip mounting on a motherboard [58]

Reliable models for the chip to carrier transitions are vital at microwave frequencies, otherwise package parasitics can seriously degrade the performance. The stud bumps used have a height of 50μm. According to EM simulations the transition from chip to a 50Ω line on the carrier can be modelled by a shunt capacitance of 60-70fF, dependent on e.g. line distance to signal ground and the position of bridges over CPW lines.

A SOP 24GHz VCO with 20% tuning range (Paper V) is shown in Figure 21. The oscillator core operates at 6GHz and is followed by two cascaded on-chip frequency doublers. The oscillator core utilizes a differential high-Q inductor on the carrier, which is visible to the left of the chip. The lower core frequency reduces the impact of package transition parasitics and the losses due to large on-chip MOS varactors as the Q is inversely proportional to frequency. The VCO output was probe measured on the carrier and the DC signals were wirebonded to a PCB. The VCO achieves an FOM of 191dB and an FOM$_T$ of 197dB, which is comparable to [59] where ferroelectric varactors were used to achieve an FOM of 191dB and an FOM$_T$ of 195dB. The ferroelectric varactors have low losses (Q higher than 50) but they require high control voltages [60].

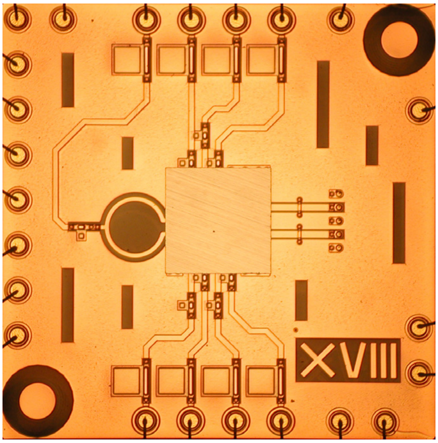

Figure 21: 24GHz 20% tuning range SOP VCO (5x5mm^2)

A fully differential 24GHz CMOS front-end (Paper IV) using low loss baluns on carrier is shown in Figure 22. The baluns are used generate differential RF and LO input signals to the chip, and they exhibit an insertion loss of only 0.3dB at the frequencies of interest. In measurements the RF and LO signals were connected by Cascade Infinity GSG probes, whereas the DC and low frequency IF signals were wirebonded from the carrier to a PCB. A SOP front-end using single-ended (SE) input and another type of balun for the LO signal (Paper IV) is depicted in Figure 23, where the RF input CPW line can be seen to the left of the chip.

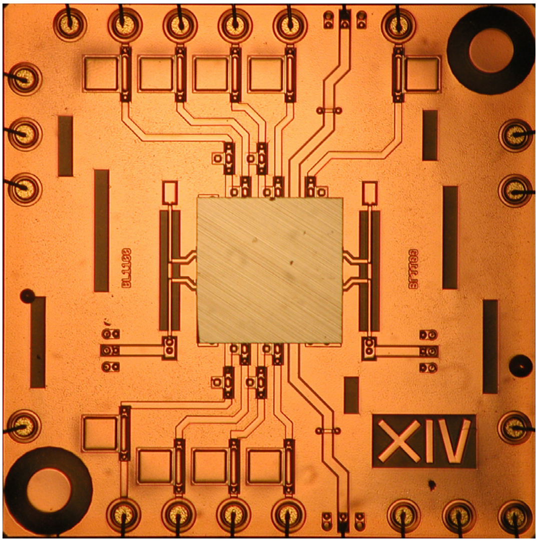

Figure 22: A fully differential SOP front-end (5x5mm^2)

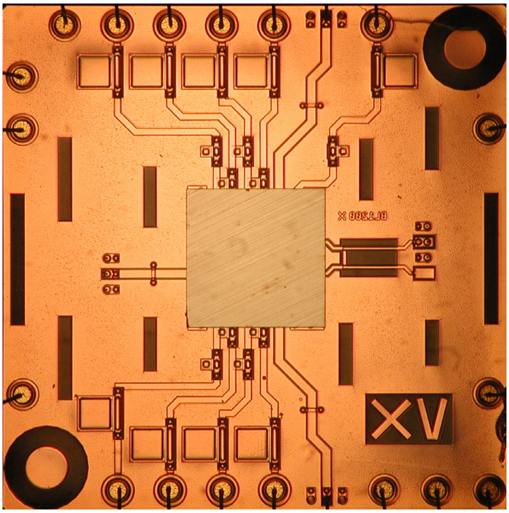

Figure 23: A SOP front-end with SE input (5x5mm^2)

Chapter 5

Discussion and Future Work

The results presented in this thesis for microwave front-end receiver blocks are very encouraging as several designs show high performance, but more research is still needed. This section discusses the work in this thesis and some ideas for future work.

Different microwave System-on-Package (SOP) front-ends featuring LNAs and Mixers in 130nm CMOS technology, flip-chipped to glass carriers with low loss baluns for the LO and RF input signals, have been designed, fabricated, and measured (Papers I and IV). For one of the front-ends in Paper IV only a balun for the LO signal is required as the RF input is single-ended. A single-ended RF input is also used for the 90nm CMOS quadrature receiver front-end (including QVCO) of Paper VI. To further improve the front-end performance an interesting approach would be to move the on-chip inductors to the carrier. This can, however, be difficult due to the limited reactance of the resonance tanks, compared to the chip to carrier transition parasitics, but worth to investigate.

Different microwave CMOS oscillators achieving high FOMs are also presented in this thesis; a differential VCO in Paper II, a differential SOP VCO in Paper V, and QVCOs in Papers III and VI. To further improve the oscillator phase noise performance, any oscillator would in general benefit from moving the resonator to a low loss carrier. For the continuously tuned 24GHz SOP VCO with 20% tuning range, an alternative would be to use a bank of switched varactors and a smaller continuously tuned varactor, like in the QVCO of paper III.

For the future it would also be interesting to look more at the transmitter side. This has already been initiated with a 60GHz injection-locked PA design in 65nm CMOS, which has been sent for fabrication. It would also be interesting to combine the excellent CMOS switches with carrier technology to investigate tunable duplex filters for cellular devices.

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Paper I

Paper I

A 20-GHz 130-nm CMOS Front-End using Baluns on Glass Carrier

M. Törmänen and H. Sjöland, “A 20-GHz 130-nm CMOS Front-End using Baluns on Glass Carrier,” ⓒ 2008 IEEE. Reprinted, with permission, from *IEEE Proc. 2nd International Conference on Signals, Circuits & Systems, SCS 2008*, pp. 1-4, Nov. 2008, Hammamet, Tunisia.

A 20-GHz 130-nm CMOS Front-End using Baluns on Glass Carrier

Markus Törmänen
Department of Electrical and Information Technology
Lund University, Box 118, 221 00 Lund Sweden
Email: Markus.Tormanen@eit.lth.se

Henrik Sjöland
Department of Electrical and Information Technology
Lund University, Box 118, 221 00 Lund Sweden
Email: Henrik.Sjoland@eit.lth.se

***Abstract*—A 20-GHz 130-nm CMOS front-end using baluns on glass carrier is presented. The front-end consists of a CMOS die featuring a differential two-stage LNA, a passive double balanced mixer, and output buffers, which is flip-chipped on a glass carrier where baluns are realized for the RF and LO signals. The front-end measures a conversion gain of 11 dB, a noise figure of 7 dB, a 60 dB LO to RF isolation, an ICP$_{1dB}$ of -16 dBm, an IIP3 of -5.2 dBm, and an IIP2 of +34.5 dBm. The power consumption, excluding output buffers, is 38 mW. Furthermore, the RF input is well protected as it can withstand a simulated 3 kV HBM ESD event.**

I. INTRODUCTION

The evolution of high data rate wireless communication systems has increased the demand for more bandwidth, which can be fulfilled by employing more and wider bands at higher frequencies for communications. The scaling of CMOS has now made it a viable technology for high frequency cost sensitive consumer applications. Publications have demonstrated high performance CMOS receiver front-ends at 60 GHz [1], and 24 GHz [2].

Differential receiver topologies are known to have higher linearity and a higher degree of stability compared to single-ended topologies, at the expense of higher power consumption. These properties were reported already 1965 [3]. A disadvantage of differential topologies is that the antenna signal typically is single-ended, and that a balun then is needed to convert it to differential form. To achieve good noise performance the balun must have low losses, which makes it difficult to realize on chip.

This paper presents measurement results of a front-end using a differential topology for increased linearity, and capacitive cross-coupling for increased LO to RF isolation. The CMOS die is flip-chipped on a glass carrier, where low loss baluns are realized for the RF and LO input signals.

II. CIRCUIT DESIGN

The block schematic of the front-end is shown in Fig. 1. It consists of a differential two-stage LNA, a passive double balanced mixer, and open drain output buffers. The baluns on the glass carrier, to generate the differential RF and LO input signals, are also shown in the figure.

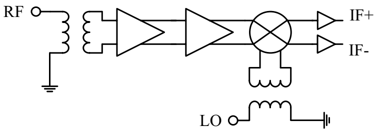

Fig. 1. Front-end block schematic

The first stage of the LNA is an inductively degenerated common-source stage with a cascode device as shown in Fig. 2. This topology provides good input matching, a low noise figure, and high reverse isolation. To further increase the differential isolation, a capacitive cross-coupling technique is used. Capacitors C1 and C2 form voltage dividers used to feed part of the output signal to the gate of the opposite cascode devices. By setting the voltage division ratio correctly, the currents due to the drain-source conductance of the cascode devices can be cancelled for differential signals. Techniques like this will become more important when the MOS transistors are scaled to shorter channel lengths, since the drain-source conductance then increases. Spiral shunt inductors, Lsh, are used at the input to resonate with the capacitances of the pad and the flip-chip bump. The shunt inductors also provide good ESD protection to the input transistor gates. The gate inductance, Lg, is realized by two wires close to each other, and a small loop, which can be seen in the die photograph, Fig. 11. Differential inductors are used to provide inductive degeneration, Ls, and to resonate the output, La. The ouput of the first stage is loaded by the input impedance of the second stage of the LNA.

The second stage of the LNA is a differential common-source stage with cascode devices and capacitive cross-coupling, as shown in Fig. 3. The output is resonated by a differential inductor, Lb, and is also loaded by the input impedance of the mixer.

Having a two-stage LNA provides sufficiant gain for a passive mixer to be used. In this circuit, a double-balanced passive mixer is used. To enable measurements, open-drain buffers designed to drive 50 Ω loads are connected to the ouputs of the mixer. The mixer and open-drain buffers are shown in Fig. 4. The RF signal is AC-coupled to the mixer, pre-

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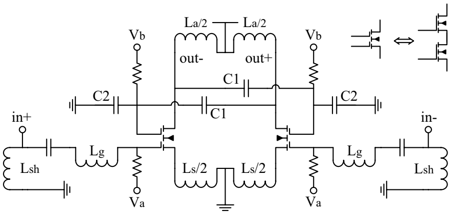

Fig. 2. First stage of the LNA

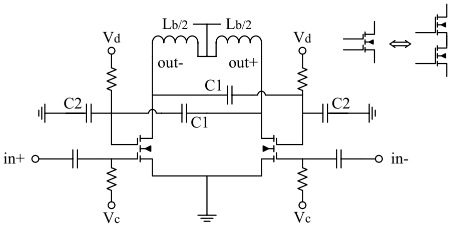

Fig. 3. Second stage of the LNA

venting DC-current, and setting the DC-voltage to zero through 40 kΩ resistors. In this way fast NMOS mixer devices can be used.

This circuit uses differential single turn and two turn spiral inductors. Their geometries were found by using FastHenry in combination with the in-house inductor optimization tool, Indentro [4]. Patterned ground shields in metal 1 are used beneath the inductors to block capacitively coupled substrate losses. The simulated inductance, quality factor, and self resonance frequency of the inductors are shown in Table I.

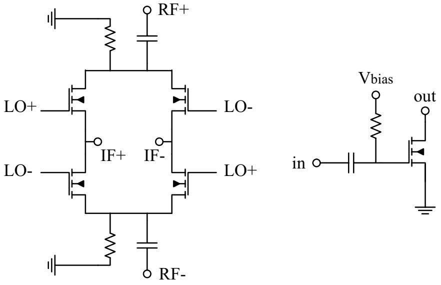

Fig. 4. Passive mixer and output buffer

TABLE I
INDUCTOR DATA

Inductor	Turns	Inductance (pH)	Q	fs (GHz)
Lg	1	170	15	140
Lsh	2	220	18	56
Ls	1	230	27	126
La	1	180	29	130
Lb	1	240	32	97

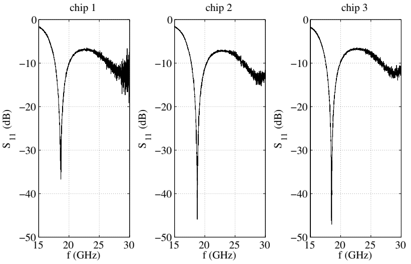

Fig. 5. Measured input matching of the three chips

III. LAYOUT

To minimize parasitic capacitance between the common-source and cascode transistors of the LNA, and thereby the noise contribution of the cascode device, a double-gate transistor layout was used [5]. The reduced capacitance also has a positive effect on the gain. The joint layout is indicated by the double gate transistor symbols used in Fig. 2 and 3.

The chip layout was designed as symmetrical as possible to minimize amplitude and phase errors. The die photo is shown in Fig. 11, where the padframe area measures

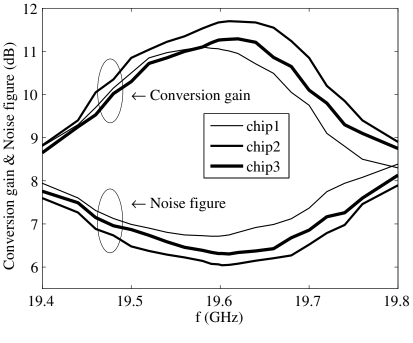

Fig. 6. Measured conversion gain & noise figure with LO = 19.6 GHz

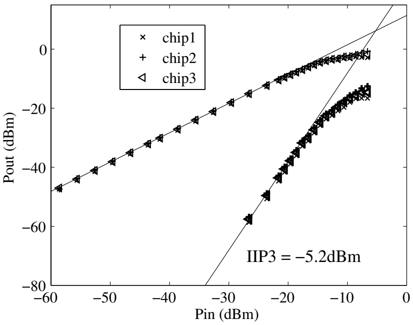

Fig. 7. Measured third order nonlinearity

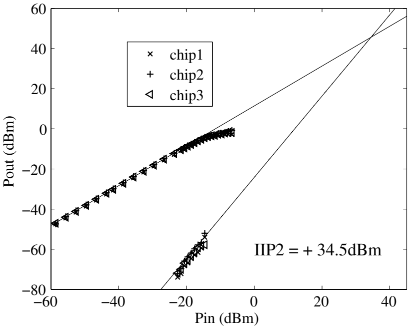

Fig. 8. Measured second order nonlinearity

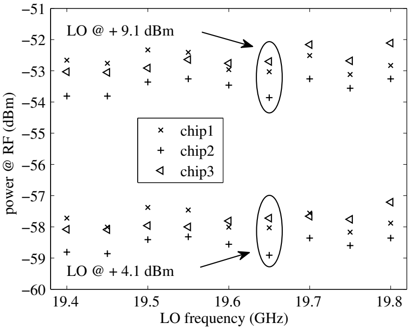

Fig. 9. Measured LO-RF isolation

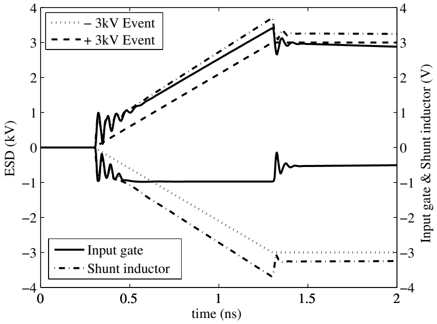

Fig. 10. Simulated HBM ESD events

1435μm x 985μm. The die was flip-chipped on a glass carrier, which is shown in Fig. 12. The chip can seen in the middle of the figure and the baluns for the RF and LO inputs can be seen on the left and right sides of the chip. The padframe area of the carrier measures 5620μm x 4960μm. The carrier was then glued to a PCB, and DC connections (supply, bias and ground) and IF outputs were wire-bonded from the carrier to the PCB.

IV. RESULTS

Three samples of the front-end have been measured. Instruments used were Rhode & Schwarz spectrum analyzer (FSU50), Agilent network analyzer (E8361A) and signal generators (E8257D).

The measurements were performed with a probestation using Cascade Microtech ground-signal-ground (GSG) probes for the RF and LO input signals on the carrier. The IF outputs were connected to a Minicircuits balun, T2-1T (0.07 to 200 MHz), through bias-T:s. The best performance of the front-end was found at 1.35 V supply and 28 mA current for the LNA. The power consumption is then 38 mW, excluding the buffers. The open-drain buffers were biased to a drain voltage of 1.35 V and a drain current of 8.4 mA each, which gives a total power consumption of 60 mW. The following results were measured at this bias point.

The measured input matching for the three chips is shown in Fig. 5. The matching is good just below 20 GHz, where also the highest gain is observed. A second resonance that could not be seen in simulations was observed for all chips. This is probably due to improper modeling of the transition from chip to carrier.

The conversion gain and noise figure have also been measured, Fig. 6, where the LO frequency and amplitude was kept at 19.6 GHz and 9.1 dBm, respectively. At about 19.6 GHz, close to zero-IF, the conversion gain is above 11 dB and the noise figure below 7 dB.

The linearity was measured using two tone tests, one for

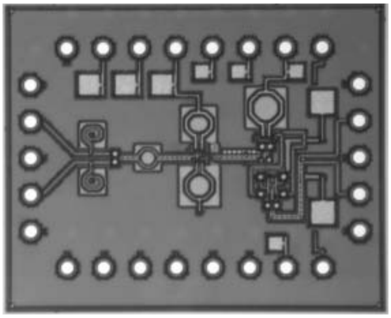

Fig. 11. Die photograph (1435μm x 985μm)

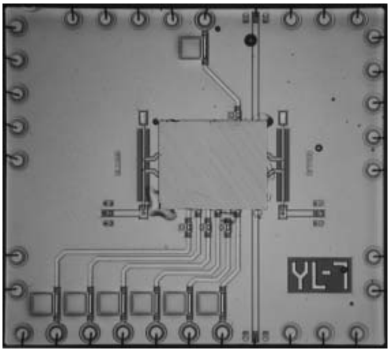

Fig. 12. Photograph of the die mounted on carrier (5620μm x 4960μm)

third order and one for second order intermodulation.

The two tones and the LO frequency were chosen such that the intermodulation product occured at an IF of 3 MHz. When measuring the second order nonlinearity a fifth order low-pass filter with a cut off frequency of 5 MHz was used to prevent intermodulation of the first order IF output tones (placed at 20 MHz and 23 MHz) in the spectrum analyzer. The input-referred 1 dB compression point, ICP_{1dB}, and third-order intermodulation, IIP3, are shown in Fig. 7. The ICP_{1dB} and IIP3 measures -16 dBm and -5.2 dBm, respectively. The second-order intermodulation measures +34.5 dBm and is shown in Fig. 8.

The LO to RF isolation has been measured at two different LO amplitudes, Fig. 9. As can be seen in the figure the isolation is at least 60 dB.

The ESD protection at the RF input has been simulated using the human body model (HBM), [6] [7]. A capacitor of 100 pF is first charged and then discharged through a 1500 Ω resistor to the test circuit. In Fig. 10 the voltages at the shunt inductor and input gate of the LNA are plotted for two simulated ESD events, +3 kV and -3 kV, with a rise time of 1 ns. As can be seen in the figure, the input gate of the LNA is well protected. For the negative event the gate is also protected by a diode used to prevent antenna errors during the chip fabrication, hence the lower voltage at the gate in Fig. 10.

V. CONCLUSION

A 20-GHz front-end in 130-nm CMOS using baluns on glass carrier has been presented. It achieves a conversion gain of 11 dB and a NF of 7 dB. The balanced topology enables a measured third-order input referred intercept point, IIP3, of -5.2 dBm, a second-order input referred intercept, IIP2, of +34.5 dBm, and an input-referred 1 dB compression point, ICP_{1dB}, of -16 dBm. The front-end uses a differential cross-coupling to increase the LO to RF isolation and measures an isolation of 60 dB. The RF input is well protected by a shunt inductor, and according to simulations it can withstand a 3 kV HBM ESD event.

VI. ACKNOWLEDGMENT

The authors would like to thank Ericsson AB in Mölndal Sweden for financing this research as part of a MEDEA+ project (2T401 HI-MISSION). They would also like to thank Infineon Technologies for access to the state-of-the-art CMOS technology, STMicroelectronics for access to their glass carrier technology, and the Knut and Alice Wallenberg foundation for financial support in building up the high frequency measurement laboratory.

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Paper II

Paper II

A 25-GHz Differential LC-VCO in 90-nm CMOS

M. Törmänen and H. Sjöland, “A 25-GHz Differential LC-VCO in 90-nm CMOS,” © 2008 IEEE. Reprinted, with permission, from *IEEE Proc. Asia Pacific Conference on Circuits and Systems, APCCAS 2008*, pp. 554-557, Nov. 30 - Dec. 9, 2008, Macao, China.

A 25-GHz Differential LC-VCO in 90-nm CMOS

Markus Törmänen
Department of Electrical and Information Technology
Lund University, Box 118, 221 00 Lund Sweden
Email: Markus.Tormanen@eit.lth.se

Henrik Sjöland
Department of Electrical and Information Technology
Lund University, Box 118, 221 00 Lund Sweden
Email: Henrik.Sjoland@eit.lth.se

***Abstract*—A 25 GHz 90-nm CMOS differential voltage controlled oscillator is presented. Filtering is used at the common source node of the cross-coupled transistors to lower the phase noise. The frequency tuning is accomplished by a continuously tuned accumulation-mode MOS varactor. The oscillator measures a frequency tuning range of 8.7%, and a worst case phase noise over the tuning range of -106 dBc/Hz at 1 MHz offset, with a 1.1 V supply and a power consumption of 6.6 mW. The phase noise figure of merit, FOM, is between 185 dB and 187 dB over the tuning range.**

I. INTRODUCTION

Local oscillator signals with low phase noise are needed in radio frequency (RF) transceivers, and the development of the complementary metal oxide semiconductor (CMOS) technology in the past decade has made it a viable technology for high frequency applications. The differential cross-coupled LC oscillator is well known for its good phase noise performance and ease of implementation [1]. This work presents measurement results of such an oscillator operating at 25 GHz, implemented in 90-nm CMOS, featuring a continuously tuned accumulation-mode varactor [2]. According to the measurements, the circuit is capable of generating low phase noise signals that could be used in e.g. a fully integrated 25 GHz CMOS wireless transceiver.

II. CIRCUIT DESIGN

The schematic of the voltage controlled oscillator (VCO) is shown in Fig. 1. It consists of two cross-coupled transistors that realize a negative resistance to compensate for the resonator losses, a source inductor, a FET current source, and a capacitor in parallel with the current source. The three latter components form a filtered current source [3], which improves the phase noise performance of the oscillator. The FET current source is used because the best phase noise performance is achieved when the amplitude in the resonance tank is on the limit of being current limited. The current source should ideally be noiseless, and have a high impedance at $2f_0$ to prevent the cross-coupled pairs triode resistance from loading the resonator in the switched state, i.e. when one transistor is off and the other one is in the triode region. A source inductor is therefore used to resonate the parasitics of the source node at $2f_0$. Also, a capacitor in parallell with the current source shunts the high frequency noise from the current source to ground. The filtering technique thereby prevents tail current noise at $2f_0$ from creating phase noise, but low frequency tail current noise will still cause amplitude noise, which can be converted to phase noise by the nonlinearities of the varactor [4].

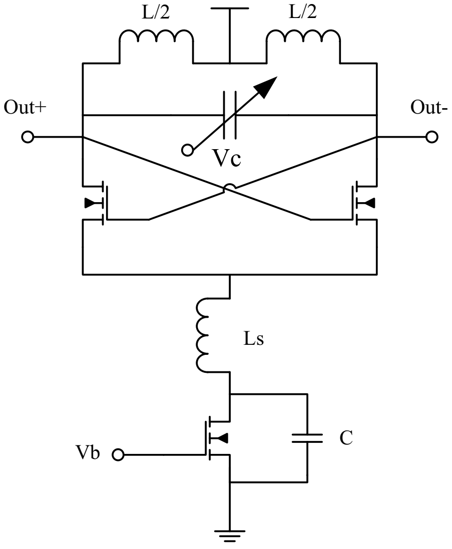

Fig. 1. VCO Schematic

A major challenge in oscillator design is to simultaneously achieve a low phase noise and a wide frequency tuning range. In oscillators using continuous frequency tuning, a wide tuning range is obtained using a large varactor with a high C$_{max}$/C$_{min}$ ratio. Unfortunately the losses of such a varactor will degrade the quality factor of the resonator, resulting in increased phase noise.

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TABLE I
SIMULATED INDUCTOR DATA

Inductor	Turns	Inductance (pH)	Q	fs (GHz)
L @ f_0	2	315	26	82
Ls @ $2f_0$	1	90	18	157

An accumulation-mode varactor [2], [5] was used in this work since it offers low losses. It operates in the accumulation and depletion regions, and has a non-minimum channel length, L, of 110 nm. A compromise was made not to use minimum channel length (90 nm), since although it would have given the varactor a slightly larger quality factor, Q, it would also have resulted in a smaller tuning range. It can be shown that the Q of the varactor is proportional to L^{-2} in the accumulation region [6], and to L^{-1} in the depletion region [7]. Since the losses of the varactor are dominated by series resistance, Q is inversely proportional to frequency, and the varactor will limit the total Q of the resonator at high frequencies and tuning ranges. There are no extra process steps used in the fabrication of the accumulation-mode varactor, but its generally not supported by the foundries. An inversion-mode varactor was used during the simulation phase, since no model of a high frequency accumulation-mode varactor with short channel length was available.

The inductor geometries were found by using FastHenry in combination with the in-house inductor optimization tool, Indentro [8]. The tank inductor was realized as a two turn differential inductor, and the source node inductor as a single turn spiral. The simulated inductor data is shown in Table I. The capacitively coupled substrate losses are blocked by patterned ground shields in metal 1 used beneath the inductors.

To enable measurements the oscillator was connected to open drain buffers designed to drive 50 Ω loads, Fig. 2, which were implemented on the same chip.

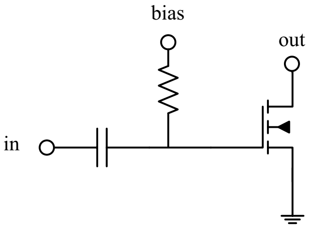

Fig. 2. Open drain buffer

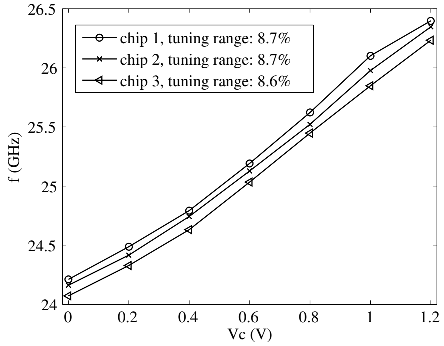

Fig. 3. Frequency vs. control voltage

III. LAYOUT

The die photo of the oscillator is shown in Fig. 8, where the padframe area measures 600 μm x 600 μm. The core area of the VCO measures just 120 μm x 310 μm, and is dominated by the two inductors. The entire layout was designed as symmetric as possible to minimize amplitude and phase errors. The pads on the top side are the RF-output signals (G-S-G-S-G) from the open-drain buffers. The pads on the bottom side are used for supply and bias voltages. The parasitic inductances of the wires to the inductors have been taken into account by adjusting the value of the tank inductor, L, and the source inductor, Ls, respectively. Also, all pads, except for the two RF outputs, are ESD protected. The ESD protection is realized using pn diodes for the pads, and multiple distributed clamps between the supply voltage and ground.

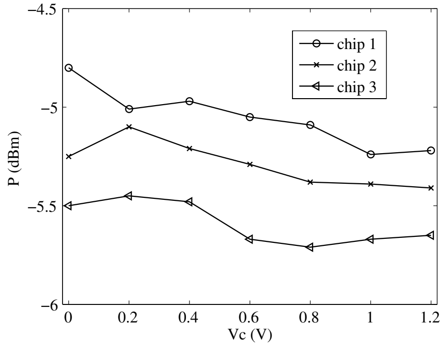

Fig. 4. Output power vs. control voltage

TABLE II
PERFORMANCE OF SOME PREVIOUSLY REPORTED CMOS VCOS AND THIS WORK

Ref.	Process	f_0 (GHz)	Tuning (%)	P_{DC} (mW)	PN @ 1 MHz (dBc/Hz)	FOM (dB)	FOM_T (dB)
This work	90nm CMOS	25.3	8.7	6.6	-105.8*	185	184
[9]	90nm CMOS	18	8.3	4.2	-116*	195	194
[10]	0.13μm CMOS	18	5.6	17.3	-117	190	185
[11]	0.13μm CMOS	11.55	5.5	8.1	-110.8	183	178
[12]	0.18μm CMOS	16	5.6	8.1	-111	186	181

*worst case phase noise over the tuning range

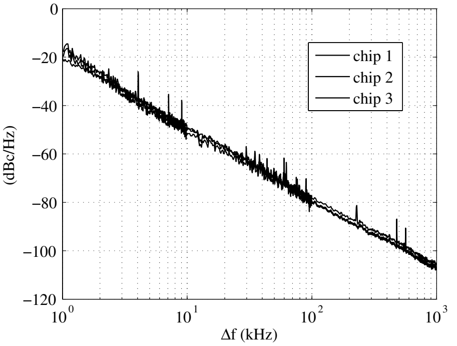

Fig. 5. Phase Noise vc. offset frequency, Vc=0.6 V

IV. EXPERIMENTAL RESULTS

Three different samples of the oscillator have been measured. The measurements were performed with a probe station using on-wafer probing with Infinity RF and Quadrant DC probes from Cascade Microtech. The best performance of the oscillator was found at 1.1 V supply and 6 mA current. This gives a power consumption of 6.6 mW for the oscillator core. The open-drain buffers were biased to a drain voltage of 1 V and a drain current of 6.5 mA per buffer. The following results were measured at this bias point.

A spectrum analyzer, Rhode & Schwarz FSU50, was used to measure the frequency tuning characteristic and the buffer output power. The results for the three different samples are shown in Fig. 3 and Fig. 4. As can be seen the tuning range measures 8.7%.

The phase noise of the three chips was measured using a Europtest PN9000 phase noise measurement system together with an external downconversion mixer, Marki M90765. A signal generator, Agilent E8257D, was used to generate the LO signal for the mixer.

The phase noise was measured versus offset frequency (Δf) for a varactor control voltage (Vc) of 0.6 V, see Fig. 5. The phase noise was also measured versus the varactor control voltage, Fig. 6. As can be seen in the figure, there is a phase noise variation of about 3 dB over the tuning range. Also shown in the legend of Fig. 6 is the phase noise figure of merit, FOM, which is between 185 dB and 188 dB for the measured samples, calculated at 1 MHz offset frequency using

$$FOM = 10\, log_{10}\left(\left(\frac{f_0}{\Delta f}\right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}}P}\right) \qquad (1)$$

,where P is the power consumption of the oscillator in mW, f_0 the oscillation frequency, Δf the offset frequency, and $L\,(\Delta f)$ the phase noise at Δf. To take also the tuning range into account, the expression (1) can be modified [13] to

$$FOM_T = 10log_{10}\left(\left(\frac{f_0 \cdot tuning\,(\%)}{10 \cdot \Delta f}\right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}}P}\right) \quad (2)$$

,which is between 184 dB and 187 dB for the measured samples at 1 MHz offset.

A performance comparison of some published state-of-the-art CMOS VCOs above 11 GHz and this work is shown in Table II. Some of the references in the table report only the best case value for the phase noise figure of merit, but to avoid sweet spots it is the worst case value over the tuning range that should be used for comparison. As can be seen in Table II the oscillator presented in this work compares well both in FOM and FOM_T. However, excellent performance is reported by Jacobsson et. al. [9], using post-processed high-Q inductors. This work instead uses standard CMOS without post processing or extra thick top metal options.

The oscillator pushing has also been measured and is shown in Fig. 7. As can be seen in the figure, there is approximately a 270 MHz frequency increase for a supply voltage change from 1.2 V to 0.9 V.

V. CONCLUSION

A differential 25 GHz LC VCO using an accumulation-mode varactor has been implemented in a 90-nm CMOS process. The oscillator measures a frequency tuning range of 8.7%. A good phase noise performance is measured over the entire tuning range, at worst -106 dBc/Hz at 1 MHz offset, with a power consumption of 6.6 mW for the oscillator core. This gives a phase noise figure of merit, FOM, of

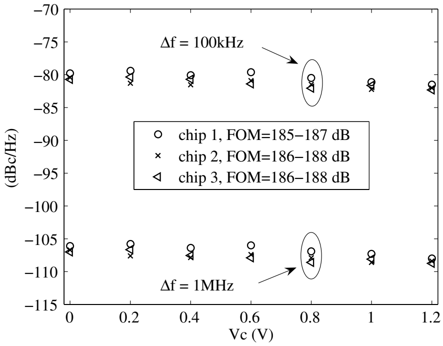

Fig. 6. Phase noise vs. control voltage

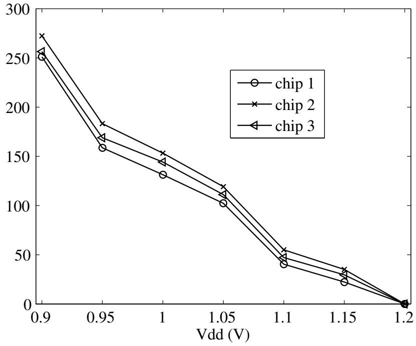

Fig. 7. Oscillator frequency pushing, Vc=0.6 V

185 dB. Taking also the tuning range into account gives a figure of merit, FOM$_T$, of 184 dB.

VI. ACKNOWLEDGMENT

The authors would like to thank UMC (United Microelectronics Corporation) for access to the state-of-the-art CMOS technology. They would also like to thank the Knut and Alice Wallenberg foundation for financial support in building up the high frequency measurement laboratory.

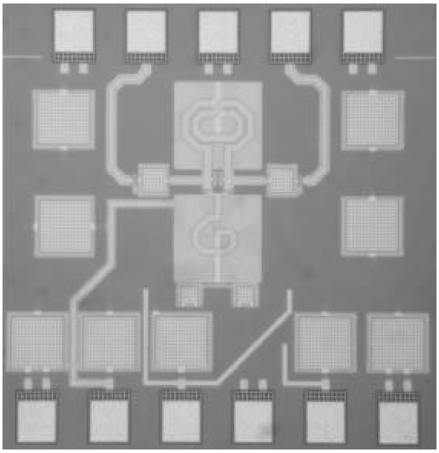

Fig. 8. Die photograph of the VCO (600 μm x 600 μm).

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Paper III

Paper III

A 24-GHz LC-QVCO in 130-nm CMOS using 4-bit Switched Tuning

M. Törmänen and H. Sjöland, "A 24-GHz LC-QVCO in 130-nm CMOS using 4-bit Switched Tuning," © 2008 IEEE. Reprinted, with permission, from *IEEE Proc. International Conference on Microelectronics, ICM 2008*, pp. 462-465, Dec. 2008, Sharjah, United Arab Emirates.

A 24-GHz LC-QVCO in 130-nm CMOS using 4-bit Switched Tuning

Markus Törmänen
Department of Electrical and Information Technology
Lund University, Box 118, 221 00 Lund Sweden
Email: Markus.Tormanen@eit.lth.se

Henrik Sjöland
Department of Electrical and Information Technology
Lund University, Box 118, 221 00 Lund Sweden
Email: Henrik.Sjoland@eit.lth.se

Abstract— **A 24 GHz 130-nm CMOS quadrature voltage controlled oscillator using 4-bit switched frequency tuning is presented. It consists of two differential oscillators coupled to oscillate in quadrature through transistors and mutual inductance between the source nodes. The frequency tuning is accomplished by 4 bits controlling an array of MOS varactors in each resonance tank, combined with a small continuously tuned varactor. The oscillator measures a frequency tuning range of 4.3%, and a worst case phase noise over the tuning range of -111.6 dBc/Hz at 1 MHz offset, with a 1.35 V supply and a power consumption of 24 mW.**

I. INTRODUCTION

Quadrature local oscillator signals are extensively used in modern wireless transceivers, which often use direct conversion or low-IF architectures. A commonly used technique to generate such quadrature signals is to use two coupled differential LC oscillators. This paper presents measurement results of such a quadrature oscillator operating at 24 GHz. The frequency tuning is realized using switched coarse tuning combined with continuous fine tuning [1]. In each resonance tank there is a small continuously tuned varactor, as well as an array of MOS varactors controlled by 4 digital bits. This is a modification of an oscillator previously reported by the authors [2], which was based on the original QVCO topology proposed by Rofougaran [3].

II. CIRCUIT DESIGN

The oscillator schematic is shown in Fig. 1. The QVCO previously reported by the authors [2] had a significant phase noise variation over the tuning range. The resonator was therefore modified to use 4 digital coarse tuning bits and a reduced size continuously tuned varactor. The ratio of the width of the coupling transistor to the width of the switch transistors was kept at 1/3.

As in the previous QVCO the phase noise is minimized by using a FET current source and applying filtering [4] at the source nodes of the two LC-oscillators. A current source is used because the best phase noise performance is achieved when the amplitude in the resonance tank is on the limit of being current limited. This requires a noiseless and high impedance current source to prevent the cross-coupled pairs triode resistance from loading the resonator in the switched state, i.e. when one transistor is off and the other one is in the triode region. Thus, a differential source inductor is used to resonate the parasitics of the source nodes at $2f_0$. The source inductor then approximates a high impedance current source at $2f_0$. Also, a capacitor in parallell with the current source shunts the high frequency noise at $2f_0$ from the current source to ground.

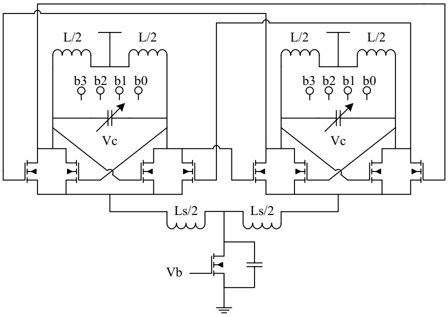

Fig. 1. QVCO Schematic

Simultaneously achieving a large frequency tuning range and a low phase noise is a major challenge in oscillator design. In oscillators using continuous frequency tuning, a large tuning range is obtained using a large varactor with a high maximum to minimum capacitance ratio. Noise and spuriouses on the varactor control voltage can then translate into significant phase noise and sidebands. The filtering technique described above prevents tail current noise at $2f_0$ from creating phase noise, but low frequency tail current noise will still cause amplitude noise. As shown in [5], the nonlinearities of the varactor convert harmless amplitude noise into phase noise. The larger the varactor the larger the problem. Furthermore, the Q of the varactor is due to series resistance inversely proportional to frequency. At high frequencies and wide tuning ranges, the varactor will therefore limit the total Q of the tank.

The varactors in this circuit are implemented using nMOS transistors operating in inversion-mode. By accepting a smaller maximum to minimum capacitance ra-

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TABLE I
RELATIVE TANK CAPACITANCE

b3	b2	b1	b0	Vc
4x	2x	1x	1x	2x

TABLE II
SIMULATED INDUCTOR DATA

Inductor	Inductance (pH)	Q	fs (GHz)
L @ f_0	200	33	115
Ls @ $2f_0$	190	37	140

tio, the minimum channel length could be used, maximizing the Q of the varactor and thereby the whole resonator. For layout reasons the relative capacitance of the different bits and the continuous part was chosen according to Table I. Ignoring the parasitics, there will then be nine different states that can be used. The different states are set by applying either 0 V or 1.5 V on the digital control bits. The continuously tuned varactor has size 2x to ensure overlap between the different states.

Differential single turn inductors are used in this circuit. The capacitively coupled substrate losses are blocked by using patterned ground shields in metal 1 beneath the inductors. The in-house inductor optimization tool, Indentro [6], was used to find the inductor geometries. The simulated inductor data is shown in Table II. The source inductor has the same size as in the previous QVCO, [2], but the tank inductors were made slightly larger to lower the oscillation frequency.

The oscillator is connected to open drain buffers implemented on the same chip. The buffers are used to enable measurements and are designed to drive 50 Ω loads.

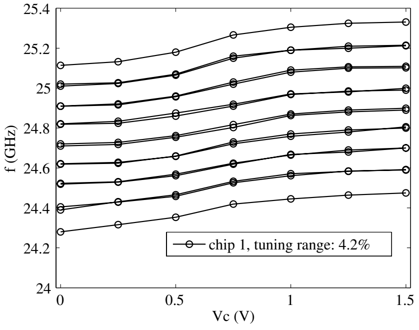

Fig. 2. Frequency vs. control voltage for chip 1

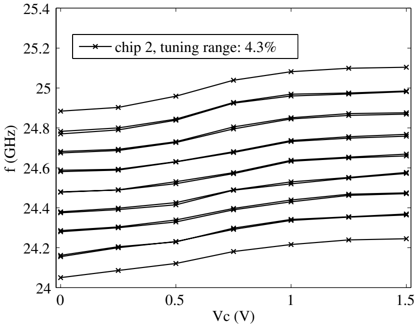

Fig. 3. Frequency vs. control voltage for chip 2

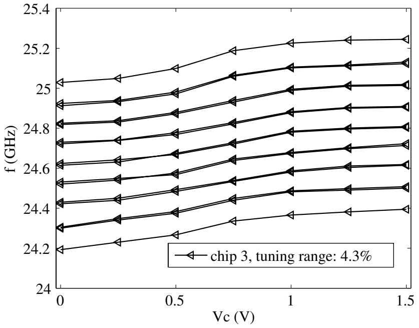

Fig. 4. Frequency vs. control voltage for chip 3

III. LAYOUT

The die photo of the oscillator is shown in Fig. 10, where the padframe area measures 985μm x 843μm. The pads on the top side are the four digital control bits and the varactor control voltage, Vc. The pads on the bottom side are used for supply and bias voltages. The outputs of the buffers are located on the left and right sides of the padframe. There are four coupling signal lines between the two differential oscillators. The length of these lines were kept as equal as possible to minimize phase errors. For the same reason the entire layout was designed as symmetric as possible.

IV. EXPERIMENTAL RESULTS

Three different samples of the oscillator have been measured. The measurements were performed with a probestation using on-wafer probing with signal-ground-signal (SGS) probes for the RF output and DC probes for biasing. The best performance of the quadrature oscillator was found at 1.35 V supply and 18 mA current. This gives a

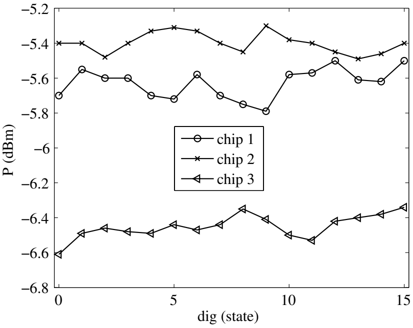

Fig. 5. Output power vs. dig (state) for Vc=0.75 V

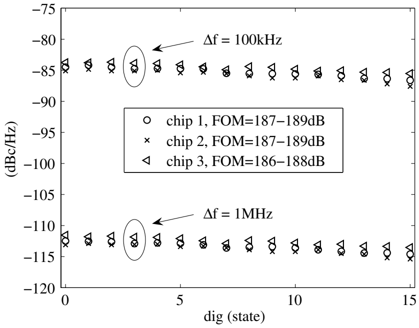

Fig. 7. Phase noise vs. dig (state) for Vc=0.75 V

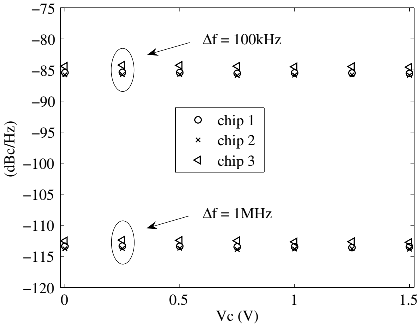

Fig. 6. Phase noise vs. control voltage for state 8 (1000)

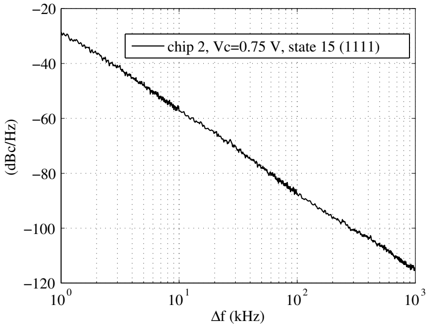

Fig. 8. Phase Noise, state 15 (1111) & Vc=0.75 V, for chip 2

power consumption of 24 mW for the quadrature oscillator core. The open-drain buffers were biased to a drain voltage of 1 V and a drain current of 9.4 mA per buffer. The following results were measured at this bias point.

A spectrum analyzer was used to measure the frequency tuning range and the buffer output power. The tuning characteristic for the three different samples can be seen in Fig. 2 - 4. As can be seen in the figures the tuning range is 4.3% and overlap between the different states guarantees continuous frequency coverage. The output power from the buffer for the three chips is shown in Fig. 5.

The phase noise of the three chips was measured using a Europtest PN9000 phase noise measurement system together with an external downconversion mixer. The previous QVCO had the worst phase noise in the middle of the tuning range. This is why the phase noise was measured for the mid state (b3b2b1b0=1000) versus the varactor control voltage, Fig. 6. As can be seen in the figure, the phase noise is almost flat over the varactor control voltage range, which corresponds to about 200 MHz in frequency tuning. The phase noise was also measured for the different states while keeping the varactor control voltage at Vc=0.75 V, Fig. 7. There is a phase noise variation of about 3 dB over the different states. Also shown in the legend of Fig. 7 is the phase noise figure of merit, FOM, which is between 186 dB and 189 dB for the measured samples, calculated at 1 MHz offset frequency using

$$FOM = 10\, log_{10} \left(\left(\frac{f_0}{\Delta f} \right)^2 \frac{1}{10^{\frac{L(\Delta f)}{10}} P} \right) \qquad (1)$$

,where P is the power consumption of the oscillator in mW, f_0 the oscillation frequency, Δf the offset frequency, and $L\,(\Delta f)$ the phase noise at Δf. The phase noise is also plotted versus offset frequency, Δf, for state 15 (1111) and Vc=0.75 V for chip 2, Fig. 8. A performance comparison of some previously reported QVCOs and this work is shown in Table III. Some references in the table report only the best case value of the phase noise, but it is the worst case value over the tuning range that should be used for comparison. To take also the tuning

TABLE III
PERFORMANCE OF SOME PREVIOUSLY REPORTED QVCOS AND THIS WORK

Ref.	Process	Frequency (GHz)	PN @ 1 MHz (dBc/Hz)	Core P_{DC} (mW)	FOM (dB)	FOM_T (dB)
This work	0.13μm CMOS	24.19-25.25	-111.6*	24	186	178
[7]	0.18μm CMOS	10.18-11.37	-118.7	11.8	188	189
[8]	0.13μm CMOS	44.8-45.8	-98.9	40	176	163
[2]	0.13μm CMOS	25.7-26.5	-96*	24	171	161
[9]	0.4μm SiGe	24.8-28.9	-84.2	129	152	156
[10]	0.25μm SiGe	30.6-32.6	-97	140	166	162

*worst case phase noise over the tuning range

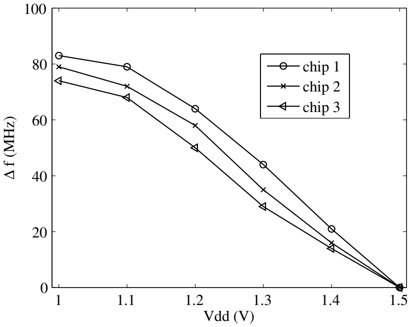

Fig. 9. Oscillator frequency pushing, state 8 (1000) & Vc=0.75 V

range into account expression (1) can be modified [11]

$$FOM_T = 10log_{10}\left(\left(\frac{f_0 \cdot tuning\,(\%)}{10 \cdot \Delta f}\right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}}P}\right) \quad (2)$$

,which is also shown in Table III for comparison.

The oscillator pushing is shown in Fig. 9. As can be seen in the figure, there is approximately an 80 MHz frequency change for a supply voltage change from 1.5 V to 1 V.

V. CONCLUSION

A 24 GHz P-QVCO using 4-bit switched tuning has been implemented in a 130-nm CMOS process. The oscillator measures a frequency tuning range of 4.3%. A good phase noise performance is measured over the entire tuning range, at worst -111.6 dBc/Hz at 1 MHz offset, with a core power consumption of 24 mW. This gives a phase noise figure of merit, FOM, of 186 dB.

VI. ACKNOWLEDGMENT

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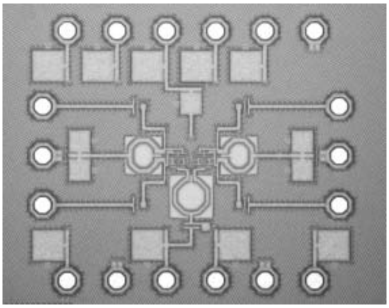

Fig. 10. Die photograph of the QVCO (985μm x 843μm).

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Paper IV

Paper IV

Two 24 GHz Receiver Front-ends in 130-nm CMOS using SOP Technology

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M. Törmänen and H. Sjöland, “Two 24 GHz Receiver Front-ends in 130-nm CMOS using SOP Technology,” © 2009 IEEE. Reprinted, with permission, from *IEEE Proc. Radio Frequency Integrated Circuits Symposium, RFIC 2009*, pp. 559-562, June 2009, Boston, Massachusetts, USA.

Two 24 GHz Receiver Front-ends in 130-nm CMOS using SOP Technology

Markus Törmänen and Henrik Sjöland

Department of Electrical and Information Technology, Lund University, Lund, SE-221 00, Sweden

***Abstract* — Two 24 GHz 130-nm CMOS receiver front-ends using System-on-Package (SOP) technology are demonstrated. CMOS dies featuring a two-stage LNA, a passive mixer, and output buffers are flip-chipped to a glass carrier featuring low loss baluns. One design uses glass baluns for both RF and LO input, whereas the other uses an active RF balun on-chip. The fully differential front-end measures; 20.7dB conversion gain, 7.8dB NF, -23.3dBm CP$_{1dB}$, -12.6dBm IIP3, 16.3dBm IIP2, and 44dB LO to RF isolation. The single-ended input front-end measures; 14.7dB conversion gain, 8.5dB NF, -21.1dBm CP$_{1dB}$, -10.4dBm IIP3, 17.6dBm IIP2, and 51dB LO to RF isolation.**

***Index Terms* — CMOS integrated circuits, Flip-chip devices, Frequency conversion, Microwave mixers, Microwave receivers.**

I. INTRODUCTION

The evolution of CMOS technology in the past decade along with its excellent integration capabilities has made it an attractive technology for microwave and millimeter wave wireless transceivers. Publications have shown good performance for CMOS receivers at 60 GHz [1], and 24 GHz [2], using single-ended topologies.

Differential receiver topologies are known to have higher linearity and better stability compared to single-ended ones, at the cost of higher power consumption. A disadvantage of differential topologies, however, is that the antenna signal typically is single-ended, and that a balun is needed to convert it to differential form. To achieve good noise performance the balun must have low losses, which makes it difficult to implement on a CMOS chip. The System-on-Package [3], SOP, concept can improve the performance by moving critical passive components like baluns from chip to a low loss glass carrier [4]. However, at microwave frequencies, reliable models for chip to carrier transitions are vital, otherwise package parasitics can seriously degrade the performance. An illustrative example of the SOP concept possibilities is shown in Fig. 1.

This paper presents measurement results from two different SOP front-ends. One front-end uses a fully differential chip, and the other has a chip with single-ended RF input. The single-ended chip features a novel active low noise balun, and the idea is to compare the performance of the two different solutions, one relying on SOP technology and the other mainly on CMOS integration. The CMOS dies are flip-chipped to glass carriers where low loss baluns are realized for RF and LO input signals (the chip with the single-ended RF input just uses an LO balun on the carrier).

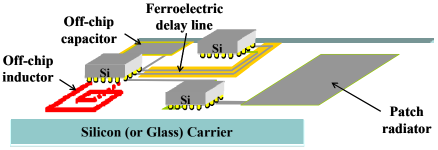


Fig. 1. Example of System-on-Package (SOP) possibilities.

II. CIRCUIT DESIGN

The block schematics of the two front-ends are shown in Fig. 2. The part implemented on the CMOS die consists of a two-stage LNA, a passive double balanced mixer, and open-drain IF output buffers.

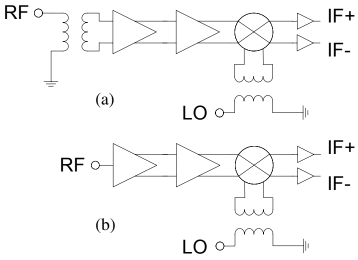
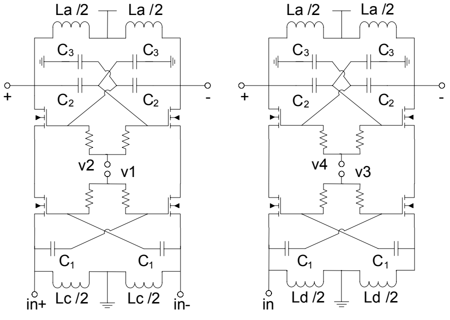


Fig. 2. Front-end block schematics. (a) Fully differential front-end using glass carrier baluns for RF and LO. (b) Front-end with single-ended RF input using glass carrier balun for LO.

The baluns, to generate the differential RF and LO signals, implemented on the glass carrier are also shown in the figure.

A. Chip design

The input stages of the two front-ends are shown in Fig 3. The differential front-end input stage consists of a common gate (CG) stage with cascode devices for increased isolation. Common-gate stages are known to provide wide band input match. Capacitive cross-coupling with capacitors C_1 is used for increased stability and noise performance. Techniques using capacitive-cross coupling at the input, or feed-forward noise cancellation, to improve the noise performance of LNAs are well known [5]-[7]. An inductorless active balun LNA with good wideband performance has also been reported [8]. However, with 130-nm CMOS inductorless techniques are not feasible at 24 GHz, so differential input and output inductors are used to tune the circuit to the operating frequency. The single-ended front-end input stage is similar to the differential one, except that one input terminal has been removed. The differential output signal is achieved through the capacitive cross-coupling and the coupling of the differential source inductor, Ld, [9].

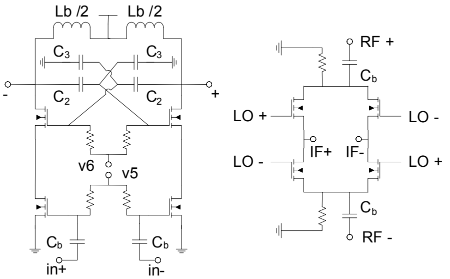


(a) (b)

Fig. 3. First stage of the LNAs. (a) The differential input stage. (b) The single-ended input stage.

A capacitive cross-coupling technique is used also at the output. The purpose is to further increase the differential signal isolation. Capacitors C2 and C3 form voltage dividers used to feed part of the output signal to the gate of the opposite side cascode devices [4]. Using this technique the currents due to the drain-source conductance of the cascode devices can be cancelled for differential signals.

Both front-ends have the same second stage of the LNA. It consists of a differential common-source (CS) stage with cascode devices and capacitive cross-coupling, as is shown in Fig. 4(a). The two stages of the LNA provide sufficient gain for a passive mixer to be used. The output of the second LNA stage is loaded by the input impedance of the mixer and is tuned to the operating frequency by the differential inductor Lb. The passive double-balanced mixer is shown in Fig. 4(b). The RF signal is AC-coupled to the mixer, preventing DC current, and setting the DC voltage to zero using the resistors.



(a) (b)

Fig. 4. (a) The second stage of the LNA. (b) The passive double-balanced mixer.

The LNAs use differential inductors. Their geometries were found using FastHenry in combination with an in-house inductor optimization software, Indentro [10]. The ADS Momentum tool was also used to simulate the interconnect to the inductors. The simulated inductor data for 24 GHz is shown in Table I. Patterned ground shields in metal 1 are used beneath all inductors to block capacitively coupled substrate losses.

TABLE I
INDUCTOR DATA

Inductor	Turns	Inductance (pH)	Q	fs (GHz)
La	2	300	16.4	114.3
Lb	2	410	18.8	87.2
Lc	2	490	20.2	71.1
Ld	3	610	23.5	49.8

Also included on the chip for measurement purposes, shown in the block schematics of Fig. 2, are open-drain IF buffers designed to drive 50 ohm loads.

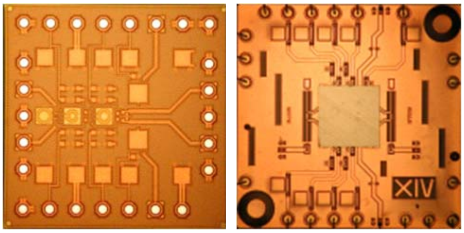
B. Glass carrier

The glass carrier is fabricated in STMicroelectronics commercial integrated passive process optimized for high-Q RF passive components. The carrier uses three metal layers. The baluns realized on carrier have a measured insertion loss of approximately 0.3 dB at the frequencies of interest.

III. LAYOUT

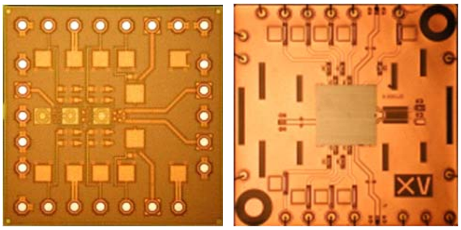
The CMOS dies were fabricated in a 6 metal layer, 4 Cu and 2 AlCu, 130 nm RF CMOS process from Infineon Technologies. Each front-end die version was flip-chipped to two different glass carrier designs, using two different versions of baluns, denoted hereon after as balun 1 (B1) and balun 2 (B2). This means that there are four different carrier designs in total.

A die microphotograph of the fully differential front-end is shown in Fig. 5(a). This chip mounted on a glass carrier using balun 1 for the RF and LO input signals is shown in Fig. 5(b). The chip can be seen in the middle of the figure and the baluns to the left and right of the chip.



(a) (b)

Fig. 5. (a) Die microphotograph of the fully differential front-end, 1.53 mm^2. (b) Photograph of the chip mounted on carrier using balun 1 for RF and LO input signals, 5x5 mm^2.



(a) (b)

Fig. 6. (a) Die microphotograph of the front-end with single-ended input, 1.53 mm^2. (b) Photograph of the chip mounted on carrier using balun 2 for the LO input signal, 5x5 mm^2.

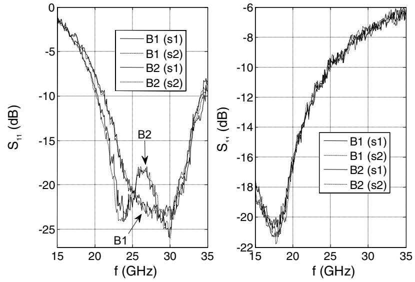
A die microphotograph of the front-end with single-ended input is shown in Fig. 6(a). This chip mounted on a glass carrier using balun 2 for the LO signal is shown in Fig. 6(b). The balun can be seen on the right side of the chip, and the RF input to the left of the chip, where a CPW line connects the RF input to the probing pads. The supply, bias and IF output signals were wire bonded from the carrier to a PCB. The supply and bias lines are decoupled using capacitors on the chip, carrier and PCB.

IV. MEASUREMENT RESULTS

There are four different designs, since each CMOS die type was flip-chipped to two different carriers using balun 1 and balun 2. Two samples of each design have been measured. The DC power consumption using a 1.2 V supply, excluding the open-drain buffers, is 28.6 mW for the fully differential front-end and 33.8 mW for the single-ended one. The two open-drain buffers consumed 12.5 mW altogether from a 1 V supply.

The measurements were performed with a probe station, using Infinity GSG probes from Cascade Microtech for the RF and LO inputs signals on the carrier. The IF outputs were connected to a Minicircuits balun, T2-1T (0.07 to 200 MHz), through bias-Ts.

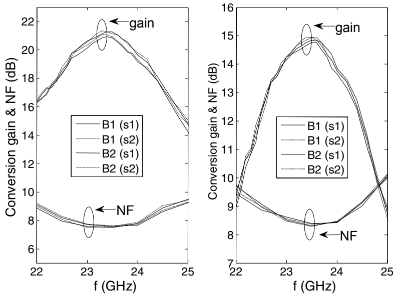
The measured input matching for both front-end versions is shown in Fig. 7. A second resonance is observed for the fully differential front-end using balun 2 in Fig. 7(a). The input matching shifted down in frequency for the front-end with single-ended input, although with S_{11} below -10 dB up to 25 GHz. This was probably due to improper modeling of the input CPW line on the carrier.



(a) (b)

Fig. 7. Input matching (two samples measured for each design). (a) The fully differential front-end. (b) The front-end with single-ended input.

The measured (de-embedded) conversion gain and noise figure is shown in Fig 8. The conversion gain was measured at an IF frequency of 3 MHz and the noise figure at 25 MHz. The fully differential front-end achieves a conversion gain of 20.7 dB and an NF of 7.8 dB, whereas the front-end with single-ended input achieves a conversion gain of 14.7 dB and an NF of 8.5 dB.



(a) (b)

Fig. 8. Conversion gain and NF (two samples measured of each design). (a) The fully differential front-end. (b) The front-end with single-ended RF input to the die.

The linearity was measured using two-tone tests, one for third order and one for second order intermodulation. The tones were chosen such that the intermodulation product to measure occurred at an IF of 3 MHz. A fifth order low-pass filter, with a cut off frequency of 5 MHz, was used when measuring the second order nonlinearity to prevent intermodulation of the first order IF output tones (placed at 20 and 23 MHz) in the spectrum analyzer. The measured linearity is summarized in Table II, where the result for each design is an average from two measured samples.

TABLE II
FRONT-END LINEARITY

Design	CP_{1dB} (dBm)	IIP3 (dBm)	IIP2 (dBm)
Diff. B1	-23.3	-12.6	16.3
Diff. B2	-24.5	-13.7	15.7
SE B1	-21.1	-10.4	17.6
SE B2	-21.5	-10.6	17.1

The LO to RF isolation has also been measured in the frequency band 22 to 25 GHz. In this frequency range the isolation is at least 44 dB for the fully differential front-end and at least 51 dB for the front-end with single-ended input.

V. CONCLUSION

Two SOP front-ends have been demonstrated, one using a fully differential CMOS die with low loss baluns on glass carrier for the RF and LO input signals. The other one using a single-ended RF input to the chip, converted to differential form in a novel merged low noise amplifier and balun, using a low loss balun on glass carrier only for the LO input signal.

The fully differential version achieves a conversion gain of 20.7 dB, NF of 7.8 dB, CP_{1dB} of -23.3 dBm, IIP3 of -12.6 dBm, IIP2 of 16.3 dBm, and an LO to RF isolation of 44 dB. The single-ended version achieves a conversion gain of 14.7 dB, NF of 8.5 dB, CP_{1dB} of -21.1 dBm, IIP3 of -10.4 dBm, IIP2 of 17.6 dBm, and an LO to RF isolation of 51 dB.

Although the single ended version uses one glass balun less, thanks to the novel low noise active balun its performance is not far from that of the fully differential design. If the input matching could be improved the performance would probably be even better.

ACKNOWLEDGEMENT

The authors wish to acknowledge the support of Ericsson AB for financing this research as part of the MEDEA+ project 2T401 HI-MISSION. They would also like to thank Infineon Technologies for access to their CMOS technology, STMicroelectronics for access to their glass carrier technology, and the Knut and Alice Wallenberg foundation for financial support in building up the high frequency measurement laboratory.

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Paper V

Paper V

A 24 GHz VCO with 20 % tuning range in 130-nm CMOS using SOP Technology

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M. Törmänen and H. Sjöland, “A 24 GHz VCO with 20 % tuning range in 130-nm CMOS using SOP Technology,” © 2009 IEEE. Reprinted, with permission, from *IEEE Proc. Radio Frequency Integrated Circuits Symposium, RFIC 2009*, pp. 473-476, June 2009, Boston, Massachusetts, USA.

A 24 GHz VCO with 20 % tuning range in 130-nm CMOS using SOP Technology

Markus Törmänen and Henrik Sjöland

Department of Electrical and Information Technology, Lund University, Lund, SE-221 00, Sweden

***Abstract* — A 24 GHz System-on-Package (SOP) VCO is demonstrated. The core operates at 6 GHz and employs a high-Q on-carrier inductor. Using two cascaded on-chip frequency doublers the centre frequency is 24.6 GHz with a 20 % tuning range. The phase noise is below -107 dBc/Hz at 1 MHz offset over the tuning range, with a FOM between 188 and 192 dB at a power consumption of 6.9 mW.**

***Index Terms* — CMOS integrated circuits, Flip-chip devices, Microwave oscillators, Phase noise, Voltage controlled oscillators.**

I. INTRODUCTION

Microwave link transceivers put stringent performance requirements on the local oscillator signals. They must have both low phase noise and preferably also a high tuning range to cover multiple frequency bands. This is a major challenge to achieve at microwave frequencies, as the limited quality factor of large varactors and on-chip inductors degrade the performance of oscillators. The System-on-Package, SOP, concept can improve the performance by moving critical passive components from chip to a low loss glass carrier [1]. However, at microwave frequencies, reliable models for chip to carrier transitions are vital, otherwise package parasitics can seriously degrade the performance. An illustrative example of the SOP concept possibilities is shown in Fig. 1.

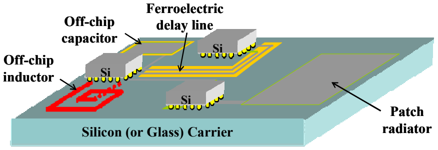

Fig. 1. Example of the System-on-Package (SOP) concept.

We demonstrate a 24 GHz VCO with a 20% tuning range in a 130 nm RF CMOS process using the SOP concept. The differential LC-oscillator core operates at 6 GHz, using a high-Q inductor on the glass carrier. The lower frequency reduces both the impact of package parasitics, and the losses of the large on-chip MOS varactors. The frequency of the signal is then multiplied by four using two cascaded frequency doublers. Using this technique a frequency tuning range of 20% is achieved, combined with a phase noise below -111 dBc/Hz at 1 MHz offset from a 24 GHz carrier, at a total power consumption of 6.9 mW.

II. CIRCUIT DESIGN

The schematic of the VCO including frequency doublers is shown in Fig. 2. A source node filtering technique is used to prevent the cross-coupled pairs triode resistance from loading the resonator in the switched state [2], i.e. when one transistor is off and the other one is in triode region. The source node inductor then approximates a high impedance current source as it resonates the parasitics at the source nodes at twice the operating frequency. A FET current source is used to set the DC current, and thereby also the oscillation amplitude. A capacitor in parallel with the current source shunts the high frequency noise from the current source to ground.

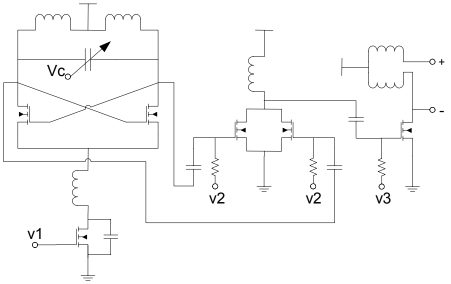

Fig. 2. Schematic of the VCO including frequency doublers.

The symmetric inductor of the LC-oscillator is realized on a glass carrier, fabricated in STMicroelectronics commercial integrated passive process optimized for high-

Q RF passive components. The carrier uses three metal layers and the process stack-up is shown in Fig. 3. The Q of the inductor at 6 GHz is above 80.

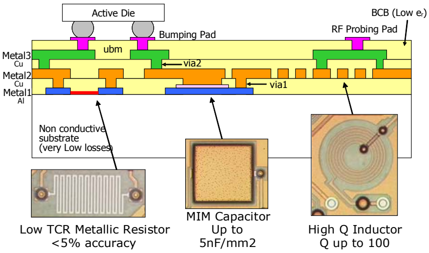

Fig. 3. Glass carrier process stack-up.

The varactor is continuously tuned, realized on-chip, and operates in the inversion and depletion regions. The varactor Q-value has been simulated in Fig. 4 at the VCO operating frequency, 6 GHz, and at the output frequency after the frequency doublers, 24 GHz. As can be seen the large varactor has a limited Q at the higher frequency. This would degrade the phase noise significantly if used in an oscillator at 24 GHz. Introducing the frequency doublers allows the oscillator to operate at 6 GHz, resulting in an acceptable varactor Q. The lower frequency also reduces the impact of the parasitics of the flip-chip interface between chip and carrier. To increase the second order non-linearity of the two frequency doublers their gate bias is set below the threshold voltage of the transistors. The outputs are tuned to 12 GHz and 24 GHz, respectively, using on-chip inductors. A symmetric inductor is used in the last frequency doubler to provide a differential output signal. Patterned ground shields are used beneath all on-chip inductors to block capacitively coupled substrate losses.

III. LAYOUT

The die microphotograph is shown in Fig. 5. Stud bumps used for flip-chipping can be seen on top of the pads. The chip is fabricated in a 6 metal layer, 4 Cu and 2 AlCu, 130 nm RF CMOS process from Infineon Technologies and is 0.97 mm^2, with an active area of 0.11mm^2.

A photograph of the chip mounted on carrier, using a regular commercial surface mount pick-and-place process, is shown in Fig. 6. The symmetric single-turn inductor on carrier can be seen to the left of the chip. To the right the differential output signal is seen, where CPW lines connect the RF signals to the probing pads. The supply and bias signals were wire bonded from the carrier to a PCB and the lines are decoupled using capacitors on the chip, carrier and PCB.

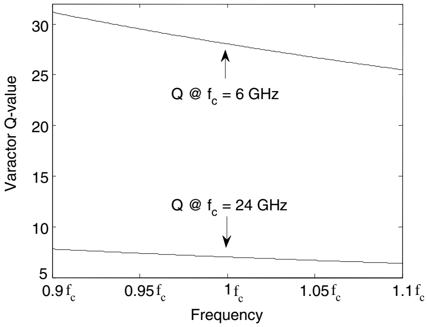

Fig. 4. Simulated varactor Q-values at 6 and 24 GHz over 20% tuning range.

Also included on the chip for measurement purposes, but not shown in the schematic of Fig. 2, are open-drain buffers designed to drive 50 ohm loads.

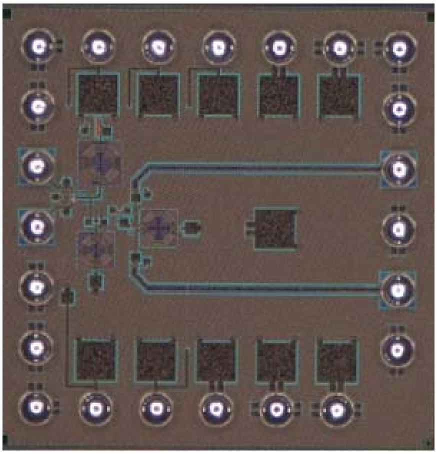

Fig. 5. Die microphotograph, 0.97 mm^2. The active area is 0.11 mm^2.

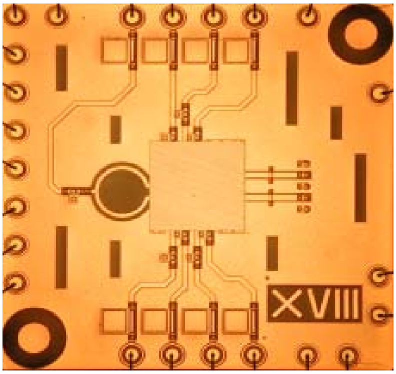

Fig. 6. Photograph of chip mounted on carrier, 5x5 mm^2.

IV. MEASUREMENT RESULTS

There are two VCO versions, one using regular Vt and one using low Vt transistors. Two samples of each VCO version have been measured. The RF output signal was measured on the carrier using Infinity probes from Cascade Microtech. A supply of 1.3 V was used for the VCO core and 1 V for the frequency doublers. The regular Vt VCO consumed 7.3 mW, with a core current consumption of 4.1 mA and 2 mA used in the doublers. The low Vt VCO consumed slightly less, 6.9 mW, with 3.9 mA and 1.8 mA in the doublers. A Rhode & Schwarz FSU50 Spectrum Analyzer was used to measure the frequency tuning characteristic and the buffer output power. The output power was between -19.6 and -16.5 dBm for the regular Vt VCO, and slightly lower at -20.8 to -17.6 dBm for the low Vt VCO. The frequency tuning characteristic of the VCO is shown in Fig. 7. As can be seen the tuning range is 20%.

The phase noise was measured using a Europtest PN9000 phase noise measurement system with an external down conversion mixer, Marki M90765. A signal generator, Agilent E8257D, was used to generate the LO signal to the mixer. In Fig. 8 the phase noise is plotted versus varactor control voltage, Vc. As can be seen it is below -107 dBc/Hz at 1 MHz offset over the tuning range for both VCO versions. The phase noise is also plotted versus offset frequency, for chip 3, in Fig. 9. The phase noise figure of merit, FOM, is between 188 and 192 dB over the tuning range.

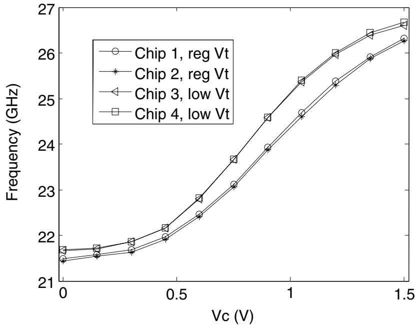

Fig. 7 Frequency tuning characteristic of the VCO.

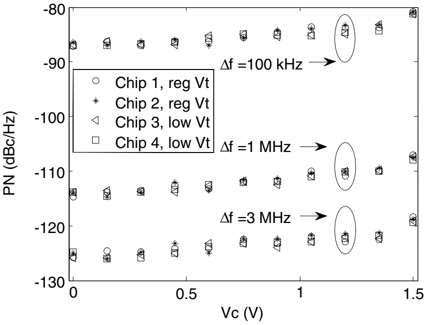

Fig. 8. Phase noise versus varactor control voltage.

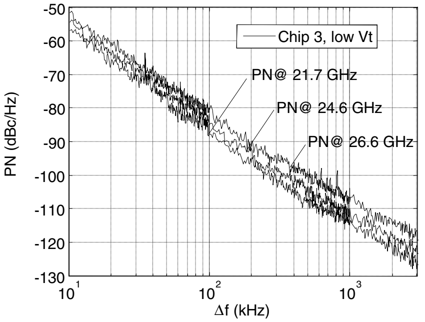

Fig. 9. Phase noise versus offset frequency, for three different frequencies, Chip 3.

TABLE I
SUMMARY OF SOME STATE-OF-THE-ART PUBLISHED VCOs

Ref.	Technology (µm)	F_C (GHz)	Tuning range (%)	P_{DC} (mW)	PN@1MHz* (dBc/Hz)	FOM (dB)	FOM_T (dB)
This work	CMOS 0.13 SOP	24.6	20	6.9	112	191	197
[4]	CMOS 0.13 SOP	28	17	5.3	109	191	195
[5]	CMOS 0.13	24.7	4.3**	24	111.6	186	178
[6]	CMOS 0.18	40	20**	27	100	178	184
[7]	CMOS 0.09 ***	18	8.3	4.2	120	199	197

* measured at centre frequency ** not continuously tuned ***post-processed

The oscillator frequency pushing was also measured, Fig. 10. There is approximately a 1.9 GHz and 1.8 GHz frequency increase for a supply voltage change from 1.5 to 1 V for the low Vt and reg Vt versions, respectively. This frequency shift is mainly due to the large varactors, and by referencing the control voltage to vdd instead of ground the pushing can be significantly reduced. In practise this can be accomplished by connecting the RC loop filter of the frequency synthesizer to vdd instead of ground.

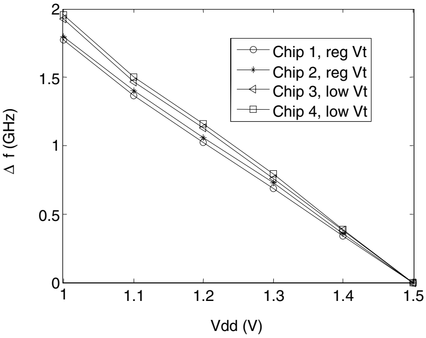

Fig. 10. Oscillator frequency pushing, Vc=0.75V.

The performance of some previously published state-of-the-art VCOs and this work is shown in Table I. The performance listed is measured at centre frequency. Also shown is the figure of merit taking tuning range into account, FOM_T, [3]. For this work it is between 194 and 198 dB over the tuning range. This is comparable to [4], which uses high-Q ferroelectric varactors.

V. CONCLUSION

The System-on-Package concept has been demonstrated for a microwave VCO. A high-Q symmetric inductor on a glass carrier is used in an LC-oscillator operating at 6 GHz. The VCO core and two frequency doublers, realized on a CMOS chip in 130 nm technology, was flip-chipped on the glass carrier. Thanks to the high Q value of the inductor on the carrier, excellent phase noise performance is achieved over a wide tuning range. It is below -107 dBc/Hz at 1 MHz offset over a 20% tuning range centered at 24.7 GHz, at a power consumption of 6.9 mW.

ACKNOWLEDGEMENT

The authors wish to acknowledge the support of Ericsson AB for financing this research as part of the MEDEA+ project 2T401 HI-MISSION. They would also like to thank Infineon Technologies for access to their CMOS technology, STMicroelectronics for access to their glass carrier technology, and the Knut and Alice Wallenberg foundation for financial support in building up the high frequency measurement laboratory.

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Paper VI

Paper VI

A 24-GHz Quadrature Receiver Front-end in 90-nm CMOS

M. Törmänen and H. Sjöland, “A 24-GHz Quadrature Receiver Front-end in 90-nm CMOS,” © 2009 IEEE. Reprinted, with permission, from *IEEE Proc. Asia Pacific Microwave Conference, APMC 2009*, Dec. 2009, Singapore.

A 24-GHz Quadrature Receiver Front-end in 90-nm CMOS

Markus Törmänen, Henrik Sjöland

Electrical and Information Technology, Lund University
Lund, Sweden
Markus.Tormanen@eit.lth.se
Henrik.Sjoland@eit.lth.se

***Abstract* — A 24 GHz quadrature receiver front-end in 90-nm CMOS is presented. It consists of a two-stage LNA, passive mixers, and a QVCO. The RF input is single-ended and is converted to differential form in the first LNA stage. The LNA has two bands of operation within the frequency range of the QVCO. The oscillator measures a centre frequency of 23.7GHz with a 7.2% tuning range, a worst case phase noise over the tuning range of -102 dBc/Hz at 1MHz offset, and a power consumption of 22mW. The front-end achieves; 18dB conversion gain, 8.9dB NF, -23dBm ICP1dB, -11dBm IIP3, 12dBm IIP2, and a power consumption of 42mW (excluding QVCO).**

***Index Terms* — CMOS integrated circuits, Frequency conversion, Microwave mixers, Microwave oscillators, Microwave receivers, Phase noise, Voltage controlled oscillators.**

I. INTRODUCTION

With an increasing demand for high data rates, wireless communication systems utilize more and wider bands at higher frequencies. The evolution of Si CMOS has made it a viable technology for cost sensitive radio transceivers operating at micro-wave and millimeter-wave frequencies. Publications have demonstrated high performance for silicon receivers in the Industrial, Scientific, and Medical (ISM) bands at 60 GHz [1]-[2], and 24 GHz [3]-[4].

In this paper we present measurement results of a quadrature receiver front-end consisting of a two-stage LNA, passive mixers, and a quadrature voltage controlled oscillator (QVCO). The performance of the QVCO has been measured separately. Differential topologies are known to have a higher linearity and better stability compared to single-ended topologies, at the cost of higher power consumption. The larger part of the front-end is therefore designed using differential topologies. However, the RF input signal to the chip is single-ended and is converted to differential form in a merged LNA and balun implemented in the first stage of the LNA [4]-[5]. This eliminates the need for an external RF input balun.

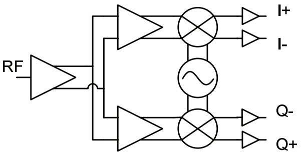

Fig. 1. Front-end block schematic.

II. CIRCUIT DESIGN

The block schematic of the front-end is shown in Fig. 1. The implementation consists of a two-stage LNA with separated second stages for the I and Q branches, passive double balanced mixers, a QVCO, and open-drain IF output buffers. The separated second LNA stages isolate the two passive mixers from each other, minimizing performance degradation due to mixer interaction.

A. LNA and Mixer

The first and second stages of the LNA are shown in Fig. 2(a), and Fig. 2(b), respectively. The first stage consists of a differential common gate (CG) stage with cascode devices for increased isolation. CG stages are known to provide wide band input match. Although the stage is differential, a single ended input is used, connected to one of the differential input terminals. Capacitive cross-coupling with capacitors C1 is used to increase the noise performance, and also to make the stage perform as a balun. The differential output signal is achieved through the capacitive cross-coupling and the coupling of the differential source inductor, La, [4]-[5]. A capacitive cross-coupling technique, with capacitors C2 and C3, is used also at the output. The purpose is to further increase the differential isolation by cancelling the currents due to the drain-source conductance for differential signals [4]. The output of the first stage is loaded by the inputs of the two second stages, one for I branch and one for Q, and is tuned to the operating frequency by the differential inductor Lb. The second stage consists of a differential common source (CS) stage with cascode devices and capacitive cross-coupling.

Both LNA stages have a small varactor in the resonator enabling two frequency bands of operation, denoted hereon after as (00) and (11). The varactors were sized for a 4% frequency difference between the two bands. The lower band, (00), is enabled when the varactor control voltages are at ground potential, whereas the upper band, (11), is enabled when the control voltages are at the same potential as the supply.

The two LNA stages provide sufficient gain for passive mixers to be used. In each branch, the output of the second LNA stage is loaded by the input impedance of a mixer and is tuned to the operating frequency by the differential inductor Lc. Inductor data for the LNA is shown in Table I. The passive double-balanced mixer is shown in Fig. 3(a). To facilitate measurements, the mixer outputs are connected to

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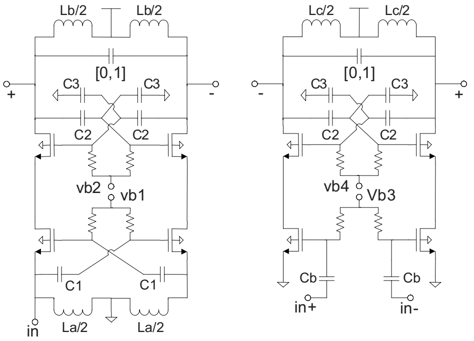
open-drain output buffers designed to drive 50 Ohms. The buffer schematic is shown in Fig. 3(b).

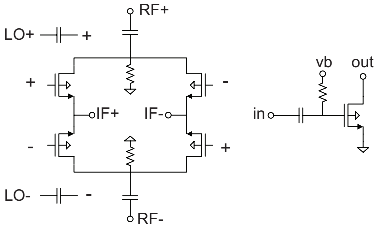
B. QVCO

The oscillator schematic is shown in Fig. 4. The QVCO consists of two differential LC oscillators coupled through capacitor Cc to oscillate in quadrature. The source node inductor, Ld, and the capacitor in parallel with the FET current source form a source node filter [6]. The filter is designed to not dominate over the capacitive coupling of the source nodes. As long as the oscillator works in the current limited region the second-order harmonics of the source nodes will be in anti-phase, and the two VCO outputs will have a quadrature phase relation to each other [7]-[9]. Inductor data for the QVCO is also shown in Table I.



(a) (b)

Fig. 2. LNA. (a) The input stage. (b) The second stage.



(a) (b)

Fig. 3. (a) Passive mixer. (b) Open-drain output buffer.

III. MEASUREMENTS

The circuits were implemented in a 90nm RF CMOS process. The layouts were designed as symmetrical as possible to minimize amplitude and phase errors. Die microphotographs of the complete front-end and a separate QVCO are shown in Fig. 5(a), and Fig. 5(b), respectively. The RF input can be seen on the left side of the front-end die. The supply, bias and IF output signals were wire bonded from the chip to a PCB. Decoupling capacitors were used both on chip and PCB for the supply and bias lines. The oscillator output signal pads are on the top side of the QVCO die, and the supply and bias pads on the bottom side.

TABLE I
INDUCTOR DATA

Inductor	Turns	Inductance (pH)	Q	fs (GHz)
La	3	554	18.4	74.1
Lb	2	300	20.8	95.6
Lc	2	476	22.2	75.3
Ld	2	245	14.5	111.8
Le	2	290	20.6	100.2

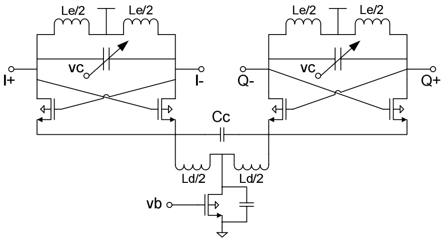
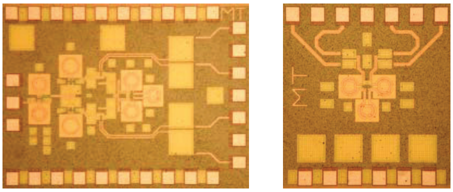


Fig. 4. QVCO schematic.



(a) (b)

Fig. 5. Die microphotographs. (a) Complete front-end including QVCO (1075μm x 800μm). (b) Separate QVCO (650μm x 720μm).

Two different samples of each front-end and QVCO have been measured. The measurements were performed using on-chip probes from Cascade Microtech. Infinity RF probes were used for the front-end RF input and the QVCO output signals, and a 6 needle DC Quadrant probe was used for the QVCO biasing.

The performance of the oscillator was measured at a power consumption of 21.6mW from a 1.2V supply for the QVCO core, and the open-drain buffers were biased to a drain voltage of 1 V and a current of 6.5mA per buffer. The tuning characteristic of oscillator can be seen in Fig. 6. As can be seen in the figure the tuning range is 7.2%. The output power from the buffers is between -1.8dBm and -0.6dBm over the tuning range. The phase noise was measured with a Europtest PN9000 phase noise measurement system together with an external down conversion mixer. The phase noise versus varactor control voltage is shown in Fig. 7. The legend of the figure includes the phase noise figure of merit (FOM), calculated at 1 MHz offset frequency using (1), where P is the power consumption of the oscillator in mW, f_0 the oscillation frequency, Δf the offset frequency, and $L(\Delta f)$ the phase noise at Δf .

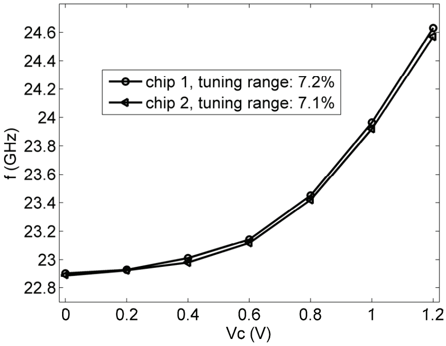


Fig. 6. QVCO frequency tuning charactesistic.

$$FOM = 10\log_{10}\left(\left(\frac{f_0}{\Delta f}\right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}} P}\right) \qquad (1)$$

A performance comparison with some previously reported QVCOs and this work is shown in Table II. The table also includes the figure of merit taking the tuning range into account, FOM_T (2).

$$FOM_T = 10\log_{10}\left(\left(\frac{f_0 \cdot tuning(\%)}{10 \cdot \Delta f}\right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}} P}\right) \qquad (2)$$

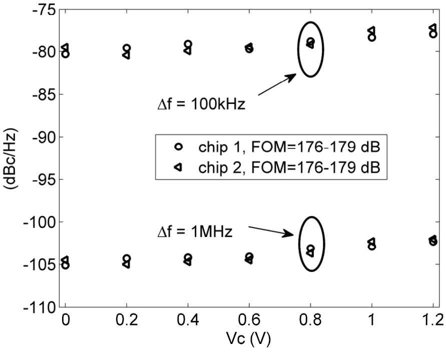
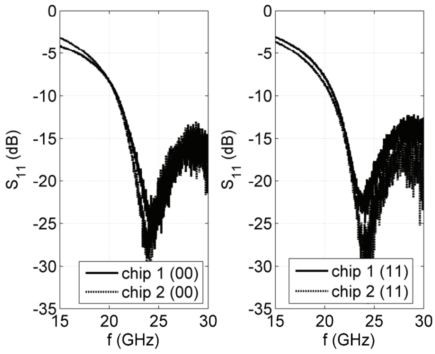


Fig. 7. Phase noise versus varactor control voltage.

The performance of the front-end was measured at a power consumption of 41.8mW from a 1.1V supply, excluding the power consumption of the QVCO. The open-drain buffers were biased to a drain voltage of 1 V and a current of 6mA per buffer. The measured input match, for both LNA bands, is shown in Fig. 8.



(a) (b)

Fig. 8. Front-end input match. (a) The (00) band. (b) (11) band.

The measured and de-embedded conversion gain and noise figure for an IF of 10MHz is shown in Fig. 9. In the (11) band the conversion gain and NF measures 18.1 dB and 8.9 dB, respectively, and in the (00) band the conversion gain and NF measures 15.7 dB and 9.5 dB.

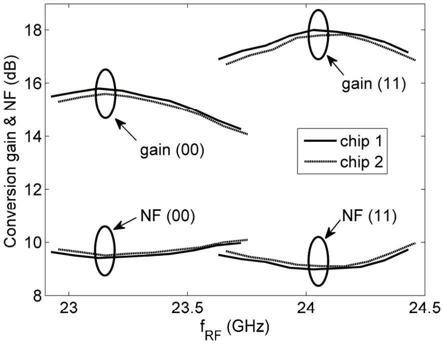


Fig. 9. Front-end conversion gain and NF.

The front-end linearity was measured and summarized in Table III, where the result is an average of the two measured samples. The linearity was measured using two-tone tests, one for third order and one for second order intermodulation. The tones were chosen such that the intermodulation product of interest occurred at an IF of 3MHz. A fifth order passive low-pass filter with a cut off frequency of 5 MHz was used when measuring the second order nonlinearity. This

TABLE II

SUMMARY OF SOME PREVIOUSLY REPORTED QVCOS AND THIS WORK

Ref.	Technology (μm)	Frequency (GHz)	P_{DC} (mW)	PN@1MHz* (dBc/Hz)	FOM (dB)	FOM_T (dB)
This work	CMOS 0.09	22.9-24.6	21.6	-102*	176	174
[10]	CMOS 0.13	24.19-25.25	24	-111.6*	186	178
[11]	CMOS 0.18	10.18-11.37	11.8	-118.7	188	189
[12]	CMOS 0.13	44.8-45.8	40	-98.9	176	163
[13]	SiGe 0.40	24.8-28.9	129	-84.2	152	156
[14]	SiGe 0.25	30.6-32.6	140	-97	166	162

* worst case phase noise over the tuning range

prevented the intermodulation of the first order IF output tones in the spectrum analyzer from affecting the measurement result.

TABLE III

FRONT-END LINEARITY

Band	CP_{1dB} (dBm)	IIP3 (dBm)	IIP2 (dBm)
(00)	-21.4	-10.3	13.7
(11)	-22.8	-11.2	12.1

The quadrature phase error of the complete front-end including QVCO was measured with a digital oscilloscope at an IF of 10MHz, Fig. 10. The quadrature error is below 6 and 8.5 degrees in the (00) and (11) band, respectively.

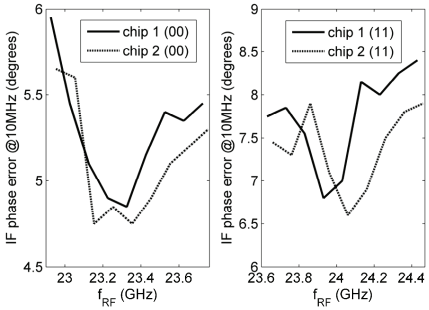


Fig. 10. Front-end IF quadrature phase error.

The oscillator leakage to the front-end RF input was also measured. The measured LO power at the RF port was below -84dBm over the VCO tuning range for both LNA frequency bands. This low value was achieved by using an on-chip oscillator, a symmetric layout, and cross-coupled cascodes in the LNA.

IV. CONCLUSION

A complete 24 GHz RF front-end featuring LNA, passive mixers, and QVCO, has been implemented in a 90-nm RF CMOS process. The LNA has two bands of operation within the tuning range of the QVCO. Measurement results for the complete front-end have been presented and the oscillator performance was also measured separately.

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