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RF and DC Analysis of Stressed InGaAs MOSFETs

Guntrade Roll, Erik Lind, Mikael Egard, Sofia Johansson, Lars Ohlsson, and Lars-Erik Wernersson

***Abstract*—A complete reliability study of the DC and RF characteristics for InGaAs nMOSFETs with Al_2O_3/HfO_2 dielectric is presented. The main stress variation at high frequencies is related to a threshold voltage shift, whereas no decrease is found in the maximum of the cut-off frequency and RF-transconductance. Constant gate stress leads to a charge build up within the gate oxide causing a threshold voltage shift. Furthermore, electron trapping at the drain side degrades the performance after hot carrier stress. The maximum DC-transconductance is reduced following constant gate bias stress, by an increase in charge trapping at border defects. These border defects at the channel/high-κ interface are filled by cold carrier trapping when the transistor is turned on, whereas they do not respond at high frequencies.**

***Index Terms*—high-κ, InGaAs, MOSFET, reliability, RF**

I. INTRODUCTION

III-V metal oxide semiconductor field-effect transistors (MOSFET) are promising candidates for future application that require low-power and high-frequency [1]. Due to the high electron mobility and large injection velocity, InGaAs n-channel transistors can reach high on-currents at low source-drain voltages [2]. Major process improvements, including high-κ to channel interface quality and source/drain series resistance have been made in the last few years [2]–[4]. Currently, there are only a few investigations of relevant reliability issues [5]–[7]. In this work, we investigate the key degradation problems of raised source/drain InGaAs transistors after hot carrier injection and bias temperature instability. A complete degradation study of the DC- and RF device characteristics is presented.

II. DEVICES AND MEASUREMENT

Figure 1(a) shows the basic structure of the investigated InGaAs nMOSFET. A SiO_2-like dummy gate, on top of the not intentionally doped 10-nm-thick $In_{0.53}Ga_{0.47}As$ channel, was used as hard mask for epitaxial MOCVD regrowth. The Sn doping concentration in the 40-nm-thick $In_{0.6}Ga_{0.4}As$ source/drain is about $5{\cdot}10^{19}$cm^{-3}. After dummy gate removal with a buffered oxide etch, the sample surface was treated with $(NH_4)_2S$ (10%) for 20min. The gate oxide was deposited by ALD using 10 cycles of TMA and H_2O at 300°C and 40 cycles of TDMAHf and H_2O at 120°C. The Al_2O_3 and HfO_2 layer have a thickness of approximately 1nm and 4.5nm. The metal electrodes were deposited by evaporation and a post metallization anneal at 400°C under N_2 finalized the process. The measured equivalent oxide thickness of this structure is 2.3nm. The total width of the two gate fingers is 15μm. A detailed description of the process can be found in [4].

Direct current (DC) and high frequency (RF) measurements were performed using a Keithley SMU and an Agilent PNA network analyzer with a frequency range of 40MHz to 67GHz. For *S*-parameter calibration, the off-chip load-reflect-reflect-match method and on-chip de-embedding short and open structures were used. Source- and drain resistances of 17Ω were determined using the channel resistance method. Constant DC stress at room temperature was applied and subsequently I_dV_g and *S*-parameters were measured. The I_dV_g was measured from -1V to +1V after positive stress and from +1V to -1V after negative stress. An initial recovery occurs at the starting bias of the IV sweep. The I_dV_g measurement was repeated after the S-parameter measurement, showing no significant further recovery due to the parameter determination. The recovery process was not analyzed in this study. The threshold bias was determined taking the point and slope of the maximum transconductance and extrapolating the linear function to zero current. Especially the increase in transconductance (g_m) with frequency (f), deduced from the RF measurements (Y_{21}-parameter), was analyzed (Fig. 1(b)). The $g_m(f)$ dependence in high-κ InGaAs MOSFETs is generally modeled by cold carrier trapping into the oxide [8]–[10]. A similar model is used to explain the small stable I_dV_g hysteresis found also in early high-κ/silicon devices [11]. Using the g_m-frequency increase, the amount of charges trapped at border defects (N_{bt}) and tunneling depth (x_m) was calculated based on an elastic tunneling model (eq. 1) [9], [10]. It should be noted that the model assumes a constant capture cross section and neglects inelastic trapping, as used in recent Si/SiO_2 stress models [12].

$$\begin{aligned} N_{bt}(x_m) &= \frac{(C_s+C_{ox})\cdot g_{mi}}{e^2\lambda g_m^2(f)}\cdot\frac{\partial g_m(f)}{\partial ln(2\pi f)} \\ x_m &= \lambda\cdot ln(f_{mi}/f) \end{aligned} \quad (1)$$

Here, e is the elementary charge, g_{mi} is the transconductance at a frequency (f_{mi}) high enough that g_m is constant, C_s and C_{ox} are the semiconductor- and the oxide capacitance, respectively. For the tunneling parameters, λ=1.6$\cdot10^{-8}$ cm was chosen [10]. The measured trap density is also depending on the energy which is determined by the band bending at a certain gate bias and threshold bias (V_g-V_{th}).

III. RESULTS AND DISCUSSION

Figure 1(b) illustrates the change in measured RF characteristic due to positive bias temperature stress (PBTI). The *RF*-g_m ($\approx$ real part of Y_{21}) is plotted taking the threshold shift (ΔV_{th}=0.095V) after PBTI into account. The $g_m(f)$ dispersion increases after stress. Figure 1(b) shows that the RF-g_m curves overlap above 20GHz, which shows that they are only shifted by ΔV_{th}. The same trend is valid after negative bias temperature stress (NBTI). The maximum of the cut-off frequency (f_t), which is directly related to the g_m maximum

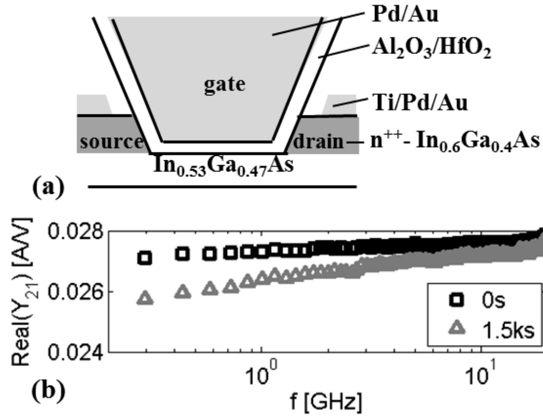

Fig. 1. The schematic structure of the high-κ InGaAs MOSFETs with raised source/drain structure is shown in (a). The measured RF transconductance ($\approx$ Real(*Y21*)) for V_G-V_{th}=0.28V at 0.525V drain bias and 25°C for a typical nMOSFET (L_{Gate}=50nm) is shown (b). The increase of transconductance with the frequency before and after 3V PBTI gate stress are compared.

[13], is constant and shifted to higher or lower gate biases for PBTI - and NBTI stress, respectively (Table I).

Applying BTI stress leads to a degradation in V_{th} and a decrease in the maximum transconductance (g_{max}) under DC conditions (Table I, Fig. 2). The degradation follows a power law. The time slope (*n*) is determined with an error due to the initial recovery [14]. The time slope of the V_{th} degradation is stress bias independent within small variations. Applying a positive gate stress leads to a V_{th} increase with a time slope of 0.25±0.06 independent of the gate length (Fig. 2(a)). Applying a negative gate stress leads to a V_{th} decrease with a time slope of 0.17±0.04 (Fig. 2(a)). The V_{th} reduction gets worse, with decreasing gate length (Table I), due to a higher initial trapping

TABLE I
KEY PARAMETER SHIFT AFTER STRESS

Unstressed V_D=0.525V			
	V_{th} [V]	*DC-g_{max} [mS/μm]	**max(f_t)* [GHz]
L_{Gate}=50nm	-0.04±0.14	0.98±0.14	163±40
L_{Gate}=200nm	0.12±0.01	0.79±0.01	100±11
PBTI V_G=V_{Stress}, V_D=V_S=0V, 1500s, 25°C, L_{Gate}=50nm			
V_{Stress} [V]	Δ V_{th} [mV]	Δ g_{max} [mS/μm]	Δ f_t [GHz]
2	+70	-0.08	+2
3	+84	-0.19	**o.r.
NBTI V_G=V_{Stress}, V_D=V_S=0V, 1500s, 25°C			
L_{Gate}=50nm			
V_{Stress} [V]	Δ V_{th} [mV]	Δ g_{max} [mS/μm]	Δ f_t [GHz]
-2.5	-306	-0.15	+10
-3	-403	-0.19	+6
L_{Gate}=200nm			
V_{Stress} [V]	Δ V_{th} [mV]	Δ g_{max} [mS/μm]	Δ f_t [GHz]
-3	-273	-0.13	-1

Unstressed V_D=0.525V			
	V_{th} [V]	*DC-g_{max} [mS/μm]	**max(f_t)* [GHz]
L_{Gate}=100nm	0.05±0.04	0.95±0.03	156±21
HCI V_G=V_{Stress}, V_D=1V, V_S=0V, 1500s, 25°C, L_{Gate}=100nm			
V_{Stress} [V]	Δ V_{th} [mV]	Δ g_{max} [mS/μm]	Δ f_t [GHz]
1	+209	+0.09	+16

*Maximum measured f_t and extrinsic DC-g_{max} are given.
**Maximum f_t outside S-parameter measurement range (0.1V to 0.8V).

(*C*). The measured time slope is independent of gate length. This indicates that the density of charges initially trapped from the transistor contacts is higher than the density of charges trapped from the middle of the channel during stress. Charges at the nMOSFET edges have a higher influence on the barrier height, which determines the V_{th}, for short channel transistors. A higher trapping rate at the gate edges can be related to the high leakage current flow from the gate to the regrown contacts under NBTI conditions and a reduced oxide quality/thickness at the sidewall of the raised source/drain transistor. The V_{th} shift is measured at both high and low frequencies. Different models are available to explain the build up of permanent charges or charges with long detrapping time constants ($\geq$1d) after BTI stress in high-κ silicon technology. Electron trapping inside the gate stack is a common theory for PBTI degradation [14], the reaction-diffusion model for H bond breaking or the switching oxide trap model are used to explain the NBTI reliability [12], [15].

The time slope for the DC-Δg_{max} after PBTI stress is similar to that of the ΔV_{th} increase with an average of 0.27±0.03 (Fig. 2(b)). This indicates similarities in the degrading process. After NBTI stress the time slope (*n*) of the DC-g_{max} degradation decreases from 0.8 to 0.2 with increasing stress bias from -2.5V to -3.5V (Fig. 2(b)). The time slope variation could indicate a strong saturation effect [15]. High frequency results show no g_{max} and consequently nearly no f_t degradation after both PBTI and NBTI (Table I). The amount of trapped charge in border defects (N_{bt}) extracted from the g_m frequency dispersion increases with constant gate stress (Fig. 3). Charge trapping at border defects occurs during transistor on-state at frequencies below 20GHz (Fig. 1(b)). This leads to the decrease in DC-g_{max} with stress. The increase in charge trapping can possibly be explained by creation or an activation of defects, due to diffusion or charging processes near to or at the high-κ/InGaAs interface after stress. The PBTI results are in agreement with other studies on InGaAs transistors with Al_2O_3 gate [5], [7], in which the creation of permanent traps is described. Further investigation will give a clearer insight in the charge trapping and defect creation process at the S passivated InGaAs/Al_2O_3 interface after BTI stress and its time constants.

Hot carrier stress (HCI) leads to a large V_{th} increase, as compared to PBTI results (Table I, Fig. 2(a)). In our earlier work, we found a current flow caused by impact ionization at large drain biases [4]. High energy channel electrons and possibly secondary electrons created by impact ionization are injected at the drain side [16] and cause the positive V_{th} shift. Also, the high-κ quality/thickness towards the drain contact is essential for HCI reliability. The measured time exponent (n) of the V_{th} shift is between 0.1 and 0.2. No DC-g_{max} decrease is found if a low stress potential of 1V at the gate is applied (Table I). The number of defects available for cold carrier trapping in the channel is not increased, possibly because the HCI damage is concentrated at the drain edge for the raised source drain structure. The RF results further show a slight increase in f_t (Table I), which could be related to changes in source/drain resistance. The transconductance results after stress agree with the observation made for bulk

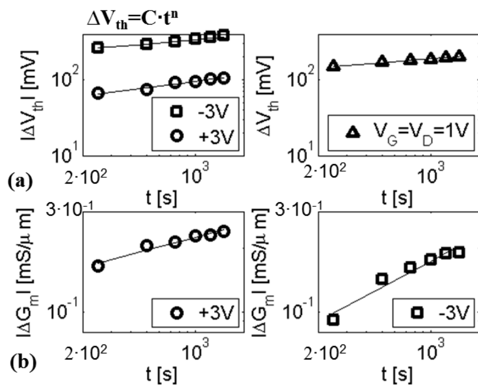

Fig. 2. ΔV_{th} with stress time at 25°C is plotted in (a). To the left, the results after BTI stress for a 50nm long MOSFET with a time exponent (n) of 0.18 and 0.27 for NBTI and PBTI. To the right, the results after HCI stress for a 100nm long transistor with n of 0.16. The DC-Δg_{max} is plotted in (b). For PBTI at +3V, n is determined to be 0.2 (left) and for NBTI at -3V, n is measured to be 0.4 (right).

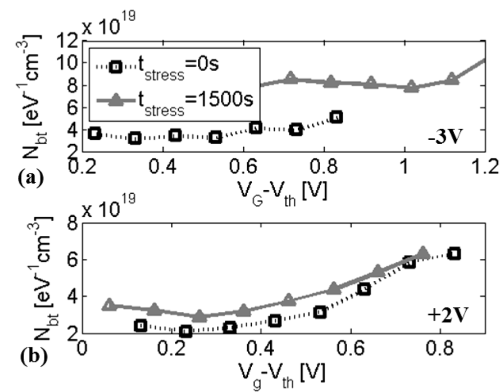

Fig. 3. Charges trapped at border defects $3\dot{A}$ from the semiconductor/high-κ interface before and after a BTI stress for a typical transistor (L_{Gate}=50nm) at 25°C is shown. A negative and positive gate stress of -3V (a) and +2V (b) is applied.

InGaAs MOSFET with Al_2O_3 dielectric [6], but the V_{th}-shift was observed in both the subthreshold and inversion region for the S passivated InGaAs/Al_2O_3/HfO_2 gate oxide.

IV. Conclusion

The reliability characteristics of a raised source/drain InGaAs nMOSFET with high-κ dielectric are investigated. Prestress border defects, available for cold carrier trapping, are responsible for transconductance frequency dispersion and current hysteresis. An increase in cold carrier trapping to border defects and a decrease in maximum DC transconductance with both positive and negative gate stress is observed. The threshold bias shift under constant positive and negative gate stress is mainly caused by charge accumulation, possibly deeper within the gate oxide. Those charges do not influence the maximum transconductance measured at high frequencies. The threshold bias related transconductance shift is the main factor for cut-off frequency variation. Hot carrier stress at a gate bias of 1V does not effect the cold carrier trapping when the transistor is turned on, but electron trapping increases the threshold voltage.

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