1/f-noise in Vertical InAs Nanowire Transistors

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1/*f*-noise in Vertical InAs Nanowire Transistors

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***Abstract*—The material quality at high-k interfaces are a major concern for FET devices. We study the effect on two types of InAs nanowire (NW) transistors and compare their characteristics. It is found that by introducing an inner layer of Al_2O_3 at the high-κ interface, the low frequency noise (LFN) performance regarding gate voltage noise spectral density, S_{Vg}, is improved by one order of magnitude per unit gate area.**

Keywords—1/f-noise; high-κ; nanowire; InAs; FET

I. Introduction

InAs nanowire (NW) FETs are a good candidate for future RF electronics, promising both low power dissipation and high speed operation [1][2][3]. To verify the feasibility in the technology, however, it is vital to fabricate high performance devices. By utilizing different evaluation methods, the delicate balance of different processing conditions can be evaluated; for a FET, good control over the interfaces is essential. Besides measurements of the *I-V* characteristics, it is of interest to determine the trap density and one common method is measurement of low frequency noise (LFN). In this abstract, we investigate the differences in LFN as well as I_{ON}, *SS*, *DIBL*, and other metrics for devices fabricated with two different high-κ films, HfO_2 and Al_2O_3/HfO_2, implemented for DC and RF operation, respectively [4][5].

II. Fabrication

A. DC Devices

InAs NWs are grown on a doped InAs substrate. Seed Au particles defined with electron beam lithography (EBL) determines diameter, here 40 nm, and placement. The growth is made in a metal-organic-vapor-phase-epitaxy (MOVPE) growth chamber at 420 °C and with a Sn dopant molar fraction of $3.49 \cdot 10^{-8}$. The high-κ film is deposited both before and after the fabrication of the first separation layer. The two high-κ films, consisting of HfO_2, is deposited with atomic layer deposition (ALD) at 250 °C and is in total 7 nm, with an EOT of 1.5 nm. The source-gate separation layer consists of a 30 nm evaporated SiO_x film. During evaporation, the sample is tilted so that there will be a buildup of flakes on sides of the NWs, which can be removed in a wet-etch, leaving the lateral layer intact. This process is also used for the evaporated Ni gate and the film thickness sets L_G = 35 nm (Fig. 1a). The evaporated top metal is elevated with a spin-on polymer resist which is back etched.

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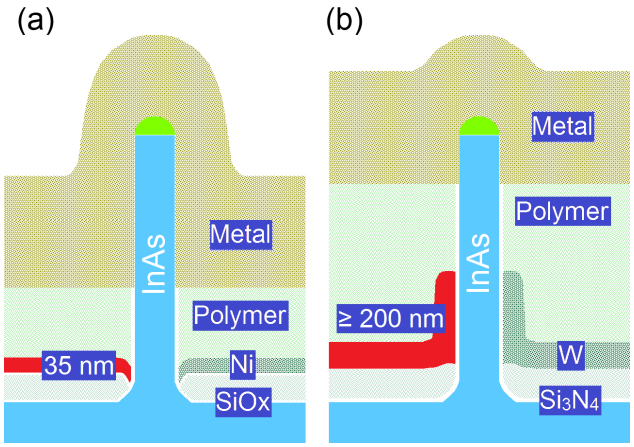

Fig. 1. (a) The DC device structure with specified materials and L_G = 35 nm. (b) The refined, RF device structure with specified materials and $L_G \geq 200$ nm.

B. RF Devices

To accommodate RF transistors and circuits, the DC device structure was refined; devices are placed on an isolating substrate. Also, targeting high yield, the gate process is exchanged. The processing flow chain begins with growth of a 300-nm-thick InAs layer on top of a Si substrate to mitigate growth of InAs NWs, and also, to act as contact mesa structure after being etched out. NWs with a diameter of 45 nm are grown at 420 °C and with a Sn dopant molar fraction of $1.07 \cdot 10^{-7}$. For both devices, the NWs are homogenously doped. The high-κ film is deposited with ALD and consists of 0.5 nm Al_2O_3 at 250 °C and 6.5 nm of HfO_2 at 100 °C, with a total EOT of 1.8 nm. The W-gate is sputtered with a layer thickness of 60 nm and is separated from the source mesa with a 60 nm Si_3N_4 film deposited with plasma enhanced chemical vapor deposition (PECVD) in a preceding step. The nitride film is removed from the sides of the NWs with a dry etch. The gate length is set by a defining polymer and a dry etch, giving $L_G \geq$ 200 nm (Fig. 1b). The top metal is sputtered and is elevated by a spin-on polymer resist that is back etched.

III. Measurement and Results

Devices are measured with a Keithley 4200 SCS and for the LFN characterization, a Lock-in amplifier and a LNA are added to the setup. The 1/*f*-noise is measured for V_{DS} = 50 mV and f = 10 Hz. Obtained data from measurements of normalized current noise spectral density, S_{Id}/I_{DS}^2, is shown in

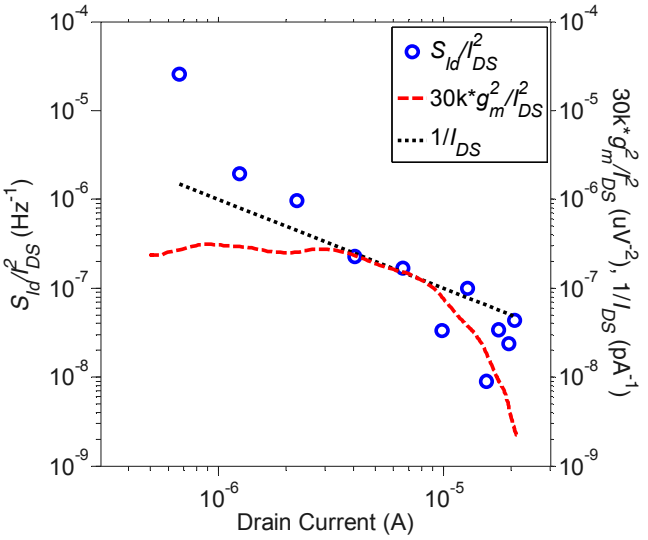

Fig. 2. S_{Id}/I_{DS}^2 plotted versus I_{DS} at V_{DS} = 50 mV and f = 10 Hz. Two curves have been added, g_m^2/I_{DS}^2 and $1/I_{DS}$, where the shape of the curves are indicative for LFN dominated by number fluctuations and mobility fluctuations, respectively. The factor of 30k was multiplied with the g_m^2/I_{DS}^2 curve to position it relevant to the S_{Id}/I_{DS}^2 data.

Fig. 2. Two curves have been added, g_m^2/I_{DS}^2 and $1/I_{DS}$, respectively. All measured performance metrics for the DC device and the refined RF device are benchmarked in Table I.

IV. Discussion

Analyzing the data in Fig. 2, the S_{Id}/I_{DS}^2 seems to be dominated by mobility fluctuations in the subthreshold region, whereas number fluctuations better explain the data around threshold. The observed increase in S_{Id}/I_{DS}^2 for large I_{DS} could be explained by noise generated by a combination of mobility fluctuations and series resistance. This interpretation differs from the analysis of data measured for the DC devices, where the entire I_{DS} range could be explained by number fluctuations stemming from oxide traps [4]. Still, the shown data in Fig. 2 is representative as other RF devices on the same batch sample show similar tendencies and have comparable gate voltage noise spectral density, S_{Vg}, ranging between 310 - 410 $\mu m^2 \mu V^2/Hz$. Comparing S_{Vg} and S_{Id}/I_{DS}^2 for the two different high-κ devices, the improvement is one order of magnitude for S_{Vg} and about two orders of magnitude for S_{Id}/I_{DS}^2. As the numbers given for the S_{Vg} are normalized to the gate area, the difference in the amount of charges for different channel lengths is accounted for. The data suggest that there is a lower interface trap concentration with the introduction of an Al_2O_3 film and the improvement can possibly be traced to a reduction in sub-oxides [6]. The reason for the SS degradation can be explained by the increase in doping and the inability to deplete the channel all the way through. This is partly the explanation for the increase in DIBL as well, where the undepleted carriers form a parallel parasitic resistance. The DIBL is also likely to be caused by other effects such as band-to-band tunneling. To accommodate the issue concerning the channel depletion, the wire diameter, D_{NW}, should be scaled and it has been shown that scaling the diameter to 28 nm improves the off characteristics (SS = 80/140 mV/V for V_{DS} = 0.05/0.5 V) keeping other parameters constant (although EOT = 1.3 nm) [5]. To maintain good on-performance when scaling, however, it is necessary to address the increase in series resistance; this could be done by, for example, introducing a heterogonous doping profile and/or thinning down the separation layers [3].

TABLE I. Performance Metrics

	HfO2	***Al_2O_3 / HfO_2***
D_{NW}	40 nm	45 nm
L_G	35 nm	200 nm
EOT	1.5 nm	1.8 nm
Doping	~$1 \cdot 10^{18}$ cm^{-3}	~$3 \cdot 10^{18}$ cm^{-3}
$I_{ON}^{a,b,c}$	104 mA/mm	670 mA/mm
R_{ON}^{b}	3.7 Ωmm	0.33 Ωmm
$g_m^{b,c}$	227 mA/mm	1190 mA/mm
SS^{c}	110 mV/decade	500 mV/decade
$DIBL^{c}$	100 mV/V	320 mV/V
S_{Vg}	5700 $\mu m^2 \mu V^2/Hz$	410 $\mu m^2 \mu V^2/Hz$
S_{Id} / I_D^2	$7.3 \cdot 10^{-7}$ Hz^{-1}	$8.9 \cdot 10^{-9}$ Hz^{-1}

a. $V_{DS} = V_{GS} - V_t = 0.5$ V

b. Values normalized to the NW circumference, $W = D_{NW} * \pi$

c. Measured at $V_{DS} = 0.5$ V

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