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A DDC LOOP BETWEEN LUND AND KIRUNA
FOR CONTROL OF AN ORE CRUSHER

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TILLHÖR REFERENSBIBLIOTEKET

UTLÄNAS EJ

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Lund Institute of Technology

Division of Automatic Control

A DDC LOOP BETWEEN LUND AND KIRUNA FOR CONTROL OF AN
ORE CRUSHER.

L Andersson U Borisson R Braun R Syding

ABSTRACT.

This report describes an arrangement for controlling a crusher at the ore-crushing plant in Kiruna from a process computer in Lund. The data transmission was done with modems and a public telephone line. A description is given of the special process interface that was constructed. The organization of the software is discussed and program listings are presented.

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1. INTRODUCTION.

The DDC loop described here was constructed for a feasibility study of self-tuning control and remote processing. The controlled process was a crusher at the ore-crushing plant in Kiruna belonging to LKAB. The PDP 15 computer at the Division of Automatic Control, Lund, was connected to the crushing plant via a public telephone line, Fig. 1.1. The data transmission distance was about 1800 km.

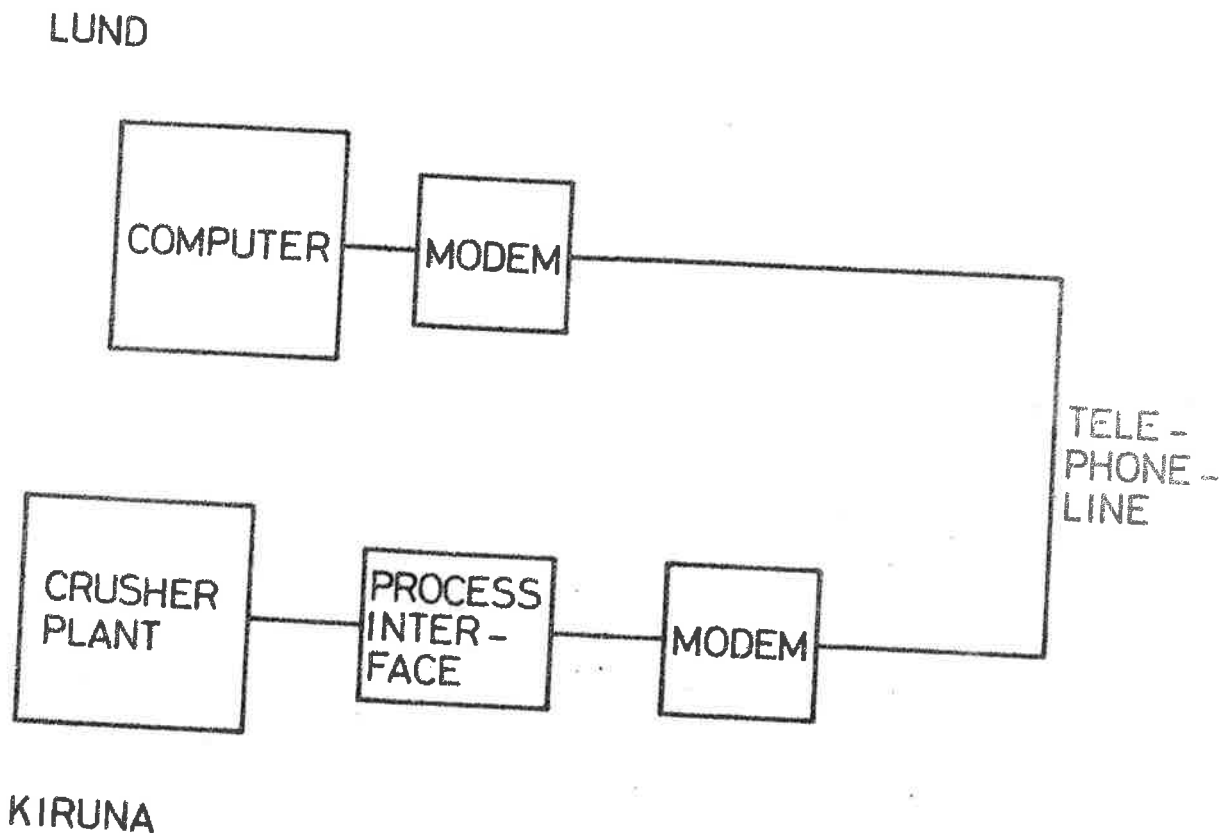


Fig. 1.1 - Schematic figure of the DDC loop between Lund and Kiruna.

Data entered and left the computer via an ordinary teletype interface. Low speed modems were used for the transmission. The process interface includes a remote control terminal transducing digital signals to analog signals.

This report is organized as follows:

In Section 2 the crushing plant is described. The modems are discussed in Section 3 and the process interface in Section 4. The software for the computer is described in Section 5. A detailed description of the remote control terminal is found in Appendix I. Listings of the programs are given in Appendix II.

2. DESCRIPTION OF THE PROCESS.

The ore crushing plant in Kiruna (Kiruna Finkrossverk) is the link between the underground mine (Kiirunavaara) and the sorting plant (Kiruna Sovringsverk).

In the crushing plant the ore is crushed to lumps of maximum grade of 25 mm, in order to deliver a product adapted to the following sorting and separation process in the sorting plant and adapted to the metallurgical processes of the customers.

The crushing plant consists of six identical crushing lines, each including one crusher driven by a 200 kW electrical motor and two screens, Fig. 2.1.

The ore enters the crushing line on electromechanical feeders, which are controlled to feed enough material to maintain constant power withdrawal from the crusher motor. Then it passes the first screen, if not already undersize, on its way to the crusher. The crusher leaves some oversize lumps which will pass the second screen to be recycled to the crusher.

To maintain constant power withdrawal it is necessary to vary the ore inlet to compensate for disturbances in crushability and size as well as for changes of the crusher depending on wear down.

The crushability depends mainly on the waste rock content. The more waste rock the ore contains, the more specific crusher work is needed. Sometimes about 75% of the ore may be undersize at the first screening, another time only about 25%

These disturbances also affect the process parameters and thus indicate a need for tuning the regulator according

to the disturbances in the ore inlet and to the crusher condition. A wrongly tuned regulator will give rise to bad performance of the system, resulting in great fluctuations in the power signal.

Because of the great deadtimes of the system, 42 seconds between crusher and feeder and 74 seconds in the recycle loop, compared with the time constants of the crusher and the feeders, each around 20 seconds, a regulator that takes account of the deadtimes is preferable.

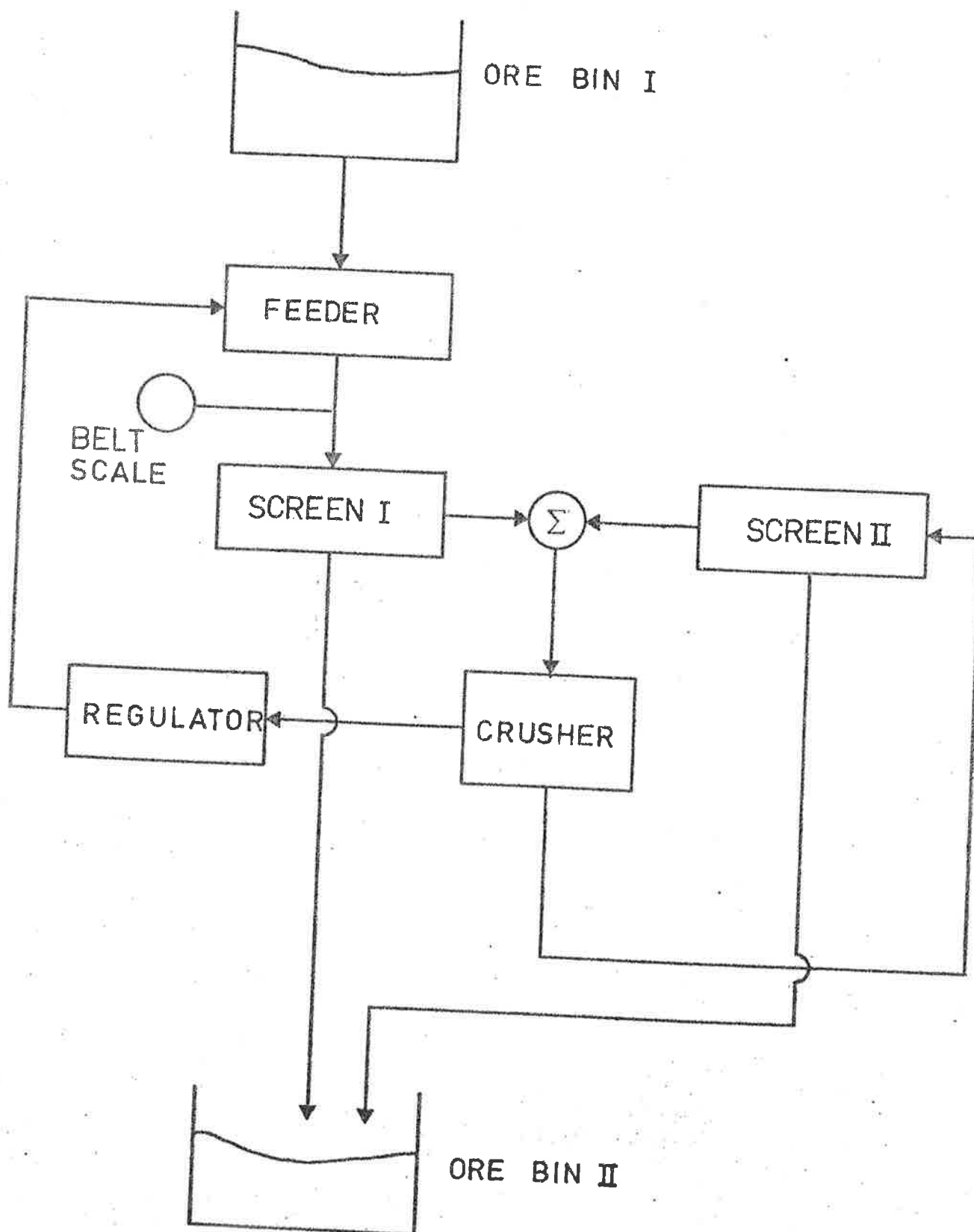


Fig. 2.1 - The flow scheme of Kiruna Finkrossverk.

3. MODEMS.

3.1. General Description.

The primary function of modems is to make the digital signals from a computer or a computer terminal transmissible over telephone lines. This is accomplished by a modulation process where the DC levels used for logical signals are changed into audio frequencies between 300 and 3400 Hz. Similarly by a demodulation process the audio frequencies from the telephone line are reconverted into logical DC levels.

3.2. Transmission Speeds.

The transmission rates possible with modems over telephone lines range between zero and 9600 bits/sec.

Low speed modems - up to 200 bits/sec. - may transmit in full duplex, i.e. in both directions simultaneously, through one line in the public switched network.

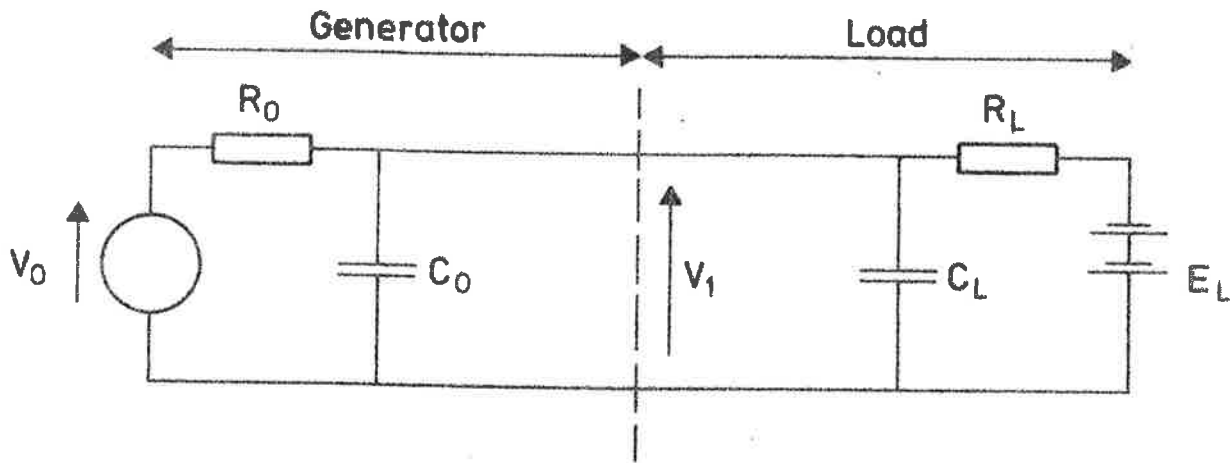
Medium speed modems - 600-1200 bits/sec. - may still use the public switched network, but transmission is possible in only one direction at a time.

High speed modems - 2400-9600 bits/sec. - must use leased lines and can transmit in only one direction at a time.

3.3. International Standardization.

The properties of modems are governed by recommendations issued by CCITT, Comité Consultatif International de Telephone et Telegraph. These recommendations describe the signals that appear at both sides of the modem. The only signals the user needs to be concerned with, however, are those at the data processing side, either before modulation or after demodulation. A brief description of the standardized signals is given in Fig. 3.1, which shows an interchange equivalent circuit.

Apart from data the modem also receives and sends certain control signals such as "Request to send", "Ready to send", etc. These signals may either come from the data processing equipment or from a special control unit provided with the modem. For a detailed description, see [1].



$$|V_0| < 25 \text{ V}$$

R_0, C_0 not specified explicitly

$$3 \text{ k}\Omega < R_L < 7 \text{ k}\Omega$$

$$C_L < 2.5 \text{ nF}$$

$$|E_L| < 2 \text{ V}$$

$$\text{For } E_L = 0 \quad 5 \text{ V} < |V_1| < 15 \text{ V}$$

$$\text{For binary 1} \quad V_1 < -3 \text{ V}$$

$$\text{For binary 0} \quad V_1 > +3 \text{ V}$$

Fig. 3.1 - Interchange equivalent circuit.

4. PROCESS INTERFACE.

The process interface consists of a multichannel Data Logger and a Remote Control Terminal. The Data Logger measures the ore flow signal from the belt scale immediately before the first screen, the control signal from the current transducer and the power signal from the power transducer. These measurements are formatted and then go to a Teletype. They also go to the Remote Control Terminal, where they are converted to suit the modem input (see Sec. 3). The process connections are shown in Fig. 4.1.

In the other direction the signals from the modem go to the Remote Control Terminal, which performs a serial-to-parallel conversion and a D/A conversion. The resulting analog signal is the control input to the process.

To give the computer access to the process a switch was placed before the feeder actuator. It was then possible to choose between remote digital control and local analog control.

The Data Logger, the Remote Control Terminal and the modem were placed in the Kiruna office about 2000 m from the ore crushing plant. The communication between the control room at the plant and the office building was maintained with four local telephone lines.

To permit a coarse check of the experiment conditions a three channel recorder was connected in parallel with the Data Logger. The power signal, the ore flow to the first screen and the control signal were recorded.

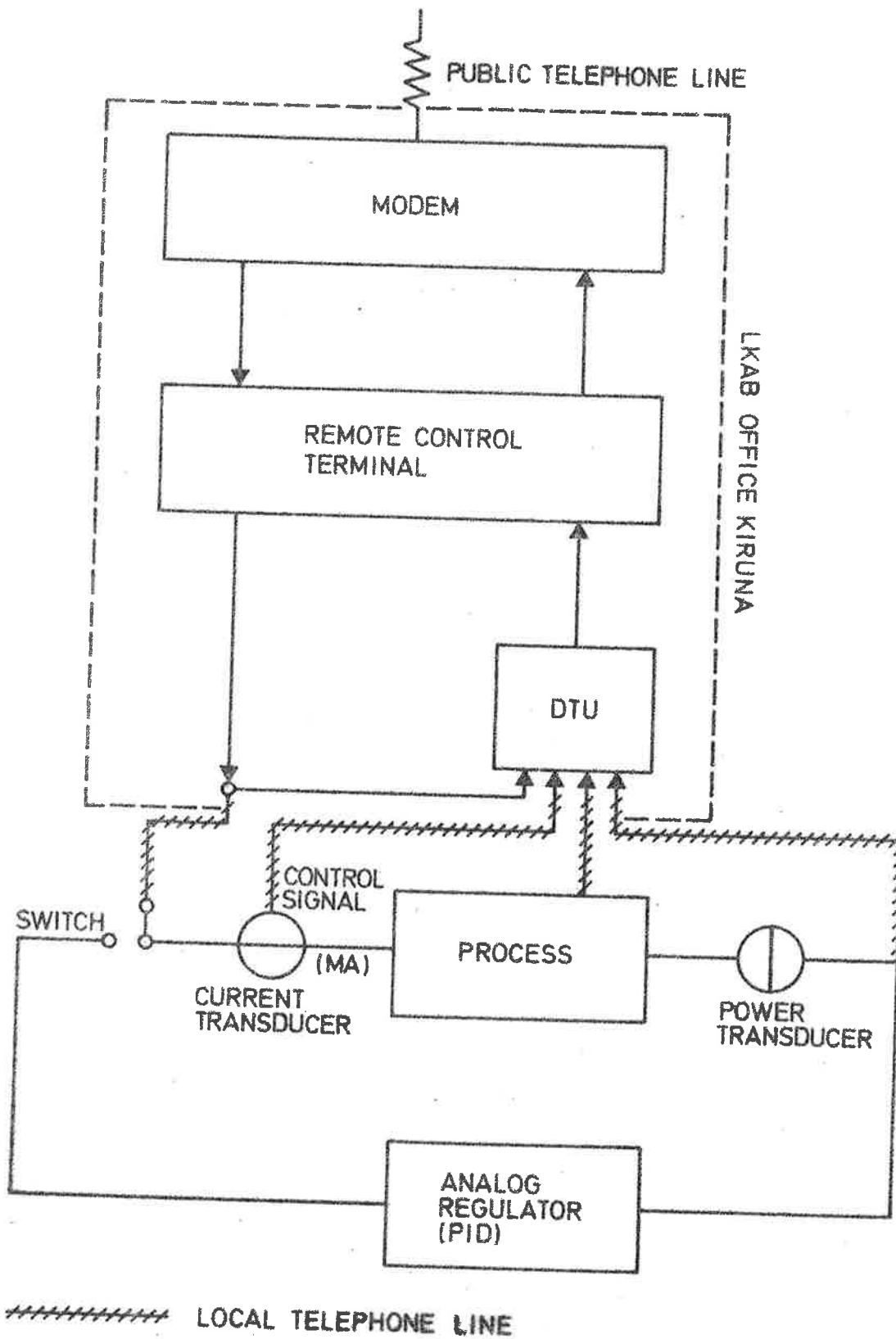


Fig. 4.1 - Process connections in Kiruna.

5. COMPUTER SOFTWARE.

First the regulator programs will be discussed. Then a small modification of the teletype handler in the standard version of the real time monitor will be described.

5.1. Programs.

The programs run under the real time monitor RSX. The core memory is divided into partitions and each program, "task", runs in a preselected partition. The following tasks were used in the experiments:

Name	Function	Partition
INIT	Initializes the regulator	PUSER
REGUL	Receives data and computes the control signal	PPRUS
PRINT	Prints data on line printer	PUSER
TAPE	Writes data on tape	PUSER
SEND	Sends the control signal to Kiruna	PIRUS

Listings of the programs are given in Appendix II. Some of the standard variables in BLANK COMMON were used. It was then possible to use the library program SET to initialize the variables and to change values of the variables during the experiments.

The structure of the self tuning regulator was specified in the task INIT. In this task it was also given start values for the regulator parameters, set point for the process and limits for the control signal. The task was executed at the start up and could then be executed at any time during the experiment, e.g. to make a set point adjustment.

In the beginning of task REGUL the data from Kiruna were received. A teletype input/output (TT2) was used for the data communication. Data were read in free format. Normally the teletype handler sends back the same data as it receives. As this was not desired, a small modification of the teletype handler was made, so that the data were sent to TT1 instead of TT2. In this way automatic logging was obtained on TT1. In Sec. 5.2 the modification is described in detail.

When data had been received, the control signal was computed. Then task SEND was requested. The tasks PRINT and TAPE could also be requested from REGUL, which was core resident all the time.

The task PRINT logged process variables and results on the line printer. The task TAPE stored the same information on DEC tape. The data were written in such a way that standard programs could be used for plotting and statistical analysis.

The task SEND, which was written in assembler, transferred the computed control signal to Kiruna by making a write instruction directed to TT2. It was possible to let SEND execute several times during a sampling interval to reduce the problems occurring if one value was lost. The sampling interval was 20 seconds.

5.2. A Monitor Modification.

The Teletype handler of the RSX always assumes that the TTY:s connected to the computer operate without local copy, i.e. when a key is depressed the character is sent to the CPU, but it is not printed locally. Obviously this would not be practical for the operator, and therefore the Teletype handler "echoes", i.e. sends back, any character that it receives. For the particular application at hand this was undesirable, since every character received by the remote control terminal corresponds to a unique output voltage.

Every time the CPU receives an interrupt from a Teletype keyboard it goes through a skip chain to determine which TTY that caused the interrupt. If the flag is found at e.g. the third entry down the list, the program goes to another list of output instructions and executes the third entry, which, of course, normally is an output to the same TTY that caused the interrupt. The modification necessary to avoid the echo is now quite obvious: reverse the order of two output instructions so that the echo goes to another TTY. This has the further advantage of providing a log of incoming data without any additional programming.

Outgoing data does not go through the Teletype handler at all because the handler uses the eighth bit as a parity bit.

6. REFERENCES.

- [1] CCITT recommendation V24, Geneva, 1964, amended at Mar del Plata, 1968.

APPENDIX I
Remote Control Terminal.

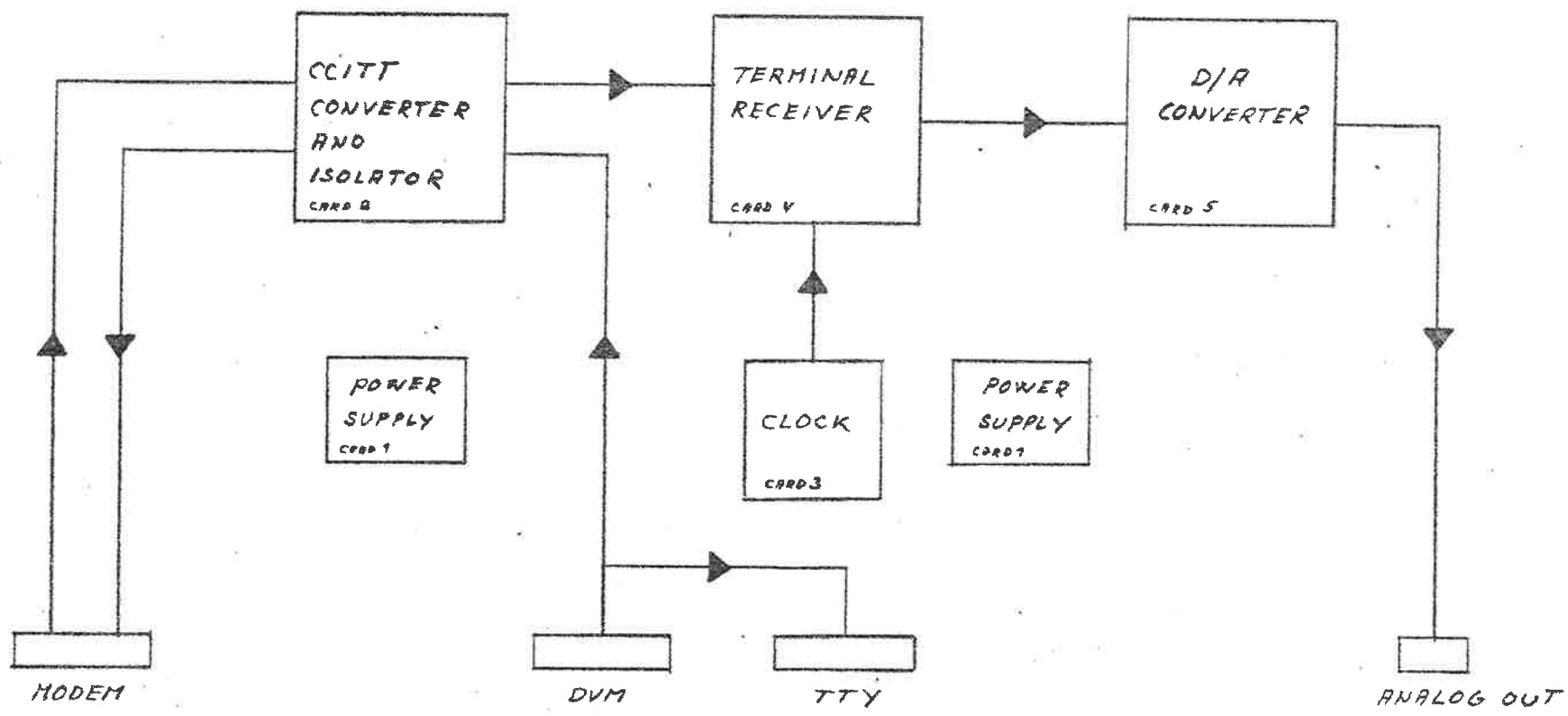
DESCRIPTION

The data signals from the modem pass the CCITT receiver circuit SN75152 which converts them to TTL levels and then they pass an optically coupled isolator TIL111. To provide higher output current, the isolator is followed by an inverter. The inverted signal goes to the terminal receiver card, where the MOS circuit MC2259L converts the 8-Bit serial data word to parallel form. When a whole word is converted, it is transferred to the output buffer register.

The output from the register consists of eight open drain transistors and therefore a resistor must be connected between each output and -12 volts to make it compatible with the D/A converter circuit, which has TTL logic inputs. The MC2259L is synchronized by an external clock generator with the frequency $16 \cdot \text{Bit rate} = 1760 \text{ Hz}$. This clock generator is placed on the clock card and is a transistorized astable flip-flop followed by an integrated JK flip-flop to give a symmetrical waveform. The frequency of the clock is adjustable.

The 8-Bit parallel data word from the output buffer register of the MC2259L circuit goes to the D/A converter card, where the circuit ZD430 converts it. The output of the ZD430 is protected by an operational amplifier 741C connected as a voltage follower. The 741C is an unexpensive circuit and it is socket mounted for easy replacement.

Data signals from the Solatron data logger to the DVM input connector pass the CCITT driver SN75150, which converts them to standard CCITT signals. Then the CCITT signals go directly to the modem. The DVM input is optically isolated from the CCITT driver by the TIL111 circuit.



R/B

REMOTE CONTROL TERMINAL
BLOCK DIAGRAM

NR R/B 7000
 DAT. 02.02 75
 R/B
 BLOCK DIAGRAM

SPECIFICATION AND INSTRUCTION

Power : 220 V 50 Hz

Signal ground isolated from protect ground.

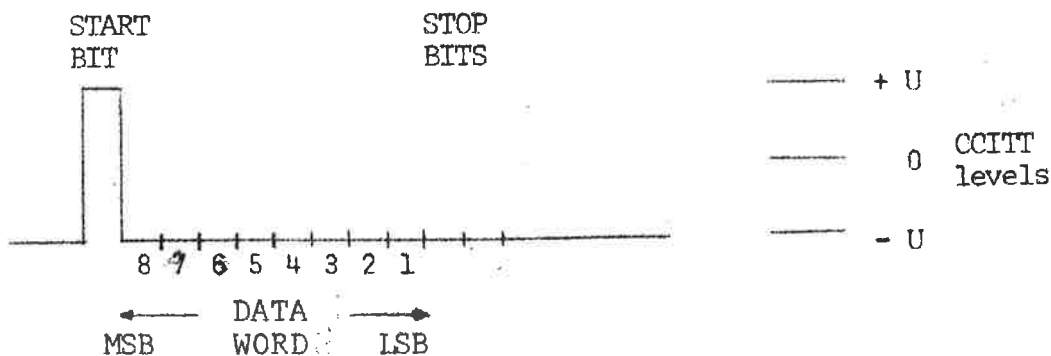
Outputs: Analog output, TTY output, CCITT output.

Inputs: CCITT input, DVM input.

ANALOG OUTPUT:

The analog output receives input from the modem connector (Cannon 25S pin 2 signal, pin 7 ground).

The input should be an 8-bit serial data word with signal levels in accordance with CCITT recommendations (figure 1, table 1). The input is optically isolated from the remote control terminal.



Logical 1" = low voltage
Logical 0" = high voltage

The start bit corresponds to logical 0".
The stop bits correspond to logical 1".

Figure 1: Input signal.

Analog output	Input code							
	MSB							LSB
	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	8	7	6	5	4	3	2	1
Fs - LSB	1	1	1	1	1	1	1	1
3/4 Fs	1	1	0	0	0	0	0	0
1/2 Fs	1	0	0	0	0	0	0	0
1/4 Fs	0	1	0	0	0	0	0	0
LSB	0	0	0	0	0	0	0	1
0 volts	0	0	0	0	0	0	0	0

Fs = 10,00 volts 1 Bit = 40 mV.

Table 1: Coding for analog output.

DVM INPUT:

A data signal on the DVM input connector Cannon 37P pin 13 and 12 will be converted to a signal in accordance with CCITT recommendations at the modem output (Modem connector Cannon 25S pin 3 signal pin 7 ground). The input signal is optically isolated both from the remote control terminal and the modem. A positive voltage between pin 13 (+) and pin 12 (-) of the DVM input connector will give a negative voltage at the modem output (figure 2).

Min input current 10 mA
 Min input voltage 2,5 V
 Max input current 1 A

TTY OUTPUT:

A standard TTY may be connected to the TTY output connector Cannon 37P.

All control wires for the TTY are directly connected to the DVM input connector. The data signal for the TTY is connected as in figure 2.

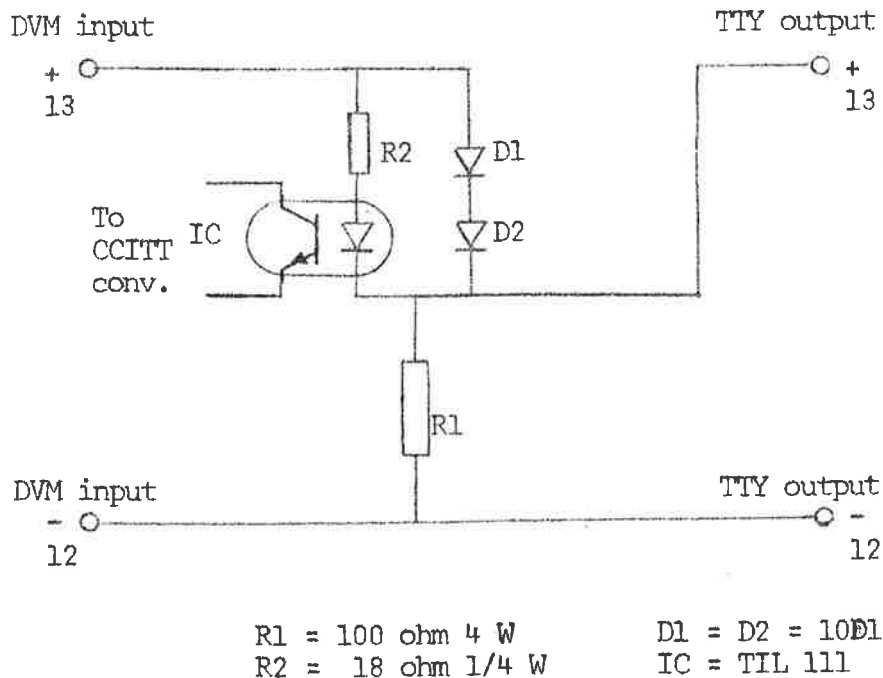
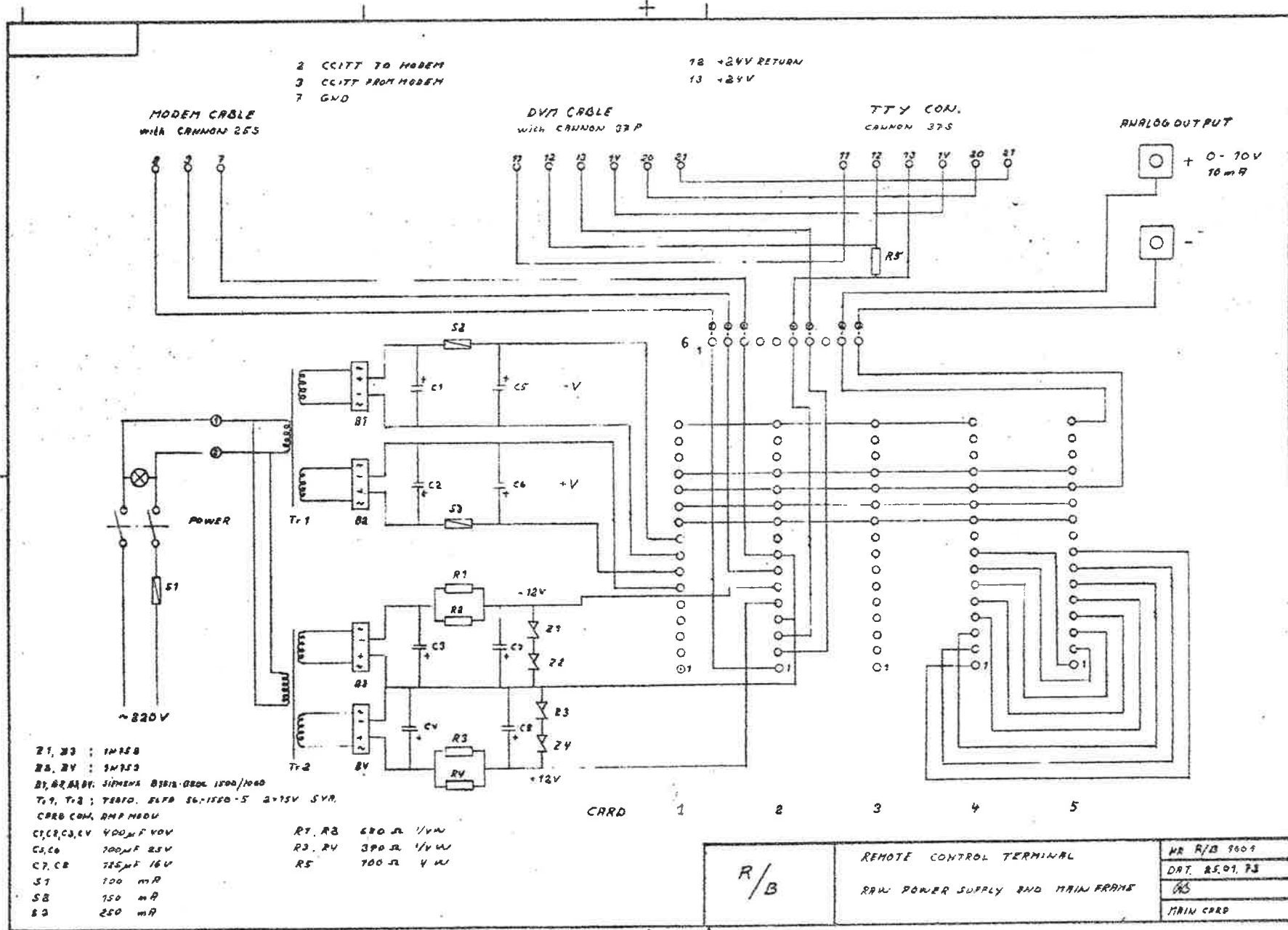


Figure 2: TTY connection



2 CCITT TO MODEM
3 CCITT FROM MODEM
7 GND

12 +24V RETURN
13 +24V

MODEM CABLE
WITH CANNON 25S

DVI CABLE
WITH CANNON 37P

TTY CON.
CANNON 37S

ANALOG OUTPUT

- Z1, Z2 : 1M50
- Z3, Z4 : 1M50
- B1, B2, B3, B4: SIEMENS B812-GR0L 1500/1000
- Tr-1, Tr-2 : Y8170. ELFA 56-1550-5 0-150V 5VA
- CARD CON. AMP MODU
- C1, C2, C3, C4 400µF 50V
- C5, C6 100µF 25V
- C7, C8 75µF 16V
- S1 100 mA
- S2 150 mA
- S3 250 mA
- R1, R2 680 Ω 1/4W
- R3, R4 390 Ω 1/4W
- R5 700 Ω 1/4W

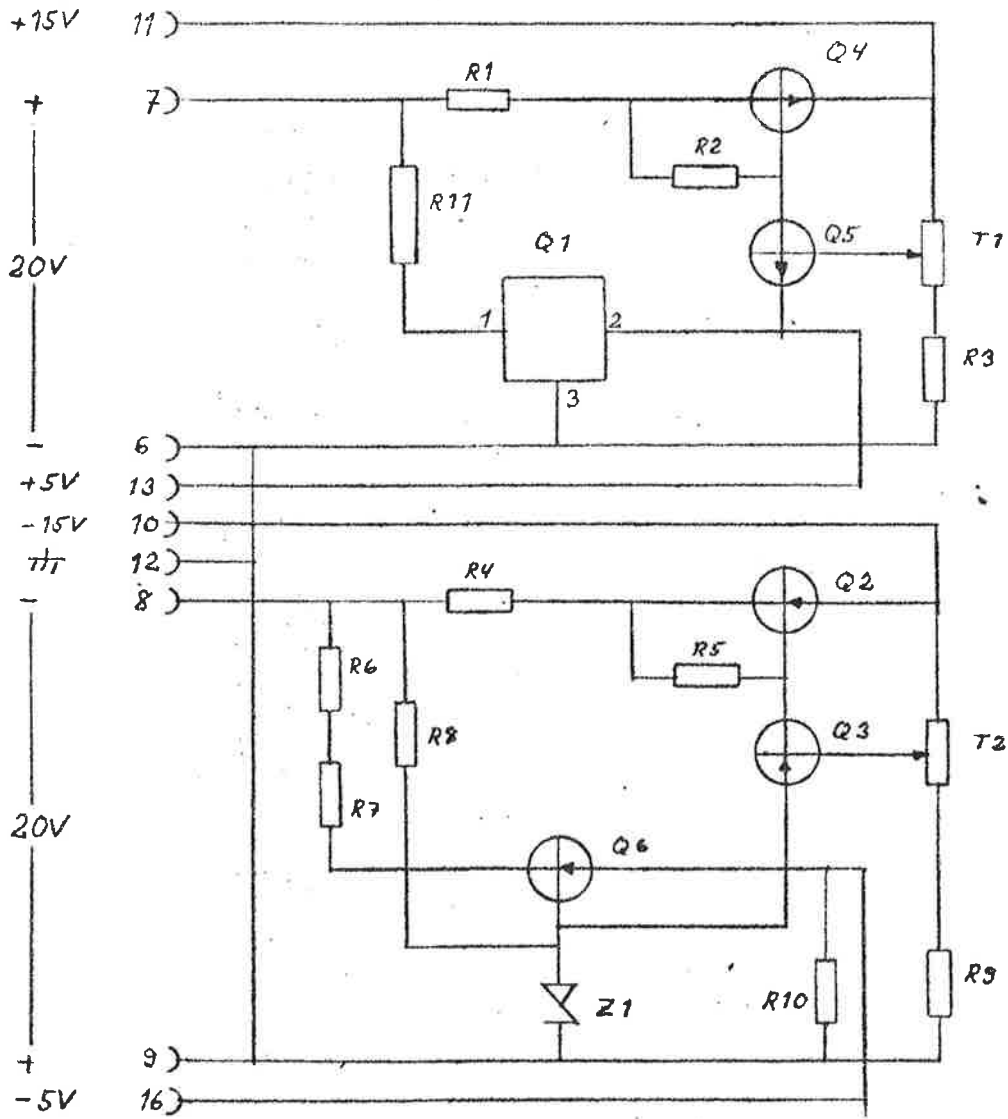
CARD 1 2 3 4 5

R/B	REMOTE CONTROL TERMINAL	MR R/B 9609
	RAW POWER SUPPLY AND MAIN FRAME	DAT. R.E. 01. 73
		68
		MAIN CARD

R/B

REMOTE CONTROL TERMINAL
VOLTAGE REGULATOR
+15V 20mA -15V 70mA
+5V 70mA -5V 20mA

NR R/B 1002
DAT 18.11.72
AS
CARD 1



R/B

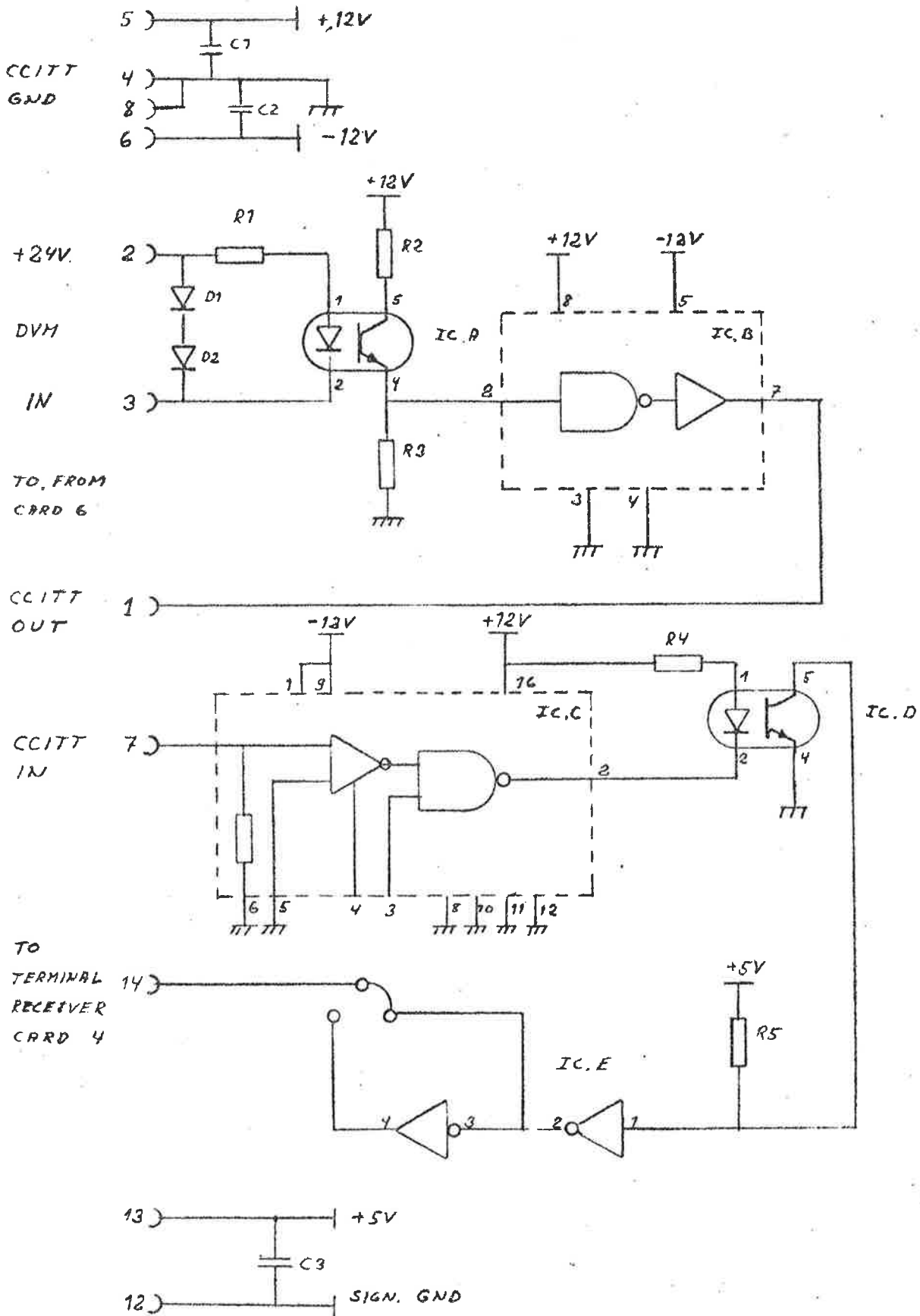
REMOTE CONTROL TERMINAL
CCITT CONVERTER

NR R/B 1003

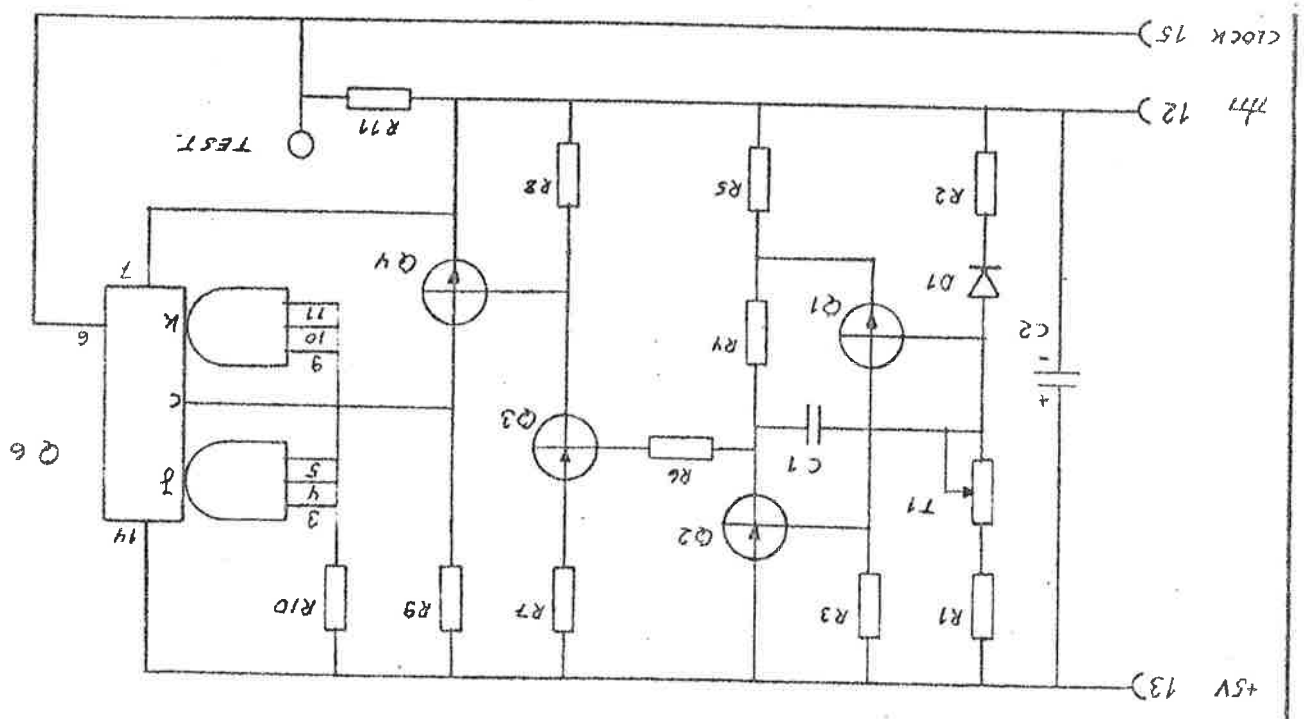
DATE 4.12.72

RS

CARD 2



R/B		REMOTE CONTROL TERMINAL		VARIABLE CLOCK 1960 HZ 568MS	
NR R/B 1004		DRT 12.17.72		PC	
CARD 3					



R/B

REMOTE CONTROL TERMINAL

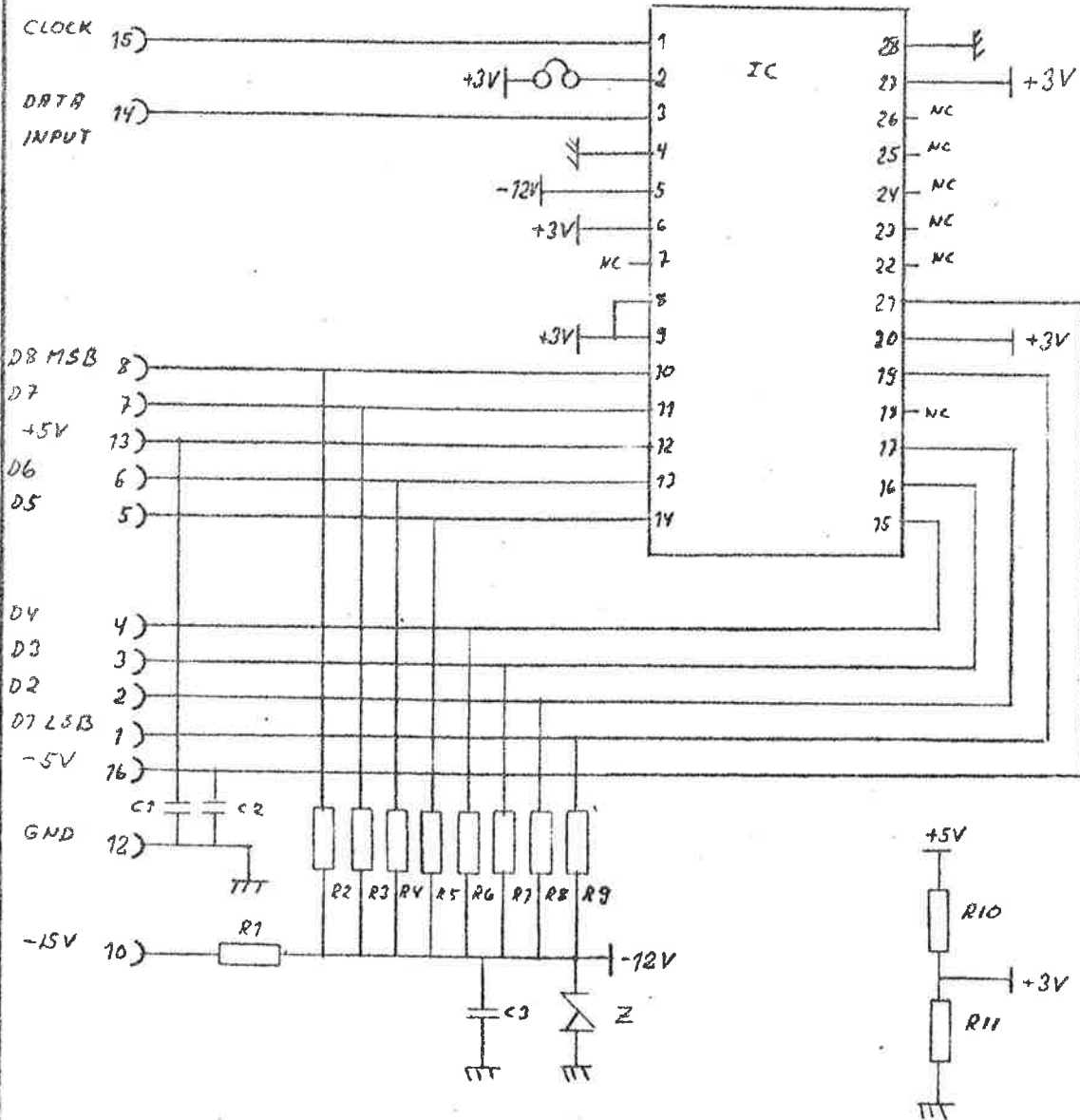
TERMINAL RECEIVER

NR R/B 1005

DATE 25.01.73

RS

CARD 4



R/B

REMOTE CONTROL TERMINAL

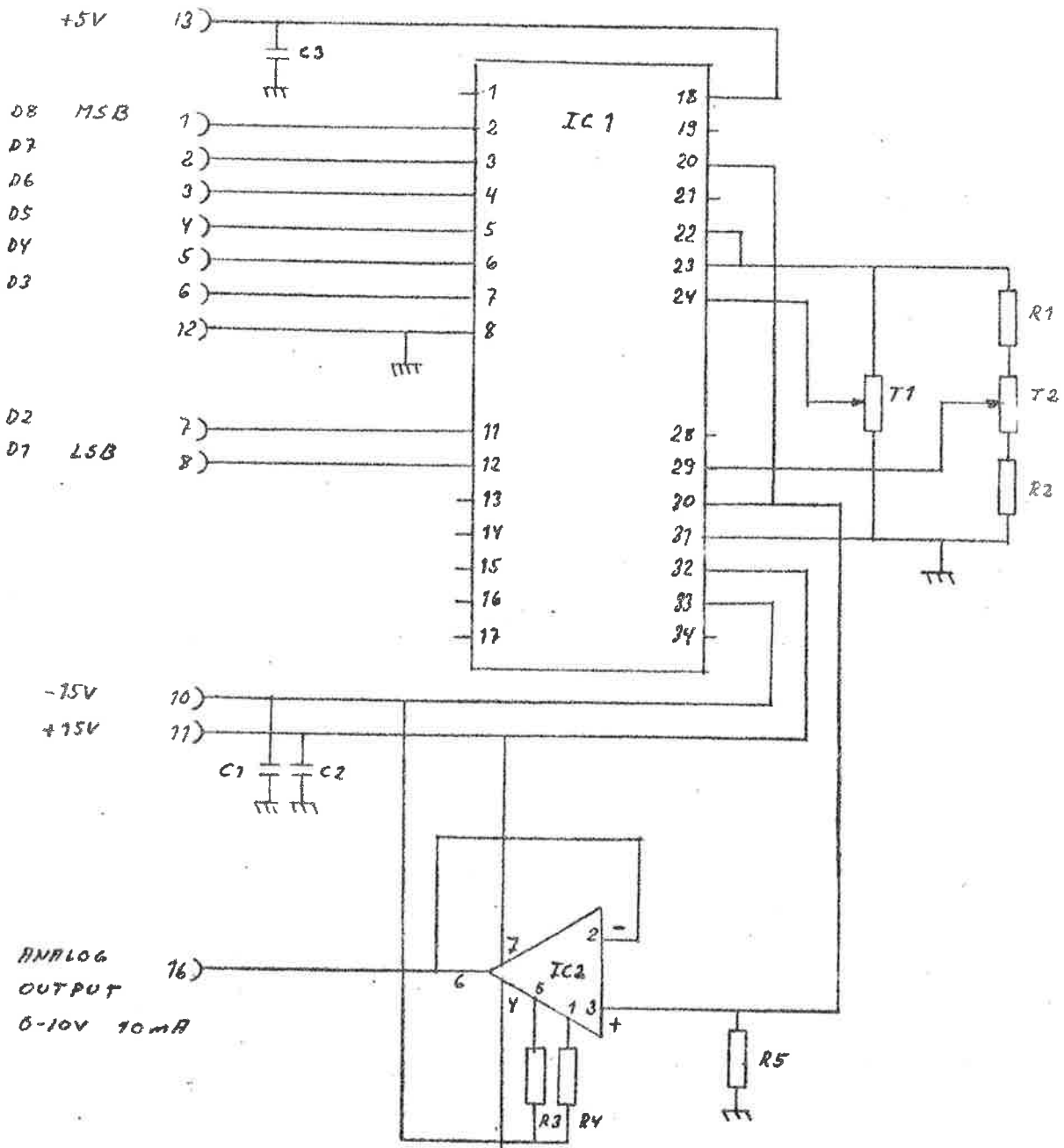
8 BIT D/A CONV.

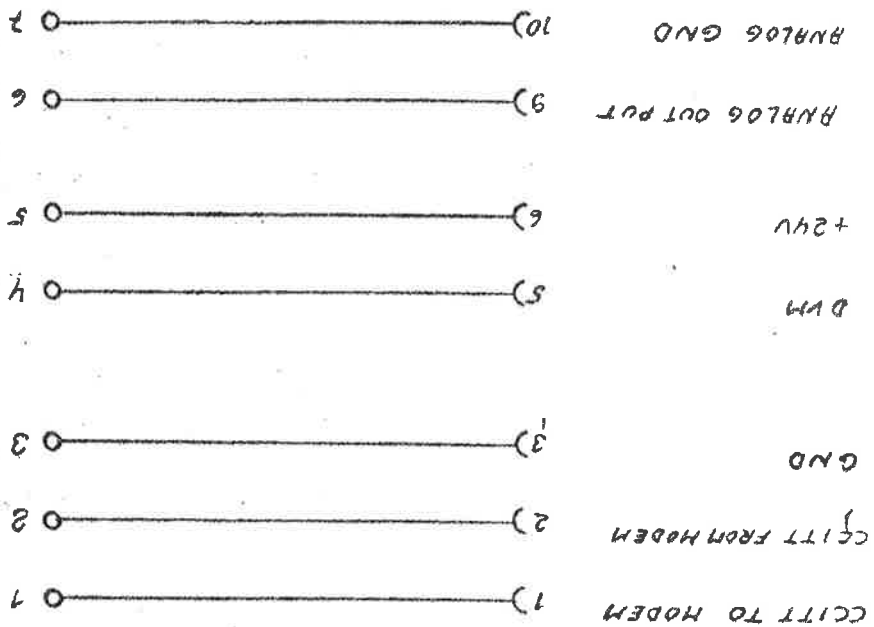
NR R/B 1000

DATE 25.01.73

AS

CARD 5



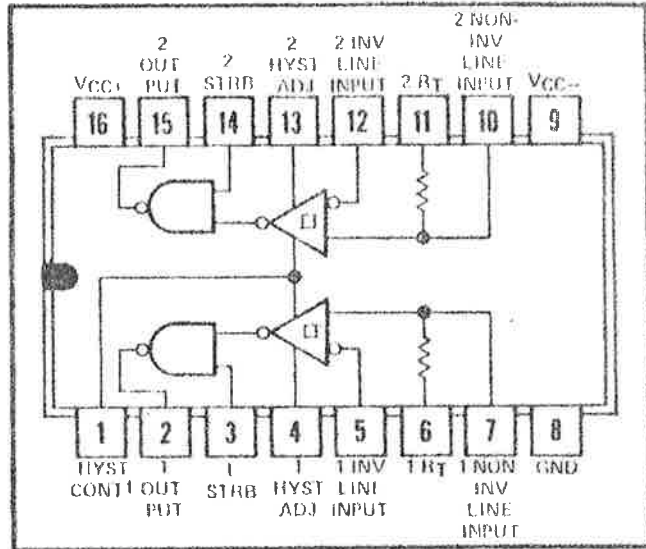


CABLE

REMOTE CONTROL TERMINAL CABLE CON. CARD		R/B	
		NR R/B 1007	
		DAT. 25.01.73	
		MS	
CARD 6			

- Meets Specifications of EIA RS-232-C or MIL-STD-188C†
- Dual Differential Receiver with Independent Strobes
- Common-Mode Input Voltage Range . . . ±25 V
- Differential Input Capability with One Input Grounded . . . ±25 V
- Continuously Adjustable Hysteresis with External Resistors
- Standard Supply Voltages . . . +12 V and -12 V
- Input Hysteresis (Double Thresholds) Remain Approximately Fixed for Power Supply and/or Temperature Variations

JORN
DUAL-IN-LINE PACKAGE (TOP VIEW)



†To meet the specifications of EIA Standard RS-232 C, connect Hysteresis Control (Pin 1) to V_{CC} (Pin 9). Also, connect pin 6 to pin 5 and pin 11 to pin 12. To meet the specifications of MIL-STD-188, leave Hysteresis Control (pin 1) and termination resistors (pin 6 and 11) open.

Description

The SN75152 is a dual differential line receiver designed to meet the requirements of EIA standard RS-232-C or MIL-STD-188 interfaces. A single control (pin 1) sets the input hysteresis for the required operation. An added feature is the capability of adjusting the hysteresis to any voltage between ±0.3 volt typical and ±5 volts typical by means of the hysteresis adjust terminals (pin 4 and 13) making the SN75152 useful for a wide variety of line receiver and Schmitt trigger applications. The large common mode input voltage range and differential input voltage (±25 volts) give the circuit added versatility. The SN75152 is designed for operation from standard ±12-volt supplies with ±10% variation. Each receiver has an output strobe that is TTL compatible.

**FUNCTION TABLE
(EACH RECEIVER)**

LINE INPUT	STROBE	OUTPUT
H	H	H
L	H	L
X	L	H

Definition of logic levels:

For the strobe: H (high) is any voltage between V_{IH} min and V_{CC}
L (low) is any voltage between ground and V_{IL} max

For the line input: H (high) is any differential input voltage (V_{ID}) † more positive than V_T, once the level of V_T has been reached
L (low) is any differential input voltage (V_{ID}) † more negative than V_T, once the level of V_T has been reached.
X (irrelevant) is any input voltage permitted by maximum ratings.

†Differential input voltages (V_T and V_{ID}) are at the noninverting input terminal with respect to the inverting input terminal.

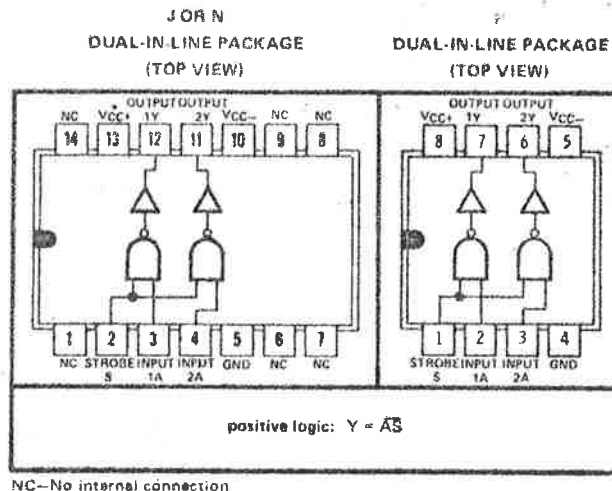
**SYSTEMS
INTERFACE CIRCUITS**

**CIRCUIT TYPE SN75150
DUAL LINE DRIVER**

SATISFIES REQUIREMENTS OF EIA STANDARD RS-232-C

CIRCUIT TYPE SN75150
BULLETIN NO. DL-S-711428, JANUARY 1971

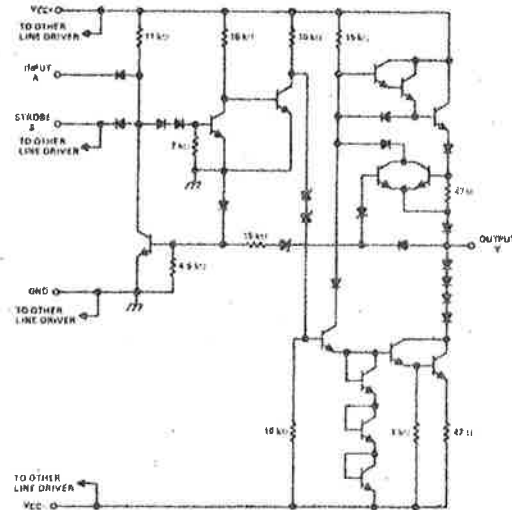
- Withstands Sustained Output Short-Circuit to any Low-Impedance Voltage between -25 V and 25 V
- 2 μ s Max Transition Time through the +3 V to -3 V Transition Region under Full 2500-pF Load
- Inputs Compatible with Most TTL and DTL Families
- Common Strobe Input
- Inverting Output
- Slew Rate can be Controlled with an External Capacitor at the Output
- Standard Supply Voltages . . . ± 12 V



description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12-volt and -12-volt power supplies. The SN75150 is characterized for operation from 0°C to 70°C.

schematic (each line driver)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage VCC+ (see Note 1)	15 V
Supply voltage VCC- (see Note 1)	-15 V
Input voltage (see Note 1)	15 V
Applied output voltage (see Note 1)	± 25 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



MOTOROLA
Semiconductors

MC2259L

Advance Information

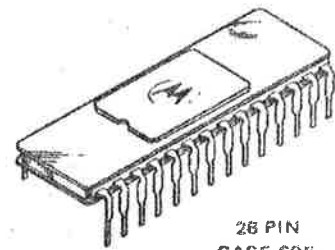
TERMINAL RECEIVER

The terminal receiver is a synchronous/asynchronous data communications adapter that receives serial digital data from a modem, organizes the data into fixed word lengths corresponding to characters, and transfers these characters to a buffer register from which the character may be accessed in a parallel format.

- One Character of Buffer Storage
- Buffer Storage Status Output Provided
- Externally Selectable Character Lengths of 5, 6, 7, or 8 Bits
- Synchronization of Clock to Data Input for Both Synchronous and Asynchronous Modes of Operation
- Externally Selectable Parity Checking -- Odd or Even
- Provision for External Character Synchronization in the Synchronous Mode
- In the Asynchronous Mode, Provides for Generating a BREAK Signal When the Absence of a STOP Bit Is Detected
- Overrun Indicator Denotes Lost Character
- Input Clock Frequency 64, 16 or 1 Times Bit Rate
- Operating Frequency of DC to 10k Bits per Second ($\div 64$ Mode) and 200k Bits per Second ($\div 1$ Mode)
- Input and Output Compatible with TTL Devices

MOS (P-CHANNEL, LOW THRESHOLD) TERMINAL RECEIVER

ADI-142



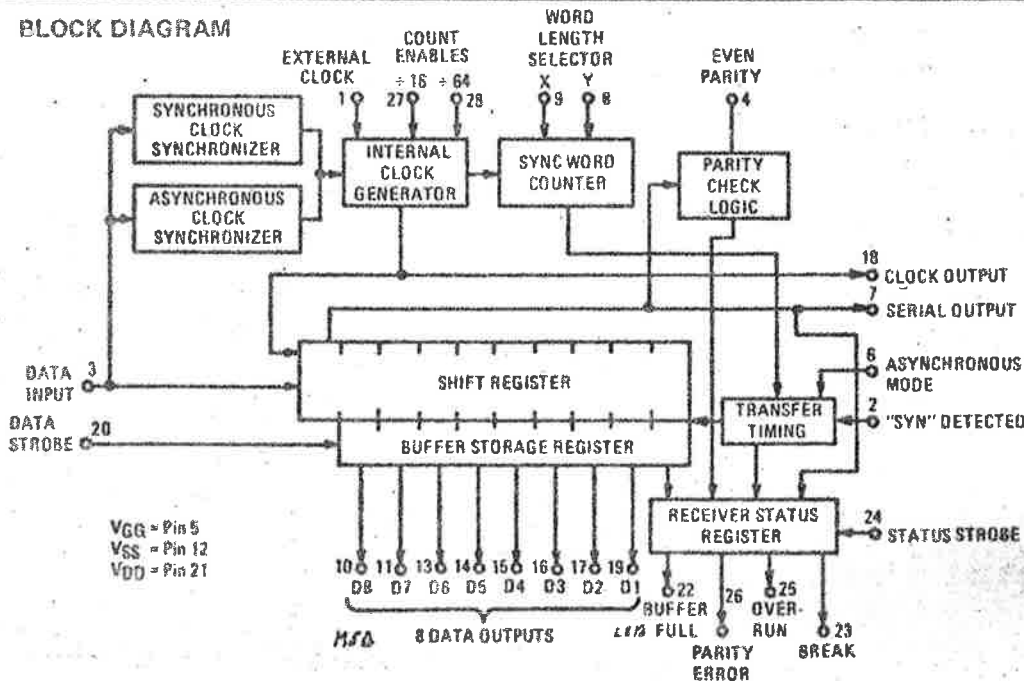
26 PIN
CASE 695

MAXIMUM RATINGS (Voltages referenced to V_{SS})

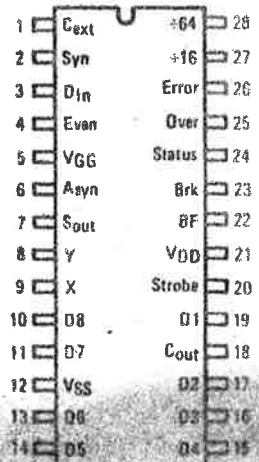
Rating	Symbol	Value	Unit
Supply Voltage	V _{DD} , V _G	-20 to +0.3	V _{dc}
Data Input Voltage	V _{in}	-20 to +0.3	V _{dc}
Operating Temperature Range	T _A	0 to +75	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



PIN ASSIGNMENT



APPLICATIONS INFORMATION

ASYNCHRONOUS OPERATION

The function of the terminal receiver is to respond to input data and synchronize with that data. The normal state of the data line during the time when no character is being transmitted is the Mark state. The initial change in state of this line will occur upon receipt of the Start bit. This "Mark-to-Space" transition (of the Start bit) causes the internal clock generator to be initialized for synchronization of the internal clock with the data. The data line is continuously monitored until the internal clock signal is generated at the midpoint of the Start bit period. This assures the presence of a valid Start bit. The synchronizing logic is then disabled until the complete character (following the Start bit) is received. If the data line returns to the Mark state (as in the case of noise) during the monitoring period, the bit is ignored and the terminal receiver resumes looking for a valid Start bit.

After the Start bit has been detected and the synchronization accomplished, data is shifted through the shift register and the Start bit appears in the Start bit flip-flop (the last stage of the shift register). The complete character is now stored in the shift register and the receiver automatically generates a transfer command to load the character in the buffer storage register. At the same time, the state of the Stop bit flip-flop is monitored to verify the presence of a Stop bit. Its absence will result in an error output called Break being stored in the receiver status register.

As the character shifts through the shift register, parity for the character is accumulated. The resulting parity bit condition is compared with correct parity (odd or even) and, in the case of error, Parity Error will be stored in receiver status register.

When the character is transferred to the buffer storage register, a Buffer Full signal will be stored in the receiver status register. If the transfer occurs during a full buffer condition, the old character will be lost and an error signal called Overrun will be stored in the receiver status register. The receiver status information will be retained throughout the character time until a new character is received and the new status is stored.

The access of data in the buffer storage register by means of the Data Strobe will reset the buffer status output, indicating that the last character stored in the buffer storage register has been taken by the system.

The internal clock generator divides the bit time for each data bit into 16 or 64 segments, depending upon the externally selected ratio. A single cycle of the oscillator input signal is gated out of the clock generator at the center of a bit. This pulse is the internal clock signal which samples the data and provides the internal timing for the entire terminal receiver. The clock generator and synchronization circuitry can be bypassed by a low level on both the $\div 16$ Enable and the $\div 64$ Enable. In this case, the oscillator input signal becomes the internal clock.

A master reset is provided by means of these same two clock enable lines. When both the $\div 16$ Enable and the $\div 64$ Enable are at a high level, the chip is held in a master reset condition.

SYNCHRONOUS OPERATION

Synchronous data transmission has several characteristics which require special consideration in the synchronization of incoming data with the receiving system. Synchronous data appears as a continuous bit stream with no interval between characters and no control bits (Start and Stop bits). Therefore, synchronization must be accomplished by means of the regular characteristics of the data itself. Two degrees of synchronization are required in order to receive a valid message. These are bit synchronization (which synchronizes the internal clock of the receiving system to the data bits) and character synchronization (which establishes a character reference by means of sync codes and utilizes the fixed bit length of the characters to maintain character synchronization).

The technique of bit synchronization provided in the terminal receiver for the synchronous mode of operation utilizes each

"Mark-to-Space" transition of the data. The data transition causes an incremental correction of the internal clock timing of $1/32$ or $1/128$ of the bit time (depending upon the counter ratio selected, $\div 16$ or $\div 64$). The process of incrementing the clock with respect to the data continues with each Mark-to-Space transition of the data until the clock signal occurs at the midpoint of the data bit. The synchronization logic will continuously attempt to correct the phase error between the midpoint of the data bit and the internal clock. This results in the internal clock maintaining lock within 0.8% of the reference ($\div 64$ clock mode). The advantage of this technique is that the data transition (Mark-to-Space transition) times are averaged; therefore, signal noise pulses or other data aberrations will not cause the receiver to completely lose bit synchronization. This feature is particularly important in synchronous transmission because of the problem of maintaining character synchronization and the necessity of re-establishing character synchronization whenever bit synchronization is lost.

Character synchronization is performed external to the terminal receiver by means of a sequence of comparisons between the received data and a synchronization code (e.g., "Syn") or set of synchronization codes. The terminal receiver is designed to facilitate this external character synchronization in the following manner. When the "Syn" Detected input is low and the receiver is operating in the synchronous mode, the buffer storage register is "transparent" so that data can be monitored as it ripples through the shift register. After the first sync code has been detected, the "Syn" Detected signal is applied, which returns the buffer storage register to its normal mode of operation and initializes the character counter. The second character in the sync detection sequence will then be transferred automatically to the buffer storage register when complete. This character is then accessed for verification as a sync code. The process is repeated until it has been determined that character synchronization has been achieved. (If the required sync code is not present in the buffer storage register during the synchronization comparison, the "Syn" Detected signal is removed and the process starts over.) Once the synchronization sequence is complete, the external sync comparison logic is disabled and the incoming data message is processed as data.

As the character shifts through the shift register (bypassing the Stop bit flip-flop), parity for the character is accumulated. The resulting parity bit condition is compared with correct parity (odd or even) and, in the case of error, Parity Error will be stored in the receiver status register.

When the character is transferred to the buffer storage register, a Buffer Full signal will be stored in the receiver status register. If the transfer occurs during a full buffer condition, the old character will be lost and an error signal called Overrun will be stored in the receiver status register. The receiver status information will be retained throughout the character time until a new character is received and a new status word is stored.

The access of data in the buffer storage register by means of the Data Strobe will reset the buffer status output, indicating that the last character stored in the buffer storage register has been taken by the system.

The internal clock generator divides the bit time for each data bit into 16 or 64 segments depending upon the externally selected ratio. A single cycle of the oscillator input signal is gated out of the clock generator at the center of a bit. This pulse is the internal clock signal which samples the data and provides the internal timing for the entire terminal receiver. The clock generator and synchronization circuitry can be bypassed by a low level on both the $\div 16$ Enable and the $\div 64$ Enable. In this case, the oscillator input signal becomes the internal clock.

A master reset is provided by means of these same two clock enable lines. When both the $\div 16$ Enable and the $\div 64$ Enable are at a high level, the chip is held in a master reset condition.



FUNCTION DESCRIPTION

INPUTS

Data Input — The serial data from the modem or other sources is entered into the Terminal Receiver by means of this terminal. The data is not inverted within the receiver and appears at the output in the same sense as it enters.

Data Strobe — The Buffer Storage latches are sampled whenever a high level is applied to the Data Strobe input.

Status Strobe — The latches of the Receiver Status Register are sampled whenever a high level is applied to the Status Strobe line.

Even Parity — A high level on the Even Parity input causes a check for an even number of high-level data bits, including the parity bit. A low level checks for odd parity in a similar manner. There is no provision to inhibit the Parity Check logic for "no parity" data transmission.

Word Length Selector — Two input lines (X, Y) are provided to define the character bit length. A character will always appear at the output in a right justified bit position for the selected word lengths. The following table shows the character length for each input combination.

X	Y	Word Length (Including parity, if applicable)
1	1	8 bits
0	1	7 bits
1	0	6 bits
0	0	5 bits

A high level is defined as a positive logic "1".

$\div 16$ and $\div 64$ Counter Enables — These two inputs provide a means of producing the internal clock from an oscillator that is either 16 or 64 times the bit rate. Provision is also made to bring the already synchronized clock from a source such as a modem into the Terminal Receiver to act as the internal clock. Available options are shown in the following table.

$\div 16$	$\div 64$	Oscillator Frequency at the External Clock Input
0	0	= Bit Rate
1	0	= 16 x Bit Rate
0	1	= 64 x Bit Rate
1	1	Master Reset*

*A typical design of the external system is such that one of the divider enables is selected for the applicable external clock frequency. The other enable input then becomes a Master Reset for the Terminal Receiver.

External Clock Input — This is the oscillator input that controls the transmission rate of the Terminal Receiver.

Asynchronous Mode — A high level on the Asynchronous Mode input enables the device for operation in the asynchronous mode using control bits (START and STOP). The START bit is used to indicate the presence of a character and for synchronization of the internal clock with the character. The presence of a STOP bit verifies character synchronization.

A low level on this input enables the device for synchronous operation and disables all asynchronous logic. A transition monitor samples each "Mark-to-Space" transition of the data, compares the $\div 16/\div 64$ clock counter state with the preferred coincidence state, and incrementally adjusts one-half clock step toward correct bit synchronization. The character synchronization is handled externally by means of the detection of a series of sync characters (e.g., "SYN").

"Syn" Detected — A high level on this input enables the system to operate in the synchronous mode by cycling in synchronization with each character. The high level indicates to the receiver that external logic has determined character sync. A low level on this line holds the Buffer Storage Register latches open so that data ripples across the outputs to permit external detection of sync codes on the receiver outputs.

OUTPUTS

Data Outputs — Data is transferred to the eight parallel open-drain outputs from the Buffer Storage Register latches. The outputs are enabled by an input signal to the Data Strobe terminal and provide compatibility with TTL plus bussing capability. For character lengths of 5 to 8 bits, data appears in a right justified position.

Serial Output — The data being shifted into the shift register is simultaneously available at the Serial Output. The stop bits are automatically stripped from the data. This provides a convenient means for externally accumulating longitudinal parity.

Receiver Status Outputs — Information on the status of data within the receiver is provided by means of four outputs that supply their indication upon receipt of a strobe signal at the Status Strobe input. The functions of these four status indicators are as follows:

1. **Buffer Full** — This output shows that a character is in the Buffer Storage latches and has not been sampled at the eight data outputs by using the Data Strobe input.

2. **Overrun** — This output provides an indication that two or more characters have been transferred into the Buffer Storage Register latches in succession without an intervening sampling of the buffer contents by use of the Data Strobe. This means that at least one character has been lost. Use of the Data Strobe removes this indicator after the transfer of the next character into the Buffer Storage Register.

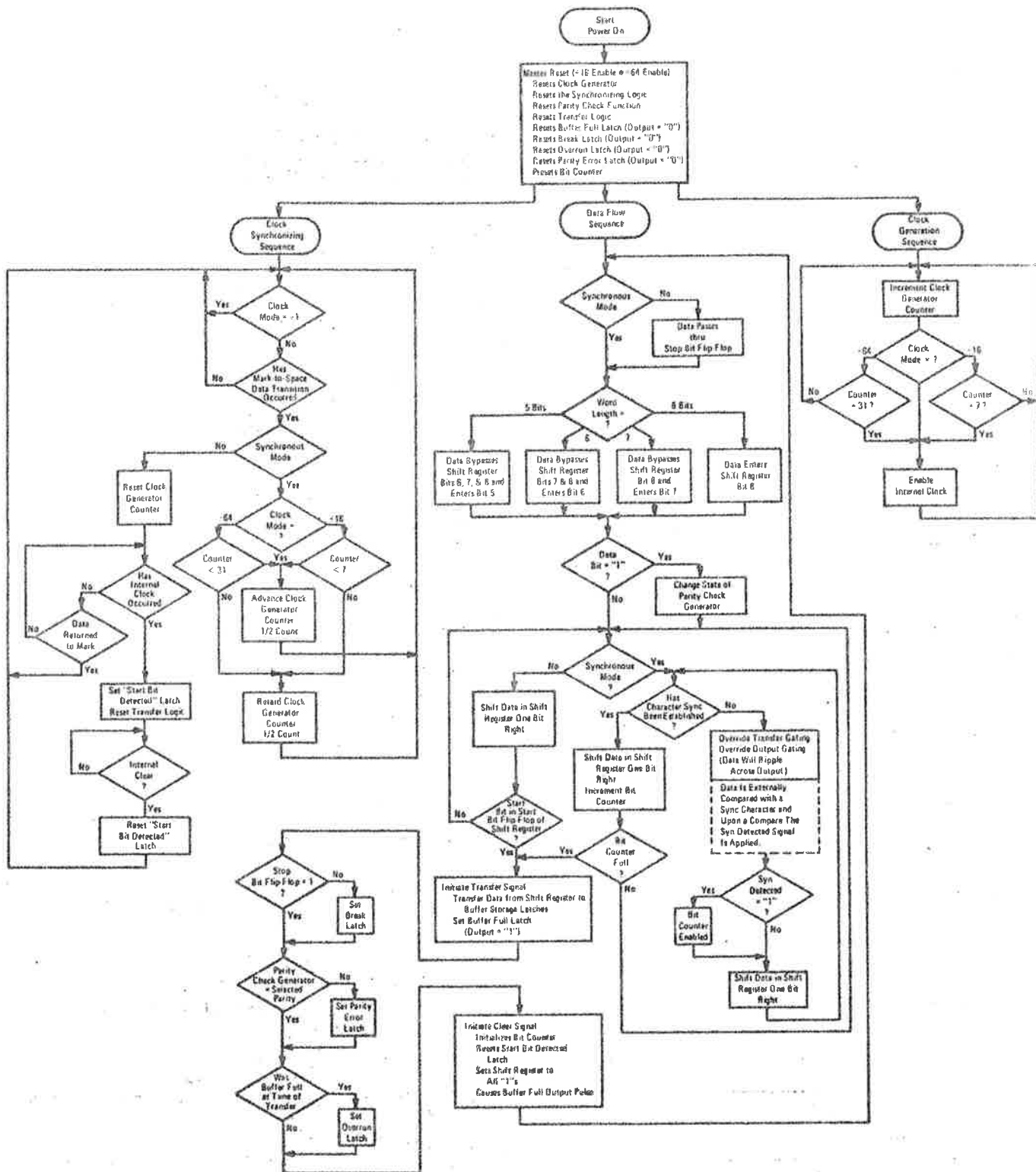
3. **Parity Error** — Incorrect parity for a particular character causes an error signal (high level) to be generated and made available at the Parity Error terminal for the period that the character is present in the Buffer Storage Register.

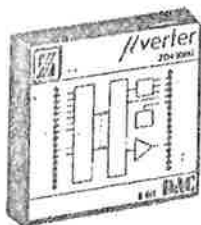
4. **Break** — The absence of a STOP bit following the character causes a Break signal to be stored in the Receiver Status Register for the character time (asynchronous operation only).

Clock Output — The internal clock that has been synchronized with the data is available for external use by means of this output.



FIGURE 8 - TERMINAL RECEIVER FLOW DIAGRAM





- 0° – 70°C Operation
- TTL/DTL Compatible
- Selectable Voltage Ranges
- Fits Standard DIP Matrices
- Adjustable FSR and Zero Offset
- All Models Interchangeable, Pin-for-Pin

M-SERIES

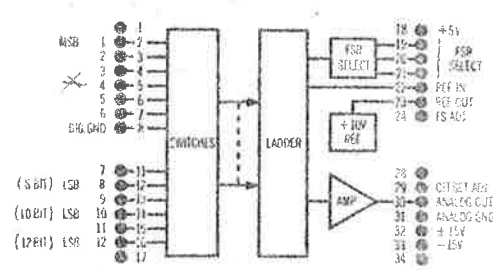


8-, 10-, 12-BIT BINARY
2-, 3-DIGIT BCD

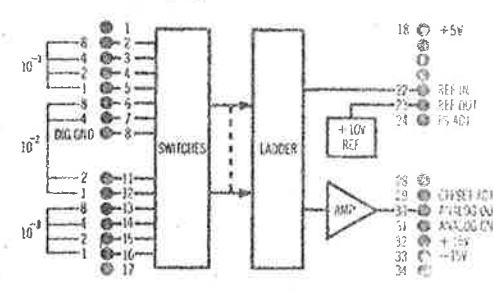
PERFORMANCE SPECIFICATIONS

Model No.	ZD430	ZD431	ZD432	ZD440	ZD441	ZD429	ZD433																																
RESOLUTION	8-Bit	10-Bit	12-Bit	8-Bit	10-Bit	2-Digit	3-Digit																																
SETTLING TIME (to 1/2 LSB) 0V to +10V -5V to +5V -10V to +10V	20 μs 20 μs 25 μs	20 μs 20 μs 25 μs	20 μs 20 μs 30 μs	2 μs 2 μs 5 μs	5 μs 5 μs 10 μs	20 μs --																																	
ACCURACY @ 25°C	<table border="1"> <tr> <td>Scaling error: (% of Reading) max.*</td> <td>±0.1% (±0.005%/°C)</td> <td>±0.1% (±0.005%/°C)</td> <td>±0.05% (±0.002%/°C)</td> <td>±0.1% (±0.005%/°C)</td> <td>±0.1% (±0.005%/°C)</td> <td>±0.2% (±0.005%/°C)</td> <td>±0.1% (±0.005%/°C)</td> </tr> <tr> <td>Zero offset (% of FSR), max.*</td> <td>±0.2% (±0.005%/°C)</td> <td>±0.05% (±0.005%/°C)</td> <td>±0.05% (±0.002%/°C)</td> <td>±0.2% (±0.002%/°C)</td> <td>±0.05% (±0.002%/°C)</td> <td>±0.5% (±0.005%/°C)</td> <td>±0.05% (±0.005%/°C)</td> </tr> <tr> <td>Linearity (% of FSR), max.</td> <td>±0.2% (±0.002%/°C)</td> <td>±0.05% (±0.002%/°C)</td> <td>±0.01% (±0.002%/°C)</td> <td>±0.2% (±0.002%/°C)</td> <td>±0.05% (±0.002%/°C)</td> <td>±0.2% (±0.002%/°C)</td> <td>±0.05% (±0.002%/°C)</td> </tr> <tr> <td>Long Term Stability (% of FSR)</td> <td colspan="2">±0.2%/1000 hr.</td> <td colspan="3">±0.1%/1000 hr.</td> <td colspan="2">±0.2%/1000 hr.</td> </tr> </table>							Scaling error: (% of Reading) max.*	±0.1% (±0.005%/°C)	±0.1% (±0.005%/°C)	±0.05% (±0.002%/°C)	±0.1% (±0.005%/°C)	±0.1% (±0.005%/°C)	±0.2% (±0.005%/°C)	±0.1% (±0.005%/°C)	Zero offset (% of FSR), max.*	±0.2% (±0.005%/°C)	±0.05% (±0.005%/°C)	±0.05% (±0.002%/°C)	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	±0.5% (±0.005%/°C)	±0.05% (±0.005%/°C)	Linearity (% of FSR), max.	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	±0.01% (±0.002%/°C)	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	Long Term Stability (% of FSR)	±0.2%/1000 hr.		±0.1%/1000 hr.			±0.2%/1000 hr.	
Scaling error: (% of Reading) max.*	±0.1% (±0.005%/°C)	±0.1% (±0.005%/°C)	±0.05% (±0.002%/°C)	±0.1% (±0.005%/°C)	±0.1% (±0.005%/°C)	±0.2% (±0.005%/°C)	±0.1% (±0.005%/°C)																																
Zero offset (% of FSR), max.*	±0.2% (±0.005%/°C)	±0.05% (±0.005%/°C)	±0.05% (±0.002%/°C)	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	±0.5% (±0.005%/°C)	±0.05% (±0.005%/°C)																																
Linearity (% of FSR), max.	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	±0.01% (±0.002%/°C)	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)																																
Long Term Stability (% of FSR)	±0.2%/1000 hr.		±0.1%/1000 hr.			±0.2%/1000 hr.																																	
INPUTS	Data coding: Modified 2's complement-bipolar, Straight binary-unipolar Data configuration (TTL/DTL compatible): 1 line/bit logical 1 = V _H , logical 0 = V _L Data loading: 1 TTL load/line						Binary-coded Decimal																																
OUTPUTS	Unipolar (FSR): 0V to +10V Bipolar (FSR): ±10V, ±5V Output drive (short circuit proof): 5 mA Output capacitive load: 1000 pF, 1000 pF, 1000 pF, 300 pF, 300 pF, 1000 pF Output impedance @ DC: 0.1 ohm Output noise: < 1 mV Internal reference output: +10V (±1%) @ 4 mA, ±0.1% (no load - full load)						0V to +10V - only -																																
ENVIRONMENTAL	Operating temp.: 0 to 70°C Storage temp.: -25° to 85°C Relative humidity: 90% non-condensing																																						
POWER REQUIREMENTS (±5%)	±15V @ 10 mA +5V @ 40 mA		+15V @ 25 mA -15V @ 10 mA +5V @ 50 mA		±15V @ 25 mA +5V @ 40 mA		±15V @ 10 mA +5V @ 40 mA																																

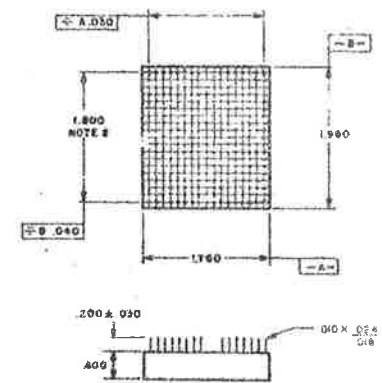
Specifications subject to change without notice.
*Adjustable to zero error with external trim potentiometers.



Pin Connections (Top View)
Binary Models ZD430, 431, 432, 440, 441



Pin Connections (Top View)
BCD Models ZD429, ZD433



- NOTES:
1. Tolerance: ±0.010 unless noted.
 2. Leads "float" to accommodate error in connector location.
 3. Pin spacing shown on 0.1 inch grid.
 4. Case material: transfer molded epoxy.
 5. Leads: beryllium copper, gold-plated.
 6. Bottom surface double coated with epoxy - Dielectric insulation of 450 V/mil or greater.

DAC Outline Dimensions (All Models)



TELEMETRIC Instrument AB

Box 341 • S-172 03 SUNDBYBERG 3 • Tel. 08/29 30 90-93
Schælegatan 13 • S-212 28 MALMÖ • Tel. 040/18 55 00-01

OPERATION

Several external connections must be made for proper operation of each digital-to-analog converter. Internal or external reference, and full scale voltage ranges are selected by jumpering pins as shown in Table 1.

CAUTION

BCD units are internally wired for 0V to +10V full scale operation and do not require external jumpering. Do not strap pins for other FSR's as damage may result.

Table 1. External Connections for DAC Operation

DESIRED OPERATION	CONNECTIONS
Internal Reference	Pin 22 to Pin 23
External Reference +10V ($\pm 10\%$), 4 mA	Connect to Pin 22
$\pm 10V$ FSR	Pin 21 to Pin 22
$\pm 5V$ FSR	Pin 20 to Pin 30 Pin 19 to Pin 22
0V to +10V FSR	Pin 20 to Pin 30

INTERNAL REFERENCE

The internal reference of each D/A converter can be used to drive three additional units. To use, connect pin 23 of first unit to pin 22 of each additional converter.

OPTIONAL ADJUSTMENT

Each converter is ready to operate within given specifications without external adjustments. However, special full scale settings or fine adjustment of offset voltage can be made using the circuit shown in Figure 1. The circuit provides a full scale adjustment range of $\pm 10\%$, and an offset adjustment range of ± 40 mV.

NOTE: Full scale is not adjustable when using external reference.

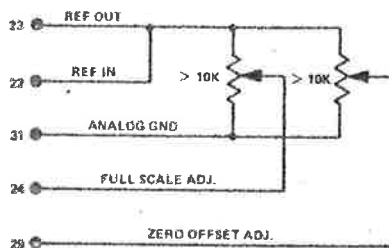


Figure 1. Full Scale and Zero Offset Adjustments

ANALOG OUTPUT AND INPUT CODING

ANALOG OUTPUT (BIPOLAR)	INPUT CODE							
	MSB							LSB
	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-n}
F.S. - 1 LSB	1	1	1	1	1	1	1	1
+½ F.S.	1	1	0	0	0	0	0	0
0V + 1 LSB	1	0	0	0	0	0	0	1
0 Volts	1	0	0	0	0	0	0	0
0V - 1 LSB	0	1	1	1	1	1	1	1
-½ F.S.	0	1	0	0	0	0	0	0
-F.S. + 1 LSB	0	0	0	0	0	0	0	1
-F.S.	0	0	0	0	0	0	0	0

Table 1. Modified 2's Complement (Bipolar n-Bits)

ANALOG OUTPUT (UNIPOLAR)	INPUT CODE							
	MSB							LSB
	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-n}
F.S. - 1 LSB	1	1	1	1	1	1	1	1
+¼ F.S.	1	1	0	0	0	0	0	0
+½ F.S.	1	0	0	0	0	0	0	0
+¾ F.S.	0	1	0	0	0	0	0	0
0V + 1 LSB	0	0	0	0	0	0	0	1
0 Volts	0	0	0	0	0	0	0	0

Table 2. Straight Binary (Unipolar n-Bits)

ANALOG OUTPUT (UNIPOLAR)	INPUT CODE											
	10^{-1}			10^{-2}			10^{-3}					
	8	4	2	1	8	4	2	1	8	4	2	1
F.S. - 1 LSD	1	0	0	1	1	0	0	1	1	0	0	1
+½ F.S.	0	1	0	1	0	0	0	0	0	0	0	0
0V + 1 LSD	0	0	0	0	0	0	0	0	0	0	0	1
0 Volts	0	0	0	0	0	0	0	0	0	0	0	0

Table 3. Binary Coded Decimal (Unipolar 3-Digits)

MSB	2^{-1}	.5
2	2^{-2}	.25
3	2^{-3}	.125
4	2^{-4}	.0625
5	2^{-5}	.03125
6	2^{-6}	.015625
7	2^{-7}	.0078125
8	2^{-8}	.00390625
9	2^{-9}	.001953125
10	2^{-10}	.0009765625
11	2^{-11}	.00048828125
LSB	2^{-12}	.000244140625

Table 4. Binary Weights

Program Listings

APPENDIX II

TASK INIT

INITIALIZES THE SELF TUNING REGULATOR AND ADJUSTS PROCESS VARIABLES ON-LINE

RUNS IN PARTITION PUSER
DEFAULT PRIORITY 490

AUTHOR: ULF BORISSON 1972-11-15

THE PROGRAM PACKAGE FOR CONTROL OF KIRUNA FINKROSSVERK CONTAINS THE FOLLOWING PARTS:

- TASK INIT
- TASK REGUL
- TASK PRINT
- TASK TAPE
- TASK ERROR
- TASK SEND

THE FOLLOWING VARIABLES IN BLANK COMMON ARE USED FOR SPECIAL PURPOSES. REGULATOR PARAMETERS ARE GIVEN VALUES BY THE MCR-FUNCTION SET.

IEV3 SIGNALS IF COMMON/SLASK/ IS AVAILABLE

IEV4 CONTAINS THE VALUE OF THE EVENT VARIABLE RECEIVED WHEN AN ERROR HAS OCCURRED

IEXT8 DETERMINES THE TYPE OF EXECUTION OF TASK PRINT

IEXT7 IS USED FOR COMMUNICATION WITH THE TASKS ON-LINE
BIT 17 SET TO 1 GIVES LOGGING ON LP
BIT 16 SET TO 1 GIVES LOGGING ON DT
BIT 15 SET TO 1 AVOIDS UPDATING OF U-VECTOR WITH SIGNALS FROM THE PI-REGULATOR IN KIRUNA

IEXT6 DETERMINES THE TYPE OF EXECUTION OF TASK TAPE
IEXT6=1: OPEN FILE AND WRITE INITIAL DATA
IEXT6=2: WRITE DATA FROM A SAMPLE POINT
IEXT6=3: CLOSE FILE

IEXT5 DETERMINES THE TYPE OF EXECUTION OF TASK ERROR

IEXT4 DETERMINES THE TYPE OF EXECUTION OF TASK INIT
IEXT4=0 GIVES INITIALIZATION OF THE SELF TUNING REGULATOR
IEXT4=1 GIVES NEW VALUES TO SOME SPECIAL PARAMETERS
IEXT4=2 GIVES NEW VALUE TO UTOT

IEXT3 IS USED TO SEND SPECIAL CONTROL SIGNALS TO KIRUNA
BIT 17 SET TO 1 GIVES THE CONSTANT CONTROL SIGNAL
UTOT AND THE SELF TUNING REGULATOR IS NOT CALLED
(THE BIT IS AUTOMATICLY RESET IN THE PROGRAM)
BIT 15 HAS THE SAME ACTION AS BIT 17, BUT BIT 15 MUST BE RESET BY USER

SUBROUTINES REQUIRED
NONE

COMMON (SYSA(25), IOA(26), MPXA(40), ICOMVA(45), FLA1(16), FLA0(8), IUSER(36)

COMMON/SLASK/ IDUM(704),

```
1NA,NB,K,NSTEP,MSTEP,IPOINT,NCHAN,IYCHAN,ICOUN,  
1B0,RL,PDIAG,YREF,UMAX,UMIN,UTOT,DUMAX,UPI,DUPI,  
1YMIN,YMAX,  
1T(10),P(10,10),YS(10),U(10),YA(10),IDATE(6),  
1IUTOT
```

EQUIVALENCE

```
1(I1,ISYSA(17)),  
1(IEXT3,ISYSA(20)),  
1(IEXT4,ISYSA(21)),  
1(IEXT5,ISYSA(22)),  
1(IEXT6,ISYSA(23)),  
1(IEXT7,ISYSA(24)),  
1(IEXT8,ISYSA(25)),  
1(IEV2,ICOMVA(42)),  
1(IEV3,ICOMVA(43)),  
1(IEV4,ICOMVA(44))
```

```
CALL PAXA(IEV2)  
CALL PAXA(IEV3)
```

THE FOLLOWING PARAMETERS MAY BE CHANGED WITHOUT DOING
INITIALISATION OF OTHER REGULATOR PARAMETERS

```
IF (IEXT4.EQ.0 .OR. IEXT4.EQ.2) UTOT=USER(4)  
YREF=USER(1)  
YMIN=USER(2)  
YMAX=USER(3)  
DUMAX=USER(6)  
RL=USER(7)
```

```
IF (IEXT4.EQ.1 .OR. IEXT4.EQ.2) GO TO 40  
GO TO 50
```

```
IEXT8=3  
CALL REQST(5HPRINT,0)  
IEXT4=0  
GO TO 210
```

```
H0=USER(11)  
PDIAG=USER(12)
```

GIVE INITIAL VALUES TO THE REGULATOR PARAMETERS

```
DO 60 I=1,10  
T(I)=USER(I+20)
```

SET ARRAYS TO ZERO

```
P(1,1)=0.  
CALL REMOVE(P(1,1),1,P(2,1),1,99)  
CALL REMOVE(P(1,1),1,U(1),1,10)  
CALL REMOVE(P(1,1),1,YA(1),1,10)  
CALL REMOVE(P(1,1),1,YS(1),1,10)
```

CALL DATE(IDATE)

```
NA=MPXA(1)  
NB=MPXA(2)  
K=MPXA(3)  
NCHAN=MPXA(4)  
IYCHAN=MPXA(5)
```

```
NSTEP=1
MSTEP=1
ICOUN=0
```

```
UMIN=0.
UMAX=5.0
```

```
L=NA+NB
DO 100 I=1,L
P(I,I)=PDIAG
```

```
100 IEXT8=1
CALL REQST(5HPRINT,0,IEV4)
CALL WAITFR(IEV4)
IF (IEV4) 150,160,160
150 IEXT5=1
CALL REQST(5HERROR,0)
```

```
C
160 CALL GETBIT(IEXT7,16,LOG)
IF (LOG) 170,210,210
170 IEXT6=1
CALL REQST(4HTAPE,0,IEV4)
CALL WAITFR(IEV4)
IF (IEV4) 200,200,210
200 IEXT5=2
CALL REQST(5HERROR,0)
```

```
C
210 IEV2=1
IEV3=1
999 CALL EXIT
GO TO 999
END
```

```
001 C TASK REGUL
002 C
003 C READS MEASUREMENTS AND CALLS THE SELF TUNING REGULATOR
004 C
005 C RUNS IN PARTITION PPRUS
006 C DEFAULT PRIORITY 150
007 C
008 C AUTHOR: ULF BORISSON 1972-11-15
009 C
010 C SURROUTINES REQUIRED
011 C RECIV
012 C STREG/TUNE,REG
013 C
014 100 CALL RECIV
015 CALL STREG
016 GO TO 100
017 C
018 END
```

```

SUBROUTINE RECIV          C 001
RECIVS DATA FROM A TELETYPE UNIT   C 003
AUTHOR: ULF BORISSON 1972-11-15    C 005
SUBROUTINES REQUIRED              C 007
RLINE                            C 008
RFP                                C 009
DIMENSION BUFF(32)              C 011
COMMON IYSYA(25),IOA(26),MPXA(40),ICOMVA(45),FLAI(16),FLAO(8) C 012
IUSER(36)                        C 014
COMMON/SLASK/ IDUM(704),         C 016
IJA,NB,K,NSTEP,MSTEP,IPPOINT,NCHAN,IYCHAN,ICOUN,
I80,RL,PDIAG,YREF,UMAX,UMIN,UTOT,DUMAX,UP1,DUPI,
IYMIN,YMAX,
I(10),P(10,10),YS(10),U(10),YA(10),IDATE(6),
IUTOT
EQUIVALENCE(IEV3,ICOMVA(43))    C 023
ISTEP=0                          C 025
I=3                               C 026
CALL RLINE(0,17,BUFF,0)        C 028
NEWLIN=1                          C 030
ICCHANL=1                         C 031
CALL RFP(I,FRES,IRES,IND)      C 033
IF (IND-3) 60,50,60           C 035
IF (IND-4) 70,10,70          C 036
IF (IND-5) 100,7,100         C 037
IF (NEWLIN) 200,400,200      C 038
NEWLIN=0                         C 039
IF (IRES) 10,400,300         C 040
CALL PAXA(IEV3)              C 041
IPPOINT=IRES                   C 042
IEV3=1                          C 043
I=1                              C 044
GO TO 10                        C 045
IF (ICCHANL) 410,420,410     C 047
ICCHANL=0                       C 048
GO TO 50                       C 049
ICCHANL=1                       C 050
ICCHANL=1                       C 051
ICCHANL=1                       C 052
CALL PAXA(IEV3)              C 053
YA(ISTEP)=FRES                C 054
IEV3=1                          C 055
IF (ISTEP-NCHAN) 50,999,999 C 056
C                                C 057
RETURN                          C 058
END

```

SUBROUTINE STREG

THE SELF TUNING REGULATOR

AUTHOR: ULF BORISSON 1972-11-15

SUBROUTINES REQUIRED

TUNE

REG

COMMON ISYSA(25), IOA(26), MPXA(40), ICOMVA(45), FLAI(16), FLAO(8),
IUSER(36)

COMMON/SLASK/ IDUN(704),
INA, NB, K, NSTEP, MSTEP, IPOINT, NCHAN, IYCHAN, ICOUN,
IBO, RL, PDIAG, YREF, UMAX, UMIN, UTOT, DUMAX, UFI, DUPI,
YMIN, YMAX,
IT(10), P(10,10), YS(10), U(10), YA(10), IDATE(6),
IUTOT

EQUIVALENCE

1(IEXT3, ISYSA(20)),

1(IEXT5, ISYSA(22)),

1(IEXT6, ISYSA(23)),

1(IEXT7, ISYSA(24)),

1(IEXT8, ISYSA(25)),

1(IEV2, ICOMVA(42)),

1(IEV3, ICOMVA(43)),

1(IEV4, ICOMVA(44))

CALL PAXA(IEV3)

TEST IF THE EFFECT EXCEEDS ANY LIMIT SO THAT BIT 17 IN IEXT3
SHOULD BE SET

EFF=YA(IYCHAN)*0.4651

YS(1)=(EFF-YREF)/BO

IF (EFF-YMIN) 20,36,36

CALL SETBIT(IEXT3,17,-1)

GO TO 36

TEST IF A SPECIAL CONTROL SIGNAL IS TO BE USED

CALL GETBIT(IEXT3,17,LOG)

IF (LOG) 37,38,38

U(1)=0.

THE OLD UTOT IS USED ONCE MORE

GO TO 90

CALL GETBIT(IEXT3,15,LOG)

IF (LOG) 41,42,42

U(1)=0.

THE OLD UTOT IS USED ONCE MORE, AND IEXT3 MUST BE RESET
BY USER

GO TO 90

CONTINUE

OPTIONAL UPDATING OF U-VECTOR WITH THE PROCESS INPUT
FROM THE PI-REGULATOR IN KIRUNA

CALL GETBIT(IEXT7,15,LOG)

```

50 IF (LOG) 60,50,50
60 U(1)=DUPI
CONTINUE

CALL TUNE(YS,U,T,P,RL,NA,NB,K,NSTEP)
CALL REG(YS,U,T,NA,NB,K,MSTEP)

SET ALWAYS IEXT3, BIT 17 TO ZERO

CALL SETBIT(IEXT3,17,0)

IF (U(1)-DUMAX) 110,100,100
U(1)=DUMAX
GO TO 130
110 IF (U(1)+DUMAX) 120,120,130
120 U(1)=-DUMAX
130 UTOT=UTOT+U(1)
IF (UTOT-UMAX) 150,150,140
140 UTOT=UMAX
GO TO 165
150 IF (UTOT-UMIN) 160,160,165
160 UTOT=UMIN
165 CONTINUE

255 BITS CORRESPOND TO 5 MA

NBIT=FIX(UTOT*51.)

ONE MORE LIMIT CHECK OF THE PROCESS INPUT SENT TO KIRUNA

IF (NBIT-255) 167,167,166
166 NBIT=255
GO TO 170
167 IF (NBIT) 168,170,170
168 NBIT=0
170 IUTOT=NBIT

DUPI=YA(2)/160.-UPI
UPI=YA(2)/160.

CALL GETBIT(IEXT7,17,LOG)
IF (LOG) 180,190,190
180 IEXT8=2
CALL REQST(5HPRINT,0,IEV4)
CALL WAITFR(IEV4)
IF (IEV4) 185,190,190
185 IEXT5=3
CALL REQST(5HERROR,0)

CALL GETBIT(IEXT7,16,LOG)
IF (LOG) 195,210,210
195 IEXT6=2
CALL REQST(4HTAPE,0,IEV4)
CALL WAITFR(IEV4)
IF (IEV4) 200,210,210
200 IEXT5=4
CALL REQST(5HERROR,0)

CONTINUE
210 IEV3=1
300 RETURN
END

```

SUBROUTINE TUNE(YS,U,T,P,RL,NA,NB,K,NSTEP)

PERFORMS THE TUNING IN THE SELF TUNING REGULATOR

AUTHOR: ULF BORISSON 1972-05-02

REFERENCE: ASTRÖM,K.J., WITTENMARK,B.: ON SELF TUNING REGULATORS
REPORT 7209(R), MAY 72, LUND INSTITUTE OF TECHNOLOGY
DIVISION OF AUTOMATIC CONTROL

THE ALGORITHM IS BASED ON THE MODEL

$$Y(T+K+1)-Y_0+A(1)*(Y(T)-Y_0)+\dots+A(NA)*(Y(T-NA+1)-Y_0)= \\ =B_0*(U(T)+B(1)*U(T-1)+\dots+B(NB)*U(T-NB)) \quad (*)$$

WHERE Y0 IS THE REFERENCE VALUE OF Y

THE TUNING IS DONE WITH A REPEATED LEAST SQUARES ESTIMATION OF THE
MODEL PARAMETERS

THE NUMBER OF SAMPLE INTERVALS BETWEEN THE TUNINGS IS DENOTED
BY NSTEP. THE MAXIMUM VALUE OF NSTEP IS DENOTED BY MSTEP.

YS-VECTOR OF SCALED PROCESS OUTPUTS OF DIMENSION NA+K+MSTEP+1
YS IS NOT CHANGED IN TUNE AND IS ORGANIZED AS FOLLOWS

$$YS(1)=(Y(T)-Y_0)/B_0 \\ YS(2)=(Y(T-1)-Y_0)/B_0$$

U-VECTOR OF PROCESS INPUTS OF DIMENSION NB+K+MSTEP+1
U IS NOT CHANGED IN TUNE AND IS ORGANIZED AS FOLLOWS

$$U(1)=U(T-1) \\ U(2)=U(T-2)$$

T-VECTOR OF ESTIMATED PARAMETERS OF DIMENSION NA+NB AND ORGANIZED
AS FOLLOWS (AE(I) DENOTES THE ESTIMATED VALUE OF A(I), ETC.)

$$T(1)=AE(1) \\ T(2)=AE(2)$$

$$T(NA)=AE(NA) \\ T(NA+1)=BE(1)$$

$$T(NA+NB)=BE(NB)$$

P-COVARIANCE MATRIX OF THE PARAMETER ESTIMATES OF ORDER (NA+NB)*
(NA+NB)

RL-BASE OF THE EXPONENTIAL WEIGHTING FUNCTION

NA-NUMBER OF A-PARAMETERS IN (*)

NB-NUMBER OF B-PARAMETERS IN (*)

K-NUMBER OF PURE TIME DELAYS IN THE PROCESS

SUBROUTINES REQUIRED

NONE

DIMENSION YS(1),U(1),T(1),P(1,1),F(12),RK(12),S(12)

TUNING LOOP

DO 60 LOOP=1,NSTEP

ORGANIZE DATA FOR IDENTIFICATION

LI=K+1+NSTEP-LOOP


```

DO 10 I=1,NA
L=L1+I
10 FI(I)=-YS(L)
N1=K+1+NSTEP-LOOP
IF (NB) 21,21,11
11 DO 20 I=1,NB
L=NA+I
N2=N1+I
20 FI(L)=U(N2)
21 L=1+NSTEP-LOOP
RES=YS(L)-U(N1)
N1=NA+NB

C
C IDENTIFICATION
DO 40 I=1,N1
R=0.
DO 30 J=1,N1
30 R=R+P(I,J)*FI(J)
40 S(I)=R
DENOM=1.
DO 50 I=1,N1
DENOM=DENOM+FI(I)*S(I)
50 RES=RES-FI(I)*T(I)
DO 60 I=1,N1
RK(I)=S(I)/DENOM
T(I)=T(I)+RK(I)*RES
DO 60 J=1,I
60 P(I,J)=(P(I,J)-RK(I)*S(J))/RL
P(J,I)=P(I,J)
RETURN
END

```

SUBROUTINE REG(YS,U,T,NA,NR,K,MSTEP)

COMPUTES THE CONTROL SIGNAL OF THE SELF TUNING REGULATOR

AUTHOR: ULF BORISSON 1972-05-02

REFERENCE: ÅSTRÖM, K.J., WITTENMARK, B.: ON SELF TUNING REGULATORS
REPORT 7209(B), MAY 72, LUND INSTITUTE OF TECHNOLOGY
DIVISION OF AUTOMATIC CONTROL

THE CONTROL SIGNAL TO BE APPLIED AT TIME T IS COMPUTED FROM

$$U(T) = (AE(1)*(Y(T)-Y_0) + \dots + AE(NA)*(Y(T-NA+1)-Y_0)) / B_0 - BE(1)*U(T-1) - \dots - BE(NB)*U(T-NB) \quad (*)$$

WHERE Y_0 IS THE REFERENCE VALUE OF Y . $AE(I)$ AND $BE(I)$ ARE THE LEAST SQUARES ESTIMATES FROM THE SUBROUTINE TUNE

YS-VECTOR OF SCALED PROCESS OUTPUTS OF DIMENSION $NA+K+MSTEP+1$
YS IS SHIFTED ONE STEP IN REG AND IS BEFORE THE SHIFT ORGANIZED AS FOLLOWS

$$YS(1) = (Y(T) - Y_0) / B_0$$
$$YS(2) = (Y(T-1) - Y_0) / B_0$$

U-VECTOR OF PROCESS INPUTS OF DIMENSION $NB+K+MSTEP+1$
U IS SHIFTED ONE STEP IN REG AND IS BEFORE THE SHIFT ORGANIZED AS FOLLOWS

$$U(1) = U(T-1)$$
$$U(2) = U(T-2)$$

T-VECTOR OF ESTIMATED PARAMETERS OF DIMENSION $NA+NR$ AND IS ORGANIZED AS FOLLOWS ($AE(I)$ DENOTES THE ESTIMATED VALUE OF $A(I)$, ETC.)

$$T(1) = AE(1)$$
$$T(2) = AE(2)$$

$$T(NA) = AE(NA)$$
$$T(NA+1) = BE(1)$$

$$T(NA+NB) = BE(NB)$$

NA-NUMBER OF A-PARAMETERS IN (*)
NB-NUMBER OF B-PARAMETERS IN (*)
K-NUMBER OF PURE TIME DELAYS IN THE PROCESS

SUBROUTINES REQUIRED
NONE

DIMENSION YS(1),U(1),T(1)

COMPUTE CONTROL SIGNAL

```
R=0.  
DO 10 I=1,NA  
R=R+T(I)*YS(I)  
IF (NB) 21,21,11  
DO 20 I=1,NR  
L=NA+I  
R=R-T(L)*U(I)  
NS=NR+K+MSTEP  
DO 30 I=1,NS
```

30 L=NS+1-I
U(L+1)=U(L)
U(1)=R

2 REORGANIZE DATA
NS=NA+K+MSTEP
DO 40 I=1,NS
10 L=NS+1-I
YS(L+1)=YS(L)
RETURN
END

```

001 C      TASK PRINT
002 C
003 C      PRINTS PROCESS DATA ON LUN 6 (LP)
004 C
005 C      RUNS IN PARTITION PUSER
006 C      DEFAULT PRIORITY 350
007 C
008 C      AUTHOR: ULF BORISSON   1972-11-15
009 C
010 C      SUBROUTINES REQUIRED
011 C          BCDIO (OLD VERSION)
012 C
013 C
014 C      DIMENSION IYA(10)
015 C
016 C      COMMON ISYSA(25), IOA(26), MPXA(40), ICOMVA(45), FLA1(16), FLA0(8)
017 C      IUSER(36)
018 C
019 C      COMMON/SLASK/ IDUM(704),
020 C      INA, NB, K, NSTEP, MSTEP, IPOINT, NCHAN, IYCHAN, ICOUN,
021 C      IB0, RL, PDIAG, YREF, UMAX, UMIN, UTOT, DUMAX, UPI, DUPI,
022 C      YMIN, YMAX,
023 C      IT(10), P(10,10), YS(10), U(10), YA(10), IDATE(6),
024 C      IUTOT
025 C
026 C      EQUIVALENCE
027 C      1(IT, ISYSA(17)),
028 C      1(IEXT7, ISYSA(24)),
029 C      1(IEXT8, ISYSA(25)),
030 C      1(REQNM1, ICOMVA(31)),
031 C      1(IEV2, ICOMVA(42)),
032 C      1(IEV3, ICOMVA(43)),
033 C      1(IEV4, ICOMVA(44))
034 C
035 C      CALL PAXA(IEV3)
036 C      GO TO (100,200,300), IEXT8
037 C
038 C      PRINT PROCESS DATA
039 C
040 C      100 WRITE(6,1100) (IDATE(I), I=4,6), (IDATE(J), J=1,3)
041 C      WRITE(6,1110) NA, NB, K, NSTEP, MSTEP
042 C      WRITE(6,1120) B0, RL, PDIAG, YREF
043 C      WRITE(6,1125) YMIN, YMAX
044 C      WRITE(6,1130) UMAX, UMIN, UTOT, DUMAX
045 C      WRITE(6,1131) IT, NCHAN, IYCHAN
046 C      WRITE(6,1132) IEXT4, IEXT7
047 C      L=NA+NB
048 C      WRITE(6,1134) (T(I), I=1,L)
049 C      WRITE(6,1140) REQNM1
050 C      WRITE(6,1150)
051 C      GO TO 999
052 C
053 C      200 L=NA+NB
054 C      DO 230 I=1, NCHAN
055 C      230 IYA(I)=IFIX(YA(I))
056 C      DEFF=YS(1)*80
057 C
058 C      ICOUN=ICOUN+1
059 C      WRITE(6,1200) ICOUN, IPOINT, (IYA(I), I=1,5), DUPI, UPI,
060 C      DEFF, U(1), UTOT, IUTOT, (T(J), J=1,L)
061 C
062 C      GO TO 999
063 C

```



```

001 C TASK TAPE
002 C
003 C WRITES DATA FROM THE SELF TUNING REGULATOR ON TAPE (LUN 14)
004 C
005 C RUNS IN PARTITION PUSER
006 C DEFAULT PRIORITY 400
007 C
008 C AUTHOR: ULF BORISSON 1972-11-15
009 C
010 C SUBROUTINES REQUIRED
011 C BINIO (OLD VERSION)
012 C
013 C DIMENSION KOD(10),A(1,30)
014 C
015 C COMMON /SYSA(25),IOA(26),MPXA(40),ICOMVA(45),FLAI(16),FLAO(8),
016 C /USER(36)
017 C
018 C COMMON/SLASK/ IDUM(704),
019 C INA,NB,K,NSTEP,MSTEP,IPOINT,NCHAN,IYCHAN,ICOUN,
020 C IB0,RL,PDIAG,YREF,UMAX,UMIN,UTOT,DUMAX,UPI,DUPI,
021 C IYMIN,YMAX,
022 C IT(10),P(10,10),YS(10),U(10),YA(10),IDATE(6),
023 C IUTOT
024 C
025 C EQUIVALENCE
026 C 1(IT,ISYSA(17)),
027 C 1(IEXT5,ISYSA(22)),
028 C 1(IEXT6,ISYSA(23)),
029 C 1(REQNM1,ICOMVA(31)),
030 C 1(IEV3,ICOMVA(43)),
031 C 1(IEV4,ICOMVA(44))
032 C
033 C
034 C GO TO (100,200,300),IEXT6
035 C
036 C OPEN FILE AND WRITE INITIAL DATA
037 C
038 100 CONTINUE
039 KOD(1)=0
040 KOD(2)=7+NA+NB
041 KOD(3)=0
042 KOD(4)=IT
043 KOD(5)=IDATE(5)*10000+IDATE(4)*100+IDATE(6)
044 KOD(6)=IDATE(1)*100+IDATE(2)
045 KOD(7)=1
046 KOD(8)=0
047 KOD(9)=0
048 KOD(10)=0
049 C
050 CALL ENTER(14,REQNM1,'BIN',IEV4)
051 CALL WAITER(IEV4)
052 IF (IEV4) 110,120,120
053 110 IEXT5=5
054 CALL REQST(5HERROR,0)
055 C
056 120 WRITE(14) (KOD(I),I=1,10)
057 GO TO 999
058 C
059 C WRITE DATA FROM ONE SAMPLE POINT
060 C
061 200 CONTINUE
062 CALL PAXA(IEV3)
063 C

```

```

064      A(1,1)=FLOAT(IPJINT)
065      A(1,2)=YA(IYCHAN)*0.4651
066      A(1,3)=YA(2)/160.
067      A(1,4)=YA(3)*1.212
068      C
069      A(1,5)=YS(1)*80
070      A(1,6)=U(1)
071      A(1,7)=UTOT
072      IA=8
073      C
074      L=IA+NA+NB
075      J=0
076      DO 250 I=IA,L
077      J=J+1
078      250 A(1,I)=T(J)
079      C
080      WRITE(14) (A(1,J),J=1,L)
081      IEV3=1
082      GO TO 999
083      C
084      C      CLOSE FILE
085      C
086      300      CONTINUE
087      CALL CLOSE(14,REQNM1,'BIN',IEV4)
088      CALL WAITFR(IEV4)
089      IF (IEV4) 310,999,999
090      310      IEXT5=6
091      CALL REQST(5HERROR,0)
092      GO TO 999
093      C
094      999      CALL EXIT
095      GO TO 999
096      END

```


/ TASK SEND
/
/ SENDS DATA FROM THE LAST CELL IN COMMON/SL/
/
/ RUNS IN PARTITION PIRUS
/ DEFAULT PRIORITY 250
/
/ AUTHOR: LEIF ANDERSSON 1972-11-15
/
/ SUBROUTINES REQUIRED
/ NONE
/
/

```
704026 A      TLS2=704026      /LOAD BUFFER, PRINT AND CLEAR FLAG  
00000 R 220003 R START LAC* (20707)  
00001 R 704026 A      TLS2  
00002 R 000004 R      CAL (10)  
00000 R      000000 R      .END START  
00003 R 020707 A *L  
00004 R 000010 A *L  
SIZE=00005 NO ERROR LINES
```