Antimonide Heterostructure Nanowires - Growth, Physics and Devices

Borg, Mattias

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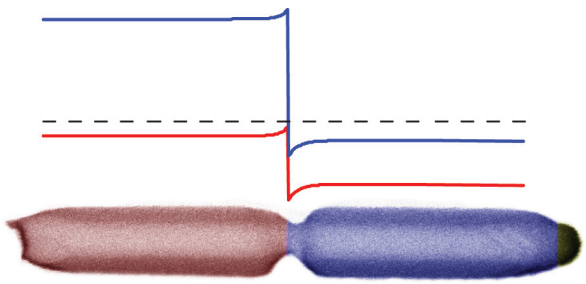

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Division of Solid State Physics
Department of Physics
Lund University 2012

Antimonide Heterostructure Nanowires

- Growth, Physics and Devices

Doctoral Thesis

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Abstract

This thesis investigates the growth and application of antimonide heterostructure nanowires for low-power electronics. In the first part of the thesis, GaSb, InSb and InAsSb nanowire growth is presented, and the distinguishing features of the growth are described. It is found that the presence of Sb results in more than 50 at. % group-III concentration in the Au seed particle on top of the nanowires. It is further concluded that the effective V/III ratio inside the seed particle is reduced compared to the outside. This enables the suppression of radial growth with remaining high axial growth rate. Furthermore, the low effective V/III ratio may affect the crystal structure formation, which is pure Zinc-blende in all investigated Sb-based nanowires. The strong segregating properties of Sb results in a strong Sb memory effect, and a difficulty to nucleate Sb-based nanowires directly on substrates.

The second part of the thesis deals with the growth and application of GaSb/InAs(Sb) nanowires for tunnel device applications. The GaSb/InAs(Sb) nanowire heterojunction has a defect-free crystal structure with an extremely abrupt heterojunction due to an inherent delay before the initiation of InAs (Sb) growth. The Sb carry-over from the GaSb growth step into the InAs growth leads to a high Sb background in the InAs(Sb) segment. The diameter of the heterojunction can be reduced below 30 nm by an in-situ annealing treatment, in which material is selectively etched from the region near the heterojunction.

The performance of GaSb/InAs(Sb) tunnel diodes is modeled and measured on fabricated single nanowire devices. The diodes exhibit peak current levels of 67 kA/cm^{2} , peak-to-valley current ratio between 2 and 3 at room temperature and a tunnel current at V_{D} = -0.5 V of 1.7 MA/cm^{2} . The expected performance of GaSb/InAs(Sb) tunnel field-effect transistors is discussed and preliminary measurement data on top-gated devices with 300 nm gate length is also presented.

Key words: Nanowires, epitaxy, antimonides, tunnel diode, tunnel field effect transistors, GaSb, InSb, InAsSb

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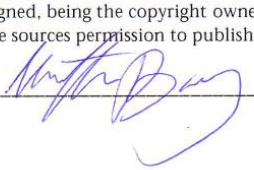
Signature 

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Doctoral Thesis

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Cover: SEM image of a GaSb/InAsSb heterostructure nanowire with a selectively etched heterojunction. The calculated band structure of the heterostructure is also displayed.

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To June, my inspiration.

The best way to have a good idea is to have a lot of ideas.

Linus Pauling (1901-1994)

Contents

Abstract

This thesis investigates the growth and application of antimonide heterostructure nanowires for low-power electronics. In the first part of the thesis, GaSb, InSb and InAsSb nanowire growth is presented, and the distinguishing features of the growth are described. It is found that the presence of Sb results in more than 50 at. % group-III concentration in the Au seed particle on top of the nanowires. It is further concluded that the effective V/III ratio inside the seed particle is reduced compared to the outside. This enables the suppression of radial growth with remaining high axial growth rate. Furthermore, the low effective V/III ratio may affect the crystal structure formation, which is pure Zinc-blende in all investigated Sb-based nanowires. The strong segregating properties of Sb results in a strong Sb memory effect, and a difficulty to nucleate Sb-based nanowires directly on substrates.

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Populärvetenskaplig sammanfattning

Om man idag frågar människor om de skulle klara sig utan datorn eller mobiltelefonen skulle de allra flesta utan tvekan svara nej. Elektroniken har blivit själva blodomloppet i vårt samhälle, och vi sköter vårt arbete, vardag och nöjen med hjälp av datorer. Vi betalar våra räkningar via internet, beställer flygbiljetter online, lyssnar på musik på från mobiltelefonen, och när tåget är försenat delar vi vår frustration med vännerna på Facebook. På gott och ont så är dagens samhälle definitivt ett resultat av de senaste femtio årens elektronikrevolution.

Den moderna datorn har sett ungefär likadan ut sedan mitten av 1900-talet, då datorns motsvarighet till hjärnceller uppfanns, nämligen transistorn och den integrerade kretsen. Sedan dess har datorns beräkningskraft och effektivitet ökats genom storleken på transistorerna har minskats och man har på så sätt fått plats med många fler transistorer i samma krets. Precis som att det är fördelaktigt med fler hjärnceller i en hjärna så har klipskheten hos datorerna också ökat allt eftersom de fått fler och snabbare transistorer. Idag innehåller datorns hjärna (processorn) så många som 1 miljard transistorer, och alla dessa får plats på ett kretskort stort som en tumnagel.

Tyvärr finns det en gräns för hur små man kan göra datorns transistorer. Denna gräns bestäms av storleken på atomen. Dagens transistorer börjar faktiskt närma sig denna gräns vilket gör att man inte kan minska deras storlek mycket mer. Istället har man ökat prestandan i kretsarna genom att öka effektförbrukningen. Detta har lett till att datorer idag drar mycket energi (och blir väldigt varma), vilket går stick i stäv med det mobila samhället där lång batteritid i elektronik har blivit allt viktigare. Dessutom är elektronikens höga energiförbrukning även förödande för miljön, och det är därför viktigt att efterforska nya lös-

ningar som kan minska energikonsumtionen i världens elektronik och i bästa fall även möjliggöra för en fortsatt ökad prestanda.

Denna avhandling behandlar en sådan eventuell lösning, nämligen ultratunna kristaller kallade nanotrådar. Nanotrådar är mindre än hundra nanometer i diameter, vilket motsvarar endast cirka tusen atomer. Deras längd är ofta tusen gånger längre än diametern och de ser därför ut som smala cylindrar. I nanotrådar kan man sätta ihop material som normalt inte går ihop och därmed öppnas nya möjligheter för att realisera elektronik som tidigare inte varit möjlig. Nanotrådar kan växas med hjälp av små guldpartiklar som lagts på en kristall-platta. Denna platta läggs in i en ugn vilken hettas upp till mycket hög temperatur. Genom att tillföra en ånga av speciella ämnen kan man få guldpartiklarna att samla in atomer och spotta ut dem igen undertill. Resultatet blir att nanotrådar växer fram med varsin guldpartikel på toppen.

En nanotrådskristall kan bestå av mer än ett material genom att man varierar ångans sammansättning under växtens gång. Nanotrådarna kallas i detta fall för en heterostruktur. När olika material kombineras kan trådarna komma att bete sig helt annorlunda jämfört med när de endast består av ett material. Detta ger ökade möjligheter för att designa innovativa elektroniska komponenter i nanotrådar.

Antimon (Sb) är en relativt tung atom som kan bilda halvledande kristaller tillsammans med atomer från grupp III i periodiska systemet (B, Al, Ga och In). Dessa material har bra elektriska egenskaper vilket gör dem attraktiva för framtidens elektronik. Det är dock ofta svårt att producera heterostrukturer av hög kristallkvalitet i dessa material, och i denna avhandling studeras därför nanotrådsväxt av Sb-baserade material som ett alternativt sätt att åstadkomma dessa heterostrukturer. Sb-baserade nanotrådar har inte tidigare studerats i detalj och är därför intressanta även ur ett grundforskningsperspektiv. Växt av GaSb, InSb och InAsSb-nanotrådar behandlas i artikel I-VII.

En särskild heterostruktur som är av stort intresse för framtidens elektronik är GaSb/InAsSb. Denna heterostruktur kan verka som ett filter vilket "kyler" av strömmen som leds igenom den. En sådan kall ström möjliggör transistorer som kan stängas av mycket mer effektivt än dagens och som förbrukar 50-75% mindre energi. Dioder och transistorer av GaSb/InAsSb-nanotrådar har studerats i denna avhandling, och behandlas i artikel VI-IX.

Sammantaget har arbetet som presenteras i denna avhandling möjliggjort utvecklingen av Sb-baserade nanotrådar från att ha varit helt okända strukturer till att nu framgångsrikt implementeras i innovativ heterostruktur-elektronik.

List of Papers

The author changed his last name from Jeppsson to Borg during the course of his PhD studies.

I *Growth of GaAs/GaSb nanowire heterostructures using MOVPE*
M. Jeppsson, K.A. Dick, J.B. Wagner, P. Caroff, K. Deppert, L. Samuelson and L.-E. Wernersson, *J. Cryst. Growth* **310**, 4115-4121 (2008)

I wrote the paper, did the epitaxial growth and analyzed the data.

II *Characterization of GaSb nanowires grown by MOVPE*
M. Jeppsson, K.A. Dick, H.A. Nilsson, N. Sköld, J.B. Wagner, P. Caroff, and L.-E. Wernersson, *J. Cryst. Growth* **310**, 5119-5122 (2008)

I wrote the paper, did epitaxial growth, HRXRD, and the growth simulation.

III *High-quality InAs/InSb nanowire heterostructures grown by MOVPE*
P. Caroff, J.B. Wagner, K.A. Dick, H.A. Nilsson, **M. Jeppsson**, K. Deppert, L. Samuelson, and L.-E. Wernersson, *Small* **4** (7), 878-882 (2008)

I participated actively in the discussions regarding the data.

IV *InAs/InSb heterostructure nanowires: MOVPE growth under extreme lattice mismatch*
P. Caroff, M.E. Messing, **B.M. Borg**, K.A. Dick, K. Deppert, and L.-E. Wernersson, *Nanotechnology* **20**, 495606 (2009)

I coordinated the project, did part of the epitaxial growth, and took part in writing the paper.

V *Enhanced Sb incorporation in InAsSb nanowires grown by MOVPE*
B.M. Borg, K.A. Dick, J. Eymery, and L.-E. Wernersson, *Appl. Phys. Lett.* **98**, 113104 (2011)

I planned the project, wrote the paper, did the epitaxial growth and HRXRD.

VI *InAs/GaSb Nanowires for Tunnel Field-Effect Transistors*
B.M. Borg, K.A. Dick, B. Ganjipour, M.-E. Pistol, L.-E. Wernersson and C. Thelander, *Nano Lett.* **10** (10), 4080-4085 (2010)

I planned the project, wrote the paper, did the epitaxial growth and data analysis.

VII *Formation of a sharp GaSb/InAs heterointerface in nanowires with high crystal quality*
M. Ek, **B.M. Borg**, A.W. Dey, B. Ganjipour, C. Thelander, L.-E. Wernersson and K.A. Dick, *Cryst. Growth & Design* **11** (10), 4588-4593 (2011)

I was heavily involved in the project, did the epitaxial growth, and took part in writing the paper.

VIII *Diameter Reduction of Nanowire Tunnel Heterojunctions using In-Situ Annealing*
B.M. Borg, M. Ek, K.A. Dick, B. Ganjipour, A.W. Dey, C. Thelander and L.-E. Wernersson, *Appl. Phys. Lett.* **99**, 203101 (2011)

I planned the project, did the annealing experiments and wrote the paper.

IX *High Current Density Esaki Tunnel Diodes Based on GaSb-InAsSb Heterostructure Nanowires*
B. Ganjipour, A.W. Dey, **B.M. Borg**, M. Ek, M.-E. Pistol, K.A. Dick, L.-E. Wernersson and C. Thelander, *Nano Lett.* **11** (10), 4222-4226 (2011)

I was heavily involved in the project, did the modeling and took part in writing the paper.

Papers not included in thesis

x *MOVPE growth and and structural characterization of extremely lattice-mismatched InP-InSb nanowire heterostructures*
B.M. Borg, M.E. Messing, P. Caroff, K.A. Dick, K. Deppert and L.-E. Wernersson, *Indium Phosphide and Related Materials (IPRM)* (2009)

xi *Vertical InAs Nanowire Wrap Gate Transistors with f_t>7GHz and f_{max}>20GHz*
M. Egard, S. Johansson, A.-C. Johansson, K.-M. Persson, A.W. Dey, **B.M. Borg**, C. Thelander, L.-E. Wernersson and E. Lind, *Nano Lett.* **10** (3), 809-812 (2010)

xii *Analysis of strain and stacking faults in single nanowires using Bragg coherent diffraction imaging*
V. Favre-Nicolin, F. Mastropietro, J. Eymery, D. Camacho, Y.M. Niquet, **B.M. Borg**, M.E. Messing, L.-E. Wernersson, R.E. Algra, E.P.A.M. Bakkers, T.H. Metzger, R. Harder and I.K. Robinson, *New J. Physics* **12**, 035013 (2010)

xiii *Uniform and position-controlled InAs nanowires on 2" Si substrates for transistor applications*
S. Gorji Ghalamestani, S. Johansson, **B.M. Borg**, E. Lind, K.A. Dick and L.-E. Wernersson, *Nanotechn.* **23**, 015302 (2011)

xiv *RF Characterization of Vertical InAs Nanowire Wrap-Gate Transistors Integrated on Si Substrates*
S. Johansson, M. Egard, S.G. Ghalamestani, **B.M. Borg**, M. Berg, L.-E. Wernersson and E. Lind, *IEEE Trans. Microwave Theory Tech.* **59** (10), 2733-2738 (2011)

xv *Temperature and annealing effects on InAs nanowire MOSFETs*
S. Johansson, S.G. Ghalamestani, **M. Borg**, E. Lind, L.-E. Wernersson, *Microelectron. Eng.* **88** (7), 1105-1108 (2011)

xvi *Self-Aligned Gate-Last Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFET with Selectively Regrown Source and Drain Contact Layers*
M. Egard, L. Ohlsson, **B.M. Borg**, L.-E. Wernersson and E. Lind, *IEEE Device Research Conference (DRC), 69th Annual* (2011)

xvii *High Transconductance Self-Aligned Gate-Last Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFET*
M. Egard, L. Ohlsson, **B.M. Borg**, F. Lenrick, L.-E. Wernersson, E. Lind, *IEEE International Electron Device Meeting (IEDM)* (2011)

xviii *15 nm diameter InAs nanowire MOSFETs*
A.W. Dey, C. Thelander, M. Borgström, **B.M. Borg**, E. Lind, L.-E. Wernersson, *IEEE Device Research Conference (DRC), 69th Annual* (2011)

xix *Interface composition of InAs nanowires with Al_2O_3 and HfO_2 thin films*
R. Timm, M. Hjort, A. Fian, **B.M. Borg**, C. Thelander, J.N. Andersen, L.-E. Wernersson, and A. Mikkelsen, *Appl. Phys. Lett.* **99**, 222907 (2011)

xx *GaSb Nanowire Single-Hole Transistor*
B. Ganjipour, H. A. Nilsson, **B.M. Borg**, L.-E. Wernersson, L. Samuelson, H.Q. Xu, C. Thelander, *Appl. Phys. Lett.* in press.

Abbreviations

at. %	Atomic percent
CBE	Chemical Beam Epitaxy
CMOS	Complementary Metal-Oxide-Semiconductor
DHBT	Double Heterojunction Bipolar Transistor
DOS	Density of states
FET	Field-Effect Transistor
HEMT	High Electron Mobility Transistor
HRTEM	High Resolution Transmission Electron Microscopy
HRXRD	High-Resolution X-Ray Diffraction
LWIR	Long Wavelength Infrared
MBE	Molecular Beam Epitaxy
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOVPE	Metal-Organic Vapour Phase Epitaxy
NDR	Negative Differential Resistiance
RSM	regular solution model
SEM	Scanning Electron Microscopy
SL	Superlattice
SS	Subthreshold Swing
STEM	Scanning Transmission Electron Microscopy

TDMASb	Tris(dimethylamino)antimony
TD	Tunnel Diode
TEGa	Triethylgallium
TEM	Transmission Electron Microscopy
TESb	Triethylantimony
TFET	Tunneling Field-Effect Transistor
TMGa	Trimethylgallium
TEIn	Triethylindium
TMIn	Trimethylindium
TMSb	Trimethylantimony
TPB	Three-Phase Boundary
TSL	Twin-plane Super Lattice
VLS	Vapour-Liquid-Solid
WKB	Wentzel-Kramers-Brillouin
WZ	Wurtzite
XEDS	X-ray Electron Dispersive Spectroscopy
ZB	Zinc-blende

Chapter 1

Background

Modern semiconductor technology began with the invention of the *trans*fer res*istor* (transistor) by John Bardeen, Walter Brattain and William Shockley at Bell Labs in 1947. The purpose of a transistor is to modulate the amount of electric current in a conduit between two connected electrodes via the electric potential applied to a third electrode. The transistor is thus an amplification device, because small voltage variations in the control electrode are transferred to the larger current in the conduit. The control electrode may also completely prevent current from flowing through the device.

The first transistor consisted of Au contacts and a semiconducting Ge crystal on top of a Cu base contact. In their first experiments, the team at Bell Labs connected a microphone and a speaker via the transistor and could thus amplify their spoken voices. This was the beginning of the electronic revolution which would completely change the world. Today the transistor is the most important fundamental building block in logic circuits and amplifiers, and there are transistors in practically every type of electronic device; from cell phones and computers to credit cards and satellites.

The second technological leap came with the invention of the integrated circuit based on the complementary metal-oxide-semiconductor (CMOS) field-effect transistor (FET) technology. By then Ge had been replaced by Si as the active semiconductor material in transistors. Si is one of the most abundant materials on earth and is as such relatively inexpensive. The main reason for the change, however, was that the Si native oxide, SiO_2, forms a very good interface to Si, thus enabling the highly controllable inversion mode operation of standard CMOS FETs [1]. With integrated circuits, thousands of transistors could be integrated on a single chip, enhancing the complexity and computational power of logic circuits by orders

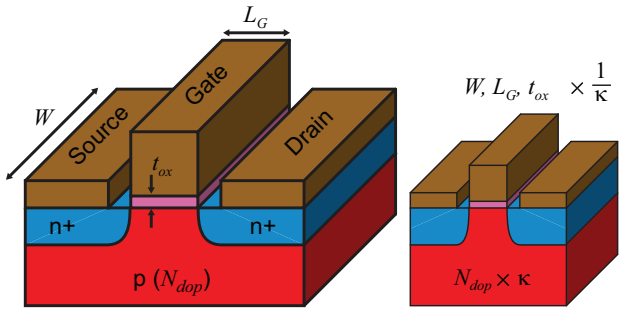

Figure 1.1: *Schematic illustration of a Si MOSFET, and how it is scaled by a factor* $\kappa > 1$.

of magnitude.

Since its invention, Si CMOS technology has been the fundament of the semiconductor industry and development of the transistor has mainly consisted of scaling down its dimensions (See Figure 1.1). In 1965 a guy named Gordon Moore predicted that the number of transistors on an integrated circuit would double every 18 months. As it happens, Mr Moore is the co-founder of Intel, and thus the industry took him very seriously and have worked extremely hard to keep fulfilling his prophecy (denoted Moore's law) for the rest of the 20th century. The scaling of CMOS circuits follows specified rules to keep the electric field in the devices constant. In Table 1.1 the effect of scaling a CMOS device by a factor of κ (> 1) are shown. Most noteworthy is that the intrinsic delay time, τ, is decreased by $1/\kappa$, thus meaning that smaller CMOS equals faster operation frequency ($f \sim 1/\tau$). Also the power-delay product, which is a good measure of the power efficiency of the circuit is effectively decreased by scaling ($1/\kappa^3$). Packing more transistors onto the same chip area thus equals a more power efficient circuit. Today there are roughly a billion transistors in a single computer processor, giving modern computers a fantastic calculating power.

1.1 The end of Scaling

Until about the year 2005 Moore's law has provided a practical road-map for the scaling rate of CMOS technology. There is a limit, however, to how small you can make a transistor. This fundamental limit to scaling is ultimately set by the finite size of the atom which is around 0.1 nm. Scaling beyond the size of the atom while still maintaining the same device operation is of course impossible. But long before this fundamental limit is

Parameters	Multiplication factors
Device dimensions, L_G, t_{ox}, W	$1/\kappa$
Channel doping level, N_{dop}	κ
Supply Voltage, V_{dd}	$1/\kappa$
Electric field	1
Output current, I_D	$1/\kappa$
Active device area, $A = L_G W$	$1/\kappa^2$
Gate Capacitance, $C_G = \varepsilon_{ox} A/t_{ox}$	$1/\kappa$
Intrinsic delay, $\tau \sim C_G V_{dd}/I_D$	$1/\kappa$
Power-delay product, $P \cdot \tau \sim I_D V_{dd} \cdot \tau$	$1/\kappa^3$

Table 1.1: Rules for constant electric field scaling of Si CMOS.

reached one runs into problems. This is because some parameters do not scale, for example the size of the electronic band gap of the semiconductor and the thermal excitation energy (kT). Even Moore himself confessed in an interview in 2005 [2] that:

> "It can't continue forever. The nature of exponentials is that you push them out and eventually disaster happens."

And indeed, in recent years the CMOS scaling rate has decreased and Moore's law is no longer perfectly valid. The major obstacles are a large increase in both the active (∼30 %) and passive (∼300 %) power dissipation with each sucessive CMOS generation [3]. The active power dissipation originates in a difficulty in scaling down the supply voltage, V_{dd}, and threshold voltage, V_T, with maintained on-current, I_{on}, without increasing the off-state current, I_{off}. This is limited by the inverse subthreshold slope, or subthreshold swing (SS) defined as

$$\mathrm{SS} = \left[\frac{\partial(\log_{10} I_D)}{\partial V_G}\right]^{-1} \tag{1.1}$$

which sets how much gate voltage change is required to turn off the device, and cannot be decreased below the thermal limit ($kT/q \times \ln(10) \approx 60$ mV/dec) in conventional MOSFETs (See Figure 1.2).

The passive power dissipation has become an increasing problem in the latest CMOS generations. A major contributor to the passive power is the electron tunneling current through the gate oxide, which increases exponentially with decreasing oxide thickness. Because of this, the gate oxide thickness (t_{ox}) was not reduced further between the 90 and the 65-nm nodes

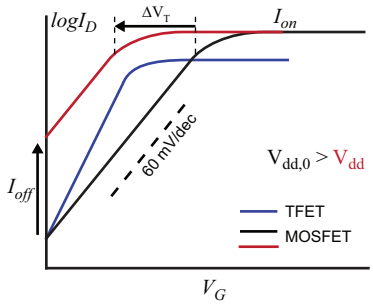

Figure 1.2: *Schematic image showing why I_{off} is increases when V_{dd} and V_T are reduced to maintain I_{on}. SS is limited to* 60 mV/dec *for MOSFETs.*

(2006), which limited the performance improvement. Since then, new materials and device geometries have been entering the manufacturing lines. For example, in Intel's 45-nm (2008) and 32-nm (2010) processes a significant step away from the standard CMOS process was introduced. The SiO_2 gate dielectric was exchanged for a high-κ dielectric (HfO_2), and metal gate electrodes were also introduced. These changes enabled a thicker oxide to be used to reduce gate leakage, while still maintaining a high capacitance between gate and channel. An even greater change in the process flow is that Intel recently announced that it would use a Tri-gate structure with multiple wire-shaped channels for its 22-nm node process (2011-2012). This is a major step, as it is the first time that a non-planar MOSFET is used in a commercial production line. The tri-gate structure improves the electrostatic control over the channel, and allows for further scaling down the gate length without losing device performance to short-channel effects. With tri-gate MOSFETs now in mass-production, it is clear that the semiconductor industry is opening up for novel device concepts to be able to meet the demands for increased computing power and low power consumption.

1.2 The next generation of electronics

With scaling of planar Si-CMOS no longer a long-term option, other approaches to improved device performance are investigated. The specific approach dealt with in this thesis is III-Sb nanowires for tunneling devices. To motivate this choice, the benefits of III-V semiconductors and nanowires for electronics are introduced here.

1.2.1 III-V semiconductor channels

The faster electrons can cross the channel of a transistor, the faster the transistor can respond to a varying gate potential. Additionally, a better performance is obtained due to a higher drive current. The main parameters which determine the transport properties of carriers in a semiconductor are the carrier mobilities, μ_e and μ_h, for electrons and holes, respectively. At low and moderate electric fields, F, the carrier velocity is a linear function in F ($v_e = \mu_e F$).[1] A high value of μ is thus beneficial for the device performance, and an enhanced mobility can be obtained by straining the channel material along the transport direction [4] or by choosing a channel material with a higher bulk mobility value. In Table 1.2 the properties of common III-V semiconductors are compared with Si and Ge. The III-V semiconductors, such as GaAs, InAs and InSb are attractive substitutes for Si because of their higher electron mobilities. InAs and InSb in particular have roughly 18 and 55 times higher bulk electron mobility compared to Si, and are suitable for n-type devices. For the same reason Ge and strained GaSb [5] would be best suited for p-type devices. However, by exchanging the channel material one also alters other important parameters, such as the lattice parameter, band gap and density of states.

The **lattice parameter** is the width of the crystal unit cell and is important to consider for the successful integration of one material onto another, since a difference in lattice parameter between two materials induces defects at the heterointerface. Because GaAs and Ge are essentially lattice-matched (have the same lattice parameter) there are strong efforts to combine these two materials into a CMOS architecture. The move to III-V nMOS and Ge pMOS has even been included into the International Technology Roadmap for Semiconductors for the 16-nm node [6].

The **band gap** is the width of the gap of forbidden electron energies in the crystal band structure. This determines the maximum light absorption wavelength and also the intrinsic carrier concentration of the material. In a transistor a wide band gap equals a large breakdown voltage and low minimum off-state currents [7].

The **density of states** (DOS) describes how many available electron states there are at a specific energy, and thus determines how many free charge carriers there can be in a device. It is beneficial to have a large DOS in a transistor, to obtain high current levels. In three dimensions the DOS depends on the effective mass, m_{eff}, as DOS$\sim m_{eff}^{3/2}$. Thus, a low effective

[1] At high electric fields the velocity saturates because of scattering processes which are extremely efficient at high electric fields ($v = v_{sat}$).

	Si	Ge	GaAs	GaSb	InAs	InSb
a_0 (Å)	5.431	5.658	5.653	6.096	6.058	6.479
E_g (eV)	1.12	0.66	1.42	0.726	0.354	0.17
μ_e (cm^2/Vs)	1400	3900	8500	3000	25000	77000
μ_h (cm^2/Vs)	450	1900	400	1000	500	850
m^c_{eff} ($\times 10^{-2}$)	m_l=98 m_t=19	m_l=159 m_t=8.2	6.3	4.1	2.3	1.4

Table 1.2: *Comparison of the lattice parameter (a_0), band gap (E_g), electron mobility (μ_e), hole mobility (μ_h) and conduction band effective mass (m^c_{eff}) of common semiconductors. Data from Ref.[9].*

mass means a small DOS. Since a high electron mobility usually correlates with a low electron effective mass it has been argued that the low DOS of InAs and InSb may ultimately limit the usefulness of these materials in III-V CMOS [8].

Despite the beneficial properties of the III-V semiconductors it is highly unlikely that they will completely replace Si in large-scale logic circuits. The main reason for this is the relative scarceness of the group-III and -V materials on Earth, which makes Si wafers the only economically viable choice for production in large quantities. In addition, the semiconductor industry has invested countless billions of dollars into facilities and research devoted to Si processing. Thus if Ge and III-V materials are to be used in CMOS, they must be integrated into the Si process flow [1].

1.2.2 Semiconductor nanowires for electronic devices

As device dimensions are scaled down to the sub-20-nm range it becomes extremely difficult to define device patterns by optical lithography techniques. An alternative approach is to let nature do the work, and allow at least parts of the device self-assemble. This is the core idea behind nanostructures; self-assembled structures with at least one dimension below 100 nm [10]. Important classes of nanostructures are DNA-strands, nanoparticles, semiconductor quantum dots and nanowires, carbon nanotubes and graphene. This thesis focuses on semiconductor nanowires, but it is important to note that other material systems are also important for electronics, in particular nanotubes and graphene.

Self-assembled semiconductor nanowires are thin and long semiconduc-

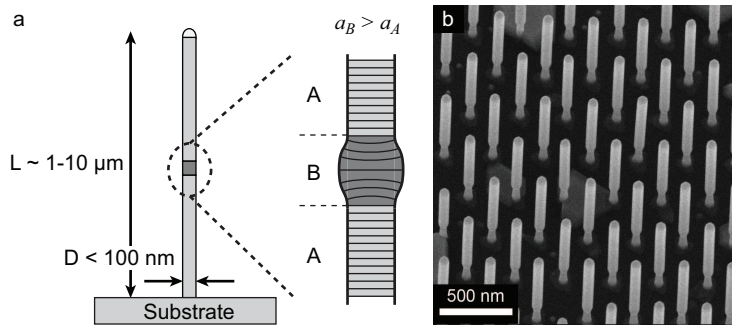

Figure 1.3: *(a) Schematic image of a nanowire of material A with a small insert of another material (B) with larger lattice parameter. The zoomed-in schematic visualizes how elastic strain may be relaxed by radial expansion in nanowires. (b) SEM image of an ordered InAs/InSb nanowire array grown on an InAs substrate with 7% lattice-mismatch (30° tilt angle).*

tor crystals which grow epitaxially out from a crystalline substrate (Figure 1.3). Nanowires have been demonstrated in a multitude of materials, including Si, Ge and all the Ga- and In-based III-V semiconductors. Nanowires with diameter far below 10 nm have been demonstrated [11, 12] and the structures are thus promising building blocks for future scaled down electronic devices.

Crystal lattice-mismatch can cause enormous problems when integrating different materials into heterostructures. High strain energies are released to form misfit dislocations which are detrimental for the device performance. Due to their small radial dimension, the requirement for lattice-matching is relaxed in heterostructure nanowires. Inside a nanowire a free edge is always near, and strain due to lattice-mismatch can be released simply by expanding (or contracting) the edge of the structure (Figure 1.3a). One is thus not as limited in the choice of material by the requirement of lattice-matching, and nanowires thus constitute a viable approach to III-V integration on Si substrates. As an example of a successful integration of two highly lattice-mismatched materials, a typical ordered array of InSb nanowires grown on an InAs substrate (7% lattice-mismatch) is shown in Figure 1.3b.

Another possible benefit of nanowires is the vertical geometry which enables vertical transistors where the gate length can be controlled with high precision through the deposited metal thickness. Additionally, wrap-all-around gate electrodes and the thin one-dimensional nanowire channels give an opportunity for ideal channel control. For example, vertical wrap-gate InAs nanowire transistors on Si have been demonstrated by our group

with decent RF performance (f_t = 9.3 GHz, f_{max} = 20 GHz) limited at this stage by parasitic resistances and capacitances [13].

The nanowire geometry is also a practical geometry for realizing steep-slope devices such as tunneling field effect transistors (TFETs). The cylindrical geometry simplifies gate positioning at the tunnel junction, and the possibility to combine lattice-mismatched materials gives a great flexibility in the design of the tunnel junction. Furthermore, one-dimensional transport, which is attainable in nanowires, could potentially be a requirement for sub-60 mV/dec operation [14]. Nanowire tunnel devices based on the GaSb/InAsSb heterojunction will be described in detail in Chapter 5.

1.3 Aim of thesis

This thesis deals with the epitaxial growth, characterization and application of antimony-based nanowires. The first aim has been to investigate the mechanism behind the formation of antimonide nanowires by metal-organic vapour phase epitaxy (MOVPE) and to connect these findings to the knowledge from planar antimonide epitaxy and nanowire growth in general. Chapter 3 thus serves as an overview of the research field of antimonide epitaxy, followed by Chapter 4 in which nanowire growth in general and growth of antimonide nanowires in particular are discussed.

The second aim of the thesis has been to develop GaSb/InAsSb heterostructure nanowires, a heterostructure with an unusual broken band line-up which is attractive for steep-slope transistor devices operating at low supply voltage. In Chapter 5 the epitaxial growth of the heterostructure nanowires is described, as well as theoretical modeling of the electrical properties and electrical characterization of complete tunnel diode devices. Finally, some preliminary modeling and experimental results on full transistor devices is presented together with a discussion of the prospects of GaSb/InAsSb TFET.

Chapter 2

Semiconductor Crystals

In crystallic semiconductors, the atoms are ordered in a periodic manner with an interatomic distance specific for each material. A crystal is translationally invariant, meaning that you can describe the entire crystal by a so-called unit cell. The unit cell is the smallest piece of the crystal with which one can build the full crystal merely by translating it along the crystallographic axes. In this chapter the various aspects of semiconductor crystals is described. In Section 2.1 the common crystal structures of semiconductors are discussed. Section 2.2 describes electronic band structure and the physical origin of the electron effective mass. In Section 2.3, metalorganic vapour phase epitaxy, the method used in this thesis for realizating epitaxial crystals is described, and finally in Section 2.4 the two most important methods of characterizing crystals are described; electron microscopy and x-ray diffraction.

2.1 Crystal structure of Semiconductors

Most common semiconductors crystallize in similar crystal structures. Si and Ge exhibit the diamond crystal structure, while the III-Vs typically have the zinc-blende (ZB) crystal structures. The nitrides (GaN, AlN, and InN) are exceptions and typically form the wurtzite (WZ) crystal structure, which is also an important crystal structure in nanowires (See Section 4.1.1). The diamond and ZB structures have cubic symmetry, while WZ has hexagonal symmetry. In all these structures the atoms bind to each other with four hybridized sp^3 electron orbitals. sp^3 orbitals form very strong and directional covalent bonds arranged into the corners of a tetrahedron (Figure 2.1a). In the III-V materials, the extra electron in the group-V atom transfers to the group-III atom to form the sp^3 orbitals, thus making

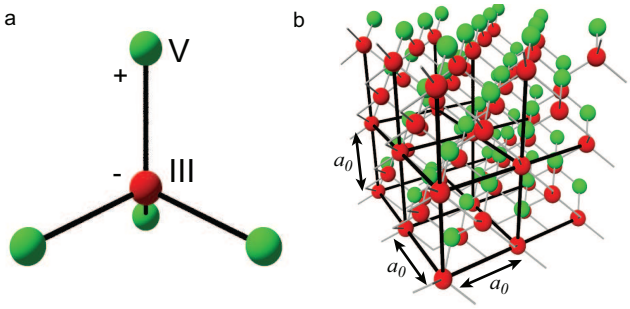

Figure 2.1: *(a) Tetrahedal bonds of a III-V semiconductor indicating that the bonds are slightly ionic due to the different number of valence electrons between the group-III and group-V atoms. (b) A ZB crystal built up from cubic unit cells with a lattice parameter* a_0.

the bonds slightly ionic.

The unit cell of both the diamond and ZB crystal structures is the same and is cubic with a side length a_0, called the lattice parameter. The diamond unit cell can be described as one face-centered cubic (fcc) unit cell interlayed with another translated by $a_0/4$ along all three axes. The two fcc sub-lattices contain different species of atoms in the ZB structure. In the case of GaSb one sub-lattice consists of Ga atoms and the other Sb atoms. Different semiconductors have different atomic bond strengths and consequently obtain different lattice parameters, even though the crystal structure can be the same.

If two kinds of crystals are combined they form a so-called heterojunction. High-quality heterojunctions are of great importance for electronic applications, but are often not trivial to realize due to a difference in lattice parameters. When combined, the unit cells at the interface are either compressed or stretched to fit to each other. The effect of laterally compressing a unit cell is visualized in Figure 2.2a. It is observed that an elongation occurs in the axial direction, $a_{||}$, as the lateral dimensions are compressed. The strain in a crystal lattice can be defined as the relative change in unit cell width:

$$\epsilon = \frac{a_0 - a}{a_0} \tag{2.1}$$

where a is the width of the strained unit cell. The tension that is built up as the unit cell dimensions is modified away from its equilibrium size is called strain energy. The strain energy in a uniaxially strained thin film increases linearly with the film thickness, and at some point it will become

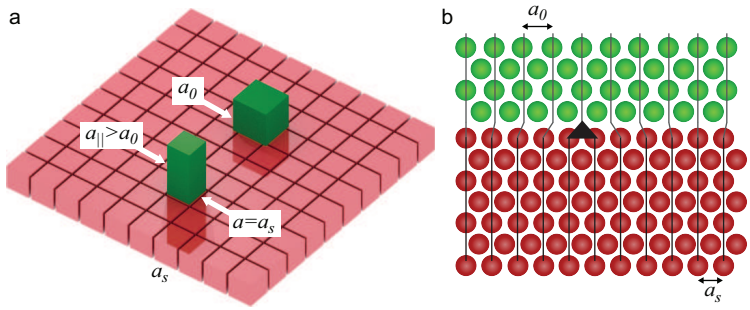

Figure 2.2: *(a) Schematic image of unit cell deformation due to compressive strain, showing that a lateral compression gives rise to an axial elongation. (b) Atomic distribution of a relaxed heterojunction which includes a single misfit dislocation (indicated by triangle) since an atomic row is missing in the top epitaxial layer. The vertical lines are included as guides for the eye.*

too high and is released. This process is called relaxation and can occur via the formation of misfit dislocations or, if possible, by a lateral expansion of the crystal lattice. Misfit dislocations are an abrupt change in the periodic lattice of a crystal (Figure 2.2b). For electric transport a dislocation act as a scattering center, reflecting the electron wave and reducing the conductivity of the material. Dislocations are thus detrimental for electronic devices and the most critical challenge of heterostructure electronics is to avoid the formation of dislocations and retain a high crystal quality.

2.2 Physics of Semiconductors

The fundament to understanding how current is transmitted through a crystal lies in understanding what energies electrons can carry in such an environment. This can be formulated into the electronic band structure, which simply put expresses which energy an electron has if it is travelling in a certain direction with a certain momentum, $\mathbf{k} = (k_x, k_y, k_z)$. In the simple case of a free electron plane wave $\Psi(\mathbf{r}) = e^{i\mathbf{k}\cdot\mathbf{r}}$ travelling through vacuum this energy is given by the usual expression for the kinetic energy with the electron velocity expressed as $\hbar\mathbf{k}/m_0$,

$$E_{free}(\mathbf{k}) = \frac{m_0 v^2}{2} = \frac{\hbar^2 \mathbf{k}^2}{2m_0}. \tag{2.2}$$

An electron travelling through a crystal, however, is not free but is travelling through a periodical attractive potential created by the Coulomb forces of

the atomic nuclei (Figure 2.3a). In a lattice with the volume Ω and period $\mathbf{R}$ the electron wave function can be expressed as a Bloch function

$$\Psi_n(\mathbf{r}) = e^{i\mathbf{k}\cdot\mathbf{r}} u_n(\mathbf{k}, \mathbf{r}), \tag{2.3}$$

where $u_n(\mathbf{k}, \mathbf{r})$ is a periodic function such that $u_n(\mathbf{k}, \mathbf{r}) = u_n(\mathbf{k}, \mathbf{r} + \mathbf{R})$. A common form of this function is

$$u_n(\mathbf{k}, \mathbf{r}) = \frac{1}{\Omega} e^{i\mathbf{G_n}\cdot\mathbf{r}}, \tag{2.4}$$

where $\mathbf{G_n}$ is a reciprocal lattice vector such that $\mathbf{G_n} \cdot \mathbf{R} = 2n\pi$, with n being an integer. In one dimension $\mathbf{R} = a_0$, so that $\mathbf{G_n} = \frac{2\pi}{a_0} n$. The total Bloch wave function is thus given by

$$\Psi_n(\mathbf{r}) = \frac{1}{\Omega} e^{i[\mathbf{k}+\mathbf{G_n}]\cdot\mathbf{r}} = \frac{1}{\Omega} e^{i\mathbf{K}\cdot\mathbf{r}}, \tag{2.5}$$

which means that one can view the wave function as a plane wave with a crystal momentum $\mathbf{K}$. This is called the nearly-free electron model. The energy dispersion in this model is then given by

$$E_{nearly}(\mathbf{k}) = \frac{\hbar^2 \mathbf{K}^2}{2m_0} = \frac{\hbar^2 (\mathbf{k} + \mathbf{G_n})^2}{2m_0}, \tag{2.6}$$

which in one dimension becomes $E(k) = \frac{\hbar^2 (k + \frac{2\pi}{a_0} n)^2}{2m_0}$. This means that for each $\mathbf{G_n}$ vector there is a parabolic energy dispersion in k, corresponding to Eq. 2.2. The region of $\mathbf{k}$ vectors such that $|\mathbf{k}| < \mathbf{G_n}/2$ is called the 1st Brillouin zone, and one can always translate a $\mathbf{K}$ vector back into the 1st Brillouin zone by choosing an appropriate $\mathbf{G_n}$ vector. By doing this one "folds" the parabolic E-$\mathbf{k}$ dispersions of higher order Brillouin zones into the 1st Brillouin zone. The same $\mathbf{k}$ vector then corresponds to multiple energies (Figure 2.3b). It is important to remember, however, that these energies belong to different Brillouin zones, i.e. their $\mathbf{K}$ vectors are different. One can also say that they belong to different energy bands. Due to the crossing of bands some states would be degenerate. This degeneracy is lifted due to interaction from the periodic crystal potential, $V(x)$. Physically one can view this as the formation of standing waves at certain $\mathbf{k}$ vectors due to reflection of the wave function against the crystal lattice. The different bands are thus separated from each other by band gaps, which magnitudes, E_g, are determined by the strength of the crystal potential [15, 16].

The electron band structure of a semiconductor is completely filled with valence electrons up to one of these band gaps. The highest occupied bands

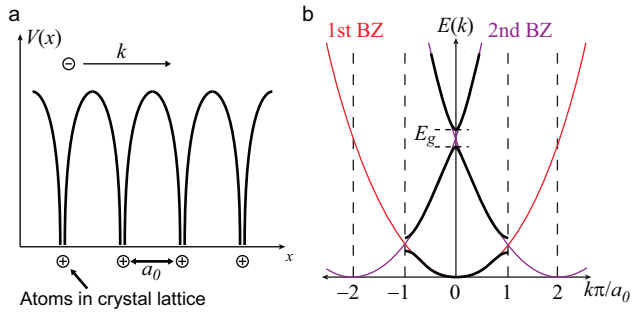

Figure 2.3: *(a) An electron travelling in a periodic potential landscape caused by the attractive forces of the atoms in the crystal lattice. (b) The orgin of the band structure (black line) from the free electron energy dispersions of the 1st and 2nd Brillouin zones (red and purple lines). Band gaps arise at degenerate states due to interaction with the crystal potential.*

are denoted the valence bands. Because these bands are completely occupied their electrons cannot carry any current. The lowest empty band above the band gap is called the conduction band. Electrons which are transferred from the valence band to the conduction band can respond to an applied electric field by changing their momentum, and can thus carry current. The highest valence bands and the conduction band are thus the most important bands for electronic transport in semiconductors.

2.2.1 The effective mass approximation

To get an expression for the dispersion of the energy bands in a semiconductor crystal, $\mathbf{k}\cdot\mathbf{p}$ theory can be utilized. Inserting the Bloch wave functions of Eq. 2.3 into the Schrödinger equation gives

$$\left[\frac{\mathbf{p}^2}{2m_0} + V(\mathbf{r}) + \frac{\hbar}{m_0}\mathbf{k}\cdot\mathbf{p} + \frac{\hbar^2 k^2}{2m_0}\right] u_n(\mathbf{k},\mathbf{r}) = E_n(\mathbf{k}) u_n(\mathbf{k},\mathbf{r}), \tag{2.7}$$

where $\mathbf{p}$ is the momentum operator $\mathbf{p} = -i\hbar\nabla$. Now suppose that the solution to Eq. 2.7 for $\mathbf{k} = \mathbf{0}$ is known. The eigenstates $u_n(\mathbf{0},\mathbf{r})$ form a complete basis in which one can expand the solutions for other $\mathbf{k}$'s. The last two terms on the left hand side of Eq. 2.7 can be treated as a perturbation to the known solution, and second order perturbation theory can be used to obtain the energy dispersion:

$$E_n(\mathbf{k}) \approx E_n(\mathbf{0}) + \frac{\hbar^2 k^2}{2m_0} + \frac{\hbar^2}{m_o^2}\sum_{m,m\neq n} \frac{|\langle m\mathbf{0}|\mathbf{k}\cdot\mathbf{p}|n\mathbf{0}\rangle|^2}{E_n(\mathbf{0}) - E_m(\mathbf{0})}. \tag{2.8}$$

By applying symmetry arguments, one can realize that many of the matrix elements in Eq. 2.8 vanish [15]. For the conduction band, one then obtains an energy dispersion given by

$$E_c(\mathbf{k}) \approx E_c + \frac{\hbar^2 k^2}{2m_0} + \frac{\hbar^2}{m_0^2}\frac{|k(im_0/\hbar)P|^2}{E_c - E_v} = E_c + \frac{\hbar^2 k^2}{2m_0 m_{eff}} \tag{2.9}$$

where $1/m_{eff} \equiv 1 + E_p/E_g$, is the inverse of the effective electron mass and $E_p = 2m_0P^2/\hbar^2$. P is a material dependent matrix element equal to $2\pi\hbar/a_0$. Eq. 2.9 means that the energy dispersion in the conduction band is exactly the same as for a free electron, but with a reduced mass, denoted the electron effective mass. A similar treatment can be done for the valence bands to obtain three distinct hole effective masses. Because of the perturbation treatment, the effective mass approximation is only valid for small $\mathbf{k}$. For larger $\mathbf{k}$'s the bands are no longer parabolic and a more rigorous treatment, such as the Kane model, is required [17].

2.2.2 Charge distribution in semiconductors

Because of the band gap between the valence bands and the conduction band, semiconductors normally have very few free charge carriers compared to metals. Due to thermal fluctuations there are always some electrons, however, which obtain enough energy to transfer to the conduction band. The thermal equilibrium distribution of electrons is described by the Fermi distribution:

$$f(E, E_f) = \left(1 + e^{(E-E_f)/k_BT}\right)^{-1} \tag{2.10}$$

where E_F is called the Fermi energy or Fermi level and k_B is Boltzmann's constant. At low temperature one may approximate the Fermi distribution as being equal to one below the Fermi level and zero for energies above it. For a semiconductor, which have most electrons in the valence band, the Fermi level is thus close to the middle of the band gap. To make it useful for electronic applications one can extrinsically dope the semiconductor. In this process a small fraction of atoms in the crystal lattice are replaced by atoms with fewer (acceptor) or more (donor) valence electrons. In practice, these impurities are either added during the crystal growth itself or by ion implantation during the device processing. The electron states introduced by the dopant atoms lie inside the band gap, either close to the valence band edge (acceptors) or close to the conduction band edge (donors). These atoms are thus easily ionized either by donating an electron to the conduction band or accepting an electron from the valence band, resulting

in either a free electron in the conduction band or a positively charged hole in the valence band.[1] Such semiconductors are labeled n-type and p-type, respectively. The purpose of doping is to control the type and number of free charge carriers in the material, and this causes the Fermi level to move closer to the appropriate band gap edge. The number of free electrons in the conduction band of an n-type semiconductor is obtained by summing over the DOS in the conduction band, multiplied with the Fermi distribution

$$n = \int_{E_c}^{\infty} \mathrm{DOS}(E) f(E, E_f) dE \tag{2.11}$$

One can sometimes approximate $f(E, E_f)$ as $f_B(E, E_f) = e^{-(E-E_f)/k_B T}$. This is called the Boltzmann approximation and is only valid when $E_c \gg E_f$ so that only the tail of the Fermi distribution has to be accounted for. It is thus not valid for degenerately doped semiconductors for which $E_f > E_c$ [18].

2.3 Metalorganic vapour phase epitaxy

There are many techniques by which crystals can be grown. Large single crystals can be pulled from melts or thin crystallic films can be deposited on crystalline substrates in a process called epitaxy. The chemical precursors can be crystallic powder, beams of single atoms or even complex molecules, and the growth can be performed at pressures ranging from ultra-high vacuum to hundreds of atmospheres. The technique used in this thesis is metalorganic vapour phase epitaxy (MOVPE) and is a technique which is, for instance, used commercially in manufacturing lasers and light emitting diodes. The principle behind the technique is best described in the form of an example following Figure 2.4. Assume that one wants to grow an epitaxial thin film of the III-V semiconductor GaSb on a substrate of the same material. One then uses two types of metalorganic precursors to supply Ga and Sb; for example triethylgallium (TEGa) and trimethylantimony (TMSb). These precursors are liquids at room temperature and are stored in metal bottles, called bubblers, which are kept in temperature-controlled baths. In the most common bubbler design, two pipes enter the bubbler from the top, the inlet pipe continues to the bottom while the outlet ends just at the top of the bubbler.

[1] A hole can be treated as a particle, similar to the electron, but with a positive charge. It's effective mass, like that of the electron, is determined by the second derivative $\left(\frac{\partial^2 E}{\partial k^2}\right)$

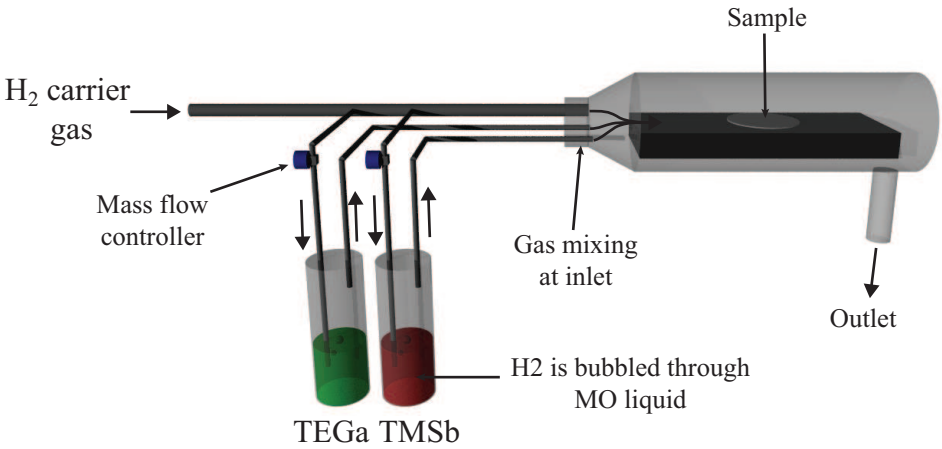

Figure 2.4: *Schematic illustration of a MOVPE reactor for GaSb growth. H_2 gas is bubbled through containers of growth precursors, which are then transported into the heated growth chamber where the sample is located and the epitaxial growth occurs.*

To extract the precursor from the bubbler, H_2 gas is led through the inlet and bubbles through the liquid and exit the bubbler through the outlet pipe. The H_2 gas carries with it a specific amount of metal-organic chemical. The molar flow of extracted metalorganic chemical is determined from the temperature and pressure in the bubbler using the following expression:

$$\Phi_M^{MO}[mmol/min] = 0.0446 \frac{p_v^{MO}(T)}{p_{bubbler} - p_v^{MO}(T)} \Phi_V^{H_2}[cm^3/min] \qquad (2.12)$$

where $\Phi_V^{H_2}$ is the volume flow of H_2 led through the bubbler, $p_{bubbler}$ is the total bubbler pressure and p_v^{MO} is vapour pressure of the metal-organic chemical. p_v^{MO} is most often approximated by

$$log_{10}(p_v^{MO}) = A + B/T \qquad (2.13)$$

where A and B are table values specific for each chemical. The pipes leading from the bubbler transport the H_2 gas containing the metalorganic chemicals into a tube made of quartz glass, called the reactor, in which the substrate crystal is located on a holder called the susceptor. The susceptor is heated to a temperature suitable for crystal growth. When the precursors enter the hot reactor the fragile bonds between the metal atom (Ga or Sb)

of the band in which it is located.

and alkyl groups are broken and the metals are adsorbed on the surface of the susceptor and substrate[2]. Here the adatoms diffuse around, driven by heat, until they either desorb again or are incorporated into the growing crystal via chemical reactions.

2.3.1 Chemistry of MOVPE

Chemical reactions are driven by the thermodynamical force to minimize the Gibbs' free energy (G) of a system. The chemical potential, μ_i, for a component i of a solution or reaction is defined as

$$\mu_i = \left(\frac{\partial G}{\partial n_i}\right)_{T,P,n_j} \tag{2.14}$$

In a reaction A $\leftrightarrow$ B the number of particles in each state, n_A and n_B, changes. At thermal equilibrium, G is at a minimum, which implies that an infinitesimal change in either n_A or n_B will not change G, i.e. the chemical potential of each phase is the same ($\mu_A = \mu_B$). In non-equilibrium, the reaction will go in the direction from high to low chemical potential, with the driving force to restore equilibrium being $\Delta\mu_{A\to B} = \mu_A - \mu_B$. Thus, if B is the vapour phase and A is the solid phase of the substrate a supersaturation ($\Delta\mu$) of particles in the vapour phase will drive a phase transition from the vapour phase into the solid phase. These transition events occur on the surface of the crystal, resulting in epitaxial growth of a new crystal on top.

In practice, the kinetics of surface reactions and diffusion in the reactor are not fast enough to establish thermal equilibrium throughout the whole reactor. There will thus be a $\Delta\mu$ gradient throughout the reactor and two different regimes of epitaxial growth are possible; kinetics-limited growth and diffusion-limited growth [19].

The first type of growth occurs when the chemical reactions at the growth interface are slow. Then there is always sufficient transport of reaction material to the growth interface and the crystal growth rate is determined by the reaction rates at the growth interface. The chemical reaction rate, R, can be reduced to a temperature-dependent exponential function,

$$R = Ae^{-E_a/k_BT} \tag{2.15}$$

This type of equation is called an Arrhenius function, and here A is a constant and E_a is the activation energy for the chemical reaction. Often, epitaxial growth consists of a long chain of reactions. It is then the reaction

[2]The precursors are not necessarily completely decomposed before adsorbing on the surface, so surface reactions are often very important for the growth process.

with the highest activation energy (i.e. the slowest reaction) which determines the overall growth rate. Because of the direct relation between the reaction rate and the epitaxial growth rate, the temperature dependence of the growth rate follows Eq. 2.15 and is exponential. It is thus possible to obtain useful information about the growth chemistry from growth rate data. However, controlled epixatial growth in the kinetics-limited regime is problematic because a small variation of the temperature gives a large variation in the growth rate.

In contrast, if the chemical reaction kinetics are much faster than the diffusion kinetics then the growth interface will almost be at thermal equilibrium even though the supersaturation can be high at the inlet to the growth chamber. The rate of epitaxial growth is then decided by the rate at which new growth material is supplied; this is called diffusion limited growth. In this regime, the temperature dependence is much weaker compared to the kinetics-limited regime, making the growth rate easier to control [19].

Even though MOVPE is a quite straight-forward technique, in practice there are many factors which determine how the result of the crystal growth will be. Important parameters include the temperature in the reactor, which governs the decomposition efficiency of the precursors and the diffusion length of adatoms before they incorporation. Also important are the absolute and relative concentrations of the precursors, the pressure in the reactor, as well as the gas flow speed. These parameters, among others, will ultimately determine the quality of the grown crystal, and controlling them is thus vital.

2.4 Characterization Methods

2.4.1 Electron microscopy

For characterization of nanostructured crystals optical microscopy does not supply sufficiently high resolution. The reason for this is that nanostructures per definition have dimensions below the wavelength of visible light (300-800nm). To be able to image nanostructures with high detail one instead can use electron microscopes. The principle of an electron microscope is similar to an optical microscope, the difference being that the photons are replaced by electrons. The de Broglie wavelength of an electron is

$$\lambda_{el} = \frac{h}{p}, \tag{2.16}$$

where h is the Planck constant and p is the momentum of the electron. The wavelength of the electron is thus inversely proportional to its velocity,

and therefore very small wavelengths can be obtained. For example, with a kinetic energy of 100 eV the electron wavelength is only 0.12 nm, which is roughly the same as the size of an atom. Monochromatic electrons can be generated using a field emission source, where a high voltage is applied to a very sharp metal tip. At the end of the metal tip, the electric field is high enough so that electrons can tunnel out of the metal. These electrons are accelerated in a electric field to kinetic energies normally between a few to hundreds of keV and the beam is focused using electrostatic lenses, allowing the microscopist to image features with sizes much smaller than what is possible to see with optical microscopes. The resolution of electron microscopes is not limited by the wavelength of the electrons, but by the non-ideality of the electron lenses. This can be somewhat compensated for by using a higher electron energy, which is why 100-300kV microscopes are quite common .

A very useful by-product of using electrons to obtain microscope images, is that some electrons can interact with the atoms in the studied material, resulting in the emission of x-rays. Apart from the continous bremsstrahlung x-rays generated as an electron pass by close to an atom and is slowed down, an electron can collide with and ionize the atom. As electrons from the outer shells fall down into the empty position, x-rays are emitted with a wavelength that is characteristic for each atomic species. By detecting the energy of these x-rays one may quantitatively measure the atomic composition of the studied material. This technique is called x-ray electron dispersive spectroscopy (XEDS) and is used extensively throughout this thesis to obtain compositional maps of nanowires and their seed particles.

The two common types of electron microscopy methods are scanning electron microscopy (SEM) and transmission electron microscopy (TEM). In a SEM you scan a focused electron beam over the sample, and measure the amount of secondary generated or back-scattered electrons. SEM is a faster and cheaper technique compared to TEM, and also resembles an optical microscope in the type of images one obtains.

TEM on the other hand is a much more powerful and complex technique. In TEM one measures the transmitted electron beam, and from it reconstructs an image of the sample. With high-resolution TEM (HRTEM) it is possible to resolve the individual atomic rows of a crystal. This technique relies on the fact that electrons are diffracted by the atomic lattice of a crystal. The diffraction pattern is inversely Fourier-transformed by the imaging lens and a high resolution image is formed in the image plane. One can also capture the diffraction pattern directly by putting the detec-

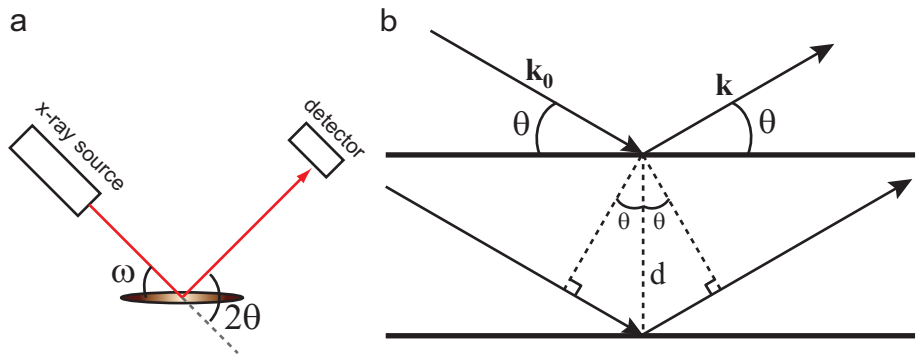

Figure 2.5: *(a) A simplified schematic of an HRXRD setup. (b) X-rays reflected off two consecutive crystal planes with incidence and exit angles θ relative to the planes. Note that $\omega = \theta$ is only true if the normal of the diffraction planes is parallel to the sample normal. This is generally not the case.*

tor in the diffraction plane. One can also operate a TEM in scanning mode (STEM), thus focusing and scanning the electron beam as in a SEM. STEM mode is often used in conjunction with XEDS to obtain spatial maps of the chemical composition of the samples [20].

2.4.2 X-ray diffraction

One of the most important techniques for characterizing crystals is high-resolution x-ray diffraction (HRXRD). In HRXRD one irradiates a crystal with x-rays at a specific angle of incidence relative to the plane of the sample, ω, and then detects the reflected x-rays at an angle 2θ (see Figure 2.5a).

Reflection of light can be explained by an interaction of light with the the electron cloud around the atom, forcing the electron cloud to oscillate and radiate with the same wavelength as the incoming light. This type of scattering is called elastic scattering. A crystal is essentially a periodic array of atoms, which all will interact with the incoming light beam in this manner.

An X-ray beam can be approximated as a plane wave $Ae^{i\mathbf{k_0}\mathbf{r}}$, where A is the amplitude of the wave and $\mathbf{k_0}$ is the wave vector of the light defined with a length of $1/\lambda$. Assuming that there is no inelastic scattering, the wave vector $\mathbf{k}$, of the x-rays after scattering will have the same magnitude as before, namely $|\mathbf{k}| = |\mathbf{k_0}| = 1/\lambda$.

Because of the wave nature of x-rays, the waves reflected off an atomic

plane will interfere and cancel out in most directions. Only for a reflection angle equal to the incidence angle to the plane, θ, will the interference be constructive and the intensity be amplified. Consider the situation depicted in Figure 2.5 where a beam of light is incident on a set of crystal planes with a certain angle of incidence, θ. Light reflected at various positions in the same plane will be in phase even after the reflection, much like light reflected off a mirror. Light reflected by two consequtive parallel planes, however, will have traveled different distances. The additional distance traveled by a beam reflected in a second plane is $2d\sin\theta$, obtained by simple geometry (Figure 2.5). The two reflected beams will interfere with each other, constructively only when the path difference equals integer numbers, n, of λ. This is the Bragg refraction condition and is expressed as:

$$n\lambda = 2d\sin\theta \tag{2.17}$$

The significance of the Bragg condition is that each lattice-spacing in a crystal will give rise to one set of diffraction peaks at specific angles. By measuring these angles one can measure lattice plane spacings of a crystal with very high precision and thus calculate the material composition and strain. Many other parameters also are measurable with HRXRD, for example, mosaicity, porosity, epilayer tilt, crystal symmetry, roughness and layer thickness [21]. HRXRD was used in Paper V to simultaneously measure the composition of InAsSb nanowires and an InAsSb surface layer.

Chapter 3

Antimonide planar epitaxy

Antimonides are III-V semiconductor materials consisting of group-III atoms in combination with the group-V atom Sb. The binary antimonides consist of AlSb, GaSb and InSb. In this chapter, the epitaxial growth of antimonide thin films is reviewed. In Section 3.1 the general properties of the antimonides and promising application areas are described. The challenges that distinguish epitaxial growth of antimonides from other III-V semiconductors are discussed in Section 3.2.

3.1 Properties of Antimonide Semiconductors

The antimonide family of semiconductors are extreme in many ways. They hold the record among the III-Vs when it comes to the most narrow band gap, highest carrier mobilities and lowest charge carrier effective masses. In Figure 3.1 the band gap of Si, Ge and common III-V materials are compared with respect to their lattice parameter. The antimonides stand out in this plot as being the materials with both largest lattice parameters and most narrow band gaps. InSb is the most extreme example, having a band gap of 170 meV and a lattice parameter of 6.479 Å, 19% larger than that of Si.

GaSb, InAs and AlSb form an almost lattice-matched family close to a lattice parameter of 6.1 Å, often denoted the 6.1 Å family [22]. The similar lattice parameter makes it relatively easy to realize heterostructures of these materials in various combinations, without introducing misfit dislocations. This makes the 6.1 Å family very attractive from an applications point of view.

InSb and the ternary alloy InAsSb both have a very small electron effective mass. Consequently, quantum confinement effects appear in much larger structures than in other materials. If one defines a confined system

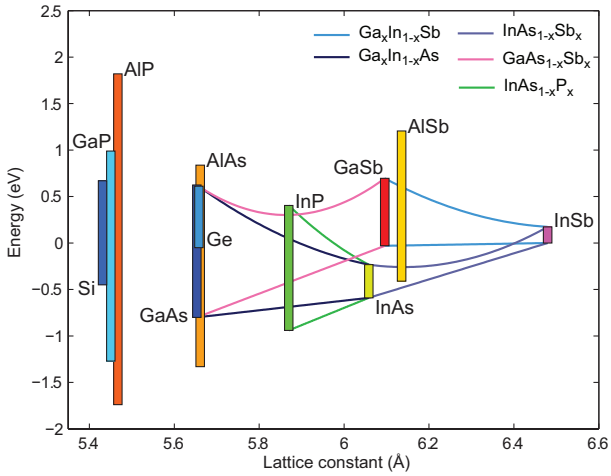

Figure 3.1: *Band gaps and band alignment of the group IV and selected III-V binary and ternary semiconductors plotted as function of the cubic lattice parameter. The lines correspond to the valence band and conduction band positions for ternary alloys over their whole composition range (Data from Ref. [23]).*

as one with a width for which the energy separation between the ground state and the first exited energy level is the same size as kT, then for InSb ($m_e = 0.015m_0$) and $InAs_{0.37}Sb_{0.63}$ ($m_e = 0.010$) this happens for structures as large as 54 nm and 65 nm, respectively (Figure 3.2a). These dimensions are readily obtainable in nanowire growth, making InSb and InAsSb highly interesting for fundamental studies of quantum transport [24].

3.1.1 Optical Applications

InAsSb has a minimum band gap of only 84 meV (14.7 µm) for $InAs_{0.37}Sb_{0.63}$ (Figure 3.2b). Optoelectronic devices of InAsSb can thus be useful for optical applications in the long-wavelength infrared (LWIR) range. For instance, an InAsSb photodetector could be used to detect the presence of environmentally important gases such as CO_2, CO, CH_4 N_2O and O_3, which all have absorption bands in the range between 8 µm and 12 µm [25]. Another application area which is of military interest is thermal imaging [26]. The conventional material choice for LWIR photodetectors is HgCdTe. However, one drawback of HgCdTe is that it is very soft and has a low thermal conductivity, which requires that detectors are actively cooled when in operation. Additionally, discarded HgCdTe chips can be very harmful for the

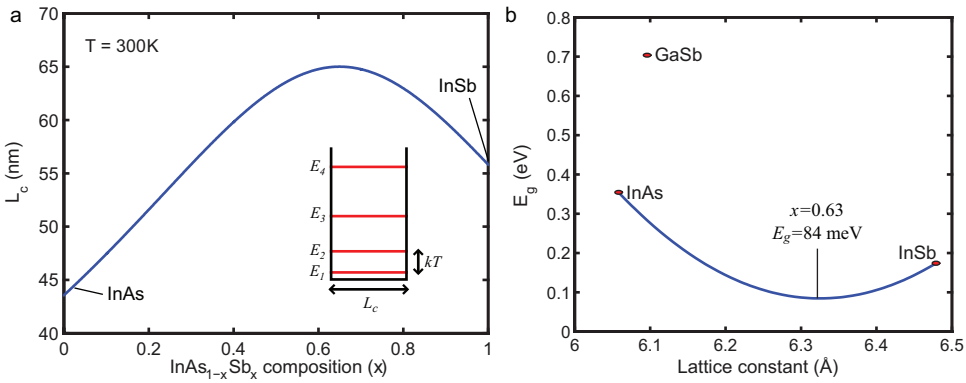

Figure 3.2: *(a) Critical length in $InAs_{1-x}Sb_x$ below which there is quantum confinement at room temperature, as a function of composition. (b) Band gap of InAsSb, GaSb, InAs and InSb as function of the lattice parameter.*

environment. InAsSb is harder and conduct heat better, as well as being less harmful to the environment.

GaSb and InAsSb in heterostructures with InAs is also widely studied because of the unique band alignment, where the conduction band edge of InAs lies below the valence band edge of both GaSb and InAsSb ($x > 0.6$). This type of band alignment is called a broken type-II alignment[1]. By growing such broken type-II superlattices (SL's), one can obtain very narrow effective band gaps within the superlattice. The application of these structures is in long-wavelength infrared (LWIR) or terahertz photo-detectors. By tailoring the widths of the SL layers the energy gap can be controlled to match the appropriate wavelength. Complex p-i-n photodetectors with different effective band gaps in the p, i, and n-regions have been realized in the GaSb/InAs system, with excellent detectivity and responsivity [26]. The single GaSb/InAs heterojunction is discussed in more detail in Chapter 5, in terms of GaSb/InAs(Sb) nanowire tunnel devices.

3.1.2 Electrical Applications

The antimonides are also very interesting because of their electrical properties. The interest is mainly due to the extremely high electron mobility of InSb which can be as high as 77 000 cm^2/Vs at room temperature and reach several hundred thousands at 77 K. Intel and the British-based company QinetiQ has had major success in the last decade with the development

[1]Sometimes it is denoted a type-III alignment to highlight its very different properties compared to the ordinary type-II alignment.

of a high electron mobility transistor (HEMT) based on an InSb quantum well structure. To date, the best reported high-frequency performance is for an 85-nm gate length HEMT with unity gain cut-off frequency, f_t, as high as 305 GHz [27]. These devices have recently also been integrated on a Si platform with maintained performance [28].

The electron mobility of GaSb is also reasonably high (3750 cm^2/Vs) in comparison to Si, but GaSb is typically considered to be more attractive for p-type devices, because of its high hole mobility of almost 1000 cm^2/Vs, which is rivaled only by Ge (1900 cm^2/Vs). The mobility of GaSb can be further improved by straining the material [5]. There are several examples of type-II double heterojunction bipolar transistors (DHBTs) using InP-based emitter and collector layers and a p-type GaAsSb base layer. The benefit of such structures is the type-II band alignment which results in hot carrier injection into the collector and large breakdown voltages. The best device performance reported thus far is an AlInP/GaAsSb/InP DHBT with f_t = 455 GHz and maximum oscillation frequency f_{max}= 400 GHz. A similar device structure with $f_t \approx$ 200 GHz is now produced on 3" wafers for Agilent's commercial high speed measurement instruments [29].

3.2 Epitaxial Growth of Antimonides

Antimonides are typically more difficult to grow with standard epiaxy techniques than the arsenides and phosphides. There are several reasons for this, including the lack of suitable substrates and a tendency for the materials to obtain native and impurity related defects. Here, the major concerns one faces when growing antimonides are reviewed. More comprehensive reviews can be found in Refs. [30, 31, 32].

3.2.1 Precursors and Impurity incorporation

Traditionally in MOVPE of III-V semiconductors one uses a metalorganic precursor for supplying the group-III atoms and a hydride precursor (AsH_3 or PH_3) for supplying group-V atoms. The common metalorganic molecules (TMGa, TEGa, TMIn, TEIn) most often do not decompose completely but result in a metal cation attached to an alkyl-group (methyl- or ethyl-). If not removed, this alkyl-group could result in a high C incorporation in the grown crystal film. Hydride molecules adsorbed to the growth surface can transfer atomic hydrogen to the metal-alkyl molecules and form methane or ethane, which is then flushed away. In the case of GaAs growth from TMGa and AsH_3 the simplified reactions are

$$\begin{aligned} AsH_3(a) &\rightarrow AsH_2^*(a) + H^*(a) \\ Ga(CH_3)_3(a) + H^*(a) &\rightarrow Ga(CH_3)_2(a) + CH_4(g) \end{aligned} \tag{3.1}$$

where (a) refers to an adsorbant and (g) to a gas [33]. This has the beneficial effect of reducing the amount of C incorporated into the crystals [34], and has allowed for high purity 2DEG GaAs/AlGaAs and InP/InGaAs structures to be grown by MOVPE [**?**]. Additionally, a lower C incorporation is often observed in films grown from ethyl-precursors as compared to methyl-precursors [35] presumably due to the larger size of the alkyl group [36]. Unfortunately, the Sb hydride stibine (SbH_3) is very unstable, and cannot be stored or transported reliably. Thus, one instead normally uses a MO precursor for supplying Sb in epitaxial growth. Common Sb precursors are trimethylantimony (TMSb), triethylantimony (TESb) and tris(dimethylamino)antimony (TDMASb). The molecular structures of these precursors are shown in Figure 3.3. Because a hydride Sb precursor can not be used, C incorporation is a major problem in antimonide growth. C impurities significantly reduces the carrier lifetime in semiconductors, and are thus detrimental for both the optical and electrical properties. In addition, C is an amphotheric dopant in III-V semiconductors. The problem of C impurity incorporation is especially severe for InSb which must be grown temperatures below 500 °C where the TMSb decomposition is only partially complete. AlSb growth is also particularily problematic, and extremely high C content is obtained when using TMAl and TMSb as precursors [30, 31]. Similarily to the group-III MO sources, TMSb and TESb can by themselves further increase C incorporation in the grown films. This has led to the development of alternative MO precursors which do not directly bind C to Sb. These have had only limited success due to instability and parasitic reactions, but the most successful alternative Sb precursor is TDMASb, which is used predominately for low-temperature InSb growth [37].

3.2.2 The V/III ratio

When growing arsenide and phosphide thin films the ratio between the group-V and group-III precursors, called the V/III ratio, is normally kept rather high (25-150) to ensure that there is enough supply of the group-V hydrides. This methodology is possible because the vapour pressures of As and P are high enough (15 torr [38] and 2000 torr [39]) to allow excess As and P to evaporate without agglomorating on the growth surface. Sb, however, has a much lower vapour pressure (2×10^{-4} torr at 450 °C [40]) and excess Sb thus sticks to the epitaxial surfaces and may lead to irregular growth. One must thus carefully balance the V/III ratio (equal to one) at

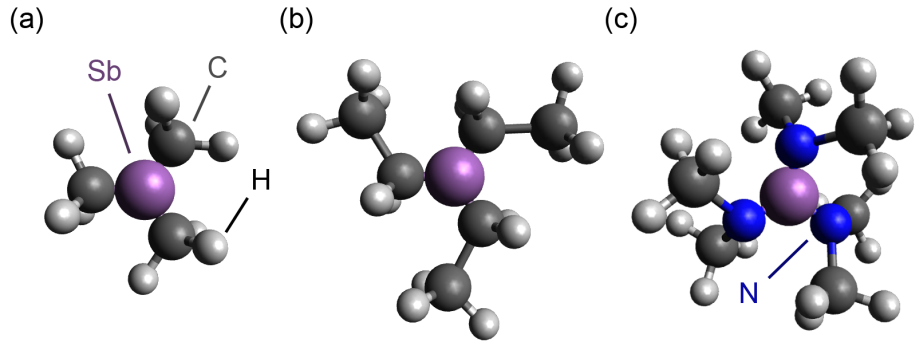

Figure 3.3: *Molecular structures of common Sb MO precursors (a) trimethylantimony, (b) triethylantimony (c) tris(dimethylamino)antimony.*

the growth interface during antimonide growth. Unfortunately, this is often not as simple as setting the same flows of the group-III and Sb precursors. There are several factors that can affect what the effective V/III ratio will be, one important factor being the decomposition of the precursors. For GaSb growth, TMGa and TMSb are expected to both decompose at around 450 °C, but a temperature dependent growth rate has been observed up to 600 °C [41], indicating that complete decomposition may require even higher temperature. Fortunately, since the two precursors decompose similarily the effective V/III ratio is not expected to vary much with temperature, and so a nominal V/III ratio close to 1 can be used. However, alternative precursors such as TEGa, TESb or TDMASb must be employed for applications where a low carbon incorporation is essential. These precursors decompose at very different rates, and parasitic reactions in the vapour phase can further alter the effective V/III ratio from its nominal value.

3.2.3 Miscibility gaps

Antimonides are interesting from a material scientist's point of view because of the occurence of very large miscibility gaps and long-scale ordering in ternaries and quaternary alloys, such as $InP_{1-x}Sb_x$ and $Ga_xIn_{1-x}As_{1-y}Sb_y$ [42]. $InAs_{1-x}Sb_x$ is another example of a ternary material which can be treated as a two-component (InAs and InSb) solid solution. In the following InAsSb is used to demonstrate how thermodynamics can predict the occurence of miscibility gaps.

The change in Gibb's free energy (ΔG_{mix}) when InAs and InSb are mixed can be expressed in terms of the change of enthalpy (ΔH_{mix}) and

entropy (ΔS_{mix}):

$$\Delta G_{mix} = \Delta H_{mix} - T\Delta S_{mix} \tag{3.2}$$

where T is the temperature at which the mixing takes place. A solid solution is typically not an ideal solution[2] due to interaction between the constituents, and the non-ideality of the solution needs to be taken into account. There are many different solution models, the simplest but still useful one being the regular solution model (RSM). Assuming a completely random arrangement of the InAs and InSb components in the solution, the entropy of mixing of $InAs_{1-x}Sb_x$ is the same as in an ideal solution, namely

$$\Delta S_{mix} = -R\left[x\ln x + (1-x)\ln(1-x)\right] \tag{3.3}$$

where R is the ideal gas constant [43, 44]. The enthalpy of mixing on the other hand is not the same as in an ideal solution, but can be expressed atomistically as a summation of bond energies of the nearest-neighbor atoms in the solution. For the case of an alloy where the mixing is only on one sublattice, like $InAs_{1-x}Sb_x$, the two binary phases are treated as if they were single atoms. That is, the possible bond arrangements are InAs-InAs, InAs-InSb and InSb-InSb, resulting in the following bond energies: $\varepsilon_{InAs-InAs}$, $\varepsilon_{InAs-InSb}$ and $\varepsilon_{InSb-InSb}$. The bond energy summation is contained in the so called interaction parameter, Ω_i, giving the following expression for ΔH_{mix}:

$$\begin{gathered}\Delta H_{mix} = x(1-x)\Omega_i \\ \Omega_i = N_0 z\left[\varepsilon_{InAs-InSb} - \tfrac{1}{2}(\varepsilon_{InAs-InAs} + \varepsilon_{InSb-InSb})\right]\end{gathered} \tag{3.4}$$

where N_0 is the total number of "atoms", and z is the number of nearest neighbors surrounding an "atom" [43, 44]. Thus, if the InAs-InSb bond has lower energy than the same-species bonds, then $\Delta H_{mix} < 0$, and if the InAs-InSb bond has higher energy than the same-species bonds then $\Delta H_{mix} > 0$.[3] For ternary systems with a large difference in lattice parameter between the binaries ΔH_{mix} can often have very large positive values. For InAsSb, the interaction parameter has been determined to be 2250 cal/mol [45], and ΔG_{mix} for various InAsSb compositions can be calculated from Eq. 3.2. The result is displayed in Figure 3.4 for temperatures between 400 and 900 K. The significance of this plot is understood by realizing that when InAs and InSb are mixed the system wants to minimize ΔG_{mix}. For high temperatures (>566 K) the ΔG_{mix}-x plot is completely concave, and there

[2]The definition of an ideal solution is that the composition, x_i, is $x_i = p_i/p_{total}$, where p_i is the partial pressure of the species i.

[3]In an ideal solution all the bonds have the same energy and $\Delta H_{mix} = 0$.

is a single composition which minimizes the mixing energy. Below 566 K, however, the curves develop a positive inflexion at mid-range composition. Thus there are now two composition minimas instead. Thus below a critical temperature $T_c = 566$ K there opens up a gap in the miscibility between InAs and InSb, a gap which becomes wider with decreasing temperature. The dashed line in Figure 3.4(b) indicates the temperatures at which ΔG_{mix} becomes concave. This region is called the spinoidal region and solutions with compositions within this region have the extraordinary property of reverse diffusion, so that atoms diffuse towards areas of higher concentration instead of lower. Such a solution will thus separate, and two phases with distinctly different compositions result. This process is called spinoidal decomposition and is a major concern for growth of some ternary III-V alloys, including GaPSb and InPSb, for which the critical temperatures are very high (1996 K and 1319 K, respectively). These materials thus have miscibility gaps spanning almost the whole composition range even at normal growth temperatures (∼500 °C) [46]. The materials are thus very difficult to grow with high compositional homogeneity, and one has to employ techniques operating far from thermal equilibrium, such as MOVPE or molecular beam epitaxy (MBE). Even with such techniques it is difficult to achieve high quality InPSb and GaPSb films, and the materials have thus found only limited use in applications.

3.2.4 Ordering

Ordering is another phenomenon which is observed for essentially all III-V alloys, but in particular for the Sb-containing alloys. In Figure 3.5 a schematic representation of an ordered structure along the ⟨111⟩ direction in GaAsSb is shown. This type of structure is called CuPt ordering, because of it's resemblance to the crystal structure of CuPt. Ordering can occur along various crystallographic directions, and may result in a narrowing band gap and even an anisotropic resistivity [47]. The simple picture presented by the RSM cannot explain the occurence of ordering in systems with positive deviation from ideality ($\Delta H_{mix} > 0$), such as GaAsSb, InPSb and GaPSb. On the contrary, the RSM predicts that an ordered structure is only energetically favorable for systems with negative deviations ($\Delta H_{mix} < 0$). The full answer to why ordering occurs in III-V alloys is still not clear, however it is generally accepted that it is a surface-related phenomenon, driven by strain between the binary constituents in the alloy. Ordering may then minimize the number of bonds between identical "binary

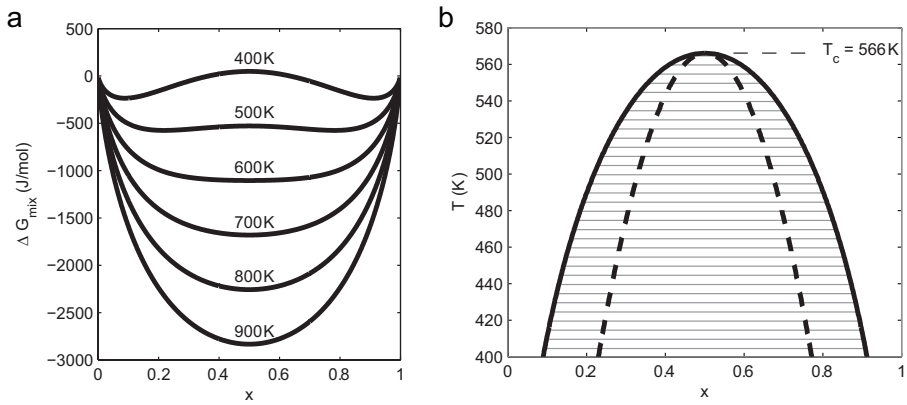

Figure 3.4: *(a) The change in Gibbs free energy when mixing an $InAs_{1-x}Sb_x$ alloy with composition* x*. Note the double minima developing for the lowest temperatures. These points give rise to the solid black line in (b), below which there is a miscibility gap (grey horizontal lines). The dashed lines indicate the spinoidal region in which decomposition into two separate phases is preferential.*

atoms", leading to a total decrease in the strain energy.[4]

Since ordering likely occurs as the crystal is grown it is a surface-related phenomenon which is strongly affected by the reconstruction of the surface. This can be influenced by growth parameters such as temperature, V/III ratio and reactor pressure. Surfactants can also strongly modify the composition of surfaces, and the surfactant Bi has been shown to enhance ordering in GaInP [48]. Sb is also a well known surfactant, and it's effect on crystal growth and ordering is treated in the next section.

3.2.5 Sb Surfactant Effect

Sb atom is a relatively heavy atom (atomic number 51) which covalent bonds are longer than those of Al, Ga, As and P. Therefore it tends to float on top of the growing layer without incorporating [30, 31]. This type of behavior is called a surfactant effect, and can have a strong influence on all surface related processes. To take an example; Stringfellow et al. performed an extensive investigation of the effects of Sb surfactant on the structural ordering of GaInP [49, 50]. They showed that even an extremely low concentration of Sb destroyed the usual CuPt ordering observed in their

[4]For example, many In-Sb-In bonds in one region of an InAsSb alloy would lead to a local high level of strain energy.

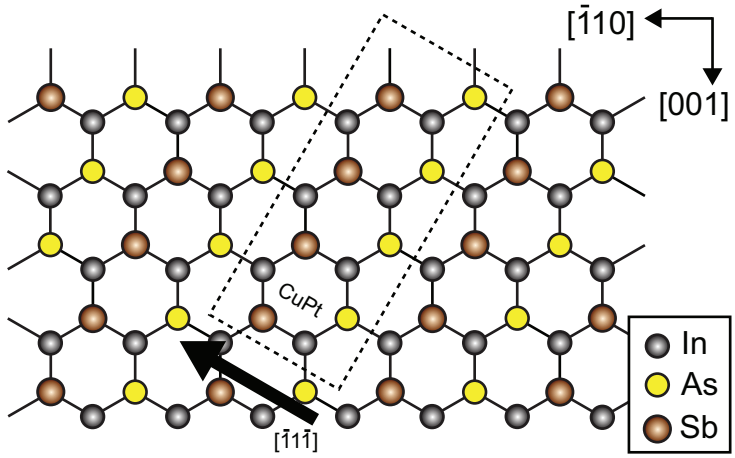

Figure 3.5: *A schematic image of an* $InAs_{0.5}Sb_{0.5}$ *crystal exhibiting CuPt ordering in the* $[\bar{1}1\bar{1}]$ *direction.*

GaInP films, and resulted in a band gap shift of 135 meV. The proposed mechanism is that a high Sb surface coverage results in the loss of $[1\bar{1}0]$ P dimers on the GaInP(001) surface. These dimers are the believed to be the main cause for CuPt ordering in GaInP.

The presence of a Sb surface layer can be a challenge when growing Sb-containing heterostructures, because it often leads to graded interfaces, with a slowly decaying Sb concentration in the subsequently grown layers (Figure 3.6). For example, the InAs-to-InAsSb interface in InAs/InAsSb super-lattice heterostructures is typically atomically abrupt whereas the InAsSb-to-InAs interface is graded at least on a 10-nm scale [51]. The corresponding observation has been made also for InAs/AlSb and InAs/InPSb heterostructures [52].

The desorption of Sb from a surface follows the general exponential form:

$$\theta_{Sb}(t) = \theta_{Sb}(0)e^{-t/\tau} \tag{3.5}$$

where $\theta_{Sb}(t)$ is the surface coverage fraction of Sb at time t, and τ is a decay time constant. The decay time constant is has been measured to be 1.5 min for Sb desorption from GaInP at 620 °C [53]. This means that the Sb surface coverage will still be significant several minutes after the Sb precursor has been turned off. At lower temperature this problem is exacerbated, as τ becomes even larger due to the considerably lower Sb vapour pressure. It is often observed that consecutive growth runs are clearly affected by Sb deposition in earlier runs, and reactor bake-out or

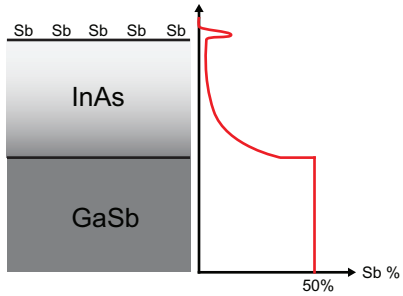

Figure 3.6: *Schematic image illustrating the effect of an Sb surface layer on the Sb concentration gradient into an InAs layer grown on top of GaSb.*

other forms of cleaning procedures are often needed to obtain run-to-run reproducibility.

When growing heterostructures one can decrease the carry-over of Sb into the next epitaxial layer by including growth interrupts after concluding the growth of an Sb-containing material. During such a growth interrupt surfactant Sb is given time to desorb and be purged away. The introduction of TBAs has been shown to promote the desorption of Sb from GaAs(001) surfaces, resulting in a decay time constant of 33 s at 500 °C [54]. Similarily, a purge step including AsH_3 was successfully used to decrease the Sb background concentration in the InAs(Sb) segment of GaSb/InAs(Sb) nanowires in Paper VII.

Chapter 4

Antimonide nanowires

In this chapter, epitaxial growth of Au-seeded antimonide-based nanowires using MOVPE will be described. To be able to understand and appreciate the details specific to antimonide nanowires, the growth of conventional III-V nanowire materials (GaAs, GaP, InAs and InP) is first presented in Section 4.1, serving as a basis to understand antimonide nanowire growth, which is described in the rest of the chapter. The effect of growth parameters is detailed in Section 4.2. Effects on the growth due to the seed particle is described in Section 4.3. The crystal structure and the nucleation mechanism of the nanowires are discussed in Section 4.4 and 4.5, respectively.

4.1 Au-seeded Nanowire Growth

Semiconductor nanowire growth is unlike conventional growth of epitaxial thin films in that it occurs under growth conditions where conventional epitaxy typically fails. This means either that the growth temperature is too low, that the precursor molar fractions are very low, or that the growth substrate is contaminated. While originally being an unwanted side effect in planar epitaxy, nanowire growth has nowadays become a blossoming research field, with new materials and practical applications being realized every year. Nanowires can grow either from metal seeds, be self-seeded or grown by selective area epitaxy. Self-seeded nanowire growth is mostly observed for III-V nanowires, and is realized by initially flowing the group-III precursor (ex. TMGa) to form metallic droplets (Ga), after which growth is commenced by also introducing a group-V precursor (ex. AsH_3) with a V/III ratio held low to keep the particle from being consumed [55]. This thesis, however, focuses on metal-seeded nanowire growth, and more specifically on Au-particle assisted nanowire growth.

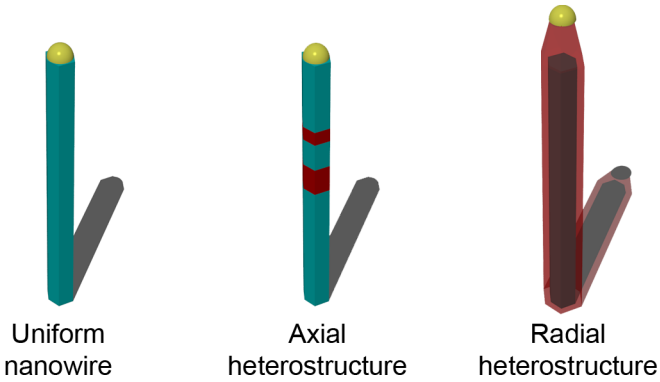

Figure 4.1: *Examples of possible nanowire structures. It is possible to include either axial or radial heterostructures into the nanowire crysal. Because of the small diameters of nanowire, lattice-matching requirements are relaxed.*

Semiconductor nanowires nucleated from Au seed particles are most often grown on a (111)-oriented single crystalline substrate. Au seed particles are deposited on such as substrate, either randomly distributed by nanoparticle deposition from aerosols or colloidal solutions [56], or at specified positions by electron beam lithography [57] or nanoimprint lithography [58]. For III-V nanowires the preferred growth direction is the $[\bar{1}\bar{1}\bar{1}]$ direction, which is often written as [111]B. With an appropriately chosen substrate one thus obtain nanowires standing perpendicular out from the substrate. Due to the small diameter of nanowires ($<$100 nm), it is possible to grow lattice-mismatched heterostructures with maintained crystal quality which would not be possible in epitaxial thin film growth. The heterostructures can be either axial or radial (See Figure 4.1), or a combination of both.

Prior to commencing nanowire growth, the substrate is typically heated in the MOVPE reactor to a high temperature ($>$500 °C) to evaporate the surface oxide, possible contaminants, and in some cases to let the particles alloy with the substrate. After this pre-growth annealing step the temperature is lowered to the nanowire growth temperature, which is typically between 400 and 500 °C. The precursor sources are introduced into the reactor in controlled amounts which initiate the nanowire growth.

At these relatively low temperatures the growth rate of thin film epitaxy is low, and adsorbants can nominally diffuse until they are collected by the deposited particles or desorb. The mechanism behind nanowire growth is still not fully understood, but the original Vapour-Liquid-Solid (VLS) model was proposed already in 1963 by Wagner and Ellis [59]. The VLS

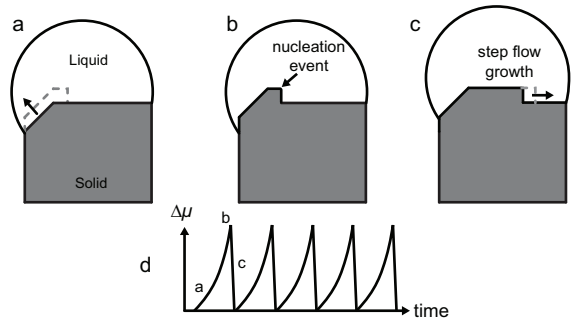

Figure 4.2: *Facet truncation driven nucleation for nanowire growth. (a) Gradual increase in supersaturation ($\Delta\mu$) which is reflected in a decrease in the size of the truncated facet until (b) $\Delta\mu$ is sufficient for nucleation and (c) step flow growth of a new monolayer. (d) Visual representation of the supersaturation in the particle during multiple growth oscillations.*

model proposes that a liquid particle alloy becomes super-saturated with the precursor atoms due to the constant supply of material. The particle will thus release some of the excess material and deposit a solid crystal. The original VLS model does not however give a proper answer to where exactly the nucleation of the solid occurs and can also not explain the polymorphism observed in many nanowire systems (see next section). In recent years several groups have worked to improve the nanowire growth models, most noteworthy are the works of Glas et al. [60], Dubrovskii et al. [61] and Wacaser et al. [62]. In summary, the general opinion to date is that nanowire growth proceeds by step-flow growth underneath the seed particle, which may be either a solid or a liquid. Each monolayer nucleates at the three-phase boundary (TPB) between the vapour, the particle and the substrate crystal [60, 62]. Once the crystal nucleus is formed at the TPB it quickly grows out to completely cover the area beneath the seed particle. Consecutive nucleation-growth cycles then leads to the formation of a nanowire under the particle. The particle is lifted up from the substrate and if the growth is stable it remains on top as the nanowire grows.

Very recent experimental results have further progressed the understanding of the nanowire growth mechanism. Additional tilted facets have been observed at the TPB by *in-situ* TEM. The size and angle of these facets seem to oscillate in time with each addition of a new monolayer to the nanowire top facet [63, 64, 65] (Figure 4.2). These results have the important implication that nucleation does not in fact happen at the TPB, but instead at the intercept between the oscillating facet and the top facet.

The tilted facet is a quickly equalizing facet, which means that its size is directly related to the supersaturation of the growth species in the particle. The truncation at the TPB thus constitutes a visual representation of the supersaturation of the particle, with a small or large truncation corresponding to a high or low supersaturation, respectively. The observed truncation oscillations thus show that before the nucleation of each monolayer the supersaturation is increasing gradually (Figure 4.2a) until it is enough to overcome the barrier for nucleation (b) on the top facet, which occurs as an extension of the truncated facets. Then a new monolayer quickly grows over the complete top facet via step flow growth (III). This partly depletes the particle, and the supersaturation is reduced, and the particle will then refill again for the next nucleation event [65].

4.1.1 Polytypism of III-V nanowires

An important parameter that is believed to determine the preferred crystal structure of binary semiconductors (II-VIs and III-Vs) is the ionicity of the bonds in between the atoms. Because binary III-V semiconductors consist of two different atomic elements, the bonds between these atoms will be of more or less ionic nature depending on the difference in electronegativity, X_i of the atomic species. The ionicity, f_i, for a compound AB is defined in its simplest form as

$$f_i = 1 - e^{-(X_A - X_B)^2/4}. \tag{4.1}$$

The nitrides have the most ionic bonds of all the III-Vs and preferentally form the WZ crystal structure. The bonds in the phosphides are less ionic, closely followed by the arsenides which all form the ZB crystal structure in bulk. The least ionic of all III-Vs are GaSb, which according to this model should be very stable in the ZB crystal structure [66].

In the $[\bar{1}\bar{1}\bar{1}]$ direction the cubic ZB structure consists of three distinct atomic bi-layers stacked (ABCABCABC). The WZ structure on the other hand has only two of these bi-layers (ABABAB), and has tri-fold symmetry. While most III-V semiconductors are ZB in bulk, this is not the case for III-V nanowires. For example, InAs nanowires are typically observed to be predominately WZ for small diameters [67], although this can be tuned with the growth parameters. In many cases a random mixture of WZ and ZB segments is observed, indicating that the formation of WZ and ZB can have similar probability for some conditions.

Random polymorphism is detrimental to the performance of nanowires in electronics and optics [68]. Recently, however, the understanding and

control over the formation of the WZ and ZB crystal phases in nanowires have improved significantly. It is now understood that the growth parameters, such as temperature, V/III ratio and growth rate play a major role for the formation of the crystal structure in nanowires. Also the nanowire diameter has a huge influence on the crystal structure [67]. This has enabled the demonstration of regular twin plane superlattices (TSLs) in ZB InAs nanowires [69], and WZ/ZB superlattices with extreme regularity [70]. Furthermore, it has also been reported that high doping levels also can change the crystal structure of nanowires [71]. For example Zn doping of InP nanowires tunes the nanowires from WZ into ZB TSLs [71, 72]. Similarily a high Se doping level turns InAs nanowires completely into defect-free ZB [73]. Highly sulphur-doped InP on the other hand is reported to have pure WZ structure [74].

4.1.2 Adatom diffusion length in MOVPE

A very important parameter in nanowire growth is the diffusion length of the adsorbed atoms on the various available surfaces. The diffusion length is the average length an adatom can diffuse on a surface before it is either incorporated into the solid or is desorbed. Because nanowires are very thin, most material adsorbs to the substrate and nanowire growth thus often relies on material supply from the substrate through surface diffusion [75]. This situation is depicted in Figure 4.3a where nanowires are shown collecting material from a circular substrate area around themselves. If this collection area is overlapping with that of another nanowire the nanowires will compete with each other for material. Dense nanowire arrays thus often have longer nanowires on the edges of the array than in the center, because the nanowires on the edge have fewer neighbors to compete with (Figure 4.3b) [76].

The high supply of material from the substrate surface can lead to a high supersaturation on the nanowire side facets. If nanowires are longer than a diffusion length, atoms adsorbed to the substrate or the lower part of the nanowire have only a small chance of reaching the seed particle on the nanowire top, and the supersaturation remains high on the nanowire side facets. This in turn can lead to significant radial growth, resulting in a tapered nanowire morphology. Thus long nanowires tend to look like bottles or bowling cones (Figure 4.3c), where the thin top part is roughly as long as the diffusion length of the growth rate-limiting species.

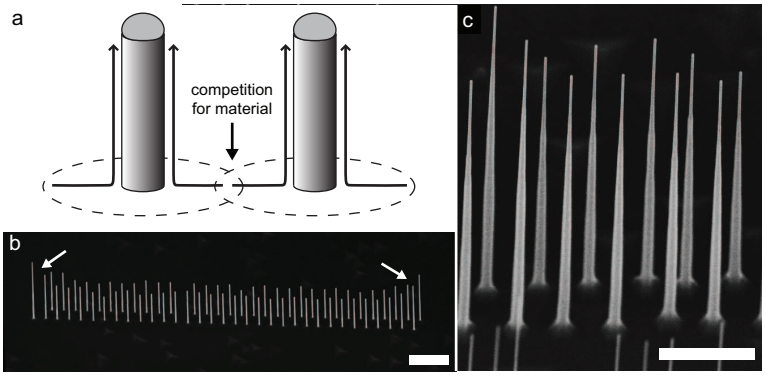

Figure 4.3: *(a) Schematic illustration of two nanowires positioned close enough to each other so that their substrate collection areas overlap. (b) Double line of InAs nanowires grown on an InAs/Si substrate. The nanowires at the edges of the pattern are longer due to having fewer neighbors to compete with for material. (c) InAs nanowires which are longer than the side facet diffusion length. Radial growth is evident in the lower part of the nanowires giving them a bottle-like shape. SEM images are taken at* 30° *tilt angle and scale bars correspond to* 1 µm *of length.*

4.2 Growth parameters in III-Sb nanowire growth

Antimonide nanowire growth via Au particles most probably proceeds via the same growth mechanism as the arsenides and phospides, and the fundamental issues such as competitive planar growth, radial growth and polymorphism are present also for the antimonides. There are, however, some important differences which arise due to the properties of the antimonide materials, the Sb atom and the Sb precursors.

Examples of GaAs/GaSb and InAs/InAsSb nanowires are shown in Figure 4.4. What is instantly clear from these images is that the antimonide nanowire segment has a larger diameter than the stem on which it is grown. The reason for this is detailed in Section 4.3.1. A more closer investigation of the nanowire morphology reveals that the side walls of all antimonide nanowires consist of {110} facets.

Radial growth on antimonide nanowires does not give rise to a tapered morphology. Instead the radial growth is uniform and proceeds in a faceted growth mode in which a new nucleated layer is completed before the next nucleation event occurs. The reason is that the diffusion length is very long on the flat {110} side facets of antimonide nanowires.[1]

[1]Pure WZ nanowires have flat $\{10\bar{1}0\}$ side facets, on which diffusion should also be

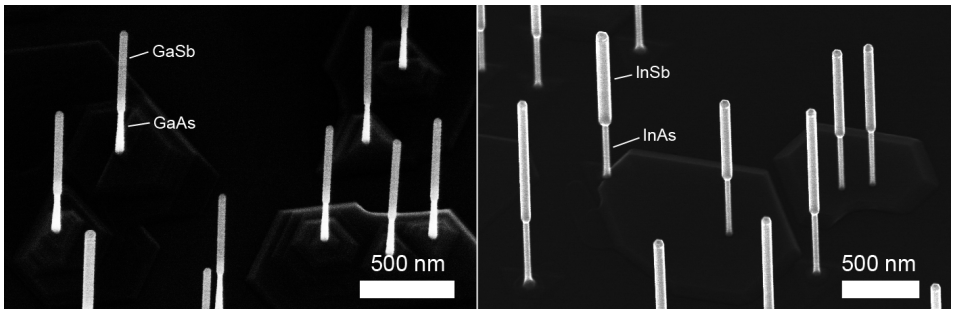

Figure 4.4: *SEM images taken at* 30° *tilt angle of typical (a) GaAs/GaSb and (b) InAs/InSb heterostructure nanowires.*

Similar to the case of III-Sb thin film growth, the low vapour pressure and segregating properties of Sb result in a strong Sb memory effect also for antimonide nanowire growth. This complicates the switching from a Sb-rich material to another as there is often a very high Sb background in the reactor. It is also necessary to clean the reactor inbetween consecutive antimonide-containing nanowire runs to obtain reproducibility. This can be done either through an in-situ HCl etching procedure or by heating up the reactor to at least 650 °C, at which temperature the Sb vapour pressure is reasonable high. This heating procedure can even be performed with a sample in the reactor as long as the substrate is unharmed by the high temperature. This procedure has been successfully used for GaSb nanowire growth (Paper I and II) and GaAsSb nanowire growth [77].

4.2.1 GaSb

A thorough study of the growth parameters for GaSb nanowire growth is made in Paper I, by growing GaAs/GaSb axial nanowire heterostructures. Here it was observed that the growth rate of the GaSb nanowires is dependent on the chosen TMSb molar fraction for V/III ratios of two and below (Figure 4.5a), but independent on the TMGa molar fraction. This means that the growth rate is limited solely by the group-V molar fraction for these conditions. For MOVPE growth of III-V semiconductors this is unusual, instead group-III limited growth is often observed.

The high sticking coefficient of Sb requires the TMGa and TMSb molar fractions to be roughly balanced, but it is observed that the growth rate is insensitive to the TMSb molar fraction for V/III ratio of two to four.

efficient. Such nanowires may thus also exhibit non-tapered radial growth.

This is probably related to an excess of Sb in the reactor. Even higher TMSb molar fraction ($>6 \times 10^{-5}$, V/III $>$ 3-4) leads to kinking nanowires or non-epitaxial growth (Figure 4.5d). Unpractically slow growth rates on the order of a few nm/min are obtained when supplying too low TMSb flow ($< 1 \times 10^{-5}$, V/III < 1).

Varying the TMGa molar fraction has some significant effects on the morphology of the GaSb nanowires. When using a low TMGa molar fraction ($< 1 \times 10^{-5}$) it is often observed that an an irregular GaSb shell forms around the GaAs nanowire stem instead of an axial heterostructure (Figure 4.5c). A too high TMGa molar fraction ($> 2 \times 10^{-5}$) on the other hand results in radial growth, making the nanowires uniformly thicker as they become longer (Figure 4.5e). In the middle of the parameter space, there is a small window in which straight nanowires GaSb nanowires are obtained with high yield and without any radial growth (Figure 4.6). These optimized conditions are reached with a relatively low TMGa molar fraction (1×10^{-5}) and a TMSb molar fraction below 3×10^{-5}. The reason why radial growth can be completely suppressed while the GaSb nanowire growth rate is still high is that the growth on the side walls of the nanowires is group-III-limited, in contrast to the group-V-limited GaSb nanowire growth. This implies that the effective V/III ratio inside the particle is much lower than outside.

The growth rate of GaSb nanowires was found to be kinetics-limited for growth temperatures up to 470 °C. Above this temperature the growth rate decreases because of the onset of parasitic growth on the GaAs substrate. For a V/III ratio of 1.2, the activation energy for the growth was evaluated from the slope of an Arrhenius plot to be 137 kcal/mol (Figure 4.5b). This is very close to the reported value for homogenous TMSb decomposition [78], implying that it is the decomposition of the TMSb precursor that sets the limit to the growth rate of the GaSb nanowires for this V/III ratio. It is important to note however, that this does not mean that the decomposition is complete already in the vapour phase, only that the rate limiting step is a homogenous reaction.

4.2.2 InSb

InSb nanowire growth in InAs/InSb, InP/InSb and GaAs/InSb axial heterostructures is investigated in Papers III and IV. The nanowires are successfully grown at temperatures between 400 and 460 °C. At 400 °C the nanowires have very large diameters and the growth does not progress in a stable manner.

There are many similarities between GaSb and InSb nanowire growth.

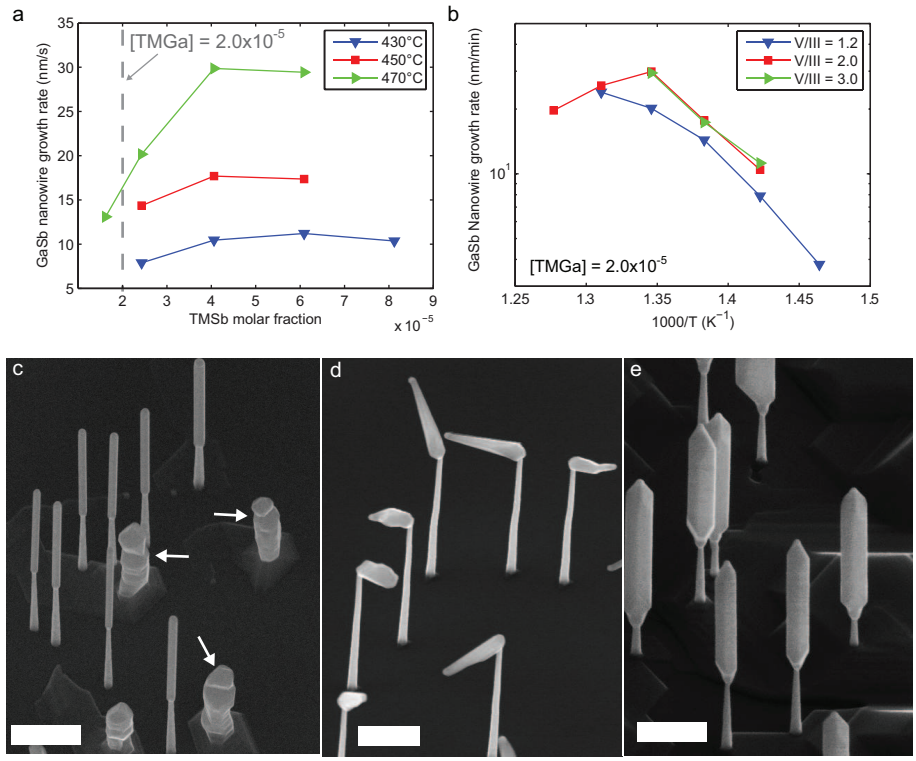

Figure 4.5: *(a) GaSb nanowire growth rate as function of TMSb molar fraction. (b) Arrhenius plot of the GaSb nanowire growth rate for three different V/III ratios. (c) GaSb nanowires grown with a very low TMGa molar fraction leading to rough core-shell nanowires indicated by the arrows. (d) When using a too high TMSb molar fraction GaSb nanowires grow non-epitaxially. (e) A high temperature or high molar fractions lead to significant radial growth without tapering. The scale bars correspond to* 500 nm.

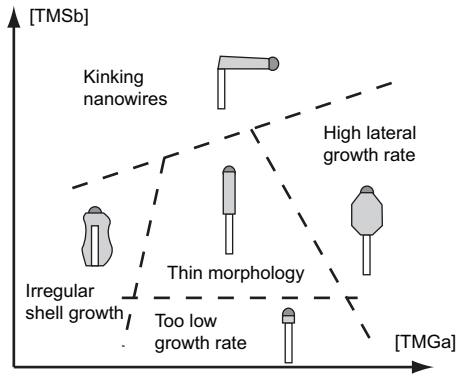

Figure 4.6: *Influence of the growth parameters in GaSb nanowire growth.*

As in the GaSb case, the InSb nanowire growth rate is strongly dependent on the TMSb molar fraction up to a V/III ratio of 15. For higher V/III ratios the growth rate decreases again. The decrease in growth rate at high V/III ratios is most probably caused by the rapidly increasing growth rate of parasitic InSb on the substrate surface.

Kinking was not observed for the InAs/InSb heterostructure despite high TMSb molar fractions (V/III $>$ 70). An explanation for this is that the effective V/III ratio inside the seed particles may still be low despite a very high nominal V/III ratios. TMIn decomposes already at 350 °C in hydrogen carrier gas, and is expected to be completely decomposed at typical nanowire growth temperatures, while TMSb is only partially decomposed. The effective V/III ratio is thus probably much lower than the nominal one[2], and the growth parameters in InSb nanowire growth are probably most often somewhere in the lower left part of the "thin morphology" window of Figure 4.6. Alternative Sb precursors, such as TESb or TDMASb, with lower decomposition temperatures can be used to improve the V/III balance. TDMASb has been used successfully in chemical beam epitaxy (CBE) at growth temperatures at which it is readily decomposed [79]. Additionally, precracked TESb has been used successfully in CBE to grow InSb nanowires from Au and Ag seed particles at temperatures below 400 °C [80, 81]. However, these nanowires suffer from significant radial growth and despite the low temperature there is much parasitic surface growth. This can be related to a short adatom diffusion length, because of the higher amount of free Sb, higher effective V/III ratio and also lower temperature.

[2]The seed particle itself may also take part in the reduction of the V/III ratio, as is discussed in Section 4.2.3.

The use of incompletely decomposed TMSb could thus be beneficial, since the partially decomposed Sb-alkyls may not react as strongly as free Sb with In, leading to decreased parasitic growth and longer diffusion length.

4.2.3 InAsSb

In Paper V the growth of ternary $InAs_{1-x}Sb_x$ nanowires is demonstrated. Nanowires were grown on InAs stems with solid compositions (x) ranging from only 4 at. % Sb up to almost pure InSb (see Figure 4.7a-b), and the composition of as-grown nanowires and InAsSb surface growth was evaluated by HRXRD. It was found that there is a significantly enhanced incorporation of Sb into the nanowires compared to the parasitic thin film growth (Figure 4.7c). For a V/III ratio of 15 the solid-vapour distribution coefficient for Sb is unity, giving a one-to-one relationship between the composition in the vapour (x_v) and the obtained x. This has been reported only to occur for V/III ratios of one or below in thin film InAsSb growth [45]. The results thus indicate that the V/III ratio at the nanowire growth front is about 15 times lower than elsewhere in the system. This important conclusion is the same as was made for GaSb and InSb nanowire growth, and may be general for antimonide nanowires. It may also have major implications for the crystal structure of the nanowires, as is discussed in Section 4.4.

The thermodynamic model used to extract the effective V/III ratio in the seed particles, assumes completely decomposed TMSb. At the growth temperature used in this work (450 °C) TMSb may only be partially decomposed, which should have resulted in a less than unit slope of the V/III = 15 curve in Figure 4.7c. Since it *does* have a unit slope, this implies that the TMSb *is* completely decomposed after all. AsH_3 is known to enhance the decomposition of other trimethyl- precursors [82, 83]. A possible explanation would thus be that the presence of AsH_3 enhances the decomposition of TMSb.

It is also observed that radial growth becomes significant on InAsSb nanwires if the solid composition is above $x > 0.5$, for all V/III ratios investigated here. It is possible that this is caused by a high Sb side wall coverage. AsH_3 can help to desorb Sb [54], and this could prevent radial growth when the AsH_3 molar fraction is high (and x is low). This does not explain, however, the lack of tapering when pure InSb nanowires are grown using the same conditions. The possibility of enhanced TMSb decomposition in conjunction with AsH_3 proposed in the above may however lead to enhanced radial growth. It is not clear at this point, however, why it is the solid composition and not the vapour composition that determines the

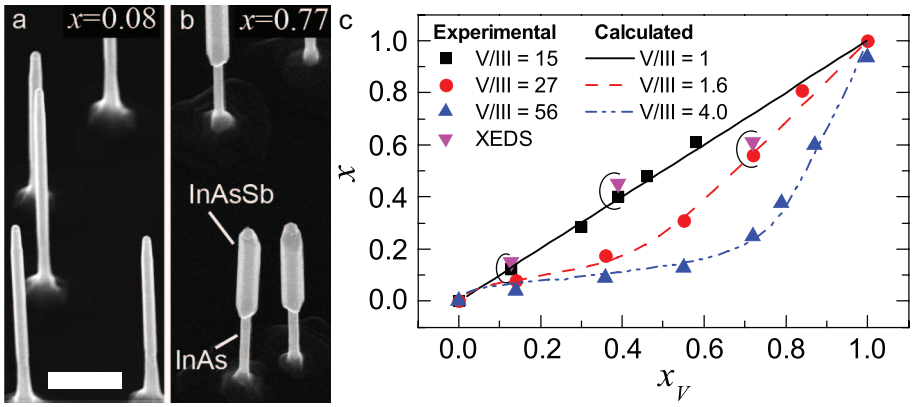

Figure 4.7: *SEM images at 30° tilt angle of $InAs/InAs_{1-x}Sb_x$ nanowires with (a) $x = 0.08$ and (b) $x = 0.77$ grown using the same V/III ratio and growth time. (c) InAsSb nanowire solid composition (x) for various x_v when grown with nominal V/III ratio=15, 27, and 56. For comparison, XEDS composition measurements are also shown for a few samples. The lines are solutions of a thermodynamic calculation using only the V/III ratio as a variable parameter.*

radial growth rate.

4.3 Seed particles in III-Sb nanowire growth

The metal seed particle plays a crucial role in the dynamics of the nanowire growth. First of all, the nanowire crystal grows at the interface between the particle and the epitaxial substrate, so it is the volume of the particle and its contact angle to the substrate that directly determines the diameter of the grown nanowire. One can get a rough estimate of the expected nanowire diameter from the pre-growth diameter of the seed particles. However, since the particles normally alloy with the group-III material, and may change both size and shape during this process, it is likely that the exact size of the nanowires will be somewhat different.

While the group-III species (Ga, In and Al) are all highly soluble in Au, this is not the case for neither As, P or N [84]. To understand growth of binary compounds from a Au-III-V alloy one must consider the ternary systems. In the Au-Ga-As system there is a pseudo-binary tie-line between Au and GaAs [85]. This means that the Au and GaAs phases can be in equilibrium with each other, and that supersaturation of GaAs in Au can result in deposition of solid GaAs, i.e. crystal growth. It is generally

believed that such pseudo-binary tie-lines are required for nanowire growth to be possible [84]. In support of this, the measured post-growth Ga content of gold particles on top of GaAs nanowires is typically very low (∼10%). For InAs and InP growth one often measure around 30% In in the particle post-growth [84]. Consistent with this, the Au-In-As system does lack the Au-InAs pseudobinary tie-line, but have pseudo-binary tie-lines for the γ-phase (29-32 at-%). The same is true for the Au-In-P system, and it is thus believed that InAs and InP growth occur along the γ-InAs and γ-InP pseudo-binary tie-lines, respectively.

In contrast to the other group-V species, Sb does have a significant, although low, solubility in Au at normal growth temperatures (1.12 at. % at 600 °C) [85]. Thus, one may expect to find a low Sb concentration in the seed particles after GaSb or InSb nanowire growth. Often around 1 at. % Sb is measured in the particles, but the quantification of such low Sb concentrations in XEDS is very uncertain due to the overlap between the In- and Sb-related core-level peaks. The particles consist of almost stochiometric AuGa or $AuGa_2$ in the GaSb case, and AuIn or $AuIn_2$ in the InSb case. The reason for this becomes evident when studying the Au-Ga-Sb and Au-In-Sb ternary phase diagrams (Figure 4.8). For example in the Au-Ga-Sb system, the only compounds that have pseudo-binary tie-lines with GaSb are AuGa and $AuGa_2$. These are thus the only compounds that can exist in equilibrium with GaSb. It should be noted however, that the phase-diagram for the Au-Ga-Sb system data is valid only for room-temperature. It is possible that at elevated temperatures other pseudo-binary systems are present. Our results indicate that at least up to 470 °C there are no pseudo-binary tie-lines to GaSb from Au-Ga phases with lower Ga content than 50 at. %. The same is also true for InSb.

Which of the two possible phases (AuGa or $AuGa_2$) that are observed after growth depends on the TMSb molar fraction in GaSb growth. A high TMSb molar fraction results in a AuGa phase, while a low molar fraction results in a $AuGa_2$ phase. A similar observation is made for InSb nanowires, although a very high V/III ratio (> 100) is needed to observe the AuIn phase, possibly because of the lower effective V/III ratio during InSb growth compared to GaSb growth with the same nominal V/III ratio.

4.3.1 Diameter increase

The high group-III concentration during GaSb and InSb nanowire growth has a very distinct effect when growing these nanowires in heterostructures with their As-counterparts. For example, as the growth is switched from GaAs nanowire growth to GaSb growth there is a clear diameter increase

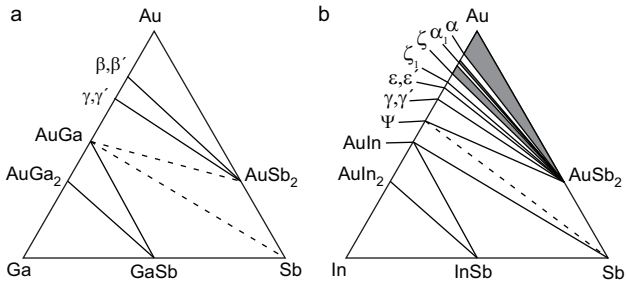

Figure 4.8: *Ternary phase diagrams for the (a) Au-Ga-Sb and (b) Au-In-Sb systems. The lines indicate pseudo-binary tie-lines. Dashed lines mean that a tie-line is likely but has not been verified [85].*

occurring (Figure 4.4). During the GaAs growth, the particle contains a low concentration of Ga. As Sb is introduced into the reactor the equilibrium state of the particle is altered and Ga is collected until it contains more than 50 at-% Ga. Obviously this must increase the particle diameter drastically, and in turn also the diameter of the GaSb segment. Additionally, it is very likely that the contact angle of the particle is changed during this phase change, which could also influence the final size of the GaSb nanowires. A difference in lattice parameter between the two materials may also contribute to the diameter difference.

A high In content in the seed particles is also observed in InSb nanowire growth, leading to a similar diameter increase as for GaAs/GaSb. The length over which the diameter transition occurs appears to be on the order of tens of nanometers, but the transition region may be smoothened out by overgrowth at the junction. The transition region is less abrupt for InAs/InAsSb nanowires, possibly due to the more gradual compositional change in these nanowires.

4.3.2 Switching the group-III atom

The high group-III content of the seed particles complicates the growth of heterostructure nanowires in which the group-III atom is switched. For example, when switching from GaSb to InAs growth, the high amount of Ga in the particle needs to be depleted and the amount of In must be increased above the equilibrium concentration before growth of InAs is initialized. The dynamics of this process was studied in Paper VII by *ex-situ* analysis of the particle and nanowire composition of samples grown with various InAs growth times. It was found that there is a delay between the introduction

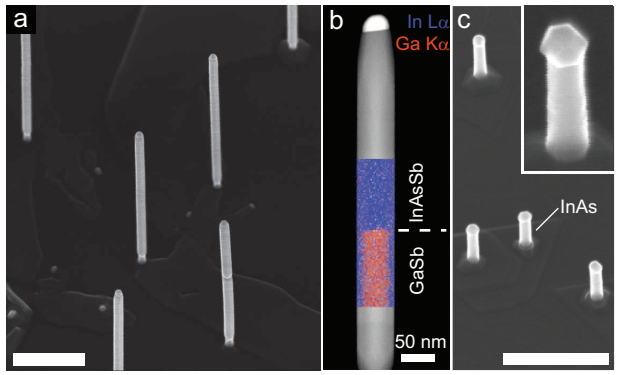

Figure 4.9: *(a) SEM image of InAs-on-GaSb nanowires which have long InAs(Sb) segments grown on top of the GaSb nanowires. (b) XEDS map overlayed on a STEM image in the* ⟨112⟩ *direction, revealing an abrupt Ga-to-In transition as well as a thin InAs(Sb) shell around the GaSb segment. (c) SEM image of GaSb-on-InAs nanowires. No GaSb axial segment grows at* 450 °C*, but the particle is faceted (inset).*

of TMIn and AsH_3 into the growth reactor and the actual start of the InAs growth. The length of this delay was found to be 2-3 minutes at 460 °C. During the time before growth commences, the Ga atoms in the particle are substituted by In atoms. This process is effective and complete, probably due to the higher affinity for In in Au, compared to Ga in Au [86, 87]. The In concentration increases until the particle consists of roughly 70 at. % In and 30 at. % Au. Since no growth occurs until all Ga is depleted from the particle, the heterojunction is extremely abrupt for the group-III elements, below the spatial resolution of XEDS (∼3 nm) (Figure 4.9b).

The growth of nanowires with GaSb segments on InAs segments is studied in Paper VI. In contrast to InAsSb growth on GaSb, it was found that growth of GaSb nanowires on InAs nanowires is more challenging. Even when utilizing very long growth times, high precursor flows, or long purge steps GaSb nanowire growth on InAs was not achieved (Figure 4.9c). In this case, the particle contains 30-40 at. % In before the introduction of Sb, and this makes it difficult for Ga to enter the particle. Thus, even after a 60 min GaSb growth step, the In concentration in the seed particle has not decreased. In fact, it was found that the In concentration relative to Au was even higher after the GaSb growth step (Au:In:Ga = 40:40:20), which is explained by that the Sb introduction changes the equilibrium composition towards a higher In content. The lack of GaSb growth was explained by the lack of a suitable pseudo-binary tie-line at low Ga concentrations.

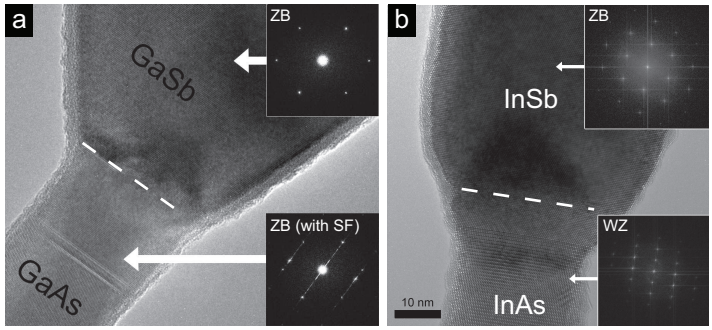

Figure 4.10: *HRTEM images of (a) GaAs/GaSb and (b) InAs/InSb nanowire heterojunctions depicting the pure ZB crystal structure of the III-Sb nanowires. The insets of (a) are the diffraction patterns for the two nanowire segments, while the insets of (b) are the Fourier transformed image of the two segments of the nanowire.*

In very recent experiments where instead a growth temperature of 500 °C was used, it was possible to grow axial GaSb nanowire segments on InAs nanowires. The particles in this case have very similar compositions as on the nanowires grown at lower temperature (Au:In:Ga = 42:42:16). That GaSb growth on InAs nanowires is possible at 500 °C indicates the existance of a pseudobinary tie-line between GaSb and a low-Ga alloy which is not present at lower temperatures.

4.4 Crystal Structure of III-Sb nanowires

In bulk and in thin films all antimonides crystallizes in the ZB structure. The crystal structure observed in GaSb and InSb nanowires is also typically pure, defect-free ZB crystal structure, without either stacking faults or twin planes (Figure 4.10). In fact, the tendency for the antimonide materials to form ZB is so strong that in ternary nanowires such as GaAsSb and InAsSb, only a few at. % of Sb is needed to turn the crystal structure from WZ into pure ZB [88, 89]. Dheeraj et al. [88] produced GaAsSb inserts in WZ GaAs, and observed a direct transition into ZB at the GaAs-to-GaAsSb interface and a ZB-WZ transition at the other interface at which the Sb supply was terminated.

As was described in Section 4.1.1, the crystal structure of nanowires is typically either WZ or ZB or even a mixture of both. A general tendency of a material to form either WZ or ZB structure can be eluded from the ionicity of the atomic bonds, and since GaSb has the lowest ionicity of all III-Vs it

is thus tempting to explain its preference for ZB simply by this argument. InSb however, has higher ionicity [66] than GaAs which is often found to be WZ in nanowires [90]. Despite this, InSb is in most conditions found to be pure ZB. Mandl et al. [91] however, report InSb nanowire growth using In particles instead of Au particles, and do observe a change in crystal structure from pure ZB to pure WZ along the length of the nanowires. This was explained by a gradually increased V/III ratio as the growth proceeds, due to a gradual build-up of the Sb background in the reactor. In addition, InSb nanowires grown using Ag particles at temperatures below 410 °C in CBE exhibit numerous stacking defects and twin planes [81]. In a very detailed study of the crystal structure control of InAs nanowires, it was observed that the V/III ratio has a strong effect on which crystal structure the nanowires form, with a high V/III ratio promoting the formation of WZ over ZB [67].

The influence of growth parameters on the crystal structure in nanowires is a subject which is still under investigation. However, the reports described above, in combination with the observations of a reduced effective V/III ratio for GaSb, InSb, and InAsSb nanowire growth (see Section 4.2), suggest that the typical observation of ZB in Au-nucleated antimonide nanowires could be explained by a low effective V/III ratio rather than the ionicity of the bonds. The ionicity probably sets the crystal structure preference, but the growth parameters are likely the main determinators.

4.5 Nucleation of III-Sb nanowires

One important challenge for antimonide nanowire growth is the difficulty to nucleate the nanowires directly on a substrate. This has resulted in that most reported antimonide nanowires are grown on a stem of some other material. For some applications, the use of a stem may be unwanted and it is thus important to investigate how to grow antimonide nanowires also without a stem. This chapter has discussed several examples of III-Sb nanowires grown with III-As nanowire stems. Figure 4.11c instead displays the result of an attempt to grow GaSb nanowires without a stem (470 °C, TMGa m.f. $= 7.1 \times 10^{-6}$, V/III = 3.4). Clearly, the growth is particle-assisted, but without the inclusion of a nanowire stem there is no GaSb nanowire growth. Instead, the seed particles are "pushed" around, leaving a trail of GaSb crystal on the GaAs substrate.

To investigate what is the effect of Sb exposure during the nucleation phase of nanowire growth, Au nanoparticles deposited on GaAs(111)B substrates were annealed under either AsH_3 or TMSb flow. Afterwards, the

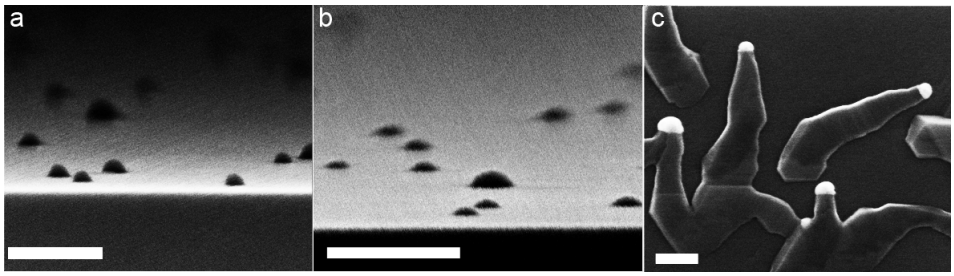

Figure 4.11: *Au particles on a GaAs(111)B substrate after annealing at* 700 °C *and cooling under (a) AsH_3 or (b) TMSb flow. Note the difference in contact angle between the two cases. (c) Au-Ga particles with GaSb trail after an attempt to nucleate GaSb nanowires directly on a GaAs(111)B substrate at* 470 °C. *Scale bars correspond to* 200 nm.

samples were inspected in SEM and a significant difference in the particle shape was observed. The particles annealed in AsH_3 (Figure 4.11a) were almost hemispherical, while the ones annealed in TMSb (Figure 4.11b) were much flatter. Sb exposure thus has a significant effect on the morphology of the Au particles. With this observation in mind, a possible model to explain the difficulty for III-Sb nanowire nucleation directly on planar substrates is developed in the following subsections.

4.5.1 Particle contact angle

The wetting angle, θ_c, of a liquid drop on a surface is determined by the interface energies of the liquid-vapour interface (γ_{lv}), the liquid-solid interface (γ_{sl}) and the vapour-solid (γ_{sv}) interface (Figure 4.12a). Interface energies originate from the dangling atomic bonds at the edge of a phase, and the total interface energy of a multi-phase system is minimized by reshaping geometry of the interfaces. In the vapour-liquid-solid system here, the contact angle of the liquid drop to the substrate can be calculated by the Young equation:

$$\gamma_{sl} + \gamma_{lv} \cos\theta_c = \gamma_{sv} \tag{4.2}$$

A large contact angle leads to an almost spherical drop, which is nearly not in contact with the substrate. A very small contact angle on the other hand means that the drop almost completely wets the substrate. It is believed to be critical for the contact angle to be larger than 90° for stable growth of nanowires [92]. This criterion may be used to explain why III-

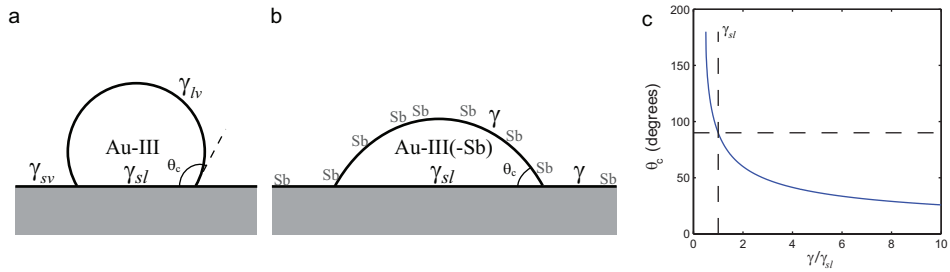

Figure 4.12: *A seed particle on a substrate (a) without and with (b) a coverage of Sb, and definition of the surface energies and contact angle. (c) Contact angle as function of the γ/γ_{sl} ratio.*

Sb nanowire nucleation often fails when performed without the use of a nanowire stem.

4.5.2 Effect of Sb on surface tension

As was discussed in Section 3.2.5, the low volatility and high segregation coefficient makes Sb a very strong surfactant which modifies the properties of surfaces that it adsorbs to. If Sb is introduced into the system depicted in Figure 4.12a, it will thus stick to any surfaces available, namely the vapour-solid and vapour-particle interfaces (Figure 4.12b). The chemisorption of Sb to GaAs(111)B surfaces has been studied in detail by Moriarty et al. [93] who concludes that Sb forms long trimer-chains on the surface. Below 375 °C, these chains are partial and coexist with single Sb-trimers, but above this temperature they form a long-range ordered (1×3) reconstruction. It was further determined that this surface has a higher surface energy than the clean GaAs (2×2) reconstruction. It is thus possible that the solid-vapour interface of our system similarily obtains an increased surface energy due to the high Sb coverage. Since similar surface structures have been observed also on other Sb-rich surfaces [94] one may assume that the vapour-particle interface also obtains an increased surface energy when there is a high Sb coverage. The particle-solid interface, on the other hand, may not be significantly affected by the Sb coverage because of the low Sb concentration inside the particle. As a first approximation one may thus assume that $\gamma_{sv} = \gamma_{lv} \equiv \gamma$, so that one can express the contact angle as

$$\theta_c = \cos^{-1}\left(1 - \frac{\gamma_{sl}}{\gamma}\right). \tag{4.3}$$

This relation is plotted as function of γ/γ_{sl} in Figure 4.12c, where for $\gamma/\gamma_{sl} > 1$, θ_c is smaller than 90°. Even if γ_{sv} and γ_{lv} are not equal, one still obtains $\theta_c < 90°$, as long as γ_{sv} and γ_{lv} are both larger than γ_{sl}. Although no absolute values for the interface energies are available, it is noteworthy that a high Sb coverage may indeed result in a particle contact angle below what is necessary for nanowire nucleation [92]. This may be the reason for why antimonide nanowire nucleation often fails when performed directly on substrates. It should also be noted that Nebolsin et al. [92] previously reported that the surfactants Sb, Sn and Bi should prevent Si nanowire growth for this very reason. Suppression of Si nanowire growth by Sb addition has also been verified experimentally by Nimmatoori et al. [95]. The reason why III-Sb nanowires can be grown successfully on top of nanowire stems, may be that the finite size of the (111)B facet on the top of the nanowire prevents the particle from expanding the solid-liquid interface, thus keeping the contact angle above 90° in size.

4.5.3 Nucleation directly on a substrate

There are numerous reports on Au-nucleated GaSb and InSb nanowire growth without a stem, but in most of these the nanowire growth is nonepitaxial [96, 97]. However, there are reports on epitaxial growth of both GaSb and InSb nanowires without the use of nanowire stems [80, 81, 91, 98**?**]. These reports will be briefly discussed here.

Park et al. [98] have successfully grown InSb nanowires from Au particles on InSb(111) substrates. The growth was performed in a chemical vapour deposition (CVD) reactor and the substrate temperature was 400 °C. The nanowires appear to grow epitaxially in the ⟨110⟩ direction but with the particles wetting a horizontal (111)B facet. The authors also observe an irregularily shaped crystalline deposit at the base of each nanowire from which the nucleation seems to originate. Judging from the presented data, the yield of epitaxial growth appears to be rather low.

Vogel et al. reported CBE growth of InSb nanowires from Au particles directly on InSb(111)B substrates [80]. At temperatures below 400 °C epitaxial growth in the ⟨111⟩B direction is obtained, while above 400 °C they observe no nanowire growth unless the V/III ratio is kept higher than six. In contrast to the work of Park et al., here the yield of epitaxial nanowires is high.

Finally, Ghalamestani et al. [99] demonstrate MOVPE growth of GaSb nanowires using Au particles directly on GaSb/InAs thin films on Si(111) substrates. In this case, also a low growth temperature (420 °C) is necessary in addition to high source flows. Judging from the SEM images, the GaSb

nanowires do not grow perpendicular to the substrate surface. The growth direction is thus unclear in this case.

What these studies have in common is the low growth temperature and the usage of a high V/III ratio. A high nominal V/III ratio probably increases the Sb concentration in the particle and could thus reduce the difference between the various interface energies (by increasing γ_{sl}). Furthermore, at temperatures around 400 °C the high-energy Sb-rich surface reconstruction may be incomplete [93]. Both these effects could in turn lead to an increase in the particle contact angle, and possibly successful nanowire nucleation.

4.6 Summary

This chapter has described the properties of Sb-based nanowire growth in terms of growth parameters, crystal structure and nanowire nucleation. The most important conclusion is that, upon introduction of Sb into the MOVPE system, the equilibrium concentration of the group-III elements in the Au seed particle increases to 50% or more. It was concluded separately for GaSb, InAs and InAsSb nanowires that the effective V/III ratio is reduced inside the seed particle compared to elsewhere in the system. This is explained by the high group-III content of the seed particle. The direct consequence of the reduced V/III ratio is the possibility to choose growth parameters for which parasitic growth is suppressed and the axial nanowire growth rate is high. The indirect consequences may be an strong tendency to form defect-free ZB crystal structure, and to complicate the nucleation of Sb-based nanowires directly on substrates.

Chapter 5

GaSb/InAsSb tunnel devices

The utilization of quantum tunneling can fundamentally alter the way that electronic devices operate. Devices with current transport based on tunneling, such as resonant tunneling diodes, interband tunneling diodes (TDs) and tunneling field effect transistors (TFETs), may reduce the need for aggressive device scaling by improving performance and reducing power consumption by other means. In Papers VII-IX, the GaSb/InAsSb nanowire heterojunction has been investigated for application as TDs and TFETs. An introduction to these papers is given in this chapter. In Section 5.1, the growth of GaSb/InAsSb axial nanowires is described. Section 5.2 presents a novel in-situ annealing technique that selectively etches the GaSb/InAsSb heterojunction and thus possibly enables a heterojunction with a 1D DOS in connection with three dimensional contact regions. In Section 5.3 and 5.4, electrical characterization and theoretical simulations are presented of GaSb/InAsSb TDs and TFETs, respectively.

5.1 Growth of GaSb/InAsSb nanowire heterostructures

As described in Section 4.3.2, an axial GaSb/InAs heterojunction nanowire is characterized by a very abrupt heterointerface, a high Sb carry-over into the InAs segment and a significant amount of InAs shell growth on the GaSb segment. Because of the high Sb content in the nominal InAs segment, the grown material will in the following be denoted as InAsSb while the growth of the material will be referred to as InAs growth.

Figure 5.1 consists of typical SEM images of GaSb/InAsSb nanowires grown on GaAs nanowire stems taken at 30° tilt angle. The GaAs stem at

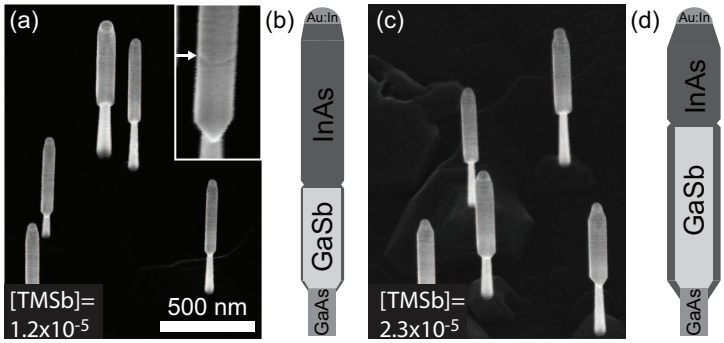

Figure 5.1: *SEM images at 30° tilt angle of GaSb/InAsSb nanowires grown on GaAs stems using a TMSb molar fraction of (a)* 1.2×10^{-5} *and (c)* 2.3×10^{-5} *during the GaSb growth step, respectively. The arrow in the inset indicates the occurrence of additional faceting near the GaSb/InAsSb heterojunction. The schematic images (b,d) clarifies the structural differences between the nanowires in a and c, respectively.*

the bottom of the nanowires has smaller diameter than the GaSb/InAsSb heterostructure which has a uniform hexagonal cross-section with {110} side facets. The InAsSb shell, which forms uniformly over the full length of the GaSb/InAs(Sb) heterostructure, could potentially result in an alternative current pathway into the InAsSb nanowire segment, thereby by-passing the tunnel junction and may considerably degrade the electrical properties of the structure.

The parameters for InAs nanowire growth on GaSb nanowires were optimized to minimize radial growth, but despite a large effort this was not successful. Remarkably, instead it was found that the growth parameters for the preceding GaSb growth step is what primarily determines the InAsSb radial growth rate. Figure 5.1c shows a SEM image of GaSb/InAsSb nanowires where the GaSb segment was grown with a TMSb molar fraction of 2.3×10^{-5} (V/III=3.2). A reference sample allow us to estimate the InAsSb shell thickness to be on average 15 nm thick, giving a radial growth rate of 1.3 nm/min. In contrast, the thickness of the InAsSb shell on the nanowires in Figure 5.1a is less than 4nm, corresponding to a growth rate of 0.5nm/min. Most remarkably, the axial InAsSb growth rate in this sample is twice as high as in Figure 5.1c. The same InAs growth parameters were used for both these samples; the only difference was in the chosen TMSb molar fraction during the GaSb growth step, which in Figure 5.1a is only 1.2×10^{-5}. It is very likely that excess Sb deposited during the GaSb growth step lingers on the nanowire side walls, and strongly enhances the InAsSb

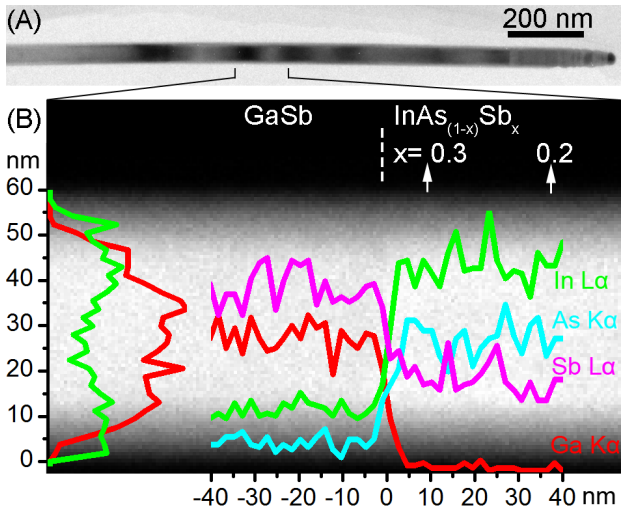

Figure 5.2: *(a) TEM image of a GaSb/InAsSb nanowire. (b) STEM image of the heterojunction region with superimposed radial and axial EDS line profiles with quantified point-measurements also included above the nanowire. The Sb signal decreases and As increases abruptly, although a significant Sb background remains in the InAsSb segment.*

nucleation rate on the {110} side facets during the InAs growth step. The enhanced axial growth rate for the nanowires in Figure 5.1a, is caused by the reduction of parasitical shell growth.

5.1.1 Sb content

The large carry-over of Sb into the InAs growth step leads to the formation of InAsSb instead of pure InAs. An XEDS linescan overlayed on a STEM image is displayed in Figure 5.2, depicting a typical GaSb/InAsSb nanowire heterojunction. At the heterojunction, the Sb signal drops abruptly, but remains finite. Point analysis near the interface gives an Sb concentration of 15 at. % ($x = 0.3$). Away from the interface the Sb signal gradually decreases, and XEDS point analysis near the seed particle measures an Sb concentration of 5 at. % ($x = 0.1$). The gradual decrease of Sb is interpreted as a gradual reduction of background Sb in the reactor, since no Sb is supplied after completion of the GaSb growth step. To reduce the Sb concentration in the InAsSb nanowire a pause in AsH_3 ambient can be included after the first minute of nominal InAs growth (after which the particle has already evacuated most Ga). The result of a 5 min long growth

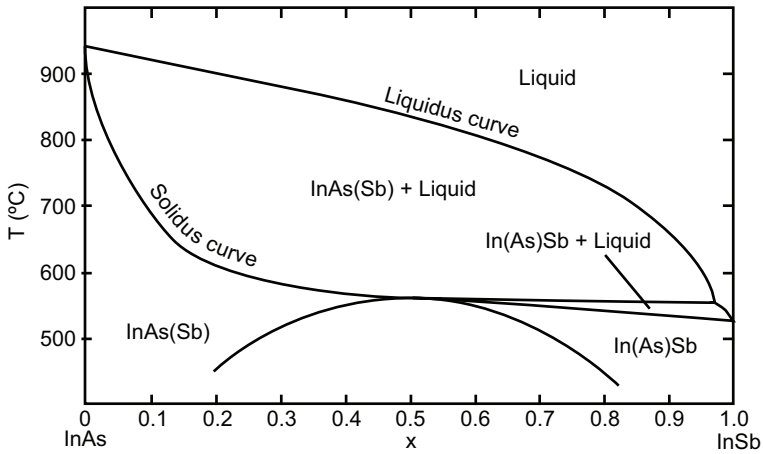

Figure 5.3: *Calculated InSb-InAs pseudo-binary phase diagram. Adopted from Ref. [100].*

interrupt while flowing AsH_3 followed by 6 min of consecutive InAs growth was to significantly decrease the Sb content in the InAsSb nanowire, to 7-8.5 at. % (x=0.14-0.17) at the heterojunction and to only 2 at. % (x=0.04) near the seed particle. By optimizing the V/III ratio during the GaSb growth to minimize the excess Sb, it may be possible to further decrease the Sb carry-over into the InAs nanowire growth.

5.2 Heterojunction diameter control

An observation that was made when investigating GaSb/InAsSb nanowires in SEM was that GaSb/InAsSb nanowires cooled in H_2 instead of AsH_3 often had a constriction close to the axial heterojunction. A more detailed investigation of these nanowires in HRTEM identified this contriction as a set of {111}A, {111}B, {001} and {113}-like facets, located predominately on the InAsSb side of the interface. It is hypothesized that these facets arise during the cooling phase after growth, due to the lack of AsH_3 stabilization. This hypothesis can be understood through the InSb-InAs pseudo-binary phase diagram. InSb and InAs have melting temperatures of 527 °C and 942 °C, respectively. The large difference in melting temperature results in that the phase stability of the InAsSb alloy depends strongly on its chemical composition. The InAs-InSb pseudo-binary phase diagram as calculated by Stringfellow [100] is shown in Figure 5.3. Here the solidus curve for $InAs_{1-x}Sb_x$ drops rapidly with increasing Sb content in the range

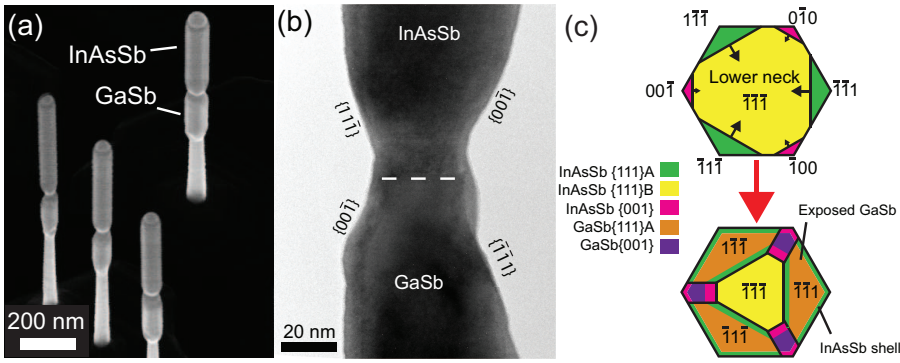

Figure 5.4: *(a) SEM image at 30° tilt and (b) HRTEM image in the* $\langle 1\bar{1}0 \rangle$ *zone of GaAs/GaSb/InAsSb nanowires annealed at 490 °C for 10 min. (c) Schematic visualization of the selective etching process in which* $\{111\}A$ *facets are preferentially etched.*

$0 < x < 0.3$, and is close to 550 °C already for $x > 0.2$. This range corresponds closely to the compositional gradient in the GaSb/InAsSb nanowires, and it is thus likely that the part of the InAsSb segment close to the heterojunction is much less stable than the rest of the nanowire. The solidus curve may move to even lower temperatures due to the high curvature at the edges of the hexagonal nanowire cross-section, and exaggerate this effect. Furthermore, it is well established that a group-V overpressure is needed to stabilize III-V semiconductors at elevated temperatures. The constrictions at the heterojunctions may thus form through removal of unstabilized InAsSb with high Sb-content.

The observations described above where used to selectively reduce the heterojunction diameter of GaSb/InAsSb nanowires by annealing at elevated temperatures without AsH_3 stabilization. The result of this process is shown in Figure 5.4a, from which it is clear that a significant diameter reduction can be achieved. Neck diameters as small as 25 nm were often observed (Figure 5.4b). This type of structures are attractive for device applications since a one-dimensional DOS may be obtained at the tunnel junction, connected to thicker contact regions with less resistance. Furthermore, a heterojunction clearly visible in SEM is convenient for transistor processing, where precise gate alignment may be crucial [101].

It is observed that both the presence of Sb and As during the annealing stabilizes the nanowires and strongly reduces the etching rate. Even Sb remaining from the GaSb growth can prevent efficient etching at the GaSb/InAsSb interface. An Sb purge step under AsH_3 flow can be intro-

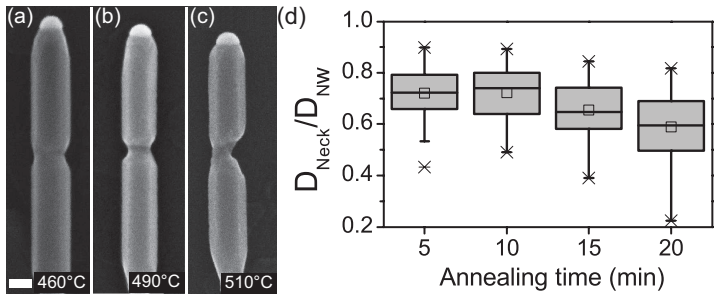

Figure 5.5: *Side-view SEM images of representative GaSb/InAsSb nanowires annealed at (a) 460, (b) 490, and (c) 510 °C for 10 min. (d) The ratio between the neck width (D_{Neck}) and overall nanowire diameter (D_{NW}) plotted as a function of annealing time.*

duced before the annealing step to achieve improved control of the etching.

Detailed analysis of etched nanowires indicate that the etching progresses to a large extent through etching of {111}A facets on the InAsSb side of the heterojunction (Figure 5.4b-c). These facets are group-III-terminated, and it is likely that the group-V deficit environment promotes etching of these facets.

Using the annealing technique the diameter of the heterojunction can now be controlled by choosing annealing temperature and annealing time (Figure 5.5). The etching proceeds faster and with larger variation at higher temperatures. This is consistent with the proposed model, from which a temperature controlled process is expected, and the selectivity should decrease for higher temperatures. The annealing procedure has also been successfully performed at a later occasion, on samples that have been exposed to air for some time. This gives flexibility to the procedure, with the added possibility of performing it in other types of equipment.

5.3 Modeling of TDs

To understand the transport properties of the GaSb/InAsSb heterojunction devices, a theoretical model has been developed. In this section, the model is described and is used to explain the I-V characteristics of GaSb/InAsSb nanowire TDs. A brief introduction to the operation of conventional TDs is also given in subsection 5.3.4.

5.3.1 Wentzel-Kramers-Brillouin approximation

The Schrödinger equation, $\mathbf{H}\psi = E\psi$, describes the energies of electron waves in quantum mechanics. For most electric potentials there is no analytic solution to the Schrödinger equation, and approximate methods need to be applied. The Wentzel-Kramers-Brillouin (WKB) approximation is a versatile approximative method for solving the Schrödinger equation in various potentials, and is described here in its simplest form for one spatial dimension (z) [102]. The plane wave part of the Bloch wave function (Eq. 2.3) can be expressed as

$$\psi(z) = e^{i\phi(z)}, \tag{5.1}$$

where $\phi(z)$ is the phase of the plane wave. Inserting Eq. 5.1 into the Schrödinger equation and assuming a slowly varying potential, $U(z)$, one obtains

$$\phi(z) \approx \pm \int_z k(z')dz' + C, \tag{5.2}$$

where $k(z)$ is the wave vector of the electron, which may vary with z due a varying potential landscape. Thus, in this approximation the wave function becomes

$$\psi(z) \approx \exp\left(\pm i \int_z k(z')dz'\right). \tag{5.3}$$

This relation is very useful for many applications where there is an arbitrarily varying electric potential[1]. For electrons in a semiconductor $k(z)$ can be defined using Eq. 2.9 as

$$k(z) = \sqrt{\frac{2m_0 m_{eff}}{\hbar^2}[E - E_c(z)]}, \tag{5.4}$$

where $E_c(z)$ is the energy of the spatially varying conduction band edge. In this thesis the WKB approximation is used to calculate the probability for tunneling through a potential barrier and for estimating the energy levels in an arbitrary potential. These applications will be described in the following sub-sections.

[1] This is a zero-order approximation $\left(\frac{\partial^2\phi}{\partial x^2} \approx 0\right)$. A less crude first-order approximation yields a relation very similar to Eq. 5.3, namely: $\psi(x) \approx \frac{1}{\sqrt{k(x)}} \exp\left(\pm i \int k(x)dx\right)$.

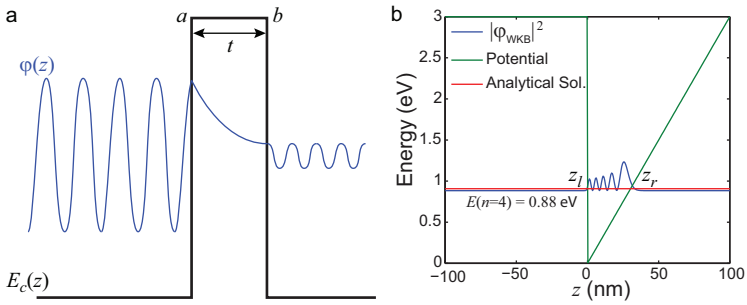

Figure 5.6: *(a) Schematic image of an electron wave tunneling through a potential barrier. (b) Example of a bound state in a triangular potential well 3 eV deep. The result from using the WKB approximation is here compared with the analytical solution to an infinite triangular well.*

5.3.2 Tunneling through a potential barrier

An electron incident onto a potential barrier of a certain thickness has a finite probability of being transferred through it. This phenomenon is called *tunneling* and is an important consequence of the wave nature of the electron. The tunneling probability through a barrier defined from $z = a$ to $z = b$ with the thickness, t, (Figure 5.6a) can be expressed as the probability of finding the electron at $z = b$ divided by the probability of finding it at $z = a$, i.e. $T = |\psi(b)|^2/|\psi(a)|^2$. Since $E < E_c(z)$ within the barrier, $k(z)$ is a complex function typically written as $k(z) = -i\kappa(z)$, and the wave function has the form of a decaying exponential. Using Eq. 5.3 the tunneling probability can be written as

$$T(a \to b) = \exp\left(-2\int_a^b \kappa(z)dz\right). \tag{5.5}$$

It is clear that T decreases exponentially with increased barrier thickness. Also, since $\kappa(z) \sim \sqrt{E_c(z) - E}$, T decreases exponentially with increasing barrier height. The tunneling mechanism is thus very strongly dependent on the geometry of the tunnel barrier. As an example, consider an electron which tunnels through a 0.5 eV high potential barrier with a thickness of either 1.0 or 5.0 nm. Using Eq. 5.5 one obtains $T_{1\,nm} = 0.46$, and $T_{5\,nm} = 0.021$ for the two barriers, respectively.

5.3.3 Bound states in a well

The WKB approximation can also be used to calculate the energies of bound electron states in a potential well, such as the one depicted in Figure 5.6b. The most important limitation of the WKB approximation is that it assumes a slowly varying potential. This assumption fails near the classical turning points, z_l and z_r, where $E = E_c(z_l) = E_c(z_r)$. One can, however, define connection formulas which connect the wave function outside and inside potential barriers, to obtain conformable WKB solutions in the separate regions. To obtain the discrete energy levels within the potential well one can imagine a plane wave with initial phase ϕ_0 making the round trip from the left edge of the well to the right and back again. To prevent destructive interference the phase of the wave after the round trip should be equal to $\phi_1 = \phi_0 + 2\pi n$, where $n = 0, 1, 2, ...$ This condition can also be written as

$$2\int_{z_l}^{z_r} k(z)dz + \partial\phi_L + \partial\phi_R = 2\pi n \tag{5.6}$$

where the first term is the phase picked up during the round trip within the well, while $\partial\phi_L$ and $\partial\phi_R$ are the phases picked up by the reflection of the wave in the left and right interfaces, respectively. The phase change at the interfaces depend on the connection formulas which are used, and are thus dependent on the steepness of the well edges. For a vertical wall $\partial\phi = \pi$, while a softer wall leads to $\partial\phi = \pi/2$. By choosing the correct phase changes for the geometry of the specific potential well Eq. 5.6 can be solved for various values of n to give the energy of the bound states [102].

5.3.4 Conventional TDs

Conventional TDs typically consist of a degenerately doped p-n junction in which the Fermi level on each side of the junction lies either within the conduction band or the valence band, respectively. This gives a very sharp band bending and a short spatial distance between the p- and n-regions which electrons or holes can tunnel across. The tunnel barrier is formed by the band bending in the space-charge region, and it is thus the band gap that determines the height of the tunnel barrier. This means that a narrow band gap results in a high tunnel probability. Furthermore, the higher the doping level, the thinner are the depletion regions of the p-n junction. This leads to a shorter tunneling distance and consequently a higher tunneling probability.

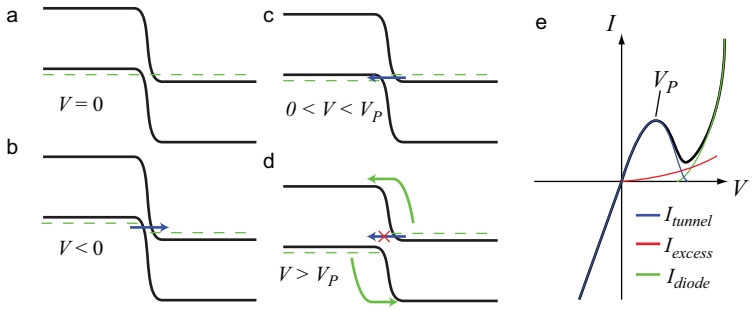

Figure 5.7: *(a-d) Schematic band diagrams of a conventional homojunction TD under various bias conditions. (e) Schematic I-V diagram depicting each of the current components.*

A conventional TD operates as follows: In reverse bias (Figure 5.7b) the p-side valence band and n-side conduction band overlap and electrons can tunnel from the p-side to the n-side, resulting in an increasing negative current with increasing reverse bias. At small forward bias (Figure 5.7c) the bands still overlap and because the Fermi level lies within the valence band on the p-side there are empty states for electrons in the n-side conduction band to tunnel into, resulting in a positive current. At forward biases beyond a particular voltage, V_P, the bands cease to overlap and there are no longer any available states on the p-side for electrons to tunnel into. The current thus decreases, leading to a region of negative differential resistance (NDR). For even larger biases the current starts to increase again, because of thermionic emission across the p-n junction (I_{diode}). This current follows the standard diode current relation $I_{diode} = I_0\,(exp[qV_D/\eta kT] - 1)$, where η is the ideality constant. There may also be a contribution to the current called the **excess current** (I_{excess}), which is due to tunneling through defect-states within the p-n junction.

The NDR behavior has traditionally generated the interest in TDs, since NDR devices are useful for efficiently driving oscillator circuits. The maximum current level before the NDR region is called **peak current**, I_P, and occurs at the **peak voltage**, V_P. The lowest current level within the NDR region is called **valley current**, I_V, occuring at the **valley voltage**, V_V. Useful figure of merits for TDs are I_P and the peak-to-valley current ratio (PVR) defined as PVR$= I_P/I_V$. For homojunction TDs, a common value of the PVR is between 1.5 and 5 at room temperature [103]. The efficiency of a NDR-based oscillator circuit is depending on a steep NDR region, and the PVR should thus be at least larger than two. The output power is proportional to the peak current level of the TD, and thus large values are

beneficial.

5.3.5 Broken-gap TDs

The GaSb/InAsSb heterojunction differs from conventional TDs in that it has a broken type-II band alignment, besides also being a natural p-n junction even without intentional doping. This means carriers in the GaSb valence band can freely tunnel into the InAsSb conduction band without an intermediate tunnel barrier that decreases the tunneling probability. Instead the tunneling probability is determined solely by the coupling between the GaSb light hole band and the InAsSb conduction band.[2] This coupling is rather strong and the tunneling probability has been calculated to be roughly equal to 0.4 [104].

Broken-gap TDs should be able to obtain very high current levels due to the absence of a tunnel barrier. It is less obvious, however, that they can be turned off and exhibit NDR in forward bias. In Figure 5.8a-c, the calculated bandstructure of a GaSb/$InAs_{0.9}Sb_{0.1}$ TD is shown for three different applied biases, assuming that the entire voltage drop occurs at the heterojunction. In Figure 5.8b, when no bias is applied, holes and electrons accumulate on the GaSb and InAsSb side of the heterojunction, respectively. For a reverse biased heterojunction, as in Figure 5.8a (V_D = -0.3 V), there is a preference for electrons to flow from left to right. This flow of electrons consist of valence electrons in GaSb, tunneling into the InAsSb conduction band. The current for negative bias thus increases almost linearly with applied bias, as more states become available for tunneling[3]. This is similar to the operation of a conventional TD.

The behaviour of the junction in forward bias is more complex. At low forward bias the accumulation regions become increasingly stronger and electrons from the InAsSb conduction band tunnel into available states in the GaSb valence band. However, the band bending quickly becomes very large, especially on the InAsSb side where the DOS is low. This leads to confinement of the electron states in the accumulation region, which splits the electron subbands and pushes up them up to higher energies. At some bias voltage the lowest electron subband will obtain higher energy than the highest light hole subband on the GaSb side. At that point there is no longer

[2] The coupling between two bands translates to how well the bands can "communicate" with each other. If the coupling is large, then it is easy for an electron to transfer in between the two bands.

[3] This is a simplification. After flat-band conditions, the added current will come from tunneling through the depletion regions formed at the junction. The current will then actually increase somewhat sublinearly with voltage.

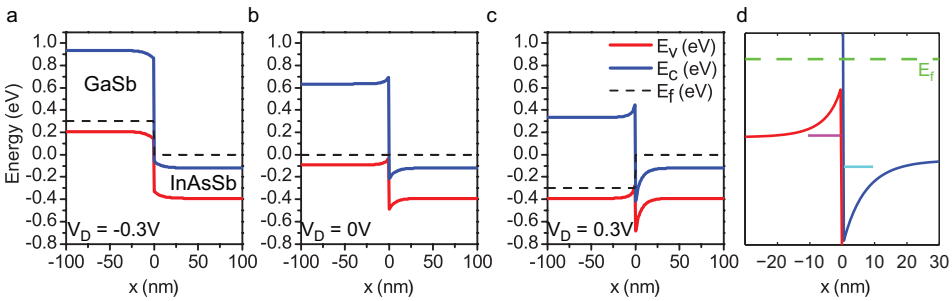

Figure 5.8: *Band diagrams of $GaSb/InAs_{0.9}Sb_{0.1}$ heterojunctions obtained from a psuedo-1D Poisson solution using 2-band $\mathbf{k}\cdot\mathbf{p}$ model to calculate the DOS, for (a) V_D = -0.3 V, (b) V_D = 0 V, and (c) V_D = 0.3 V. (d) Close-up of the accumulation regions (V_D = 0 V) including the position of the lowest subbands on either side of the heterointerface.*

any overlap between the electron states on the two sides of the tunnel junction and, assuming that there is no scattering, the tunnel transport path is closed. Exactly at which applied voltage this happens depends critically on the position of the subband levels. These are not trivial to calculate due to the interaction between the two sides of the heterojunction, leading to a quasi-bound nature of the bound states. However, a first approximation is to assume no interaction at all, resulting in quantum wells with one hard wall and the other side varying as the conduction band potential (See Figure 5.8d). The energy levels can then be calculated using the WKB approximation as described in Section 5.3.3. This approximation underestimates the peak voltage of TDs, since including the band-to-band interaction would reduce the confinement effect and lower the energies of the bound states, thus enabling current transport at higher voltages.

5.3.6 Tunnel current in broken-gap TDs

To fully understand the current transport, one important task is to calculate the expected current of electrons tunneling through the GaSb/InAsSb heterojunction for a specific bias. This can be accomplished by assuming that all voltage drop occurs in the tunnel junction and express the tunnel current density using the standard integration:

$$J = q \int_{E_c^{InAsSb}}^{E_v^{GaSb}} \left[f_l(E, E_{f,l}) - f_r(E, E_{f,r}) \right] v(E) \mathrm{DOS}_j(E) T(E) dE, \qquad (5.7)$$

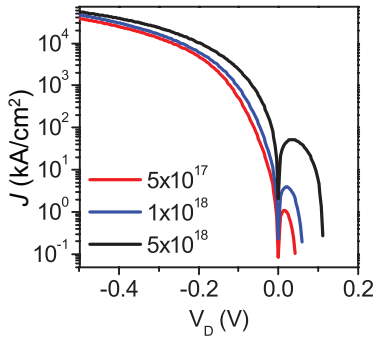

Figure 5.9: *Calculated J-V characteristics of a GaSb/InAsSb TD for three different doping levels in the GaSb segment and* $N_D^{InAsSb} = 1 \times 10^{18}$ cm^{-3}.

where $f_i(E, E_{f,i})$ is the carrier distribution in region i, $v(E)$ is the velocity dispersion of the carriers, and $\mathrm{DOS}_j(E)$ is a joint DOS between the two sides of the heterojunction, which can be defined as $\mathrm{DOS}_j(E) = \sqrt{\mathrm{DOS}_{GaSb}(E)\mathrm{DOS}_{InAsSb}(E)}$ [101]. The transmission probability, $T(E)$, depends on the size of the tunneling barrier and also the coupling between the two bands. If there are depletion regions, such as in a reverse biased junction (Figure 5.8c), $T(E)$ is determined via the WKB approximation as described in Section 5.3.2. The integration limits are the band edges, either just at the interface[4] (in forward bias) or further away (reverse bias). The result of this integration for various GaSb doping levels can be seen in Figure 5.9. It is clear that doping has only a limited effect on the current level at high reverse bias ($V_D < -0.2$ V), but a very large effect on the current in forward bias, where a higher doping level results in a higher peak current level. This analysis does not, however, include the effect of series resistance in the GaSb segment, which in real systems may often limit the current in reverse bias. Series resistance is of course significantly affected by the GaSb doping level.

A further limitation with this model is the neglect of charge rearrangement due to drift-diffusion currents. Thus the model implicitly assumes that the current levels are small enough as to not significantly alter the charge distribution from its equilibrium value. Additionally, Eq. 5.7 does not take carrier scattering into account. Both phonon and impurity scattering can lead to a reduced abruptness in the filtering of the Fermi distribution and consequently a less effective blockage of the tunneling current in forward bias. The results here should thus be considered an ideal case, but can still

[4]Then defined by the lowest confined subband energy.

be useful for understanding the device operation. A more comprehensive model would self-consistently solve Poisson's equation, the continuity relations and drift-diffusion equations on a finite element grid of the device, and may include the tunnel current as a boundary condition.

5.4 Measurement of GaSb/InAsSb TDs

In Paper IX, single-nanowire GaSb/InAsSb TD devices were fabricated and measured. The measured nanowires were annealed using the process described in Section 5.2 so that the connection between the InAsSb shell and InAsSb axial segment was removed. A measured I-V sweep of a typical device is presented in Figure 5.10a. As predicted in Section 5.3, the I-V has a characteristic NDR region at small forward bias and high negative current levels in reverse bias. For forward bias larger than 100 mV, thermionic hole transport gives rise to an exponential increase in the current level. For the device in Figure 5.10a, V_P = 0.11 V, I_P= 840 nA and PVR = 2.1. The best measured PVR for any device in Paper IX was 3.5. By assuming a neck diameter of 40 nm the peak current density was estimated to 67 kA/cm^2. This value roughly 120 times higher than for the best reported nanowire TDs at this time [105**?**]. Furthermore, the current density level at V_D= -0.5 V is 1750 kA/cm^2, similar to the highest reported number for MBE-grown InGaAs TDs (2000 kA/cm^2) [106].

The temperature dependence of a similar device is displayed in Figure 5.10b. Tunneling is not a temperature-activated process, and as such the temperature-dependence should be weak in a pure tunneling device[5]. Indeed, the measured current level for most biases is only weakly dependent on temperature in the range from 4 K to room temperature. Only the current at large forward bias has a strong temperature dependence, which verifies that this originates in thermionic excitation across the valence band barrier in the InAsSb.

5.4.1 Charging of trap states

An interesting observation is that the chosen biasing range has a significant impact on the measured peak current level, as is highlighted in Figure 5.11a. A larger bias range (up to 0.8 V) results in larger tunnel current, in both forward and reverse bias. This can be explained by the presence of trap states near the tunnel junction, which are charged as the device is forward

[5]A small variation with temperature may be observed due to the temperature-dependent band-offsets of the heterostructure.

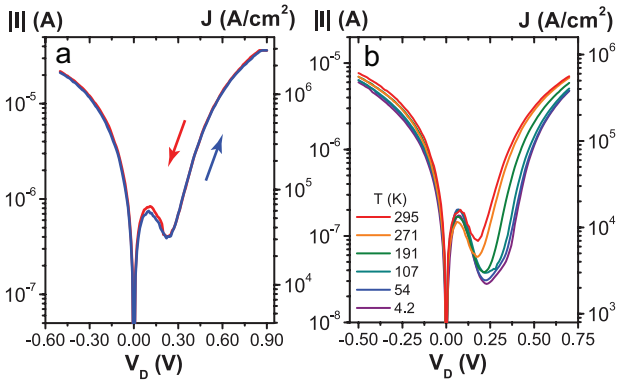

Figure 5.10: *(a) /I/-V characteristics of a processed GaSb/InAsSb single nanowire TD at room temperature. The two scans represent forward and reverse sweep directions. A clear NDR region is visible in forward bias. (b) Temperature dependence of the /I/-V characteristics of another similar device. Note the very weak temperature dependence in reverse and small forward bias, indicating a pure tunneling current mechanism.*

biased. The effect of such local charges can be to cause band bending, which may increase the effective band overlap between the two sides of the junction. An example of this depicted in Figure 5.11b, where a charge of $-50e$ is inserted 5 nm from the heterojunction on the GaSb side. These charges causes an upward-bending of the bands, resulting in less efficient hole confinement near the junction and consequently an increased band overlap.

Since the lifetime of the "charge" effect on the measurements is on the order of minutes, it is highly unlikely that the trapped charges reside within the crystal, as the normal bulk recombination process (Shockley-Read-Hall) typically has a lifetime in the nanosecond range [107]. It is more probable that the charged states are surface defects, possibly in the exposed GaSb neck close to the junction. This hypothesis is strengthened by the fact that further processing of the nanowires by depositing a dielectric (HfO_2) and gate metal considerably reduces this charge effect in many devices.

5.4.2 Performance limits

It is concluded in Paper IX, by fitting the simulation modified with a series resistance, R_s, to measured data, that the TDs are completely limited by series resistance. From measurements on GaSb segments only it was concluded that most series resistance originates from the GaSb seg-

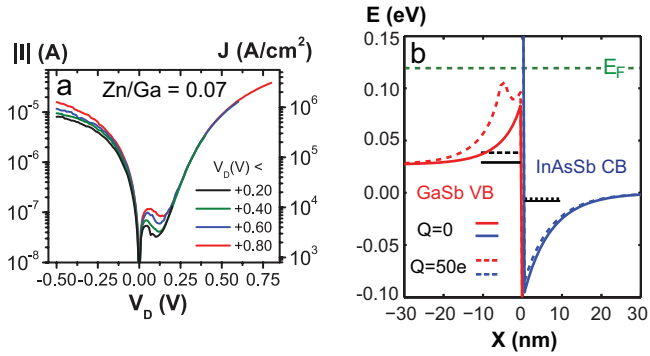

Figure 5.11: *(a) /I/-V sweeps on a single NW TD with various V_D magnitudes. (b) Simulation of the GaSb-InAsSb interface with and without an extra negative 50e charge inserted 5 nm from the interface on the GaSb side. The black lines indicate the energy of the lowest sub-band in the wells. The extra charge broadens the GaSb well (dashed) and lifts up the light-hole sub-band.*

ment. An excellent fit in reverse bias was obtained when using $R_s = 10$ kΩ, $N_A(GaSb) = 2 \times 10^{18}$ cm^{-3}, and $N_D(InAsSb) = 1 \times 10^{18}$ cm^{-3}. It should thus be possible to further improve the performance of the GaSb/InAsSb TDs by increasing the doping levels of the GaSb segment. This has the additional benefit of increasing the peak current level in forward bias.

The PVRs of these devices are typically higher than two or even three, which are decent values. However, the PVR here is mainly an effect of a very high peak current, meaning that the valley current is also high compared to conventional TDs. The origin of this current may be defects in the heterojunction, but likely a large contributor is the narrow band gap of the InAsSb which allows for holes on the GaSb side leak through into the InAsSb valence band. This may be improved by reducing the Sb content further in the InAsSb segment.

5.5 Performance of GaSb/InAsSb TFETs

A conventional homojunction TFET consists of a gated p-i-n TD, where the p- and n-regions are degenerately doped, and the gate is located in the intrinsic region. The interband tunnel current between the p-type source into the intrinsic channel is controlled by modulating the band bending in the intrinsic region with the gate potential. Since the Fermi distribution of the electrons injected into the channel are thermally filtered by the tunnel

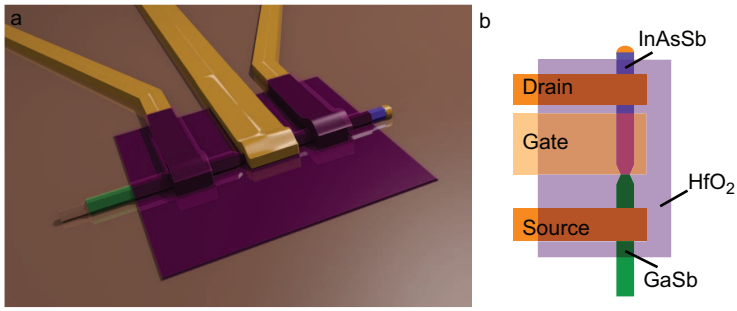

Figure 5.12: *(a-b) Schematic illustrations of a GaSb/InAsSb n-type TFET device. The source-drain contacts are processed first, followed by the gate dielectric and finally the gate contact positioned on the InAsSb segment aligned to the heterojunction.*

junction it is possible for the subthreshold swing to be smaller than roughly 60 mV/dec ($\ln(10) \times kT/q$ at room temperature). Ideally one would expect a subthreshold swing limited by the sharpness of the DOS at the heterojunction [108]. The on-current level, however, is typically limited by a low tunneling probability similar to the peak current in homojunction TDs.

The GaSb/InAsSb TDs presented in the previous section may be processed into complete TFET devices by including gate dielectric and gate metal definition steps after the initial contact processing. Because of the core-shell structure of the GaSb-segment (with an InAsSb shell) the most straight-forward transistor devices are those in which the gate is positioned on the n-type InAsSb segment. A schematic of a typical finished device is displayed in Figure 5.12. The high current levels and decent PVR of the GaSb/InAsSb TDs demonstrate the potential of this structure for achieving TFETs with high current levels.

The purpose of this section is to discuss the expected performance of GaSb/InAsSb TFETs. To accomodate our TD model to TFET devices, the gate-induced semiconductor charge is modeled as being equal to the charge on the gate electrode, and uniformly distributed throughout a circular nanowire cross-section. In other words it is assumed that the gate-induced band bending is constant throughout the whole nanowire cross-section. The amount of band bending for a specific gate voltage is then calculated by relating the induced charge to the DOS in the semiconductor.

5.5.1 Biasing the TFET

An important consideration is how to bias the GaSb/InAsSb TFET devices. Figure 5.13a and b presents the band diagrams obtained from the Poisson equation for a GaSb/$InAs_{1-x}Sb_x$ TFET with $N_A = 1 \times 10^{19}$ cm^{-3}, $N_D = 5 \times 10^{17}$ cm^{-3} and $x = 0.1$. These diagram should be fairly accurate when the transistor is in the off-state, but may deviate considerably in the on-state due to the neglected drift-diffusion currents. A 5-nm-thick HfO_2 oxide and 20 nm nanowire radius was assumed, with flat bands at $V_G = 0$ V. Depending on how the device is biased the voltage drop will occur in different places. In Figure 5.13a, a bias of -0.3 V is applied on the GaSb source electrode ($V_S = -0.3$ V), thus lifting up this side relative to the whole InAsSb side. These are the same biasing conditions as was used for the TDs, and results in the same band structure. To turn the device off, the InAsSb side thus needs to be raised by more than $V_S + V_P$, where V_P is the peak voltage of the TD. In this bias configuration it will thus be more difficult to turn the device off the larger V_S is. By applying the equivalent bias on the InAsSb drain electrode instead ($V_D = 0.3$ V) as in Figure 5.13b, the voltage drop will instead occur mostly at the gate/drain interface in the InAsSb. The channel region now only needs to be raised by roughly V_P, thus requiring a much smaller applied gate voltage to turn off the tunnel current. Sub-60 mV/dec subthreshold swing may be possible even in this bias configuration because the carriers are still supplied through the tunnel junction.

The small bandgap of InAsSb may ultimately limit the off-current level achievable in GaSb/InAsSb TFETs. The reason for this is that InAsSb may be inverted as the devices are turned off, leading to a thermally activated hole leakage current into the GaSb source (Figure 5.13c-e). The higher the Sb content is in the InAsSb, the more severe this problem becomes ($0 < x < 0.5$), because the valence band offset in the heterostructure quickly decreases while the conduction band offset almost does not change at all (See Figure 3.1). It may thus be important to minimize the Sb content to obtain optimal off-state performance.

5.5.2 Gate alignment

There are three possible ways in which the gate can be aligned to the GaSb/InAsSb tunnel junction. The gate can be underlapping, meaning that the gate is located completely on the InAsSb and somewhat away from the interface. This may lead to weak gate modulation at the heterojunction, or in the worst case in an ordinary InAsSb MOSFET in series with the

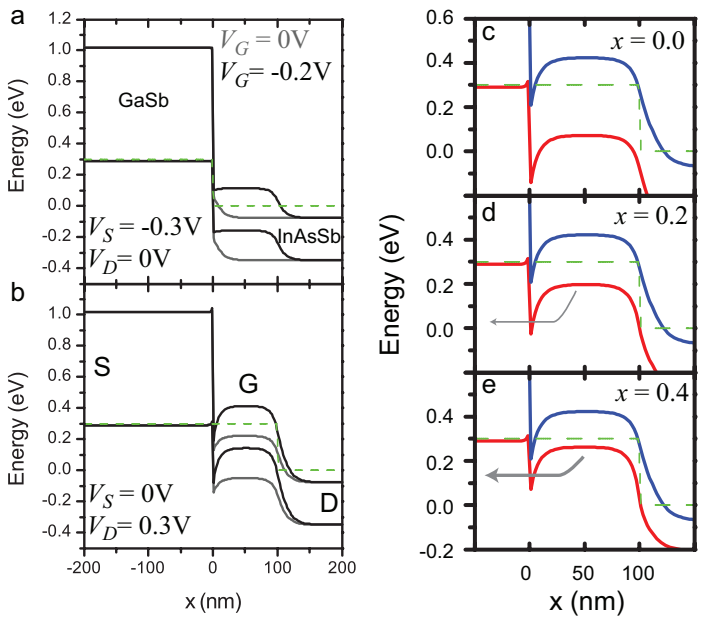

Figure 5.13: *Approximate band diagrams of GaSb/InAsSb TFETs which do not take into account carrier redristribution due to currents in the structure. Comparison of the resulting band diagram when applying an equivalent bias ($|V_{S/D}| = 0.3$ V) to the (a) GaSb source or (b) InAsSb drain contact, respectively. Panels c-d show the effect of an increased hole leakage current due to inversion for increased Sb content in the InAsSb.*

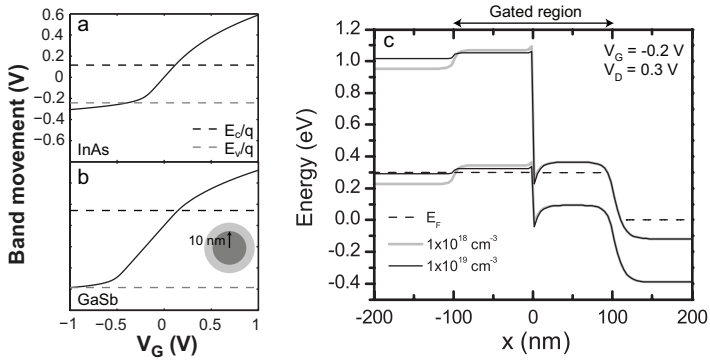

Figure 5.14: *Calculated band movement with applied gate voltage for a 20 nm-diameter (a) InAs and (b) GaSb nanowire, respectively. The gate dielectric is assumed to be 5 nm thick HfO_2 ($\varepsilon_r = 25$). (c) $GaSb/InAs_{0.9}Sb_{0.1}$ band movement with overlapping gate for two distinct p-doping levels in the GaSb source ($N_A = 1\times10^{18}$ and 1×10^{19} cm^{-3}) and n-doped InAsSb channel ($N_D = 1\times10^{18}$ cm^{-3}).*

tunnel junction. However, if the transport inbetween the tunnel junction and the MOSFET is ballistic, sub-60-mV/dec SS may still be accomplished [109].

The gate can also be overlapping the GaSb source region, in which case one would have band modulation on both sides of the heterojunction. In principal this should make it difficult to turn off the tunnel current. However, the band bending in the two different materials may be very different due to the large difference in the DOS between the GaSb valence bands ($N_V = 1.8\times10^{19}$ cm^{-3}) and $InAs_{1-x}Sb_x$ conduction band ($N_C = 6.8\times10^{16}$ cm^{-3}, for $x = 0.1$). Figure 5.14a and b display the calculated band bending for these two materials as a function of applied gate voltage, V_G. Figure 5.14c shows the corresponding band structure with an overlapping gate and V_G = 0 and -0.3 V, respectively. It is clear that as long as the GaSb is sufficiently doped so that the Fermi level is below the valence band edge, the detrimental effect of an overlapping gate is negligible.

The third and obvious gate alignment is to have the gate perfectly aligned to the heterojunction, in which case gate modulation would occur predominately on the InAsSb side of the junction. Although this seems to be the obvious best choice, the practical difficulty to achieve perfect alignment may result in large device-to-device variations. It may thus actually be preferable to instead choose to intentionally "misalign" the gate with respect to the heterojunction. At this point it is however still an open

question which alignment will be the best.

5.5.3 The gate dielectric

The single most critical issue with III-V MOSFETs in general is the poor quality of the interface between the III-Vs and the gate-dielectric. This is of course equally important for a III-V TFET device. A high concentration of interface charges, D_{it}, and traps within the dielectric film lead to large hysteresis in the device transfer characteristics (I_D/V_G) and a reduced effect of the gate on the channel potential. HfO_2 is a high-κ dielectric which is nowadays used commercially for Si CMOS. On InAs however, the D_{it} values are on the order of 10^{13} cm^{-2}, at least a factor of ten too high for practical applications. Improvements in D_{it} values have been achieved by using an AlO_x inter-layer below the HfO_2 [110], which react with and reduces the native oxides [111]. The chemical composition of various crystallographic surfaces also differ, and it is possible that the charge neutral {110} facets of the GaSb/InAsSb nanowires presented here may exhibit lower D_{it} compared to other facets. This is yet to be verified, however.

5.5.4 Preliminary measurements

Here some preliminary electrical measurement data on GaSb/InAsSb TFET devices is presented. These devices have a 10-nm-thick HfO_2 gate dielectric, and a gate contact located on the InAsSb side of the heterojunction. The gate length was roughly 300 nm and the diameter of the devices is estimated to be 30 nm. When biasing the devices on the InAsSb side the I-V characteristics exhibit clear current saturation behaviour for positive bias, as expected for a MOS-based device (Figure 5.15a). At negative bias the NDR behavior is clearly seen, and I_P is suppressed by a negative gate potential.

The logarithmic transfer characteristics (Figure 5.15b) reveal that the SS is strongly varying with temperature. Values of the SS have been extracted and are plotted as a function of temperature in Figure 5.15c. The SS of the measured data is also compared to that of an ideal MOSFET, and it is clear that the temperature dependence follows that of a conventional MOSFET, but with higher values probably due to a non-ideal gate-dielectric interface. For a true TFET the SS should be close to constant with varying temperature. Our results may thus indicate that the tunnel junction is in series with a MOSFET device and is only indirectly affected by the gate potential. Alternatively, there might be trap-assisted tunneling across the heterojunction, possibly through mid-gap surface traps [112].

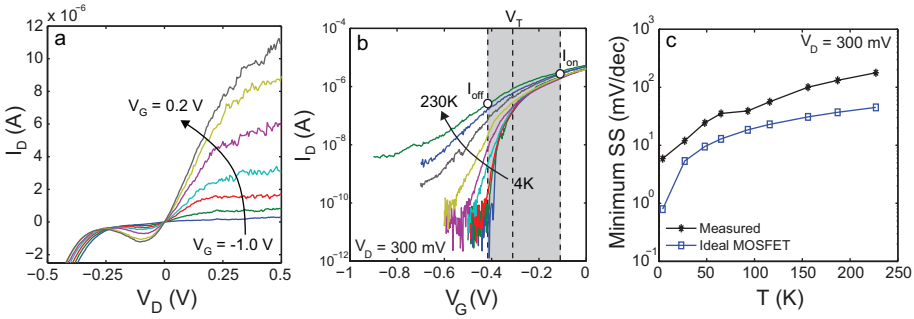

Figure 5.15: *(a) Room temperature I-V for various applied gate bias of a single nanowire TFET device. (b) Temperature dependence of subthreshold characteristics. The operation voltage window around V_T used to evaluate I_{on} and I_{off} at* 230K *is also included in this figure. (c) Temperature variation of the minimum SS for a single device, compared to the SS of an ideal MOSFET device.*

V_T was evaluated by linear extrapolation from the maximum slope in the measured transfer characteristics, and lies between -0.3 V and -0.4 V. The devices are thus clearly operating in depletion mode. In accordance with Ref [113], the operation voltage is defined as $V_{CC} = V_D$, and I_{on} and I_{off} are evaluated at $V_T + \frac{2}{3}V_{CC}$ and $V_T - \frac{1}{3}V_{CC}$, respectively (Figure 5.15b). This results in $I_{on} = 20$ mA/mm which is constant with changing temperature. The current thus appears to be limited by the tunnel junction in the on-state. The I_{on} value is similar to planar InGaAs TFETs [112] and Si nanowire TFETs [114], despite the fact that our devices operates at much lower voltage (0.3 V compared to 0.75 and 1.2 V, respectively). This highlights the benefit of having a broken-gap heterostructure in our case. However, due to the temperature dependent SS, I_{off} varies very much with temperature. This results in I_{on}/I_{off} as high as 10^5 below 100K, but only roughly equal to 10 at higher temperature.

Some devices also exhibit a current component in the off-state which appears to have a weak p-type gate dependence. The origin of this current could be inversion of the InAsSb channel which causes hole injection into the GaSb source segment as illustrated in Figure 5.13e. It is also possible that trap- or phonon-assisted tunneling could contribute to the off-current [112]. To obtain low off-currents it may thus be critical to have a larger bandgap in the InAsSb.

Chapter 6

Conclusions

Nanowire heterostructures in general, and III-Sb heterostructure nanowires in particular are generating an increased amount of attention, due to their many promising applications in high-speed electronics and optoelectronics. The results of this work have led to an significantly increased understanding of antimonide nanowires, in terms of the growth chemistry, their physical properties and the feasibility of Sb-based nanowire electronic devices.

The Sb-based nanowires all exhibit an extraordinary high crystal quality without stacking faults or twin defects, which are commonly observed in other material systems. The side facets are smooth and charge-neutral {110} facets, and should thus be suitable for device integration. The single most important denominator in Sb-based nanowire growth is the low vapour pressure of Sb, which makes it important to carefully control the V/III during growth, and leads to very severe memory effects.

The Sb-based nanowires are characterized by a high group-III content in the Au seed particle, resulting in a reduced effective V/III ratio for the nanowire growth as compared to the parasitic planar growth. It also complicates the switching of the group-III atom in heterostructures, but is beneficial for acquiring an abrupt Ga-to-In heterojunction in GaSb/InAs nanowires, because the Ga is given time to be completely depleted from the particle before InAs growth commences.

Finally, Sb-based nanowires have difficulties to nucleate directly on a substrate, and normally require a nanowire stem for proper nucleation. This is believed to be related to the surfactant properties of the Sb atom, but further investigation is needed for a full understanding of this issue.

The second part of the thesis considers the application of GaSb/InAsSb heterojunctions for tunnel device applications, as a demonstration of the novel device concepts which are made possible in antimonide heterostructure

nanowires. Here, the broken band alignment of GaSb and InAsSb is utilized to create TDs with very high current levels. A novel method of selectively decreasing the diameter of the GaSb/InAsSb junction is also demonstrated. Finally, the performance and potential limits of GaSb/InAsSb TFETs is discussed with respect to the band structure and performance of the TDs.

6.1 Outlook

During the course of this thesis work, the field of antimonide nanowires has progressed from being in its infancy to becoming an established material system in research. Although there are obviously many details about the growth mechanism that are still not fully understood, it is clear that many research groups are now focusing more on the application of antimonide nanowires, rather than fundamental growth studies. Most research is at this point devoted to InSb nanowires, mostly because of its fascinating low-temperature transport physics [24, 115]. InSb nanowires are, however, also investigated for photodetectors and FETs [97, 116]. A promising future application for InSb is in thermoelectrics, since it has been predicted that InSb nanowires may provide a material with an extremely high thermoelectric figure-of-merit [117].

GaSb nanowires may also spur an even larger interest in the coming years, as GaSb (together with Ge) is now seriously considered as the p-type channel material in future CMOS [5]. Also, GaSb may be used as an electron barrier in photovoltaic InAsSb nanowire photodetectors in the long wave-length region.

The ternary GaAsSb and InAsSb nanowire materials will likely be studied more and more intensely in the coming years. As noted above, InAsSb is of interest for long-wavelength optoelectronic devices, for emission of detection of wavelengths up to 12 µm. With low Sb content InAsSb is also attractive for high speed electronic applications due to its high-quality ZB crystal structure and smooth and neutral side facets, which may improve integration with high-κ dielectrics.

The GaSb/InAsSb nanowire tunnel devices are very promising for real device applications. Although there are some caveats, such as a high off-state leakage current, these structures constitute a viable architecture for realization of TFET devices with performance that may eventually overcome that of Si CMOS. To reach that goal the off-state currents need to be decreased, possibly through the insertion of a very thin tunnel barrier, and the interface to the gate dielectric need to be optimized.

For antimonide devices to be viable for mainstream production it is im-

portant to integrate them onto a Si substrate, to reduce the manufacturing cost. The use of Au particles may be problematic, since Au impurities result in mid-gap defect-states in Si and III-V semiconductors. At this point, such defects have not been observed in III-V nanowires, and it is possible that the Au seed particles on III-V nanowires remain stable. Even so, Au-free antimonide nanowire heterostructures will probably be an important field of study in the next few years, similar to what where research on Si nanowires i heading [118, 119]. Although both Au-free GaAsSb and InSb nanowires have already been demonstrated [77, 81, 91, 120] much more work is needed to obtain a higher degree of control of the nanowire morphology and crystal structure.

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