Digitally Assisted Adaptive Non-Linearity Suppression Scheme for RF front ends

Gangarajaiah, Rakesh; Abdulaziz, Mohammed; Liu, Liang; Sjöland, Henrik

Published in:
2014 IEEE 25th Annual International Symposium on Personal, Indoor, and Mobile Radio Communication (PIMRC)

DOI:
10.1109/PIMRC.2014.7136240

2015

Digitally Assisted Adaptive Non-Linearity Suppression Scheme for RF front ends

Rakesh Gangarajaiah, Mohammed Abdulaziz, Liang Liu and Henrik Sjöland Department of Electrical and Information Technology, Lund University, Sweden
Email: {Rakesh.Gangarajaiah,Mohammed.Abdulaziz,Liang.Liu,Henrik.Sjoland}@eit.lth.se

***Abstract*—This paper presents a robust and low-complexity non-linearity suppression scheme for radio frequency (RF) transceiver building blocks to efficiently mitigate intermodulation distortion. The scheme consists of tunable RF components assisted by an auxiliary path equipped with an adaptive digital signal processing algorithm to provide the tuning control. This proposed concept of digitally-assisted tuning is capable of handling a large range of non-linear behaviours without any complexity increase in the expensive RF circuitry and is robust to process, voltage and temperature variations. A case study on the third order intermodulation of the channel select filter for a full 10 MHz Long Term Evolution (LTE) reception bandwidth is used to demonstrate the feasibility and effectiveness of the technique.**

***Index Terms*—Adaptive signal processing, Interference cancellation, Intermodulation distortion, Nonlinear circuits.**

I. Introduction

The dramatic increase of wireless connections within limited spectrum has forced many radio devices to operate close in frequency. This poses very stringent requirements for building blocks like the low noise amplifier (LNA), mixer and channel select filter (CSF) in a wireless transceiver, where high linearity is needed to avoid the intermodulation distortion and the resulting interference between devices operating in close proximity. However, implementing such high-linearity building blocks is very expensive in terms of power consumption. Moreover, the constantly reduced feature size of complementary metal oxide semiconductor (CMOS) technology leads to reduced oxide thickness and lower supply voltages, making the non-linearity an even more critical issue. There is thus, an urgent demand for a robust and cost-efficient scheme to tackle the non-linearity in radio frequency (RF) circuits and reduce the interference in wireless reception.

Several techniques have been reported in literature addressing the intermodulation interference problem. One way of achieving high linearity is to implement tunable RF components and optimize the tuning so that the non-linearities cancel at the source [1]–[6]. For example, the authors in [1] used multiple transistors for linearization of a main transistor by controlling parameters such as gate width and over drive voltage. Unfortunately, the optimal tuning point of the analog circuit shifts significantly depending on process, voltage and temperature (PVT) variations, requiring frequent and inconvenient re-tuning to provide high linearity. Recently, the concept of using an auxiliary path to recreate and cancel non-linearities has been proposed to increase the robustness. An adaptive interference cancellation technique operating in the analog domain was introduced in [7]. This method requires additional power hungry analog building blocks which are themselves subject to non-linearities and PVT variations. In [8], [9], intermodulation generation is performed in the analog domain and powerful digital signal processing is employed to provide robust intermodulation cancellation. A drawback is that the alternate paths need to operate continuously leading to increased power consumption.

To address the aforementioned problems in existing non-linearity suppression techniques, we propose to exploit the advantages of both tunable RF components and adaptive digital signal processing. More specifically, we make RF components tunable to provide non-linearity suppression by eliminating this imperfection at its source. Furthermore, a digital auxiliary path is introduced, implementing adaptive signal processing algorithms for detecting errors in the tuning point of the RF components and performing the corresponding adjustments. This digitally-assisted adjustment scheme provides robustness to PVT variations. Furthermore, unlike the approach in [8], [9], this method does not need to operate continuously and can thus be powered down when the optimal operating point has been reached, leading to significant power savings. To verify the effectiveness of the proposed method, we designed a CSF for a Long Term Evolution (LTE) receiver with 10 MHz baseband bandwidth, where a bias voltage could be tuned to mitigate the third order non-linearities. Fixed-point simulation results demonstrate that the proposed method can use a low resolution analog to digital converter (ADC) and a very low complexity adaptive algorithm in the auxiliary path. Furthermore, the auxiliary path design is fast enough to tune the CSF once every Orthogonal Frequency Division Multiplexing (OFDM) symbol, achieving tuning to optimal linearity within a time period of a few OFDM symbols.

II. Background

A typical LTE Frequency Division Duplexing (FDD) receiver is shown in Fig. 1, where the duplexer is used to separate the transmit (Tx) and receive (Rx) bands. A non-ideal duplexer results in Tx power leakage into the Rx, which is typically the strongest source of interference in FDD receivers. The figure also shows an external interferer which can be from another device such as a nearby cellular phone.

The LNA and mixer are used to amplify and down convert the received signal into baseband, and a CSF is then employed

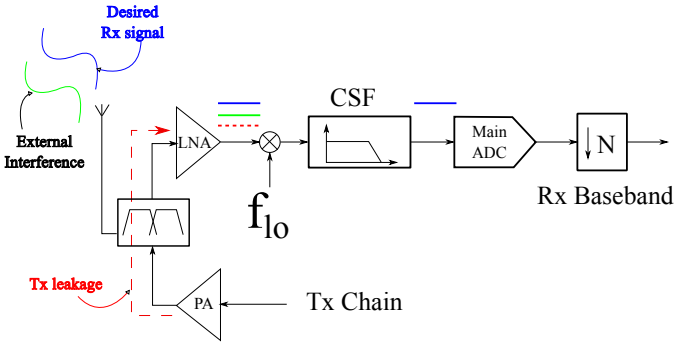
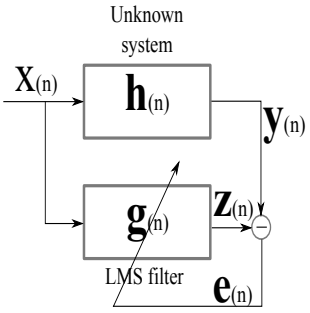


Fig. 1: Typical LTE-A receiver



(a) Block diagram

$\mathbf{g} \leftarrow \mathbf{0}$
for n=1 to ∞ **do**
  $y(n) \leftarrow \mathbf{h} * \mathbf{x}$
  $z(n) \leftarrow \mathbf{g} * \mathbf{x}$
  $e(n) \leftarrow z(n) - y(n)$
  $\mathbf{c(n)} \leftarrow \frac{\mu e^*(n)\mathbf{x}}{\mathbf{x^*x}}$
  $\mathbf{g(n+1)} \leftarrow \mathbf{g(n)} + \mathbf{c(n)}$
end for

(b) Normalized LMS algorithm

Fig. 2: LMS system with algorithm

to suppress the Tx leakage and the external interference. An ideal analog front end is linear, and should, except for the frequency translation performed by the mixer, not output any signals at frequencies not present in its input. Non-linear systems, however, produce harmonics of the input signal as well. For example, if the input signal is a sinusoid with frequency f_1, then the output will have components not only at f_1, but also at $2f_1, 3f_1, 4f_1$, etc. If the input signal has rich frequency content, non-linearities will also cause intermodulation (IM). For example, if an input signal consists of two sinusoids with different frequencies f_1 and f_2, then it can be shown that second and third order IM terms will be produced at [10]:

$$f_1 - f_2,\ f_1 + f_2,\ 2f_1 - f_2,\ 2f_1 + f_2,\ 2f_2 - f_1,\ 2f_2 + f_1$$

Some of the intermodulation terms may appear at frequencies that fall inband and contaminate the signal. The CSF is typically a bottleneck for receiver linearity, and elimination of its IM distortion would thus improve the receiver performance significantly.

Several authors have proposed different solutions for reducing inband IM to enhance Rx signal fidelity. Since the Tx leakage is often the main source of interference, previous works such as [11] have used digital cancellation techniques, where the path delay of the IM due to Tx leakage is estimated and compensated for, in the digital baseband. This method will not be able to cancel IM created due to external interferers and hence is not suitable for scenarios with strong external signals.

The author in [9] utilizes auxiliary paths to generate 3^{rd} and 5^{th} order IM by using an analog cubic term generator to avoid using a high resolution wideband ADC, which would consume more power than the original circuits. Digital adaptive algorithms are then used to synchronize the auxiliary path with the main path and cancel the IM terms in the main path by using digital subtraction. This approach requires the auxiliary paths to operate continuously for IM cancellation and is aimed at non-tunable analog components.

The use of adaptive filters [12], in particular the least mean squares (LMS) algorithm, is very common in interference cancellation techniques utilizing an auxiliary path. The LMS algorithm tunes the adaptive filter coefficients by observing the error between the estimated and the actual signal with the goal of minimizing the mean square error. The decision on tuning the filter coefficients is solely based on the error at the current time, and the rate of the filter update is configurable providing a trade off between convergence time and the variance of the error. Fig. 2a shows a system employing an LMS filter to predict the output signal $y(n)$ and Fig. 2b details the operation of the normalized LMS algorithm. The error signal $e(n)$ between the predicted output $z(n)$ and the actual output $y(n)$ is used as a parameter to tune the update vector $\mathbf{c}(n)$. One of the main advantages of the normalized LMS algorithm is its capability to handle a wider amplitude range of the input $x(n)$ enabling a stable implementation even without complete knowledge of the input signal statistics.

III. Digitally Assisted Non-Linearity Canceller

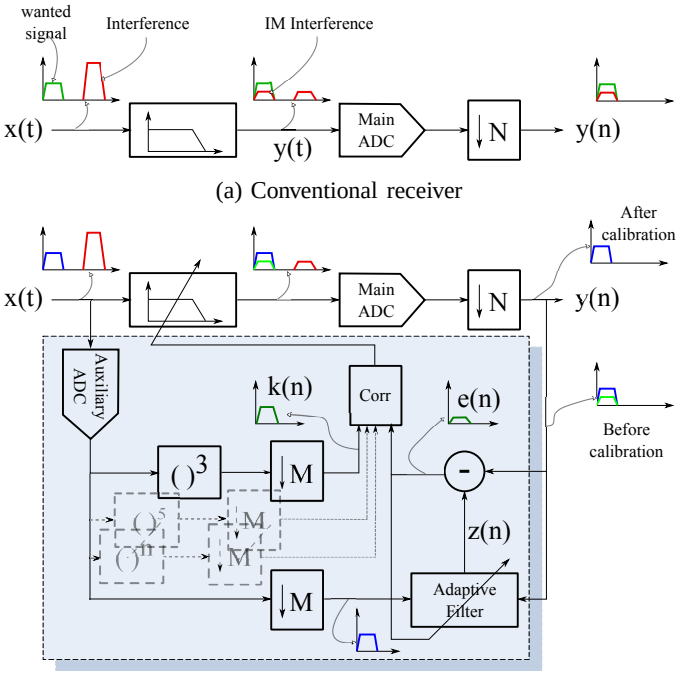
Some analog circuits can be linearized by tuning the operating point so that the non-linearities cancel. The proposed solution is aimed at such circuits and uses a digital adaptive algorithm to provide the required IM detection enabling on chip adaptive tuning of the bias to reach linearity. To the best of our knowledge, a complete solution for digitally assisted linearization has not yet been published.

The analog baseband (one of the I and Q channels) of a direct-conversion LTE receiver with a CSF is depicted in Fig. 3a. The received signal $x(t)$, obtained by down converting the RF signal is passed through the CSF to suppress out of channel interference before the analog to digital conversion. Fig. 3a also shows the frequency spectrum with the desired signal and a strong out of band interferer from the Tx operating in FDD. IM due to non-linearities falls in channel, corrupting the Rx signal. The CSF attenuates the Tx interferer, and further filtering in the main ADC and the decimator removes any remaining out of band Tx interference. The in channel IM interference, however, is unaffected and is passed onto the digital baseband.

The operation of an ideal linear CSF used for LTE channel selection can be modelled as

$$y(t) = \mathbf{h} * x(t), \tag{1}$$

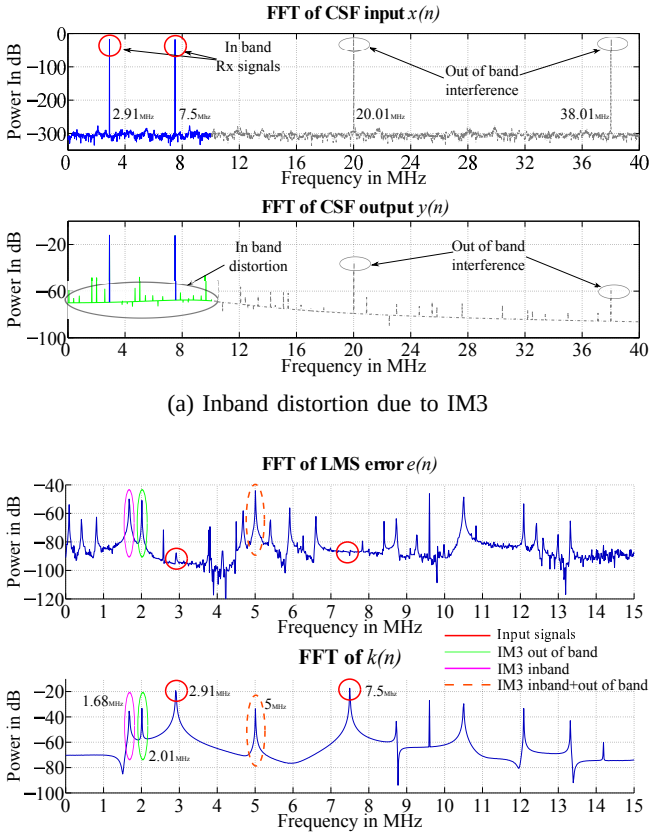
where $y(t)$ is the output, produced by the convolution of $\mathbf{h}$, the filter impulse response, and the input $x(t)$. Third order non-



(a) Conventional receiver

(b) Proposed non-linearity suppression receiver with tunable CSF non-linearities (α, β, γ)

Fig. 3: Receiver implementation with CSF



(a) Inband distortion due to IM3

(b) LMS error and non linear input

Fig. 4: FFT of CSF input, output and LMS error signals

linearities in the CSF produce distortion in the output signal $y(t)$, which can be modelled in Matlab using

$$y(t) = \mathbf{h} * x(t) + (\alpha \mathbf{h}_1 + \beta \mathbf{h}_2 + \gamma \mathbf{h}_3) * (x(t))^3 , \quad (2)$$

where $y(t)$ is the filtered output, $\mathbf{h}$ the linear component of the impulse response, and $(\alpha \mathbf{h}_1 + \beta \mathbf{h}_2 + \gamma \mathbf{h}_3)$ represents the third order non-linearities. A tunable LTE CSF aimed at the full 10 MHz baseband channel, with parameters α, β and γ controlling the amount of distortion introduced is depicted in Fig. 3b. In practice the parameters α, β and γ correspond to tunable bias voltages.

The proposed control structure consists of a wideband auxiliary ADC to capture the interference signals surrounding the Rx signal. Digital multiplication is then used to generate IM distortion and in this paper we focus on the 3^{rd} order. However, this technique can be used on other higher order non-linearities as well. Decimators are then used to reduce the sample rate to match the baseband signal $y(n)$. A finite impulse response (FIR) implementation of the normalized LMS algorithm is utilized to produce $z(n)$, an estimate of the output signal $y(n)$, and the error signal $e(n)$ is used to update the LMS filter coefficients. The LMS adaptive filter is linear and is capable of estimating the linear signal components with a much higher degree of accuracy compared to the non-linear ones. Hence the error $e(n)$ can be used as a measure of the non-linearities in the output $y(n)$. The output $k(n)$ of the digital cubing unit, contains the non-linear components which are used to correlate with $e(n)$ to measure the amount of inband IM present in $y(n)$. The output of the correlator is then used to tune the CSF towards linearity. This process is repeated iteratively until an optimal point is found and later the auxiliary path is powered down.

IV. Simulation Setup

We aim at compensating 10 MHz CSFs for LTE receivers. A sampling rate of 30.72 MHz is used as the baseband operating frequency and a high resolution linear ADC is assumed to operate with an oversampling ratio of 8 in the main path in Fig. 3, corresponding to an output rate of 245.76 M samples/s. The system is modelled using Matlab and the CSF is implemented using a 4^{th} order Butterworth filter to produce the linear component of (1). The non-linearities are generated by filtering the cubed input signal $(x(n))^3$ through three Butterworth filters of different orders to mimic the effect of non-linearities in a multistage analog CSF. Digital decimation filters provided by Matlab were used to perform the different decimation operations. The root mean square (RMS) power of the distortion was controlled by the parameters α, β and γ in (1) to simulate at different distortion levels. OFDM signalling was used for generating the input signal and 2048 subcarriers with 15 KHz spacing were assumed for data transmission [13].

Fig. 4a shows a two tone test performed on the model in Fig. 3b with two subcarriers at 2.91 MHz and 7.5 MHz respectively, and two out of band interference signals at 20.01 MHz and 38.01 MHz. The Fast Fourier Transform (FFT) of the output $y(n)$, affected by third order intermodulation (IM3) distortion with inband IM3 is also shown. The error floor is significantly increased due to the delay introduced in the Matlab model of

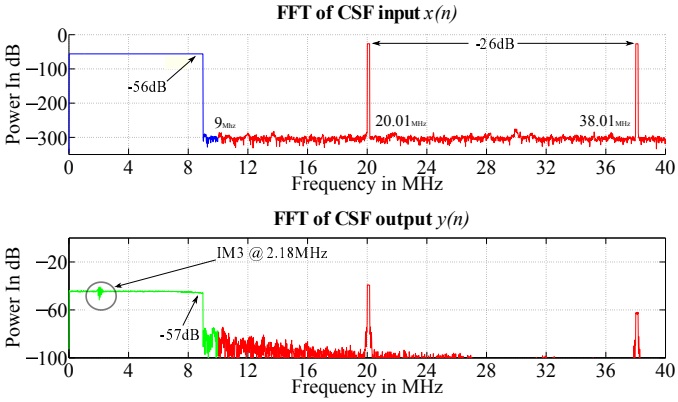


Fig. 5: Input and Output signal spectrum of CSF

the CSF and also due to fact that windowing was not used when performing the FFT, resulting in spectral leakage.

Fig. 4b shows the FFT of the the LMS error $e(n)$ and the signal $k(n)$ produced from the cubing unit in Fig. 3b. It has to be noted that the LMS operates with the baseband operating frequency of $30.72\,\text{MHz}$ corresponding to a full $10\,\text{MHz}$ baseband configuration and hence Fig. 4b depicts bins upto $15.36\,\text{MHz}$. The LMS filter is capable of producing the inband Rx component of $y(n)$ more accurately than the inband IM signals, which can be seen by observing the level of $e(n)$ at the inband subcarrier frequencies of $2.91\,\text{MHz}$ and $7.5\,\text{MHz}$. The power of the IM due to out of channel interferers present at $2 \times 20.01\,\text{MHz} - 38.01\,\text{MHz} = 2.01\,\text{MHz}$ is significantly higher than the error at the inband subcarrier frequencies. Similarly it can be noticed that the errors at $1.68\,\text{MHz}$ due to IM3 of the in channel tones, and at $5\,\text{MHz}$ due to IM3 of in channel and out of channel interferers are significantly higher than the error at in channel subcarrier frequencies. The LMS filter is linear and thus performs a much better estimation of linear components of the signal. Hence the error signal $e(n)$ contains a higher error component at the IM frequencies, and a correlation of signals $e(n)$ and $k(n)$ can be used as a measure of inband IM.

One of the main advantages of the proposed digital control structure is that it needs to be active only over a short period of time to calibrate the CSF, after which it can be turned off resulting in higher power savings compared to the methods proposed in [8] [9].

V. Results

To verify the functionality and feasibility of the proposed technique, fixed point simulations were performed to obtain an estimate of the hardware cost of the proposed technique. A very difficult scenario was considered with a full bandwidth of $10\,\text{MHz}$ for the CSF with strong continuous wave blockers present at $20\,\text{MHz}$ and $38\,\text{MHz}$. Random data was used to generate a series of OFDM symbols which are processed by the CSF and the auxiliary path. Fig. 5 shows the frequency spectrum of the input and output signals of the CSF with two strong interferers and the inband distortion generated due to IM3.

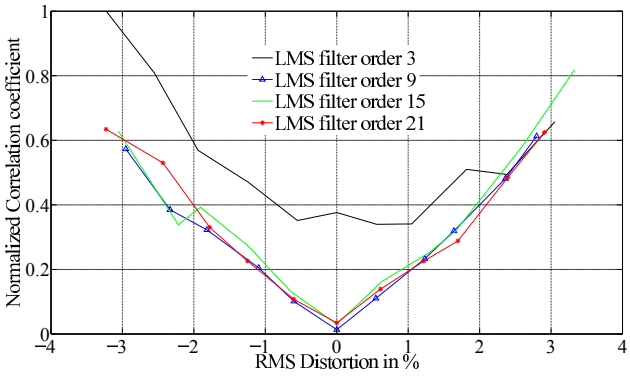
The digital control structure has several parameters such as correlation symbol length, LMS filter length and tap word lengths, downsampling ratio, and precision of the auxiliary ADC. The effects of these parameters were studied by performing simulations with input signals with a frequency spectrum shown in Fig. 5. The RMS power of the distortion was controlled by tuning the parameters α, β and γ of Fig. 3b. A correlation symbol length of 2000 samples was chosen, enabling the digital loop to perform bias adjustments once every OFDM symbol, with a margin of 48 samples left for the LMS convergence. This enables the control structure to tune the CSF to the optimal point within a few OFDM symbols. Shorter LMS filter lengths are favourable as it provides faster convergence and also results in fewer hardware multipliers. Fig. 6a depicts the effect of changing the LMS filter length on the correlation obtained for different levels of distortion. The distortion is measured by a ratio of RMS powers of the inband distortion to the desired Rx signal, with negative distortion levels indicating IM which has a $180°$ phase shift with respect to the Rx signal. It is seen that a minimum correlation is obtained when the RMS power of distortion is minimum and hence the correlation can be used as a measure of in channel IM. Furthermore, filter lengths as low as 9 can be chosen to detect very low levels of IM. The LMS coefficients were also analyzed and a width of 10 bits was chosen.

A wideband auxiliary ADC is required to capture Tx interference signals and blockers which are far away from the Rx signal. The hardware cost of implementing a high precision wideband ADC is significant, and the power consumption of such an ADC would make the digital LMS loop an inefficient approach compared to the ones proposed in [9]. Simulations were thus performed to obtain the minimum required resolution for the auxiliary ADC, and Fig. 6b shows the correlation coefficient obtained for different resolutions. A precision of 6 bits was chosen as it enables correct detection of the distortion in the inband Rx signal even at low distortion levels. Several implementations of low power ADCs have been presented in [14]–[17], and such an implementation can be utilized in the auxiliary path. It has to be noted that some of these implementations target a very large bandwidth, and the power consumption can be further reduced by implementing lower bandwidth ADCs. Furthermore, the proposed auxiliary path will need to run only when the re-tuning of the analog part is required.

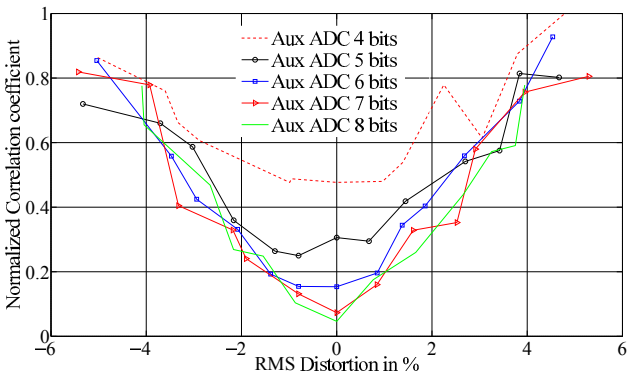
Table I provides details of precision required for the signals in the auxiliary path to be able to effectively detect and tune an LTE CSF. These parameters are obtained by performing a similar analysis as the one used to obtain the LMS filter length and auxiliary ADC width. A higher precision multiplier is needed for the correlator unit to enable detection of very low level distortion.

VI. Conclusion

A digitally assisted non-linearity suppression scheme capable of tuning a non-linear analog building block for optimal performance is proposed. As a proof of concept, simulations have been performed with an LTE signal and a non-linear CSF with $10\,\text{MHz}$ baseband bandwidth. The proposed technique is capable of effectively tuning the filter for minimum



(a) LMS filter order and correlation



(b) Auxiliary ADC resolution

Fig. 6: LMS filter length and ADC width analysis

TABLE I: Configuration of the auxiliary path components

Component	Configuration
Auxiliary ADC	6 bits
LMS filter length	9 taps
LMS coefficient width	10 bits
LMS output width	10 bits
Digital cubing unit	6 bits
Correlator multipliers	16 bits

distortion. Scenarios with strong channel interference and full bandwidth Rx signal have been investigated to obtain an estimate of the hardware overhead of the auxiliary digital control structure. The results show that the proposed scheme can be implemented with simple components resulting in a low hardware cost. Furthermore, the auxiliary control structure can be powered down once tuning is achieved resulting in power savings.

ACKNOWLEDGMENT

This work is a part of the DARE project and the authors would like to thank the Swedish Foundation for Strategic Research for funding.

REFERENCES

[1] B. Kim, J.-S. Ko, and K. Lee, "A new linearization technique for MOSFET RF amplifier using multiple gated transistors," *IEEE Microw. and Guided Wave Lett.*, vol. 10, pp. 371–373, Sep 2000.

[2] K.-H. Liang, C.-H. Lin, H.-Y. Chang, and Y.-J. Chan, "A New Linearization Technique for CMOS RF Mixer Using Third-Order Transconductance Cancellation," *IEEE Microw. and Wireless Compon. Lett.*, vol. 18, no. 5, pp. 350–352, May 2008.

[3] W.-H. Chen, G. Liu, B. Zdravko, and A. Niknejad, "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation," *IEEE J. Solid-State Circuits*, vol. 43, pp. 1164–1176, May 2008.

[4] A. Nejdel, M. Törmänen, and H. Sjöland, "A 0.7 to 3 GHz wireless receiver front end in 65-nm CMOS with an LNA linearized by positive feedback," *Analog Integr. Circuits and Signal Process.*, vol. 74, pp. 47–57, 2013.

[5] W. Huang and E. Sanchez-Sinencio, "Robust highly linear high-frequency CMOS OTA with IM3 below -70 dB at 26 MHz," *IEEE Trans. Circuits Syst. I*, vol. 53, pp. 1433–1447, July 2006.

[6] A. Lewinski and J. Silva-Martinez, "OTA linearity enhancement technique for high frequency applications with IM3 below -65 dB," *IEEE Trans. Circuits Syst. II*, vol. 51, pp. 542–548, Oct 2004.

[7] V. Aparin, G. Ballantyne, C. Persico, and A. Cicalini, "An integrated LMS adaptive filter of TX leakage for CDMA receiver front ends," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1171–1182, May 2006.

[8] E. Keehr and A. Hajimiri, "A rail-to-rail input receiver employing successive regeneration and adaptive cancellation of intermodulation products," in *IEEE Radio Freq. Integr. Circuits Symp.*, May 2010, pp. 47–50.

[9] ——, "Equalization of Third-Order Intermodulation Products in Wideband Direct Conversion Receivers," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2853–2867, Dec 2008.

[10] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge University Press, 2004.

[11] D. Filipovic and C. Komninakis, "Intermodulation distortion detection and mitigation," Jan. 2011, US Patent 7,876,867.

[12] S. Haykin, *Adaptive filter theory*, 4th ed. Prentice Hall, 2002.

[13] E. Dahlman, S. Parkvall, and J. Skold, *4G: LTE/LTE-Advanced for Mobile Broadband*, 1st ed. Academic Press, 2011.

[14] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6-bit 1.2-GS/s low-power flash-ADC in 0.13-μm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1499–1505, July 2005.

[15] C.-Y. Chen, M. Le, and K. Y. Kim, "A Low Power 6-bit Flash ADC With Reference Voltage and Common-Mode Calibration," *IEEE J. Solid-State Circuits*, vol. 44, pp. 1041–1046, April 2009.

[16] M. Chahardori, M. Sharifkhani, and S. Sadughi, "A 4-Bit, 1.6 GS/s Low Power Flash ADC, Based on Offset Calibration and Segmentation," *IEEE Trans. Circuits Syst. I*, vol. 60, pp. 2285–2297, Sept 2013.

[17] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. Van der Plas, "A 2.2 mW 1.75 GS/s 5 Bit Folding Flash ADC in 90 nm Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 44, pp. 874–882, March 2009.