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Published in:
IEEE Electron Device Letters

DOI:
10.1109/DRC.2012.6256966

2012

Link to publication

Citation for published version (APA):
Persson, K-M., Berg, M., Borg, M., Wu, J., Sjöland, H., Lind, E., & Wernersson, L-E. (2012). Vertical InAs nanowire MOSFETs with IDS = 1.34 mA/μm and gm = 1.19 mS/μm at VDS = 0.5 V. *IEEE Electron Device Letters*, 195-196. https://doi.org/10.1109/DRC.2012.6256966

Total number of authors:
7

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Vertical InAs Nanowire MOSFETs with I_{DS} = 1.34 mA/µm and g_m = 1.19 mS/µm at V_{DS} = 0.5 V

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III-V MOSFETs are currently considered for extension of, or as an add-on to, the Si CMOS technology. Following the Si-technology evolution, it is attractive to consider advanced III-V transistor architectures with non-planar geometry and improved electrostatic control [1]. We report on vertical InAs single nanowire FETs with diameter of 45 nm diameter, integrated on Si substrates with L_G = 200 nm. The devices demonstrate normalized extrinsic g_m and I_{DS} of 1.34 S/mm and 1.19 A/mm, respectively, at a V_{DS} of 0.5 V, and with an on-resistance of 321 Ωµm, all values normalized to the circumference. The improvements in g_m and I_{DS} as related to previous work [2] are attributed to the improved higk-κ interface consisting of Al_2O_3/HfO_2, as well as to the nanowire source resistance, which is reduced by applying an inorganic spacer layer. The main performance limitation is identified as the drain resistance in the ungated top part of the wire. By scaling the NW diameter to 28 nm, we also observe subthreshold swing down to 80 mV/decade at 50 mV V_{DS}. However, the on-resistance increases for the narrow wires to 75 kΩµm, and the normalized current level is reduced as compared to the larger diameter wires.

A 4” highly resistive Si wafer, which is overgrown with a 300-nm-thick InAs buffer layer, serves as sample substrates [3]. Electron-beam-lithography defined gold particles placed in arrays prior to epitaxial growth are made on 2x2 cm^2 pieces. Each sample has 160 FETs, both single- and multi-wire devices, with RF compatible layout. High-κ gate oxides are deposited with an ALD process consisting of 0.5 nm Al_2O_3 at 250 °C and 6.5 nm HfO_2 at 100 °C, directly after epitaxial nanowire growth. For device isolation and stray capacitance minimization, source mesas are etched out from the buffer layer. In a novel fabrication procedure, the first spacer layer, separating source and gate, is formed by plasma-enhanced-chemical-vapor-deposition of 60 nm Si_3N_4. The sputtered tungsten gate is defined using an etch mask and a dry-etch procedure. The top spacer layer separating gate and drain is made of a spin-coated organic film and has a thickness of 150-250 nm, making the ungated top part of the wire the largest fraction of the series resistance that limit the performance.

DC characterization is performed for single and multi NW InAs NW FETs, where the best single NW device of 45 nm diameter shows a normalized I_{DS} of 1.82 mA/µm and 1.34 mA/µm at a V_{GS} of 1.0 V and *a* V_{DS} of 1.0 V and 0.5 V, respectively. These devices also show a corresponding g_m of 1.45 mS/µm and 1.19 mS/µm at a V_{DS} of 1.0 V and 0.5 V, respectively. The V_t is extrapolated using the maximum transconductance method and determined to -0.27 at V_{ds} = 0.5 V. The device shows a low hysteresis of less than 5 mV at a V_{DS} of 0.5 V, most likely due to a low trap concentration within the low temperature deposited HfO_2 film. Devices scaled in diameter to 28 nm, with a 5.0-nm-thick Al_2O_3/HfO_2 film, and with 96 wires in parallel show a normalized I_{DS} of 0.112 mA/µm, a transconductance of 0.154 mS/µm, and a V_t of -0.23 V at a V_{DS} of 0.5 V and within 0.5 V V_{GS}. While the performance is lower in the on-state, the subthreshold swing is greatly improved down to 80 mV/decade at a V_{DS} of 50 mV. Data for both samples is benchmarked in Table 1 [4], demonstrating good performance as compared to alternative implementations. S-parameter measurements of our RF devices with 45 nm in diameter, show that FETs consisting of 192 wires in parallel, operate with f_t = 18.5 GHz and f_{max} = 32.2 GHz. Although these values represent a two fold increase to previous published data for InAs NW FETs [5], the performance is still limited by parasitic contact pad capacitances, originating from the limitations of the optical lithography used.

[1] J. A. del Alamo, *Nature*, vol. 479, no. 7373, pp. 317-323, Nov. 2011
[2] C. Thelander et al., *IEEE Electron Device Lett.*, vol. 29, no. 3, pp. 206-208, Mar. 2008
[3] S. Gorji Ghalamestani et al., *J. Crystal Growth.*, vol. 332, no. 1, pp. 12-16, Oct. 2011
[4] A. Dey et al., *IEEE Electron Device Lett.*, (Accepted for publication 2012)
[5] S. Johansson et al., *IEEE Trans. Microw. Theory Tech.*, vol. 59, no 10, Oct. 2011

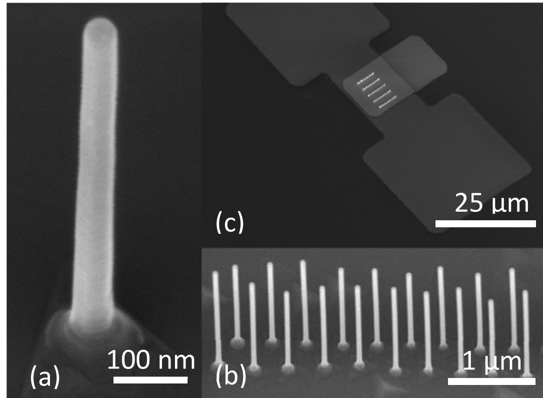

Fig 1. SEM images (30° tilt angle) of a single NW (a) and an array of NWs (b) after ALD as well as a 192 NW array with etched-out source mesa and sputtered W-gate-pad (c).

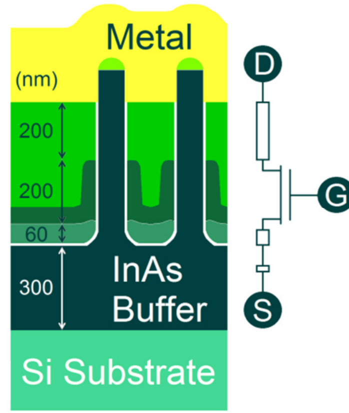

Fig 2. Schematic cross-section showing the different layer thicknesses in the fabricated device.

Fig 3. SEM image (30° tilt angle) of a single NW after the gate length definition.

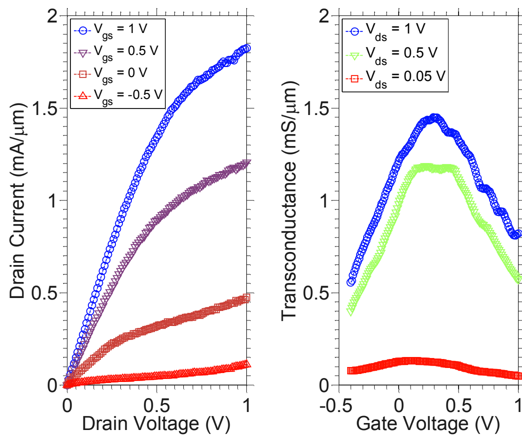

Fig 4. Normalized I_{DS} vs V_{DS} for a single 45 nm NW FET. Fig 5. Normalized g_m vs V_{GS} for a single 45 nm NW FET.

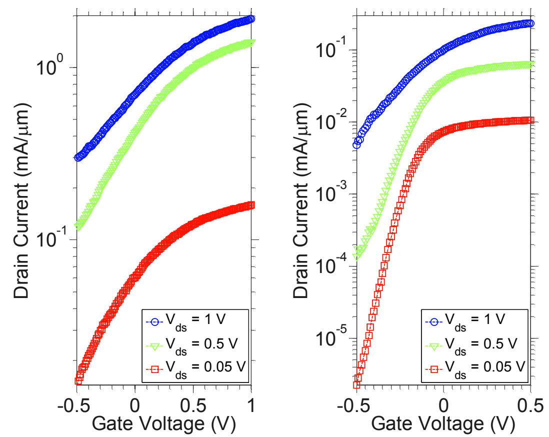

Fig 6. Normalized I_{DS} vs V_{GS} for a single 45 nm NW FET. Fig 7. Normalized I_{DS} vs V_G for a 28 nm NW array FET.

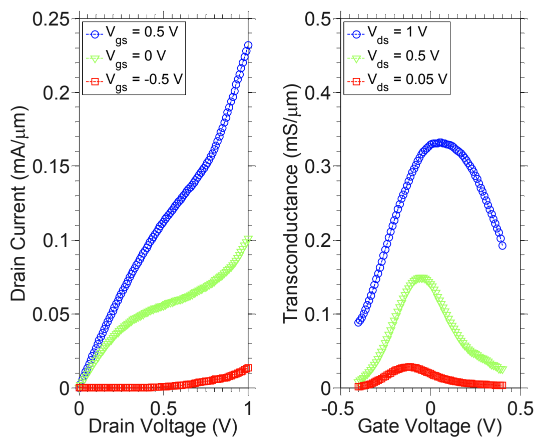

Fig 8. Normalized I_{DS} vs V_{DS} for a 28 nm NW array FET. Fig 9. Normalized g_m vs V_{GS} for a 28 nm NW array FET.

D (nm)	L_G (nm)	I_{ON} (mA/µm)	$g_{m,max}$ (mS/µm)	SS (mV/dec)	Tech	Reference
28	200	0.058	0.15	140	vertical NW	This work
45	200	0.67	1.19	560	vertical NW	This work
15	100	0.6	1.23	140	lateral NW	A. Dey et al EDL 2012
10	30	0.7	1.9	80	HEMT	D.-H. Kim et al EDL 2008
30	250	0.12	0.56	120	FinFET	J. J. Gu et al APL 2011
10	75	0.55	1.75	95	QWFET	M. Radosavljevic et al IEDM 2009
25	170	0.4	0.8	260	radial NW	X. Jiang et al Nano Lett 2007
13	230	0.9	1.72	180	XOI	K. Takei et al APL 2011

Table 1. Data benchmark for this work and other high performance technologies at a V_{DS} of 0.5 V and a V_{OD} of 0.5 V