HIGH DENSITY POWER CONVERSION ELECTRONICS ENABLED BY GAN-BASED MODULAR TOPOLOGIES

by

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This dissertation explores the use of modular multilevel converter (MMC) architectures, coupled with wide-bandgap semiconductors, to achieve high power-density in power electronics converters. At the converter level, the capabilities of the modular multilevel converter are investigated for their use in low voltage, low power, DC-DC and DC-AC applications. This investigation shows that the use of modular multilevel architectures enables low voltage Gallium Nitride high electron mobility transistors (GaN HEMTs) to be used in applications for which their voltage thresholds are not typically suited. This results in lightweight, compact, conversion systems.

GaN HEMTs have been shown to provide a low loss, low volume alternative to Silicon transistors for power conversion, but require several enabling technologies to make them ideally suited to high-density converters. This work therefore presents two enabling technologies for GaN-based conversion circuits. First, a technique is developed that optimizes the gate resistance for driving GaN HEMTs in order to ensure safe, rapid device turn on. Next, the development of planar magnetic transformers is discussed, with a focus on high-frequency converter operation. For each of these technologies mathematical analysis, circuit simulation, and hardware development are performed and compared to ensure proper functionality.

Taking advantage of those two enabling technologies, two converter architectures based on the MMC structure are developed. First, a DC-AC MMC is presented, taking advantage of GaN HEMTs and minimal filtering requirements to achieve high power density in low voltage systems. Next, that topology is extended and a novel DC-DC converter based on two coupled DC-AC MMCs is presented. Both systems are described mathematically, simulated, and developed as hardware prototypes to prove functionality. While both converter systems are relevant for applications in DC microgrids, the DC-AC converter will be specifically investigated for its application as a variable speed drive in naval power systems. Likewise, the DC-DC MMC will be shown to provide new solutions for high voltage spacecraft power systems.

Based on the work presented in this dissertation, engineers will be presented with alternatives to traditional methods of achieving high density in power conversion systems. By coupling the low filtering requirements and low losses of the modular multilevel converter with low voltage, highly efficient GaN HEMTs, the presented converter systems achieve high power density and efficiency with minimal filtering requirements. The result of this work is two novel converter systems that will enable further research into lightweight, low volume, power conversion.

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ACKNOWLEDGEMENTS

My advisor, Dr. Gregory Reed, likes to say that doctorates do not belong solely to the candidate to whom they are awarded, but also to the family and friends who have aided them in their pursuit of that degree. That sentiment could not be truer than in the case of the work presented here. While the ideas contained within the following pages are the result of my research, none of it would have been possible without my incredible colleagues, my wonderful friends, and my amazingly supportive family.

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dissertation and have individual taught me innumerable lessons about their respective areas of expertise.

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As important as my colleagues are to this work, none of it would have been possible without my friends and family outside the academic community. My friends have supported me throughout this process and have been of tremendous service to me. At the same time, my family has been the inspiration behind this work and the motivation to drive towards this accomplishment. My mom, Aenne Barchowsky, is an incredible architect and her design work has inspired me to think differently about spaces and surfaces. While she likely does not realize the impact that showing me every church in Europe had as a child, nor the impact of diligence required to reach your goals, she has been fundamental in shaping my way of thinking. My dad, Dr. Aaron Barchowsky, deserves credit for helping me to think like a scientist, introducing me to the

academic world, and teaching me from an early age that you have to fight for and earn your place within a community. My brother, Andrew Barchowsky, has likewise been an inspiration and a companion throughout my life and as we have matured from childish competition to adult support, has become an incredibly close friend. His support has been incredible and I could not be more proud of how he has likewise grown in his understanding and achievements.

Finally, and most importantly, I would like to thank my incredible wife Katelyn Barchowsky. If any who read this need to search for the true inspiration and genius behind this work, please look no further than Katelyn. Her support, her affection, her generosity, and her intelligence, and most importantly her love were instrumental in this work. Her thoughts and support and woven behind every idea, mingled with every image, and instilled in every table. Without her, this would not have been possible. She is the love of my life, the wind in my sails, and anything achieved within this work belongs just as much to her as it does to me.

1.0 INTRODUCTION

Achieving higher power-density for power conversion systems is extremely important for reduction of space requirements for electrical systems. For applications ranging from residential homes and commercial datacenters to naval vessels and spacecraft, power demands are increasing while available volume is decreasing, placing much more demanding restraints on the power conversion and distribution systems. As a result, engineers and researchers are designing converter systems optimized around power density and efficiency, enabled through the use of wide bandgap semiconductors at high switching frequencies. To present an alternative to those designs, this dissertation presents new methods for attaining high power-density in conversion systems, based on the union of GaN transistors and the modular multilevel converter topology.

Existing research avenues in wide bandgap semiconductors and modular multilevel converters have been focused on opposite ends of the power conversion spectrum. While MMC systems have been widely employed in High Voltage Direct Current (HVDC) transmission systems and Medium Voltage (MV) variable speed drives (VSDs), GaN converters have been primarily designed for low voltage, high frequency conversion systems. This dissertation aims to bring the theory and lessons learned about the MMC in high voltage transmission and medium voltage VSDs to low voltage, high-density power conversion through the use of enhancement mode GaN HEMTs in modular converter architectures. The research presented here investigates

the application of GaN-based MMC converters for DC-AC and DC-DC conversion applications, focusing on the achievement of high power-density and efficiency. .

1.1 OBJECTIVE

To meet the demands of the evolving power electronics market, many new topologies and implementations have been realized using modern power electronic converters [1]. The rapid technological development of these converters has been enabled by the maturation of wide bandgap (WBG) power semiconductors, specifically SiC [2] and GaN [3]. Devices made from these materials provide improved figures of merit when compared to traditional silicon MOSFETs and IGBTs, allowing converters to operate at high switching frequencies without incurring unbearable switching losses. Through the increase in frequency, converters require less significant filtering components to achieve the same input and output quality, leading to a drastic reduction in volume. Additionally, both of these WBG semiconductor types can sustain higher operating temperatures compared to silicon, making them particularly attractive for high power density applications [4]. To take advantage of these devices, new system topologies and control architectures are being developed, providing improved capabilities, raising efficiency, and reducing size requirements [3], [5], [6].

Numerous groups have developed DC-AC and DC-DC systems designed to be small and light, with the goal of enabling power conversion electronics to be used in more diverse applications at reduced installation cost. In the kW range, the majority of DC-AC systems utilize the H-bridge topology, while the majority of DC-DC converters in the same power range use the dual active bridge. Both apply the same principle, achieving high-density through the use of pulse

width modulation at increased switching frequencies. Low volume is achieved through the resulting reduction in size of required filtering components [1], [2], [3]. However, higher frequency operation corresponds to an increase of switching losses in the power stage of the converter, which results in a design choice of limiting switching frequency in order to improve efficiency [4]. Thus, power conversion engineers have begun exploring multilevel topologies in low voltage inverters in order to allow the use of smaller semiconductor devices, while minimizing volume and losses [4]. To this end, this work presents the adaptation of the modular multilevel converter (MMC) to low voltage, high density applications. The MMC has been shown to be a highly versatile and efficiency topology in high voltage direct current (HVDC) transmission systems, as well as medium voltage variable speed drives [5], [6], [7], [8]. The voltage division between submodules (SMs) in MMC allows for the use of low voltage switches and drastic reduction in the size of required output filtering, without the required increase in switching frequency [5], [9]. In this dissertation, the application of such MMC systems will be applied along with GaN devices in order to achieve extremely high power density in both DC-AC and DC-DC systems. Each of these two converter types will be analyzed, simulated, and demonstrated in hardware systems.

To characterize the converters presented in this dissertation, several supporting concepts must be introduced and investigated for their merits in high-frequency, GaN-based power conversion systems. First, the fundamentals of the MMC are discussed, including submodule topologies, switching states, and the well-established equations that govern the dynamics of three-phase MMC systems. Next, two essential technologies for high frequency, high density power electronics are introduced – wide bandgap semiconductors and ferrite magnetic materials. These technologies both allow for the creation of converters that are able to operate in the frequency range from several hundred kilohertz to several megahertz, which is of specific relevance to high-

density MMC design. This foundation will be used later within this work to present two adaptations of these technologies specifically for the GaN-based MMC.

The first of these enabling technologies is a study that specifically investigates the gate driving of GaN HEMTs for high-density power electronics. The gate-to-source path of GaN HEMTs tends to be much more sensitive to overvoltage excursions than those of Si or SiC MOSFETs, and as such great care must be taken when selecting gate resistance values for driving these devices in power circuits. Here a natural trade-off exists between the overshoot on the device and the speed with which turn on occurs, dependent on the resistance, inductance, and capacitance of the printed circuit board (PCB) and the GaN HEMT itself. In order to ensure safe, rapid turn on in the device, a method is presented that analytically predicts the optimal gate resistance for a system based on circuit parameters and a selected safety margin. This method is developed based on analytical models of GaN HEMTs during turn on and is then verified in a double pulse test circuit implemented in hardware. The resulting tool is then used throughout this work in order to ensure safe operation of the proposed GaN converters.

However, more than just the gate drive and device must be taken into account in order to ensure proper converter performance at high frequency. With switching frequencies ranging in into the megahertz region, however, design of magnetic elements becomes more challenging. For high density transformer applications at high frequency, these challenges include large impact from parasitic circuit elements, skin effects, and thermal restrictions [10], [11]. Magnetic components at higher frequencies must therefore be carefully selected and designed in order to ensure that they do not saturate, overheat, or contribute large amount of losses to the system. To minimize volume requirements of the transformer for the DC-DC converter system while ensuring that the converter functions as desired, a set of planar transformers is proposed and evaluated.

These transformers are based on magnesium-zinc ferrite materials and take advantage of planar cores with PCB-integrated copper windings to achieve high conversion ratios in minimal volume. The proposed transformers are analyzed mathematically, simulated using finite element analysis tools, and characterized in hardware using impedance analysis. Comparisons are made between various winding and core designs for these transformers, and the resulting best-case transformer design is inserted into the model and development of the DC-DC MMC.

Taking advantage of these two enabling technologies, two classes of converters are presented in this work. First, A DC-AC converter based on a single-phase GaN MMC architecture is shown. Through the advantages provided by the extremely low conduction and switching losses of GaN HEMTs, the DC-AC MMC achieves high efficiency and power density while operating at switching frequencies that are orders of magnitude higher than those employed by conventional HVDC MMC systems. The MMC structure further allows for the reduction in size in energy storage elements in the converter, achieving low harmonic content on the output with minimal filtering systems. The result is a converter class that will allow for high quality voltage and current outputs and low losses while in a form factor much smaller than conventional inverter architectures. Specific application of the DC-AC MMC is also discussed, using the proposed architecture as a variable speed drive (VSD) for naval vessels using DC distribution systems.

By combining two DC-AC converters via the planar transformer described previously, a GaN-based DC-DC MMC architecture is then presented. This converter takes the advantages provided by the DC-AC MMC system and furthers them through operation at a switching frequency and AC link frequency of 1 MHz. This faster operation results in a reduction of the requisite submodule capacitance by a factor of 10^6, drastically reducing the total volume of a submodule and thus the converter. However, operation at such high frequency has never before

been evaluated in the MMC architecture and special considerations need to be made to ensure proper functionality of the converter. To mitigate the extremely high switching losses that would be incurred through traditional operation of the converter, this work presents a trapezoidal modulation strategy based on nearest-level comparisons to reduce the switching operation of a given submodule to once per AC cycle. Additionally, new techniques are presented to avoid the computationally demanding capacitor balancing algorithms that have been traditionally used in HVDC systems and replace them with a sequential insertion technique resulting in natural balancing between submodules. To demonstrate this system, its application as an anode discharge power module for solar electric propulsion systems is presented. The result is a DC-DC converter with input and output voltage and power levels scalable to the needs of the system in an architecture that minimizes the volume and weight of the converter, achieving extremely high power density.

For each of the proposed converter systems, analytical description and evaluation of the converter operation is presented. The theoretical behaviors of voltages and currents through the multilevel converter structures are presented and mathematical derivations are presented to describe those behaviors. Based on those values, system development is presented, sizing converter components and submodule structures to meet the demands of proposed test systems. In addition, mechanisms for the controlled operation of these converters are described. For the DC-AC converter, a phase-shifted pulse-width modulation (PS-PWM) scheme is presented, achieving natural balancing in the arms in exchange for slightly higher switching losses than in other modulation schemes. For the DC-DC MMC, however, this modulation must be replaced with the previously described quasi-square wave nearest level modulation (QSW NLM) in order to further minimize switching losses. In that case, a new capacitor balancing algorithm, based on progressive

insertion of submodules, is presented and analyzed. Thus for each converter a complete analytical model is achieved.

Next, simulation models will be developed for the each of the proposed converter systems. The simulations are developed in MATLAB/SIMULINK with the PLEXIM plugin. The PLEXIM plugin, an independent power electronic solver that interfaces with the SIMULINK platform, allows for detailed modeling of the converter, including the switching losses of the GaN HEMTs. The combination of the PLECS and SIMULINK simulation systems allows for complete simulation of the converter systems, providing benchmarks for efficiency, total harmonic distortion (THD), ripple, and control performance, to which the physical hardware can later be compared. This dissertation presents complete simulation development and results for each converter, including applications in relevant power systems.

Finally, for each converter structure hardware prototyping is presented. First, for the DC-AC system, the development of submodule (SM) test PCBs is presented. This is used to analyze the switching performance of GaN HEMTs in isolated switched capacitor half-bridge configurations. Results for the switching performance and thermal analysis are presented. This SM design is then extended to the full DC-AC MMC architecture, presenting PCBs that contain 14-level MMC arms. These are evaluated at low voltage for functionality, demonstrating good results for the DC-AC system. Finally, initial development of the DC-DC MMC system is presented, with a high-speed two level converter design. This is used to verify the performance of the proposed changes to the circuit topology, and will be used for further development of these systems.

To conclude, it is the purpose of this work to develop new techniques, topologies, and control systems to enable the creation of high-density power converters based on the MMC architecture. Various aspects of the design of both DC-AC and DC-DC MMC systems utilizing

GaN HEMT devices will be presented, including mathematic models, simulation development, and prototype realization. This work will be supplemented with projects designed to optimize the use of GaN HEMTs and magnetic components in such high-density applications. These novel converters provide alternatives to traditional designs to achieve high power density in scalable power conversion systems.

1.2 ORGANIZATION

This dissertation is organized and sectioned based on the individual projects described previously. First, background for the operation of MMC systems in high density applications will be discussed, followed by overviews of the advantages of wide bandgap semiconductors and ferrite materials for achieving high power density. With the background established, this work will then present the enabling technologies of gate drive optimization and planar ferrite transformer design. To each of these subjects a chapter is dedicated, establishing the techniques and their relevance to high density converter design. Based on these enabling technologies and the fundamentals of MMC operation, the two proposed converters will be presented. For each of the proposed DC-AC and DC-DC MMCs, a chapter is used to describe circuit operation, analytical analysis, simulation, and hardware development. This document then concludes by addressing the importance of these proposed architectures and their relevance to the future of high density power converter design.

2.0 BACKGROUND

In order to properly describe the GaN-based modular multilevel converter systems that are presented within this work, several background technologies must first be described. This section therefore details first the application of the MMC to high-density power electronics, comparing it to existing techniques and providing an overview of the well-established 3-phase MMC structure commonly used in HVDC systems. This will serve as a background to the derivations of the single-phase DC-AC and DC-DC converters presented further in this work. Next, the background for the use of GaN HEMTs and their benefits for achieving high density and low losses in power converters is discussed. Of particular interest in this work is the ability of the MMC to allow these low voltage, highly efficient devices to be used to achieve high voltage converter operation. Finally, an overview of ferrite materials and their benefits for MHz-range switching is presented, laying the foundation for the transformer designs presented in Chapter 4. Using the background presented here, this work will then proceed to apply application-specific development techniques and achieve the desired high density MMC systems.

2.1 HIGH DENSITY MULTILEVEL POWER ELECTRONICS

The modular multilevel converter topology in HVDC converter applications boasts a number of advantages over traditional multilevel designs. These include high modularity in

hardware and software, low generation of harmonics, low switching frequency and low voltage of semiconductor devices, low filtering requirements, and high efficiency [1]. Extensive literature exists for the MMC in 3-phase HVDC applications, [5], [6] and MV VSD applications, [7], [8]. Additionally, excellent references on MMC topology, modulation, and control is provided in [2], controller design in [3], and energy storage requirements in [8] and [12].

Specifically, multilevel converter topologies, such as the neutral point clamped converter [1] provide the capability to "build" voltage waveforms from fixed step sizes, rather than relying on large filtering components to smooth out square waves generated from pulse width modulation (PWM). The MMC provides a means by which large voltages can be broken into small switching events, allowing voltage waveforms to be built from small step sizes, improving output performance, minimizing filtering requirements, and reducing stress on individual semiconductor devices. Extensive documentation exists for the MMC topology in the HVDC setting, as it provides a number of advantages for long distances transmission systems, especially when underground or underwater transmission is a necessity, or when space is at a premium. In this work, DC-AC and DC-DC MMC systems will be explored, focused on scaling systems designed for HVDC power transmission to a power and voltage levels suitable for use in low voltage, high-density systems, for application in renewable energy integration, variable speed drives, spacecraft power, and more.

A number of topologies exist for MMC systems, which range from systems comprised of half H-bridge, full H-bridge, hybrid H-bridge, and more [5]. The two most typical configurations are the half-bridge and the full-bridge, which are illustrated in Figure 1 and Figure 2, respectively.

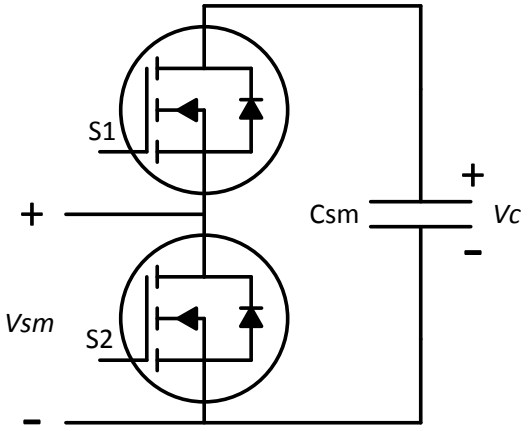


Figure 1. Half-bridge submodule for modular multilevel converter design

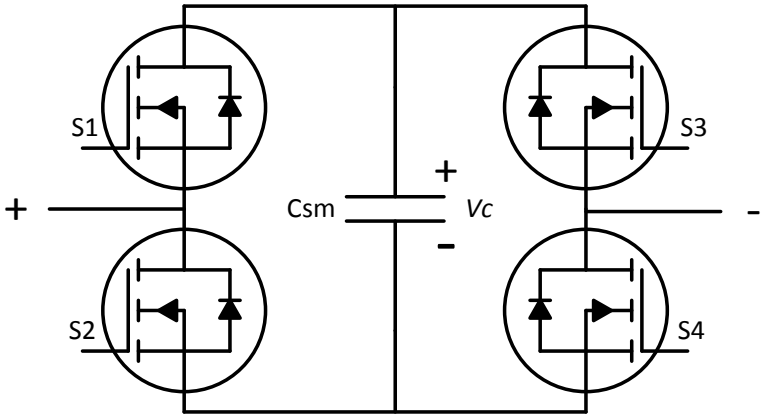


Figure 2. Full bridge submodule for modular multilevel converter design

While both are commonly used within the HVDC industry, the half-bridge topology provides lower switching losses. As the converters presented here will be operating at high switching frequencies, the half-bridge is therefore preferred. A half-bridge submodule behaves as shown in Figure 3. The two semiconductor devices in the system are switched inversely, with S_1 introducing the submodule capacitor into the system, and S_2 bypassing that same capacitor.

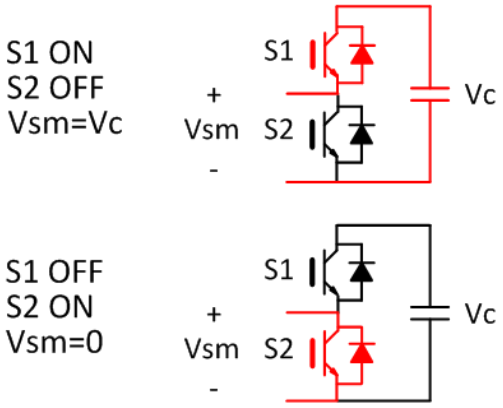


Figure 3. Switching states of a half-bridge modular multilevel converter submodule

The objective is to add or remove the voltage and charge stored on the capacitance to the system, yielding either 0 V output, or output equal to the voltage on the capacitor, based on the switching state. These submodules are then combined in series to form converter, as shown in Figure 4.

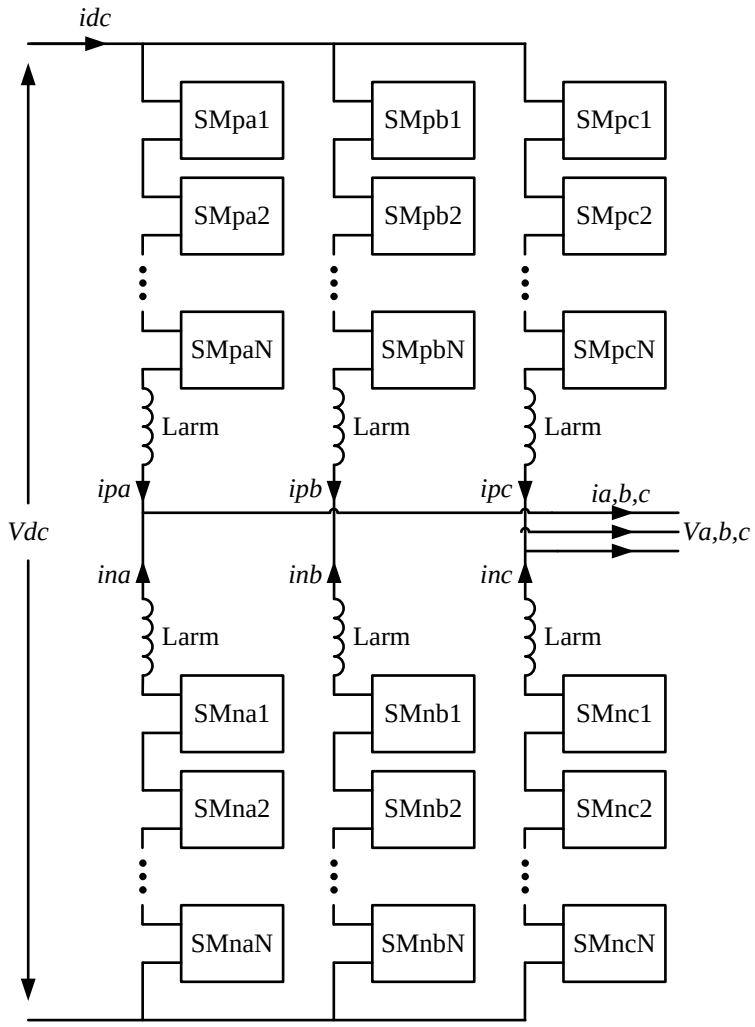


Figure 4. Three-phase modular multilevel converter topology

The series combination of submodules of the MMC allows for the creation of a voltage waveform that closely approximates a sinusoidal waveform, with little to no filtering requirements.

Based on the switching states shown in Figure 3, the voltage produced by a given phase arm can be controlled by switching the appropriate number of SMs into state 1. By treating the SM capacitors as ideal voltage sources, the phase *a* upper and lower arm voltages can be described according to (1) and (2) respectively,

$$v_{pa} = \frac{V_{DC}}{2} - V_{AC}\, sin(\omega t) = \frac{V_{dc}\big(1 - msin(\omega t)\big)}{2} \tag{1}$$

$$v_{na} = \frac{V_{DC}}{2} + V_{AC}\, \sin(\omega t) = \frac{V_{dc}\big(1 + msin(\omega t)\big)}{2} \tag{2}$$

where the modulation ratio *m* is described by (3).

$$m = \frac{2V_{AC}}{V_{DC}} \tag{3}$$

As the voltage in the arms fluctuates, the capacitors in the arms will become slightly unbalanced, inducing circular current flow between the phase arms. As a result, the currents in the upper and lower arms can then be described by (4) and (5), respectively.

$$i_{pa} = \frac{i_{DC}}{3} + \frac{i_a}{2} + i_{circ,a} \tag{4}$$

$$i_{na} = \frac{i_{DC}}{3} - \frac{i_a}{2} + i_{circ,a} \tag{5}$$

where the circulating current is described by (6),

$$i_{circ,a} = \frac{i_{pa} + i_{na}}{2} - \frac{i_{DC}}{3} \tag{6}$$

By substituting the expressions for the arm current into the equations for the voltage, the current can be re-expressed as (7) and (8),

$$i_{pa} = \frac{i_{DC}}{2}\left(1 + nsin(\omega t)\right) \tag{7}$$

$$i_{pa} = \frac{i_{DC}}{2}\left(1 - nsin(\omega t)\right) \tag{8}$$

where *n* is the ratio between the AC and DC current, as described in (9) [13].

$$n = \frac{i_a}{2i_{DC}} \tag{9}$$

It can be seen that the performance of the single-phase MMC is remarkably similar to that of its 3 phase equivalent, with the expectation of producing extremely clean sinusoidal waveforms with minimal loss.

In HVDC MMC applications the semiconductor device is typically an IGBT, as seen in [5]. The reliance on IGBTs is a result of the extremely high voltage on those systems, often 10 kV or more on a single device. In the application presented here, however, both system and device voltages are significantly lower, at most on the order of 100 V, enabling the use of WBG semiconductors for switching applications. These devices can provide significant advantages over their Si counterparts, further improving this already efficient topology. The MMC topology is perfectly suited to construction from many small WBG semiconductors, taking advantage of the superior performance and size of the WBG devices to drastically reduce converter size and improve efficiency. The well-established relationships and techniques presented in this section form the basis for the high density converter designs and derivations presented in Chapter 5 and

Chapter 6 and enable the development of systems designed to take advantage of GaN HEMTs in MMC structures.

2.2 Wide Bandgap Power Semiconductors

In order for MMCs to take advantage of GaN devices in the high power systems presented in this work, the function of the devices themselves must be well understood. As power electronics develop, the emphasis on size reduction coupled with improved efficiency cannot be understated. The goals, as expressed in [14], are twofold. First, many applications have space or weight restrictions that benefit from size minimization, such as shipboard or avionic systems or in-home PV converters. Second, many new topologies and implementations can be realized using modern power electronic devices.

Wide bandgap semiconductors based on GaN and Silicon Carbide (SiC) are well-suited transistor technologies for applications in next generation power electronic switching circuits. These applications include renewable energy integration, electric vehicular circuits, as well as aerospace and maritime systems. Due to their fast switching capability, wide bandgap semiconductors (WBGs) are able to sustain efficient operation at high switching frequencies. This attribute enables the use of smaller filter components within the converter topologies which leads to volume reduction and increased power density. In naval and aircraft applications, power density and volume are critical parameters as system weight reduction can lead to improved fuel efficiency. In addition, WBGs can withstand temperatures above 300 deg. C, making them particularly attractive in conditions where high temperatures are observed. Finally, the relatively

low on-resistance associated with WBGs makes them more efficient during steady-state conduction time.

The rapid development of WBG semiconductors and of higher voltage capabilities in both SiC [15] and GaN [16] have enabled a new generation of DC-DC converters to meet both of the previously stated goals. Both SiC MOSFETs and GaN HEMTs, the structures of which are shown in Figure 5 and Figure 6, have been shown to maintain superior performance in high switching frequency applications, thereby enabling the use of smaller filter components within the converter topology and leading to a reduction in power conversion volume. Additionally, both of these WBG semiconductor types can sustain relatively high operating temperatures, making them particularly attractive for renewable energy applications [17].

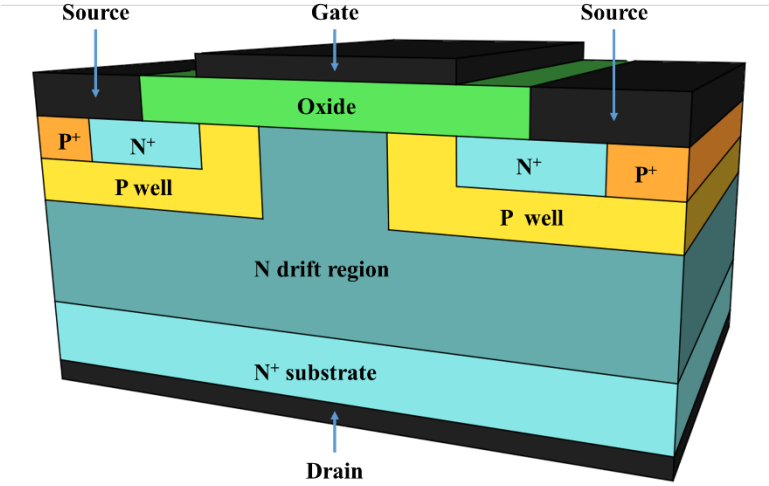


Figure 5. Device structure for a vertical SiC MOSFET

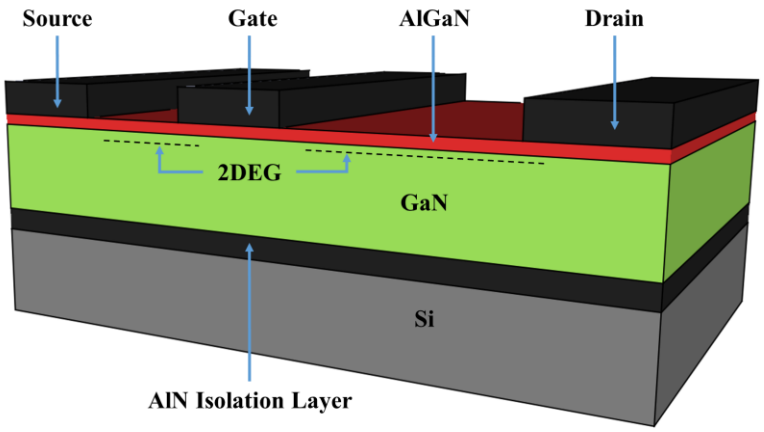


Figure 6. Device structure for a lateral GaN HEMT

In the case of high-density power conversion electronics, the application of WBG semiconductors can drastically reduce the size requirements for both DC-AC and DC-DC converters. However, the same characteristics of these devices that allow for faster state transition can result in undesired transients in either the device itself or the converter as a whole. At the device circuits level, the fast switching capability of SiC and GaN have led to detrimental transient behavior such as overshoot, ringing, and false turn-on [18], [19], [20]. In order for WBG semiconductors to deliver their full potential of enhancing DC-DC power electronics devices, the aforementioned unfavorable characteristics of GaN and SiC must be understood, modeled, and mitigated.

However, in spite of the many theoretical advantages of WBGs, considerable technological readiness challenges have hindered their widespread adoption. For example, to address the breakdown limitations associated with lateral GaN transistors, a paradigm shift towards vertical device architectures is being investigated. Optimization of printed circuit board layout is another important area of research, particularly since the fast switching capability of WBGs makes them

more prone to detrimental transient effects contributed by the parasitic loop inductance [21]. This is particularly true in GaN, where low voltage normally-off lateral devices have a 6 V maximum rating on the gate terminal. Consequently, these GaN devices are more susceptible to failure in fast switching power conversion circuits which often demonstrate second order system behavior such as overshoot and ringing. In order to keep the device safe, external resistance is applied to the gate of the GaN device which damps the problematic overshoot, at the expense of slower switching times.

This work here presents an analytical formulation that solves this apparent optimization problem by deriving an equation that finds the best value for the gate resistance, R_{G}. In order to find the optimal value of RG, the equivalent circuit models of the device during the three sub-stages of switching, as reported in are analyzed in detail [16], [17]. The circuit models consist of the parasitic nonlinear junction capacitances as well as the parasitic loop and package inductances. The third sub-stage of switching is analyzed in greatest detail to determine how R_{G} affects the voltage overshoot on the gate-terminal of the GaN device. The mathematical problem presented is solved and is then validated through hardware experimentation.

The calculated optimal value of R_{G} will enable the fastest switching time without catastrophic gate breakdown due to high overshoot. By finding the optimal gate resistance for safe, rapid turn on of GaN HEMTs allows for their use in high-frequency conversion systems that minimize the losses incurred during their switching.

2.3 FERRITE MAGNETIC MATERIALS

In order to minimize volumetric requirements for power conversion circuits, a common practice is to increase the switching frequency of the converter. The higher frequency switching allows for the reduction of reactive circuit elements, specifically the capacitive and magnetic (inductor and transformer) components that are required for the temporary storage of energy in switching applications. As a portion of the work presented here, a transformer is developed for a GaN MMC-based DC-DC converter. The transformer is based on ferrite materials, using a planar core with integrated PCB windings to help achieve 2 kW of power transfer in a minimal volume.

The advantages of ferrite materials and planar cores are discussed, the analytical selection of a core is presented, and finite element analysis (FEA) of the proposed transformer and the extraction of equivalent circuit parameters are shown. Ferrite materials are ceramic compounds combining iron oxides with other metals and metal alloys in crystalline structures. These structures "can be regarded as an interlocking network of positively-charged metal ions (Fe^{+++}, M^{2+}) and negatively charged divalent oxygen ions ($O^{=}$)" [22]. The metal ions used in these materials are ferromagnetic – that is they exhibit enhanced atomic spin effects. When combined with oxides of iron, the resulting ceramic material can maintain many of the benefits of traditional metal cores, while exhibiting improved performance at high frequency. When compared to their metal and metal alloy counterparts, tend to exhibit much lower saturation points as well as much lower permiabilities. This arises from the dilution of magnetic metal ions by the oxygen within the crystal structure and the antiferromagnetic interaction which stops ions without uncompensated spins from contributing to the magnetic moment [23]. The compounds used in power transformers are typically of the group known as soft ferrites, which exhibit low coercivity, high resistivity, and attractive magnetic properties at high frequency [23]. The tradeoff for these benefits are much

lower magnetic saturation levels, low Curie temperatures, as well as being extremely brittle [23]. In high frequency applications, these negative effects are overshadowed by their improvement over traditional transformer cores.

The most common soft ferrite cores used in power conversion electronics are Copper-Zinc ferrites Maganese-Zinc ferrites, and Nickle-Zinc ferrites, typically of the forms $Cu_aZn_{1-a}Fe_2O_4$, $Mn_aZn_{1-a}Fe_2O_4$, and $Ni_aZn_{1-a}Fe_2O_4$, respectively. As discussed in [23], the inclusion of the $ZnFe_2O_4$ component allows for enhanced saturation magnetization. Of these ferrites, MnZn and NiZn are typically used in the higher frequency range, each occupying key portions of the frequency range. MnZn is typically used in applications under 2 MHz, while NiZn is typically used in applications between 1 MHz and hundreds of MHz [24]. For the 1 MHz, 2 kW application presented in this paper, Ferroxcube's 3F4 MnZn ferrite was selected, for which the specific power loss and complex permeability curves can be seen in Figure 7 and , while key parameters for this material can be seen in Table V [24]. These properties make this MnZn ferrite ideal for power conversion in the range of 1 MHz, allowing for the design of a compact transformer to help enable high-density DC-DC converter design.

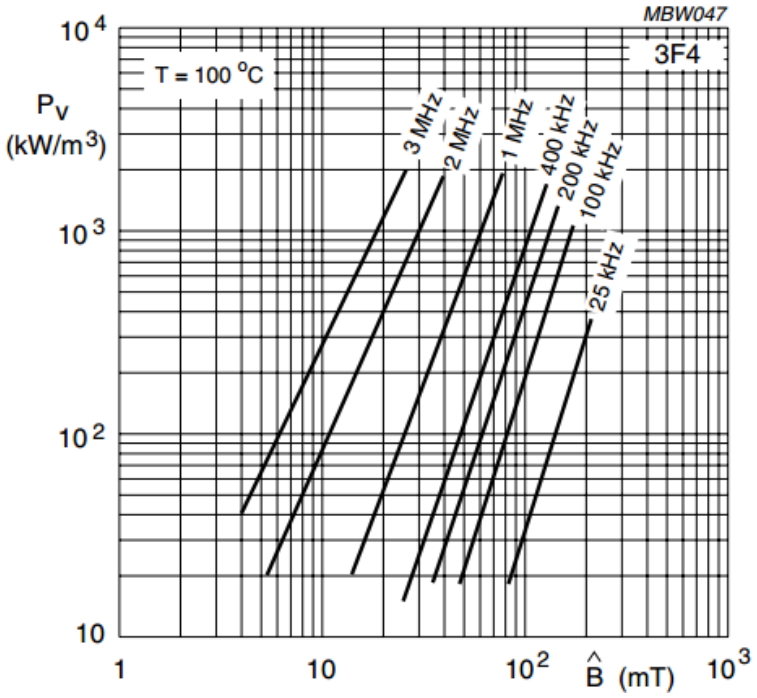


Figure 7. Specific power loss of Ferroxcube 3F4 MnZn ferrite

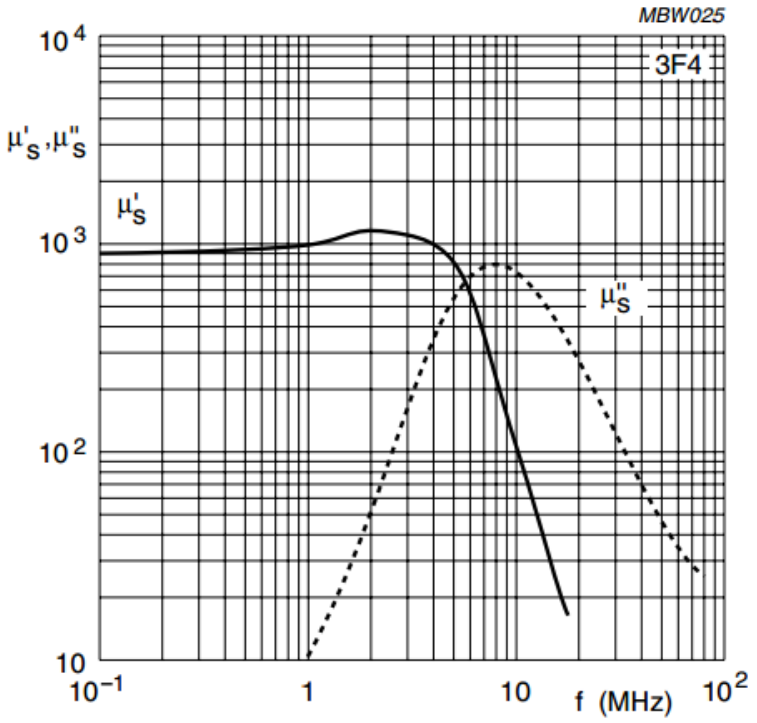


Figure 8. Complex permiability of Ferroxcube 3F4 MnZn ferrite

Table 1. Characteristic parameters of Ferroxcube 3F4

Symbol	Conditions	Value	Unit
μ_i	25 ˚C; ≤10 kHz; 0.25 mT	900 ± 20%	
μ_a	100 ˚C; 25 kHz; 200 mT	1700	
B	25˚C; 10 kHz; 1200 A/m	410	mT
	100 ˚C; 10 kHz; 1200 A/m	350	
P_v	100 ˚C; 1 MHz; 30 mT	130	kW/m^3
	100 ˚C; 3 MHz; 10 mT	220	
ρ	DC; 25 ˚C	10	Ωm
T_C		≥ 220	˚C

Planar magnetic cores for transformers and inductors are elongated, flattened devices that cover large areas, as opposed to more cubic traditional cores. Their low profile allow design engineers to achieve greater power densities by reducing the height of their converter systems, which is often dominated by the magnetic components [25]. In conventional wire-wound magnetic components, skin losses and proximity effects are extremely problematic at high frequencies. Planar magnetics replace the vertically stacked coiled wires with flat windings around a linear core. They are typically formed by the combination of two ferrite half-cores or a single ferrite half-core and a ferrite plate. Windings are typically formed horizontally around the core, and are generally comprised of Litz-wire or PCB traces.

This work presents the development of multiple transformers based on PCB integrated windings and planar cores to enable high-density power converters. Using the same core material, multiple core sizes, core compositions, and winding configurations for both parallel and series connected PCB layers are designed. The transformer design is analyzed mathematically, each is

analyzed using finite element analysis (FEA) in Ansys Maxwell, and prototypes of each core are developed and tested with assistance from the Department of Energy's National Energy Technology Laboratory. The result is a transformer that is capable of handling 2 kW of power with minimal mass and volume.

2.4 SUMMARY

This chapter has presented the basic technologies behind the modular multilevel converters presented in the remainder of the work. The well-established three-phase MMC architecture is described and the analytics as commonly seen in HVDC systems are presented. Further, its potential as an alternative to traditional topologies is discussed in the context of achieving high density in power conversion systems. To that end, two requisite enabling technologies have been introduced. First, a discussion of the use of wide bandgap semiconductors in power electronic systems is presented, with emphasis on the performance of such devices in converters operating at high switching frequencies. For such systems, the low conduction and switching losses of GaN HEMTs, combined with their low volumetric requirements and their excellent thermal performance, make them an excellent solution for achieving high density in power conversion. To further reduce volume and losses, this chapter also introduces the material fundamentals to be used to design a planar transformer using a magnesium zinc ferrite. The transformer design based on this architecture will be presented in Chapter 4, creating a solution for the MHz range DC-DC converter. Based on these basic enabling technologies, the following chapters present the development of conversion systems and their supporting features.

3.0 GATE DRIVE OPTIMIZATION OF GAN HEMTS

For certain power conversion applications, design engineers prefer "normally off" devices, which require positive gate voltages for turn-on, due to their improved safety in medium-high voltage applications [26], [27], [28]. Many manufacturers have begun fabricating normally off GaN devices, including *Efficient Power Conversion Corporation* ® (EPC), who produce the enhancement-mode GaN HEMTs used in this study. Unlike other GaN devices [18], the EPC transistor does not require a "cascode" structure to enable normally off operation. However, EPC devices do suffer from certain limitations. For example, the recommended steady state gate voltage during conduction is 5 V, however the gate insulator breaks down at voltages above 6 V [29], [30]. Therefore, only 1 V of safety margin is allowed between the recommended steady state operating voltage and potential device failure. Due to the very fast switching capability of GaN, high voltage overshoot on the gate is often observed [31]. In order to keep the device in its safe operating region, an external gate resistance is applied. While damping the overshoot, this added gate resistance comes at the expense of slower switching. Slower turn-on and turn-off can adversely affect the efficiency of the system. In order to ensure that the device operates within its safe operating regime, while minimizing device turn-on time and the resulting switching/transient losses of the system, it is desirable to determine an optimal gate resistance for the driving circuitry.

This chapter presents an analytical formulation that solves this apparent optimization problem by deriving an equation that finds the best value for the gate resistance, R_G. The calculated optimal

value of R_G will enable the fastest switching time without the catastrophic gate breakdown due to high overshoot. The mathematical problem presented is solved and is then validated through hardware experimentation.

The chapter is organized as follows. First, it describes the occurrence of voltage overshoot in GaN HEMTs, methods to mitigate overshoot, and design trade-offs for circuits using external gate resistors. Next, an analytical circuit that predicts the gate-source voltage overshoot based on a simplified 2nd order model of the device is presented. Finally, it validates the analytical model using a double-pulse test circuit with a 200V GaN HEMT. The result is a simple mathematical system that will allow design engineers to easily select the ideal gate resistance for their application.

3.1 PROBLEM CONTEXT: OVERSHOOT IN GAN HEMTS

3.1.1 Risk of Gate Overshoot in GaN HEMTs

Lateral GaN HEMTs have been shown to exhibit turn-on times that are significantly lower than Si transistors [32], [33]. Although rapid turn-on is desirable, resulting in lower switching losses in the converter, it can present problems in devices with gates that are sensitive to voltage excursions. This is the case for the EPC devices used in this study, which have a maximum rated gate voltage of 6V [18], [28], [34]. This relatively low absolute maximum rating can be problematic, since the device requires a steady-state gate-source voltage, V_{GS}, of 5 V in order to minimize conduction loss and enhance channel conductivity. Thus, only 1 V of safety margin is allowed between the device's recommended drive voltage and potential device failure.

At the same time, this class of devices exhibits relatively low input capacitance (C_{iss}) values. While enabling the desired rapid turn-on of the HEMT, the combination of this low capacitance and circuit parasitics can cause high overshoot [35]. As a result, both improved printed circuit board (PCB) design and external protective circuits are often required in order to effectively mitigate voltage overshoot experienced on the gate. PCBs should be designed such that minimal inductance is exhibited in both the gate-source and drain-source paths [34]. This can be achieved by reducing the total path length, minimizing package sizes on external components, minimizing coupling between conducting circuit elements, and taking advantage of multiple PCB layers to route traces [36]. The reduction in circuit inductance corresponds to a decrease in peak gate voltage ($v_{GS,peak}$), but is often not enough on its own to prevent exceeding the maximum rated gate-source voltage ($v_{GS,max}$). In order to further protect the gate, an external circuit typically in the form of a gate resistance, is often employed. While the addition of gate resistance is well understood to dampen voltage excursion on the gate of the device, industry practices are generally designed to ensure safety, without optimization in place for rapid switching. This work provides a means for rapid, safe turn on, by finding the optimal value for the gate resistor to be used in the circuit.

3.1.2 Effects of Gate Resistance on Turn On Transients

Several methods exist for limiting voltage transients on device gates, the most common of which are the addition of a fixed gate resistance or the addition of a Zener diode-based clamping circuit [37]. The Zener diode clamping circuit limits the voltage of transients on the gate, including potentially reducing ringing. However, that protection comes at the cost of both increased circuit complexity and the addition of the non-linear capacitance of the Zener diode. Because C_{iss} is in the picofarads range for many GaN HEMTs, the additional diode capacitance, even if small, can result

in significant increases in total gate drive capacitance. This can result in significantly increased losses in the switching circuit. Thus, it is often preferable to limit voltage transients with a simple gate resistor. The layout of a device, including the gate resistance and equivalent device parasitics, can be seen in Figure 9.

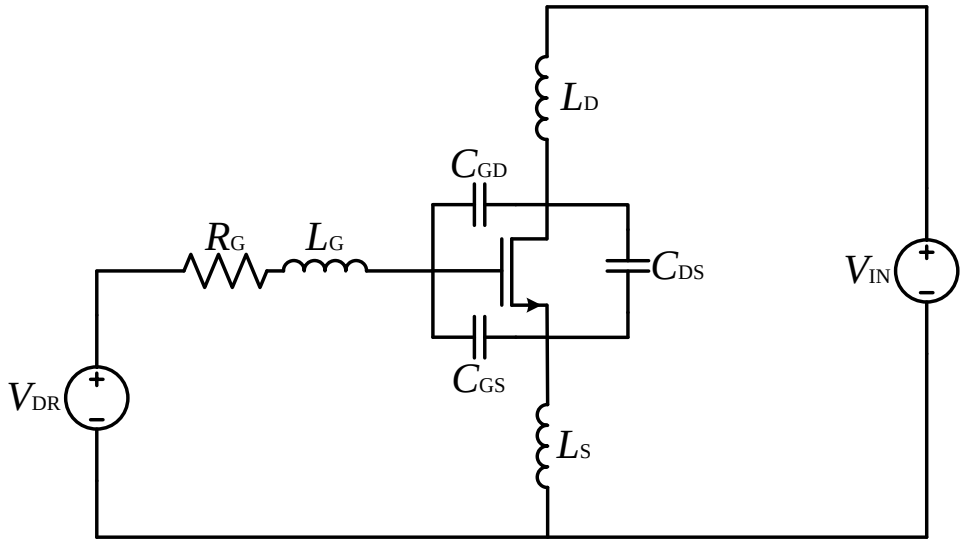


Figure 9. Circuit layout of a resistor-protected GaN HEMT illustrating device parasitics

The purpose of the external R_G is to increase the damping of the system such that the peak overshoot is reduced. This comes at the undesirable expense of increased rise time. This effect is illustrated in Figure 10, which presents three commonly observed, generic turn-on characteristics.

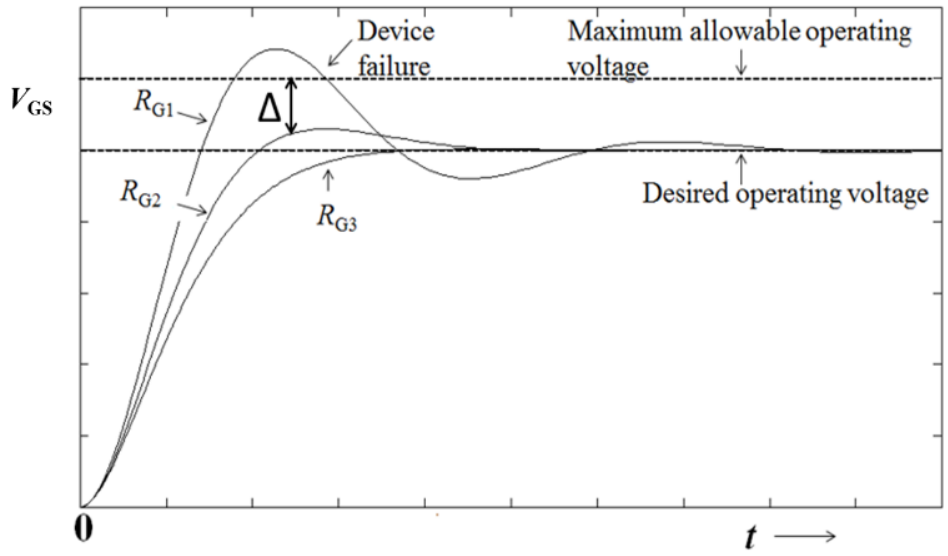


Figure 10. Commonly observed turn on characteristics for a generic device, where $R_{G1} < R_{G2} < R_{G3}$

The purpose of the external RG is to increase the damping of the system such that the peak overshoot is reduced. This comes at the undesirable expense of increased rise time. This effect is illustrated in Figure 10, which presents three commonly observed, generic turn-on characteristics. Here, $R_{G1} < R_{G2} < R_{G3}$, illustrating the trade-off in gate drive circuit design. When R_{G1} is used, the system is extremely underdamped and overshoots its steady-state operating point with fast rise time. In some cases, the overshoot can exceed $v_{GS,max}$, potentially causing device failure. When the largest resistance, R_{G3} is used, the system is close to critically damped and converges slowly to the steady-state operating point without any overshoot. Thus a design trade-off exists, in which gate overshoot can be reduced at the cost of longer rise-time of the device. Longer turn-on time corresponds to higher switching losses in the device, resulting from the extended crossover between voltage and current fall/rise times. This reduces converter efficiency and may require larger thermal management systems on both the semiconductor device and its driving circuit [38].

In order to balance switching losses with device safety, it is usually advantageous to allow for some overshoot, as long as the peak voltage does not exceed the maximum rated voltage of the device. It is convenient here to define a given turn-on curve by its safety margin, Δ, as shown in (10).

$$\Delta = v_{\mathrm{GS,max}} - v_{\mathrm{GS,peak}} \tag{10}$$

It can be seen then that there is some value of Δ that will provide the ideal balance between turn-on speed and device overshoot, as given by R_{G2} in Figure 10. Through the use of this optimal R_G value, the device turn-on is as fast as possible, with limited chance of catastrophic breakdown.

3.2 ANALYTICAL TURN ON MODEL FOR GAN HEMTS

In order to select the desired value of Δ and its corresponding R_G, the turn-on of the device must first be analyzed. The turn-on transition can be separated into three distinct sub-stages, corresponding to changes in the behavior of the device as turn-on progresses [39], [40]. The first sub-stage is the "cut-off" period, in which the gate voltage begins to increase, but before the threshold voltage is reached. In the second sub-stage, the threshold voltage has been exceeded, and the device enters saturation, acting as a current source, while the capacitances around it continue to charge and discharge. In the final sub-stage, the device enters the linear (or triode) region, acting as a resistor, while the input capacitance continues to charge. In the assumed third sub-stage model, the output capacitance of the device has been completely discharged. The equivalent circuits for sub-stages 1, 2, and 3 are given in Figure 11, Figure 12, and Figure 13, respectively [39], [40].

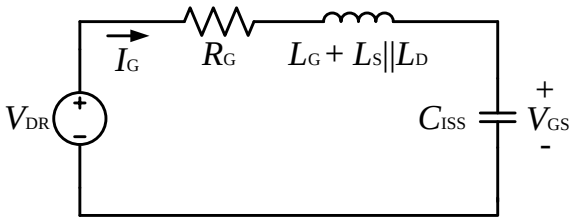


Figure 11. Equivalent circuit for sub-stage 1 of device turn on

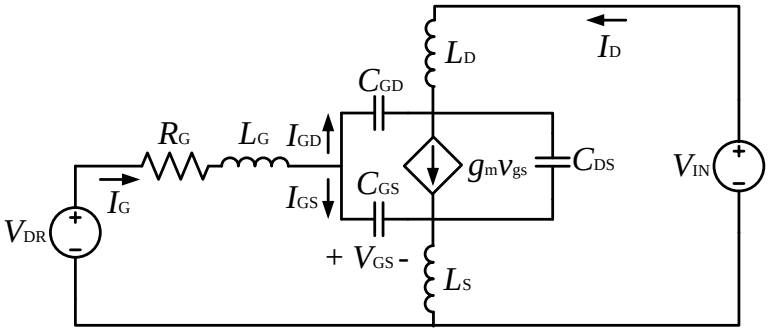


Figure 12. Equivalent circuit for sub-stage 2 of device turn on

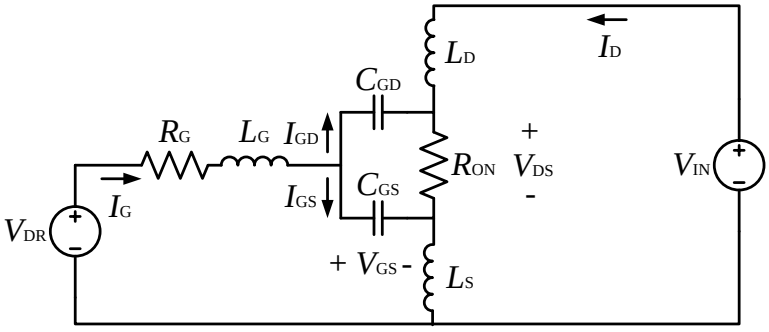


Figure 13. Equivalent circuit for sub-stage 3 of device turn on

In order to completely capture the turn-on dynamics of the device, all of the sub-stages must be analyzed. However, as the objective of this work is to determine specifically the peak overshoot, and not the complete wave-shape, simplification is possible. Specifically, circuit analysis of the three sub-stages reveals that sub-stage 1 is the least-damped of the three equivalent circuits presented in Figure 11. Therefore, sub-stage 1 is utilized to model and predict overshoot, even though overshoot occurs during sub-stage 3. This assumption results in a worst-case scenario for overshoot, and ensures that any calculated value for R_G will not allow the specified value of Δ to be exceeded. Thus, based on Figure 11, a set of equations is derived allowing engineers to select either R_G based on a desired Δ or to find the resulting value of $v_{GS,max}$ based on a selected R_G. Referring to Fig. 3(a), when V_{DR} is a step function, v_{GS} can be derived using frequency domain analysis and expressed as,

$$v_{GS}(s) = \frac{V_{DR}}{s}\left[\frac{\frac{1}{C_{iss}L_{eq}}}{s^2 + \frac{R_g}{L_{eq}}s + \frac{1}{C_{iss}L_{eq}}}\right] \tag{11}$$

where s is the Laplace variable, and L_{eq} is defined by (12).

$$L_{eq} = L_G + \frac{L_S L_D}{L_S + L_D} \tag{12}$$

Typically, this inductance is contributed by the layout of the PCB and/or the package of the device if applicable. Most GaN HEMTs, including those manufactured by EPC, do not use standard

packages on their devices; however, the inductance of the PCB and testing equipment must still be taken into account [41], [42]. The denominator of (11) can then be compared with the canonical form of second order systems, as given in (13).

$$s^2 + 2\zeta\omega_{\mathrm{n}}s + \omega_{\mathrm{n}}^2 \tag{13}$$

Here, ζ is defined to be the damping ratio and ω_{n} is the undamped natural frequency of the system. The damping ratio provides information about how much a system will overshoot its steady-state value, while ω_{n} indicates how violently the system oscillates before it settles. From inspection of (11) and (13), values for ζ and ω_{n} can be derived as shown in (14) and (15), respectively.

$$\zeta = \frac{R_{\mathrm{G}}}{2}\sqrt{\frac{C_{\mathrm{iss}}}{L_{\mathrm{eq}}}} \tag{14}$$

$$\omega_{\mathrm{n}} = \frac{1}{\sqrt{L_{\mathrm{eq}}C_{\mathrm{iss}}}} \tag{15}$$

The damping ratio also influences the maximum value of the overshoot, M_{P}, in second order systems as shown in (16) [43].

$$M_{\mathrm{P}} = V_{\mathrm{DR}}\left(1 + e^{-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}}\right) \tag{16}$$

Where, again V_{DR} is the steady-state operating voltage of the gate driver. It follows then that the right hand side of (16) should be equated with $v_{\mathrm{GS,max}} - \Delta$ as shown in (17).

$$v_{\mathrm{GS,max}} - \Delta = V_{\mathrm{DR}}\left(1 + e^{-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}}\right) \tag{17}$$

Then, from (17), ζ can be solved for as shown in (18).

$$\zeta = \frac{\frac{1}{\pi}\ln\left(\frac{V_{DR}}{V_{\mathrm{GS,max}} - V_{\mathrm{DR}} - \Delta}\right)}{\sqrt{1 + \frac{1}{\pi^2}\left[\ln\left(\frac{V_{DR}}{V_{\mathrm{GS,max}} - V_{\mathrm{DR}} - \Delta}\right)\right]^2}} \tag{18}$$

The optimal value of R_{G} can then be calculated by equating (14) with (18), and solved for if the value of C_{iss} and L_{eq} are known. The value for C_{iss} can be provided by device manufacturers, while the value for L_{eq} can be estimated by measuring ω_{n} during turn on. The value for ω_{n} is best measured by using a very small R_{G} value, so that the system is as minimally damped as possible. The resulting equation giving R_{G} for a specified Δ is presented in (19).

$$R_{\mathrm{G}} = 2\sqrt{\frac{L_{\mathrm{eq}}}{C_{\mathrm{iss}}}}\frac{\frac{1}{\pi}\ln\left(\frac{V_{DR}}{V_{\mathrm{GS,max}} - V_{\mathrm{DR}} - \Delta}\right)}{\sqrt{1 + \frac{1}{\pi^2}\left[\ln\left(\frac{V_{DR}}{V_{\mathrm{GS,max}} - V_{\mathrm{DR}} - \Delta}\right)\right]^2}} \tag{19}$$

Similarly, if a value for R_{G} is selected first, $v_{\mathrm{GS,peak}}$ can be calculated substituting (10) and (14) into (16) as given by (20).

$$v_{\mathrm{GS,peak}} = V_{\mathrm{DR}}\left(1+\exp\left(\frac{-\pi\left(\frac{R_G}{2}\sqrt{\frac{C_{iss}}{L_{eq}}}\right)}{\sqrt{1-\left(\frac{R_G}{2}\sqrt{\frac{C_{iss}}{L_{eq}}}\right)^2}}\right)\right) \tag{20}$$

Thus, this analysis provides design engineers with tools for two scenarios. If a certain safety margin is desired, (19) may be used to derive the optimal value of R_{G} necessary. However, if the designer only has a given set of resistors available, (20) may be used to find the expected overshoot for each. The result is a simple tool allowing for optimization of gate resistors based on the design constraints presented to the engineer.

3.3 EXPERIMENTAL VALIDATION WITH DOUBLE PULSE TEST CIRCUIT

In order to demonstrate the efficacy of the developed analysis tool, a hardware testbed was implemented, using a GaN HEMT in a double pulse test circuit. The circuit design is shown in Figure 14, and is similar to those presented in [44] and [45]. The device under test is once again the EPC8010 [30], while the gate driver is the LM5113 [46]. The semiconductor and IC components used in the test circuit are presented in Table 2, system and passive component parameters in Table 2. .

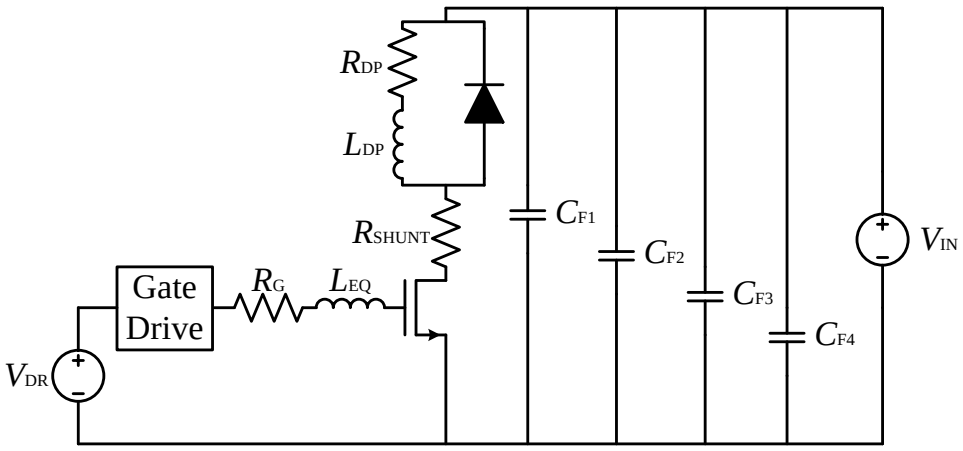


Figure 14. Double pulse test circuit for turn on measurements

Table 2. Semiconductor and IC Components

Device Type	**Parameters**		
	Part Number	***Voltage Rating***	***Current Rating***
DUT	EPC8010	100 V	2.7 A
Diode	SK310A-LTP	100 V	3 A
Driver	LM5113	100 V	

Table 3. System and Passive Parameters

Parameter	**Value**
V_{DC}	50 V
V_{DR}	5 V
R_G	1 –20 Ω
R_1	1.65 Ω
R_2	0.1 Ω
L_1	1 mH
L_{eq}	8.6 nH
C_1	1 mF
C_2	10 µF
C_3	1 µF
C_4	0.1 µF

Based on the stated parameters, a double pulse test PCB was designed and fabricated, as shown in Figure 15.

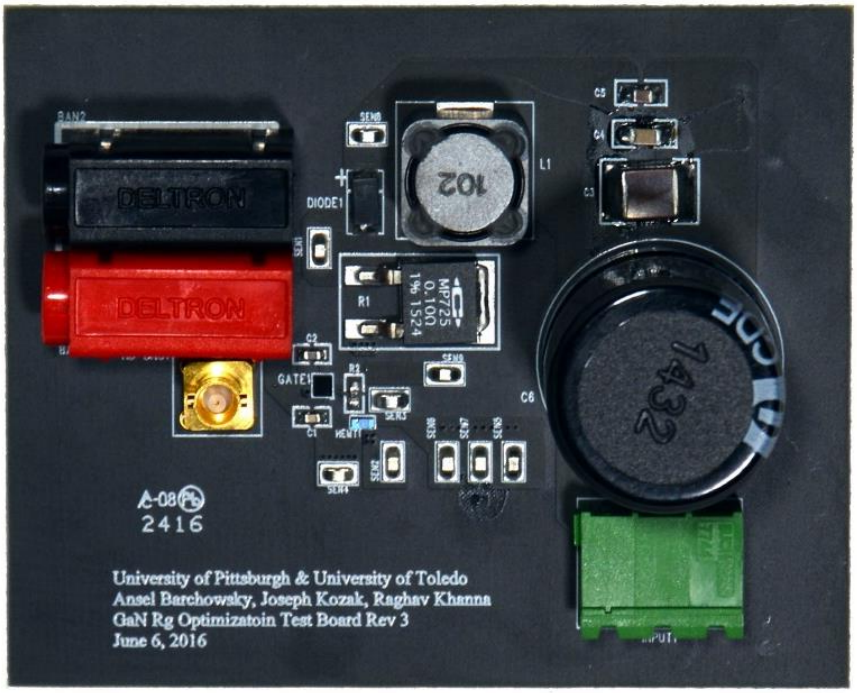


Figure 15. Double pulse test PCB for verification of R_G selection

Using this test circuit, the value for L_{eq} was experimentally determined. This was accomplished by measuring ω_n, as shown in Figure 16.

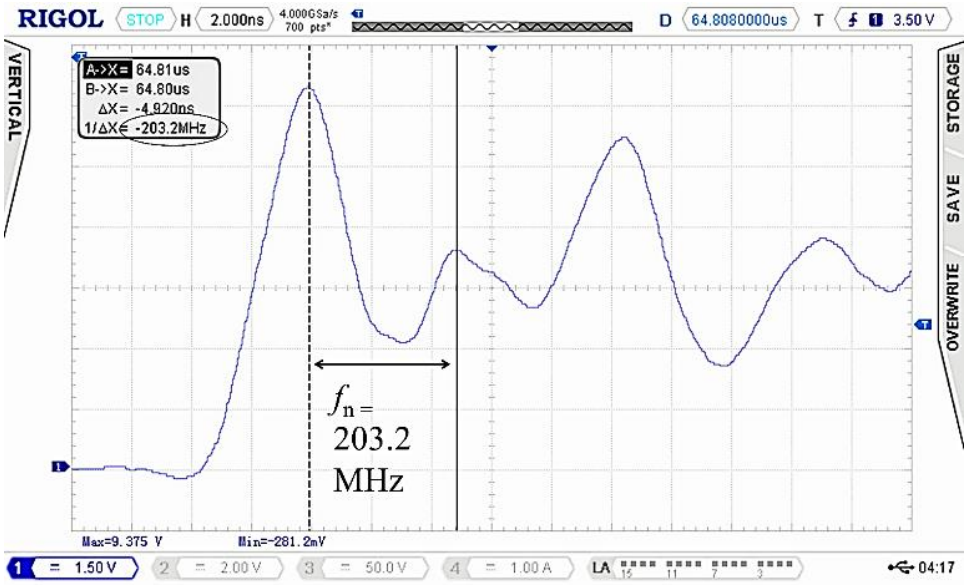


Figure 16. Un-damped measurement of v_{GS} vs t for calculation of L_{eq}

Based on the value of the input capacitance at V_{DR}, which was given by the manufacturer to be 71 pF, and using a shorted gate resistor, L_{eq} was calculated using (15) to be 8.6 nH. It should be noted that although minimization of inductance in the gate-source loop is a critical component for the proper operation of GaN HEMTs, it is not the focus of this study, and the methods presented here function regardless of the value of L_{eq}.

With all circuit parameters known, R_G for the optimal case of $\Delta = 0$ V was then calculated. Solving (19) with $\Delta = 0$ V and using the known system parameters yields a R_G value of 10 Ω, which when used in the test circuit results in the turn-on waveform shown in Figure 17.

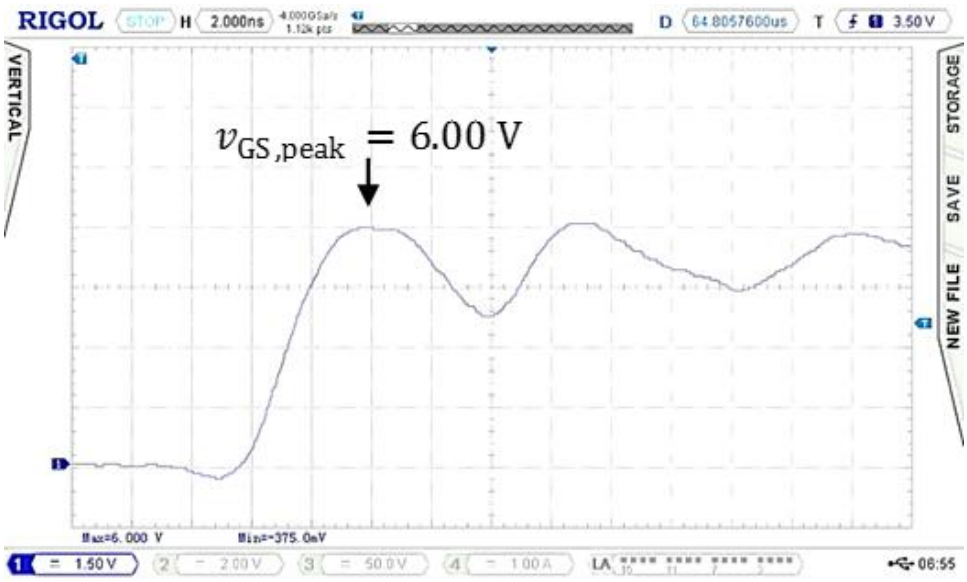


Figure 17. Turn on of EPC8010 with R_G = 10 Ω

From Figure 17, it can be seen that the value of $v_{GS,peak}$ is exactly equal to 6 V, corresponding to the desired safety margin.

Other values of R_G were inserted into the same test system in order to assess the predictive power of the relationship established in (19). The values ranged from 1 Ω to 20 Ω, including the optimal 10 Ω case, creating systems of various levels of damping. Selected turn-on transients for 5 Ω and 1 Ω are shown in Figure 18 and Figure 19, respectively.

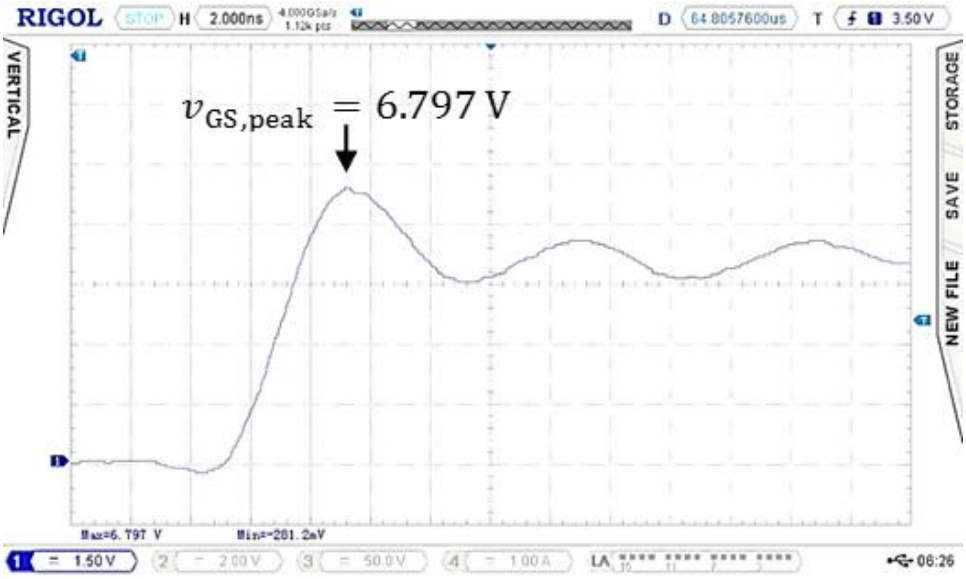


Figure 18. Turn-on of EPC8010 with R_G = 5 Ω

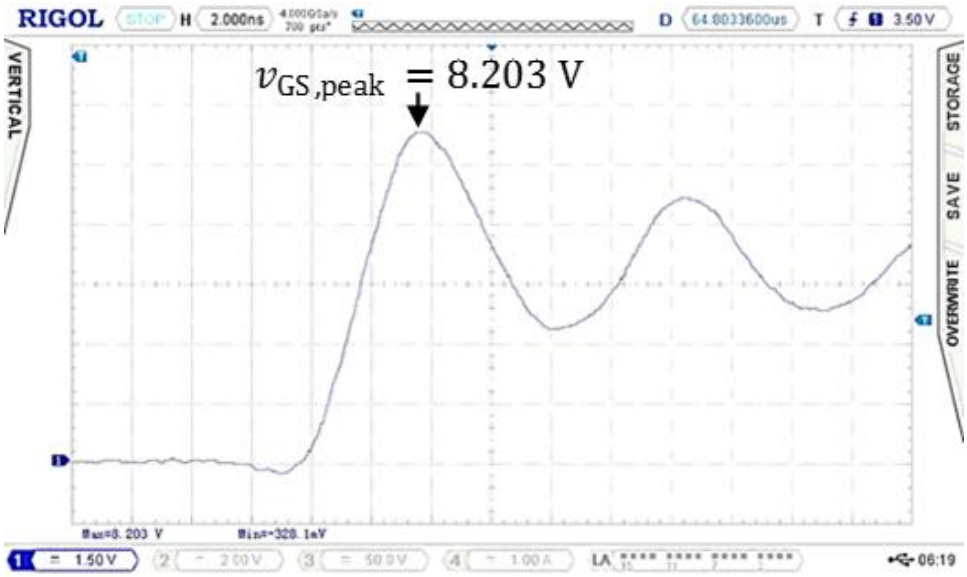


Figure 19. Turn-on of EPC8010 with RG = 1 Ω

Next, values for the expected $v_{\mathrm{GS,peak}}$ were found for each of the chosen values of R_{G} using (20) with the known system parameters. These values were then compared to the experimental results as shown in Figure 20.

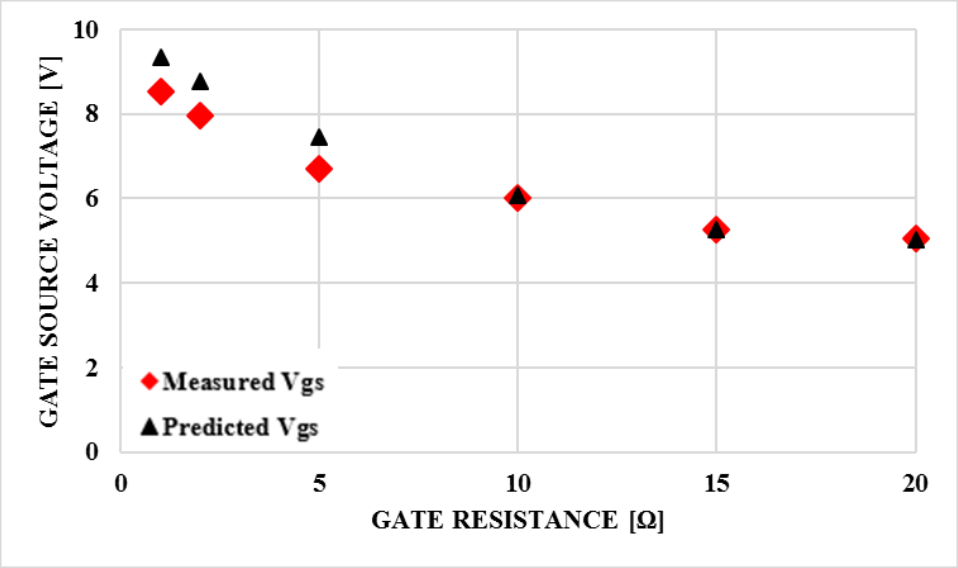


Figure 20. Predicted and measured values for v_{GS} vs R_{G}

Two key observations can be made based on these results. First, the agreement between the derived second order mathematical model and the experimental results is reasonable, with improved agreement at higher values of R_{G}. This is due to the equivalent value of R_{G} being dominated at low chosen values by parasitic resistances in the PCB and by the non-zero output impedance of the gate-drive IC. At higher values of R_{G}, the overall resistance is instead dominated by the chosen resistor. In both cases, agreement is close enough to verify that the second order model is sufficient to estimate $v_{\mathrm{GS,peak}}$ and the resulting overshoot above V_{DR}. It can also be seen that the optimal calculated resistance of $R_{\mathrm{G}} = 10\ \Omega$ results in $\Delta = 0$ V in both the modeled and

experimental cases. These results validate the ability of (19) and (20) to be used by design engineers for safe, rapid driving of GaN HEMTs either based on a selected safety margin, as in the case of the optimal 10 Ω resistance, or via calculation of predicted overshoot values based on pre-selected gate resistors.

3.4 CHAPTER SUMMARY

This chapter has presented a method for optimally selecting gate resistances utilized in driving enhancement mode GaN HEMTs. First, causes and effects of overshoot in GaN HEMTs and two potential solutions for overshoot reduction were discussed. For high-frequency GaN HEMT systems, simple gate resistance is often preferable to more complex circuit solutions.

Next, an analytical model was developed, based on a worst-case approximation of gate-source voltage transients using the equivalent circuit of sub-stage 1 during turn-on. The resulting design equations can be used in two ways. First, a safety margin can be selected for the device, yielding an optimal value of R_G which achieves the chosen safety margin with minimal resistance. Alternatively, a gate resistance can be chosen based on available values which can then be used to calculate the predicted overshoot on the device.

These two methods of analysis were then verified using a double-pulse test hardware testbed with an EPC8010 as the DUT. Variation of the gate resistance from 1 Ω to 20 Ω, using the same testbed to minimize variability, were then used to evaluate turn-on at various damping levels. Results of the un-damped system were used to calculate the equivalent inductance of the gate loop, which was then used to estimate overshoot for each of the selected resistors.

It was shown that the experimental results closely matched the values predicted by the mathematical model, converging as R_G was increased. It can therefore be seen that a second-order model for turn-on, based on the equivalent circuit of sub-stage 1, can be used to predict overshoot and optimize gate resistance values in converter design. By allowing designers to achieve safe, rapid turn on with GaN HEMTs, this work enables the reduction of switching losses in power conversion design and helps to achieve high-density power conversion.

4.0 PCB INTEGRATED PLANAR TRANSFORMERS

In high-density converter magnetics especially, PCB-based winding configurations become particularly practical. The use of a PCB allows for individual windings to be printed on each side of each layer of a board, allowing for interleaving without the typical wiring challenges in conventional transformers. The reduction in wire thickness and the added interleaving combine to reduce leakage and high frequency winding losses, which tend to dominate at high frequency. Their greater surface area to volume ratio also helps with thermal conduction around the core. These benefits do come at the cost of lower window utilization, increased footprint area, and increased parasitic capacitance. An example of a planar transformer with integrated PCB windings can be seen in Figure 21.

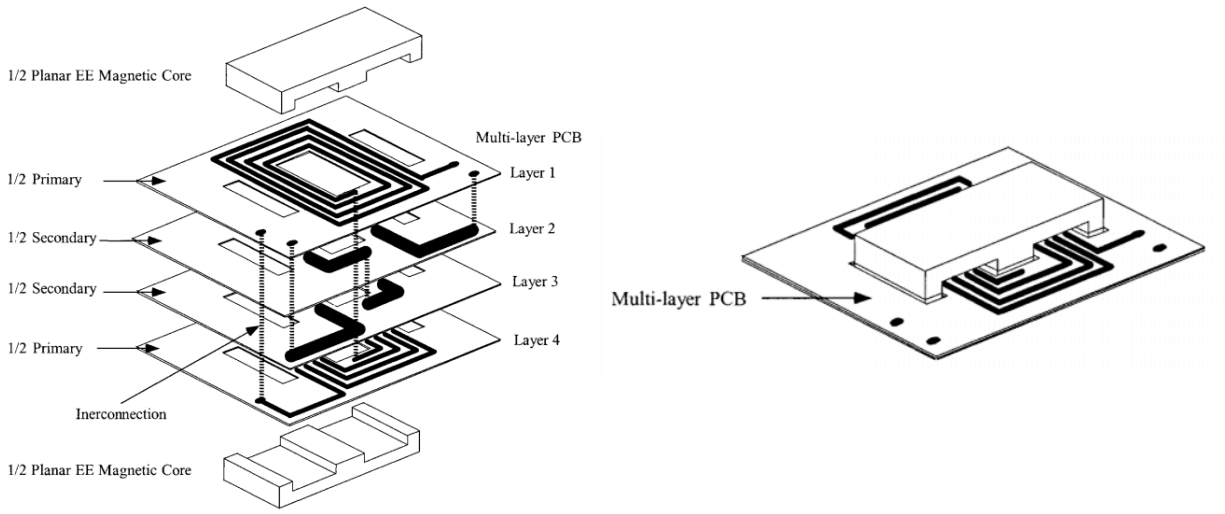


Figure 21. PCB integrated planar transformer [25]

Based on this architecture, this chapter presents the development of custom PCB integrated planar ferrite transformers. The goal is to achieve the minimal possible size for a 2 kW transformer being switched at or near 1 MHz. The result is a transformer design that is compact, repeatable, and does not saturate under the imposed converter restraints.

The selection methodology for magnetic components in power conversion electronics can be achieved through a well-established method, which is presented in [47]. The technique, known as the K_{gfe} method, compares the magnetic requirements of a given converter transformer application to the geometric limitations of a given magnetic core in order attempt to minimize the total losses of the transformer. If the converter's required K_{gfe} coefficient is less than that of the chosen transformer core, in addition to the flux density being less than the saturation point of the core, the core is suitable for the application. From that point, winding calculations and copper area allocations are performed, based on the switching frequency of the converter and the current ratings of the primary and secondary windings. The following analysis will use the table of coefficients given in Table 4.

Table 4. Transformer parameters for power converter development

Parameter	***Symbol***	***Unit***
Maximum flux density	B_{max}	T
Optimum flux density	B_{opt}	T
Applied primary volt-seconds	λ_1	Vs
Core loss	P_{Fe}	W
Core loss frequency coefficient	K_{Fe}	$W/T^{\beta}cm^3$
Core loss frequency exponent	α	
Core loss flux density exponent	β	
Applied voltage on the primary winding	v_1	V
Applied RMS voltage on the primary winding	V_1	V
Switching frequency	f_{sw}	Hz
Equivalent re-magnetizing frequency	f_{eq}	Hz
Wire effective resistivity	ρ	Ωcm
Window fill factor	K_u	
Winding loss	P_{Cu}	W
Total transformer loss	P_{tot}	W
RMS current value of the current through a winding	$I_{1,2}$	A
Total RMS current, referred to primary	I_{tot}	A
Core cross-sectional area	A_C	cm^2
Core volume	V_C	cm^3
Mean length per turn	MLT	cm
Core window area	W_A	cm^2
Magnetic path length	l_m	cm
Skin depth	δ	μm
Permeability of free space	μ_0	H/cm
Relative permeability	μ_r	

In order to properly model the core, the losses in the core must first be understood and compared to the winding losses in order to minimize total loss. Losses in magnetic cores can be estimated by the Steinmetz equation, originally presented by Charles Steinmetz in 1894, for which the general form is given in (21) [48], [49]:

$$P_v = C_m f^{\alpha} \hat{B}^{\beta} \tag{21}$$

Using the Steinmetz equation and the K_{GFE} method, core can be sized for power electronic converter applications and the expected flux density can be determined to ensure that the core does not saturate during converter operation.

4.1 CORE SIZE DETERMINATION AND MATERIAL PARAMETER EXTRACTION

In (21), P_v is the power losses per volume, f is the remagnitization frequency, and $\hat{B}$ is the peak induction. These quantities are then fit to the known loss data via three empirical parameters, as described in [49]. To fit into the K_{gfe} method described previously, this expression has been extended modified as presented in [47], taking into account geometric conditions of the core in addition its material parameters, resulting in:

$$P_{Fe} = K_{Fe} B_{max}^{\beta} A_C l_m \tag{22}$$

K_{fe} and β are extracted parameters from the manufacturers datasheet curves for the core material, while A_C and l_m are characteristics of the core size itself. However, as discussed in [49], the Steinmetz equation is only applicable for sinusoidal primary voltage excitations, as it does not properly capture the re-magnetization losses from non-sinusoidal flux waveforms, as a result of the influence of the dynamic hysteresis curves imposed by such excitations. In order to correct for dynamic change in induction over a remagnitization cycle, [48] presents an averaging technique, where,

$$\dot{B} = \frac{1}{\Delta B}\int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{23}$$

However, while (23) accurately captures the averaged remagnitization rate for non-sinusoidal excitations in magnetic components, for calculation of power losses is must be modified to be usable in a modified Steinmetz equation. To do so, [50] normalizes (23) over a sinusoidal period, using the normalization constant given in (24).

$$f_{eq} = \dot{B} \cdot \left(\frac{2}{\Delta B \pi^2}\right) \tag{24}$$

Using this expression, a modified Steinmetz expression can be derived, based on the equivalent frequency of the normalized average remagnitization rate found in (24) and the frequency with which remagnitization repeats, f_r [48]. The resulting loss expression is given by

$$P_v = \left(C_m f_{eq}^{\alpha-1} \hat{B}^{\beta}\right) f_r \tag{25}$$

As for the traditional Steinmetz equation, this expression must be modified in order to correlate with the K_{gfe} geometric method of selecting transformer cores. By including the geometric characteristics of the chosen transformer core, (24) can be re-written as:

$$P_{Fe} = K_{Fe} f_{eq}^{\alpha-1} B_{max}^{\beta} A_C l_m f_{sw} \tag{26}$$

Here, f_{eq} is again the equivalent frequency of remagnitization, with the average induction normalized as described in (23) and (24) and *B* expressed in terms of *V, f_{sw}, and λ.*

$$f_{eq} = \frac{2V_1^2}{\pi^2 f_{sw} \lambda_1^2} \tag{27}$$

which, when substituted into (26), yields:

$$P_{Fe} = K_{Fe}\left(\frac{2V_1^2}{\pi^2 f_{sw}\lambda_1^2}\right)^{\alpha-1} B_{max}^{\beta} A_C l_m f_{sw} = K_{Fe}\left(\frac{2V_1^2}{\pi^2 \lambda_1^2}\right)^{\alpha-1} B_{max}^{\beta} A_C l_m f_{sw}^{2-\alpha} \tag{28}$$

In order to evaluate this expression, the values of K_{fe}, α, and β must first be extracted from the manufacturers datasheet. This is done by curve fitting the specific core loss plot shown in Fig. 36 for various excitation frequencies. The expression used to curve fit is the traditional Steinmetz, as the excitations used to extract core losses, as shown previously in Figure 7. The curves were fit using linear regression, resulting in the curves shown in Figure 22 and the extracted Steinmetz values give in Table 5.

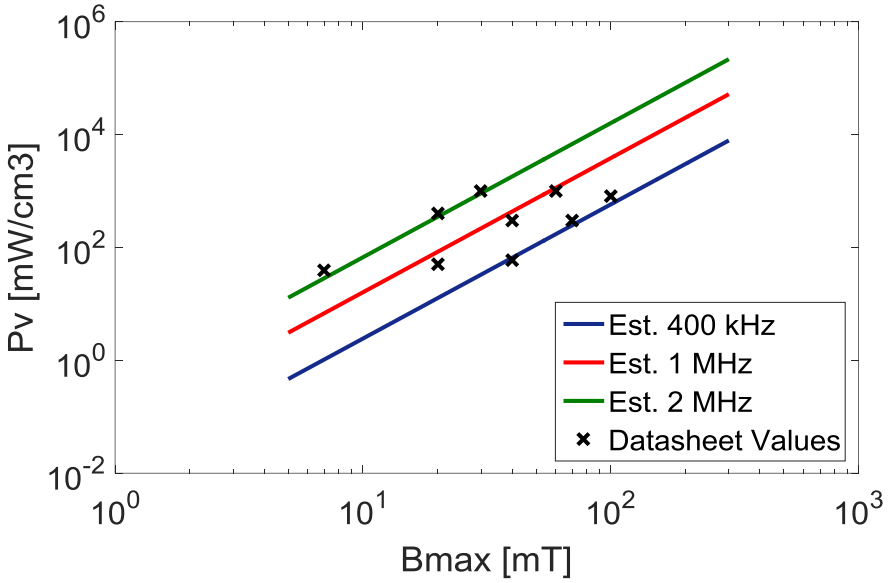


Figure 22. Matched core loss data for Ferroxcube 3F4 MnZn ferrite

Table 5. Extracted core parameters for Ferroxcube 3F4 MnZn ferrite

Parameter	Value	Units
K_{fe}	3.92E-10	$W/T^{\beta}cm^3$
α	2.0608	
β	2.377	

The winding loss for the converter was then estimated, based on the core dimensions and the available area for copper windings. The value is based on dimensions of the core, the current in the converter, and the resistivity of pure copper, as given by:

$$P_{Cu} = \left(\frac{\rho\lambda^2 I_{tot}^2}{4K_U}\right)\left(\frac{MLT}{W_A A_C^2}\right)\left(\frac{1}{B_{max}^2}\right)^2 \tag{29}$$

The total current, I_{tot}, describes the current flowing in both the primary and secondary windings, referred to the primary side of the transformer, as given by:

$$I_{tot} = I_1 + \frac{n_2}{n_1} I_2 \tag{30}$$

Based on these calculations and the extracted core parameters, the winding losses are evaluated, and are used along with the core losses to find the requisite and core geometrical constants. The ideal operating point of the transformer is when the total loss in the converter is at a minimum. That is, the derivatives of the core loss and winding loss are equal and opposite. From that condition, equations are derived in [47] to describe the two geometrical constants for the transformer. First, the required core geometrical constant for the power electronics converter is calculated based on:

$$K_{gFe,req} = \frac{\rho\lambda^2 I_{tot}^2 \left(K_{fe} f_{sw}^{\alpha}\right)^{2/\beta}}{4K_U P_{tot}^{\beta+2/\beta}} \cdot 10^8 \tag{31}$$

Next, the geometrical constant of the core itself was calculated based on:

$$K_{gFe,core} = \frac{W_A (A_C)^{2(\beta-1)/\beta}}{MLT \cdot l_m^{2/\beta}} \left[\left(\frac{\beta}{2}\right)^{-\frac{\beta}{\beta+2}} + \left(\frac{\beta}{2}\right)^{\frac{2}{\beta+2}} \right]^{\frac{\beta+2}{-\beta}} \tag{32}$$

Finally, the optimal flux density was calculated and compared to the maximum flux density of the ferrite material at 100 ˚C. The optimal flux density is given by:

$$B_{opt} = \left[10^8 \left(\frac{\rho \lambda^2 I_{tot}^2}{4K_U}\right) \left(\frac{MLT}{W_A A_C^2}\right) \left(\frac{1}{K_{Fe} \left(\frac{2V_1^2}{\pi^2 \lambda_1^2}\right) V_C f_{sw}^{2-\alpha} \beta} \right) \right]^{\frac{1}{2+\beta}} \tag{33}$$

This is an iterative process. If the chosen core is not sufficiently large for the given application, a new core must be chosen. Likewise, if the chosen core results in a flux density greater than the saturation point of the ferrite material, a larger core must be selected. The core selected for this application was the Ferroxcube E43/10/28 [51].

Once the core is chosen, the number of primary and secondary turns can be calculated based on the optimal flux density, as given by (34) and rounded up:

$$n_1 = ceil\left(\frac{\lambda_1}{2\beta_{opt} A_C}\right) \tag{34}$$

The secondary winding number can be simply obtained via the turns ratio:

$$n_2 = n_1 \cdot \frac{n_j}{n_1} \tag{35}$$

For this application there are 3 primary turns and 1 secondary, handling 4A and 12A, respectively. An additional design, using 12 primary turns and 3 secondary turns is also designed, providing an anticipated reduction in flux density experienced within the core at the expense of higher winding resistance and therefore higher winding losses.

DC currents of the expected magnitude could be carried in 140 µm copper without uneven current spreading through the conductor. However, in high frequency applications, the skin depth of copper paths must be taken into account. The skin depth for copper can be calculated using:

$$\delta = \sqrt{\frac{\rho}{\pi \mu_0 f_{sw}}} \tag{36}$$

For copper at 1 MHz, this value is approximately 66 µm. For planar transformer applications, the thickness of the trace must be less than twice the skin depth to minimize eddy current losses and thermal rise in the PCB's copper traces [52]. Thus, 140 µm copper cannot be used, and 70 µm is used in its place. However, due to the resulting loss of copper volume when using 70 µm copper thickness, parallel windings must be introduced on other PCB layers. From [25], it can be seen that the recommended limit for current density in 70 µm copper in power conversion applications is approximately 2000 A/cm^2.

4.2 FINITE ELEMENT MODELING OF TRANSFORMER DESIGNS

In order to verify the analytical designs presented in the previous section, finite element analysis (FEA) simulation tools were used to evaluate the transformers with a number of winding and core conditions. The simulation tool used in this case was ANSYS Maxwell, which solves Maxwell's equations over surfaces designed to minimize computational time in both 2D and 3D simulated environments. The objective here is to evaluate many winding configurations for the cores and many core configurations for the transformers.

In planning the modelling of 2D transformers, picking the right cross section of the core and windings is extremely important to attaining the proper results through simulation. For planar transformers, a cross section cut horizontally across the core is appropriate, capturing cross sections of all windings and the core window areas [53]. For the 2D modeling, three key fields were examined. First, the current density of the windings was examined. Next, the magnetic field through the entire system, including the air around the core was plotted. Finally, the magnetic flux density in the core was plotted.

For the core modeled in this work, the dimensions of the Ferroxcube E43/10/28 and the characteristics of the Ferroxcube 3F4 MnZn ferrite were imported into Maxwell for use in analysis. The core was constructed using parallel windings as previously described. Two cases were tested, first with two sets of parallel windings, next with four sets of parallel windings. Windings were modeled using PCB 2oz copper material, and the PCB was modeled using FR4-Epoxy.

In order to determine the best interleaving method for the primary and secondary windings, each case was constructed with multiple winding patterns. The objective was to minimize the current density in each path, ensuring that it was under the maximum of 2000 A/cm^3 and preferably under 1000 A/cm^3. Higher current densities lead directly to greater loss and higher heat dissipation

requirements in the windings, and interleaving is an excellent method to alienate such stress. The results for the various cases can be seen in Figure 23. The results from the simulation show that for case 1, interleaving pattern 4 provides the lowest current density and for case 2, interleaving pattern 2 provides the lowest current density. However, it can be clearly seen that case 2 provides overall lowered current densities. As a result, case 2, interleaving pattern 2 was selected for 3D modeling.

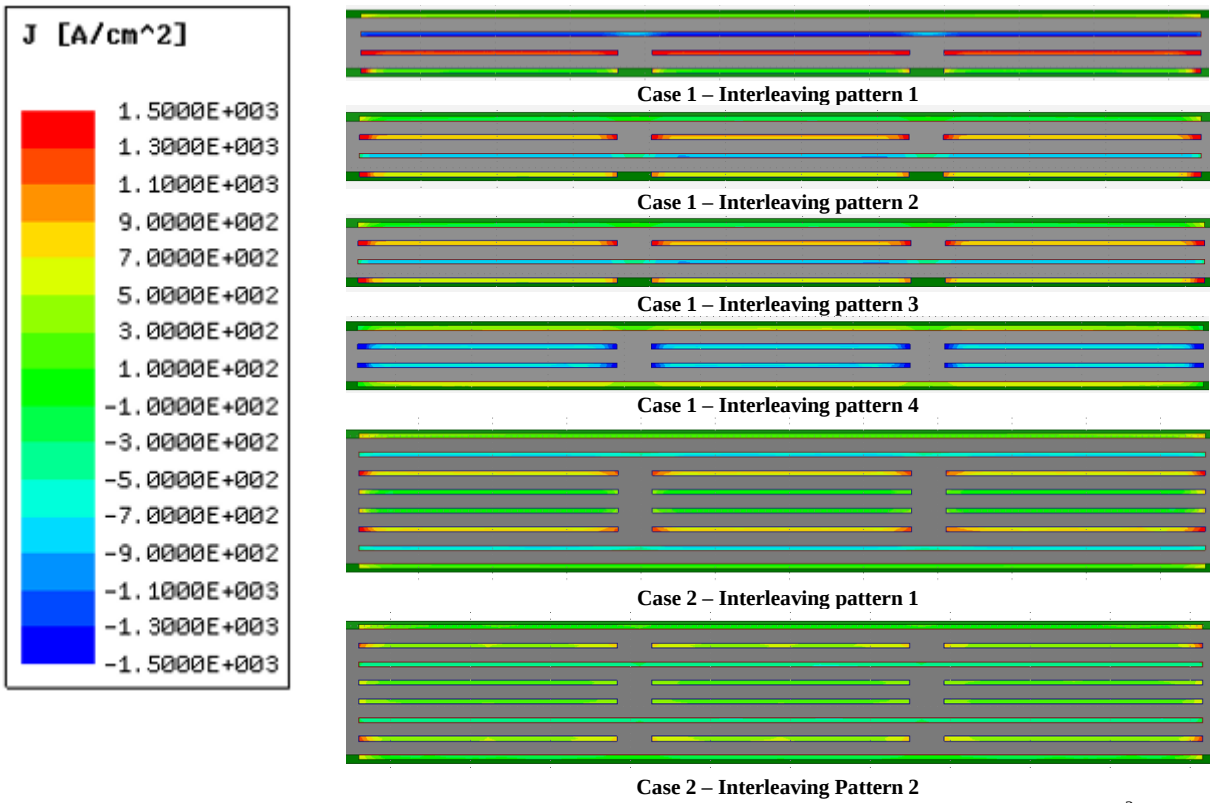


Figure 23. Current densities for various winding cases and interleaving patterns in A/cm^3

In order to accurately extract leakage inductance, magnetizing inductance, and capacitive circuit elements, 3D modeling was performed. The 3D model for the core was generated by first designing the windings and core shape in Solidworks, representing connections between PCB layers as solid copper bars. While this will result in slightly lower capacitance and inductance than true via modeling, it drastically reduces the number of curved surfaces requiring FEA meshing, speeding up simulation significantly. The Solidworks models for the primary winding, the secondary winding, and the core can be seen in Figure 24, Figure 25, and Figure 26, respectively.

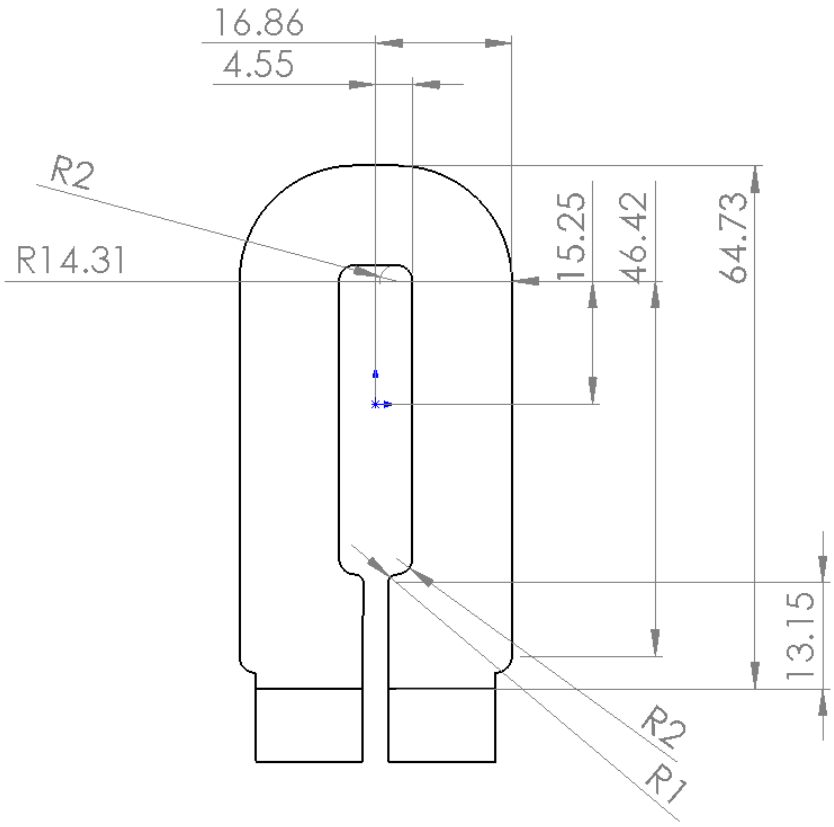


Figure 24. Solidworks drawing of transformer primary winding

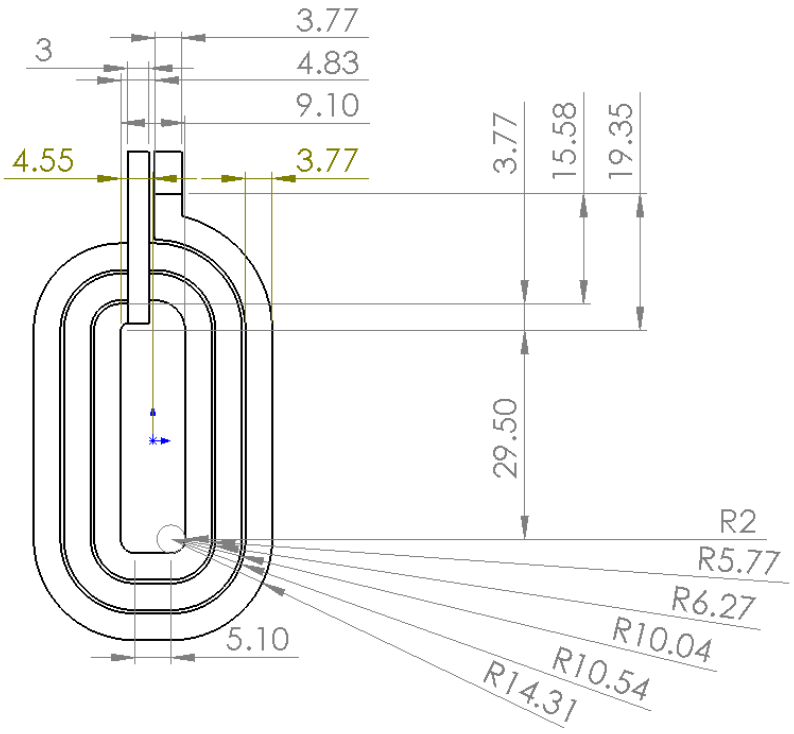


Figure 25. Solidworks drawing of transformer secondary winding

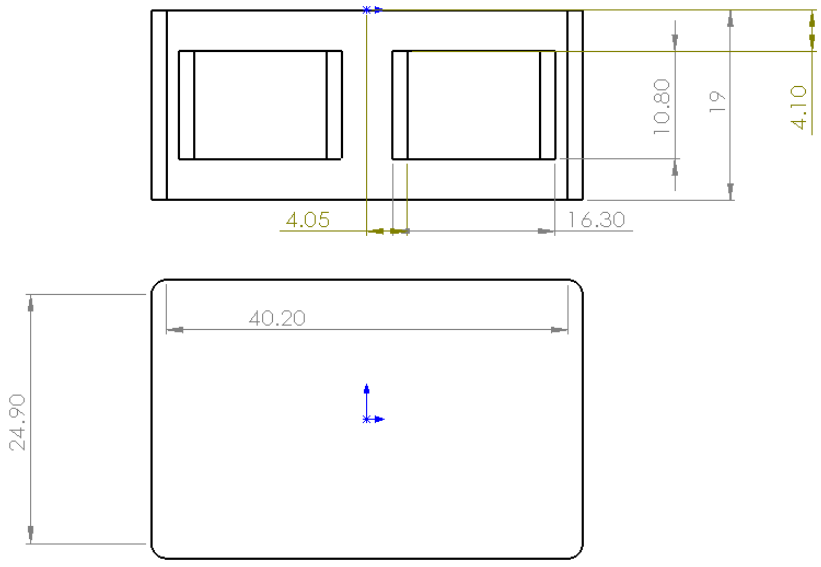


Figure 26. Solidworks drawing of paired E43/10/28 cores

These models were imported along with insulation layers into ANSYS MAXWELL for 3D FEA transient analysis. The resulting 3D model for the transformer can be seen in Figure 27.

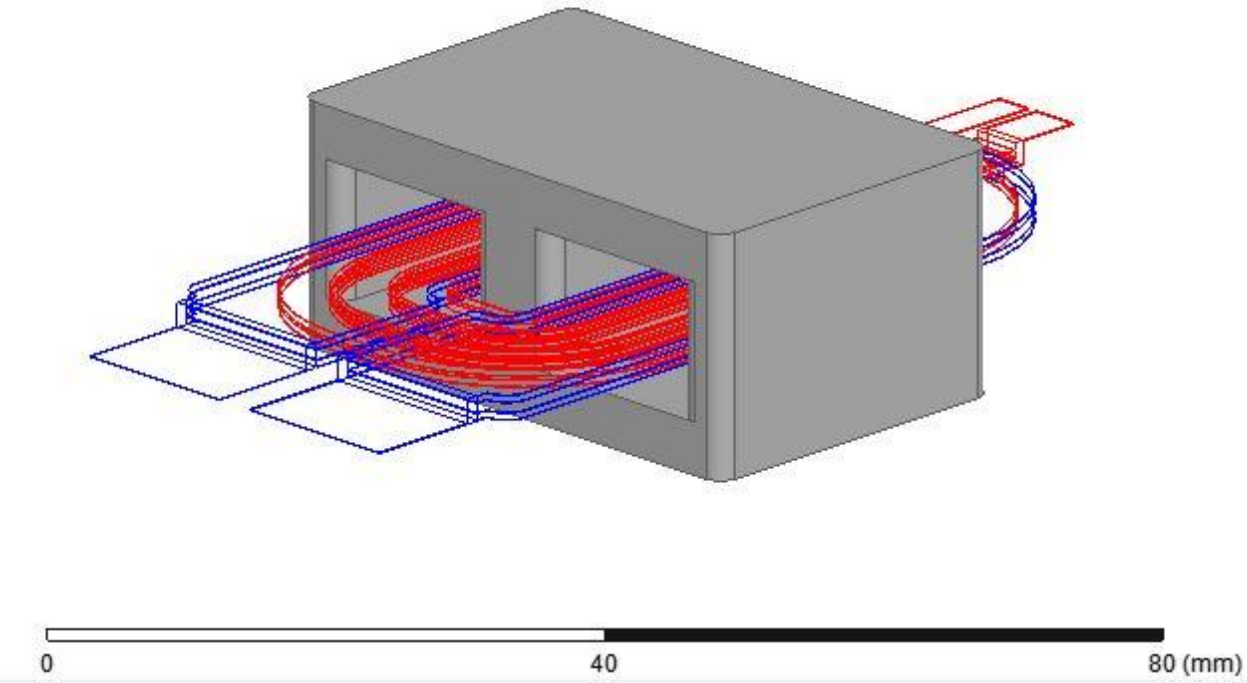


Figure 27. 3D model of planar transformer core with PCB integrated parallel windings

The system was excited utilizing an external excitation circuit and loaded using a 2 kW equivalent resistor. The system was first excited using a 200 V_{RMS} sinusoidal waveform, solving on a timeframe of 0 – 2 µs at 1 ns timesteps. The resulting voltage and current for the low-voltage primary winding are shown in Figure 28 and for the high-voltage secondary winding in Figure 29.

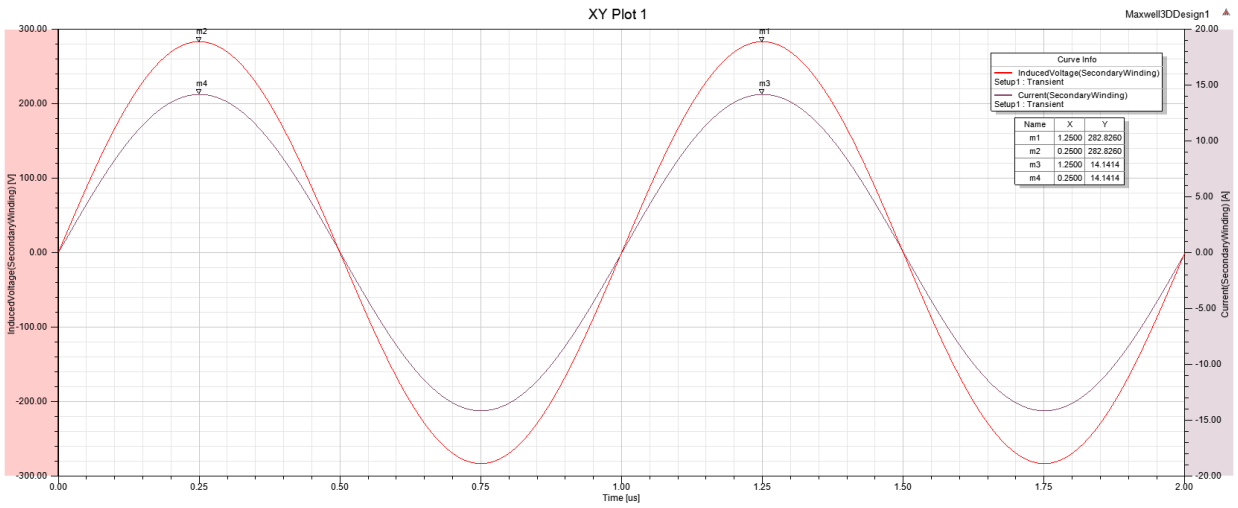


Figure 28. Primary (low-voltage) voltage and current waveforms with 200 V sinusoidal excitation and 2 kW resistive load

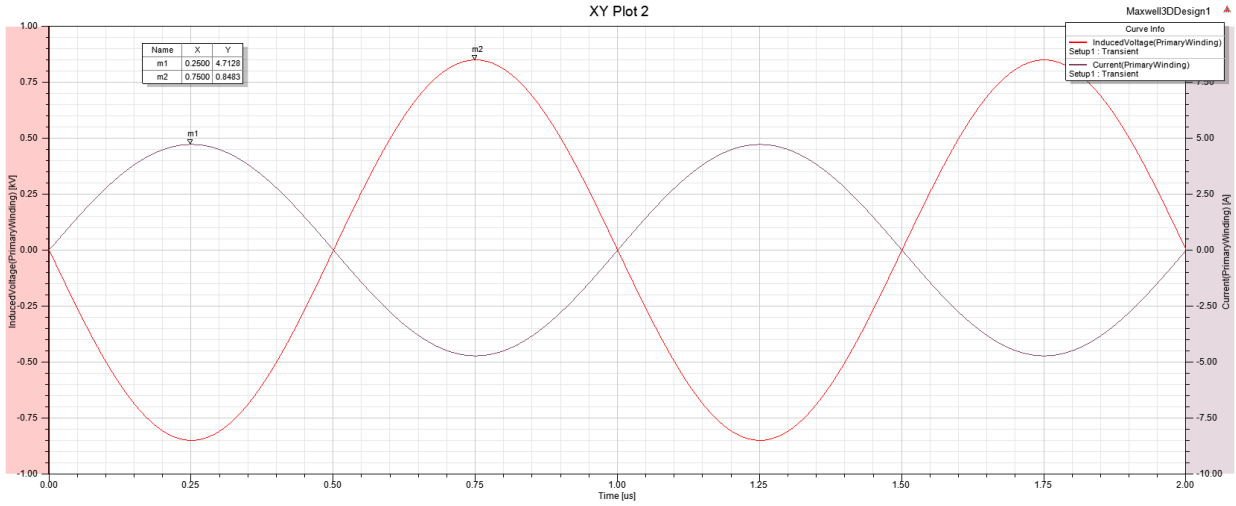


Figure 29. Secondary (high-voltage) voltage and current waveforms with 200 V sinusoidal excitation and 2 kW resistive load

The results from the sinusoidal excitations were used to verify that the transformer was performing as expected. The results indicate that the transformer model is properly converting the 200 V, 10 A input to the desired 600 V, 3.3 V output with minimal losses.

Next, the system was energized using a 200 V_{RMS} square waveform, solving on a timeframe of 0 – 2 µs at 1 ns timesteps. The resulting voltage and current for the low-voltage primary winding are shown in Figure 30 and the high-voltage secondary winding in Figure 31.

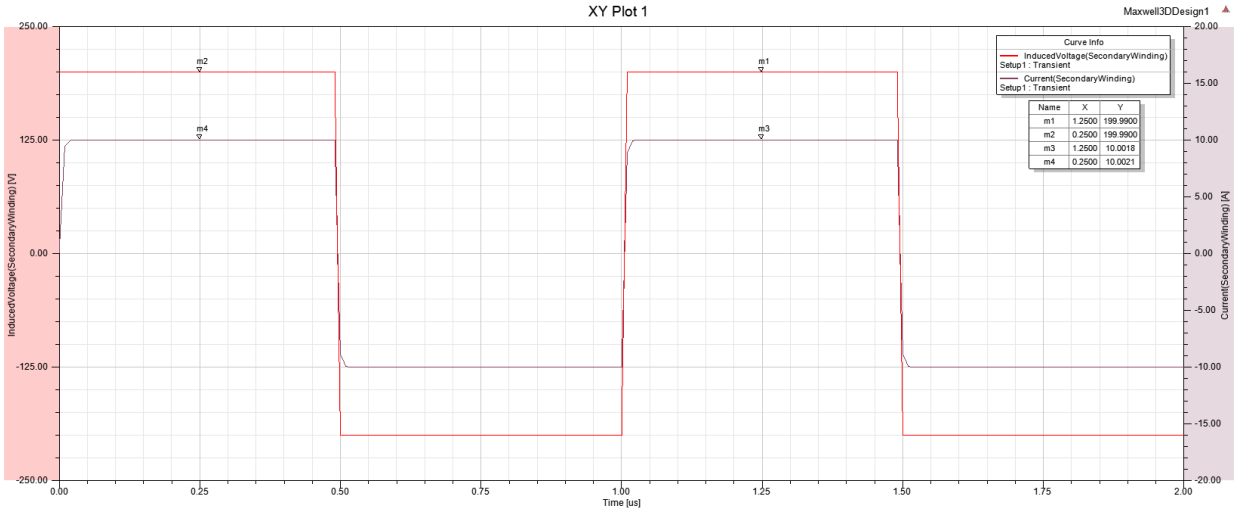


Figure 30. Primary (low-voltage) voltage and current waveforms with 200 V square excitation and 2 kW resistive load

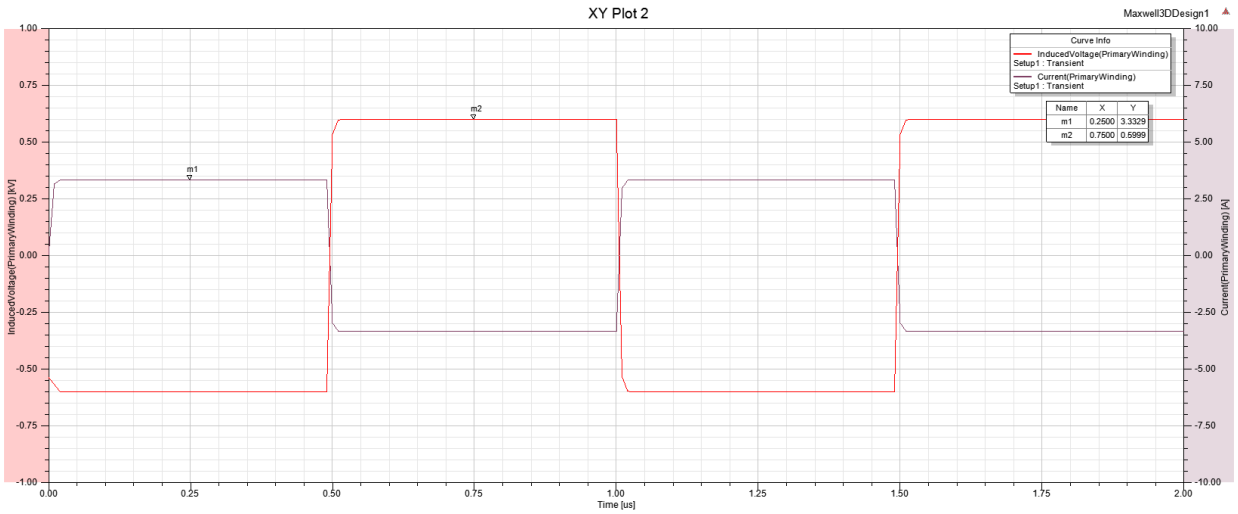


Figure 31. Secondary (high-voltage) voltage and current waveforms with 200 V square excitation and 2 kW resistive load

In addition, the flux through the core for flux is shown for high and low levels based on the point on the waveform. High flux is experienced near the end of the square wave, while low flux is experienced near the rising and falling edges of the waveform. A snapshot of the high flux can be seen in and the low flux case can be seen in Fig. 50.

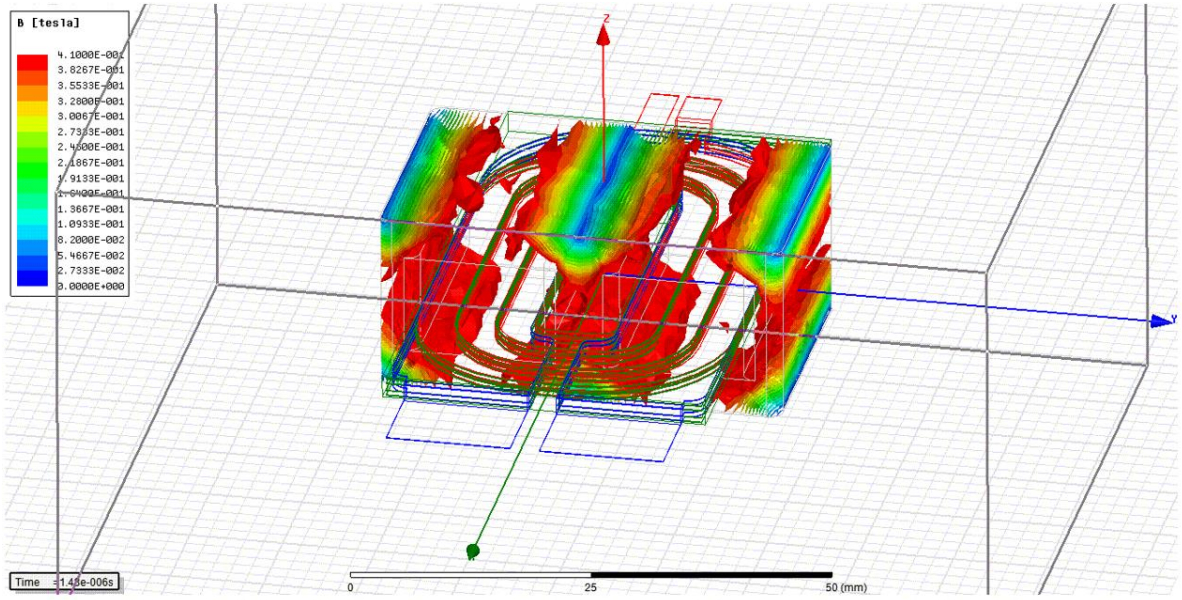


Figure 32. Highest flux point in the core when excited by 200 V square wave

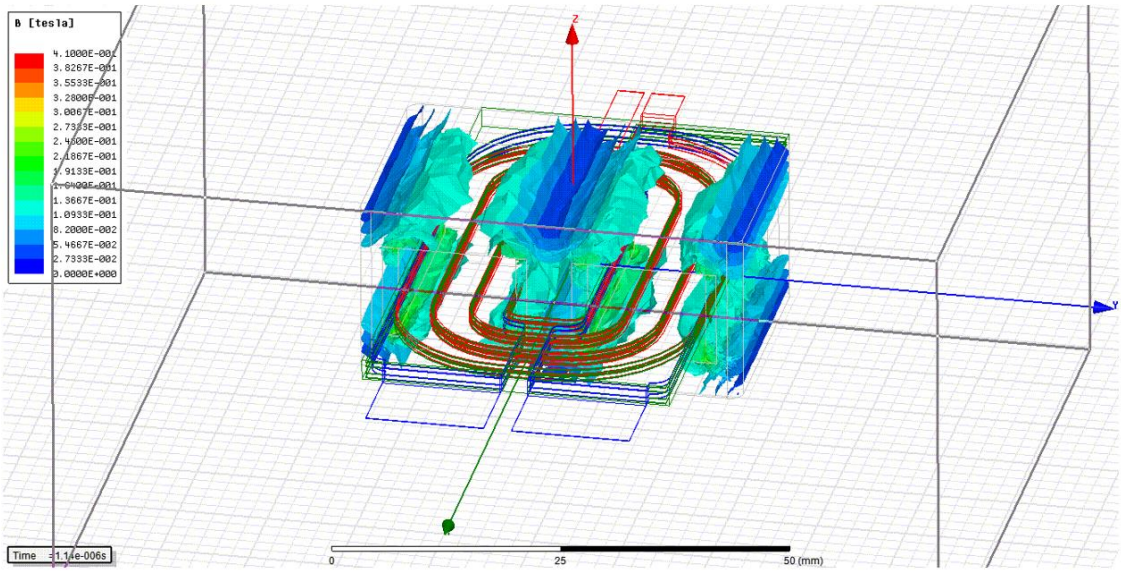


Figure 33. Lowest flux point in the core when excited by 200 V square wave

Unfortunately, these results indicate that the core saturates every cycle, which means that the current design is not suitable for the converter. However, series connecting of the windings can be used to reduce the flux density in the core at the expense of slightly higher winding losses and resistances. Thus, in order to reduce the flux within the core, the series transformer system shown in Figure 34 has been developed. With this topology, the core no longer saturates during the AC cycle of the system.

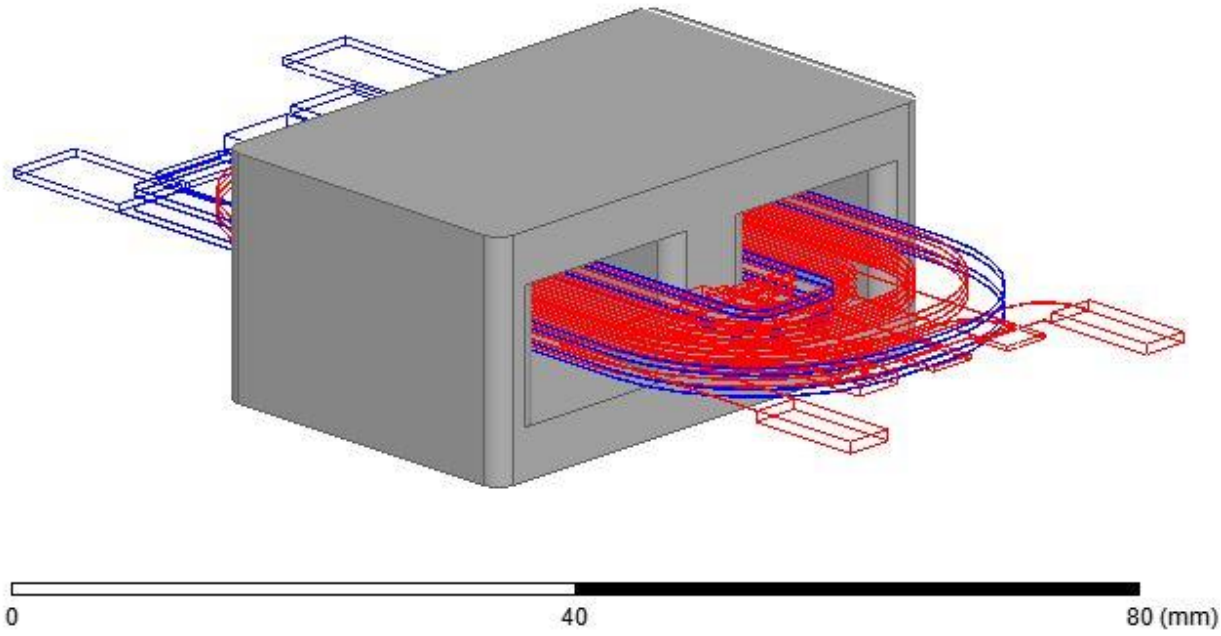


Figure 34. 3D model of planar transformer core with PCB integrated series windings

From the 3D model, ANSYS Maxwell can be used to extract equivalent circuit parameters for use in simulation circuits. The extracted parameters for the equivalent circuit are given in Table 6. The equivalent circuit used was based on the circuit shown in Figure 35 [25].

Table 6. Extracted equivalent circuit values for series planar transformer design

Parameter	Value	Units
C_{self}	97.74	pF
C_{mutual}	677.84	pF
$R_{primary}$	0.013	Ω
$R_{secondary}$	0.122	Ω
$L_{primary}$	137.9	nH
$L_{secondary}$	312.3	nH
$L_{m,primary}$	240.9	µH
$R_{m,primary}$	1051	Ω

Table 7. Extracted equivalent circuit values for parallel planar transformer design

Parameter	Value	Units
C_{self}	102.3	pF
C_{mutual}	724.3	pF
$R_{primary}$	0.0091	Ω
$R_{secondary}$	0.11	Ω
$L_{primary}$	43.96	nH
$L_{secondary}$	162.3	nH
$L_{m,primary}$	225	µH
$R_{m,primary}$	1021	Ω

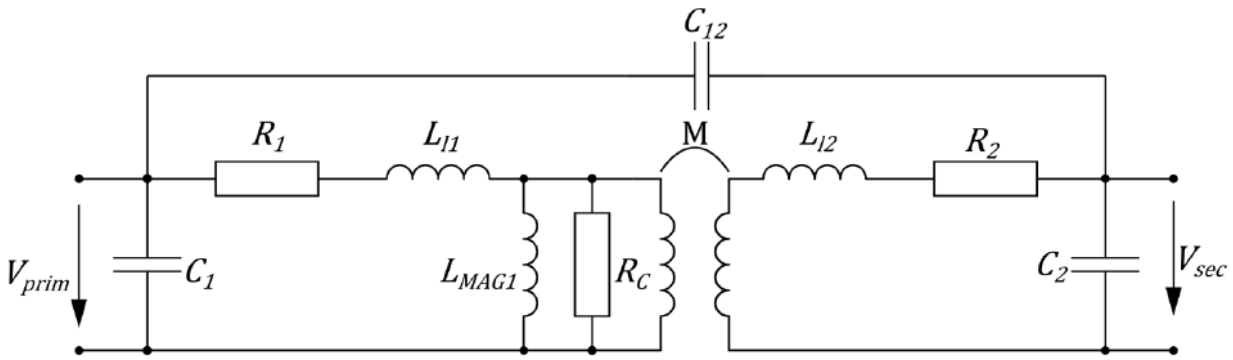


Figure 35. Equivalent circuit model for planar transformer

4.3 PRINTED CIRCUIT BOARD IMPLEMENTATION

In order to verify the results determined through simulation, prototype printed circuit boards have been designed and produced. Based on the results indicating that the E43 core saturates under square excitations, two sets of PCBs were designed. The first, as simulated and discussed previously, is based on the E43/10/28 core in the Ferroxcube 3F4 MnZn material. The second is the same material in a larger core size to mitigate peak flux levels experienced during excitation.

Both test setups are designed as required to perform the requisite tests to determine impedance characteristics of the primary and secondary sides, as specified by [54]. Primary side characteristics can be determined through primary side evaluation with an unloaded secondary. Secondary side characteristics can be determined through primary side evaluation with the secondary side loaded. Coupling capacitance between the primary and secondary can be determined via excitation of both primary terminals with identical waveforms while grounding the secondary. Capacitance between terminals on the primary side can be determined via excitation of the positive primary terminal while grounding all remaining terminals. Likewise, for the secondary

the capacitance between terminals can be determined by exciting the positive secondary terminal while grounding all remaining terminals.

In order to fulfill all test conditions, two PCBs have been developed, one for each core with the following combination of core sizes: two core halves combined, one gapped core half and one un-gapped half, one core half and a core plate. All of the core combinations share common winding configurations. For the E43/10/28 board, an example can be seen in FIG. Each board has 10 layers, of which there are 4 primary, 4 secondary, and 2 transfer. These alternate between primary and secondary windings, with two transfer layers on the innermost layers to connect the secondary windings to the transformer output.

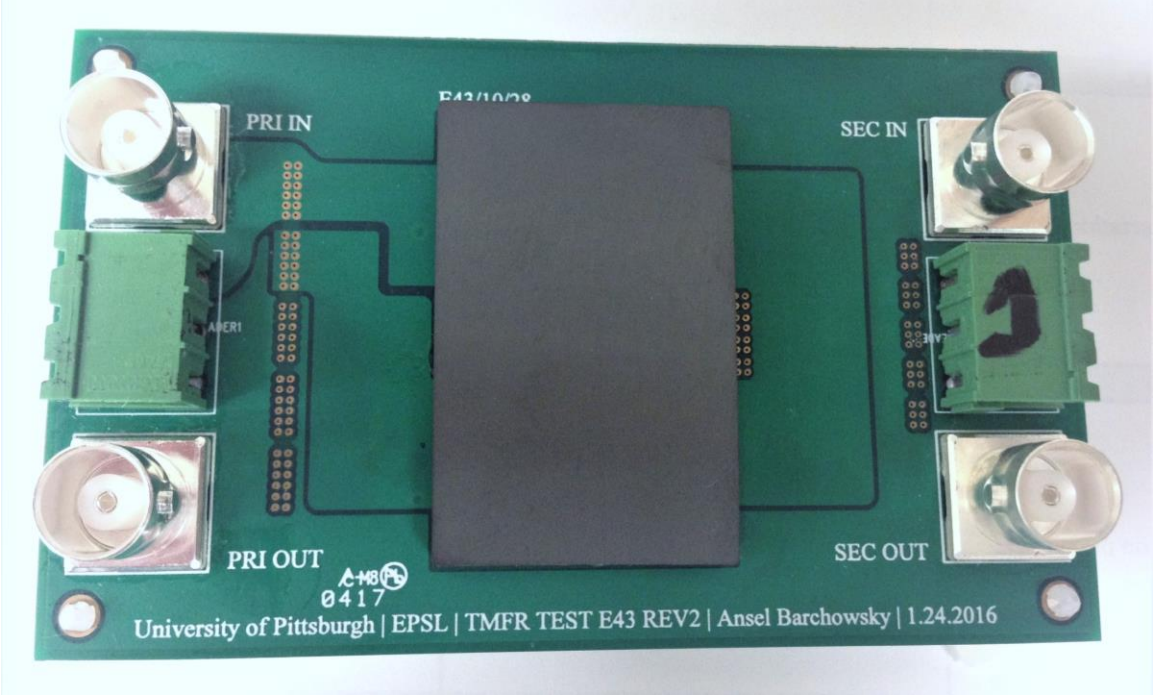


Figure 36. Prototype transformer PCB with layer-integrated windings

From impedance analysis on the test core, the parameters shown in Table 8 were extracted They can be seen to closely match the results presented in Table 6, with the exception of the winding resistance of the primary and secondary, which are both nearly an order of magnitude larger than the simulated value. Investigation is ongoing to determine the cause of the added resistance, but the remainder of the values closely match those that are expected from the simulation model of the transformer. This suggests that both the FEA model of the transformer is accurate and that based on previous simulations the flux density in the prototype cores should not saturate during converter operation.

Table 8. Extracted parameters from E43/10/28 prototype transformer

Parameter	Value	Units
C_{self}	160	pF
C_{mutual}	821	pF
$R_{primary}$	0.132	Ω
$R_{secondary}$	1.24	Ω
$L_{primary}$	176	nH
$L_{secondary}$	498	nH
$L_{m,primary}$	351	µH
$R_{m,primary}$	1238	Ω

4.4 CHAPTER SUMMARY

This section has presented the concepts behind the use of ferrite materials in high frequency power transformer circuits. The material properties of ferrites and their benefit to high frequency power conversion electronics was examined, the use of planar cores to minimize volume via PCB integration was described, the core selection process was presented, and finite element analysis was shown to model the proposed transformer. The result is a 2 kW transformer designed for a 1 MHz DC-DC converter based on the M2C architecture, which will be implemented in the final version of the converter.

Multiple cores sizes for both the 2D and 3D FEA models have been developed, with the E43/10/28 with series windings selected due to its capability for power handling at high density without saturation. PCBs were then designed and manufactured to fit the modeled systems and impedance analysis of the fabricated transformers was used to extract circuit parameters to match simulated data. This data will be used in future sections to ensure accurate simulation of the DC-DC MMC system.

In chapter, this section has presented the design, analysis, simulation, fabrication, and testing of PCB-integrated planar transformers using MnZn ferrites as the magnetic core material. Analysis has shown that these transformers are well suited to power conversion in the desired power and frequency ranges and, as a result, these transformers will be used in the design and verification of full DC-DC converter systems based on the MMC architecture.

5.0 GAN-BASED DC-AC MODULAR MULTILEVEL CONVERTERS

The three-phase MMC structure has been successfully applied to medium and high voltage transmission and variable speed drives in a number of applications, as presented in, [5], [6], [7], and [8]. These three-phase MMC systems have demonstrated greater efficiency and greater voltage control over a wide frequency range than their traditional counterparts, while providing outputs with low filtering requirements and requiring significantly reduced volumes. This work takes the lessons learned in medium and high voltage applications and presents the development of a new low-voltage, single-phase, high-density DC-AC MMC system. By taking advantage of submodules (SMs) comprised of GaN HEMT devices and minimalistic capacitor arrays, along with the higher frequency operation that they allow, losses can be drastically reduced for similar power levels. The result is a converter that demonstrates excellent performance over a wide frequency range in an extremely minimal footprint.

5.1 THEORY OF OPERATION

The diagram of the single-phase MMC is presented in Fig. 4, and is configured to allow for split generation of a 240 V_{AC} single-phase sinusoidal output from a 450 V_{DC} input. The converter is comprised of an upper (p) and lower (n) conversion arm for each phase, each of which contain 14 SMs, which are configured as half-bridges of two complimentary switches and a fixed capacitance,

C_{SM}. The half-bridge topology was selected due to its low losses compared with other MMC SM configurations and low number of switches [5]. The targeted converter was designed to the specifications of the Google/IEEE Little Box Challenge [55].

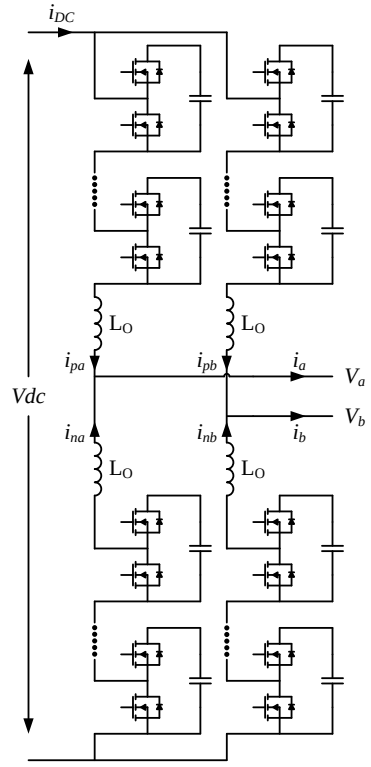


Figure 37. Single-phase MMC topology

The two phases of the MMC each produce a rectified sinusoidal from $\pm m\frac{V_{DC}}{2}$, and are offset by 180 degrees in order to double the phase voltage, achieving an output voltage of $\pm mV_{DC}$, where *m* is the modulation ratio of the converter. The converter output voltage, V_{AB}, is a 26-level sinusoidal waveform. The single-phase MMC behaves similarly to the well-documented 3-phase system [56].

The output voltage of a given SM is zero when the SM is bypassed and equal to the voltage on C_{SM} when the SM is inserted. Based on the switched insertion of the SMs, the output voltage of

each phase is expressed by (37), while the converter output is given by (38). Likewise, the upper and lower arm voltages can be described according to (39) and (40), respectively.

$$V_{AN,BN} = \pm\frac{1}{2}V_{DC}msin(\omega t + \phi) \tag{37}$$

$$V_{AB} = V_{DC}msin(\omega t + \phi) \tag{38}$$

$$v_{jp} = \frac{1}{2}V_{DC} - v_{jN} \tag{39}$$

$$v_{jn} = \frac{1}{2}V_{DC} + v_{jN} \tag{40}$$

Here, j is the AC output phase, ω is the AC output frequency, ϕ is the power factor of the load, and the value of m is $2V_{AC}/V_{DC}$. For a single-phase MMC with N SMs per arm, V_{DC} is divided evenly between the arm's SMs, yielding a maximum voltage of $v_{sm} = \frac{V_{DC}}{N}$, allowing for the use of low-voltage GaN HEMT devices as the complimentary half-bridge switches. To maintain equal SM voltages, phase shifted pulse width modulation (PSPWM) is used, ensuring natural balancing with no sensors [12], [57].

Beyond the normal design constraints of 3-phase MMC systems for power transmission, the high-density VSD application imposes additional challenges that must be considered. First, many modulation techniques exist as described in [5]. In many methods, such as level shifted PWM and staircase modulation, direct measurement and sorting of some or all of the submodule voltages is required. For high-density applications this is extremely undesirable, as it requires

measurement circuitry at each submodule, as well as increasing microcontroller ADC input requirements. As a result, a phase-shifted PWM (PS-PWM) technique, as shown in Figure 38, was employed [6].

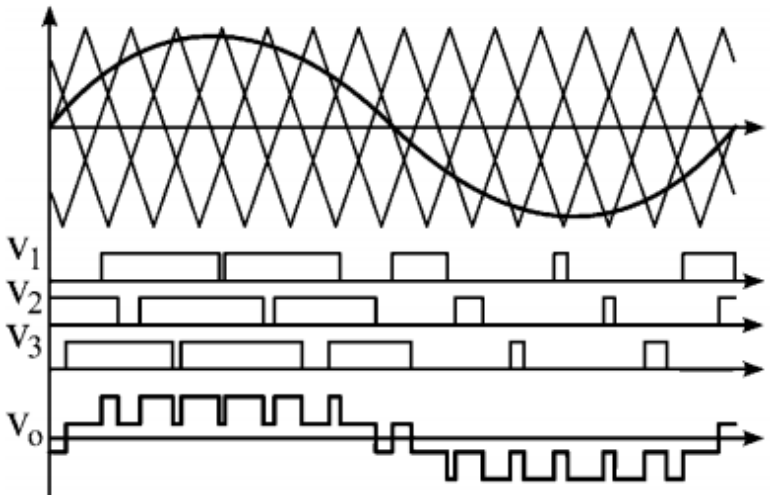


Figure 38. Phase shifted pulse width modulation signal generation and output

This is a well-established technique that yields natural voltage balancing at the expense of higher switching losses in the SM devices [6]. The resulting average switching frequency of a device can be expressed as (41).

$$f_{SM} = mf_{reference} + \frac{f_{carrier}}{N} \tag{41}$$

In high and medium voltage applications this is a serious concern, as the Si IGBTs that are generally used have extremely high switching losses, especially as switching frequency increases.

However, in the high-density applications proposed here, GaN HEMTs are used, which exhibit extremely low switching losses in the proposed range [34].

Specifically, the sizing of SM capacitors and the balancing of their associated voltages becomes increasingly challenging at lower frequencies, as the ripple voltage on the capacitors, ΔV_c will rise. The minimum required SM capacitance, $C_{sm(\min)}$, for a three-phase MMC is presented in [5] and [58]. Adjusting these equations for the single-phase case yields the expression given in (14). Note that cos(ϕ) is the system power factor.

$$C_{sm,min} = \frac{P}{2NmV_c\Delta V_c\omega cos\phi}\left(1 - \frac{mcos\phi}{2}^2\right) \tag{42}$$

It should be noted the denominator of (14) is based on the AC output frequency of the inverter, which means that for a lower output frequency, higher C_{SM} is required. However, since C_{SM} is a fixed value, in general this function results in higher capacitor ripple voltage at lower frequencies. This can be seen by solving (42) for the ripple voltage, as shown in (43).

$$\Delta V_c = \frac{P}{2C_{SM,min}NmV_c\omega cos\phi}\left(1 - \frac{mcos\phi}{2}^2\right) \tag{43}$$

We must therefore choose a capacitive design for the system that allows for the increase of voltage swing at lower frequencies. In the following section, the iterative simulation evaluation used to determine the final capacitor and inductor values will be described, as well as the resulting circuit characteristics based on the PS-PWM modulation technique.

5.2 SYSTEM SIMULATION ANALYSIS

To model the performance of the single-phase MMC in the VSD application, a testbed system was developed in MATLAB/SIMULINK and PLECS as shown Fig. 6.

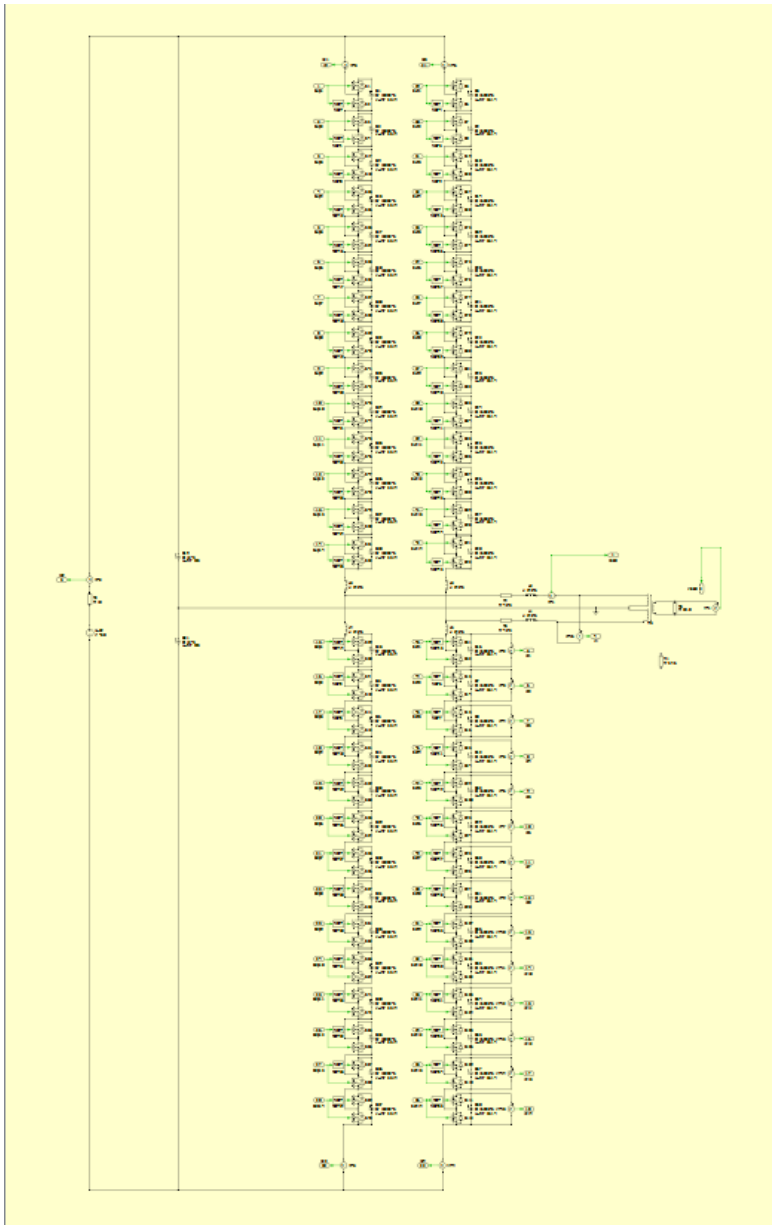


Figure 39. Overview of modeled single phase MMC system

First, a model was established for the single-phase MMC itself. The designed converter was sized based on the power input required to power a split-phase 240V, 2 kW load. Based on the specifications provided by the Google/IEEE Little Box Challenge, voltage and frequency of the system are specified to be 2 kVA, 450 V_{DC}, 240 V_{AC}, and 60 Hz [55].

Next, many design considerations had to be made to determine switching frequency, cell capacitance, arm inductance, and the number of cells in a phase arm. The selection of these values begins with the unique switching device selected for the converter design. To form the half-bridge module, two EPC 2014c GaN HEMT were used [59], which are 40V, 10A enhancement-mode devices. To meet the required input voltage, *N* was set at 14 SMs per phase arm.

These devices exhibit a conduction resistance of 12mΩ and input and output capacitances of 220pF and 150pF. With half-bridges comprised of such devices, switching frequency can be pushed to improve converter harmonic content. By evaluating (42) and observing changing effects on output THD, a switching frequency of 16 kHz was selected. This is the cutoff point at which there is no longer harmonic improvement from reduction of high frequency harmonics, and is instead dominated by multiples of the fundamental, as shown in Figure 40.

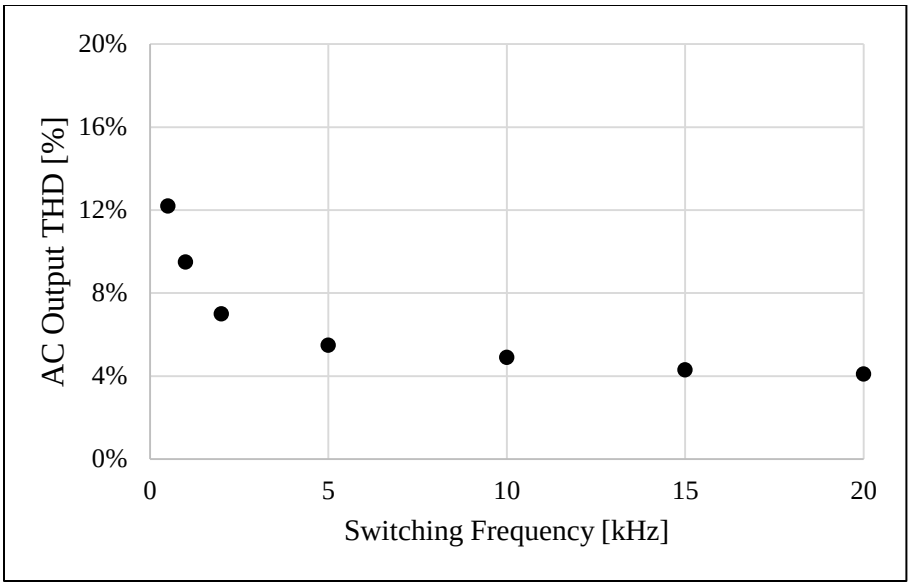


Figure 40. AC output THD as a function of switching frequency

By allowing f_{SM} to range above the very low values allowed in typical MMC circuits, the capacitance can be minimized based on the desired voltage ripple, as described in (43) and shown in Figure 41. Complete specifications for the simulated DC-AC MMC are given in Table 9.

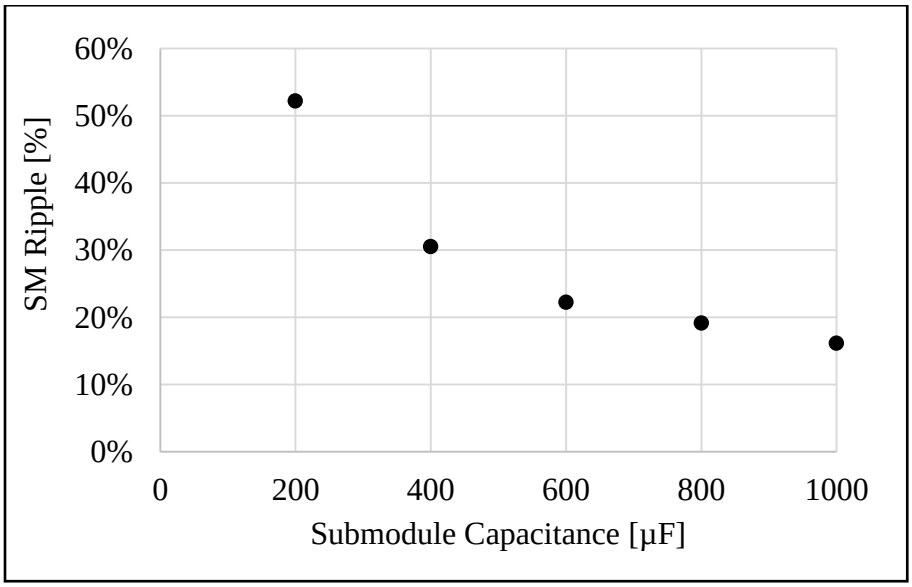


Figure 41. SM voltage ripple as a function of switching frequency

Table 9. Ratings for the DC-AC MMC system

Converter Ratings

Parameter	**Value**
Power Rating	2 kVA
Input Voltage (DC)	450V
Output Voltage (AC)	240 V
Output Frequency	60 Hz
Switching Frequency	24 kHz
Cell Capacitance	1.54 mF
Arm Inductance	17 µH
Cell Voltage	30 V
Cells per Arm	14
Total Volume	20.07 in^3

The system was simulated using MATLAB/SIMULINK in order to verify performance metrics. The simulated voltage and current waveforms are shown in Figure 42 and Figure 43, respectively, and the efficiency of the MMC at various load points is shown in Figure 44. Peak simulated efficiency is 98.1% and output THD is 4.28%.

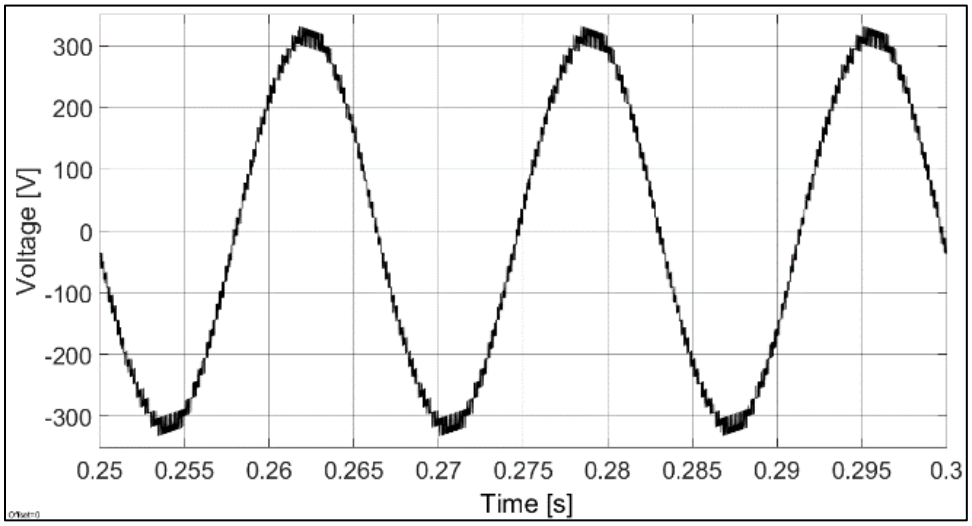


Figure 42. Simulated AC output voltage of 2 kW DC-AC MMC

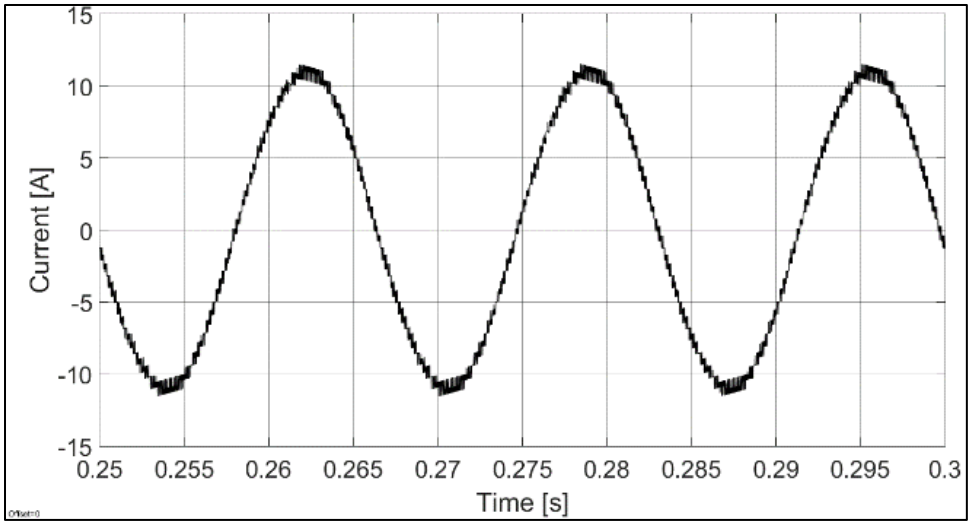


Figure 43. Simulated AC output current for 2 kW DC-AC MMC

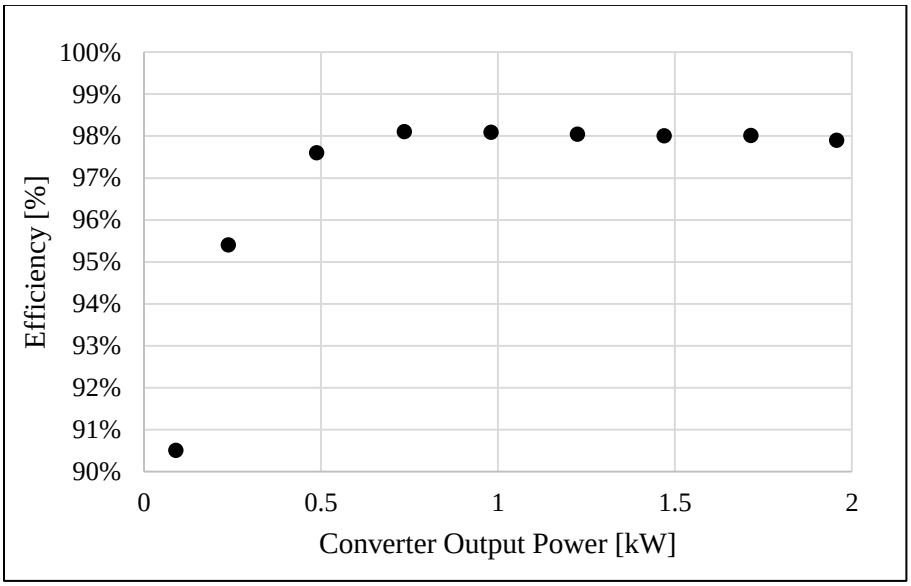


Figure 44. Simulated efficiency of DC-AC MMC

5.3 APPLICATION OF DC-AC MMCS AS NAVAL VARIABLE SPEED DRIVES

The US Navy is highly invested in the safety of all seamen serving on ships and boats. One such way to improve the security of these sailors includes technological advancements in the navy vessels they serve upon. The single most important aspect of a ship's security is the power management system, such that a ship can freely move as needed [60], [61]. The Navy has shown great interest in modernizing the fleet to increase power management adaptability, especially with the push towards the integration of modern lasers, radar systems, and DC networks [61], [62]. In such DC networks, any AC motor loads are best interfaced with by DC-connected variable speed drives (VSDs), which allow for dynamic control of AC induction motors from a DC bus. This paper will present progress towards the development of a high power-density ($100W/in^3$), single-phase VSD designed to operate off a low-voltage DC distribution network.

As electrification of naval systems and DC distribution becomes more common, the necessity of VSDs has been increasing rapidly. For variable torque applications in marine environments, such as those found in [63], [64], and [65], VSDs are already extremely prevalent. However, as the transition to DC distribution systems increase, it will become more necessary than ever for every induction motor load to have DC-based VSDs, as shown in [66].

In addition to conventional inverter application, the proposed architecture is also very suitable for application as a low-voltage VSD. The MMC VSD model was evaluated over a range of frequencies, of which three are presented here: 60 Hz, 45 Hz, and 30 Hz. The power and voltage inputs for the motor were determined using a V/Hz ratio of 3.83, as presented in [67]. The resulting input values can be seen in Table 10, based on the calculations from [68].

Table 10. VSD system input at various frequencies

Input Frequency	Apparent HP	Input Voltage	m	Power Input
60 Hz	1.5	230 V	0.8	1980 VA
45 Hz	1.125	172 V	0.6	920 VA
30 Hz	0.75	115 V	0.4	495 VA

The resulting motor input voltage, input current, load current, and the capacitor voltage variance for the 60Hz, 45Hz, and 30Hz cases are shown in Figure 45 - Figure 48. The simulation results show the effectiveness of the single phase MMC design as a variable speed drive. Several characteristic behaviors can be noted. Of specific note is the sustained performance at voltages below the nominal 60 Hz. The voltage waveform retains its sinusoidal shape with minimal harmonic increase; the output currents have almost no harmonics, even before the filtering supplied by the inductive motor; and finally the voltage fluctuation on the SM capacitors increases only minimally as the frequency is decreased.

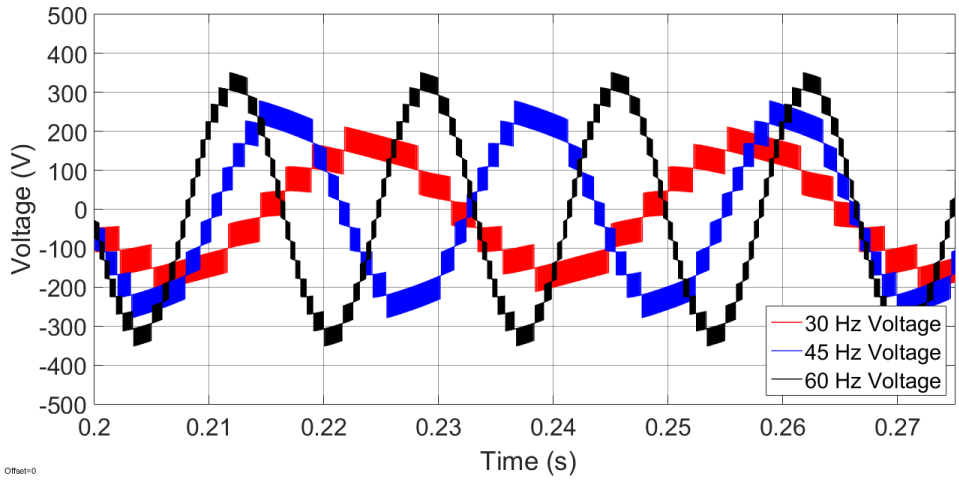


Figure 45. Line-to-line voltage output from the DC-AC MMC variable speed drive

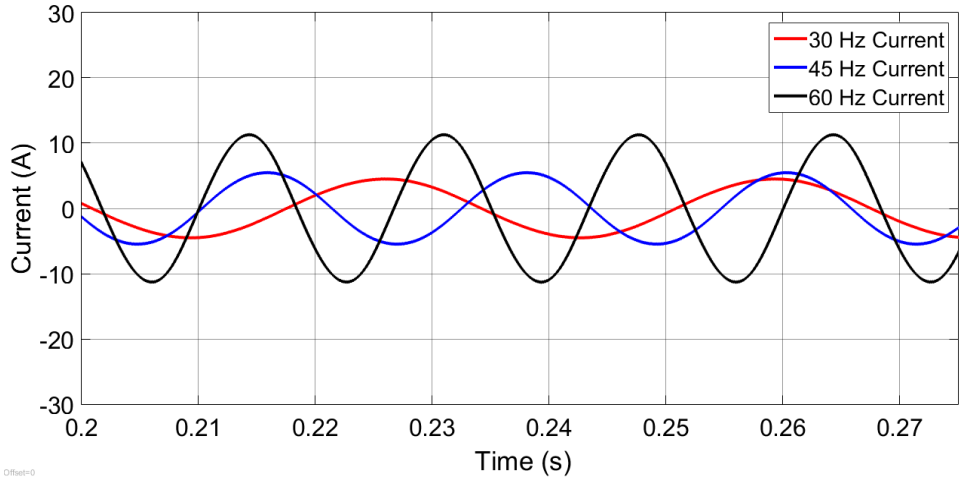


Figure 46. Motor input current from the DC-AC MMC variable speed drive

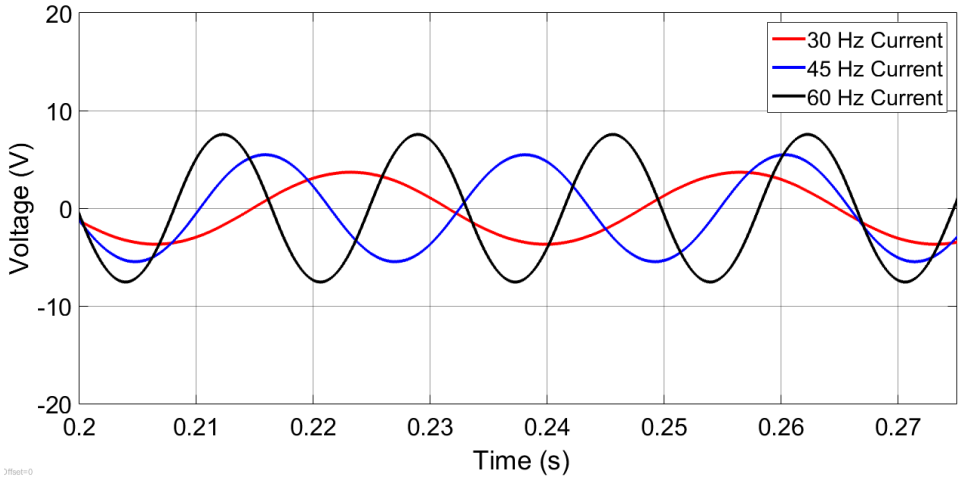


Figure 47. Motor load current from the DC-AC MMC variable speed drive

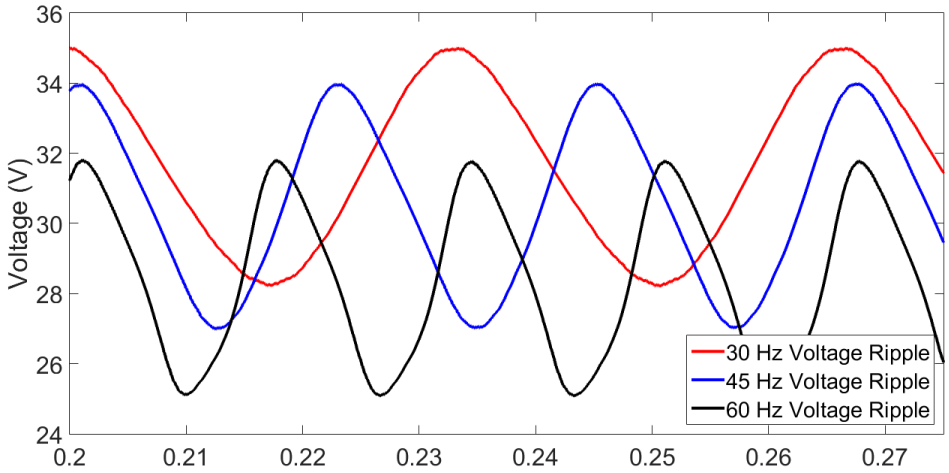


Figure 48. Voltage ripple on the SM capacitors of the DC-AC MMC variable speed drive

Here it can be seen that through the natural balancing of PSPWM for the single-phase MMC case, many of the normal challenges associated with three-phase MMCs in VSD applications can be avoided. While normally the trade-off would be extremely high switching losses, the use of GaN HEMTS in the mid kHz range allows for minimal losses while maintaining peak performance. This results in a VSD that is capable of operating in the low frequency range, as well as performing extremely efficiently across the frequency spectrum.

5.4 HARDWARE IMPLEMENTATION

The DC-AC MMC prototype was designed according to the specifications given in Table 9. The converter is comprised of four MMC arm boards. This section presents the development of the prototype converter system, with considerations for manufacturing challenges and techniques.

The MMC topology provides a unique challenge in gate drive design because of the changing voltage within the interconnection between submodules. As previously described, GaN HEMTs have a sensitive, and defined range of V_{GS} that needs to be upheld to ensure proper and

reliable operation. For the EPC 2014C, 5 volts is the required voltage to fully turn the device ON; however, the device has a maximum voltage of 6 V between the gate and source before device degradation occurs [34], [59]. An isolated gate drive system was designed to enable transistor switching events while limiting the effects of the floating source of the half-bridge transistors. To begin hardware development for the single-phase MMC, a single submodule board was designed in Mentor Graphics PADS to evaluate the gate drive circuitry and the layout thermal characteristics. This design was also helpful in demonstrating the theoretical capacitor sizing and layout.

5.4.1 Submodule PCB Design and Evaluation

In order to develop the DC-AC MMC system, submodules for the converter first needed to be well understood. To that end, submodule PCBs were developed using two GaN HEMTs and slightly reduced submodule capacitance.

The entire cell layout, shown in Figure 49, is 1.685 in. long and 0.325 in. wide and includes full voltage and signal isolation. An ADuM5240ARZ digital isolator from Analog Devices [69] and a LM5113 gate driver from Texas Instruments (TI) [46] are cascaded with the transistors to complete the gate drive circuitry. In addition to providing signal isolation, the Analog Devices digital isolator also includes full voltage isolation through an internal DC/DC converter. The voltage and control signals are then propagated to the TI gate drive chip which is a half-bridge specific driver that produces internal isolation for the upper transistor through a bootstrap topology to clamp V_{GS} at 5.2 Volts (under the 6 Volt limit). The fabricated PCB is shown in Figure 50.

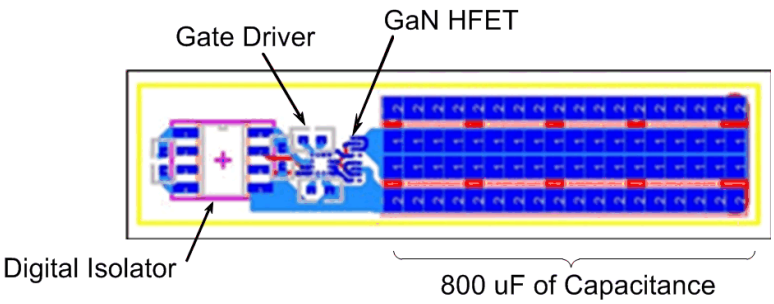


Figure 49. Printed circuit board design for one half-bridge submodule

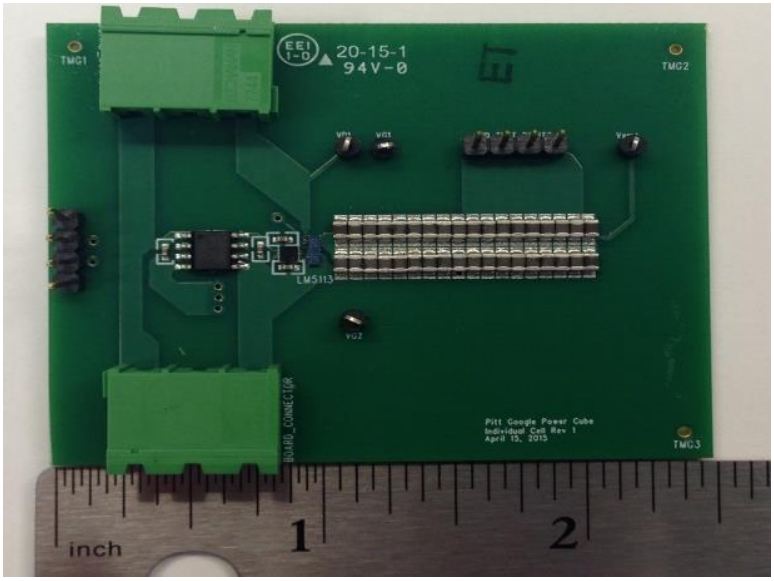


Figure 50. PCB design of a single half-bridge submodule

The PCB design shown in Figure 49 (solder pads, layer-to-layer vias, and traces) was exported from PADS Layout and imported into ANSYS Icepak for thermal behavioral modeling of the layout. An Icepak model was used to predict the thermal distribution under operating conditions within the submodule. Expected power loss metrics were assigned to each major electronic component. The power dissipation (conduction plus switching loss) through each GaN transistor was calculated and modeled in software to be 0.032W when switching at 24 kHz. The digital isolator and gate drive chips are expected to dissipate 0.42W and 0.01W, respectively.

The module equivalent capacitance and bootstrap capacitors have equivalent series resistant (ESR) values of 8.43mΩ and 0.884Ω, respectively, resulting in dissipation values of 1.63μW and 6.2mW at 24 kHz. ESR is a key variable that represents the dielectric loss, and contact and lead resistances of a capacitor as a resistive component. This is a necessary factor to represent the overall losses from capacitive components. Simulation results of the temperature distribution throughout the compact layout predicted the gate drive chip and transistors to be the most thermally sensitive. The temperatures predicted for the chip and transistors were 51.8 ºC and 50.1 ºC, respectively, as seen in Figure 51.

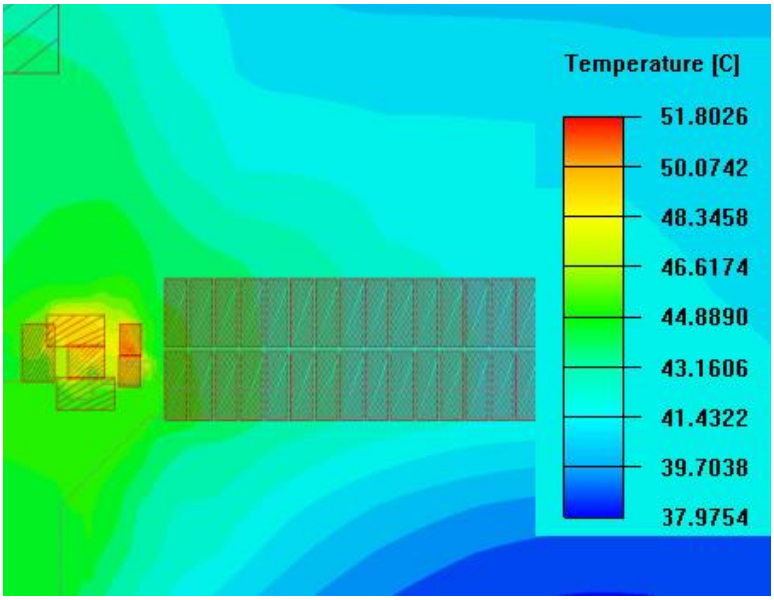


Figure 51. ANSYS Icepak thermal performance simulation results

Experimental tests were conducted to observe the effects of the power flowing through the submodule and the individual transistors, as well as the thermal performance of the overall submodule. Two 24 kHz square waves, with 180˚ phase shift, were applied to the gate circuitry

and 20 V across the whole submodule. Electrical waveforms (V_{GS}) of the turn-ON and turn-OFF characteristics of both the upper and lower transistors are shown in. Figure 52 and Figure 53.

Using a FLIR thermal imaging camera, the temperatures recorded on the gate drive chip and transistors were recorded as 53.4 ^{o}C and 52.2 ^{o}C, respectively, as shown in Figure 54. These values show a strong correlation between the simulated (Figure 51) and experimental results. With this validation of the model, simulations of operation at rated power in open air were performed; and temperatures were shown to rise to approximately 70^{o}C in the transistors and gate drive chip. This is well within thermal limits of the LM5113, EPC2014C, and GaN HEMT devices [70], [71], [72].

Figure 52. Measured turn ON (OFF) characteristics of upper (lower) transistors

Figure 53. Measured turn OFF (ON) characteristic of upper (lower) transistors

Figure 54. Thermal image of submodule operation

5.4.2 MMC Arm PCB Design and Evaluation

Having observed that the submodule circuit operates as expected, a full "power board" was designed to replicate one arm of the MMC topology. Each board contains 14 submodules, with 7 on each side. The conversion section includes the power/digital isolator, gate driver, and GaN HEMTs, which must be thermally managed with heat sinks.

A number of challenges presented themselves through this design process of the power boards. These included: regulation of maximum current through the transistors; elimination of current pathing between the interconnected submodules; incorporation of satisfactory capacitance to provide a clean waveform; and connections and isolation of communication signals from power busses.

A few modifications were made to the original submodule circuitry to provide more efficient and cooler operation as seen in Figure 55. The Digital Isolator was modified from the ADuM5240ARZ to the ADuM5210ARSZ. This change was instituted because the 5210 chip provides signal isolation for up to two signal channels [73], instead of the one that the 5240 chip offered. In addition, the 5210 provides better thermal and electrical efficiency compared to the 5240, while maintaining the same overall functionality (isolated output voltage, isolated control signal). Using the 5210 added significant physical size to this portion of the gate drive circuitry; however, this did not incur any overall system modifications because the height of the capacitor bank was comparable.

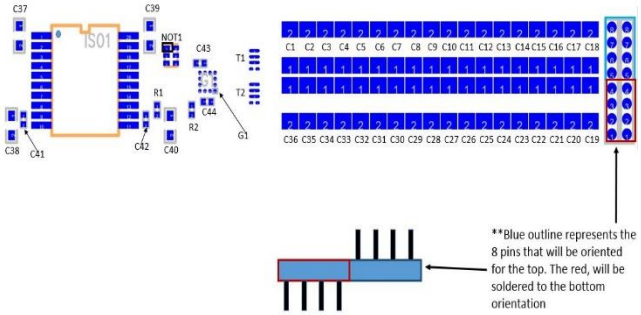


Figure 55. MMC full power board submodule with added standoffs for mezzanine capacitor boards

Annotated photographs of the top view and side view of the fabricated and populated PCB are found in Figure 56 and Figure 57. The finalized is 2.9 in. x 2.5 in x 0.394 in. for a single arm of the MMC.

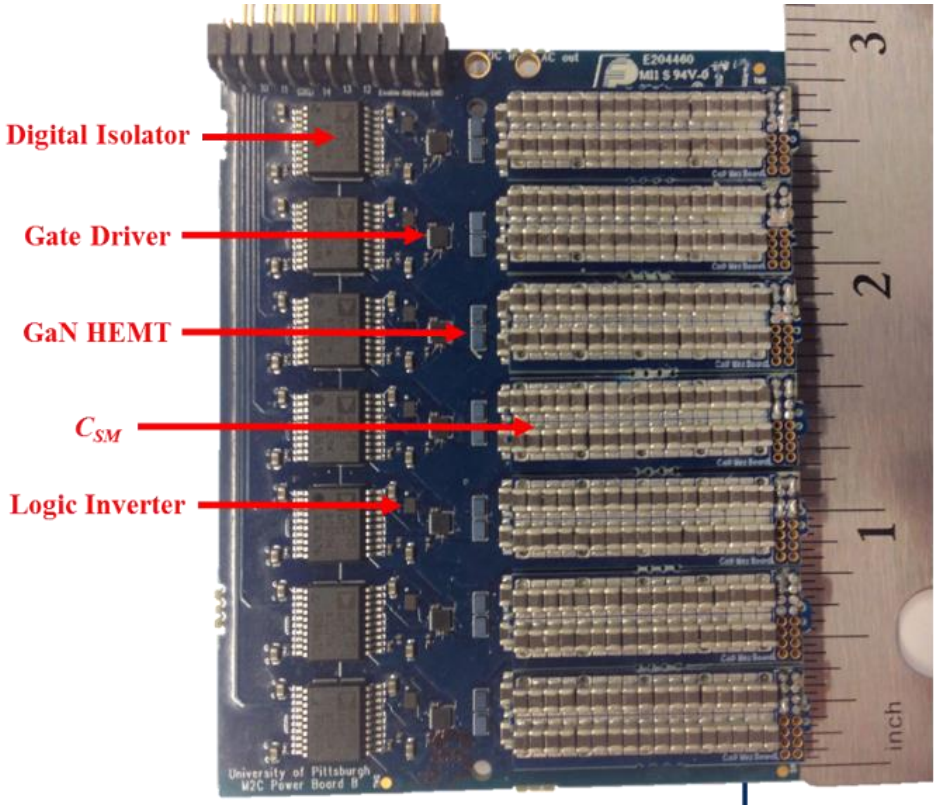


Figure 56. Top view of prototype MMC arm board

Figure 57. Side view of prototype MMC arm board

The entire MMC system is designed with four MMC arms and controlled from a separate control board. A CAD drawing of the final converter assembly with custom developed heat sink is found in Figure 58. The estimated enclosed volume is 20 in^3.

The design and manufacturing of the converter arm included multiple manufacturing challenges. The 0201 resistors, LM5113's BGA pad, or the EPC2014c's unique surface pad (solder bump) size/arrangement could pose short circuit issues for many manufacturers. While 0201 packages are extremely popular in technological areas like RF networks and cellular phone power systems, they are not as common in typical power electronic design work, and care is needed in selecting an assembler.

The greatest challenge for manufacturing was with the submodule capacitor banks, which also consume the most footprint on the PCBs. Each capacitor pad was sized at 0.051" (standard for 0805 capacitors) and is spaced 0.003" apart. The size tolerance for each capacitor is given as ±0.007" [74] and led to stack-up tolerance issues shifting some of the capacitors to the edges of their solder pads. The capacitor electrical connectivity was maintained but, in a redesign, a solid solder bank will be considered.

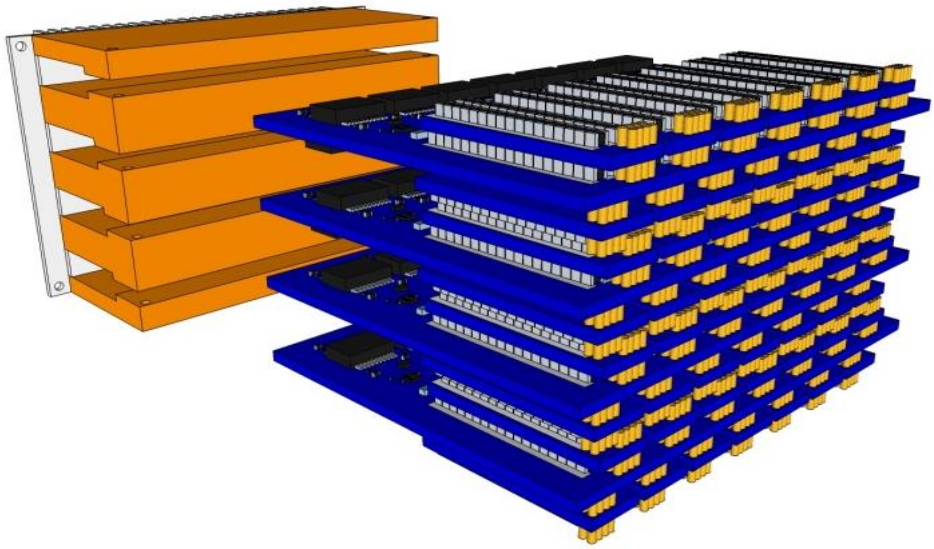


Figure 58. CAD Layout of full MMC Inverter with Heat Sink Design

Current mitigation through the transistors and between submodules was of critical concern. Because the system is required to handle 9 Amps, multiple circuit layers were connected through buried vias throughout these pathways. Initial designs specified 2 oz of copper for the external layers. Through consultation with the board fabricators, this was deemed not possible because of the small buried vias, and pathways. A redesign concluded that a 0.5 oz copper trace thickness could be set, with additional copper applied to reach a final copper trace thickness between 1 and 1.5 oz. TMG Electronics, Inc. was responsible for populating the single MMC arm PCBs shown in Figure 56. The design included miniature components, hence, precise technology was necessary to place the components. The components were placed and fed through reflow ovens to solder the surface mount components onto the board. Through-hole components and the daughter mezzanine boards were then soldered manually. TMG provided quality assurance testing of the component connections to ensure appropriate connectivity between devices and the solder pads. They also performed x-ray tests to observe if any short circuits were created while applying solder paste to the surface mount, and specifically the ball grid array components, which is shown in Figure 59. The fabricated boards are approximately 56 grams in weight and puts the overall board at 19.6 g/in^3.

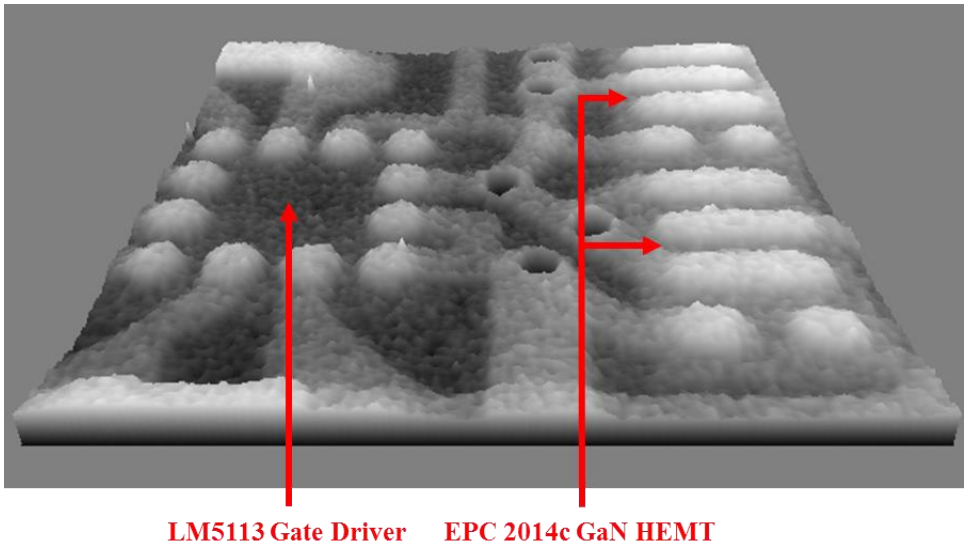


Figure 59. X-Ray Image of LM5113 Gate Driver and EPC2014c GaN HEMTs

Low voltage, two level testing has begun on the full converter, with the test parameters shown in Table III. The tests were performed at low voltage in order to evaluate and troubleshoot arm board functionality and converter performance. The resulting AC voltage waveform based on the test parameters can be seen in Figure 60, the current waveform in Figure 61, and a thermal image in Figure 62. From this image it is apparent that the generated SPWM signals are acting as desired, and that the submodules are charging to the appropriate voltage.

Table 11. Prototype test conditions

Parameter	Rating
Input Voltage	20 VDC
Load Resistance	10 Ω
Output Voltage (peak expected)	10 V_{AC}
Arm Inductance	0 µH

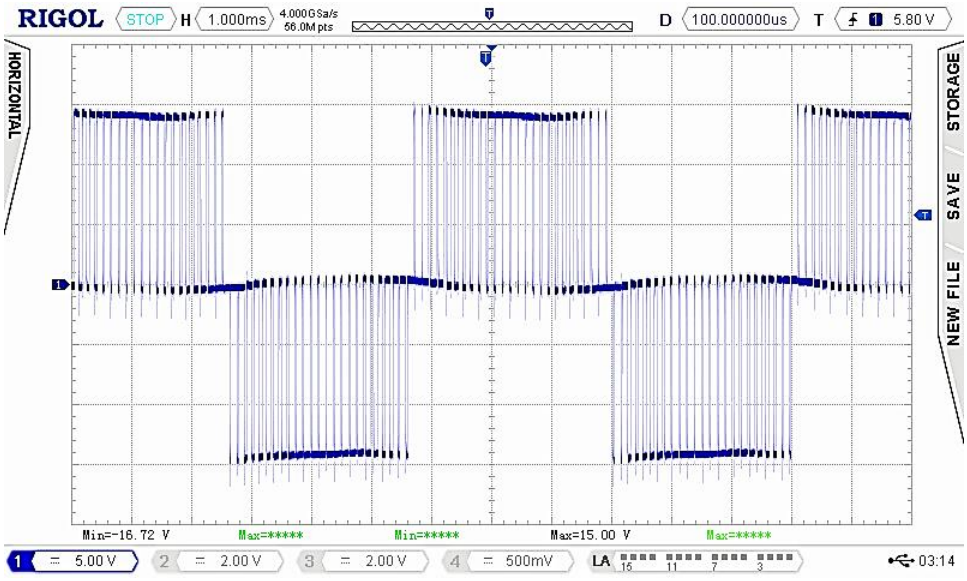


Figure 60. AC voltage output of prototype DC-AC MMC inverter

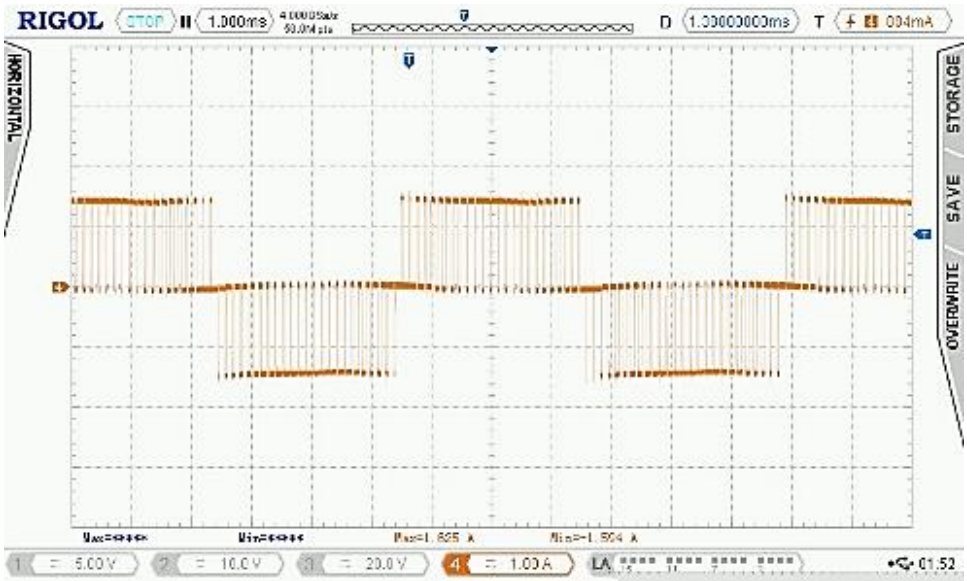


Figure 61. AC current output of prototype DC-AC MMC inverter

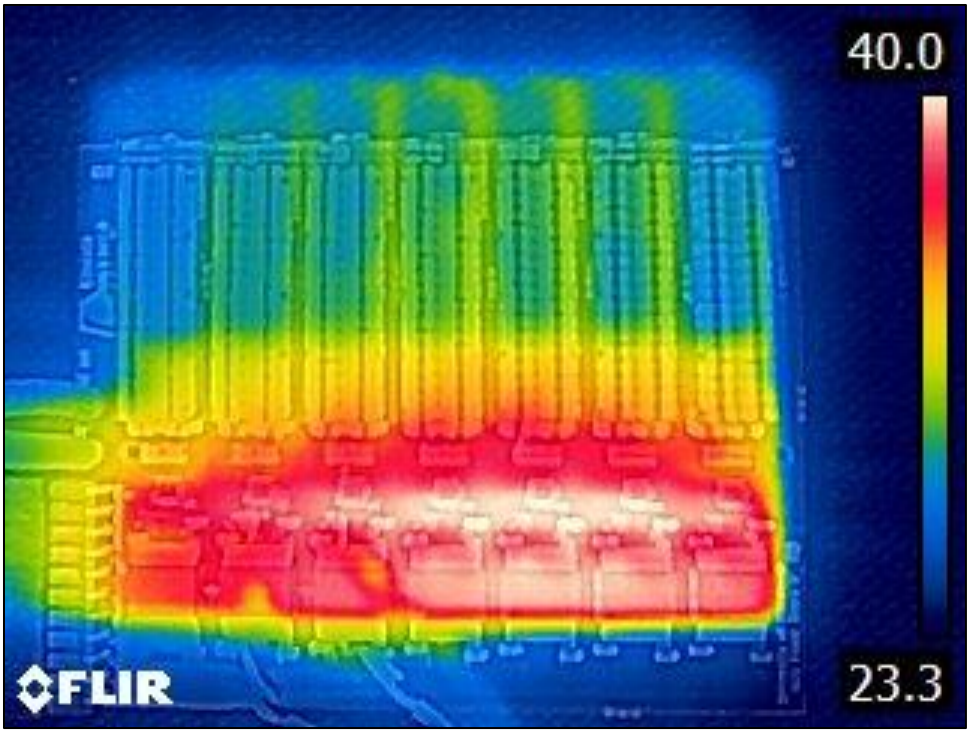


Figure 62. Thermal image of DC-AC MMC under loaded conditions

5.5 CHAPTER SUMMARY

This section has presented the development and operation of a 2 kW, 99.6 W/in^3, 98.1% efficient, GaN-based MMC inverter. It provides an alternative to the other high-density architectures, while exhibiting similar power densities and efficiency. This design brings a well-established converter for three-phase HVDC and MVDC systems to a high-density, low voltage application. The mathematical analysis, modeling and simulation, and initial hardware development have been presented, and the potential for extremely high power-density at non-MHz frequencies has been explored. The resulting single phase DC-AC MMC system is extremely efficient, demonstrates excellent performance over a wide frequency range, and initial hardware results have validated the expectation of achieving 100 W/in^3 in VSD applications for DC systems.

6.0 GAN-BASED DC-DC MODULAR MULTILEVEL CONVERTERS

As has been discussed in the previous section, the MMC shows great promise for the development of high density power electronic systems. The next proposed project is to take the knowledge gained form the implementation of the single-phase DC-AC GaN MMC and extend it to the development of a novel DC-DC architecture. This topology is based on the unification of two DC-AC architectures, operated at high frequency, and unified through a high frequency AC transformer. The proposed converter schematic is shown in Figure 63.

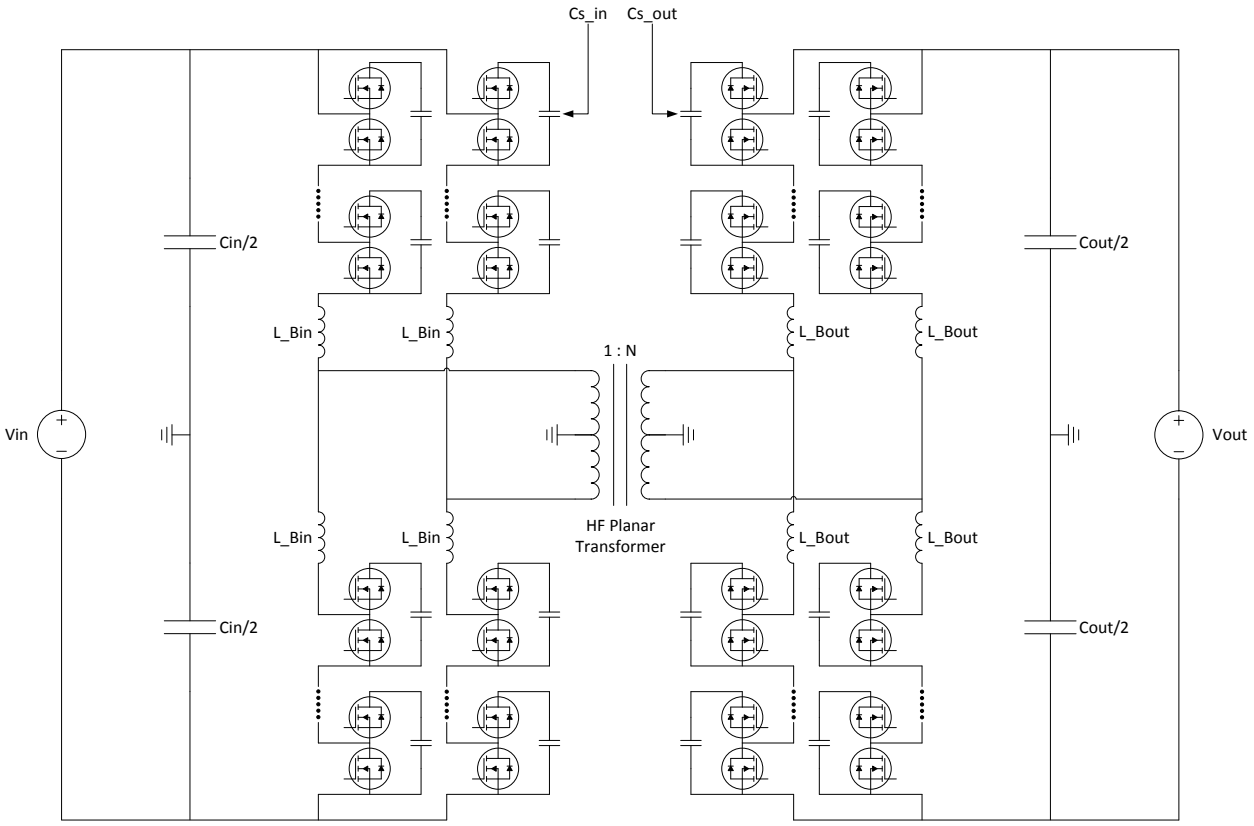


Figure 63. Proposed schematic of DC-DC MMC

This converter is comprised then of two DC-AC arms, one operating as an inverter and the other as a rectifier. Bi-directional power flow will be enabled through this design. The composition of the SMs will be the same, with slight variations in device choice and number of levels per switching section. However, the key difference hinges on the high frequency AC output of the inverter side and the AC input to the rectifier side will be at high frequency, at a proposed 1 MHz. This is of key importance, as the equation governing SM capacitor sizing, (14), dictates that the minimum required CSM is inversely proportional to the AC frequency of the converter.

That means that at extremely high operating frequencies, CSM can be significantly reduced, allowing for much higher power density. As the capacitors take approximately 50% of the DC-AC design, the conversion arms should be dramatically smaller in the DC-DC converter. The two DC-

AC converters will be joined by a high-frequency planar magnetic transformer, as described in the following sections.

To this date, few examples of DC-DC converters utilizing similar architectures have been presented, as shown in [75] and [76]. This means that the traditional balancing mechanism are not required, as all arm transistors are essentially switched simultaneously. Beyond this technical difference in operation, the operation of the circuits are largely the same, allowing for easy adoption of the principles from the DC-AC MMC to the DC-DC converter.

6.1 THEORY OF OPERATION

The MMC has been shown to be a highly versatile and efficient topology in high voltage direct current transmission systems, as well as medium voltage variable speed drives [5], [77]. The voltage division between submodules (SMs) in MMC allows for the use of low voltage switches and drastic reduction in the size of required converter output filtering [5], [78]. The result is a converter class that exhibits high power density, and high reliability when compared to traditional equivalents.

The extension of the MMC to DC-DC operation has begun to be explored for high voltage, high power systems by a number of different groups. In such systems, two MMC structures are connected front-to-front with an AC transformer acting as a coupler, similar to that seen in a Dual Active Bridge (DAB). Similar to the DAB, the frequency of the AC link can be set as desired, allowing it to be raised in order to reduce the size of both SM capacitors and AC link magnetics.

The proposed DC-DC MMC circuit, shown in Fig. 1, achieves a high conversion ratio while limiting the stress experienced by any individual switching devices.

The converter is comprised of an upper (p) and lower (l) conversion arm for each phase. The arms comprising inverter and rectifier conversion branches contain N_{I} and N_{R} SMs, respectively. Each SM is a half-bridge of GaN HEMTs with a fixed SM capacitance, C_{SM}. The half-bridge topology was selected due to its use of fewer switches which results in better efficiency relative to other MMC SM configurations [5]. The resulting SM produces voltage equal to $v_{C_{SM}}$ when inserted into the system, and 0 V otherwise.

By inserting the series SMs in the proper sequence, the AC waveform can be formed as desired. The link voltage can be driven by sinusoidal modulation as shown in [79], quasi-two-level (Q2L) wave modulation as shown in [80] and [81], or quasi-square wave (QSW) modulation (QSM) as shown in [82]. As QSW enables both improved power transfer through the transformer provided by Q2L modulation along with the voltage control provided by sinusoidal modulation, it is employed here [82]. It compares a reference trapezoidal waveform to a set of carrier signals in order to approximate a square wave while allowing for separate turn-on of the SMs. The ramp rate is therefore sized to be just greater than the total turn on of all arm SMs.

Nearest level modulation (NLM) is employed in order to create the quasi-square wave signal, while limiting the number of switching events per AC cycle [83]. This system uses DC carrier waveforms, as opposed to the triangular waveforms used in traditional pulse width modulation schemes, in order to reduce the number of switching events per cycle [84]. The QSW reference is compared with the NLM carriers, as shown in Figure 64, resulting in the ideal AC voltage waveform is shown in Figure 65.

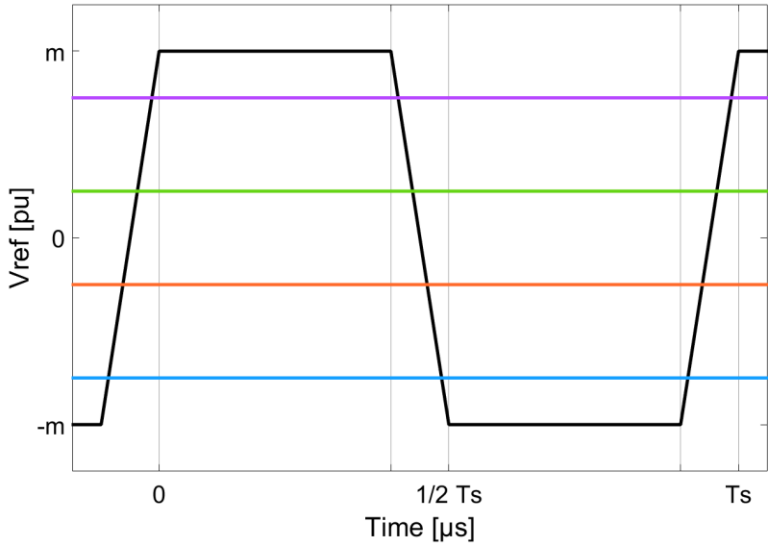


Figure 64. QSW reference and NLM carrier waveforms

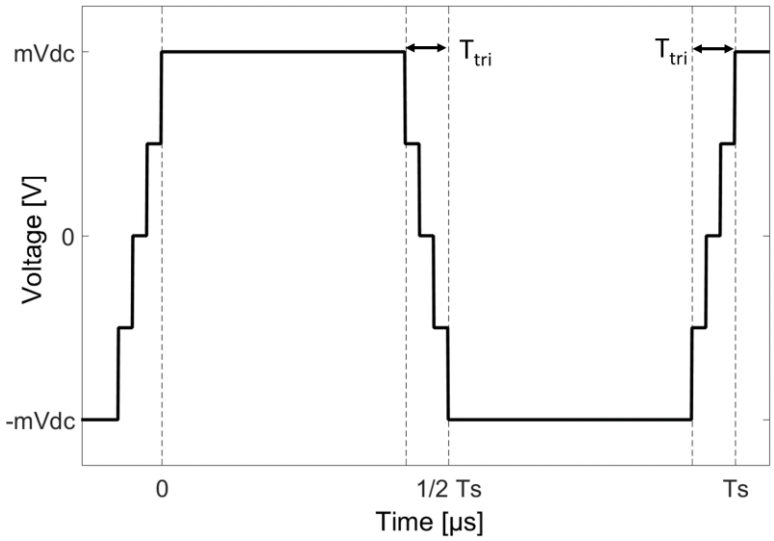


Figure 65. AC output from QSW NLM modulation

In these figures, V_{DC} represents the maximum steady state DC voltage on either the input or the output branch of the DC-DC MMC. Note that because of the split-phase configuration of the DC-DC MMC, the 2nd phase of each branch is set 180 degrees out of phase, effectively doubling the potential output voltage of the system. The modulation indices, m_I and m_R, are the control variables that provides regulation of the conversion ratio between the DC and AC portions of each converter branch. Because NLM is employed with a QSW reference, their values are confined to be fractions of N_1 and N_2, respectively. However, because each branch can be set independently, a wide range of output voltage is achievable.

The resulting AC waveform closely approximates the desired trapezoidal signal, with discrete steps indicating the insertion of a given SM. As a result of the selected modulation strategies, a given arm in either the inverter or rectifier branch of the DC-DC MMC, assuming that arm voltage is equally balanced across its SMs, the voltage on a given SM in an upper or lower arm can be expressed as (44) and (45) respectively.

$$v_{SM,p,S} = \frac{V_{DCS}}{2N_S} - v_{ACS} \tag{44}$$

$$v_{SM,l,S} = \frac{V_{DCS}}{2N_S} + v_{ACS} \tag{45}$$

Here, p represents an upper arm, while l indicated a lower arm, while S is either 1 or 2, indicating the inverting branch and rectifying branch, respectively. Since the SM voltages are equal and the converter is split-phase, the primary and secondary AC voltages can be described by (46).

$$v_{ACS}(t) = \begin{cases} \pm m_S V_{DCS} \mp 2 m_S V_{DCS} \left\lfloor \dfrac{t}{\left(\frac{T_{tri}}{N_S}\right)} \right\rfloor & , t \in T_{tri} \\ \pm m_S V_{DC} & , \text{otherwise} \end{cases} \quad (46)$$

Here, T_{tri} is the desired ramp time from base to peak of the AC waveform. It is not, however, particularly convenient to use the floor function to describe the voltage, as it does not easily allow for evaluation of the current flowing through the transformer. Instead, if a constant ramp is assumed, as is the ideal case, the voltage can instead be expressed as (47).

$$v_{ACS}(t) = \begin{cases} \pm m_S V_{DC,S} \mp \dfrac{2 m_S V_{DC} t}{t_{rise}} & , t \in T_{tri} \\ \pm m_S V_{DC} & , \text{otherwise} \end{cases} \quad (47)$$

Note that the primary and secondary voltages are separated by a phase shift based on the inductance of the transformer, imposing some phase delay ϕ between the signals. This delay is reflected in the derivation of the equivalent primary current waveforms, as shown in (48). In order to derive the current, a process similar to that shown in [82] was employed, where t_1, t_2, t_3 and t_4 are defined by (49-52).

$$\begin{matrix} , t \in (0, t_1) \\ , t \in (t_1, t_2) \\ , t \in (t_2, t_3) \end{matrix} \quad (48)$$

$$i_{AC1}(t) = \begin{cases} \left(\frac{1}{L_{eq}}\left(m_1 V_{DC1} + m_2 \frac{n_1}{n_2} V_{DC2}\right) t + I_1(0)\right) \\ \frac{1}{L_{eq}}\left(\left(-m_2 \frac{n_1}{n_2} V_{DC2}\right)/_{T_{tri}} (t - t_1)^2 + \left(m_1 V_{DC1} + m_2 \frac{n_1}{n_2} V_{DC2}\right)(t - t_1)\right) + I_1(t_1) \\ \frac{1}{L_{eq}}\left(m_1 V_{DC1} - m_2 \frac{n_1}{n_2} V_{DC2}\right) t + I_1(t_2) \\ \frac{1}{L_{eq}}\left(\left(-m_2 \frac{n_1}{n_2} V_{DC1}\right)/_{T_{tri}} (t - t_3)^2 + \left(m_1 V_{DC1} - m_2 \frac{n_1}{n_2} V_{DC2}\right)(t - t_3)\right) + I_1(t_3) \end{cases}, t \in (t_3, t_4)$$

$$t_1 = t(\phi) \tag{49}$$

$$t_2 = t_1 + T_{tri} \tag{50}$$

$$t_3 = {}^1/_2\, T_S - T_{tri} \tag{51}$$

$$t_4 = {}^1/_2\, T_S \tag{52}$$

As the applied voltage is symmetrical, as illustrated in (46) and (47), so too is the equivalent current derived in (48). That is, following t_4, the cycle repeats, with the signal inverted. By integrating across a full period, T_S, the resulting power transfer can be found, as shown in (53).

$$P = \frac{m_1 m_2 \frac{n_1}{n_2} V_{DC1} V_{DC2}}{L_{eq}} \left(\frac{t(\phi)}{2} - \frac{t(\phi)^2}{T_{AC}} - \frac{T_{tri}^2}{6T_{AC}}\right) \tag{53}$$

The result is a converter that can control power transfer in multiple ways. If a fixed output voltage is desired, m_1, m_2, V_{DC1}, and V_{DC2} can remain fixed and ϕ can be intentionally altered via

control. On the other hand, if maximum power transfer is desired at a reduced input or output voltage, m_1 and m_2 can be manipulated to reach the desired operating point.

Reductions in the size of SM capacitors can yield drastic results for improved power density in conversion systems, as they typically compose almost 50% of the volume of DC-AC MMC systems. The minimum required SM capacitance, $C_{sm(\min)}$, for a three-phase MMC is presented in [84]. Adjusting these equations for the single-phase case yields the expression given in (54). Note that cos(ϕ) is the system power factor.

$$C_{sm,min} = \frac{P}{2NmV_c\Delta V_c\omega cos\phi}\left(1 - \frac{mcos\phi^2}{2}\right) \tag{54}$$

Note that since the switching frequency is in the denominator, the capacitance is limited by AC link frequency. In most traditional systems, this means that capacitors cannot be reduced, with the exception of control pattern changes. Using the DC-DC MMC presented here, the AC frequency and carrier frequency are both set to 1 MHz, such that the capacitance can be reduced to 60,000 times smaller than the requisite DC-AC capacitance.

A balancing algorithm must be employed in all MMC designs in order to ensure that the voltages stored on each SM capacitor are the same. Failure to maintain equivalent to do so can result in extremely high voltages being applied across individual devices. Different methods address this issue in both DC-AC and DC-DC MMC systems, the most prevalent being voltage sorting insertion algorithms, natural balancing algorithms, and predictive control. Natural balancing requires specific PWM techniques to function, while voltage sorting algorithms and predictive control would be computationally intense for the MHz range system presented here [84], [85].

However, operating at high switching frequency allows this system to use a progressive insertion scheme. This functions by swapping the insertion order on every AC cycle, without measuring SM voltages. In slower systems, this results in extremely long settling times between devices, preventing it from being a useful mechanism. However, because the system presented here switches rapidly, convergence to a common voltage is extremely rapid, as shown in Fig. 4.

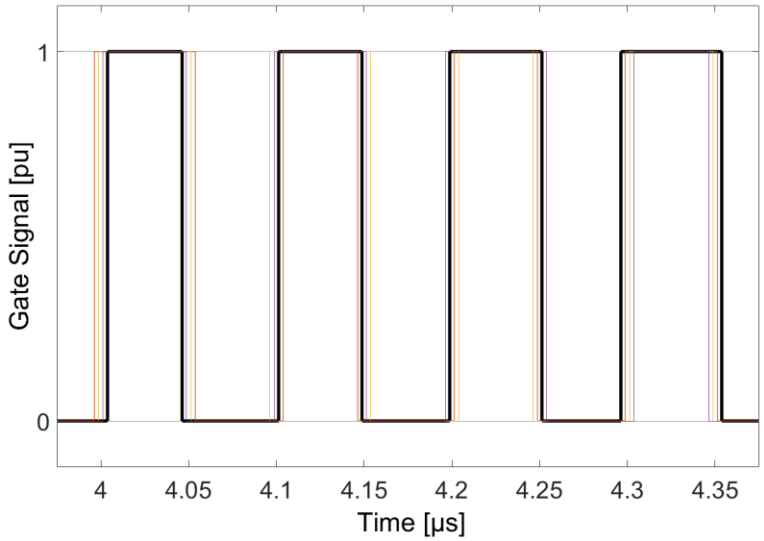


Figure 66. Progressive insertion method for voltage balancing between submodules

6.2 SYSTEM SIMULATION ANALYSIS

The DC-DC MMC system was simulated in MATLAB/SIMULINK using the PLEXIM blockset. Circuit parameters were selected based on the system ratings required for a converter of 200 V input, 600 V output, handling 2 kW. While this initial level is below the power and voltage goals laid out in NASA's technology roadmap, this project is designed as a scalable proof of concept

upon which future, full power converters can be based. The circuit parameters are presented in Table II.

Beyond ratings, however, it was critical to ensure first that the semiconductor devices selected would not suffer from issues related to TID or SEE, and would exhibit minimal losses in high frequency operation. As a result, the EPC2016c was chosen as a commercially available GaN HEMT with a rated V_{DS} of 100 V and I_D of 18 A [86]. The conversion components are listed in Table 2

Table 12. DC-DC MMC circuit parameters

Parameter	**Rating**
Total Power	2 kVA
Max V_{DC} Input	200 V
Primary Current	10 A
Primary SMs per Arm	4
Primary SM voltage	50 V
Max V_{DC} Output	600 V
Secondary Current	3.33 A
Secondary SMs per Arm	10
Secondary SM voltage	60 V
Primary C_{SM}	2 nF
Secondary C_{SM}	1 nF
Converter switching frequency	1 MHz
AC link frequency	1 MHz

The system was simulated using a fixed, stiff DC input source and a 2 kW load. The ferrite transformer was simulated using an equivalent circuit model based on the extracted parameters

presented in Table I. The resulting waveforms for the primary AC voltage and current can be seen in Figure 67 and Figure 68, the secondary AC voltage and current can be seen in Figure 69 and Figure 70, and the DC output can be seen in Figure 71 and Figure 72.

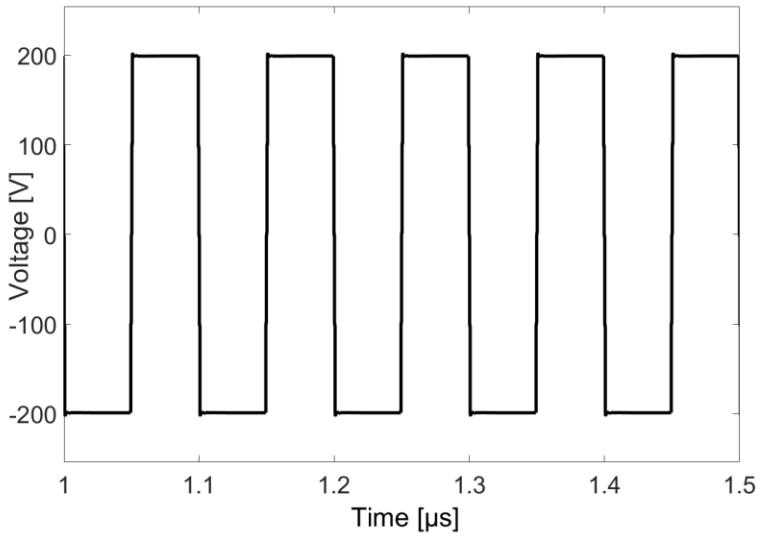


Figure 67. Voltage on primary side of DC-DC MMC AC link

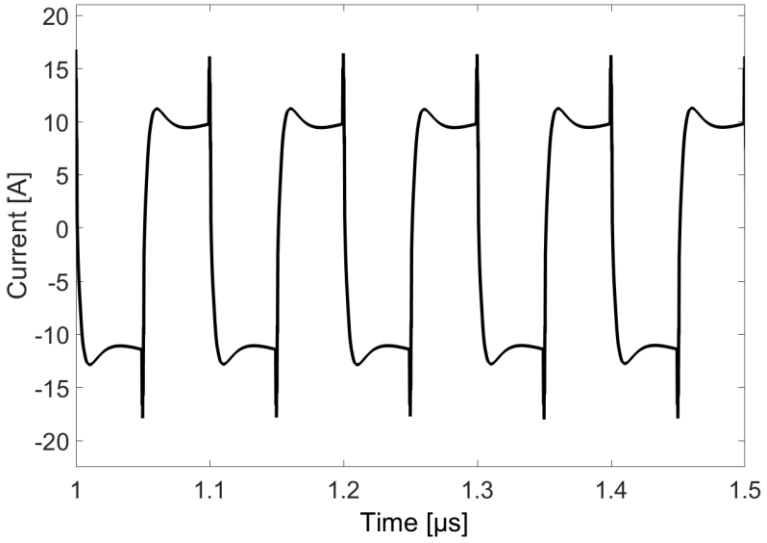


Figure 68. Current on primary side of DC-DC MMC AC link

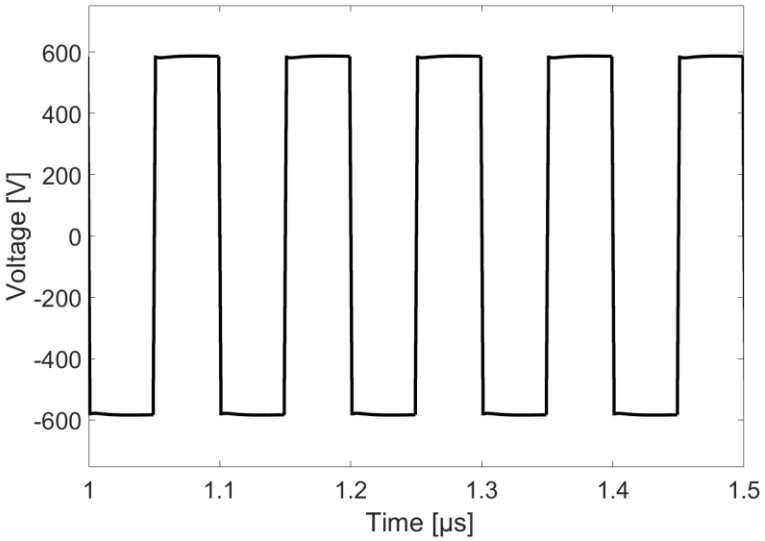


Figure 69. Voltage on secondary side of DC-DC MMC AC link

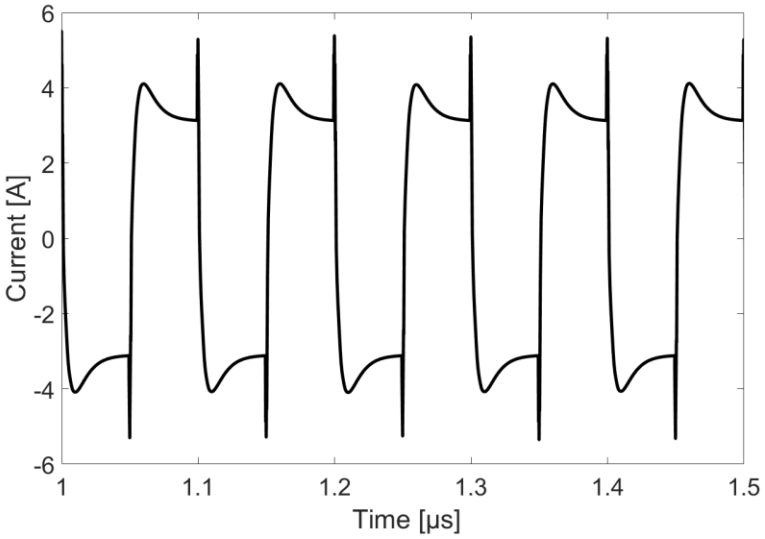


Figure 70. Current on secondary side of DC-DC MMC AC link

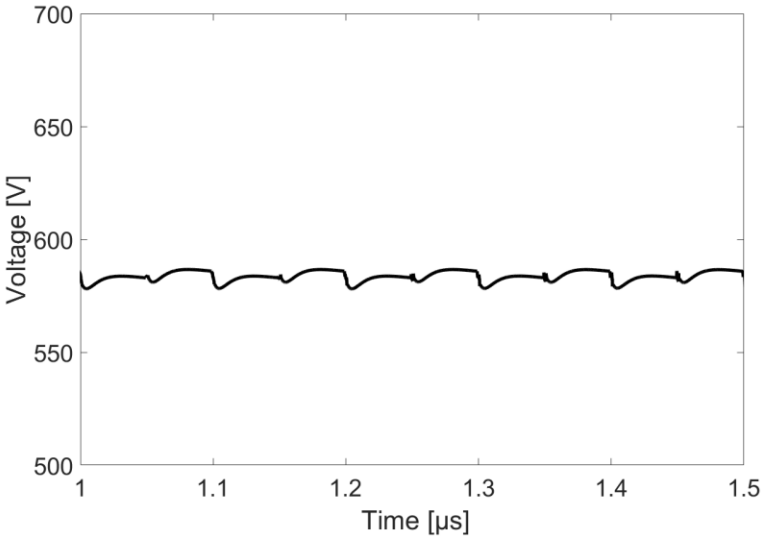


Figure 71. Voltage on DC-DC MMC output

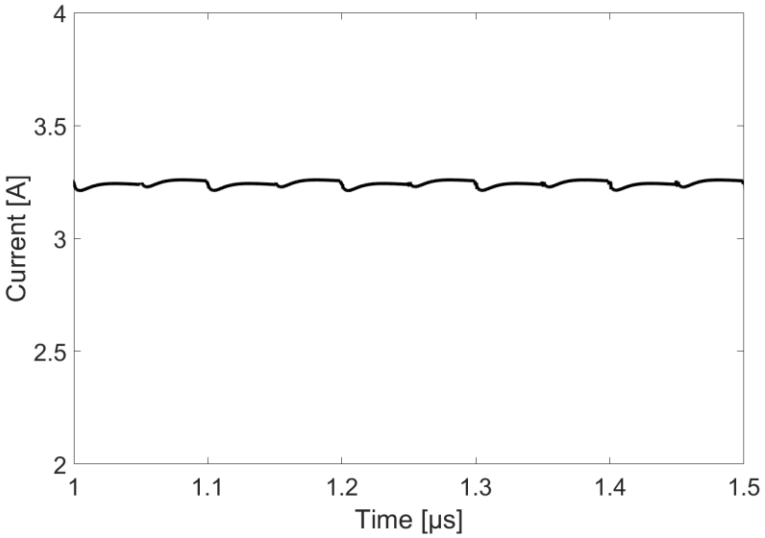


Figure 72. Current on DC-DC MMC output

It can be seen that the converter achieves proper functionality and that the waveforms closely approximate the theoretical equations presented earlier, accounting for losses and parasitics in the simulated system. The switching and conduction losses for the EPC devices, using a 1 Ω gate resistance were 106 W on the primary and 215 W on the secondary. Total losses included the

modeled transformer were 342.6 W, for an efficiency of 82.9%. While low compared to a traditional DAB system, the high frequency causes large switching losses, and this system displays efficiency in line with other MHz range GaN-based converters [87], [88]. If efficiency is a larger concern than volume, the frequency can be decreased at the expense of the transformer size, and pushed easily above 90% [81], [83].

Finally, the functionality of the progressive balancing method for the SM voltages for the primary and the secondary converters can be seen in Figure 73 and Figure 74. From these figures, it is clear that the SMs converge quickly to the same voltage and remain charged to roughly the same level at all times.

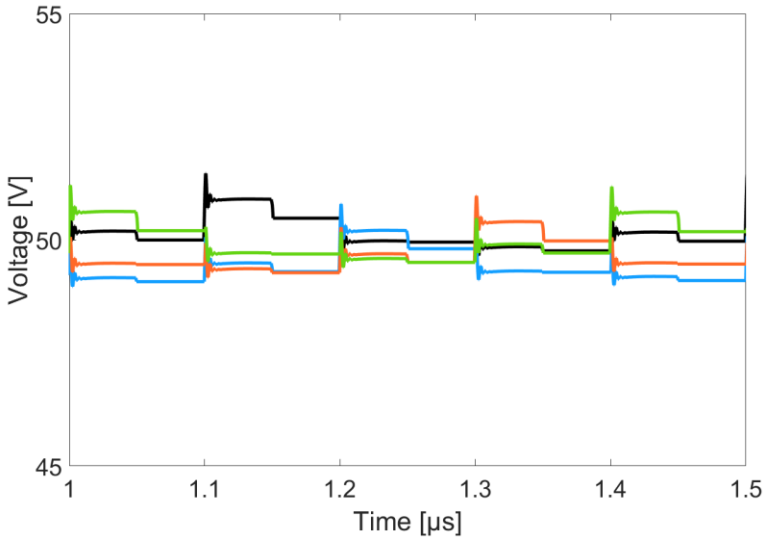


Figure 73. Capacitor voltage balancing in primary converter branch

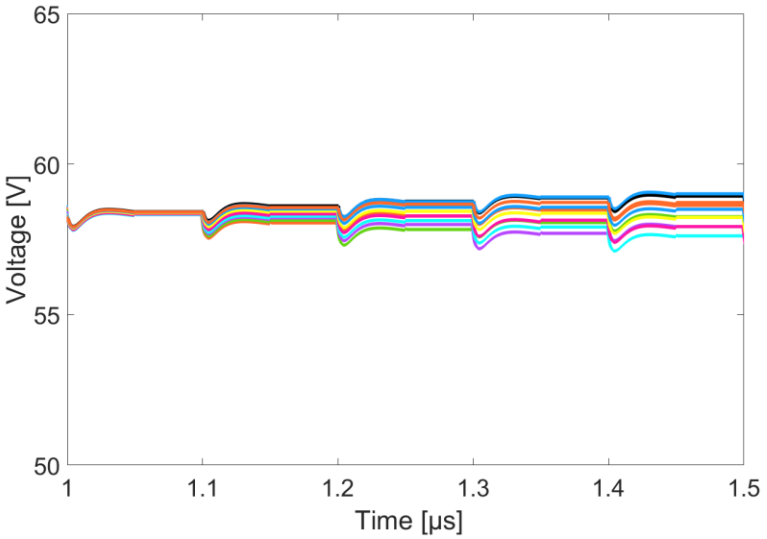


Figure 74. Capacitor voltage balancing in secondary converter branches

It is important to note that these simulated results can be scaled to achieve much higher output voltages than have been evaluated here. In fact the upper limit of SM numbers, and thus input and output voltage capability are only limited by turn-on times of devices and by computational burden experienced by the controller

6.3 APPLICATION OF DC-DC MMCS FOR ANODE DISCHARGE POWER MODULES IN SPACECRAFT SOLAR ELECTRIC PROPULSION

Solar Electric Propulsion (SEP) systems are becoming more prevalent in the design of both missions beyond earth's orbit and for satellite maneuvering and station keeping. SEP offers high specific thrust (I_{sp}), but at lower thrust than conventional propulsion methods, using fuel much more efficiently to achieve a given change in velocity (ΔV) [89]. This makes SEP particularly useful for missions that aim to achieve large ΔV once in space, drastically reducing travel time

within the solar system. SEP is also useful for smaller satellite missions orbiting earth, as it can allow for station keeping and orbital changes while minimizing fuel requirements [90]. Because of this, both Ion Propulsion and Hall Effect Propulsion (HEP) systems are desired by NASA that achieve power levels in the 100 kW range and I_{sp} of greater than 3000 s and 4000 s, respectively [91].

For HEP, increasing the power density and I_{sp} of the system can both be achieved by increasing the voltage supplied to the anode of the thruster by the Anode Discharge Power Module (ADPM) [89], [92]. Raising the voltage of the system directly correlates to a higher I_{sp}, allowing for reduction in requisite Xenon or Iodine mass [93]. Additionally, higher voltage at the same power corresponds to higher power density in the ADPM through reduction in conductor size and more efficient converter operation with certain topologies [94]. As the single largest component in the Power Processing Unit (PPU), size reduction in the ADPM is crucial. Finally, it is beneficial if ADPM designs are capable of parallel operation, such that a system might be scaled to accommodate thrusters of any voltage or power rating. Because of that, NASA has stated that the technology performance goal for next generation of PPU's are systems that operate from an input voltage of up to 250 V – 400V and achieve an output voltage of up to 1 kV, while being scalable up to 100 kW [95]. However, achieving voltages in the kV range can be difficult in PPU's due to the impact of total ionizing dose (TID) and single event effects (SEE) on semiconductors in spacecraft systems, which are more pronounced at higher drain to source voltage (V_{ds}) [96], [97]. Because of this, significant additional device research into semiconductor devices technology may be required in order to safely reach higher voltages in PPU systems.

To address the demand for higher voltage PPU systems for HEP this work proposes an ADPM based on the DC-DC modular multilevel converter (MMC) topology, which enables the

use of radiation resistant, low voltage, GaN HEMTs. The MMC divides voltage evenly across multiple submodules, allowing devices rated for fractions of the total voltage to be used, avoiding the TID and SEE effects seen in larger semiconductors. GaN HEMT devices in the lower voltage range (<100V) show promise in being resistant to both TID and SEE. Additionally, high-reliability, hermetically sealed GaN HEMT are now commercially available [98]. By combining the voltage division capability of the DC-DC MMC with the radiation resistance of low voltage GaN HEMTs, an ADPM is developed in this paper that demonstrates the capability for scalable high voltage output from a variety of input levels, while exhibiting excellent projected power-to-volume and power-to-mass ratios. The converter can be designed with currently commercially available components.

While DC-DC converters are prevalent in numerous systems, such as DC data centers, PV systems, naval vessels, and more, the MMC is particularly applicable to a problem currently being experienced with novel spacecraft propulsion systems. As described in NASA's technology roadmap, the driving converters for Hall Effect propulsion systems [99] are requiring high voltage DC outputs. Specifications for GaN-based MMC solutions to the NASA's current state of the art and future needs are presented in Table 13.

Table 13. NASA roadmap converter specifications

Converter Specifications: Current NASA Requirements	
Parameter	**Value**
Power Rating	5 kW
Input Voltage (DC)	70 – 100 V
Output Voltage (DC)	150 – 400 V
Switching Frequency	100 kHz – 1 MHz
Cells per Input Arm	1
Cells per Output Arm	4

Converter Specifications: Future NASA Requirements	
Parameter	**Value**
Power Rating	10 kW
Input Voltage (DC)	250 – 400 V
Output Voltage (DC)	800 – 1,000 V
Switching Frequency	100 kHz – 1 MHz
Cells per Input Arm	4
Cells per Output Arm	10

These voltages are not attainable using traditional Si MOSFETs or IGBTs. This is due to the impact of Single Event Effects (SEEs), which can result in damage or catastrophic failure in such devices. These events, which are most typically characterized as either Single Event Gate

Rupture (SEGR) or Single Event Burnout (SEB), are caused by single energetic particles from cosmic radiation striking a semiconductor [100].While these failure events have been troublesome for Si devices in high-radiation environments, they have been experimentally shown to not be as problematic for GaN HEMT device, which exhibit tolerance to both SEGR and SEB [101]. In high radiation environments, SEEs become serious concerns for the physical operation of semiconductor devices. Characterized as damaged caused by the passing of heavy ions through the device when bias is applied in a given state, SEEs can result in permanent damage to the semiconductor. While many forms of SEEs exist, the two most damaging and therefore most concerning effects are SEGR and SEB, both of which result in permanent failure of the device. In this section, both effects will be examined in terms of their physical occurrences in traditional semiconductors. In the next section, experimental data will be presented demonstrating the tolerance of AlGaN/GaN HEMT devices to these effects.

SEGR occurs when a high-energy ion traverses the semiconductor through the gate, generating a plasma filament through the *n*-doped region that supports the gate oxide, damaging the gate oxide insulation [102]. In the cylindrical region that is punched out by the passing of the ion, generating both electrons and holes following the passage. While the traversing time of the ion is on the order of ~0.3 ps, the electron-hole charge density can be as high as 10^5 C/cm^2, resulting in breakdown of the surrounding oxide insulation [103]. This process is illustrated in Figure 75 for a Si MOSFET, and the resulting buildup of electric field on the gate metal is shown in Figure 76. With sufficient voltage buildup, the device threshold will be exceeded, destroying the gate of the device and preventing further use.

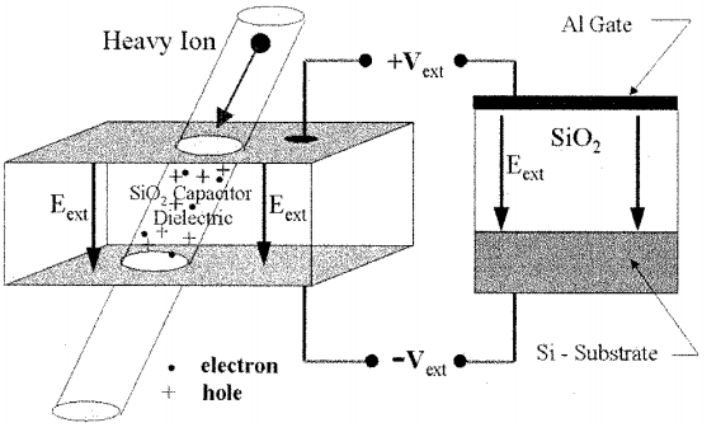


Figure 75. Generation of electron-hole pairs in an oxide following heavy-Ion strike

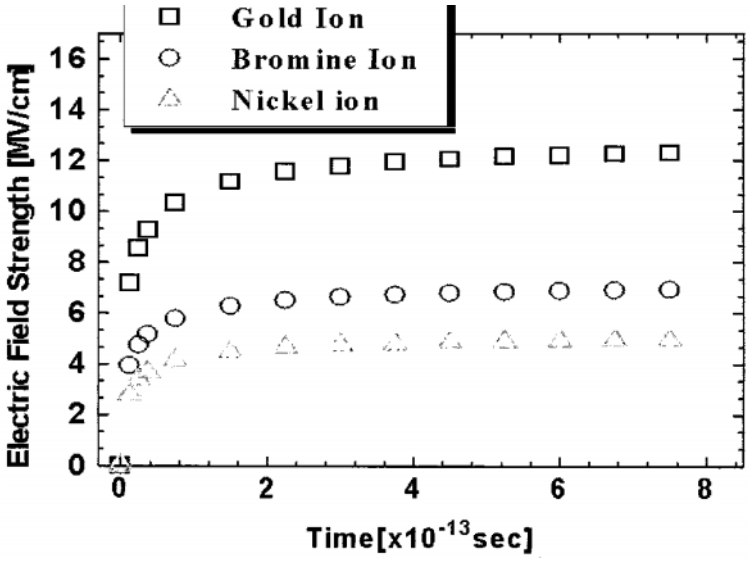
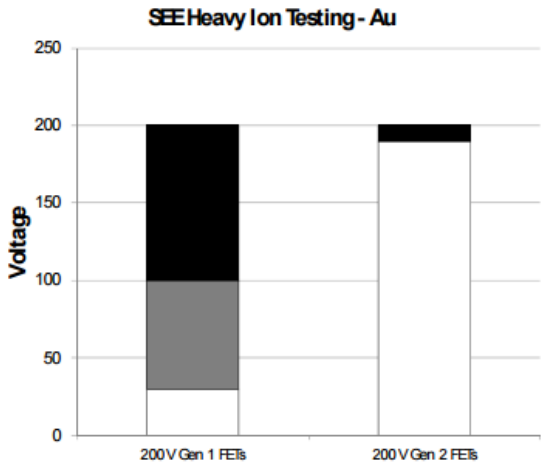


Figure 76. Buildup of the electric field strength versus time for the passage of an ion

The other major mode of failure in high-radiation environments is SEB, which occurs when a heavy-ion traverses the transistor structure through the source [102]. Induced turn-on occurs in parasitic devices, which leads to device destruction when the device is biased in its off state. As shown in Fig. 8, the parasitic bipolar transistor is inherent to the MOSFET structure, formed by

the n+ source as the emitter, the p-body as the base and the n-epitaxial layer as the collector [104]. When this device turns on with sufficient bias voltage when the main MOSFET is in its OFF state, the MOSFET responds as if it is an avalanche failure mode, exhibiting rapid voltage breakdown of the material and resulting in destruction of the device. The likelihood of this occurrence increases with higher applied V_{DS}, requiring design engineers to use reduced V_{DS} values of 65%-75% for terrestrial applications, and down to 25% for spacecraft applications [102].

GaN HEMT devices have been experimentally shown over the last several years to exhibit excellent resistance to both SEGR and SEB when exposed to heavy ionizing radiation. Specifically, enhancement-mode devices, such as those produces by EPC [86], have been shown to drastically out-perform their Si counterparts. In order to test these materials, for SEE implications, they are bombarded with Au, Xe, and Kr at linear energy transfer values as high as 87.2 [105]. Analysis of the most recent generation of GaN HEMTs is shown in Fig. 10, demonstrating both the improvement versus older versions of GaN HEMTs and the lack of de-rating requirements [105].



White – no failures

Light Grey – Continued function but drain-source leakage exceeded rated values

Black – Catastrophic device Failure

Figure 77. SEE capabilities of modern AlGaN/GaN HEMTS

Thus by combining the radiation resistance inherent to GaN HEMTs with the modular architecture provided by the DC-DC MMC, the high output voltages required by Hall Effect propulsion systems can be achieved without detrimental device impacts.

6.4 HARDWARE IMPLEMENTATION

In order to operate the MMC systems described in Chapter 5 to function properly in the MHz switching frequency proposed for the DC-DC MMC presented in this chapter, a number of changes to the physical layout of the system are required. Specifically, a number of adjustments must be made to reduce the PCB parasitic associated with the gate-source and gate-loop inductive paths of the GaN submodules, such that the losses associated with the higher frequency are mitigated. To that end, a new two-level DC-AC system has been designed, to serve as one of the conversion arms for the DC-DC system, along with the planar transformer described in Chapter 4. Additionally, as described in Chapter 3 it becomes more critical in high frequency operation to reduce the parasitics associated with the gate-to-source loop.

To that end, a half bridge circuit has been designed that specifically reduces both the mutual coupling in the paths from the gate driver to the top and bottom GaN HEMTs. To do so, a four-layer configuration was used for each submodule, which is an adaptation of the layout presented shown in Figure 78 [106]. By alternating layers for the loops, the coupling inductance between the traces is reduced. However, as the final design for the DC-DC converter needs to mount submodules on both sides of the converter PCB and requires high current paths on both the top and bottom of the submodule, the submodule capacitance has been moved from the bottom of the 4-layer layout to the side of the half-bridge. While this slightly increases the drain-source loop

inductance for both devices, the reduction of the inductance between submodules is a necessary concession to achieve lower total loss in the converter.

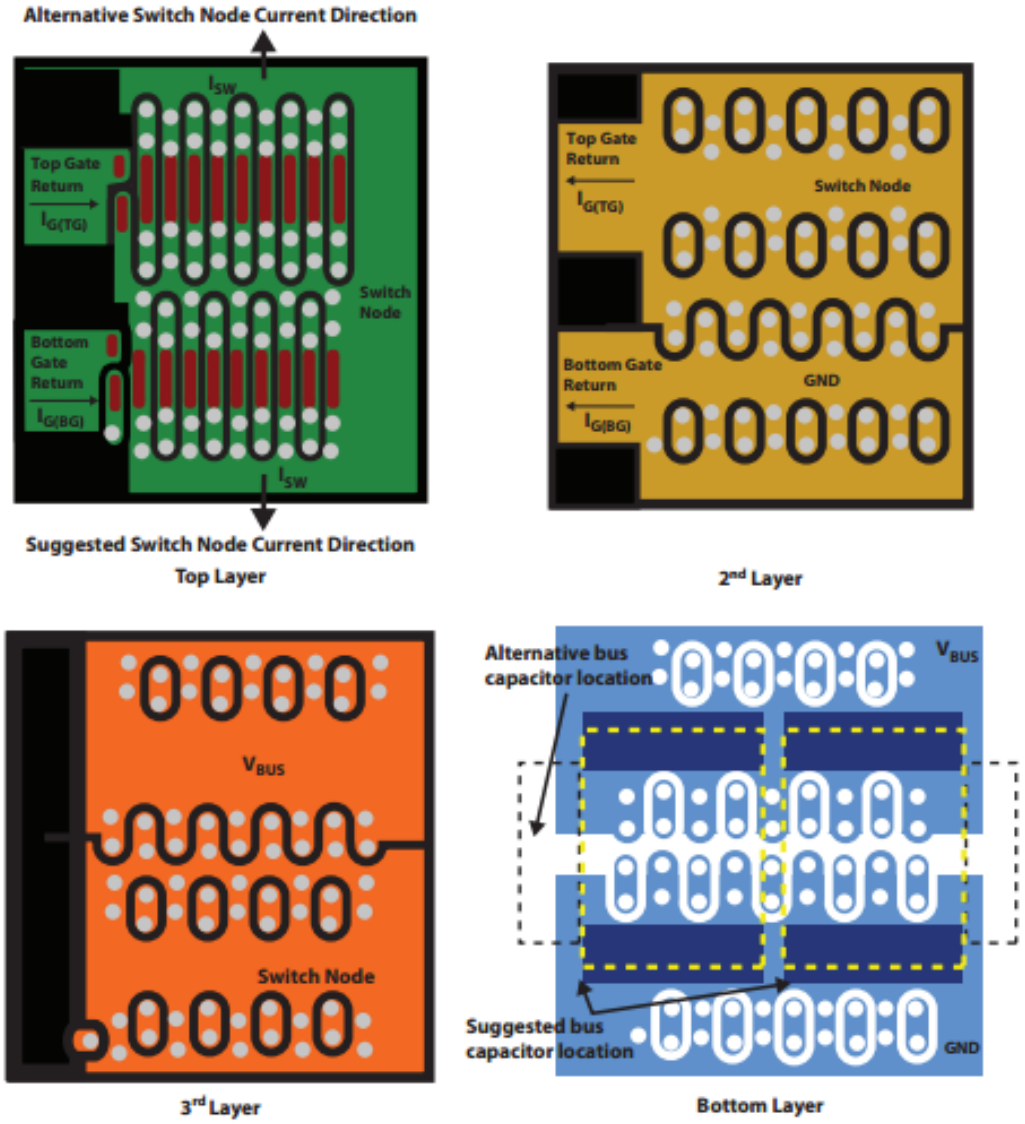


Figure 78. Recommended gate layout for GaN HEMT half-bridge from EPC

The implementation of this gate loop strategy can be seen in the isolated submodule with key components highlighted is shown in Figure 79. The submodule design allows for switching in the

1 MHz range, with minimal delay due to the isolation and driving paths. The components for the submodule are given in Table 15.

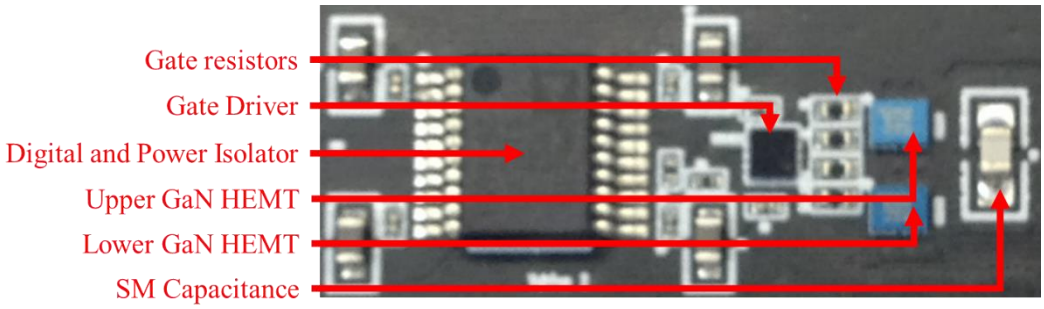


Figure 79. Isolated half-bridge PCB submodule layout

Table 14. Submodule integrated circuits for the developed test system

Device Type	Part Number	Voltage Rating	Current Rating
GaN HEMT	EPC2016c	100 V	18 A
Gate driver	LM5113	100 V	
Signal and Power Isolator	ADUM6210	5 V	

This submodule was designed as a portion of a larger two-level inverter designed to operate up to the MHz range on the AC output. The system was designed to be integrated with the transformers described in Chapter 4 and can be seen with annotated elements in Figure 80 and the parameters of the circuit components are given in Table 15.

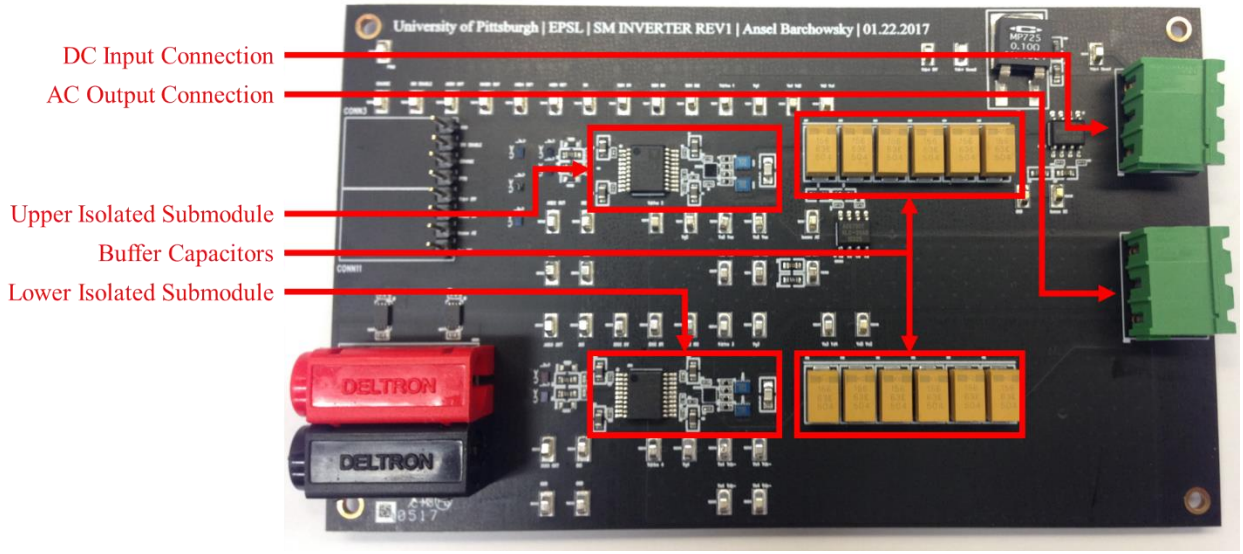


Figure 80. Annotated PCB layout of two-level isolated test system

Table 15. Parameters of MHz-range test converter

Parameter	Value	Units
Total Power	500	W
Max V_{DC} Input	50	V
Primary Current	10	A
R_G	1	Ω
C_{SM}	1	nH

The system was energized up to 30 V on the DC input and was demonstrated to provide the desired AC square wave output, as shown in Figure 81.

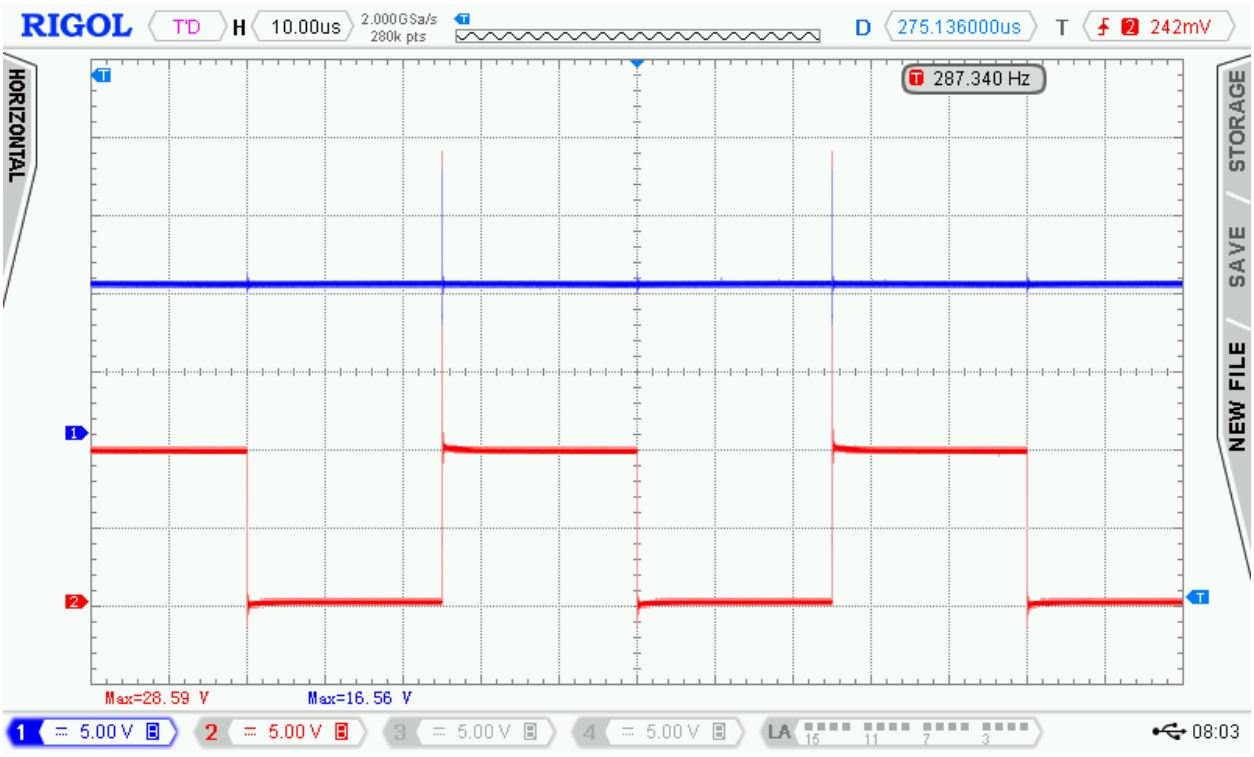


Figure 81. AC output of MHz range test converter at 10 V DC input

The system has been shown as desired, achieving clean voltage outputs in the desired frequency range. In order to evaluate the converter in a DC-DC configuration, ongoing research is being performed by subsequent scholars at the University of Pittsburgh and results will be reported on as soon as they are available.

6.5 CHAPTER SUMMARY

This chapter has presented the development and operation of a new DC-DC MMC for the purpose of achieving high voltage and high power density in DC-DC conversion applications. The proposed converter takes advantage of the voltage division properties of the MMC to enable the

use of GaN HEMTs as the switching devices, presenting an alternative to Si and SiC for high power, high voltage systems. Development of the analytical model and simulated system has been presented. The simulated converter is shown to operate as desired, producing output matching analytical predictions and operating at 83% efficiency when switched at 1 MHz. This converter is a prototype and proof of concept project, designed to illustrate new methods to achieve high voltage and power outputs in small volume converters. While this work presents a converter at 2 kW and 600 V output, the technology is scalable to reach much higher output voltages and power levels.

7.0 CONCLUSION

This document has presented two new adaptations of the modular multilevel converter, taking advantage of the higher switching frequencies enabled by GaN HEMT devices to achieve high density in power conversion electronics. The work contained within this document contains several elements crucial to the design of multilevel high density power electronics. From gate drive optimization and magnetic design to design and analysis of new converter architectures, technologies have been demonstrated in the preceding chapters that will enable designers to achieve higher output voltages and powers in smaller volumes than are achievable using conventional converter topologies.

To achieve that goal, this work has presented two key enabling technologies for converter development at switching frequencies in the hundreds of kilohertz to megahertz range. The first of these tools that is discussed is a method of optimizing the gate resistance for GaN HEMT driver loops based only on device characteristics and measurable or predictable printed circuit board parameters. This, as presented in Chapter 3, is achieved by analyzing the turn on profile of GaN HEMTs during various stages of turn on and developing a mathematical model based on the equivalent circuit of the first sub stage. This work has shown that the first sub stage is sufficient for capturing the worst case transient voltage expressed across the gate-to-source path of the device, a result that has been validated using a hardware testbed with a GaN HEMT from EPC. The derived method provides a tool for designers to choose a safety margin for the overshoot on a

device and produces the optimal gate resistance value for that safety margin. By selecting a gate resistance in this manner, a circuit can be developed that the turn on of the GaN HEMT is as rapid as possible, while avoiding overshoot on the device. By ensuring this safe, rapid turn on of GaN HEMTs, this tool enables the use of these devices in a variety of complex circuits without extensive modeling requirements.

The other technology that this work develops specifically for switching at higher frequencies is a set of planar ferrite transformers designed to operate in the low megahertz range. The transformer design takes advantage of the material properties of Ferroxcube's 3F4 MnZn ferrite along with a planar core and PCB-integrated copper windings to achieve a high conversion ratio and power handling capability in a small volume. However, significant analysis is required to ensure that the material properties of the core are not exceeded by the excitation expected from the converter. The work in Chapter 4 presented the development of the transformers to be used in the converters proposed by this dissertation. To core and winding configurations were first analytical modeled using geometric equivalents of the circuit. The resulting design was then modeled using 2D finite element analysis to determine the ideal number of windings and interleaving pattern for those windings within the PCB. Based on those results, a 3D finite element model is presented for two transformers. The first has parallel connected windings on alternating layers of a 10-layer PCB. The current is shared equally between layers to reduce winding losses. However, the resulting flux density was shown to exceed the rated maximum value for the 3F4 material. Thus, the second design instead uses series-connected PCB windings, resulting in the same conversion ratio with a much higher number of windings. This increased winding losses while reducing the flux density experienced by the core and ensured that saturation was not reached. Equivalent circuit parameters for these transformers were then extracted and compared

to results obtained from impedance analysis performed on the developed hardware testbeds. The resulting transformers parameters were used in the designs for the DC-DC MMC presented later in Chapter 6.

Following the introduction of these two supporting technologies, the converter architectures that are the focus of this work were presented. Both of the converters are based on the modular multilevel converter architecture that is seen quite commonly in HVDC, MVDC, and MV VSD systems. This topology is dependent on the simple principle of breaking large input and output voltage and current levels into smaller voltages distributed across submodules. While that is used in those high voltage systems to allow large IGBTs to reach hundreds or thousands of kilovolts, it is applied in this work to reduce voltage levels to those switchable by GaN HEMT devices. This adjustment allows for GaN HEMTs to be used in converter applications that demand voltage ratings outside the capabilities of current GaN devices. The result are DC-AC and DC-DC MMC systems that archive high voltage inputs and outputs while achieving the high power density expected of converter systems using GaN as the switching device.

First, the DC-AC MMC is presented. Using a single-phase adaptation of the three-phase architecture commonly used in HVDC systems, the converter enables the use of GaN HEMTs to achieve very high efficiency at switching frequencies that are orders of magnitude higher than those typically used in MMC architectures. This is dependent on a phase-shifted pulse width modulation and a natural capacitor balancing algorithm that are discussed within the chapter. Based on that configuration, an analytical model is developed to describe the circuit behavior of the converter system. Using this, a simulated system is then developed using SIMULINK with the PLEXIM plugin. Results for switching profiles and efficiencies were presented. Next, based on those results, a specific application was discussed, focused on using the DC-AC MMC system as

a variable speed drive in naval DC microgrids. The DC-AC MMC VSD was shown to provide excellent voltage shaping and frequency control across the desired frequency spectrum. Finally, to demonstrate the concepts behind this technology, hardware prototypes were developed to prove first the submodule design and then the full converter arm. Both were shown to perform as expected, with further development in terms of the hardware assembly of these complex compact power circuits. The end result is a DC-AC MMC system that achieves conversion from higher voltages than are supported by individual GaN devices and achieves a power density of 100 W/in^3.

Finally, a DC-DC MMC based on similar technology is presented in Chapter 6. This converter increases the frequency up to 1 MHz, drastically reducing both the size of the submodule capacitance and the other energy storage elements in the system. The planar ferrite transformer developed in Chapter 4 was used as the basis for the AC link and was reflected in analysis and modeling of the system. In order to accommodate switching at those speeds, new modulation methods were developed, combining quasi-square wave operation and nearest level modulation to achieve an AC square wave with edge rates using only two switching events per submodule per AC cycle, drastically reducing switching losses in the circuit. Similar to the DC-AC MMC system, the DC-DC converter was mathematically analyzed, simulated using SIMULINK and PLEXIM, and evaluated in hardware. First, however, it was established as a potential solution for anode discharge power supplies in spacecraft solar electric propulsion, taking advantage of the reported radiation resistance of GaN HEMTs and the MMC architecture to achieve high output voltages in spacecraft applications. To verify the analysis, the hardware prototype was developed to demonstrate the isolated GaN submodules in half of the DC-DC system. The converter was shown to achieve the desired conversion at high frequency with minimal losses in the loop. The end result

is a DC-DC MMC system that achieves excellent conversion ratio and high isolated output voltage with high power density.

As a collective then, this work has demonstrated the use of GaN HEMT devices in modular multilevel converter architectures, pushing the boundaries of both switching frequency and power density in converters based on the MMC structure. Both the DC-AC and DC-DC MMC converters presented within this work provide designers with alternatives to conventional power converters and other high density topologies that allow for the achievement of both high voltage and high power density in converter systems. With these converters topologies, along with the supporting technologies discussed within this work and the unique control architectures of each converter, new methods have been designed and presented for high density design. These topologies demand further investigation, and as power conversion continues to push towards higher voltage, frequency, efficiency, and density, designers must continue to push the boundaries of topology development. This dissertation provides a first step in that direction and the converters here can be used as building blocks for power conversion engineers in future pursuits.

BIBLIOGRAPHY

[1] C. Zhao, B. Trento, E. Jiang, A. Jones, B. Liu, Z. Zhang, D. Costinett, F. Wang, L. M. Tolbert, J. F. Jansen, R. Kress and R. Langley, "Design and Implementation of GaN-Based, 100 kHz, 102W/in3 Single-Phase Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6777, 2016.

[2] L. Zhang, R. Born, X. Zhao and J. S. Lai, "A High Efficiency Inverter Design for Google Little Box Challenge," in *WiPDA 2015*, 2015.

[3] S. Hoffmann, E. Hoene, O. Zeiter, K. Lang and G. Feix, "Reducing Inductor Size in High Frequency Grid Feeding Inverters," in *PCIM Europe*, 2015.

[4] Y. Lei, C. Barth, S. Qin, C. Liu, I. Moon, S. Andrew, D. Chou, T. Foulkes, Z. Ye, Z. Liao and R. C. N. Pilawa-Podgurski, "A 2kW, Single-Phase, 7-level GaN Inverter with an Active Energy Buffer Achieving 216W/in3 Power Density and 97.6% Peak Efficiency," in *IEEE Applied Electronics Conference 2016*, 2016.

[5] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics*, vol. 30, no. 99, 2014.

[6] M. a. Perez, S. Bernet, J. Rodriguez, S. Kouro and R. Lizana, "Circuit Topologies, Modelling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 99, 2014.

[7] J. Kolb, F. Kammerer, M. Gommeringer and M. Braun, "Cascaded Control System of the Modular Multilevel Converter for Feeding Variable-Speed Drives," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 349-357, 2015.

[8] A. Antonopoulos, L. Angquist, L. Harnefors and H. P. Nee, "Optimal Selection of the Average Capacitor Voltage for Variable-Speed Drives with Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 227-234, 2015.

[9] K. Ilves, S. Member, A. Antonopoulos and S. Norrga, "Steady State Analysis of Intraction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* pp. 57-68, 2012.

[10] D. Van Der Linde, C. A. M. Boon and J. B. Klaassens, "Design of a High Frequency Planar Power Transformer in Multilayer Technology," *IEEE Transactions on Industrial Electronics,* vol. 38, no. 2, pp. 135-141, 1991.

[11] S. Xiao, "Planar Magnetics Design for Low-Voltage DC-DC Converters," University of Central Florida, 2004.

[12] K. Ilves, S. Norrga, L. Harnefors and H. P. Nee, "On Energy Storage Requirements in Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 29, no. 1, pp. 77-88, 2014.

[13] S. Kenzelmann, "Modular DC/DC Converter for DC Distribution and Collection Networks," Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland, 2012.

[14] A. Mantooth, M. D. Glover and P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronics Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 2, no. 3, pp. 373-385, 2014.

[15] D. G. e. all, "Advanced SiC Power Technology for HIgh Megawatt Power Conditioning," CREE, 2012.

[16] Y.-F. Wu, R. Coffie, N. Fichtenbaum, Y. Dora, C. S. Suh, L. Shen, P. Parikh and U. K. Mishra, "Total GaN Solution to Electricity Power Conversion," *IEEE 69th Device Research Conference,* pp. 217-218, 2011.

[17] M. Gurfunkle, H. D. Xiong, K. P. Cheung, J. S. Suehle, J. B. Bernstein, Y. Shapira, A. J. Lelis, S. Haberstat and N. Goldsman, "Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I-V Techniques," *IEEE Transactions on Electron Devices,* vol. 55, no. 8, pp. 2004-20012, 2008.

[18] Z. Liu, X. Huang, F. C. Lee and Q. Li, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," *IEEE Transactions on Power Electronics,* vol. 60, no. 2, pp. 1977-1985, 2014.

[19] R. Khanna, A. A. Amrhein, W. E. Stanchina, G. F. Reed and Z.-H. Mao, "An Analytical Model for Evaluating the Influence of Device Parasitics on Cdv/dt Induced False Turn-On in SiC MOSFETs," in *Applied Power Electronics COnference,* Long Beach, CA, 2013.

[20] A. Lemmon, M. Mazolla, J. Gafford and C. Parker, "Stability Considerations for Silicon Carbide Field-Effect Transistors," *IEEE Transactions on Power Electronics,* vol. 28, no. 10, pp. 4453-4459, 2013.

[21] K. Chen, Z. Zhao, L. Yuan, T. Lu and F. He, "The Impact of Nonlinear Junction Capacitance on Switching Transient and its Modeling for SiC MOSFET," *IEEE Transactions on Electron Devices,* vol. 62, no. 2, pp. 333-338, 2015.

[22] A. Goldman, Modern Ferrite Technology, 2nd Ed., Pittsburgh, PA: Springer, 2006.

[23] C. W. Chen, Metallurgy and Magnetism of Soft Magnetic Materials, Mineola, NY: Dover Publications, Inc., 1986.

[24] "3F4 Material Specification Datasheet," Ferroxcube, 2004.

[25] W. M. McLyman, Transformer and Inductor Design Handbook, 4th Ed., 2011.

[26] M. Rodriguez, Y. Zhang and D. Maksimovic, "High Frequency PWM Buck Converters using GaN-on-SiC HEMTs," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2462-2473, 2014.

[27] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda and L. Omura, "Recessed-gate Structure Approach Toward Normally Off High Voltage AlGaN/GaN HEMT for Power Electronics Applications," *IEEE Transactions on Power Electronics,* vol. 53, no. 2, pp. 356-362, 2006.

[28] N. Ikeda, J. Li and S. Yoshida, "Normally Off Power AlGaN/GaN HFET," in *IEEE International Symposium on Power Semiconductor Devices,* Kitakyushu, Japan, 2004.

[29] "EPC2007 Datasheet," EPC, [Online]. Available: http://epc-co.com/epc/documents/datasheets/EPC2007_datasheet_final.pdf.

[30] "EPC8010 Datasheet," EPC, [Online]. Available: http://epc-co.com/epc/documents/datasheets/EPC8010_datasheet_final.pdf.

[31] B. Hughes, J. Lazar, S. Hulsey, M. Musni, D. Zehnder, A. Garrido and et al., "Normally-Off GaN-on-Si Multi-Chip Module Boost Converter with 96% Efficiency and Low Gate and Drain Overshoot," in *2014 IEEE Applied Power Electric Conference*, Dallas, TX, 2014.

[32] X. Gu, Q. Shui, C. W. Myles and M. A. Gundersen, "Comparison of Si, GaAs, SiC, and GaN FET Type Switches for Pulsed Power Applications," in *Pulsed Power Conference,* Dallas, TX, 2003.

[33] T. Heckel, C. Rettner and M. Marz, "Fundamental Efficiency Limits in Power Electronic Systems," in *2015 International Telecommunications Energy Conference*, Osaka, Japan, 2015.

[34] A. Liddow, J. Strydom, M. d. Rooij and D. Reusch, GaN Transistors for Efficient Power Conversion, Wiley, 2015.

[35] S. Aamir Ahsan, S. Ghosh, K. Sharma, A. Dasgupta, S. Khandelwal and Y. S. Chauhan, "Capacitance Modeling in Dual Field-Plate Power GaN HEMT for Accurate Switching Behavior," *IEEE Transactions on Electron Devices,* vol. 63, no. 2, pp. 565-572, 2016.

[36] E. A. Jones, F. F. Wang and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Baseed Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electrnics,* vol. 4, no. 3, pp. 707-719, 2016.

[37] "Application Note: How to Drive GaN Enhancement Mode Power Switching Transistors," GaN Systems, 2014.

[38] S. H. e. al., "High Switching Performance of a 1700-V, 50-A SiC Power MOSFET over Si IGBT/MOSFET for Advanced Power Conversion Applications," *IEEE Transactions on Power Electronics,* vol. 31, no. 7, pp. 4742-4754, 2016.

[39] M. Rodriguez, A. Rodriguez, P. F. Miaja, D. G. Lamar and J. S. Zuniga, "An Insight into the Switching Porcess of Power MOSFETs: an Improved Analytical Loss Model," *IEEE Transactions on Power Electronics,* vol. 25, no. 6, pp. 1626-1640, 2010.

[40] Y. Ren, M. Xu, J. Zhou and F. C. Lee, "Analytical Loss Model of Power MOSFET," *IEEE Transactions on Power Electronics,* vol. 29, no. 2, pp. 310-319, 2006.

[41] D. Reusch and J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride Point of Load Converter," *IEEE Transactions on Power Electronics,* vol. 29, no. 4, pp. 2008-2015, 2010.

[42] K. Ammous, H. Morel and A. Ammous, "Analysis of Power Switching Losses Accounting Probe Modeling," *IEEE transactions on Instrumentation and Measurement,* vol. 59, no. 12, pp. 3218-3226, 2010.

[43] N. Nise, Control Systems Engineering, John Wile & Sons, 2004.

[44] Z. Chen and D. Boroyevich, "Modeling and Simulatino of SiC MOSFET Fast Switching Behavior Under Circuit Parasitics," in *Proceedings of the 2010 Conference on Grand Challenges in Modeling and Simulation*, Vista, CA, 2010.

[45] Z. Chen, D. Boroyevich, R. Burgos and F. Wang, "Characterization and Modeling of 1.2kV, 20A SiC MOSFETs," in *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, 2009.

[46] "LM5113 Datasheet," Texas Instruments, [Online]. Available: http://www.ti.com/lit/ds/symlink/lm5113.pdf.

[47] R. W. M. D. Erikson, Fundamentals of Power Electronics, Springer, 2001.

[48] J. Reinert, A. Brockmeyer and R. W. A. A. De Doncker, "Calculation of Losses in Ferro- and Ferrimagnetic Materials Based on the Modeified Stienmetz Equation," *IEEE Transactions on Industry Applications*, vol. 37, no. 4, 2001.

[49] C. P. Steinmetz, "On the Laws of Hysteresis," *IEEE Transactions*, vol. 9, pp. 3-64, 1892.

[50] M. Albach, T. Durbaum and A. Brockmeyer, "Calculating Core Losses in Transformers for Arbitrary Magnetizing Currents: A Comparison of Different Approaches," in *Processings of EPE'95*, Seville, Spain, 1995.

[51] Ferroxcube, "Datasheet: E43/10/28 Planar E Cores and Accessories," in *Ferroxcube*, 2008.

[52] Ferroxcube, "Design of Planar Power Transformers," 2000.

[53] ANSYS, "Introduction to ANSYS Maxwell".

[54] M. Britschanau, "Bode - 100 Application Note: Transformer Modeling," in *Omnicron Labs*, 2016.

[55] "Little box challenge: detailed inverter specifications, testing procedure, and technical approach and testing application requirements for the little box challenge".

[56] M. Zhang, S. Member, L. Huang and W. Yao, "Circulating harmonic Current Elimination of a CPS-PWM-Based Modular Multilevel Converter with a Plug-In Repetitive Controller," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 2083-2097, 2014.

[57] M. Kasper, D. Bortis, J. W. Kolar and G. Deboy, "Hyper-efficient (98%) ad super-compact (3.3 kW/dm3) isolated AC/DC telecom supply module based on multi-cell converter approach," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014.

[58] R. Marquardt and A. Lesnicar, "A new modular voltage source inverter topology," in *European Power Electronics Conference*, 2003.

[59] "EPC2014c Datasheet," EPC.

[60] U.S. Department of Energy, "Energy Program for Security and Independence," October 2010. [Online]. Available: http://www.secnav.navy.mil/eie/Documents/DoNEnergyProgramforSecurityandIndependence.pdf.

[61] T. McCoy, "Naval Power Systems Technology Roadmap," Electric Ships Office, 2013.

[62] C. o. N. Operations, "The United States Navy Arctic Roadmap for 2013 to 2014," 2014. [Online]. Available: http://www.navy.mil/docs/USN_arctic_roadmap.pdf.

[63] S. Giannoutsos and S. Manias, "Energy management and D/G fuel consumption optimization in the power system of marine vessels through VFD-based process flow control," in *Environment and Electrical Engineering (EEEIC), 2015 IEEE 15th International Conference on*, 2015.

[64] S. Giannoutsos and S. Manias, "A Systematic Power-Quality Assessment and Harmonic Filter Design Methodology for Variable-Frequency Drive Application in Marine Vessels," *Industry Applications, IEEE Transactions on,* vol. 51, no. 2, pp. 1909-1919, 2015.

[65] C.-L. Su, W.-L. Chung and K.-T. Yu, "An Energy-Savings Evaluation Method for Variable-Frequency-Drive Applications on Ship Central Cooling Systems," *Industry Applications, IEEE Transactions on,* vol. 50, no. 2, pp. 1286-1294, 2014.

[66] G. F. Reed, B. M. Grainger, A. R. Sparacino and Z.-H. Mao, "Ship to Grid: Medium-Voltage DC Concepts in Theory and Practice," *Power and Energy Magazine, IEEE*, vol. 10, no. 6, pp. 70-79, 2012.

[67] J. Evans, "Motor Horsepower & Torque Versus VFD Frequency," Pumps & Systems Magazine, 2014.

[68] T. Neuberger, "VFDs Save Energy in Pump Applications," Pumps & Systems Magazine, 2014.

[69] Analog Devices, "ADuM5240ARZ Datasheet," [Online]. Available: http://www.analog.com/media/en/technical-documentation/data-sheets/ADUM5240_5241_5242.pdf.

[70] L. Bin, D. Piedra and T. Palacios, "GaN Power Electronics," in *Advanced Semiconductor Devices & Microsystems (ASDAM),* 2010.

[71] R. J. Kaplar, M. J. Marienella, S. DasGupta, M. A. Smith, S. Atcitty, M. Sun and et al, "Characterization and reliability of SiC- and GaN-based power transistors for renewable energy applications," in *IEEE Energytech*, 2012.

[72] K. Boutros, C. rongming and B. Hughes, "Recent advances in GaN power electronics," in *IEEE Custom Integrated Circuits Conference (CICC)*, 2013.

[73] "ADUM5210 Datasheet," Analog Devices.

[74] "35V, 22uF, TDK Capacitor," [Online]. Available: https://product.tdk.com/info/en/catalog/datasheets/mlcc_commercial_general_en.pdf.

[75] S. Kenzelmann, A. Rufer, D. Dujic, S. Member, F. Canales and Y. R, "Isolated DC/DC structure based on modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 89-98, 2015.

[76] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday and B. W. Williams, "Quasi two-level operation of modular multilevel converter for use in high-power DC transformer with DC fault isolation capability," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 108-123, 2015.

[77] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro and R. Lizana, "Circuit Topologies, Modelling, Control Schemes, and Applications of Modular Multielevel Converters," *IEEE Transactions on Power Electroncis*, vol. 30, no. 99, 2014.

[78] K. Ilves, S. Member, A. Antonopoulos and A. Norrga, "Steady State Analysis of Interaction between Harmonic COmponents of Arm and Line Quantities of Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, 2012.

[79] Y. Chen, Y. Cui, X. Wang, X. Wei and Y. Kang, "Design and Implementation of the Low Computational Burden Phase-Shifted Modulation for DC-DC Modular Multilevel Converter," *IET Power Electronics*, vol. 9, no. 2, 2016.

[80] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales and Y. Romulo de Novaes, "Isolated DC/DC Structure Based on Modular Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, 2015.

[81] I. A. Gowaid, A. M. Massoud, S. Ahmed, D. Holliday and B. W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer with DC Fault Isolation Capability," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, 2015.

[82] Z. Xing, X. Ruan, H. You, X. Yang, D. Yao and C. Yuan, "Soft-Switching Operation of Isolated Modular Multilevel DC/DC Converters for Applications in HVDC Grids," *IEEE Transactions on Power Electronics,* vol. 31, no. 4, 2016.

[83] X. Wang, G. Tang, W. Xiaoguang, Y. Chen, Y. Cui and Y. Kang, "A Quasi Zero-Current Switching DC/DC Modular Multilevel Converter (MMC) with LCL Circuit for DC Grids," in *Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015.

[84] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, Contro, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics,* vol. 30, no. 99, 2014.

[85] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday and B. W. Williams, "Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers," *IEEE Transactions on Power Electronics,* vol. 30, no. 10, 2015.

[86] Efficient Power Conversion, "EPC2016c - Enhancement Mode Power Transistor - Datasheet," 2015.

[87] K. D. T. N. a. J. L. N. Z. Zhang, "A 30-W flyback converter operating at 5 MHz," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014.

[88] X. Zhang, C. Yao, X. Lu, E. Davidson, M. Sievers, M. J. Scott, P. Xu and J. Wang, "A GaN Transistor based 90W AC/DC Adapter with a Buck-PFC Stage and an Isolated Quasi-Switched-Capacitor DC/DC Stage," in *IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014.

[89] D. M. Gobel and I. Katz, Fundamentals of Electric Propulsion: Ion and Hall Thrusters, Wiley, 2008.

[90] S. Enger, W. D. Deininger, S. Mitchell, J. Soto, M. Kendall, B. Unruh and M. L. McGuire, "Solar Electric Propulsion on ESPA-Class Satellite".

[91] NASA, "NASA Technology Raodmap: TA 2 In-Space Propulsion Technologies," National Aeronautics and Space Administration, 2015.

[92] G. A. Carr, J. C. Iannello, D. J. Hunter, J.-M. Lauenstein, S. A. Ikpe, L. L. Ludwig, C. Stell, T. Vo, L. Del Castillo, C. Wber, M. M. Mojarradi, S. Orellana and Y. Chan, "High Temperature Boost (HTB) Anode Power Supply for a Modular and SCalable Power Processing Unit," in *IEEE Aerospace Conference*, Big Sky, MT, 2016.

[93] R. R. Hofer, "High-Specific Impulse Operation of the BPT-4000 Hall Thruster for NASA Science Missions," in *46th AIAA/ASME/SAE/ASEE Joint Propulsion Conference & Exhibit*, Nashville, TN, 2010.

[94] Y. Chen, A. T. Bradley, C. J. Iannello, G. A. Carr, M. M. Mojarradi, D. J. Hunter, L. Del Castillo and C. B. Stell, "High Temperature Boost (HTB) Power Processing Unit (PPU) Formulation Study," NASA, 2013.

[95] NASA, "NASA Technology Roadmaps: TA 3 - Space Power and Energy Systems," National Aeronautics and Space Administration, 2015.

[96] J.-M. Lauenstein, M. C. Casey, K. A. LaBel, S. Ikpe, A. D. Topper, E. P. Wilcox, H. Kim and A. M. Phan, "Single-Event Effects in Silicon Carbide Power Devices," in *NEPP Electronic Technology Workshop*, Greenbelt, MD, 2015.

[97] J.-M. Lauenstein, "Challenges for Radiation Hardness Assurance (RHA) on Power MOSFETs".

[98] Freebird Semiconductor, "FBG10N30B Rad Hard e-GaN 100V, 30A Datasheet," Freebird Semiconductor, 2016.

[99] National Aeronautics and Space Administration, "NASA Technology Roadmaps TA 3: Space Power and Energy Storage," 2015.

[100] L. E. Selva, "Single Event Gate Rupture and Single Even Burnout Test Results Performed on High-Rel Fuji Power MOSFETs: 2SK4217, 2Sk4152, 2SK4155, and 2SK4158," NASA JPL, Pasadena, California, 2009.

[101] A. Lidow and K. Smalley, "Radiation Tolerant Enhancement Mode Gallium Nitride (eGaN) FET Characteristics," Efficient Power Conversion, 2012.

[102] Microsemi, "Technology Brief: Single Event Burnout and Single Event Gate Rupture in Linear Devices," Microsemi, 2015.

[103] e. a. Boruta, "A New Physics-Based Model for Understanding Single-Event Gate Rupture in Linear Devices," *IEEE Transactions on Nuclear Science*, vol. 48, no. 6, pp. 1917-1924, 2001.

[104] L. e. al., "Single Event Burnout and Avalanche Characteristics of Power DMOSFETs," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3379-3386, 2006.

[105] A. Liddow, J. Strydom, A. Nakata, M. Rearwin and M. Zafrani, "Single-Event and Radiation Effect on Enhancement Mode Gallium Nitride FETs," in *Radiation Effects Data Workshop (REDW)*, 2014.

[106] Efficient Power Conversion, "eGaN® FET Drivers and Layout Considerations," Efficient Power Conversion, 2016.