ELECTRICALLY-TRIGGERED ATOMIC EMISSION SPECTROSCOPY ON GRAPHENE/OXIDE/SILICON STRUCTURE

by

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Submitted to the Graduate Faculty of

Swanson School of Engineering in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

University of Pittsburgh

2017

UNIVERSITY OF PITTSBURGH

SWANSON SCHOOL OF ENGINEERING

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University of Pittsburgh, 2017

We present a device technology that promises chip-scale atomic emission spectroscopy operating in air ambient at room temperature with low voltage pulses. Analytes are placed on top of a graphene/SiO_2/Si (GOS) substrate and are atomized for atomic luminescence under electrical excitation. Here the graphene is designed to serve as an electron-transparent conducting electrode. When applying proper voltage pulses, the thin insulating layer (10-nm thermal grown SiO_2) breaks down inducing high local leakage current flow. Injection of kinetic electrons induces explosions, atomizing all the material nearby as well. This explosive fragmentation produces atoms in various excited states. The excited atoms then relax producing characteristic luminescence.

We have investigated the mechanisms of oxide breakdown in a GOS capacitor structure under high-field pulsed voltage drive. Four different configurations are analyzed and compared in terms of bias polarity and substrate conductivity type: inversion or accumulation bias on a GOS structure formed on n-Si or p-Si substrate. Electric field distributions in the GOS structure are analyzed under strong bias near the breakdown field regime, and the resulting quantum yield of electron impact ionization is calculated for SiO_2 and Si regions. Oxide breakdown is found to occur more readily in inversion bias than in accumulation bias due to the existence of depletion region. In the case of n-Si GOS under inversion bias, a cascade of impact ionization occur, first

in SiO_2 and then in Si, resulting in explosive melting of Si in the depletion region. In the p-Si GOS case, impact ionization occurs mostly in SiO_2 and near SiO_2/Si interface.

Post-AES study reveals significantly different breakdown damages in GOS structure under inversion high-field: highly localized, circular, protruding/deep melt explosion of Si for the n-Si GOS case; shallow, irregular, widely spread, meandering eruptions in SiO_2/Si for the p-Si GOS case. These very different damage morphologies are explained by the different carrier-multiplication processes: a cascade of electron impact ionization, escalating towards the Si depletion region for the n-Si case; carrier multiplication accumulating at the graphene side for the p-Si case.

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PREFACE

Foremost, I owe my deepest gratitude to my advisor, Professor Hong Koo Kim. I have worked with Dr. Kim over the last four years. His professional guidance, patience and immense knowledge helped me tremendously throughout my research and study. He encourages critical thinking that helps me question assumptions and view issues from multiple perspectives. He has mentored me to become a good researcher and scientist. Without his continuous encouragement, support and inspiration, this work would hardly have been completed. Special thanks to my committee members, Dr. William E Stanchina, Dr. Mahmoud El Nokali, Dr. Guangyong Li, and Dr. Youngjae Chun, for their time and valuable suggestions to my dissertation.

I would also like to thank Dr. Myungji Kim for the help and experience as a senior colleague and also Daud Emon and Yu Shi for generously sharing advices and ideas. Our friendship is a gift I will always treasure. To my friends here at Pittsburgh, Simai, Xuelian, Tieyuan, Jieni and Siyan, thank you for the wonderful times we shared, especially the fun snowboarding time on the slope of Seven Spring.

Finally, and most importantly, I would like to thank my parents in China for their unfailing love for me. Thank you mom and dad for supporting and guiding me to live the life I love and love the life I live.

1.0 INTRODUCTION

1.1 ATOMIC SPECTRA

In Bohr's model, the electrons orbiting around the nucleus have quantized discrete energy levels. The electron can transit from one orbit to another one by gaining or losing energy in terms of radiation. Radiative transitions includes allowed transition and forbidden transition. Allowed transition, also called dipole transition, need to satisfy the selection rule below:

$$\Delta \mathrm{l} = \mathrm{l}' - \mathrm{l} = \pm 1;\ \Delta \mathrm{m} = \mathrm{m}' - \mathrm{m} = 0, \pm 1$$

In which l is the orbital angular momentum, which takes the value of 0, 1, 2, …, n-1(denoted by Latin alphabet s, p, d, f, g, h…); m is the magnetic quantum number, which equals 0, ± 1, ± 2, …, $\pm$l. Forbidden transition, such as quadrupole radiation and magnetic dipole transition, has an extremely low probability which is around 10^5 times lower than allowed transition.

The wavelength of the electromagnetic radiation is determined by Rydberg formula. The radiation wavelength λ of transition from level n to level n' is given by

$$\frac{1}{\lambda} = \frac{\mu e^4 Z^2}{4\pi c \hbar^3}\left(\frac{1}{n'^2} - \frac{1}{n^2}\right)$$

In which μ is the effective mass of electron, Z is the relative atomic mass. For different n', the spectrum lines are grouped into Lyman, Balmer, Paschen, Brackett, Pfund and Humphreys series, corresponding to n' = 1, 2, 3, 4, 5, 6, respectively. For example, Lyman series

stands for transitions between 1s and np; Balmer series stands for transitions between 2s to np, 2p to ns and 2p to nd.

The total angular momentum j is the sum of orbital angular momentum l and spin s, taking the value of $l \pm 1/2$. The selection rule for transition from levels nlj to n'l'j' is

$$\Delta l = l' - l = \pm 1;\ \Delta j = j' - j = 0, \pm 1$$

The quantum numbers should be written in capital form when we characterize a whole atom instead of single electron. The spectra for neutral atom, singly ionized atoms, doubly-ionized atoms and triply-ionized atoms are denoted by I, II, III and IV respectively.

The full designation of a spectral term is written as $^{2S+1}L_J$. The number 2S+1 is called the multiplicity of the term, in which S is the total spin. The term equals 1,2,3,4 is called singlet, doublet, triplet and quartet respectively. L=0, 1, 2, 3, 4 … are denoted by S, P, D, F, G … The selection rule for quantum number J is $|L - S| \leq J \leq L + S$. For S terms, J takes 1/2; for P terms, J takes 1/2 and 3/2; for D terms, J takes 3/2 and 5/2.

The allowed transition between different levels can be plotted into Grotrian diagram, also known as energy level diagram. Figure 1 shows the emission transition of singlet sodium.

Theoretically atomic emission linewidth is infinitely close to zero, because the transition energy is fixed and discrete. However, several kinds of line broadening affect the observed atomic linewidth. One is called natural broadening, which relates the lifetime of the excited state with the Heisenberg uncertainty principle. The lifetime for most of the excited states is 0.1 ns to 10 ns. Therefore, the natural linewidth is around 10^{-4} Å. Pressure broadening causing by the collisions with between atoms and Doppler broadening causing by the relative movement between atom and detector produce line broadening of 0.01 to 0.05 Å. Overall the linewidth of atomic emission spectra is about 0.02 Å. [1]

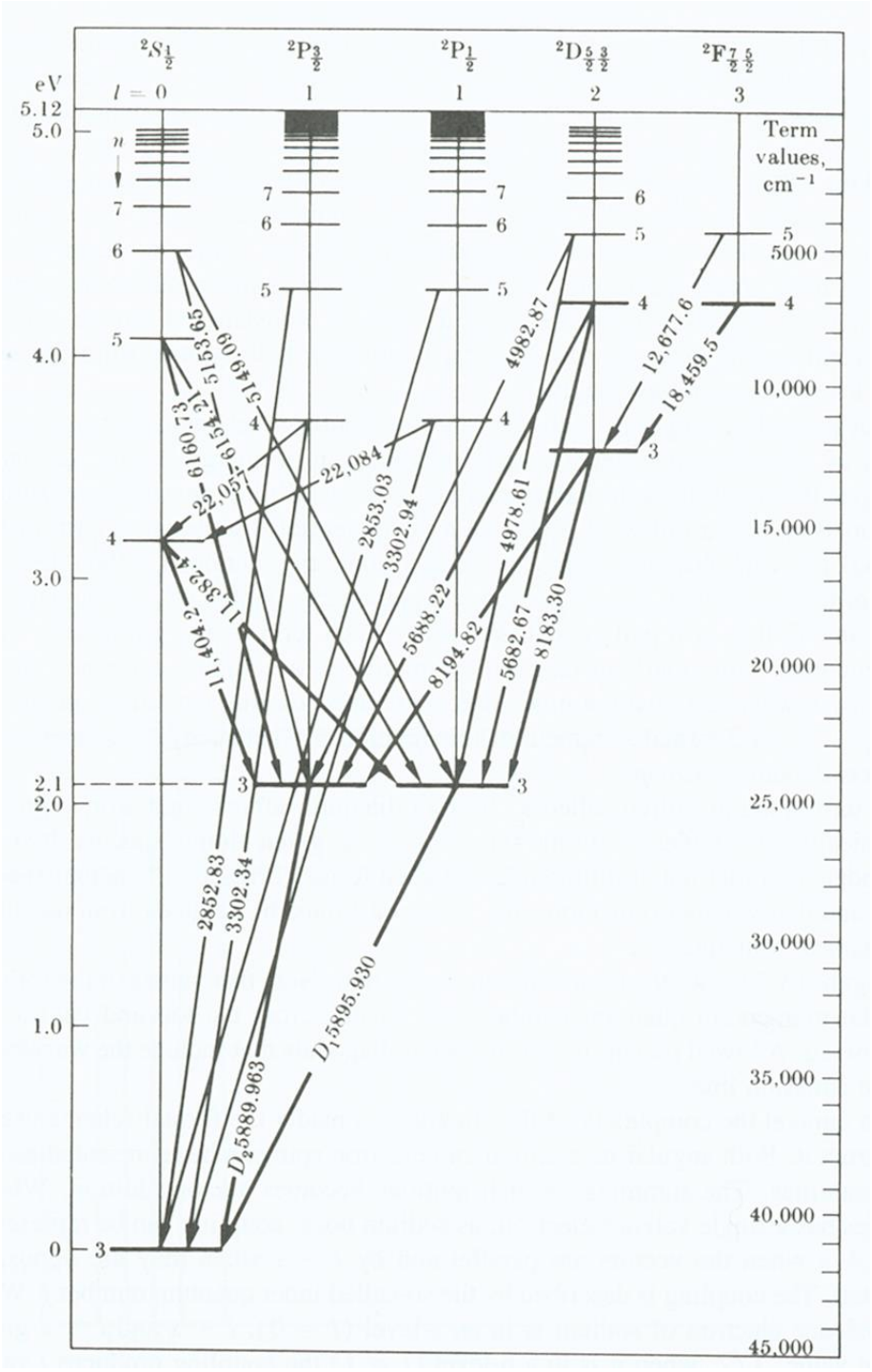

Figure 1 Grotrian diagram for singlet sodium (Na II). Emission transition are shown by arrows with wavelength in the unit of angstroms [2].

1.2 ATOMIC EMISSION SPECTROSCOPY

Atomic emission spectroscopy (AES) is a well-known technique for analyzing chemicals by obtaining the qualitative or quantitative presence of an element through the atomic emission spectra of the particular sample. To avoid the confusion with Auger electron spectrometry, optical emission spectroscopy (OES) is also referred to atomic emission spectroscopy. When the excited atoms or ions relax from a high-energy state to a low energy state, photons corresponding to the energy difference in between will emit. Usually a typical set of wavelengths will appear together depending on the electronic structure. Each element has its own identical atomic spectral line wavelength and atomic emission intensity is proportional to the amount of element. Therefore, AES has the ability to detect multiple elements at the same time.

Various sources of excitation have been developed to build atomic emission spectrometer with distinct properties and excitation efficiency. So far people are using flame source, electrical discharge source and plasma source. Among them, flame AES produces the lowest energy excitation that gives simplest atomic spectra. Therefore, the easily excited elements from the first two group of periodic table can usually be detected using flame AES. Higher energy is needed for more emission lines and more elements. Electrical discharge AES, such as spark and arc, provides higher energy input than flame AES. And plasma source gives the highest energy and the most elements. Simple spectra contain less information than line-rich spectra. However atomic lines overlapping with each other will produce spectral interference and hence requires expensive high-resolution spectrometer.

Interferences both spectral and nonspectral influence the emission spectra. Nonspectral interference mainly comes from the interaction between difference elements in the sample or the

improper emission environment. Nonspectral interferences like chemical, ionization and excitation interference can result in a decreased intensity. However spectral interference is more significant because it directly affects the spectra and introduces confusion when people analyze. One of the spectral interference is called background interference: broad emission spectra coming from the byproduct of flame combustion appear together with the sharp lines from real analyte like a background base. Another kind of spectral interference is overlapping atomic line interference. Different elements can emit in wavelength so close to each other that they cannot be distinguished by spectrometer. This interference is the major error source in high energy AES.

The basic working principle of all these AES is that an intense heat is produced to break the chemical bonds of the analyte, generates and excites the free atoms into higher energy state.

1.2.1 Flame atomic emission spectroscopy

Flame AES is usually based on a burner assembly. First a nebulizer is used to generate a spray of the liquid sample. The size of the droplet will be further reduced before entering the flame. Only around 5 percent of the vaporized solution remains after this. The high temperature in the flame will dry and atomize the sample into excited atoms. Photons generated during relaxation emission process will pass through wavelength selector (monochromator and filter), entering photo detector like charge-coupled device (CCD), charge-injection device (CID) or photomultiplier tube (PMT).

The flame is produced by the oxidation of fuel that generates the heat. The emission intensity is determined by the number of excited atoms, which is affected by the original element concentration, the amount of sample droplet, the flame component and temperature. Usually higher temperature results in higher excited energy states and more emission lines. The emission

intensity I is linearly related to the number of excited atom number N by a constant fact a, which is determined by the transition probability and photon energy E. As the Planck equation $E=hc/\lambda$ shows, the lower emission wavelength requires higher energy difference. Boltzmann distribution describes the relationship between the ratio of atom numbers N1, N2, the number of states g1, g2, the energy difference ΔE and temperature T:

$$\frac{N_1}{N_2} = \frac{g_1}{g_2} e^{-\Delta E/kT}$$

However, the excessively high temperature will ionize the easily-excited elements rather than atomizing. The electrons getting enough energy will be excited to the ion states and hence hard to return to the ground state. Figure 2 shows different type of emission and excitation. Neutral atoms produce atomic emission lines, which is very sensitive for qualitative analysis. Ionized atoms (singly or doubly ionized when using high energy excitation source) generate ion emission line, which are not reversible but less strong. Therefore, ion lines are good for quantitative analysis rather than qualitative.

1.2.2 Electrical excitation atomic emission spectroscopy

An electrical discharge is generated when high electrical field applied between two electrodes breaks down the air or inert gas in between. Direct current (DC) source is used for arc AES and alternating current (AC) source is for both arc and spark. Usually the conductive analyte serves as one of the electrode and a stable material serves as the counter, like tungsten or graphite. Since the analyte is introduced from sample electrode directly, no dissolution or dilution is needed in the sample preparation process. Even insulating materials can be analyzed by mixing them with conductive material.

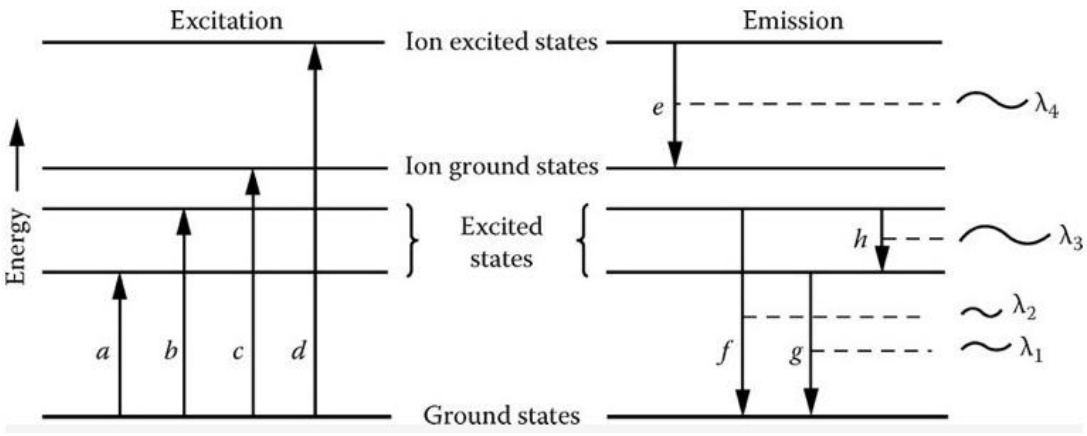

Figure 2 Atomic and ionic excitation and emission process. a and b are atomic excitation from ground states to excited states, c is ionization to ion ground state and d is the combination of ionization and excitation to ion excited state. f, g and h are atomic emission to the ground state and e is ionic emission to ion ground state [1].

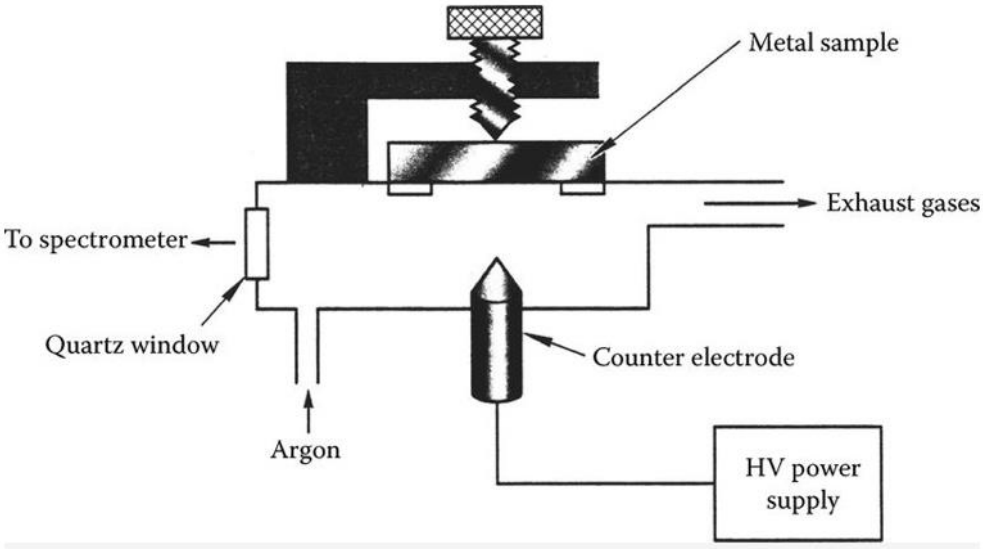

Figure 3 Spark source AES using the metal sample as the cathode and the tungsten pin as counter electrode [3].

DC breakdown needs lower voltage than AC break down. It produces atomic lines mainly and some ion lines as well. Typically, 200 V with 10 A current is applied across the electrodes as shown in the figure. Ions or plasma are generated in the small gap between two electrodes and maintained by thermal ionization. The sample is then introduced and excited both electrically and thermally. Graphite is commonly chosen as the counter electrode because of its thermal and electrical stability. Arc temperature, determined by the composition of the ions and the sample, is usually around 3000 to 8000 K and not uniform in any direction. Sample with lower ionization energy generates plasma with lower temperature.

Due to the extreme high temperature of the plasma, the sample will be burned and erode during continuous DC arc AES. When the sample serves as one of the electrode, the current tend to flow through a certain point at first. Material will be exhausted at that point, forming a pit that keeps growing till it loses conductivity. After that the plasma will start to consume another spot nearby. Therefore, the signal is unstable as many of these pits are created on the surface randomly. Although the signal is intense at first, the total emission intensity over time is relatively low with the rapid consumption. Also, the emission of different element will occur with a time delay due to the difference in volatility. Element with low melting point will evaporate faster and enter the plasma. Because of its instability, DC arc AES is mainly used for qualitative analyze.

AC spark is basically generated through the capacitor discharge on the few-millimeter gap between two electrodes in a RLC circuit. A spark source AES using the metal sample as the cathode and the tungsten pin as counter electrode is shown in Figure 3. After ignition of spark using extreme high voltage (~10kV), the operating voltage of the circuit is typically 400 to 1000 V to maintain the spark. Diode is also introduced to ensure one direction bombardment towards

the sample electrode. AC voltage frequencies are usually 200 to 600 Hz. By reducing the current flow, the system can operate in arc-like mode as well. Hundreds of sparks are generated every second that bombard the sample surface randomly, performing similar to the arc AES. Normally an inert gas ambient is used to reduce the oxidation of source and sample. Spark temperature is 10 times higher (~40000 K) than arc temperature in DC arc AES. As mentioned before, ionization occurs under high excitation energy, produce complication emission spectra. However, spark AES is more reproducible than the DC arc thus better for quantitative analysis.

1.2.3 Plasma atomic emission spectroscopy

The plasma source used in atomic emission spectroscopy includes inductively-coupled plasma (ICP), direct-current plasma (DCP), microwave-induced plasma (MIP), microwave plasma (MP) and laser-induced plasma (LIP). The plasma temperature is usually 6500 to 10000 K that most of the elements can be excited and multiple lines are produced which would require a high-resolution spectrometer because of overlapping interference.

The high temperature enables a wide range of elements analysis and also eliminates chemical interference in low temperature AES. Its stability provides longer time measurement and more accurate results for quantitative analysis. The sample introducing system is more complicated than the other two methods. Liquid sample introduction system is most commonly used. Solid sampling systems like slurry introduction, electro-thermal vaporization (ETV), spark and laser ablation are also useful depending on the sample properties. Unlike the other plasma AES, LIP use highly focused laser beam to generate plasma locally. It can be applied to all kind of samples and even remote analysis. Matrix match to eliminate spectral interference is necessary

for analyzing plasma AES results. The spectra from standard reference solution offer the information for calibration.

1.2.4 Qualitative analysis

Qualitative analysis is to identify the existence of certain element in the sample by comparing the experimental emission spectra with known atomic spectra. The Raies Ultimes (RU) lines are the emission lines with strongest intensity and should be observed in the emission spectra even at low concentrations (ppm or ppb). To confidently confirm the presence of a given element, at least RU lines should present in the spectra due to the possible overlap line interference we mentioned before. Table 1 shows the RU Lines of some common elements.

The RU lines are the most sensitive ones in atomic spectra. Therefore, it is very useful when detecting low concentration. However we cannot use it for qualitative analysis because of self-absorption effect. Self-absorption is a phenomenon that the unexcited atoms absorb the atomic emission light from same element. As the concentration grows, there would be more atoms remain unexcited. As a result, the emission intensity will drop at those wavelengths where self-absorption exists. This is also the reason why the irreversible ion lines are excellent source for quantitative analysis.

1.2.5 Temperature measurement during AES

The line-reversal method is a commonly used approach to measuring the temperature of a continuous source. The light from a filament with known temperature is focused on the source we want to measure, usually flame or plasma. A sample with known high-intensity emission line

is introduced, sodium for example. The expected emission line is monitored by a spectrometer when increasing the temperature of the filament. The temperature of the filament and the source are equal when the emission intensity drops to zero. The principle of this method is that the number of absorption transition, which stands for the incoming radiation, is equal to the number of emission transition, which stands for the source radiation [6].

1.2.6 Sample preparation

For flame AES and electrical source AES, samples are prepared to fit in the system without destroying the homogeneity and minimal matrix. Two processes are commonly taken. Dissolution is a suitable method for most of the material. As mentioned before, samples dissolved in the solution will be introduced into a nebulizer before reaching the source. Acid is often used as the solution. Ultrapure acid is needed for detecting trace elements to eliminate the impurity contaminations. Heterogeneous solid samples which are not suitable for dissolution will need a grinding process. The sample powder is then mixed with graphite powder before entering the AES system.

Table 1 RU Lines of Some Common Elements [7].

Element	Wavelength (nm)	Element	Wavelength (nm)	Element	Wavelength (nm)
Al	3961.53	Fe	3581.19	P	2535.65
	3944.03		3719.93		2553.28
	3092.71		3020.64		2534.01
	3082.16		2483.28		2554.93
Ag	3280.68	Ga	4172.06	Pb	4067.82
	3382.89		4032.98		3683.47
Au	2675.95		2943.64	Pt	2659.45
	2427.95		2874.24		3064.71
	3122.78	Ge	2651.18	Se	2039.85
B	2497.73		3039.49		8918.8
	2496.78	In	4511.32	Si	2516.12
Cd	2288.02		3256.09		2881.58
	3261.06	K	7664.91	Ti	3653.5
	3466.2		7698.98		4981.73
	6438.47		4044.14		3341.88
	3610.51		4047.2	W	4008.75
Cr	3578.69	Li	6707.84		4294.61
	4254.35		6103.64		4302.11
Cs	8521.1	Mg	2852.13		294439
	8943.5		5183.62		2946.98
	4593.18	Na	5889.95	Zn	2138.56
	4555.36		5895.92		4810.63
Cu	3247.54		3302.99	Ni	3414.77
	3273.96		3302.32		3492.96

1.3 COULOMB EXPLOSION

Coulomb explosion, also called Coulomb fragmentation or Coulomb fission, is a process driven by Coulomb force, in which a charged finite system bursts into a large number of ionic species. The size of the finite system could vary from as small as a nuclei or a cluster to as large as a droplet [8]. The Coulomb force between two charges q_1 and q_2 is defined by the Coulomb's law that

$$\mathrm{F} = k_e \frac{|q_1 q_2|}{r^2}$$

Where k_e is the Coulomb constant, r is the distance between two charges. The system is charged through external source to induce Coulomb force, mainly by intensive laser field or impinging highly charged ion [9] [10].

The Coulomb explosion is traditionally explained by the liquid drop model of Lord Rayleigh [11]. A classical spherical droplet that is charged to exceed the Rayleigh instability limit will deform to an elongated shape and then disintegrate into separate droplets which is also called Rayleigh Jets or Taylor cones [8] [12]. The Rayleigh limit is reached when the fissility parameter X exceed unity [13]. According to Lord Rayleigh, the fissility parameter X describes the ratio of repulsive and attractive energy that contributes to the fission barrier:

$$\mathrm{X} = \frac{E(Coulomb)}{2E(surface)} = \frac{Q^2}{64\pi^2 \varepsilon_0 \sigma a_0^3}$$

Where a_0 is the radius of the spherical droplet of radius, σ is the surface tension and Q is the charge [11]. Thermally activated fission over the barrier takes place when X<1. The barrier height drops to zero when X=1.

The ion energy obtained by Coulomb explosion is expressed as

$$E_{\text{coul}} = \frac{Z_1 Z_2 e^2}{4\pi\varepsilon_0 r}$$

Where Z is the charge of the ions and r is the distance between ions [10], which means that the ionized atoms should have a higher energy than this E_{coul}.

The mechanism of Coulomb explosion of a ground state hydrogen atom stimulated by high intensity laser is discussed thoroughly by Protopapas M etc. in 1997 using over-the-barrier ionization theory. When the electric field of the incident laser beam with high intensity and low frequency becomes comparable with the Coulomb field strength, the atomic potential of the atom will be distorted and a potential barrier can be formed to allow the electron tunneling within a quasi-stationary approximation [14].

About the same time, the surface Coulomb explosion process during electron beam ion trap (EBIT) experiments was also discussed [15] [16]. In the EBIT experiment, highly charged (typically larger than 40) ions (HCI) impinge the target surface with a low speed. The HCI with low kinetic energy but high internal electrostatic potential energy can create surface damage with 10 nm scale efficiently. When the ionization density of the surface atom exceeds the corresponding binding energy, particle emission can occur through mutual electrostatic repulsion, which is the so-called Coulomb explosion process. As the HCI approaches the targeted surface, within several atomic diameters distance, the Coulomb field is high enough to extract electrons from the surface. The electrons captured are kept on high-lying Rydberg state, making the ion a super-excited “hollow atom”. It can relax into ground state by ejecting electrons through Auger cascade. The ejection of electrons should be fast enough than the approaching speed of ion, so that the process can be continuously maintained. Therefore, incident ion with atomic number Z can remove at least Z number of electrons from the surface before neutralization.

According to Rayleigh [17], the maximum charge amount a sphere could hold before Coulomb explosion is calculated

$$Q = 8\pi\sqrt{\gamma\varepsilon_0 r^3}$$

Where γ is the surface tension, ε_0 = 8.85 × 10^{-12} F/m is the absolute dielectric permittivity and r is the radius of the sphere. The maximum charge amount a cylinder could hold before Coulomb explosion is:

$$Q = \pi\sqrt{6\gamma\varepsilon_0 a l^2}$$

Where l is the length and a is the radius of the cylinder. The surface energy needed for calculation is shown in Table 2 [18] [19] [20] [21] [22]. For Ag NP case, applying r = 100 nm, the Rayleigh limit $Q_{Rayleigh}$= 2.1 x 10^{-15} C. For CdSe QD case, applying r = 2 nm, the Rayleigh limit $Q_{Rayleigh}$= 5.5 x 10^{-18} C.

Table 2 Surface energy and Rayleigh limit [18] [19] [20] [21] [22].

Material	Surface energy	$Q_{Rayleigh}$
Φ49-100 nm Ag NP	0.8 J/m^2	2.1 x 10^{-15} C
Φ4 nm CdSe QD	5.4 J/m^2	5.5 x 10^{-18} C
Bulk Ag	1.2 J/m^2	
Bulk Si	2 J/m^2	
Φ200 nm (length 10 nm) Bulk SiO_2 disk	4 J/m^2	1.5 x 10^{-15} C

2.0 CARRIER TRANSPORT MECHANISM IN GOS STRUCTURE

2.1 INTRODUCTION OF GOS STRUCTURE

Metal-oxide-semiconductor (MOS) capacitor structure is a backbone of silicon microelectronics. The Si surface, when passivated by thermally grown oxide, can harbor a good quality two-dimensional electronic system (2DES). Under reverse bias an inversion channel can develop at SiO_2/Si interface, and this channel serves for carrier transport in MOS field-effect-transistor. Under illumination of light photocarriers are also generated in Si. With proper bias that provides depletion field around the interface, carrier separation occurs and photo-generated minority carriers can get trapped at the interface forming an inversion channel. In this study, we have employed a graphene/oxide/nano-channel-etched Si (GOS) capacitor structure to study atomic emission spectroscopy on a chip.

Graphene is a monolayer of carbon atoms densely packed in hexagonal lattice structure. Graphene has special electrical, optical and magnetic properties, such as high carrier mobility up to ~15000 cm^2 $(Vs)^{-1}$ at room temperature [23], quantum Hall effect under room temperature, excellent absorption of white light which renders transparency, high scalability and so forth. Recently researchers have developed various ways to produce single layer graphene with high quality, such as, mechanical and chemical exfoliation, chemical vapor deposition (CVD) on transient metal surface, and reduction of single-layer graphene oxide [24].

Graphene is a promising candidate for the new generation of conducting electrode materials because of its outstanding thermal, chemical and mechanical stability. Also, graphene is transparent over a broad spectral range, absorbing only 2.3% of incident light [25]. In this work, we are interested in using graphene as a transparent conducting electrode for optoelectronic devices.

Figure 4 shows the energy band diagrams of MOS and GOS structures with n-type and p-type silicon substrate: note that band bending occurs when Fermi level aligns. $q\Phi_M$ is the work function of metal, the minimum energy that an electron needs to gain in order to escape from metal surface. Aluminum has work function of 4.1 eV. $q\chi_S$ (~ 4.05 eV) is the electron affinity of silicon [26]. $q\chi_{ox}$ (~ 0.9 eV) is the electron affinity of silicon dioxide. The band gap of silicon is 1.12 eV and silicon dioxide has a much larger band gap, 8.5 eV. For n–type silicon with resistivity 20 to 60 Ω-cm, the Fermi level is at ~4.24 eV. For p–type silicon with resistivity 10 to 20 Ω-cm, the Fermi level locates at ~5.05 eV.

In the graphene/oxide/semiconductor (GOS) structure graphene replaces metal as a transparent conducting electrode. The Fermi level of intrinsic graphene $q\Phi_G$ is at Dirac point ~ 4.56eV and can be shifted by applying external electric field or chemical doping. However, graphene transferred on substrate will be slightly p-doped, attributed to impurities remaining on graphene. This intrinsic doping effect can be removed by applying through thermal annealing in Ar ambient under temperature of 400 ℃ [27]. The Fermi level will then shift to Dirac point.

2.2 FABRICATION OF GOS STRUCTURE

2.2.1 Wafer cleaning

We used (100) Si wafers (n-type or p-type doped: 10 ohm-cm resistivity) as substrate. The substrates were cleaned in solvent (trichloroethylene, acetone and methanol in ultrasonic bath for 5 min each) in order to remove organic contaminants. Subsequently, wafers were rinsed under running de-ionized (DI) water for 1 minute to remove remaining organic solvents. Finally, wafers were blown dried by nitrogen gas.

The RCA standard cleaning process is applied before thermal oxidation to assure the quality of silicon oxide grown on the Si substrate. For the first step of RCA standard cleaning (SC-1), a mixture of H_2O: H_2O_2 (30 wt%): NH_4OH (30 wt%) in 5:1:1 volume ratio is used to remove organic impurities and some metals. Si wafers are then immersed briefly in dilute hydrofluoric acid (49 wt % HF; diluted with DI water to 1/50 volume ratio) at room temperature in order to remove native oxide. For the next step (SC-2), a mixture of H_2O: H_2O_2 (30 wt %): HCl (38 wt %) in 6:1:1 volume ratio is used to remove remaining alkali and metals. Both solvents were heated to 70 – 80 ℃. Samples were cleaned in the hot bath solution for 10 minutes and then rinsed under running DI water for 1 minute. Cleaning was finished with nitrogen blow drying.

2.2.2 Thermal oxidation

A silicon dioxide layer with 10 nm thickness was grown in dry air ambient at 950 ℃ for 10 min. The oxide thickness (10 nm) was measured by employing a stylus-based surface profiler (Alpha-step 200) in conjunction with use of trenches/steps created by photolithography and buffered-HF-solution etching.

2.2.3 Silicon dioxide sputtering

The silicon dioxide films were deposited in an RF (13.56 MHz) magnetron sputtering unit. The RF generator with an matching network had a maximum output power of 1500 W. Sputtering target was a 50.8 mm diameter and 3.175 mm thickness silicon dioxide piece with 4N purity (99.99%). The sputtering ambient was a gas mixture of 95% argon and 5% oxygen. The sputtering pressure was maintained at 20 mTorr and the RF power was 50W. The distance between the target and the substrate was 2.0 inch. The chamber base pressure was around 2×10^{-5} Torr. Before starting the deposition, pre-sputtering was applied to remove any impurities on target and obtain stable sputtering power and pressure. Sputtering deposition was carried out room temperature without any intentional heating of substrate. We deposited a 25-nm silicon dioxide layer with 1 nm/min deposition rate.

2.2.4 Metallization

The silicon dioxide on the bottom side of the sample was removed by BHF etching. Right after that, a 100-nm aluminum layer was deposited on the backside of the sample by thermal

evaporation deposition. Deposition rate was around 1 nm/s. Annealing for Ohmic contact was carried out in nitrogen ambient at 350 ℃ for 30 min.

2.2.5 Graphene transfer

One common method of producing monolayer graphene is by exfoliation. According to the paper published in 2004 by Novoselov et al., monolayer graphene can be peeled off using Scotch tape and then transferred to another substrate [23]. This method would provide good quality graphene but with low yield and smaller size flakes. In this work, we have chosen CVD grown graphene as our source material and transferred to our substrates. CVD-grown monolayer graphene on 25-μm-thick copper foil was purchased from ACS Material. Graphene on a copper foil was cut into 1.5 mm x 1.5 mm square pieces. 2 μm PMMA (4% in anisole) was spin coated on top of graphene at 3000 rpm for 1 min. These PMMA/graphene/Cu pieces were floated (with PMMA face up) on copper etchant for 30 min to remove backside copper. After that PMMA/graphene sheets were transferred to fresh DI water for 10 min to remove the etchant residue. The transfer cleaning process was repeated three times in DI water. Graphene with PMMA on top was subsequently transferred to our destination substrate. Then the sample was baked inside an oven at 70 ℃ for 2 h. Later the PMMA/graphene/substrate was immersed into acetone and methanol in sequence for 10 min each to remove PMMA completely. After rinsing under running DI water for 2 min, our sample with graphene on it was baked at 70 ℃ for 2 hours again.

2.3 ELECTRON EMISSION AND TRANSPORT

Various transport mechanisms are possible for carriers generated in a MOS or GOS structure. Thermionic emission occurs when an electron gains enough thermal energy that exceeds work function. The current density of thermionic electron emission J_{th} is calculated according to Richardson-Dushman Equation:

$$J_{th} = -A_{th}T^2 exp\left(-\frac{\phi}{TB_{th}}\right)$$

Where T is temperature, ϕ is the work function, A_{th} and B_{th} are constants depend on material. J_{th} has an exponential dependence on the work function.

Field emission is also called cold emission in the sense that electron emission is driven by electric field, unlike the case of thermionic emission involving thermally induced hot carriers. Usually high electric field is needed to induce a triangular shape of energy barrier for electrons to transport through via a tunneling process [28]. The tunneling current density J_{FN} is calculated from Fowler-Nordheim equation [43]:

$$J_{FN} = A_{FN}E^2 exp\left(-\frac{B_{FN}}{E}\right)$$

$$A_{FN} = \frac{m_0 q^3}{8\pi h\phi m}$$

$$B_{FN} = \frac{8\pi(\phi)^{1.5}\sqrt{2m}}{3qh}$$

where E is the electric field across the oxide, ϕ is the work function difference between two sides of the tunneling barrier, q is the electronic charge, m is the electron effective mass in oxide ($m=0.4m_0$) [44]. When takeing temperature T into account, the equation becomes:

$$J_{FN} = A_{FN} E^2 exp\left(-\frac{B_{FN}}{E}\right)\frac{C}{\sin C}$$

$$C = \frac{4\pi^2 kT\sqrt{2m\phi}}{qEh}$$

The Fowler-Nordheim tunneling current through a GOS structure is plotted as a function of oxide field as shown in Figure 4. Barrier height (ϕ) between graphene and oxide is 3.66 eV and graphene electrode area is 1 mm^2. With oxide field ranging from 7 to 20 MV/cm, FN tunneling current can reach ampere level. Under high field operation, a large amount of carrier injection is initiated by FN process; a further injection, however, is limited by the space charge effect. This will be discussed in later chapters on high-field pulsed operation of GOS structure.

Fowler-Nordheim tunneling can occur across a thin oxide with thickness larger than 5 nm. When the silicon oxide thickness goes below 4 nm, the tunneling process is dominated by direct tunneling, which occurs through a rectangular/trapezoidal barrier under relatively low external applied voltage. The direct tunneling current density is

$$J_T = \frac{2q}{h(2\pi)^2}\int_0^\infty \Delta f \left(\iint P dk_y dk_z\right) dE$$

where P is the tunneling probability, Δf is the probability difference of states being occupied in and outside the barrier, k is the wave vector in the plane of barrier.

After approximation, we have:

$$J_T = A_T E^2 exp\left(-\frac{B_T}{E}\right)$$

$$A_T = \frac{q^3}{16\pi^2 h\phi}$$

$$B_T = -\frac{4\pi(\phi)^{1.5}\sqrt{2m}}{3qh}\left[1-\left(1-\frac{qV_{ox}}{\phi}\right)^{1.5}\right]$$

where V_{ox} is the voltage across the oxide layer. After approximation the direct tunneling current can be expressed analytically as a function of applied voltage, except for the low voltage regime Vox < 1V [28].

A scattering-free ballistic transport is possible in vacuum or in a transport medium whose channel length is smaller than the mean free path. The mean free path is calculated as follows:

$$\langle x \rangle = \frac{k_B T}{\sqrt{2}\pi d^2 P}$$

The mean free path in air ambient is around 65 nm. The carrier transport in highly insulating medium (such as in vacuum) is governed by the space-charge-limited effect, and the resulting current density of a scattering-free transport is determined by the Langmuir-Child's Law:

$$\mathrm{J}_{LC} = \mathrm{A}_{LC}\mathrm{V}^{1.5}$$

$$\mathrm{A}_{LC} = \frac{4\varepsilon_s}{9d^2}\sqrt{\frac{2q}{m_e}}$$

Where q is the electron charge, d is the distance of transport, m_e is the electron mass and ε_s is the dielectric constant of the transport media. J_{LC} has the power-dependence of 1.5 to the applied voltage V [29]. For q = 1.6×10^{-19} C, d = 10 nm, m_e = 9.1×10^{-31} kg, ε_s = 8.85 x 10^{-12} F/m, J_{LC} = 8.25×10^{12} A/m^2 at 50 V and 2.33×10^{13} A/m^2 at 100 V.

When electrons emit and transport in bulk solid such as semiconductor or insulator, the Langmuir-Child's Law needs to be revised taking into account the collisional/scattering effects.

Mott-Gurney's corresponds to the form of space-charge-limited transport that takes into account this scattering effect. The relationship between applied voltage V and current density J_{MG} in this case is

$$J_{MG} = A_{MG}V^2$$

$$A_{MG} = \frac{9\varepsilon_s\mu}{8d^2}$$

where ε_s is the dielectric constant of the transport media, μ is the mobility of electrons in this media and d is the distance of transport. The voltage-dependence of J is now raised to the power of 2 from 1.5.

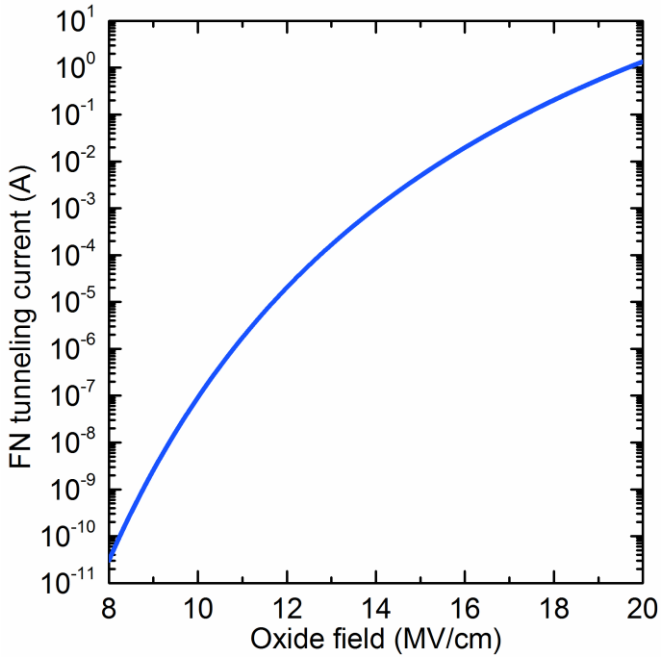

Figure 4 Oxide field versus Fowler-Nordheim tunneling current in GOS structure with graphene area of 1 mm^2.

3.0 OXIDE BREAKDOWN

3.1 INTRODUCTION

3.1.1 Models of oxide breakdown

Gate oxide thickness t_{ox} is reaching its low limit for high transistor current and speed these days. Oxide breakdown process is an important issue related to the reliability of a dielectric layer. With the increase of electrical field, the damage in oxide layer extends through interface traps, bulk traps, low level stress induced leakage and finally leads to catastrophic breakdown. Two important parameters for testing the reliability of gate oxide are the time-to-breakdown (t_{BD}) and charge-to-breakdown (Q_{BD}) [30].

Earlier, based on the thermochemical model (E model), log t_{BD} is found to be linearly related to the electric field E, as shown in the equation below. In this model the oxide layer is treated to be a collection of dipoles.

$$\log(t_{BD}) \propto \frac{\Delta H_0}{k_B T} - \beta E$$

ΔH_0 and β are the activation energy and the field acceleration factor respectively. However, ΔH_0 and β can be measured experimentally for only thick oxide under long-term low-field stress condition [31].

Another method, called hole-induced breakdown model (1/E model), explains the breakdown process by the accumulation of trapping states or defects in oxide. Initiated by localized trapped holes, the increase of current density and trapping state eventually cause breakdown. The trapped holes are localized near the cathode within 10^{-6} of the total oxide area [32] [33]. Fowler-Nordheim (FN) tunneling and impact ionization is involved in the relationship between t_{BD} and 1/E.

$$t_{BD} = \tau_0 e^{(B+H)/E}$$

$$Q_{BD} = \int_0^{t_{BD}} J_{FN}\, dt$$

In which τ_0 is 10^{-11} s; B is the B_N in equation of FN tunneling current density J_{FN} (equation shown in chapter 2.2); H is measurable through experiment [34] [35]. The oxide can sustain 100 times greater density of electrons than holes. Although electron trapping is not the major cause for oxide breakdown [32] [33], trapped electrons and holes can recombine to create neutral traps and defects that accelerate breakdown through charge assisted tunneling and trap assisted tunneling.

Both E model and 1/E model correlate oxide breakdown to electric field. However, polarity dependence that device under positive gate voltage has a higher Q_{BD} than negative voltage [36] is consistently observed. Also, the stress-induced leakage current (SILC), which is produced by the generation of traps, shows asymmetric plot against electric field but symmetric plot against voltage.

Based on hole-induced breakdown model, anode hole injection (AHI) model, which is both field-driven and voltage-driven model, is developed to explain high field breakdown. The injected electron can create electron-hole pairs through impact ionization as shown in Figure 5.

The Q_{BD} in AHI is describe as

$$Q_{BD} = \frac{Q_p}{\alpha_p} exp\left(\frac{B_N}{E}\Phi_p^{3/2}\right)$$

Where Q_p is the critical substrate hole fluency, which is 0.1 C/cm^2 for oxide thicker than 4.5 nm. And α_p (~0.08) is the probability of hole generation.

For FN tunneling we need to take into account the electron scattering within oxide:

$$q\Phi_p = E_{g,oxide} - qE\lambda\left\{1 - exp\left[-\frac{1}{\lambda}\left(t_{ox} - \frac{\Phi_b}{E}\right)\right]\right\}$$

Where λ (~1.5 nm) is the mean free path for electrons in oxide; $q\Phi_b$ is the barrier height. For direct tunneling

$$q\Phi_p = E_{g,oxide} - q\Phi_b - qV_{ox}$$

Overall Q_p will decrease with the increase of oxide voltage V_{ox} and decrease of oxide thickness t_{ox} which is because the thin oxide has a weaker tolerance of trapped holes. When the oxide goes thinner than 4.5 nm, direct tunneling current of valence-band electron becomes dominant in the substrate current. Therefore, the current density measured from the sample is no longer the leakage current that can provide useful information on oxide breakdown [37].

Some post-breakdown study reveals that the final cause of breakdown is thermal melting [38]. But some also suggests that the bond breaking by kinetic tunneling electrons forms a conductive path from anode to cathode. Oxide breakdown eventually occurs because of the capacitor discharge through these channels [39]. It is noteworthy that the electric field applied to our GOS structure under voltage pulses far exceeds the breakdown field strengths of SiO_2 and Si.

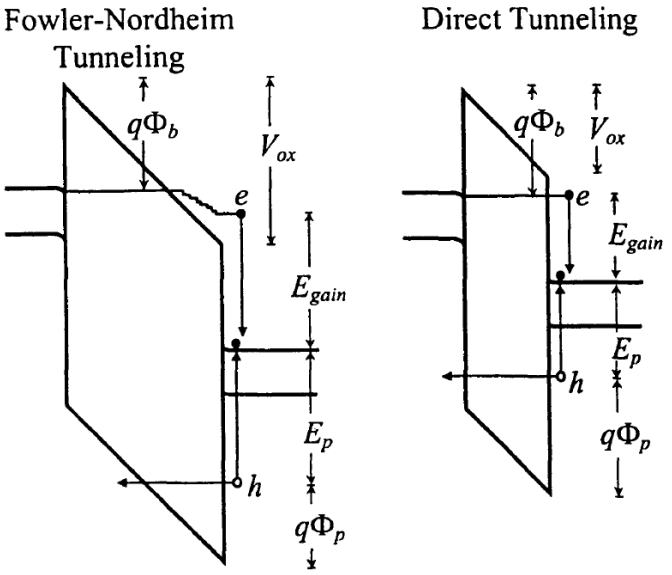

Figure 5 Anode Hole Injection process in the case of Fowler-Nordheim tunneling ($V_{ox}>q\Phi_b$) and direct tunneling ($V_{ox}<q\Phi_b$). The electron tunneled through oxide barrier transfer its energy E_{gain} towards a deep valence band electron. A hole would be created after that electron is excited to conduction band, which can tunnel through oxide as well [30].

3.1.2 Thermal breakdown and electric breakdown

Thermal breakdown and electrical breakdown are two types of oxide breakdown explained by different mechanisms. Thermal breakdown, which is caused by Joule heating, occurs uniformly over the electrode-covered-oxide area. Electrical breakdown, which is triggered by accumulated charges, produce local damage in terms of small size channels with sparks appearing simultaneously [40]. Breakdown process is initiated by the increase of electrical conductance. Instead of heating during thermal breakdown, existence of channels in oxide is the cause of conductance increase. Breakdown destructions are mainly melting (in thick oxide) and evaporation (in thin oxide). The damages are initiated by the discharge of electrostatic energy stored in the sample through those channels and enlarged by the follow-up current. Another difference between thermal and electrical breakdown is that, the breakdown field for thermal breakdown is definite and fixed but electrical breakdown occurs in a wide range of fields [41].

Klein's group found that thermal breakdown is typically observed under dc low voltage bias, while electrical breakdown is a chance event occurring under high voltage pulses. There is a limit called maximum thermal breakdown voltage V_{dm} that when applied voltage V is below V_{dm} the temperature increased by the Joule heating is negligible. As the voltage increases, electrical breakdown becomes dominant. The breakdown voltage is not influenced by pulse width but will increase a little bit if the temperature drops. There is no clear transition from thermal breakdown to electrical breakdown when increasing the voltage from below V_{dm} to above and in between there is a voltage range that both types of breakdown can occur. Electrical breakdowns are not thermal process in oxide because the leakage current before breakdown is small and there is no observable temperature increase. However, these two processes occur at the same time in most of the case [42].

When the oxide breakdown is triggered by electrical pulses, pulse thermal breakdown voltage V_{pm} is lower than electrical breakdown voltage V_B. Overall $V_{pm} < VB < V_{dm}$. In Figure 6, thermal breakdown with variable pulse duration and electric breakdown field is plotted as function of temperature. Under room temperature, much stronger field is required for thermal breakdown when the pulse width is shorter than 1 μs [40]

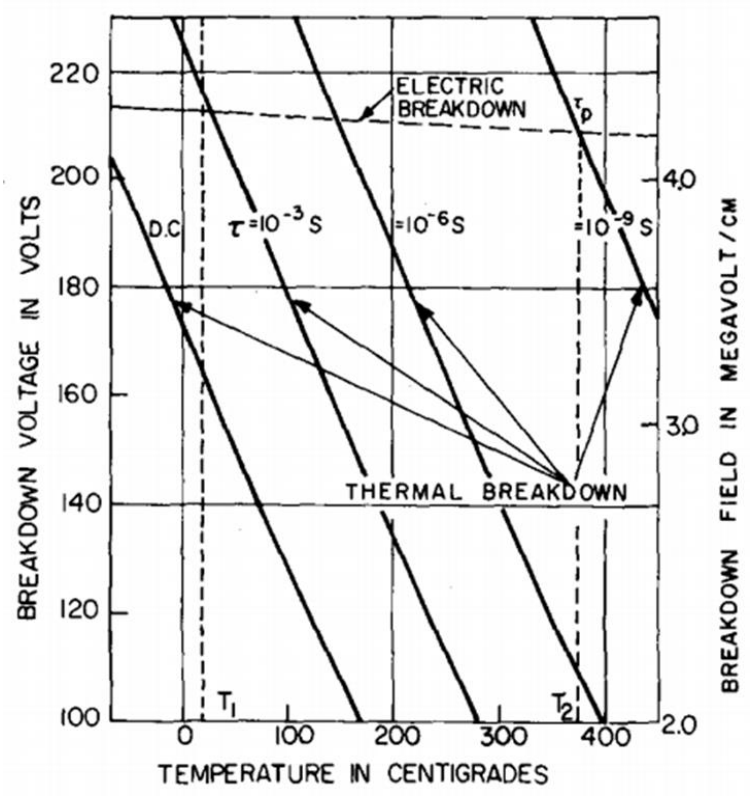

Figure 6 Thermal pulse breakdown with various pulse widths and electrical pulse breakdown field as function of temperature [40].

3.2 GOS STRUCTURE UNDER ELECTRIC FIELD

3.2.1 Graphene work function shift under electric field

Graphene is a promising 2D material at electronic and atomic levels because of its outstanding thermal, chemical and mechanical stability. Evolving from carbon nanotube, graphene is a hexagonal lattice consisting of carbon atoms in two dimensions. Graphene is transparent to electrons while impermeable to atoms. And it also has a low absorption of light over a broad spectral range, absorbing only 2.3% of incident light, which makes graphene a good candidate for flexible transparent conductive electrode in optoelectronic devices [45].

Our group reported the photodetection properties of a graphene/oxide/silicon (GOS) structure with a nano-channel [46] [47]. It demonstrates a high responsivity of ~1.0 A/W in a broad spectral range, with a UV-enhanced performance of 384% internal quantum efficiency. Under inversion bias, the electrons transport through the void channel at low bias voltage without collision before being captured by graphene electrode. People also found that the photo-generated carriers in the graphene photodetectors are transported intrinsically different from those in the semiconductor photodetectors [48]. The carriers could easily overcome the potential barrier of monolayer graphene, making it possible for high bandwidth photo detection without external bias.

Intrinsic (undoped) graphene can be considered as a semiconductor with zero bandgap. The Fermi level of the intrinsic graphene is located on the connection point (Dirac point) of conduction band and valence band. The work function of monolayer intrinsic graphene in GOS structure is measured to be 4.56 eV at room temperature [52]. However, its Fermi level can be shifted up or down by applying external electric field, resulting in n-doped or p-doped graphene,

respectively [49] [50]. Graphene can also be doped by adsorbing chemicals such as BV for n-type and $AuCl_3$ for p-type [51].

Graphene work function under electric field (ϕ_{gr}) is the sum of intrinsic graphene work function ($\phi_{ingr} = 4.56\ eV$) and graphene fermi level shift (ΔE)

$$\phi_{gr} = \phi_{ingr} + \Delta E$$

For monolayer graphene, the fermi level shift (ΔE_1) can be calculated (positive for negative gate voltage, negative for positive gate voltage) [49]

$$\Delta E_1 = \pm\hbar|v_F|\sqrt{\pi n_s}$$

which involves reduced plank constant ($\hbar = 6.58 \times 10^{-16} eV \cdot s$), Fermi velocity ($v_F = 1.1 \times 10^8 cm/s$) and carrier concentration ($n_s = Q/q$) in which (Q) is space charge density and (q) is elementary charge. Fermi velocity

For bilayer graphene, the fermi level shift (ΔE_2) is (positive for negative gate voltage, negative for positive gate voltage) [49]

$$\Delta E_2 = \pm\hbar^2\pi n_s/2m^*$$

Which involves effective mass of carrier in BLG ($m^* = 0.033m_e$) in which ($m_e = 5.11 \times 10^5 eV/c^2$) is the electron rest mass.

We plotted the graphene work function versus gate voltage ranging from 0 to 5 V in our GOS structure under reverse bias (positive gate voltage) for both monolayer graphene and bilayer graphene in Figure 7. It turns out that the amount of work function shift is significantly smaller for bilayer/multilayer graphene case. As the number of graphene layer increases above 2, the graphene performs similar to 3D material (graphite) rather than 2D material. In other words, the work function shift by electric field becomes negligible for multilayer graphene. Therefore,

since 8-layer-graphene is used in most of our experiment, we will fix the graphene work function at 4.56 eV in our further simulation.

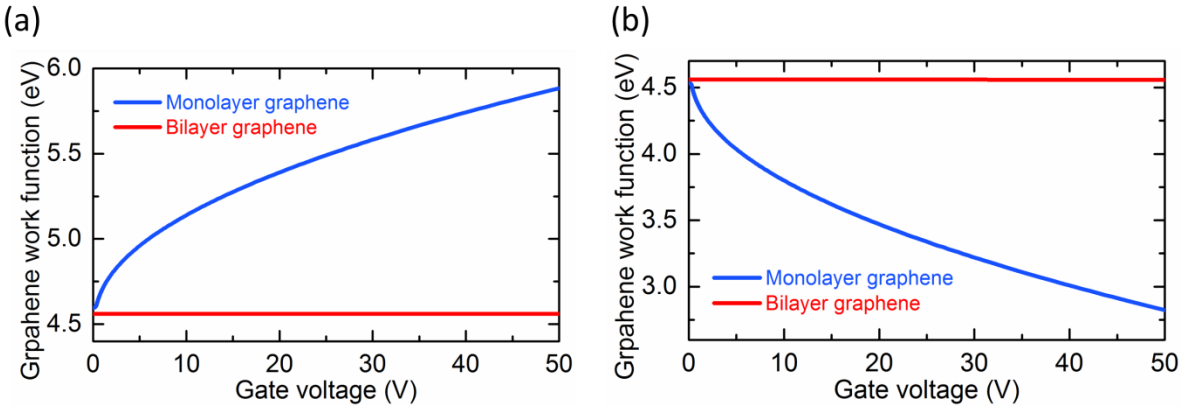

Figure 7 Gate voltage versus graphene work function in graphene/SiO_2/ Si structure with monolayer graphene and bilayer graphene under inversion bias on (a) p-Si substrate and (b) n-Si substrate.

3.2.2 Electric field and charge distribution in GOS structure

Graphene/SiO_2/Si (GOS) structure is similar to conventional MOS structure in the sense that graphene serves as metal electrode in this case. As we discussed before, multilayer graphene has a work function of 4.56 eV under room temperature. Assuming all the thin films and layers are isotropic and uniform, gate voltage (V_g) is the sum of flat band voltage (V_{FB}), surface potential (φ_s) and oxide potential (V_{ox}) [53] [54]

$$V_g = V_{FB} + \varphi_s + V_{ox}$$

Flat band voltage (V_{FB}) = graphene work function (ϕ_{gr}) – silicon work function (ϕ_{Si})

$$V_{FB} = \phi_{gr} - \phi_{Si}$$

By using the parameters shown below, we can obtain the work function of silicon substrate. Silicon's electron affinity at room temperature (χ_{Si}) is $4.05\ eV$. Silicon band gap at room temperature (E_g) is 1.12 eV. Intrinsic carrier concentration of silicon under room temperature is $n_i = 1.45 \times 10^{10} cm^{-3}$ [55]. Majority carrier concentration ($N_D\ or\ N_A$) can be calculated $N = 1/q\mu\rho$ by using carrier mobility of electron $\mu_n = 1352\ cm^2/v \cdot s$ and hole $\mu_p = 457\ cm^2/v \cdot s$ [56]. For n-type and p-type silicon with resistivity of $10\ \Omega \cdot cm$, the work function is

$$\phi_{nSi} = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} - \frac{kT}{q}\ln\frac{N_D}{n_i} = 4.31\ V$$

$$\phi_{pSi} = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} + \frac{kT}{\mathrm{q}}\ln\frac{N_A}{n_i} = 4.91\ V$$

The space charge density (Q_s) at the interface of silicon and oxide can be obtained from surface potential and dopant concentration. Same amount of charge will appear on at the interface of oxide and graphene.

$$Q_s = -\varepsilon_0 \varepsilon_{Si} E_{Si} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si} qp}{\beta}} \left[\left(e^{-\beta\varphi_s} + \beta\varphi_s - 1 \right) + \frac{n}{p} \left(e^{\beta\varphi_s} - \beta\varphi_s - 1 \right) \right]^{1/2}$$

$$\beta = \text{q/KT}$$

As we plotted in Figure 8, under low field where $Q_s \propto \sqrt{\varphi_s}$, surface charge density is low due to the depletion field. For high field operation, the inversion layer starts to form at the inter face of silicon and oxide where $Q_s \propto -e^{\beta\varphi_s/2}$. Knowing silicon dielectric constant $\varepsilon_{Si} = 11.9$ [56], hole and electron concentrations in p-Si can be obtained that $p = N_A = 1.368 \times 10^{15} cm^{-3}$ and $n = {n_i}^2/\text{N}_A = 1.537 \times 10^6 cm^{-3}$. Electron and hole concentrations in n-Si are $n = N_D = 4.623 \times 10^{14} cm^{-3}$ and $p = {n_i}^2/N_D = 4.548 \times 10^6 cm^{-3}$.

Oxide potential (V_{ox}) = space charge density (Q_s) x Oxide thickness (d) / (vacuum permittivity (ε_0) x oxide dielectric constant (ε_{ox}))

$$V_{ox} = Q_s d/\varepsilon_0 \varepsilon_{ox}$$

Where oxide thickness is $d = 10\, nm = 10^{-6}\, cm$ and oxide dielectric constant is $\varepsilon_{ox} = 3.9$ [56].

Depletion width (W) in silicon under reverse bias is

$$W = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si} \varphi_s}{qN}}$$

Surface potential (φ_s), surface charge density (Q_s), electric field strength at the interface of silicon and oxide (E_{Si}) and depletion width (W) are plotted as function of reverse gate voltage (V_g) from 0 V to 50 V for p-GOS in Figure 9 and n-GOS in Figure 10. The difference of these four parameters between n-GOS and p-GOS is marginal. For both p-GOS and n-GOS, the surface potential saturates at high gate voltage at ~ 1 V. Depletion width saturates at high gate voltage at1 μm for p-GOS and 1.6 μm for n-GOS. The surface charge density at 50 V is ~2 x 10^{-5}

C/cm^2 for both p-GOS and n-GOS. Accordingly, the electric field at the interface of Si and SiO_2 is ~16 MV/cm at 50 V which is ~ 3 times smaller than the oxide field, which is determined by the dielectric constant ratio of Si (11.9) and SiO_2 (3.9).

The space charge density on the graphene side (Q_{gr}) is equal to the density on the silicon side (Q_{Si}) which is consist of the charge density in the inversion region (Q_{inv}) and depletion region (Q_{dep}).

$$Q_{gr} = Q_{inv} + Q_{dep} = Q_{Si}$$

The charge in the depletion region is

$$Q_{dep} = qNW$$

According to literature, the inversion layer thickness in Si (t_{inv}) [57]

$$t_{inv} = \frac{5 \times 10^{-7}}{1 + \left[\left(V_g + 3V_T\right)(V)/2 \times 10^6 t_{ox}(cm)\right]^{0.7}}\ cm$$

Threshold voltage (V_T) is the voltage when the device start to enter inversion region

$$V_T = V_{FB} + 2\varphi_B + t_{ox}\sqrt{\frac{4qN\varphi_B}{\varepsilon_0 \varepsilon_{Si}}}$$

In which $\varphi_B = 0.3\ V$ is the potential difference between intrinsic level (E_i) and fermi level (E_F) of silicon.

As shown in Table 3 and Table 4, the inversion layer thickness for both p-GOS and n-GOS under 10 V, 30 V and 50 V gate voltage biases are 1.1 nm, 0.6 nm and 0.5 nm, respectively. The strong electric field ~ 16 MV at the interface of Si and SiO_2 are confined within the narrow inversion layer with thickness of less than 1 nm. Then drop to the maximum electric field within depletion region ($E_{dmax} = Q_{dep}/\varepsilon_0 \varepsilon_{Si}$), which is in the order of 10^4 V/cm.

One dimensional Poisson equation shows the relation among potential (φ), distance (x) and the total space-charge density (ρ):

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{\varepsilon_0 \varepsilon_{Si}}$$

The potential in the depletion region as a function of distance can be obtained by integrating Poisson's equation:

$$\varphi = \varphi_s \left(1 - \frac{x}{W}\right)^2$$

The electric field in the depletion region as a function of distance can be obtained:

$$E = -\frac{2\varphi_s}{W}\left(1 - \frac{x}{W}\right)$$

The electric field distribution nears the interface of silicon and oxide in 8LG/SiO_2/p-Si structure under +20 V bias is plotted as a function of the distance from interface in Figure 11 as an example. The strong electric field is confined within the inversion layer of 8 Å and sharply decreases to level of 10^4 V/cm when entering depletion region. Oxide layer takes over 95 % of the voltage drop when the gate voltage increases above 20 V.

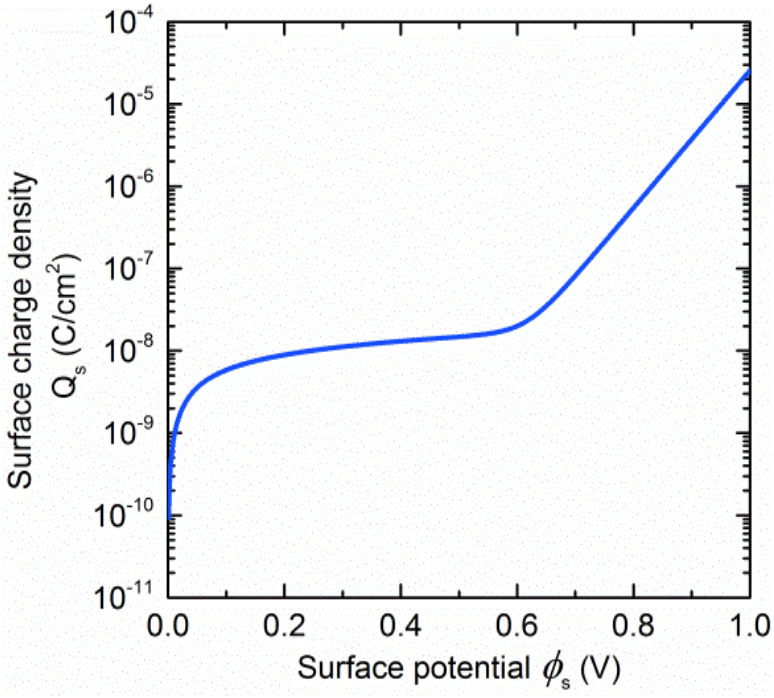

Figure 8 Surface potential versus surface charge density under reverse bias.

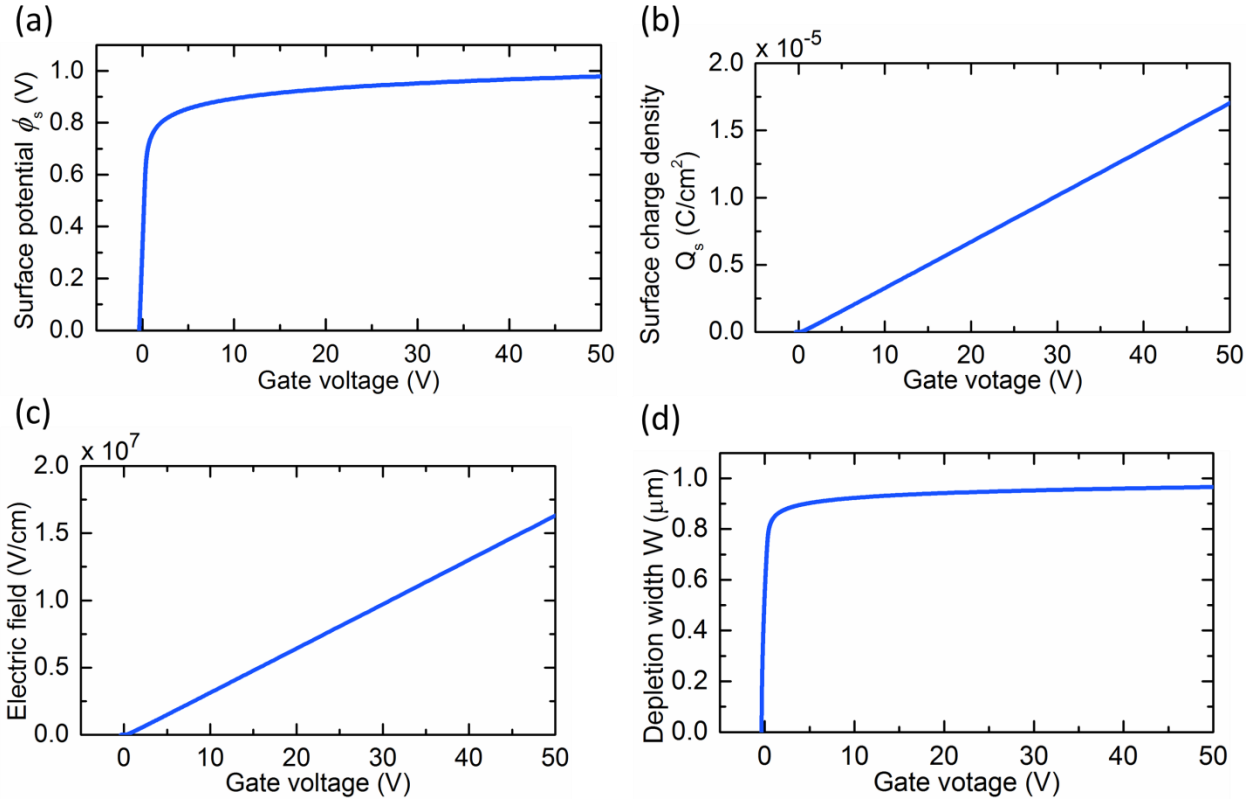

Figure 9 Surface potential (a), surface charge density (b), electric field at the Si/SiO_2 interface (c) and depletion width (d) of 8LG/(10 nm)SiO_2/p-Si under reverse bias. Gate electrode is positively biased from -0.5 V to 50 V.

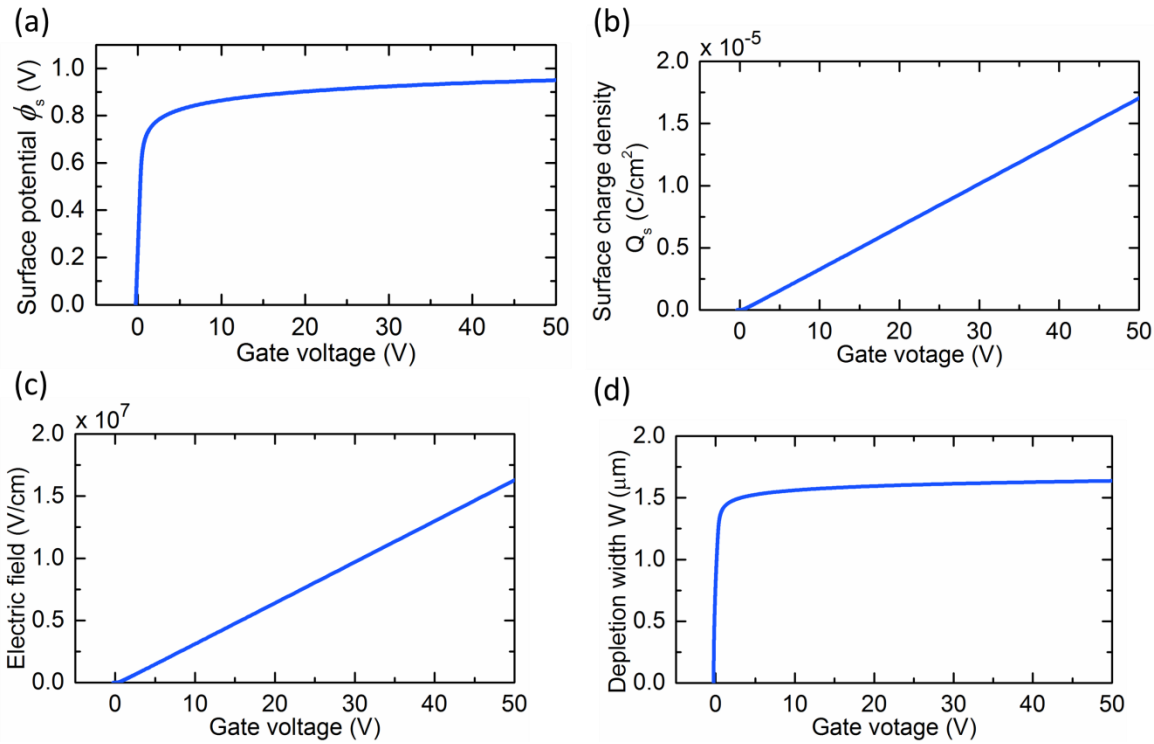

Figure 10 Surface potential (a), surface charge density (b), electric field at the Si/SiO_2 interface (c) and depletion width (d) of 8LG/(10 nm)SiO_2/n-Si under reverse bias. Gate electrode is negatively biased from -0.5 V to 50 V.

Table 3 Sample information and simulation parameters used for 8LG/10 nm SiO_2/p-Si.

Information	Parameters		
Hole concentration in p-Si:$p = N_A$	$1.368 \times 10^{15} cm^{-3}$		
Electron concentration in p-Si: n	$1.537 \times 10^{6} cm^{-3}$		
p-type silicon work function: ϕ_{pSi}	$4.91\ V$		
Flat band voltage: V_{FB}	$-0.35\ V$		
Threshold voltage: V_T	$0.27\ V$		
Voltage	10 V	30 V	50 V
Surface potential: φ_s	0.89 V	0.95 V	0.98 V
Oxide voltage: V_{ox}	8.76 V	28.7 V	48.67 V
Oxide field: E_{ox}	$8.76\ MV/cm$	$28.7\ MV/cm$	$48.67\ MV/cm$
Surface charge density: Q_s	$3.27 \times 10^{-6} C/cm^2$	$1.02 \times 10^{-6} C/cm^2$	$1.78 \times 10^{-5} C/cm^2$
Electric field at Si/(SiO_2) interface: E_{Si}	$3.13\ MV/cm$	$9.73\ MV/cm$	$16.4\ MV/cm$
Depletion width: W	$9.23 \times 10^{-5} cm$	$9.52 \times 10^{-5} cm$	$9.65 \times 10^{-5} cm$
Depletion charge density: Q_{dep}	$2.02 \times 10^{-8} C/cm^2$	$2.08 \times 10^{-8} C/cm^2$	$2.11 \times 10^{-8} C/cm^2$
Maximum depletion electric field: E_{dmax}	$1.92 \times 10^{4} V/cm$	$1.98 \times 10^{4} V/cm$	$2.00 \times 10^{4} V/cm$
Inversion layer thickness: t_{inv}	1.18 nm	0.64 nm	0.47 nm

Table 4 Sample information and simulation parameters used for 8LG/10 nm SiO_2/n-Si.

Information	Parameters		
Electron concentration in n-Si: $n = N_D$	$4.623 \times 10^{14} cm^{-3}$		
Hole concentration in n-Si: p	$4.548 \times 10^{6} cm^{-3}$		
n-type silicon work function: ϕ_{nSi}	$4.31\ V$		
Flat band voltage: V_{FB}	$0.25\ V$		
Threshold voltage: V_T	$0.86\ V$		
Voltage (reverse bias)	$10\ V$	$30\ V$	$50\ V$
Surface potential: φ_s	0.86 V	0.93 V	0.95 V
Oxide voltage: V_{ox}	8.89 V	28.82 V	48.8 V
Oxide field: E_{ox}	8.89 MV/cm	28.82 MV/cm	48.8 MV/cm
Surface charge density: Q_s	$3.24 \times 10^{-6} C/cm^2$	$1.01 \times 10^{-6} C/cm^2$	$1.70 \times 10^{-5} C/cm^2$
Electric field at Si/SiO_2 interface: E_{Si}	3.10 MV/cm	9.70 MV/cm	16.3 MV/cm
Depletion width: W	$1.56 \times 10^{-4} cm$	$1.61 \times 10^{-4} cm$	$1.64 \times 10^{-4} cm$
Depletion charge density: Q_{dep}	$1.15 \times 10^{-8} C/cm^2$	$1.19 \times 10^{-8} C/cm^2$	$1.21 \times 10^{-8} C/cm^2$
Maximum depletion electric field: E_{dmax}	$1.09 \times 10^{4} V/cm$	$1.13 \times 10^{4} V/cm$	$1.15 \times 10^{4} V/cm$
Inversion layer thickness: t_{inv}	1.08 nm	0.62 nm	0.46 nm

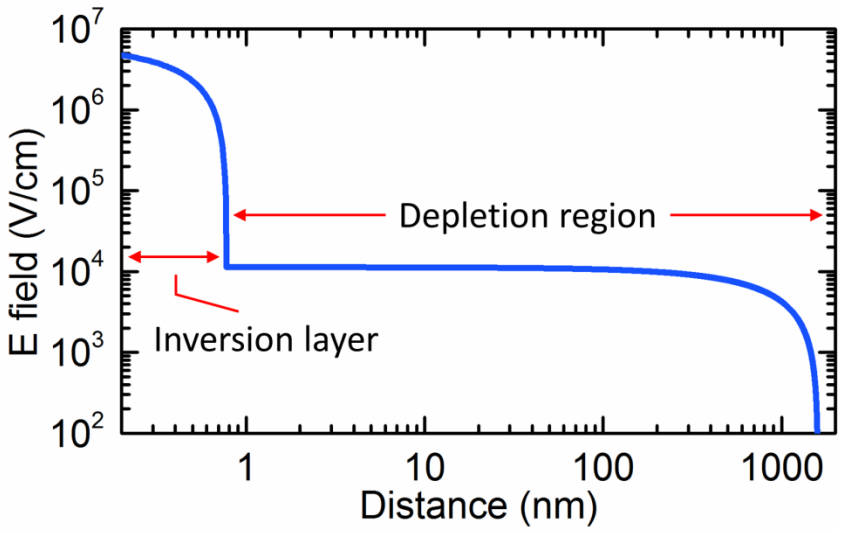

Figure 11 In 8LG/SiO2/n-Si structure under -20 V voltage bias, electric field distribution near the interface of silicon and oxide plot versus the distance starting from interface.

3.3 IMPACT IONIZATION IN GOS STRUCTURE

We investigated underlying mechanisms of oxide breakdown in a GOS structure under high-field voltage pulses of different polarities: inversion or accumulation bias on p-Si or n-Si substrate. Each configuration involves a different amount of accumulation or inversion charges with or without forming a depletion region in the capacitor structure. We have analyzed the field distributions occurring in the GOS structure in the previous section. In this section, we discuss about carrier multiplications, the governing mechanisms of oxide breakdown, which results in explosive melting and atomic emission.

3.3.1 Impact ionization under low field

Impact ionization, also called avalanche multiplication, is the process that an energetic charge carrier (electron or hole) generates new electron-hole pairs by losing its energy through a collisional process. Ionization rate is defined as the number of electron-hole pairs generated per carrier per unit distance traveled. The electron ionization rate in Si is known to be greater than that of hole, although they tend to converge at very high field. The threshold energy that a particle must gain from electrical field for impact ionization to occur is 1.5 times of E_g. E_g is the bandgap energy (1.12 eV for Si). Therefore, minimum particle energy of 1.68 eV is needed for effective ionization in Si. In general, ionization rate depends on the energy of the carrier, which is usually gained by an externally-applied electrical field.

As shown in the expression below, the ionization rate (α) is related to effective ionization energy under high-field (E_i), threshold field for carrier to overcome the barrier created by

thermal (F_{kT}), optical-phonon (F_r) and ionization scattering (F_i) and applied electric field (E) [58] [59].

$$\alpha(E) = \frac{qE}{E_i}\exp(-\frac{F_i}{E\left(1+\frac{E}{F_r}\right)+F_{kT}})$$

$$\frac{F_i}{F_{kT}} = \frac{E_i}{kT}$$

According to Grant [58] [60], For Si under room temperature, the ionization rate of electron (α_n) and hole (α_p) is plotted in Figure 12 (a) using the parameters provided in Table 5.

Another common way of calculating ionization energy is the empirical expression of Chynoweth [61]:

$$\alpha(\mathrm{E}) = \mathrm{a}\exp\left(-\frac{b}{E}\right)$$

Constant a and b can be obtained by data fitting. According to Grant [60], for electric field greater than, the ionization rates of electron (α_n) and hole (α_p) are shown in the Table 6. The parameters are only valid for low field (less than 7 MV/cm) before silicon breakdown. As we plotted in Figure 12(b), if we extend the curve to high field region, the ionization rate of electron would be smaller than hole which is not correct.

By applying the formula from the first method, we plotted the ionization rate of electron and hole in silicon respectively in our GOS structure under reverse bias as shown in Figure 12.

The multiplication factor M is defined as the output and input current density ratio of one kind of carriers (electrons or holes). This can be obtained by integrating the ionization rate over distance [62].

$$\mathrm{M} = \frac{J_{out}}{J_{in}}$$

Breakdown will occur When $\mathrm{M} \to \infty$ or when

$$\int_0^W \alpha \cdot \exp\left(-\int_0^x (\alpha_n - \alpha_p) dx'\right) dx = 1$$

For electrons:

$$M_n = \frac{1}{1 - \int_0^W \alpha_n \cdot \exp\left(-\int_0^x (\alpha_n - \alpha_p) dx'\right) dx}$$

For holes:

$$M_p = \frac{1}{1 - \int_0^W \alpha_p \cdot \exp\left(-\int_0^x (\alpha_p - \alpha_n) dx'\right) dx}$$

We calculated the multiplication factor of electron and hole shown in Table 7 by using the data we have in Figure 12. In general, the multiplication factor is a function of ionization rate and multiplication region where the field exists. Under different voltage bias, the multiplication factor is overall less than 1.2 in our case due to the narrow region for impact ionization, which corresponds to the inversion layer, thinner than 2 nm.

Table 5 Parameters for calculating the ionization rate of electron (α) and hole hole (β) in Si under room temperature [58] [60].

Parameters	Electrons	Holes
E_i	3.6 eV	5.0 eV
F_i	$1.954 \times 10^6\ eV/cm$	$3.091 \times 10^6\ eV/cm$
F_r	$1.069 \times 10^5\ eV/cm$	$1.110 \times 10^5\ eV/cm$
F_{kT}	$1.357 \times 10^4\ eV/cm$	$1.545 \times 10^4\ eV/cm$

Table 6 Parameters for calculating the ionization rate of electron (α) and hole hole (β) in Si under room temperature [60] [61].

Field strength (V/cm)	$\alpha_n(cm^{-1})$	$\alpha_p\ (cm^{-1})$
$E > 5.3 \times 10^5$	$5.0 \times 10^5 exp(-0.99 \times 10^6/E)$	$5.6 \times 10^5 exp(-1.32 \times 10^6/E)$
$2.4 \times 10^5 < E < 5.3 \times 10^5$	$6.2 \times 10^5 exp(-1.08 \times 10^6/E)$	$2.0 \times 10^5 exp(-1.97 \times 10^6/E)$
$E < 2.4 \times 10^5$	$2.6 \times 10^5 exp(-1.43 \times 10^6/E)$	$2.0 \times 10^5 exp(-1.97 \times 10^6/E)$

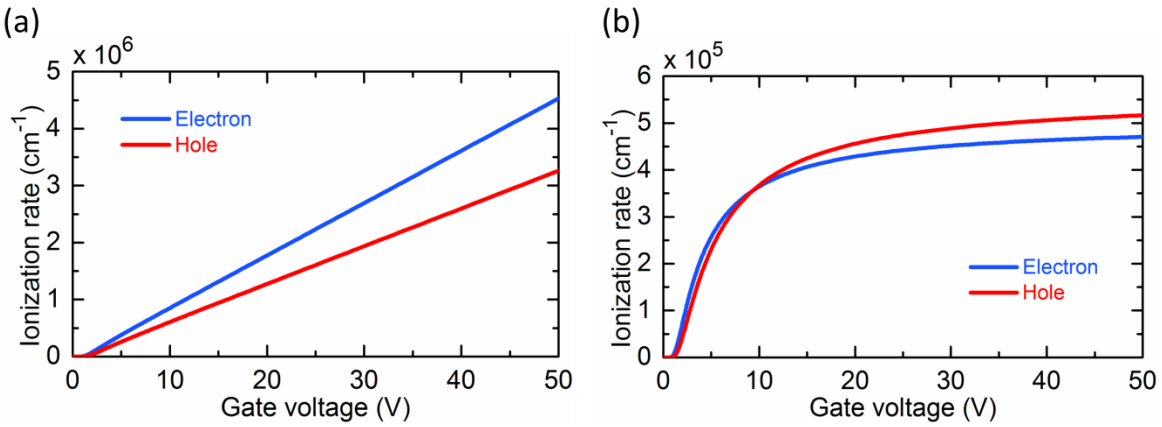

Figure 12 Ionization rate of electron and hole under different gate voltage in p-Si calculated using (a) Grant method [58] [60] and (b) Chynoweth method [60] [61].

Table 7 Multiplication factor of electron and hole under different gate voltage biases.

Substrate type	Voltage bias	Electron multiplication factor Mn	Hole multiplication factor Mp
p-Si	+10 V	1.0445	1.0306
	+30 V	1.0892	1.0637
	+50 V	1.1146	1.0823
n-Si	-10 V	1.0443	1.0305
	-30 V	1.0887	1.0634
	-50 V	1.1137	1.0817

3.3.2 Impact ionization under high field

At high field regime, the oxide field becomes predominant over the depletion field in Si. The impact ionization in SiO_2 should also be taken into account. Impaction ionization occurs initially in SiO_2. The generated electrons/holes drift towards Si or graphene sides. When electrons (or holes) enter the Si region, they suddenly become highly kinetic by gaining extra energy that corresponds to the conduction (or valence) band offset as shown in Figure 13(a) for electrons falling into Si side.

At high field (> 7MV/cm) regime, the high energy tails extending beyond the gap energy are known to develop rapidly with increasing field strength as shown in the Fig. 4 in Arnold's work [65]. The underlying transport physics can be understood by looking at the instantaneous kinetic energy of a typical sample electron. An electron spends most of its time at energies where the momentum relaxation is a strongly increasing function of energy. Once it climbs above the maximum in the acoustic rate it generally accelerates quickly until it loses most of its kinetic energy in an impact-ionization event and becomes part of its main portion of the distribution. Overall, then, much higher rates of impact-ionization are expected in this high-field regime than those estimated based on the model developed for the low-field-regime discussed in Section 3.3.1.

Arnold et al. think impact ionization of holes in the silicon is minor because of strong phonon coupling [65]. The multiplication of holes in SiO_2 is also negligible even at high fields of the order of 10 MV/cm.

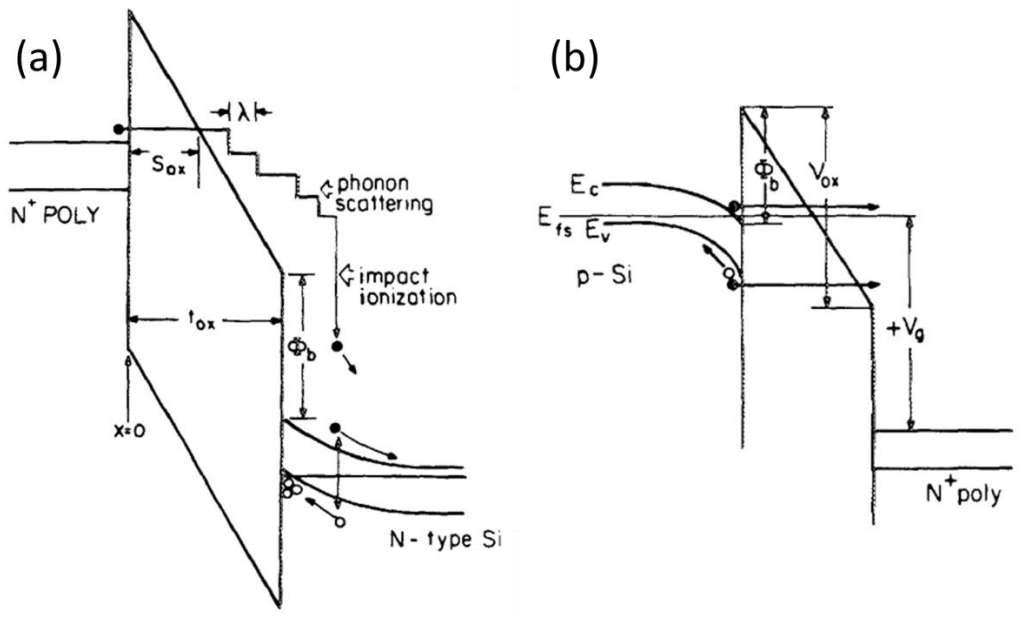

Figure 13 Electron transport of Fowler-Nordheim tunneling process in CMOS [63].

When electric field reaches a high field regime, the strong field in the oxide layer can trigger impact ionization. Electron multiplication factor (m) can be expressed as a function of oxide thickness (t_{ox}) and oxide field (E_{ox}) when t_{ox} is smaller than 30 nm:

$$m = 1 + P\left(\frac{E_{ox}}{F_{th}} - 1\right)$$

$$P = P_1 \frac{1}{t_{ox} - t_{d1}}$$

$$F_{th} = F_{th}^{\infty}\left(1 + \frac{t_1}{t_{ox} - t_{d2}}\right)$$

where $P_1 = 5.5\ nm$, $t_{d1} = 7\ nm$, $F_{th}^{\infty} = 3.8\ MV/cm$, $t_1 = 21.6\ nm$, $t_{d2} = 1.5\ nm$.

We plotted the multiplication factor versus oxide field in Figure 14 applying the formula above and extracted the number for our GOS structure. Table 8 shows the corresponding multiplication factor under various gate voltage biases. Electric breakdown field for 10 nm SiO_2 is reported to be 15~20 MV/cm [66] [67], corresponding to a multiplication factor of 1.2103 to 1.8915. From the calculation, we have an electron multiplication factor of 5.5 in SiO_2 under 50 V gate voltage bias.

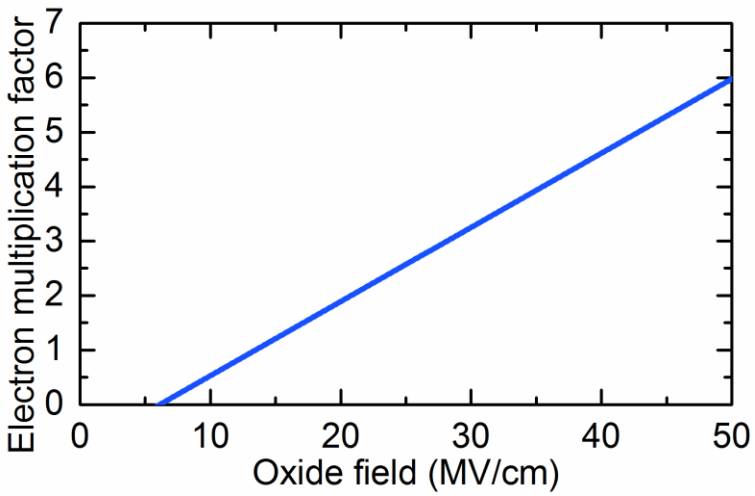

Figure 14 Oxide field versus electron multiplication factor in SiO_2 under high field.

Table 8 Multiplication factors of electron in SiO_2 of GOS device under gate voltage of 10 V, 30 V and 50 V, respectively.

Sample	Voltage	10 V	30 V	50 V
p-GOS	Oxide Field: E_{ox}	8.76 MV/cm	28.7 MV/cm	48.67 MV/cm
	Multiplication factor: m	0.3601	3.0768	5.7976
n-GOS	Oxide Field: E_{ox}	8.89 MV/cm	28.82 MV/cm	48.8 MV/cm
	Multiplication factor: m	0.3779	3.0932	5.8153

Quantum yield (γ) is the number of electron-hole pairs generated per incident electron, and is related to the multiplication factor (m): γ = m – 1. The quantum yield of impact ionization in a MOS structure was calculated as a function of incident electron energy into Si side [63] [64]. The amount of energy (E_e) that an electron can gain after Fowler-Nordheim (FN) tunneling through oxide is determined as

$$E_e = qE_{ox}\lambda\left(1 - e^{\frac{s_{ox}-t_{ox}}{\lambda}}\right) + q\phi_b$$

where E_{ox} denotes oxide field; λ is mean free path of electron in oxide; s_{ox} is the tunneling distance; t_{ox} is the oxide thickness; ϕ_b is the barrier height at the injection side. Mean free path is assumed to be ~ 4 nm. From the Figure 13, we know that tunneling distance (s_{ox}) can be calculated using energy barrier at the ionization side (ϕ_T).

$$s_{ox} = \frac{\phi_T}{V_{ox}} t_{ox}$$

We plotted the gate voltage (V_g) versus electron energy (E_e) for both p-Si and n-Si in our GOS structure as shown in Figure 15 and Table 9. Quantum yield γ(E) in silicon is plotted by Chang's group based on Alig's theory [63] [64].

$$\gamma(\mathrm{E}_e) = \sum_{n=0}^{\infty} n\, p_n(\mathrm{E}_e)$$

After two-level approximation, the probability that a particle of energy E_e ultimately creates exactly n pairs of electron-hole ($p_n(E)$) can be expressed as [64]

$$p_n(\mathrm{E}_e) = P_0(\mathrm{E}_e)\frac{\gamma_{n-1}(\mathrm{E}_e)}{\gamma(\mathrm{E}_e)} + [1 - P_0(\mathrm{E}_e)]p_n(\mathrm{E}_e - \hbar\omega)$$

which is related to the probability that the primary electron will ionize first before producing phonons ($P_0(\mathrm{E}_e)$), the three-product particles will cause (n-1) times ionization ($\gamma_{n-1}(\mathrm{E}_e)/\gamma(\mathrm{E}_e)$) and the electron after producing a phonon will cause n times ionization ($p_n(\mathrm{E}_e - \hbar\omega)$).

As both authors mentioned, it becomes linear in E when E is large. For Si, quantum yield demonstrates a slope of ~3.7 eV per pair generation when E is larger than 6 eV. We extended the curve in [63] accordingly by slope of 3.7 as shown in Figure 16.

At 50V bias the energy of electrons exiting the 10-nm oxide reaches 22 eV. These highly kinetic electrons, when impinging upon the Si side, produce a quantum yield of 5.5, corresponding to a multiplication factor of 6.5. It means 6.5 electron-hole pairs are generated during impact ionization process in Si with every one electrons injected.

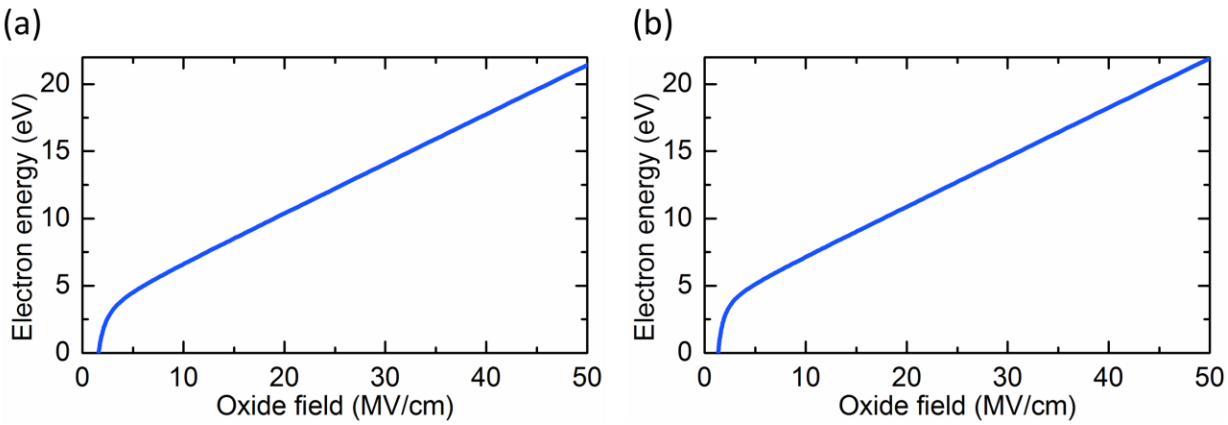

Figure 15 Oxide field versus electron energy gained after tunneling through 10 nm oxide in (a) p-Si and (b) n-Si.

Table 9 Electron energy gained by tunneling through 10-nm SiO_2 in p-GOS and n-GOS at 50 V gate voltage.

Substrate	E_{ox}	ϕ_b	ϕ_T	s_{ox}	E_e
p-GOS	48.67 MV/cm	3.15 V	3.66 V	0.752 nm	21 eV
n-GOS	48.8 MV/cm	3.66 V	3.15 V	0.645 nm	21.5 eV

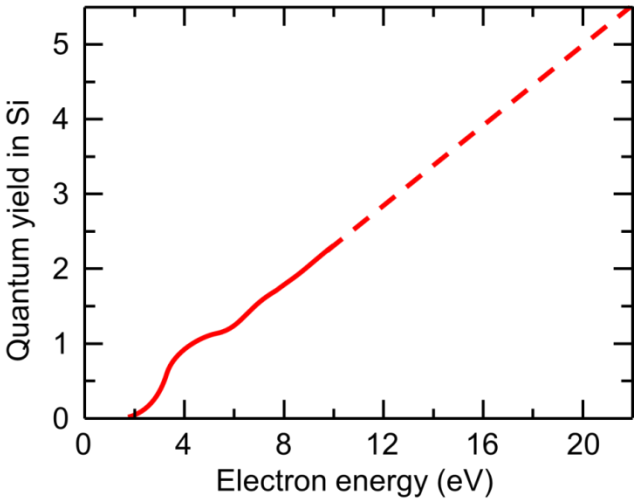

Figure 16 Electron energy versus quantum yield in Si extended into high energy region [63].

3.4 LATERAL BREAKDOWN PROPAGATION

Propagating breakdown in a MOS structure was first been discussed by Klein in 1966 [68]. The lateral propagation of oxide breakdown is only found under high voltage bias. Triggered by a single hole breakdown, the breakdown process can propagate via arc, gas and within silicon. Two types of breakdown damages were found. One is large conglomerations of disconnected single breakdown pits, the other one is connected, meandering destruction (Figure 17(a)).

For oxide propagation by arc between metal and breakdown spot in silicon, the metal is largely destroyed. When the defect density is high in oxide, oxide breakdown tends to spread via adjacent site than arc. After initial breakdown occurs in a random weak spot in oxide, it leaves a hole with a rim of high temperature. The dielectric strength of the oxide decreases as the temperature increase. Therefore, the next breakdown event will tend to occur at adjacent spot. While for oxide breakdown propagating via gas (air), extreme high voltage is required to breakdown air.

Lombardo's group discussed about this phenomenon later in 1999 [69] [70]. Extensive analysis is reported regarding the lateral propagation speed. By applying voltage pulse with 10 to 100 ns pulse width on CMOS device with thin oxide, they observed similar meandering lateral propagation line through TEM (Figure 17(b)). From the transient time and line length, they estimated the lateral propagation speed to be 2×10^6 cm/s for 35 nm oxide and 2×10^5 cm/s for 9.3 nm oxide. It rules out the possibility that atom motions such as cracks being responsible for these damages, which propagate at a rate less or equal to the sound speed in silicon (1×10^6 cm/s). It also rules out the possibility of heat diffusion which would propagate at speed of 10^3 cm/s.

The breakdown process is initiated by oxide degradation and defect generation. Percolation paths that become breakdown spot eventually are believed to form between anode and cathode after the defect density in oxide grows above threshold. The initial breakdown spot then becomes a sink of electrons with large leakage current flow through as shown in Figure 18. It is possible that the electrons of cathode gathering and breakdown an adjacent spot on their way migrating towards the initial breakdown spot.

Due to the large current flow through the breakdown spot, there is a cylindrical modification of oxide around the spot that will decay by distance Δr from the spot with a function of $\sqrt{D\Delta t}$ where D is the electron diffusivity and Δt is the time interval. A percolation path will form within the effective modification region and become the next breakdown spot. The effective modification region is related to the defect density N_{Defect} as well, that $\Delta r = \sqrt{1/N_{Defect}}$. The speed of propagation v can be derived that

$$v = \frac{\Delta r}{\Delta t} = D\sqrt{N_{Defect}}$$

As the next breakdown becomes the new sink of electrons, this process repeats and creates the lateral propagation of oxide. Lombardo called it a self-avoiding random walk that the already breakdown spot cannot breakdown again.

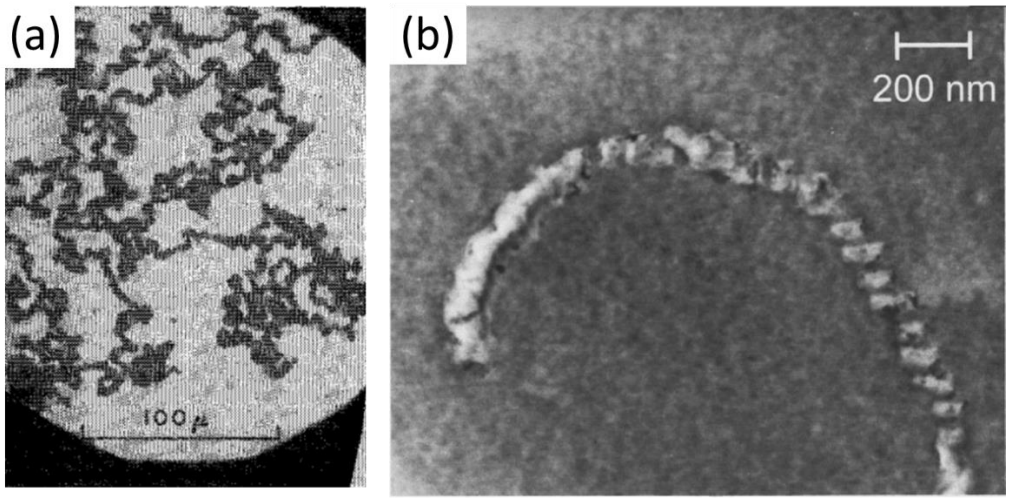

Figure 17 (a) Photo image of lateral propagation of oxide breakdown in p-Si with positive gate voltage observed by Klein [68]. (b) Plan-view bright field TEM image of lateral propagation of oxide breakdown in Si with 5.6 nm oxide [70].

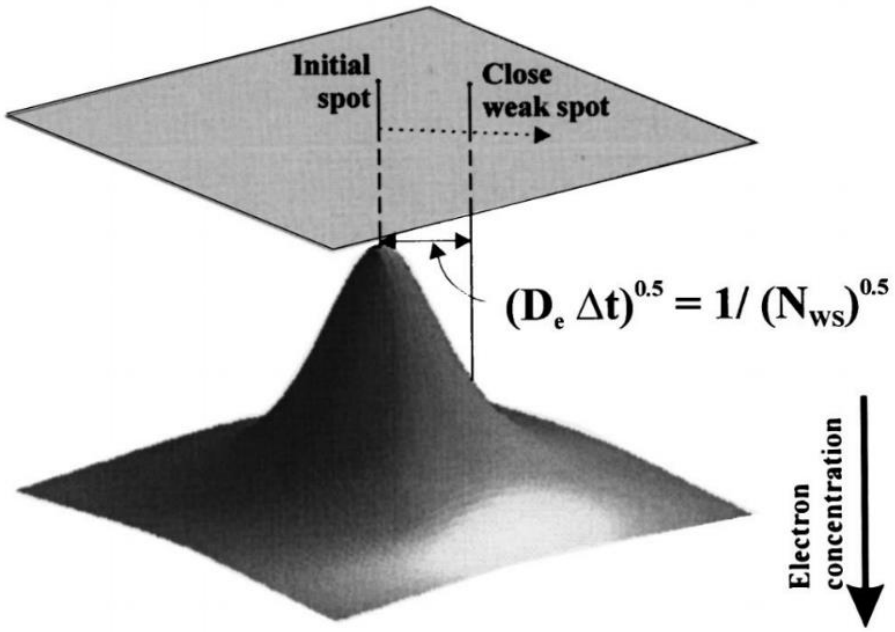

Figure 18 Mechanism of breakdown propagation proposed by Lombardo [70].

3.5 LIGHT EMISSION IN SILICON DEVICE

Light emission on silicon devices has been noticed and reported since 1950s. With the development of vision technology, light emission microscope became a common tool for failure analysis in semiconductor devices [71] [72] [73].

The light emission in silicon device can be generated by four types of current: forward and reverse current of PN junction [76], reverse current of saturated MOS transistors, tunneling currents in gate oxide [77] and current that cause Joule heating.

For the light emission from silicon, Bude classify the radiative transition into two groups: radiative recombination involving both electrons and holes as shown in Figure 19 (a and b) for intra-band transition, and radiative recombination involving only elections or holes as shown in Figure 19 (c and d) for inter-band transition [71]. All the transition satisfies energy conservation law, which means the emitting photon energy is equal to the carrier energy loss. Besides that, indirect transitions also require the momentum conservation which involves the interaction between electrons and phonons or ionized impurities through their Coulomb field.

Light emission from PN junction under reverse bias was first observed [78] [79] earlier than forward bias [80]. The light emission spectra in PN junction under forward and reverse bias is shown in Figure 20 [75]. Under forward bias, most emission light comes from inter-band transition which generates photon energy equal or larger than band gap. For the reverse bias, on the contrary, spectra peak at energy lower than band gap, indicating intra-band transitions associated with hot carriers. With the support of theoretical calculation, Bude confirmed that

light emission under forward bias is mainly caused by indirect inter-band transition. For reverse bias, direct intra-band transitions are the primary process in low field and indirect intra-band transitions are the primary process in high field.

For the light emission in oxide, the electro-luminescence is observed in thick oxide (> 50 nm) [81] [82] and ultra-thin oxide (< 4 nm) [74]. Chiang assumed that the electro-luminescence is generated at the output of the dielectric and its coming from the relaxation of the highly kinetic electrons through recombination [77].

For all the case mention above, the light emission spectra have a broad band width. The Joule heating corresponds to a broad base of black body radiation in the light emission spectra. In our AES study that we discuss in this dissertation, the light emission spectra collected from GOS device under high voltage pulses are mostly atomic spectra with nanometer line width which is different from all the cases above.

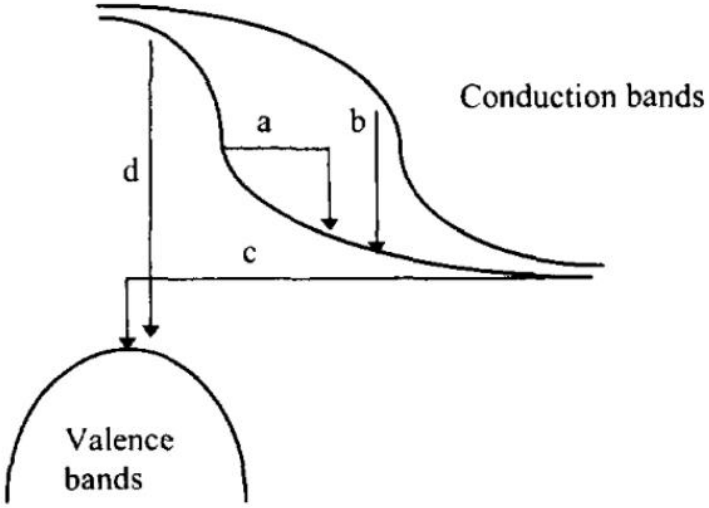

Figure 19 Distinction of various luminescence mechanisms in a realistic band structure [71] [72]. (a) Indirect c-c, (b) direct c-c, (c) indirect c-v, (d) direct c-v.

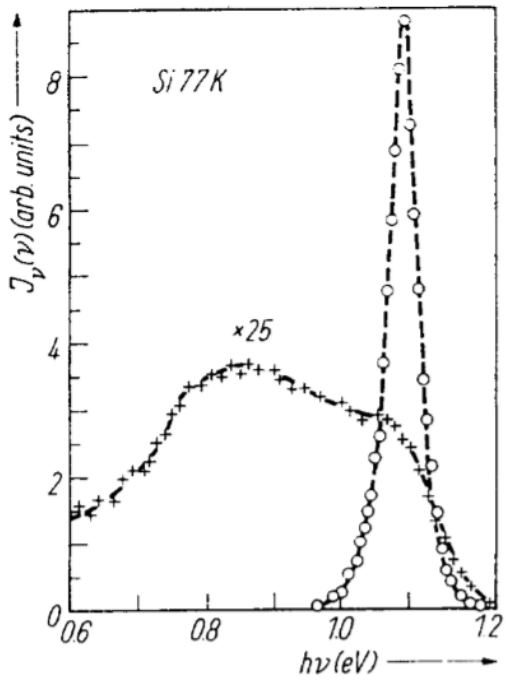

Figure 20 Emission spectrums of Si under reverse bias (+) and forward bias (o) [75].

4.0 ELECTRICALLY-TRIGGERED AES ON GOS SUBSTRATE

4.1 INTRODUCTION

As mentioned in Chapter 1.1, atomic emission spectroscopy (AES) triggered by various excitation sources provide useful information for qualitative and quantitative analysis. The flame triggered AES requires a liquid sample and inert gas ambient. The electrical triggered AES requires high voltage or current. The plasma induced AES has a complex system set-up for plasma excitation. Here we propose chip-scale AES with a simple system set-up, low voltage operation and working in air ambient and room temperature.

Similar to the case of metal/oxide/semiconductor (MOS) structure in silicon electronics, a graphene/oxide/ semiconductor (GOS) structure forms a basic building block that offers a rich device potential for electronic or optoelectronic applications [83][84][85]. We demonstrate a GOS-based device technology that promises chip-scale AES system. Analytes are placed on top of a graphene/SiO2/Si (GOS) substrate and are atomized for atomic luminescence under electrical excitation. Here the graphene layer serves as an electron-transparent conducting electrode.

4.1.1 Fabrication and system set-up

The system setup for our atomic emission spectroscopy technique is shown in Figure 21. Electrical source are manually triggered voltage pulses supplied by a pulse generator (HP 214B). Pulse width, amplitude and polarity are varied and specified as control parameters in this study. The graphene/oxide/silicon (GOS) based sample is connected with the source via a probe station. Bottom electrode is 100-nm-aluminum layer with Ohmic contact, while the top electrode connection is achieved by pressure contact with a tungsten probe.

The atomic emission spectrum is collected through a multimode optical fiber with 1 mm core diameter. There is a 2 mm gap between the sample and optical fiber head. The light collected is analyzed through Edmund (BWTek) CCD-based optical spectrum analyzer with 1.7 nm spectral resolution and broad detection wavelength range from 350 nm to 1050 nm. Optical image is taken through microscope observe from above by NIKON E995 digital camera with long exposure time such that all explosions occurring during multiple pulses are captured.

The fabrication of GOS structure with 10 nm oxide is explained in Section 2.2. Analytes are placed on top of GOS substrate through either thermal evaporation deposition (bulk layer) or spin coating (nano-particles). Mono-layer or 8-layer graphene is used and compared in GOS substrate.

CdSe/ZnS core/shell quantum dot solution in toluene as purchased is spread uniformly on GOS substrate through spin coating. Spin rate of 2500 rpm and spin time of 30 seconds is applied. As shown in the SEM image of Figure 22, quantum dots (~6 nm lateral diameter) are densely packed on top of graphene with density of $\sim 10^{12}$ cm^{-2}.

49-90 nm Ag nano-particles (NP) colloidal water-based solution is spread through drop coating instead of spin coating because of the hydrophobic nature of graphene. According to the

product information, surface treatment and dispersion is applied to prevent aggregation and clustering of the nano-particles. After drop coating, sample is kept in room temperature till water evaporate. Ag NPs as well as sodium components from original solution remain on the substrate. 2 μL volume of NP solution droplet on graphene will leave an Ag NP-coated area with around 1 mm diameter. The nano-particles are expected to have low density in the bulk area while much higher density in the region where transfer graphene are wrinkled. As shown in Figure 23, Ag NPs with ~50 nm diameter are mostly trapped within the dark area, which is folded or wrinkled graphene area. As a comparison to the Ag NP sample, 15 nm-thick silver dot arrays with 0.73 mm diameter and 1.5 mm dot-to-dot distance are deposited through thermal evaporation deposition with shadow mask. A 2-μL volume of NP solution droplet placed on graphene will leave an Ag NP-coated area with around 1-mm diameter and 10^5 cm^{-2} particle density on average.

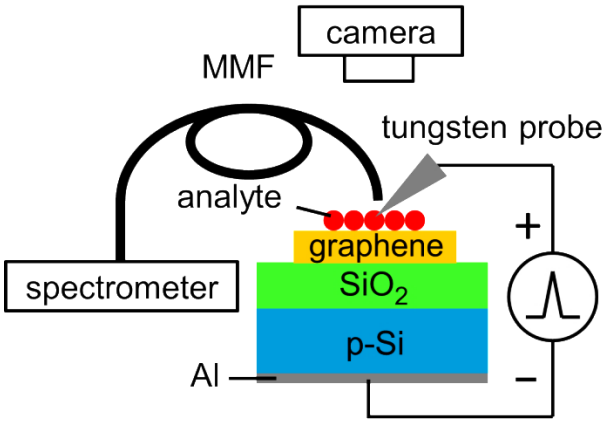

Figure 21 Scheme of system set-up for emission detection for analytes on GOS substrate.

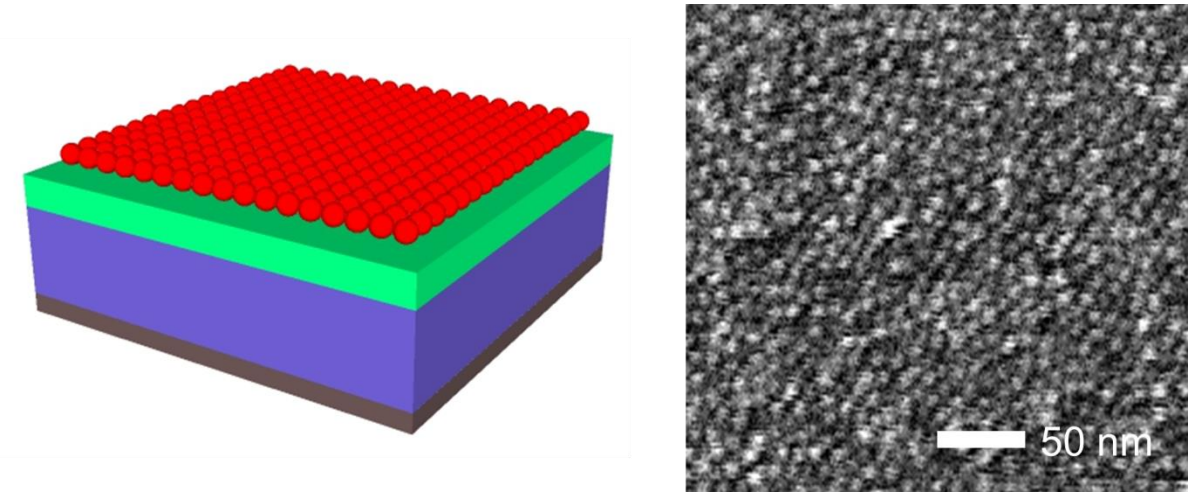

Figure 22 SEM image for CdSe quantum dot (QD) spin-coated on graphene. CdSe QD have lateral dimension of ~6 nm diameter.

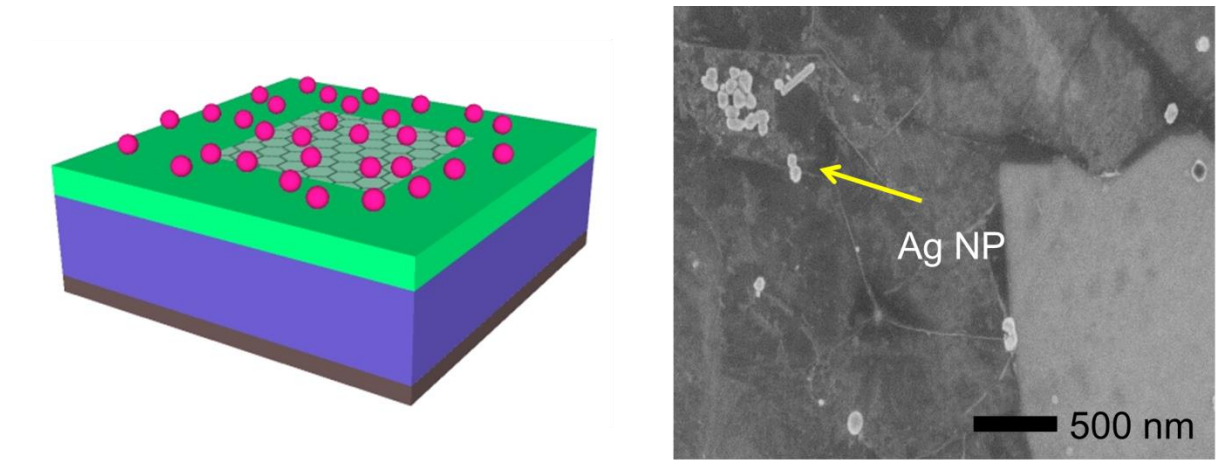

Figure 23 SEM image for Ag nano-particles (NP) drop-coated on graphene. Ag NP of ~50 nm diameter is trapped in folded or wrinkled graphene area.

The principle of oxide breakdown is discussed in detail in section 3.0. Under high field, carrier transport through the oxide layer through Fowler-Nordheim tunneling process. New electron-hole pairs are generated through impact ionization process, generating large current flow. Joule heat created by large current flow can cause melt explosion. The injection of large amount of electrons within short time interval can also charge the oxide beyond the Rayleigh limit that Coulomb explosion occurs and atomize the elements nearby as well. Photo images of the strong explosion in the following sections show visible spikes which are caused by explosion. In the meanwhile, the material will be heated by the electron collision that melting occurs simultaneously.

Graphene serves as a top electrode with good conductivity and transparency. Carbon lines that might be generated from graphene do not have any major presence in most of the visible to NIR range. This non-interfering aspect of graphene is expected to benefit resolving AES spectra. Analyte either deposited as bulk material or placed as discrete particles can be analyzed on GOS substrate.

Atomic luminescence is observed and measured during the explosion process. The atomic spectra show major difference depending on the injection direction of kinetic electrons controlled by bias polarity. When the electrons are injected upward from silicon to graphene, atomic lines from metal elements are strongly observed. However, silicon and oxide elements are dominant when the electrons are injected downward into silicon.

Atomic explosion occurs synchronized to the rising edge of the pulse until the electrode loses conductivity because of explosion. 30 or more pulses can be applied depending on the quality of the electrode. The explosions observed in this work are considered to be triggered

mostly by electrical breakdown. The damage is localized and the rest of the electrode cover area remains intact. As shown in Figure 24, 11 tests were done on 8 mm^2 area.

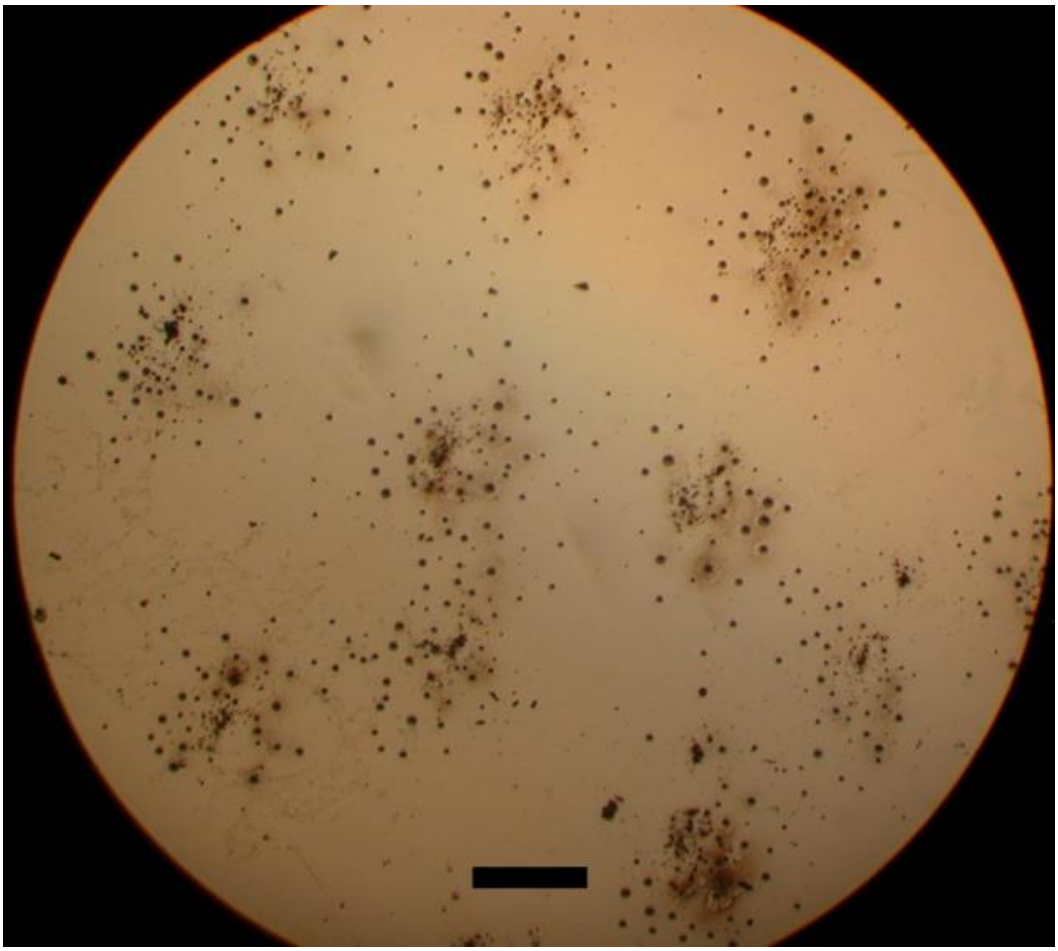

Figure 24 Localized damages of AES test on monolayer graphene/ SiO_2/ n-Si. Scale bar: 0.2 mm. 11 tests are shown in this image.

4.1.2 Atomic emission under pulse voltage drive

In our atomic emission spectroscopy, pulses with voltage ranging from 30 V to 100 V are applied to the MOS or GOS structure via HP 214B pulse generator. Tungsten probe with tip diameter of 1 μm was used as top gate electrode for applying voltage bias. Sample was mounted on copper plate with thin gallium in between. Two terminal current-versus-voltage (I-V) characterizations were carried out with semiconductor parameter analyzer HP4145B as shown in Figure 25.

Bulk Ag, Ag nano-particles or CdSe quantum dots are placed on top of GOS substrate. For p-type silicon based structure, inversion biased pulses (top electrode positively biased) are applied. Pulses with 50 V amplitude and 10 μs pulse width are triggered manually with 1 second interval. Oxide breakdown occur and analyte placed on the GOS substrate are exploded, producing atomic luminescence. After 30 to 60 pulses, electrode (graphene in this case) will lose continuity due to the explosion.

As examples, Figure 26 shows the analysis for CdSe QD/ 8-layer graphene/ 10 nm thermal oxide/ p-Si structure. Figure 27 shows the current flow during AES of 8-layer graphene/10 nm thermal oxide/ silicon (GOS) structure. Details about AES will be discussed in chapter 3.

Figure 26 presents the I-V characteristics after AES. As mentioned before, since graphene is damaged due to atomic explosion, the current level drops to nA level right under the probe area in the linear-linear plot of Figure 26(d). However unexploded area nearby maintains good conductivity as shown in Figure 26(e). The log-log plot shows a slope of 1.5 in higher voltage range. The voltage-dependence of 1.5 follows the Child-Langmuir law of space-charge-limited current, implying that void nano-channels might be created in the oxide during AES test.

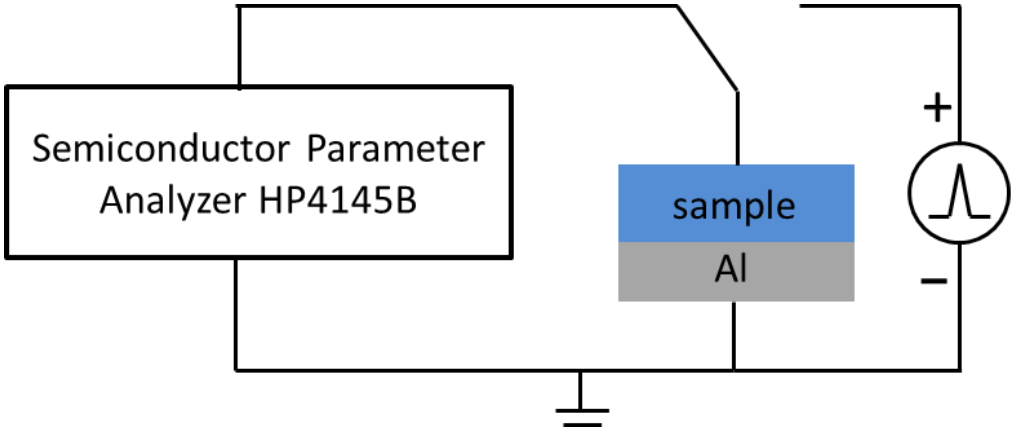

Figure 25 Two terminal I-V characterization system set up.

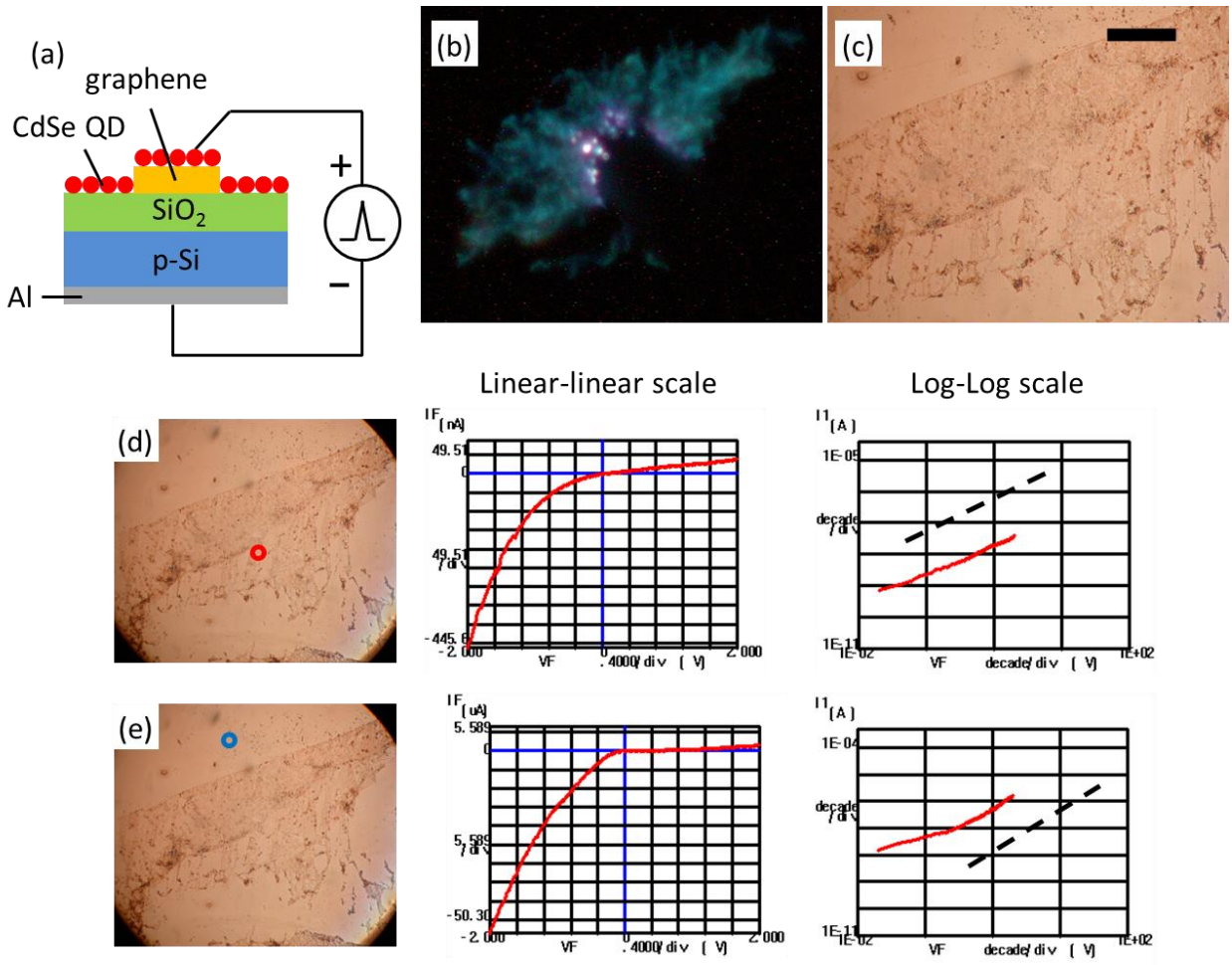

Figure 26 System set-up (a) and photo image (b) (c) of CdSe QD/ 8-layer graphene/ 10 nm thermal oxide/ p-Si with 50 V amplitude and 10 μs width pulses applied 10 times manually with 1 second interval. Scale bar shows 300 μm for photo image: (b) during test with tungsten probe on and (c) after emission.. I-V characteristic of sample after test for spot (d) right under probe area and spot (e) no emission area are plot in linear-linear scale and log-log scale. Dotted line shows slope of 1 in (d) and slope of 1.5 in (e).

We monitored the current flow through sample during emission by measuring the voltage drop across a small resistor of 0.1 Ohm connected in parallel to either p-GOS or n-GOS device under test. Figure 27 shows the circuit diagram of measurement taking into account the resistance and inductance of the cable. By comparing current waveform with and without emission observed in Figure 28, we conclude that the current injection level during emission is 5A or even larger with 50 V- 10 μs pulse applied. For both p-GOS and n-GOS, the emission process increases the current flow clearly at the middle part of the pulse. The spikes within the 10-μs pulse duration can be created by oxide breakdown and explosion occurring in different fresh spots. The ringing at the edges of the pulses is the intrinsic properties of RLC circuit.

By comparing the waveform with and without emission, we ascribe the spikes to the breakdown of fresh spots. The average width of a single spike is 0.2 μs and amplitude is 5 A, which means a total charge injection of 1 μC during a single spike. By normalizing using the graphene electrode area of 4x4 mm^2 conservatively, we can calculate the injection charge density of 0.06 C/m^2. The charge density limit is calculated to be 0.04 C/m^2 using the Rayleigh limit of the SiO_2 disk ($1.5x10^{-15}$ C in Table 2). The injected charge density (0.06 C/m^2) exceeds the Rayleigh limit (0.04 C/m^2), which makes Coulomb explosion another possible mechanism for atomic emission in our work.

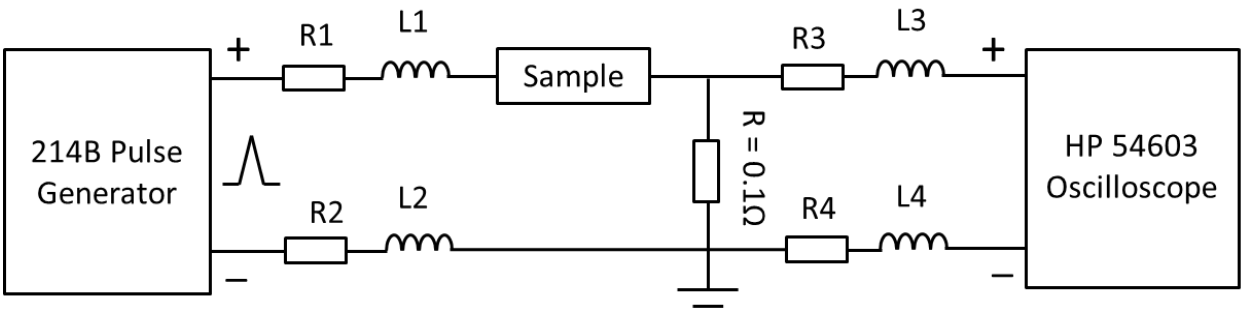

Figure 27 Circuit diagram of current flow through sample during atomic emission.

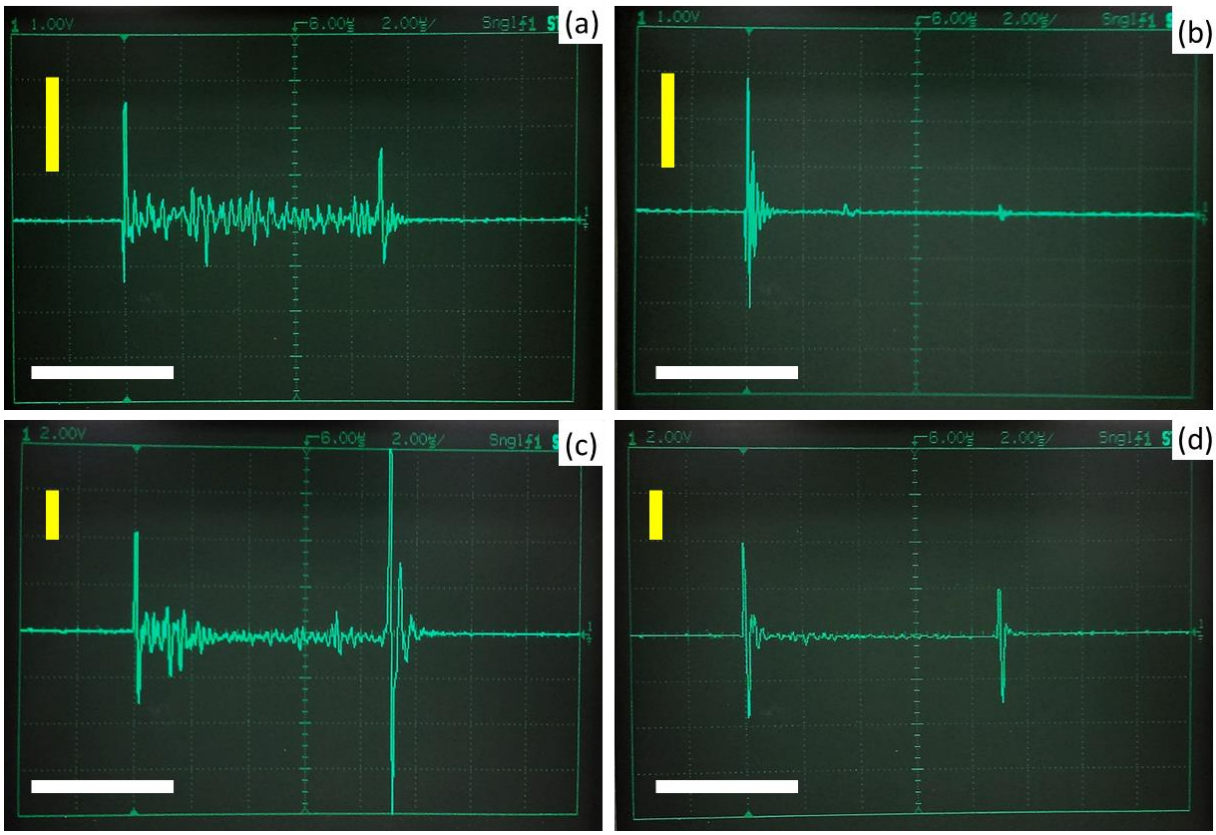

Figure 28 Oscilloscope screen photo of current waveform for 8LG/10-nm SiO_2 /p-Si (p-GOS) with (a) and without (b) emission observed and for 8LG/10-nm SiO_2 /n-Si (n-GOS) with (c) and without (d) emission observed under inversion biased pulses. Yellow vertical scale bar: 20 A. White horizontal scale bar: 5 μs.

4.2 ELECTRICALLY-TRIGGERED AES

We use our atomic emission spectroscopy (AES) for qualitative analysis of the following analyte samples: thin-film silver, silver nano-particles and CdSe quantum dots including reference AES on bare GOS substrate. Atomic lines from elements Si and O from silicon and silicon dioxide, element W from tungsten probe and element Na from background solution of Ag NPs are observed. Element Ag I (328 nm, 338 nm, 521 nm, 547 nm, 769 nm and 827 nm) and Cd I (361 nm, 468 nm, 480 nm and 509 nm) are identified out from the background lines, coming from the major transition shown in Figure 29.

For easy and strong atomic luminescence, positive pulses are applied to p-Si GOS samples and negative pulses are applied on n-Si GOS samples. More characteristics and details are explained in section 3.3.

Taking ionization energy (Table 10) into account, atomic line identification is done based on the sample structure, emission image and NIST Atomic Spectra Database [87]. Table 11 shows the detailed identification results.

Table 10 Ionization energy for atoms and ions [87].

Name	Ionization Energy	Name	Ionization Energy	Name	Ionization Energy
Ag I	7.58 eV	C I	11.26 eV	Na I	5.14 eV
Ag II	21.48 eV	C II	24.39 eV	Na II	47.29 eV
Ag III	34.83 eV	C III	47.89 eV	Na III	71.62 eV
O I	13.62 eV	Si I	8.15 eV	W I	7.86 eV
O II	35.12 eV	Si II	16.35 eV	W II	16.37 eV
O III	54.94 eV	Si III	33.49 eV	W III	26.0 eV

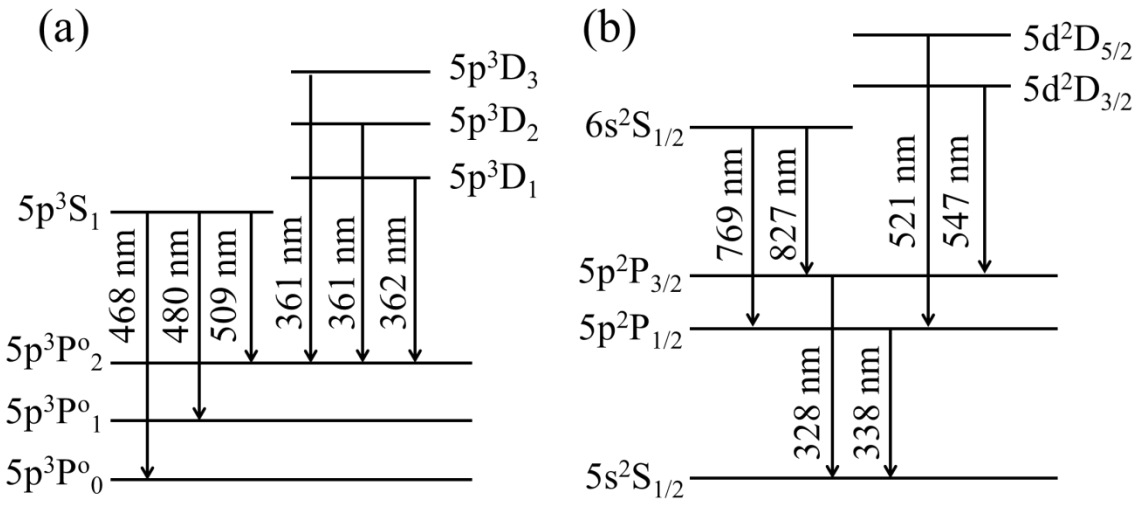

Figure 29 The energy level diagram of the Ag I (a) [86] and Cd I (b), showing radiative transitions and corresponding wavelengths.

Table 11 Atomic line identification results.

Wavelength	Name	Wavelength	Name
288 nm	Si I	501 nm	Si I
291 nm	Si II	506 nm	Si II
316 nm	W II	509 nm	Cd I
328 nm	Ag I	511 nm	Si III
336 nm	W I	521 nm	Ag I
338 nm	Ag I	527 nm	W I
358 nm	W I	547 nm	Ag I
361 nm	Cd I	560 nm	Si III
387 nm	Si II	572 nm	Si III
394 nm	O I/II	589 nm	Na I
397 nm	O II	590 nm	Si III
413 nm	Si II	617 nm	W I
418 nm	W II	635 nm	Si II
423 nm	O I	644 nm	O I
430 nm	W I	657 nm	O II
452 nm	W I	769 nm	Ag I
468 nm	Cd I	777 nm	O I
480 nm	Cd I	827 nm	Ag I
482 nm	Si III	844 nm	O I

4.2.1 AES on GOS substrate

As a reference, bare graphene/oxide/silicon (GOS) samples are tested under the same setup. Systematic comparisons were made between monolayer graphene and 8-layer graphene, n-GOS and p-GOS in order to understand the working principle.

As shown in Figure 30(a) and 30(c), positive pulse (top positive and bottom negative) with 50 V amplitude and 10 μs width are applied on monolayer or 8-layer graphene/ 10 nm thermal oxide/ p-Si. Electrons are injected upward, bombarding at the interface of graphene and oxide, showing purple atomic luminescence within radius of 4 mm Figure 30(b) and 30(d). Monolayer graphene (MLG) can sustain only 4 pulses of emission while 8-layer graphene can hold up to 14 pulses. It implies that explosion can occur damaging every time until it loses conductivity. Photo images were taken with long exposure time of 60 seconds. Therefore multiple explosions were captured by the camera and superposed into one image. Minor damage appears under the probe afterwards Figure 30(f). All the emission spectra shown in this article are normalized by the same factor for fare comparison. Si, O and W elements are identified in the atomic spectra. The purple light is mainly contributed by Si at 387 nm. Low intensity of the emission intensity leads to the high noise-to-signal ratio.

SEM images of the surface topography reveal widely spread emission area. Meandering trenches are distributed uniformly with around 100 nm diameter as shown in Figure 31(a). The edge of the trenches is covered with ~20 nm oxide and graphene layer is fractured into pieces as shown in Figure 31(b).

Negative pulse (top negative and bottom positive) with 50 V amplitude and 10 μs width are applied on monolayer or 8-layer graphene/ 10 nm thermal oxide/ n-Si as shown in Figure 32(a) and 30(c). Weak spots on oxide break down with large current flowing through. Electrons

are injected downward, bombarding at the interface of oxide and silicon. For n-GOS structure, there is no distinct difference between monolayer GOS and 8-layer GOS: both of them can sustain over 30 pulses with similar emission intensity. The majority of the graphene remains good conductivity for n-GOS because the damage on graphene is highly localized as shown in Figure 32(f). The spots with brightest luminescence in Figure 32(b) correspond to the black damage spots in Figure 32(f), indicating large current flow. SEM image gives a clear view of the surface condition after test in Figure 33. The damage location is huge and deep comparing to p-GOS case and graphene is destroyed completely within the damage area. Therefore the better endurance of 8-layer graphene no longer plays a role during multiple pulse testing. The same as Figure 30(g), Si, O and W elements are identified in Figure 32(g). Since the emission intensity is stronger due to larger current, more atomic lines appears with higher intensity level is captured within the same number of pulses. A broad base intensity of 2 is observed as well. The broad base is part of the black body radiation captured by CCD spectrometer. Comparing to the broad base intensity of 0.5 in p-GOS, n-GOS apparently reveals higher temperature.

Damages created by explosion have distinct shapes and distribution that correlates to the pulse polarity only. When top electrode is negatively biased, electrons inject through oxide into silicon. With good mobility in the graphene, electrons tend to attack and inject via intrinsic weak spot on oxide. Explosion and heat enlarge the weak spot (defect) leaving the damage locally deep into silicon as shown in Figure 33 with average diameter of 1 μm. However when the top electrode is positively biased, electrons coming from the minority carrier in p-Si try to inject upward through oxide to graphene. Due to the relative low carrier concentration and low mobility, the priority injection at defect spot is much less than the negatively biased case.

Therefore the explosion occurs uniformly across the surface, creating meandering shallow trenches.

Recalling the current waveform shown in Figure 34, the large spikes in the beginning of Figure 34(c) might be created by the large confined explosion in n-GOS and the relative small spikes in Figure 34(a) stands for the uniformly spread meadering trenches created in p-GOS.

As mentioned in Chapter 1.3, the maximum charge amount a cylinder could hold before Coulomb explosion can be calculated for a SiO_2 cylinder with length of 10 nm and radius of 100 nm, which is 1.4×10^{-16} C. For a current injection level of 5A of 0.4 μs, the injection charge density normalized by the graphene area (~10 mm^2) is 0.2 C/m^2. Therefore, the charge injection into the SiO_2 cylinder with radius of 100 nm is 6×10^{-15} C which is larger than the Rayleigh limit.

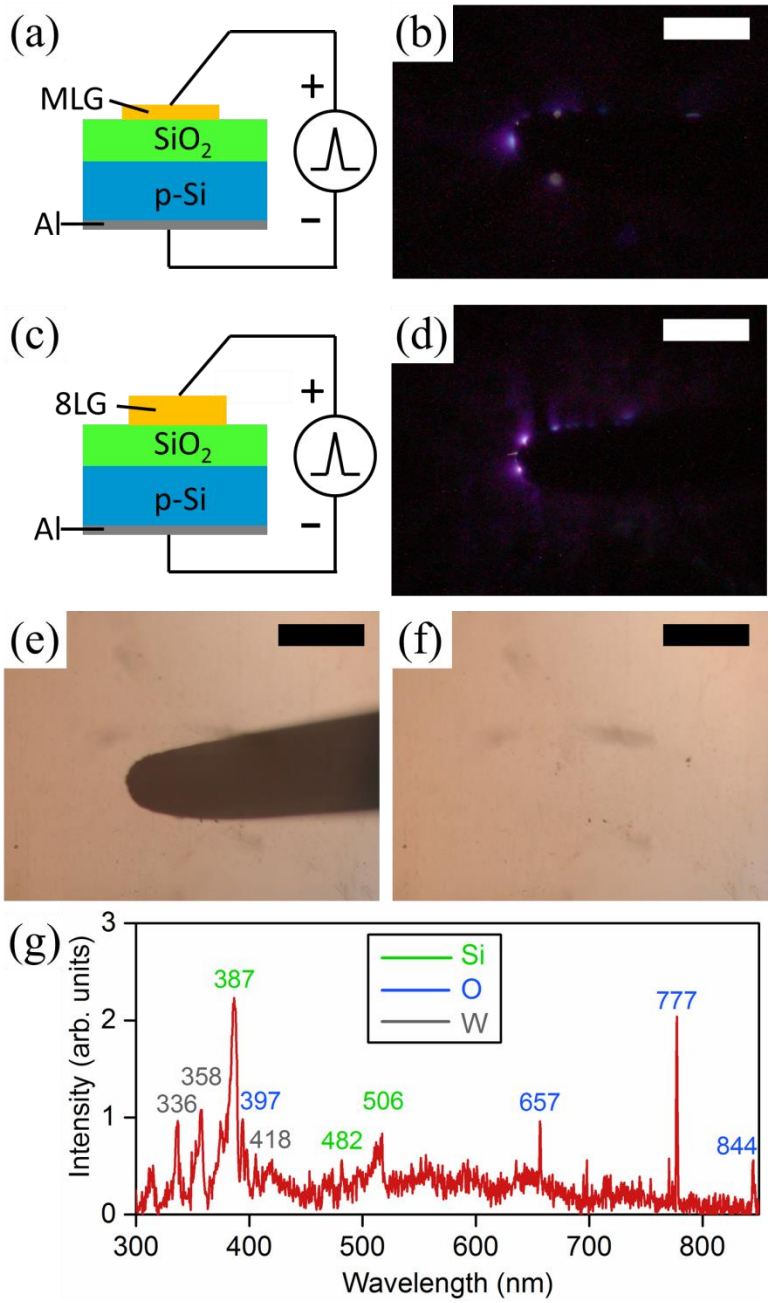

Figure 30 System set-up (a) and photo image during emission (b) of monolayer graphene (MLG) / 10 nm thermal oxide/ p-Si. System set-up (c), photo image during emission (d), after test (e) (f) and emission spectra (g) of 8-layer graphene (8LG) / 10 nm thermal oxide/ p-Si. 4 pulses for MLG and 14 pulses for 8LG with 50 V amplitude and 10 μs width are applied manually with 1 second interval. Scale bar: 400 μm.

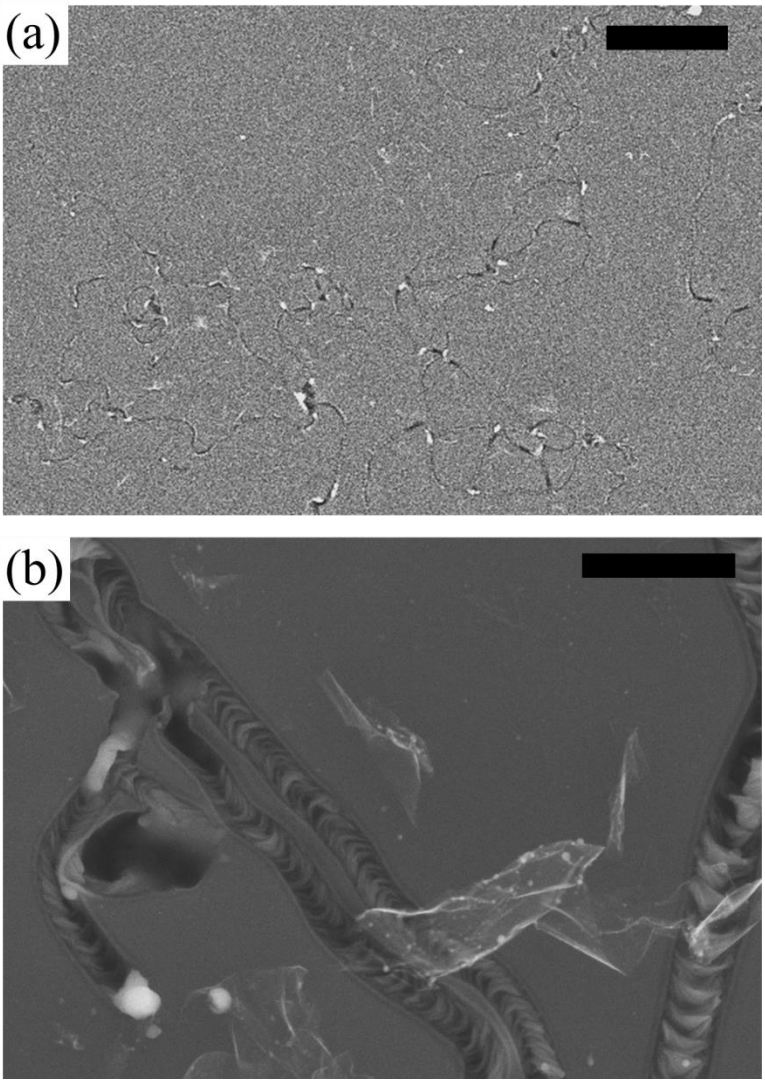

Figure 31 SEM image of 8-layer graphene (8LG) / 10 nm thermal oxide/ p-Si after emission test shown in Figure 30. (a) Scale bar: 5 μm. (b) Scale bar: 500 nm.

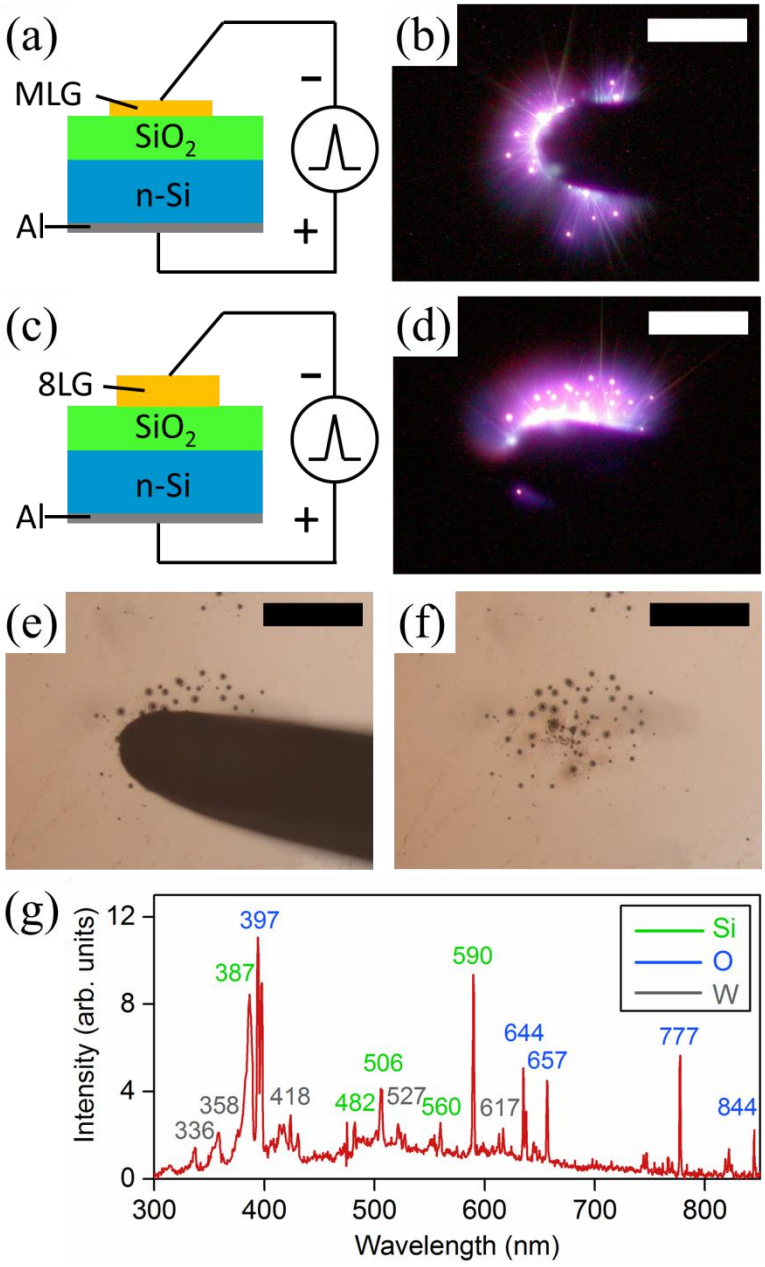

Figure 32 System set-up (a) and photo image during emission (b) of monolayer graphene (MLG) / 10 nm thermal oxide/ n-Si. System set-up (c), photo image during emission (d), after test (e) (f) and emission spectra (g) of 8-layer graphene (8LG) / 10 nm thermal oxide/ n-Si. 14 pulses with 50 V amplitude and 10 μs width are applied manually with 1 second interval. Scale bar: 300 μm.

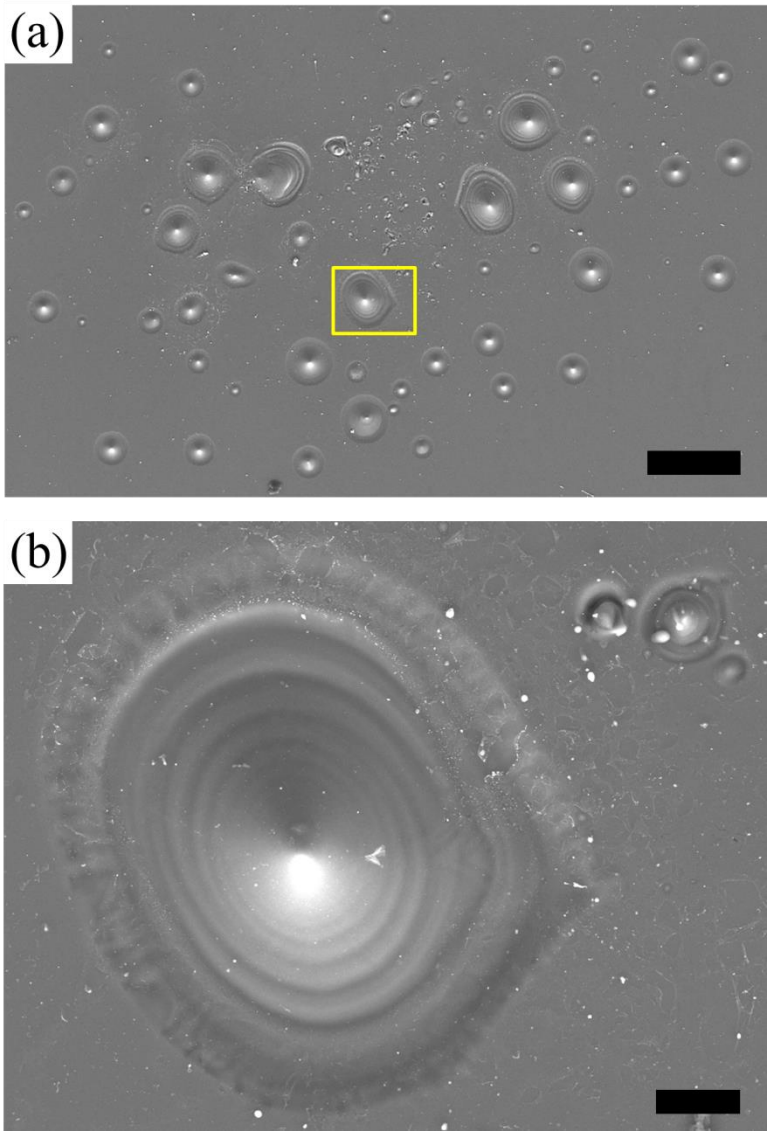

Figure 33 SEM images of 8-layer graphene (8LG) / 10 nm thermal oxide/ n-Si after emission test shown in Figure 32. (a) Scale bar: 50 μm. (b) Zoomed image of area within yellow frame in (a). Scale bar: 5 μm.

4.2.2 AES for bulk silver on GOS substrate

For comparison with silver nano-particles, Ag dot array with 0.73 mm diameter and 1.5 mm spacing is deposited on graphene/oxide/silicon (GOS) substrate and oxide/silicon substrate via thermal evaporation deposition.

As shown in Figure 34(a) and 34(d), positive pulse (top positive bottom negative) with 50 V amplitude and 10 μs width are triggered manually with 1 second interval if not specified. Electrons are injected upward, bombarding at the interface of graphene and oxide, exploding graphene, oxide and the analyte as well, showing atomic luminescence in Figure 34(c) and 34(e). Photo image was taken with exposure time of 60 seconds that multiple explosions were captured by the camera and superposed into one image. With probe directly contacting 15 nm Ag dot, potential spread on Ag uniformly and current primarily flows right under the probe, where the analyte gets exploded. In Figure 34(b), the green luminescence corresponds to wavelength of 547 nm from Ag distinctively. With an extra 8-layer graphene added on top of the original Ag-dot/GOS structure, the top electrode becomes 16-layer graphene with better conductivity. Tungsten probe touches the graphene directly and the potential spread widely which is no longer confined in the Ag dot area [88]. Therefore we are able to observe the atomic explosion of GOS area uncovered by Ag as well as shown in Figure 34(e) and 34(f). The current density reaches maximum right under the probe. Therefore more elements are exploded with higher emission intensity.

SEM images shown in Figure 35(d) and 35(e) of the surface condition after test reveal similar trenches with 200 nm diameter on GOS reference samples in Figure 31. Area with and without Ag covering are exploded with similar mechanism.

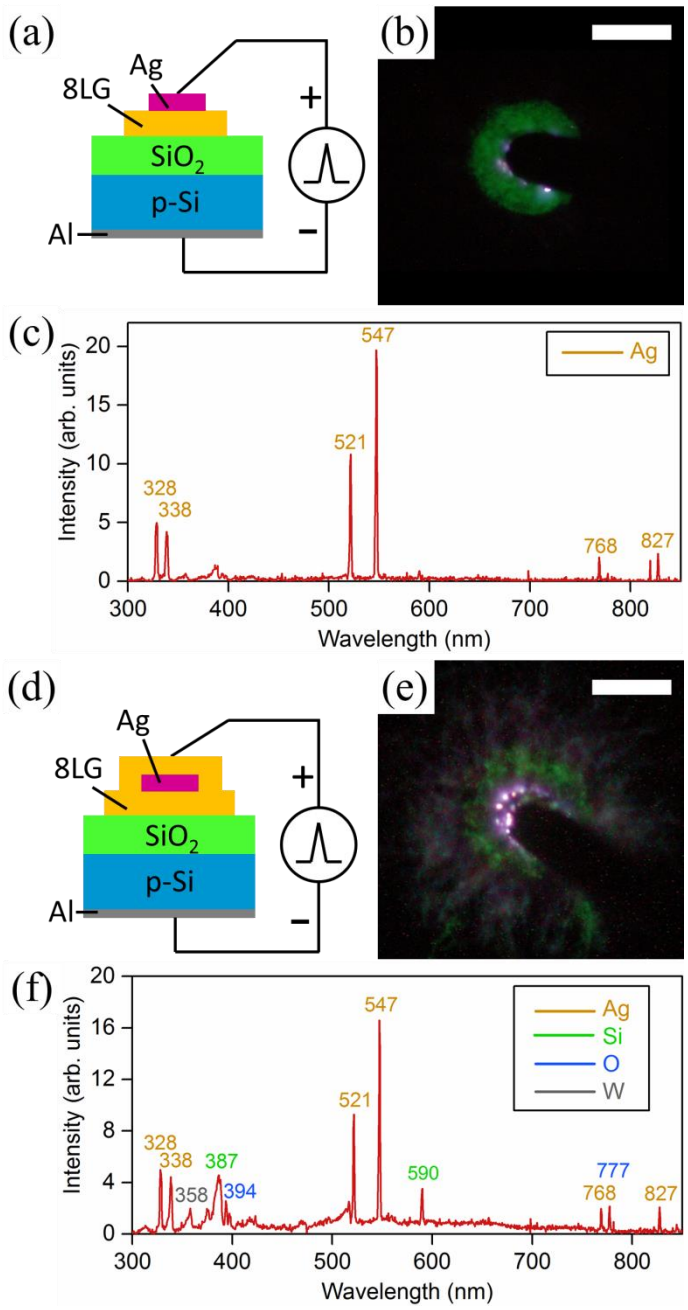

Figure 34 System set-up (a), emission photo image (b) and spectrum (c) of 15 nm Ag/ 8-layer graphene/ 10 nm thermal oxide/ p-Si with 50 V amplitude and 10 μs width pulses applied 20 times in total. A sample with extra 8-layer graphene added on top under same test condition is shown in (d) (e) (f). Scale bar: 200 μm.

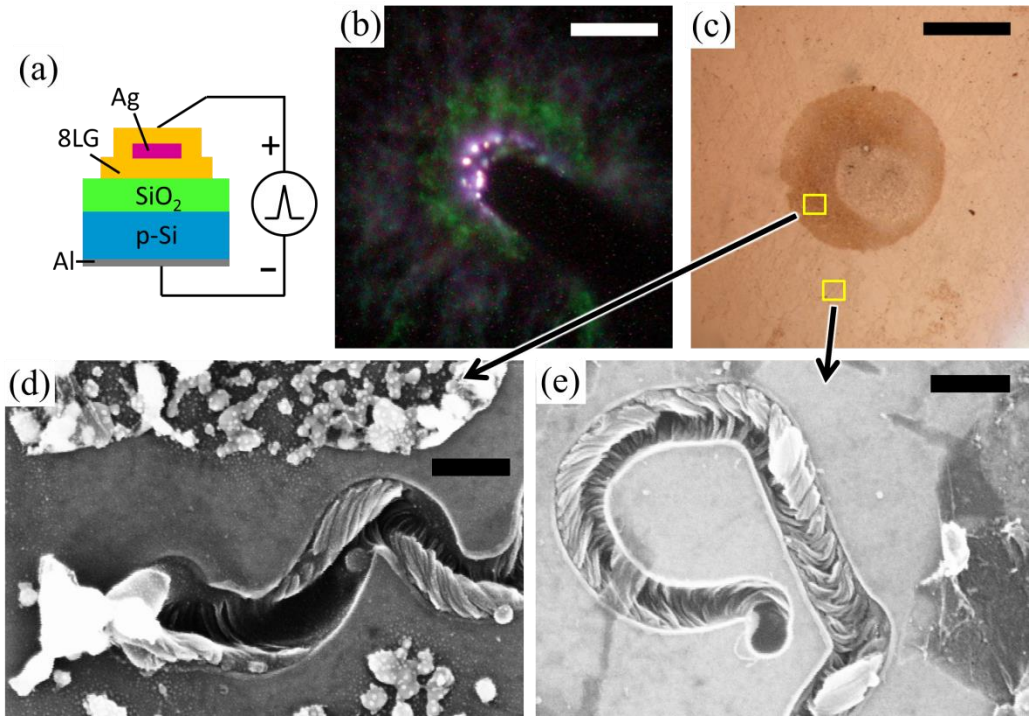

Figure 35 System set-up, photo image and SEM image after test of 15 nm Ag sandwiched by 8-layer graphene/ 10 nm thermal oxide/ p-Si under positive pulse (a) with 50 V amplitude and 10 μs width applied 20 times in total. Photo images during emission with tungsten probe on (b) and after emission (c). SEM images after test (d) (e) (f). Scale bar shows 500 μm in (b) (c), 200 nm in (d) (e).

If we reverse the pulse polarity, it's hard to trigger atomic emission under same voltage. Higher voltage (90 V) pulse is applied for negative pulse on Ag dot/p-GOS structure as shown in Figure 36(a). Combing with the photo image during emission (Figure 36(b)) and after emission (Figure 36(c)), we found that the current flow is extremely confined near the contact area between probe and sample. Therefore both the atomic luminescence and major damage area is small.

In the SEM image shown in Figure 36(e), the damage under the probe is circular and goes deep into silicon which is similar to the n-GOS in Figure 33. However, a combination of meandering trenches and circular damage spots are found at the boundary of the Ag dot shown in Figure 36(f). At the same time, there is a ring area between Figure 36(e) and Figure 36(f) which looks intact under SEM in Figure 36(d).

To understand the formation of meandering trenches, we compare the damage left after 20 pulses and 10 pulses of 15 nm Ag dot/10 nm oxide/p-Si with the same 50 V-10 μs pulse condition applied. In Figure 37, the 15 nm Ag layer become discontinuous due to heating of 20 pulses. Meandering trenches interconnect with each other (Figure 37(d)) and some of them join together and go much deeper as shown in the right corner of Figure 37(e). If we reduce the pulse number to 10, we can see the beginning of trench formation in Figure 38. The trenches start to form discretely before they connect with other trenches as shown in Figure 38(c). The trenches might be created by joule heating caused by large current flow.

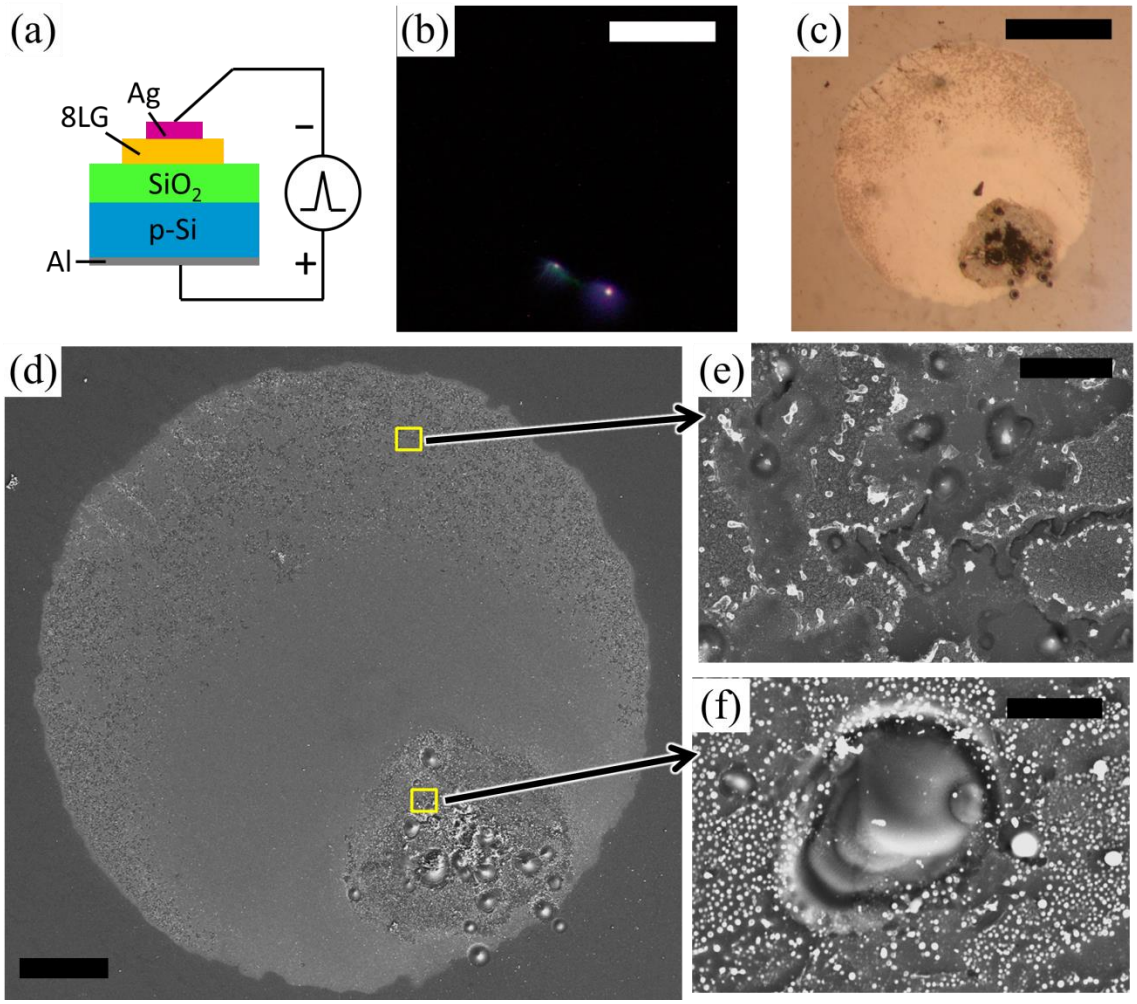

Figure 36 System set-up, photo image and SEM image after test of 15 nm Ag/ 8-layer graphene/ 10 nm thermal oxide/ p-Si under negative pulse (a) with 0.1 s period, 90 V amplitude and 10 μs width is applied by the pulse generator for 30 seconds (300 pulses in total). Photo image scale bar shows 300 μm: (b) during emission with tungsten probe on; (c) after emission. SEM image after test (d) and zoomed details (e) (f): Scale bar shows 100 μm in (c), 2 μm in (e) and 4 μm in (f).

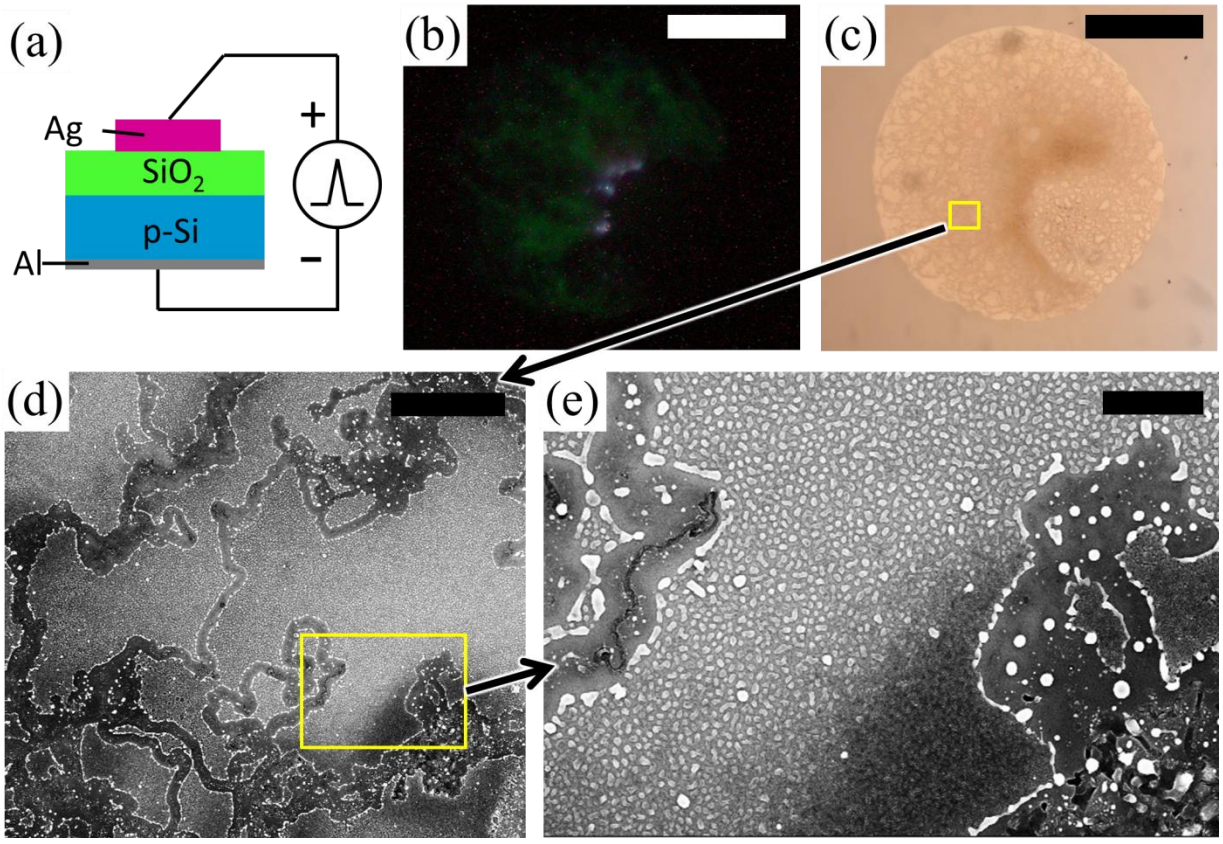

Figure 37 System set-up, photo image and SEM image after test of 15 nm Ag/ 10 nm thermal oxide/ p-Si under positive pulse (a) with 50 V amplitude and 10 μs width applied 20 times in total. Photo images during emission with tungsten probe on (b) and after emission (c). SEM images after test (d) (e). Scale bar shows 300 μm in (b) (c), 10 μm in (d) and 2 μm in (e).

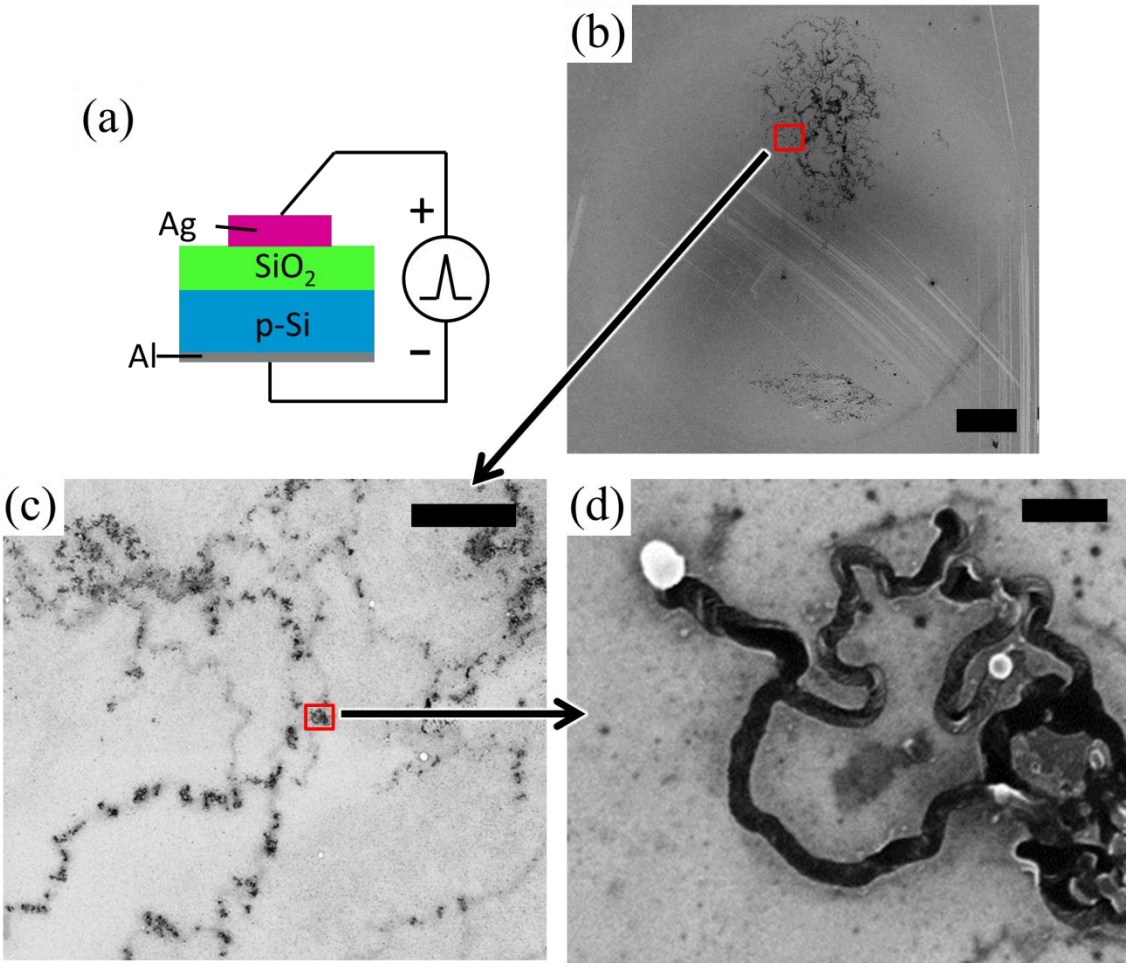

Figure 38 System set-up, photo image and SEM image after test of 15 nm Ag/ 10 nm thermal oxide/ p-Si under positive pulse (a) with 50 V amplitude and 10 µs width applied 10 times in total. Photo images during emission with tungsten probe on (b) and after emission (c). SEM images after test and Ag removal (d) (e) (f). Scale bar shows 100 µm in (b), 10 µm in (c) and 300 nm in (d).

4.2.3 AES for Ag nano-particles on GOS substrate

Ag nano-particles with 49 nm to 90 nm diameter are drop coated on GOS substrate. In the SEM image shown in Figure 22 (b), Ag nano-particles are far separated on the GOS substrate. As the density drops, the emission intensity drops. Besides, the original colloidal solution contains large amounts of Na which leaves on the substrate as well. Therefore the atomic luminescence of our Ag NP is not as green as bulk Ag visually. However the spectrometer is sensitive enough to identify the Ag. As-transferred graphene layer has wrinkles and overlaps as shown in the Figure 22 (b). The emission area seems confined by the wrinkles and the overlapping area has highest emission intensity in Figure 39. Ag, Si, O, Na and W elements are identified in the atomic spectra. The orange luminescence comes from Na at 589 nm.

Experimentally we find that it is easier for AES when positive pulses are applied on p-Si based substrate and negative pulses are applied on n-Si based substrate. Easier means lower pulse voltage, shorter pulse width and lower pulse frequency. Overall the AES difficulty is positive pulse on p-Si < negative pulse on n-Si < negative pulse on p-Si < positive pulse on n-Si.

Figure 40 gives a comparison between Ag NP/ p-GOS and Ag NP/ n-GOS under negative pulse. The emission spectra and photo image are similar for the different sample under pulses with same polarity. Since p-GOS is hard to explode, higher voltage is needed to trigger the emission. Therefore the current is larger and more confined in p-GOS than n-GOS. With a larger area of atomic emission, the spectrum of Ag NP/ n-GOS has weak Ag peaks identified at 328 nm and 338 nm.

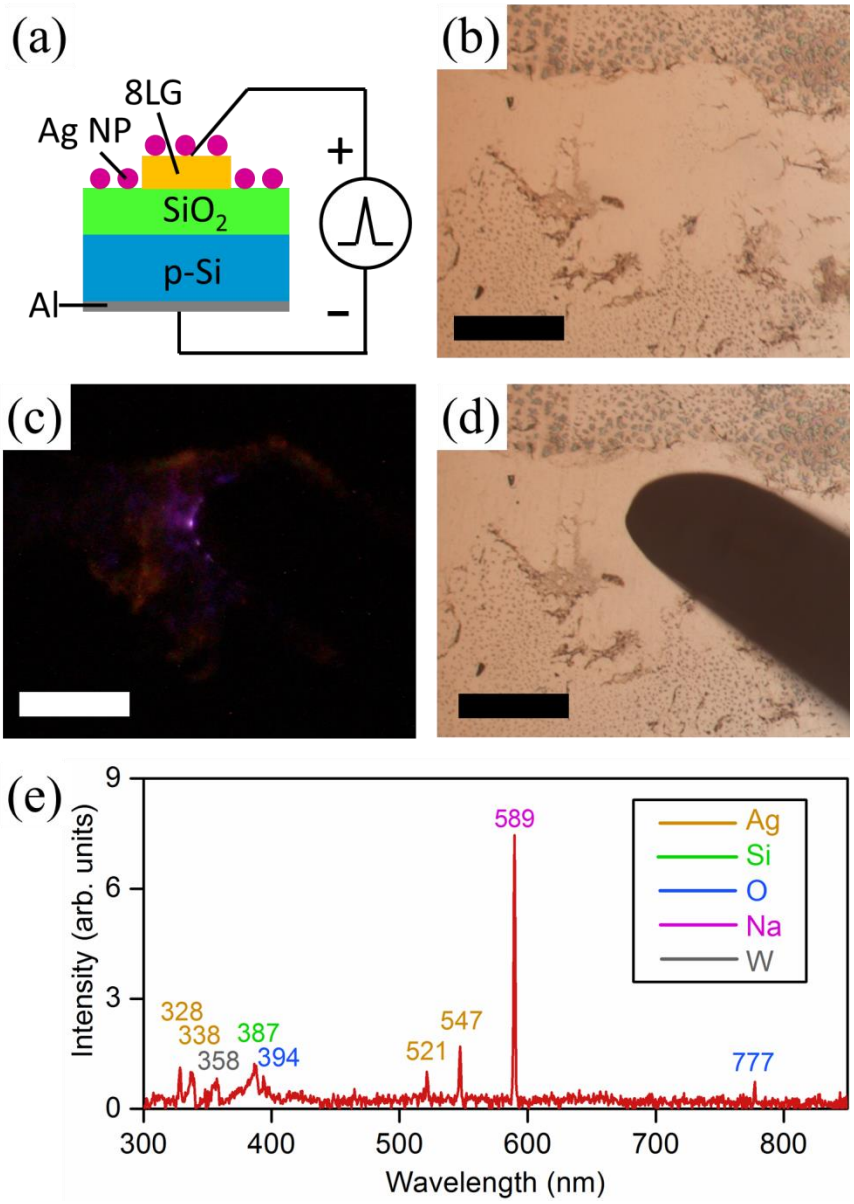

Figure 39 System set-up (a), emission spectra (f) and photo image of Ag NP/ 8-layer graphene/ 10 nm thermal oxide/ p-Si. Pulse polarity as marked with 50 V amplitude and 10 μs width. 20 pulses are applied manually with 1 second interval. Scale bar: 300 μm.

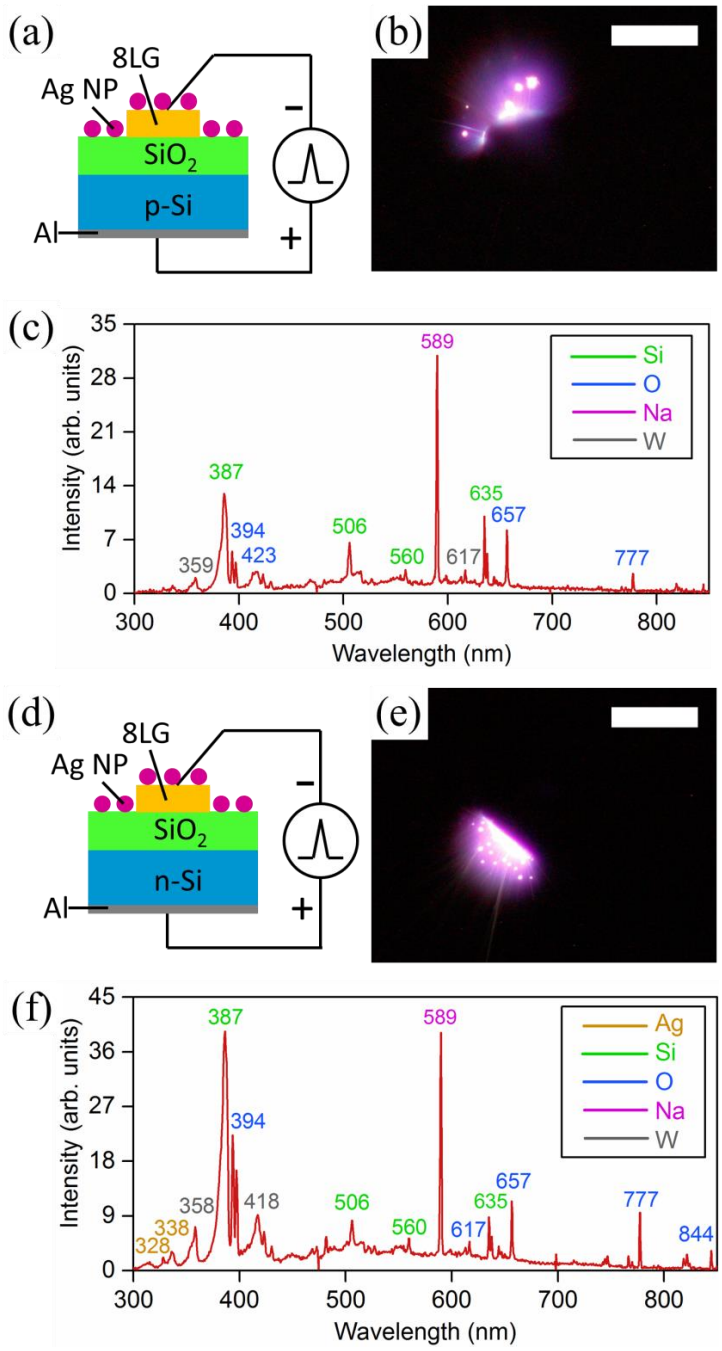

Figure 40 System set-up (a), emission photo image (b) and spectrum (c) of Ag NP/8-layer layer graphene/ 10 nm thermal oxide/ p-Si with 80 V amplitude and 20 μs width pulses applied 30 times in total. System set-up (d), emission photo image (e) and spectrum (f) of Ag NP/8-layer layer graphene/ 10 nm thermal oxide/ n-Si with 50 V amplitude and 10 μs width pulses applied 30 times in total. Scale bar: 300 μm.

4.2.4 AES for CdSe quantum dot on GOS substrate

AES of CdSe QD spin coated on 8-layer graphene/ 10 nm thermal oxide/ p-Si is shown in Figure 41. Positive pulse (top positive and bottom negative) with 50 V amplitude and 10 μs width are applied. Pulses are triggered manually with 1 second interval if not specified. The blue luminescence corresponds to wavelength of 509 nm from Cd distinctively. Like the Ag NP case, the overlapping area has highest emission intensity. Cd, Si, O, Na and W elements are identified in the atomic spectra. If the position of 8-layer graphene and CdSe QD layer is switched as shown in Figure 42, the emission intensity would drop because the CdSe QD layer reduce the graphene electrode contact and therefore carrier transport efficiency.

4.2.5 AES on sputtering deposited oxide

When nano-channels or defect exist in the oxide that allow current leak through before oxide breakdown, the emission intensity is stronger. As shown in Figure 43, both the photo image and emission spectrum proves that sputtering deposited oxide in monolayer graphene/25 nm oxide/n-Si provides higher intensity during atomic emission than thermal grown oxide. Sputtering deposited oxide is known to have intrinsic defects and possibly nano-leakage-channels. Further experiments will be done in the future on GOS sample with EBL made channels to confirm this effect.

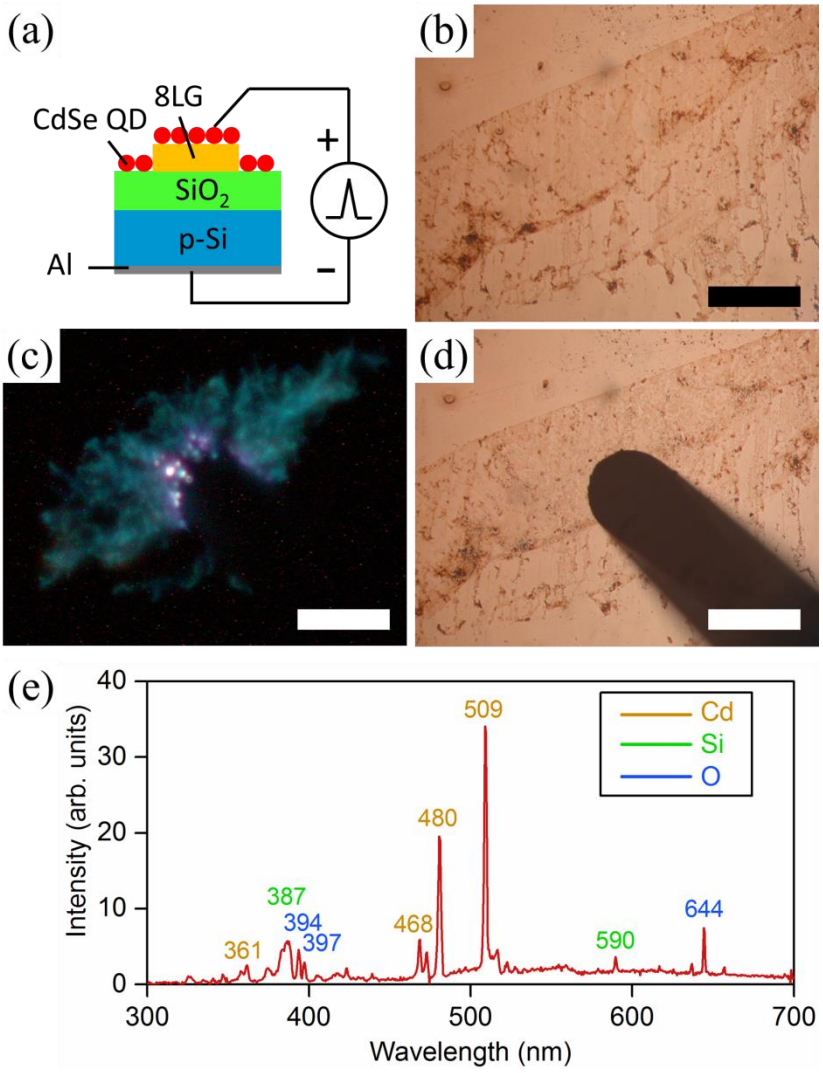

Figure 41 System set-up (a), emission spectra (f) and photo image of CdSe QD/8-layer graphene/10 nm thermal oxide/p-Si. Pulse polarity as marked with 50 V amplitude and 10 μs width. 10 pulses are applied in total. For the photo image: (b) before test. Scale bar: 300 μm.

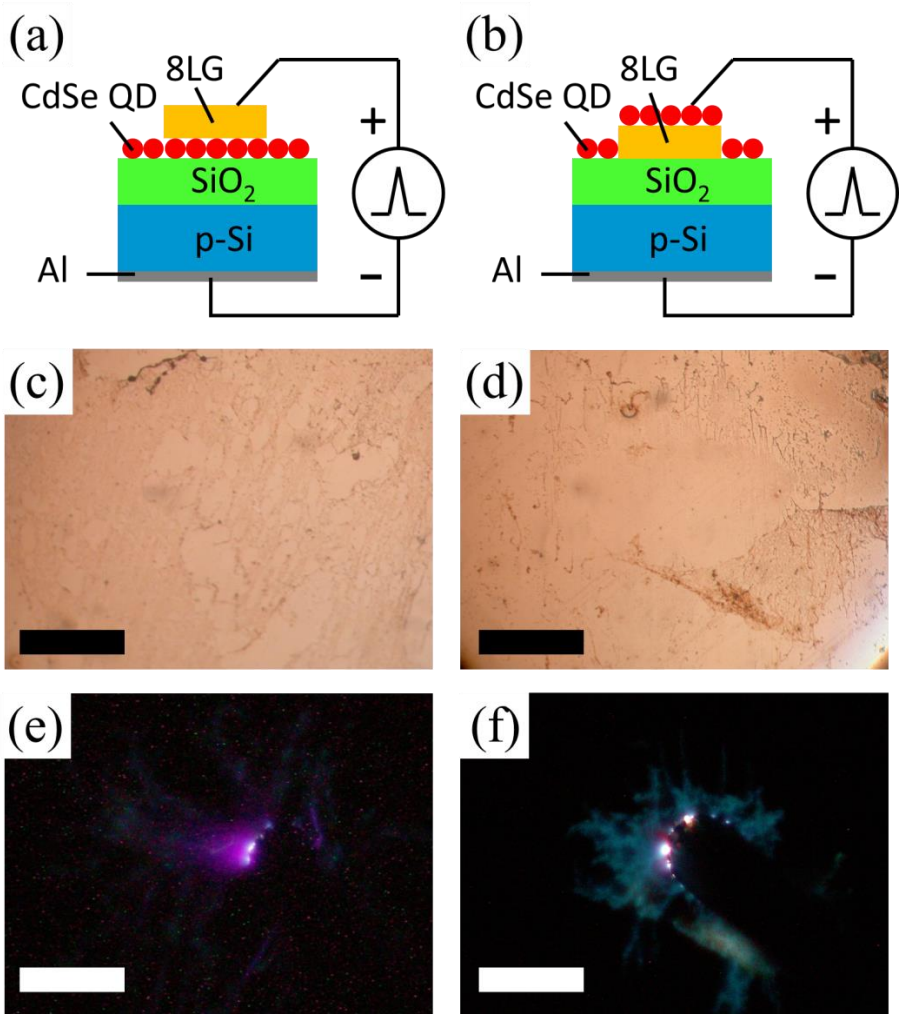

Figure 42 System set-up and photo image of 8-layer graphene/ CdSe QD (a) (c) (e) and CdSe QD/8-layer graphene (b) (d) (f) on 10 nm thermal oxide/ p-Si substrate. Pulse polarity as marked with 50 V amplitude and 10 μs width. 10 pulses are applied manually with 1 second interval. Scale bar: 500 μm.

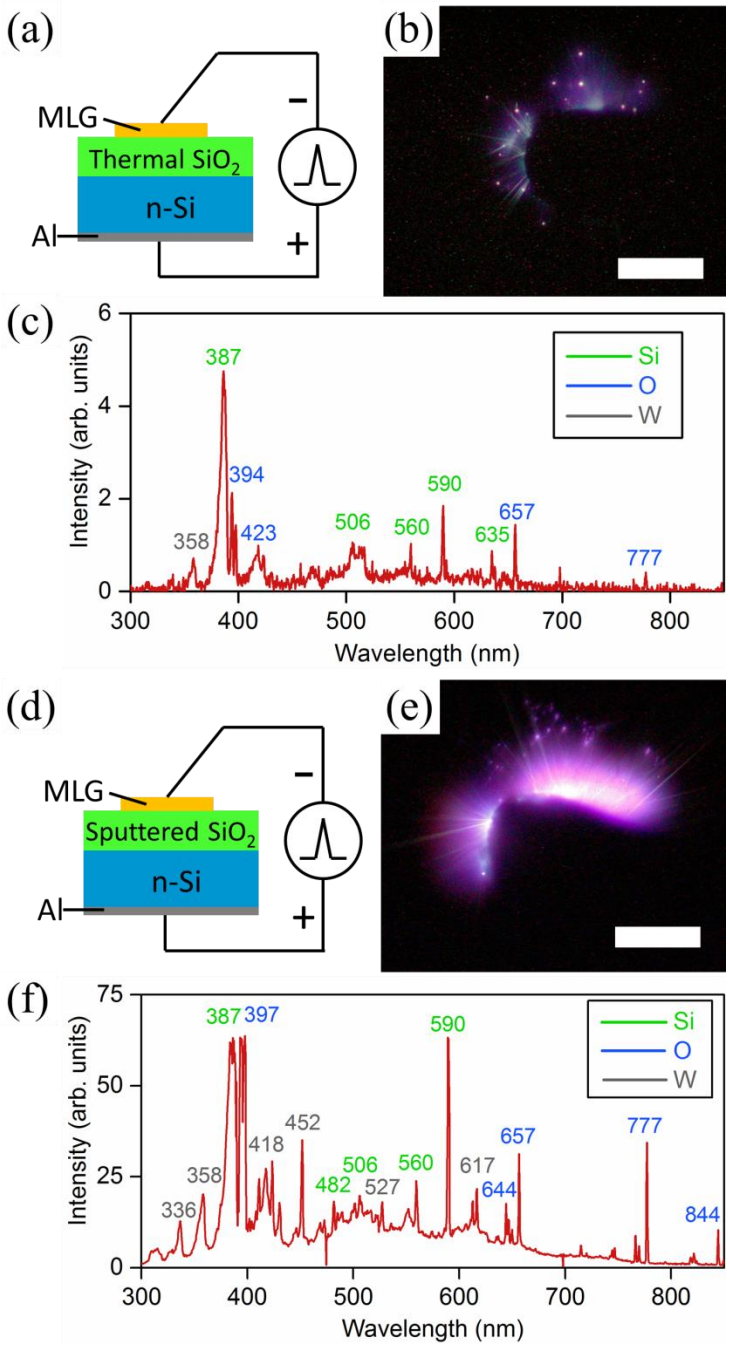

Figure 43 System set-up (a), emission photo image (b) and spectrum (c) of monolayer graphene/ 10 nm thermal oxide/ n-Si with 90 V amplitude and 10 μs width pulses applied 30 times in total. A sample with sputtered oxide instead of thermal oxide under same test condition is shown in (d) (e) (f). Scale bar: 200 μm.

4.2.6 Black body radiation from atomic emission

The spectral irradiance from a blackbody can be calculated from Planck's law:

$$\mathrm{B}(\lambda, \mathrm{T}) = \frac{2hc^2}{\lambda^5} \frac{1}{e^{hc/\lambda kT} - 1}$$

We did curve fitting in Figure 44 for two of the atomic spectrum collected from GOS structure discussed in section 4.2.1. The blackbody radiation indicates a temperature of ~6100 K during explosion. AES with clear black body radiation is observed either under high frequency pulse drive with high voltage (Figure 45) or DC bias drive (Figure 46).

In Figure 45, tungsten probe probes directly on oxide serving as top electrode. Negative pulses with 0.1 s period, 100 V amplitude and 1 ms width are applied via pulse generator for 30 seconds. Si and W elements are identified. Distinct black body radiation appears together with atomic line, causing by the heating of large injection current. The emission image presents a glowing edge and the surface is heavily burned. Si and W elements shows their atomic lines in the spectra while in a very different position as before in the other sections, indicating a different explosion property. The sample temperature during explosion is estimated to have reached ~5200 K level according to blackbody radiation curve fitting.

In Figure 46, DC voltage scans from +1 V to -25 V with step of 0.5 V for 30 seconds. The Ag is heated by continuous low voltage current injection. The atomic emission is generated due to high temperature (~4900 K) thermal melting. Only Ag is identified with low intensity.

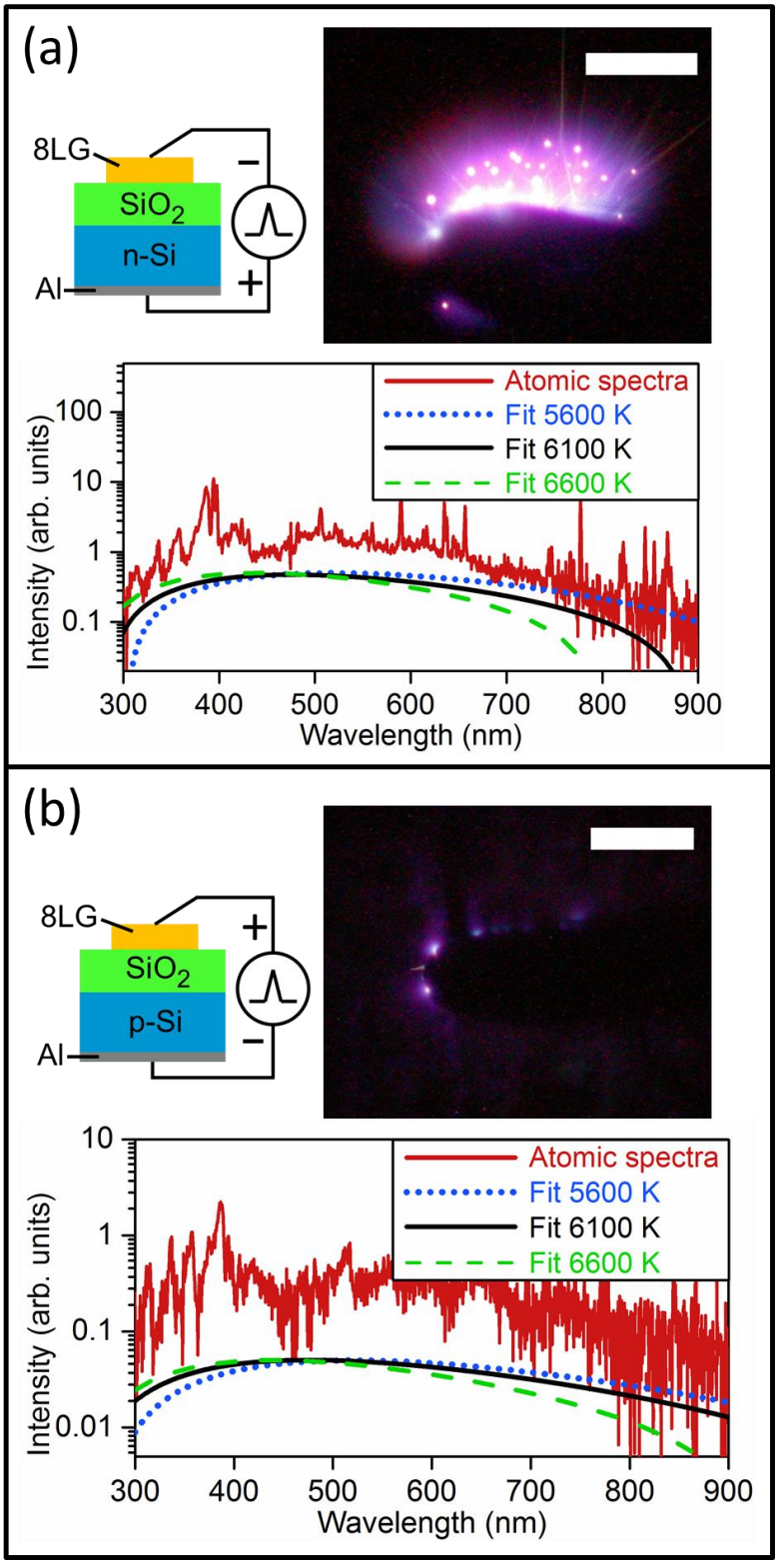

Figure 44 Blackbody radiation curve fitting for atomic emission from GOS structure under inversion bias.

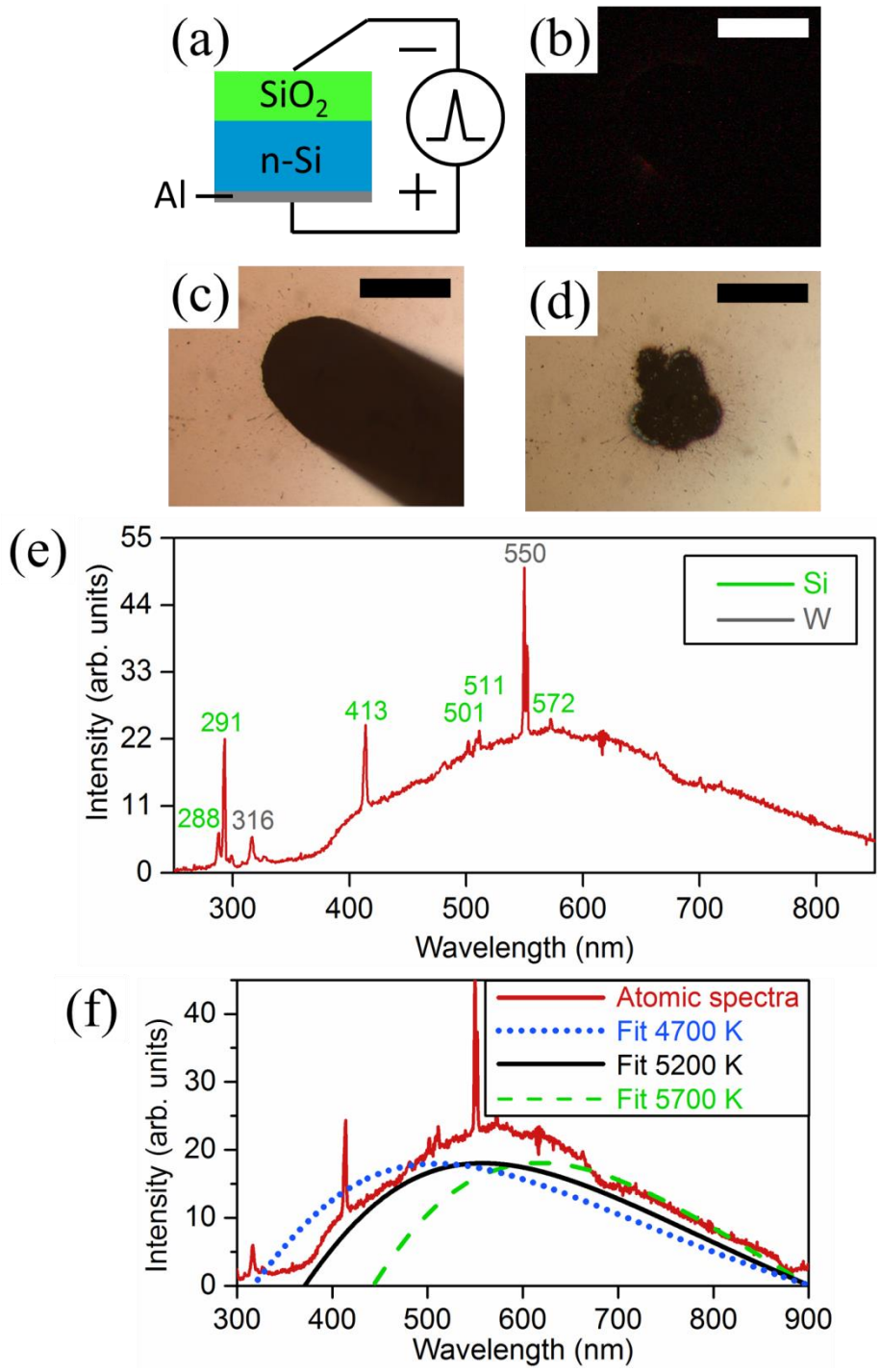

Figure 45 System set-up (a), emission spectra (e) (f) and photo image of monolayer graphene/25 nm sputtering oxide/n-Si. Pulse polarity as marked with 0.1 s period, 100 V amplitude and 1 ms width. 300 pulses are applied via pulse generator. Scale bar: 300 μm.

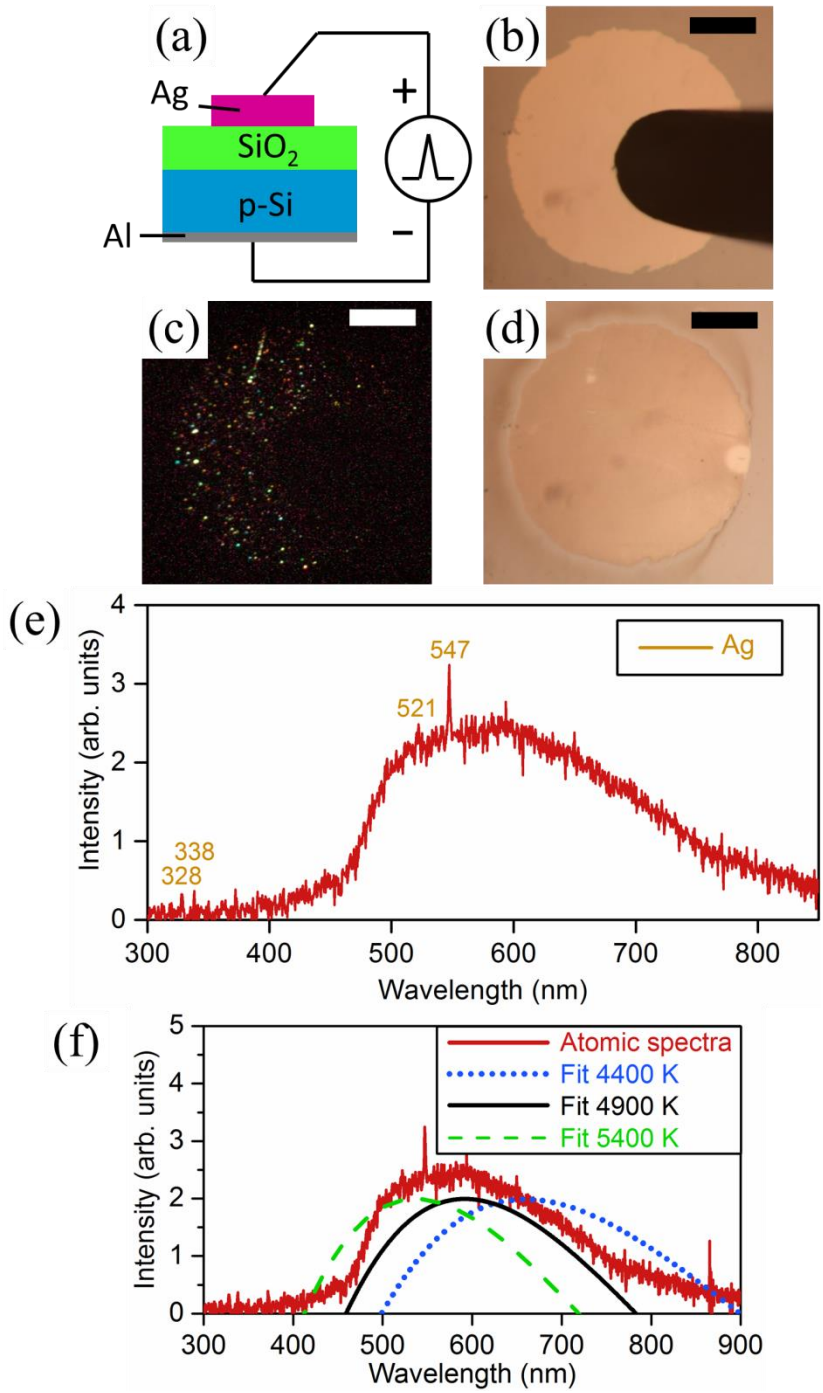

Figure 46 System set-up (a), emission spectra (e) (f) and photo image of 15 nm Ag/10 nm thermal oxide/p-Si. DC voltage scans from +1 V to -25 V with step of 0.5 V for 30 seconds. For the photo image: (b) before test; (c) during emission with tungsten probe on; (d) after emission. Scale bar: 200 μm.

4.3 POST-AES DESTRUCTION STUDY

In this work we have focused on inversion bias cases: positive gate (graphene) voltage pulses applied to p-Si GOS; negative gate (graphene) voltage pulses applied to n-Si GOS structure. The AES-tested (i.e., exploded) GOS samples were characterized in terms of their surface morphologies and damage extent. The breakdown damages are found to be significantly different between the two structures: highly localized, circular, protruding/deep melt explosion of Si for the n-Si GOS case; shallow, irregular, widely spread, meandering trench-like eruptions in SiO_2/Si for the p-Si GOS case. Based on this result we propose the underlying mechanisms of oxide breakdown/explosion of GOS under high-field voltage pulses.

4.3.1 Polarity dependence of lateral breakdown propagation

As been discussed in section 3.4, lateral breakdown propagation is observed and discussed when oxide film is exposed to high electric field. A polarity dependence of lateral propagation is found in all our experiments. Despite the doping polarity of silicon substrate, post-explosion damage reveals distinct propagation track and depth only depending on the polarity of gate voltage.

Atomic explosions of GOS device under inversion bias condition are more easily triggered than accumulation bias. Therefore, inversion bias is chosen to be our excitation condition. The optical micrograph of AES on 8-layer-graphene/SiO_2/Si are shown in Figure 47 and 48 for p-Si and n-Si substrate as examples of positive gate voltage bias and negative gate voltage bias respectively. Light emission region agrees with the post-AES damage area later presented in Figure 49 by SEM and in Figure 50 by AFM.

When the gate electrode is positively biased, the emission light has weak intensity but distributes dispersive within a certain distance away from the probe contact point (Figure 47 (b)). The spread distance confined by the potential spread area of graphene electrode on oxide. The graphene electrode around the eruption sites is fragmented/ detached into flakes by the explosion. SEM image reveals a network of randomly-distributed trenches on the sample surface. The trenches have a meandering and branched pattern. Most part of the network is well connected, indicating that the trenches formed in a laterally propagating mode during explosion. We also noticed that the connection joints of these destruction paths are more severely damaged that they either protrude up above base level or collapse down below base level. As shown in Figure 49 (c) and (d), the trenches have an average width of 200nm. From Figure 49 (d) we can clearly see the broken flakes of graphene near the destruction region. With further analyzation by AFM (Figure 50 (a) (c)), the trenches have an average depth of 20nm. Remember the original oxide thickness is 10 nm, which means these trenches only goes 10 nm deep into silicon. The relatively shallow trenches observed in the p-Si GOS samples indicate that an explosion occurred primarily in/around the oxide layer and the damage is confined to near the SiO_2/Si interface.

Totally different damage morphologies are observed when the graphene is negatively biased. Highly localized/isolated, circular, protruding eruption damages are observed. The photo images taken during and after emission agree well in the location of explosion spots shown in Figure 48. The explosion spots are more confined near the probe contact point than previous case. The circular destructions are in feasible dimension and depth that are visible under optical microscope. SEM reveals a fine image with more details of an individual spot in Figure 49(b). The extent of damages is measured to be ~1.2-μm-high above the ground level and ~200-nm deep (Figure 50). The base diameter is measured to be 1-30 μm. This dimensional information

suggests a major explosion occurred at each eruption site. The destruction goes few hundreds nanometer deep into silicon. The oxide breakdown in negative bias case is highly localized and isolated. Therefore, intensive current flow is focused on these few points, creating severe damage. Another important difference with the p-Si case is that these eruptions are well isolated and are circularly symmetric with a well-defined cone-shape profile (i.e., protruding at the center). This topography indicates a melt-explosion of Si during the breakdown process. This explosive melting suggests a large current flow through SiO_2/Si, causing Joule heating and melting of Si. (Note that Si's melting temperature is ~1700K.) The ripples (concentric rings: Figure 49(b)) in the edge area of each cone indicate the wave motion of molten material induced by shock loading, and support the melt-explosion hypothesis. It is noteworthy that the damage depth/height (0.2-1μm) approximately matches the depletion region width in Si side. This suggests a large current flow in/through the Si depletion region.

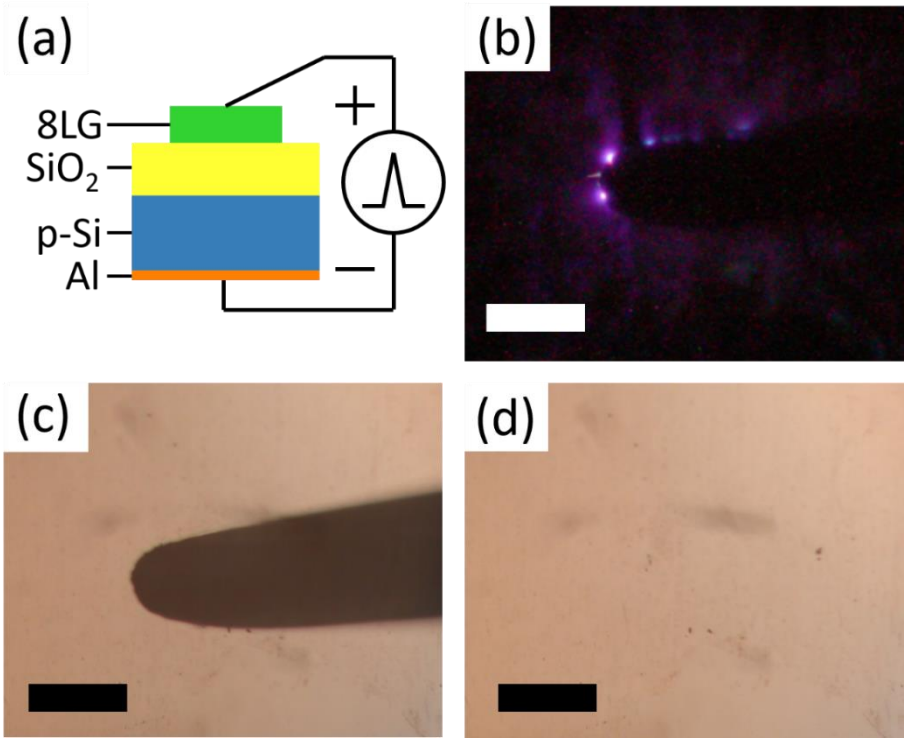

Figure 47 System set-up (a), photo image during emission (b), after test with probe on (c) and without probe on (d) of 8-layer graphene (8LG) /10 nm thermal oxide/ p-Si. 14 pulses for pulses for 8LG with 50 V amplitude and 10 μs width are applied manually with 1 second interval. Scale bar: 500 μm.

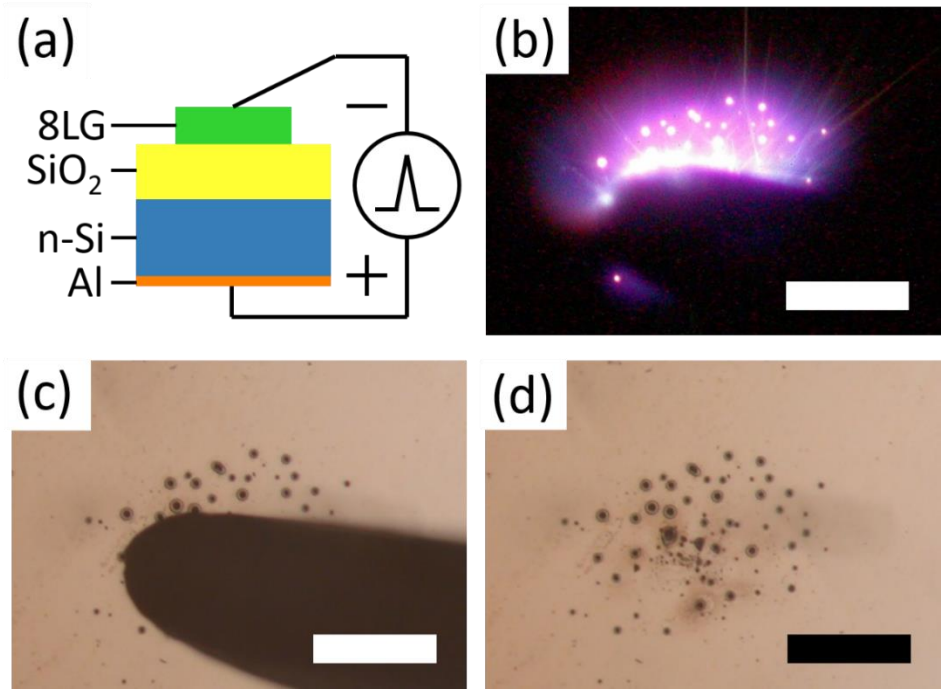

Figure 48 System set-up (a), photo image during emission (b), after test with probe on (c) and without probe on (d) of 8-layer graphene (8LG) /10 nm thermal oxide/ n-Si. 14 pulses for pulses for 8LG with 50 V amplitude and 10 μs width are applied manually with 1 second interval. Scale bar: 300 μm.

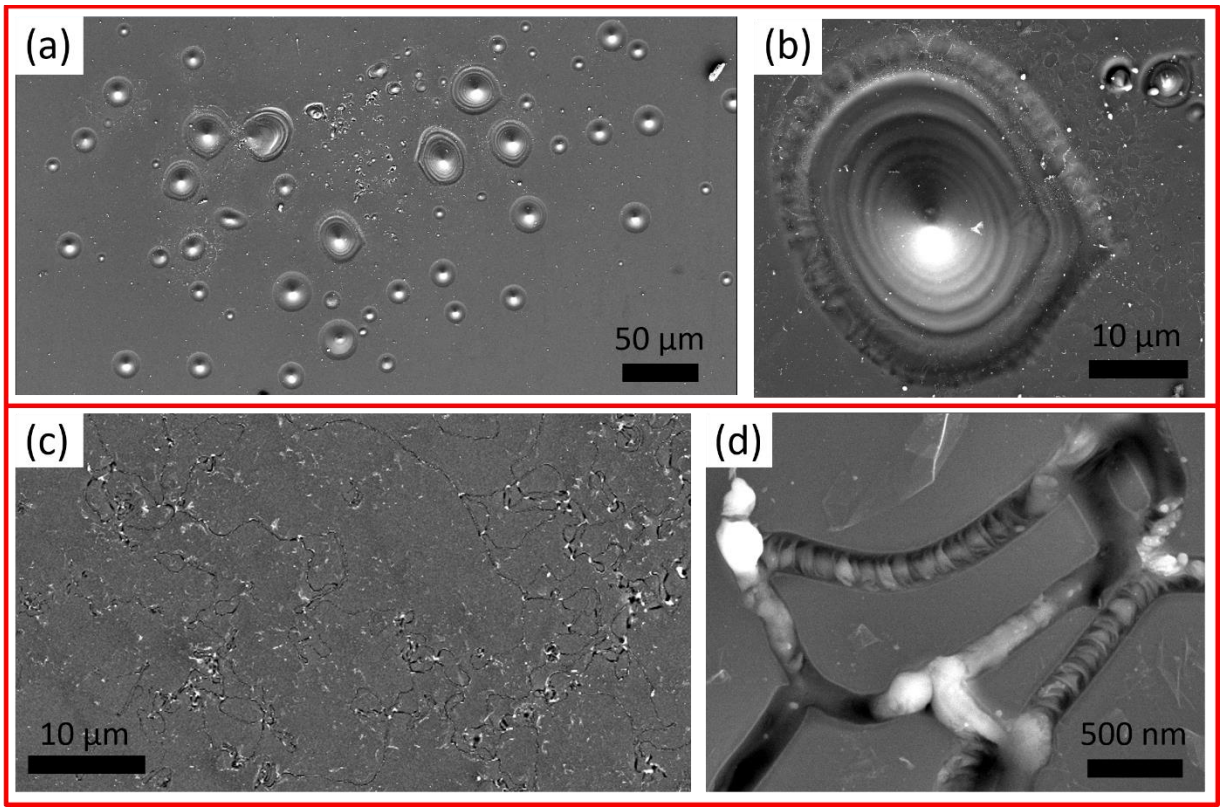

Figure 49 SEM image of post-AES topography for (a) (b) n-Si sample shown in Figure 48 and (c) (d) p-Si sample shown in Figure 47. (b) and (d) are zoomed image for (a) and (c) respectively.

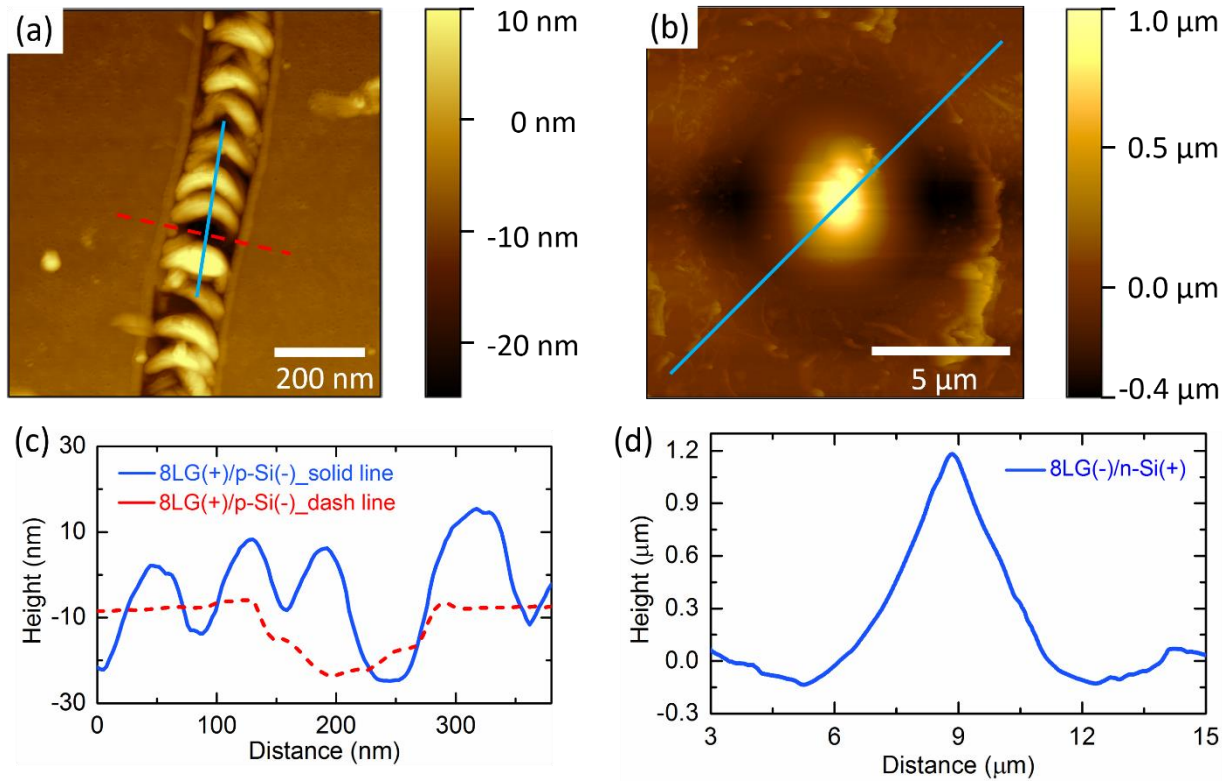

Figure 50 AFM image of post-AES topography for (a) (c) p-Si sample shown in Figure 47 and (b) (d) n-Si sample shown in Figure 48. (c) and (d) are cross-section profile for the identified line region marked in (a) and (b) respectively.

When the top electrode is negatively biased, electrons are injected into SiO_2 from the graphene electrode side via Fowler-Nordheim tunneling. Again under a high-field operation the injected electrons induce impact ionization, generating electron-hole pairs in SiO_2. The generated electrons will drift down towards Si substrate. When entering the Si region, the electrons gain extra energy that corresponds to the conduction band offset (3.15eV). These kinetic electrons will further induce impact ionization in Si depletion. The multiplication process then intensifies toward the Si side, resulting in an opposite profile compared with the p-Si case. A large current flow, deeply penetrating into the depletion region, will then result in a major melt-explosion of Si with a correspondingly large, extended damage. In the n-Si case, a center-protruding profile (cone shape) is consistently observed. When Si melts under a large current flow, the Si atoms will form ions (i.e., forming a plasma state). These positively charged Si ions will then be pulled upward by the inversion bias field (negative voltage to graphene) shaping the melt into a highly symmetric cone-shape (Figure 51). The center-protruding profile observed with the n-Si GOS case is ascribed to this Coulombic interaction of Si melt with the applied field.

The discrete nature of damaged spots can be ascribed to the relatively poor adhesion/integrity at the graphene/SiO_2. When an explosion occurs at a particular site, the graphene electrode is easily fractured and detached around that area. Note that a carrier multiplication is initiated by electron injection from the graphene side. Once the local area of graphene electrode gets detached by an explosion, there cannot be further explosion in nearby area.

The situation differs in the p-Si case, which demonstrates a laterally-extended defect profile as discussed above. In the p-Si case the carrier multiplication is initiated by electron injection from the Si side. The adhesion/integrity of thermally-grown SiO_2/Si interface is known

to be excellent and the nearby area is unlikely to be affected by the shallow/local explosion. The oxide breakdown process can laterally propagate into adjacent weak spots. The breakdown spots then become connected forming a meandering pattern. With all the adjacent spot connected, we have the meandering, self-avoiding breakdown trace with corrugated wall as shown in Figure 52.

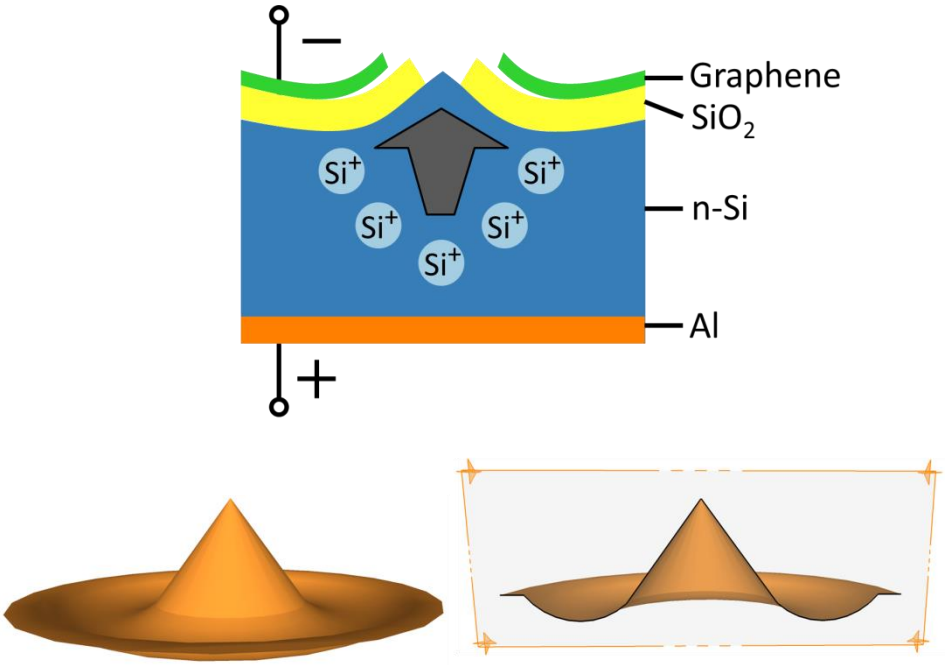

Figure 51 Scheme of GOS device under negative gate bias during explosion. Ionized Si atoms are attracted by electric field moving upward forming center-protruding damage profile.

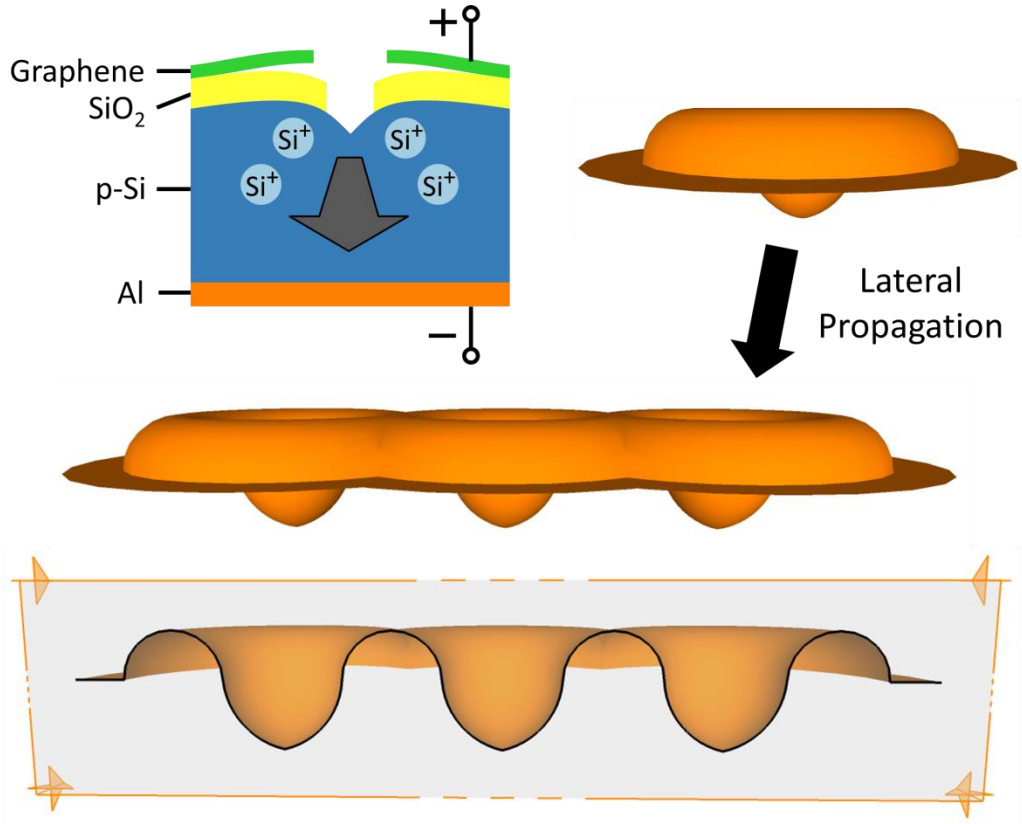

Figure 52 Scheme of GOS device under positive gate bias during explosion. Ionized Si atoms are attracted by electric field moving downward forming center-collapsing damage profile. The oxide breakdown propagates laterally while the adjacent breakdown spots join each other.

4.3.2 AES on GOS substrate with EBL-made hole arrays

The physical mechanism of laterally propagating damages observed with p-Si samples are further studied by employing a nano-hole-patterned GOS structure. First, thermal oxide with thickness of 23 nm is grown on p-Si and n-Si. After that, hole arrays pattern with 100-nm diameter are made on SiO_2/Si substrate by e-beam lithography using Raith Ultra high resolution Electron Beam Lithography e-Line. Area dose of 215 As/cm_2 and area step size of 0.02 μm is applied. The pattern is etched by Trion Technology Phantom III LT RIE system. The flow rate of CF_4 and O_2 are 45 sccm and 5 sccm respectively. The chamber pressure and RF power are set to be 150 mTorr and 60 W. Scheme and SEM images of EBL-made hole arrays are shown in Figure 53 on p-Si and Figure 54 on n-Si. Due to the etch rate difference, the etching depth of n-Si is 20 nm that the hole didn't penetrate oxide. Although the shallow hole may not perform as good as normal nano-hole in oxide, it would still show some nano-hole effects if exist.

Pulse with 50 V amplitude and 10 μs pulse width are applied to the GOS device with EBL made nano-holes. To operating under inversion bias, positive pulses are applied to p-Si based GOS (Figure 55) and negative pulses are applied to n-Si based GOS device (Figure 56). As we marked by yellow dashed square in Figure 55(b) and Figure 56(b), EBL patterned area didn't exhibit strong emission intensity in either case. The SEM image reveals the post-explosion damage tracks near hole arrays in Figure 55(e). The lateral propagation approach to the EBL patterned area and bounce back immediately before move in further. A global view of destruction map shown in Figure 56(e) also supports the fact that the EBL patterned area prohibit atomic explosion.

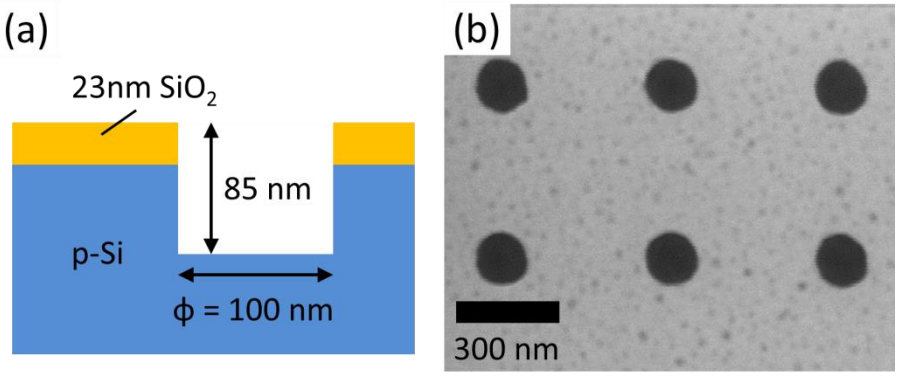

Figure 53 Scheme (a) and SEM images (b) for EBL-made hole arrays on p-Si with diameter of 100 nm, hole-hole spacing of 500 nm and depth of 85 nm.

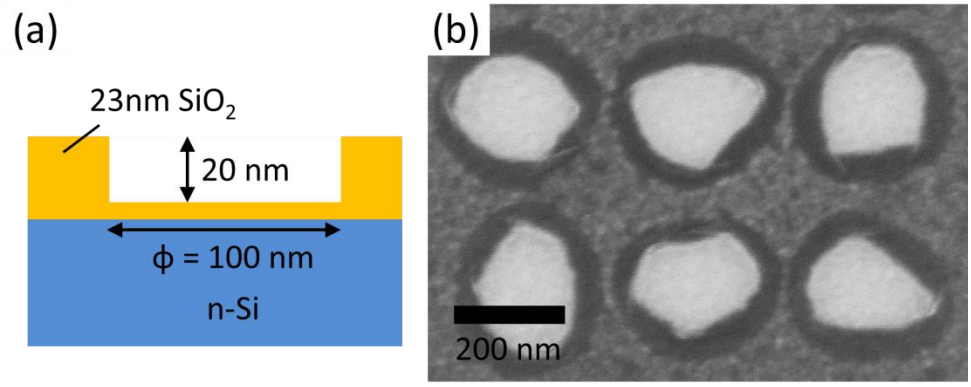

Figure 54 Scheme (a) and SEM images (b) for EBL-made hole arrays on n-Si with diameter of 100 nm, hole-hole spacing of 500 nm and depth of 20 nm.

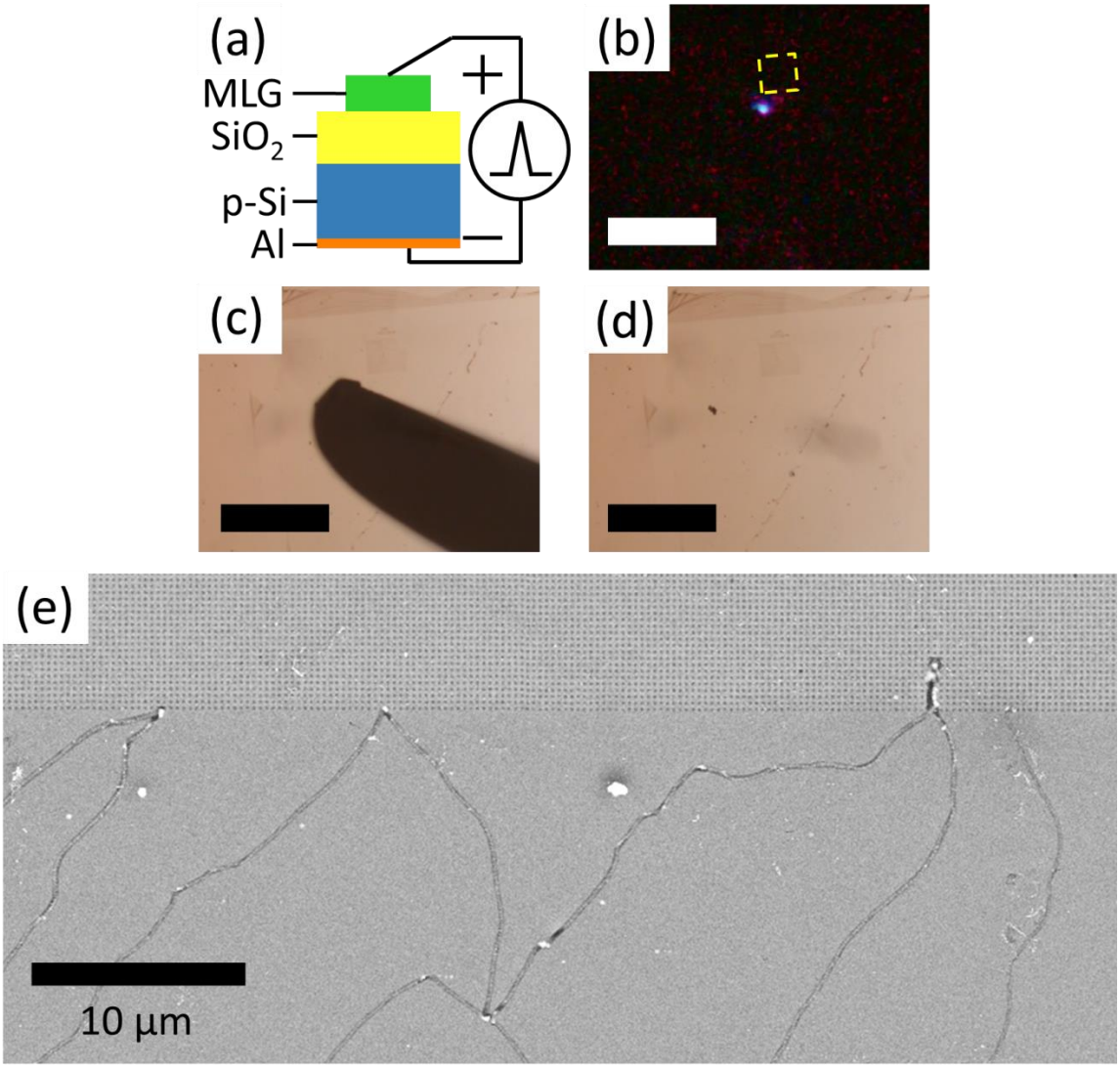

Figure 55 System set-up (a) and photo image of monolayer graphene/ 23 nm thermal oxide/ p-Si. Pulse polarity as marked with 50 V amplitude and 10 µs width. 2 pulses are applied manually with 1 second interval. Scale bar shows 300 µm in the photo images: (b) during emission with tungsten probe on; after emission with probe (c) and without probe on (d). The EBL patterned area is marked in yellow dash line in (b). SEM image near EBL hole arrays is shown in (e).

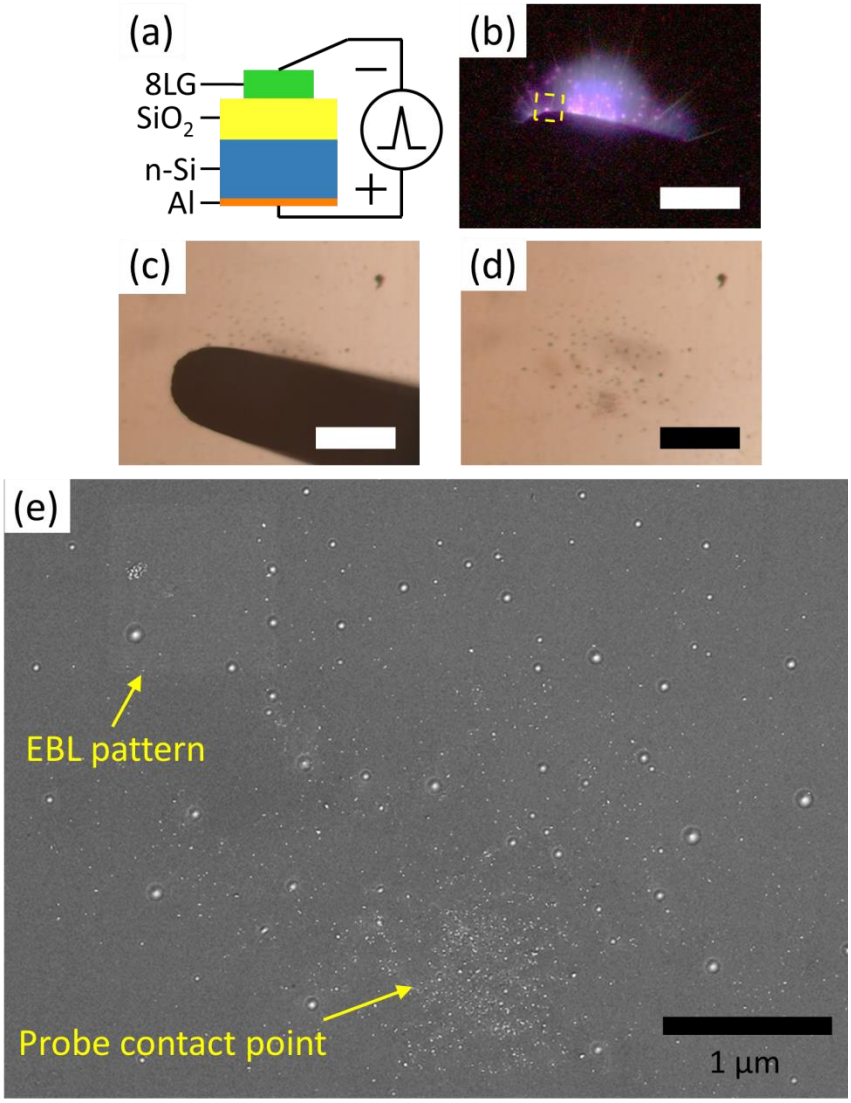

Figure 56 System set-up (a) and photo image of monolayer graphene/ 23 nm thermal oxide/ p-Si. Pulse polarity as marked with 50 V amplitude and 10 µs width. 2 pulses are applied manually with 1 second interval. Scale bar shows 300 µm in the photo images: (b) during emission with tungsten probe on; after emission with probe (c) and without probe on (d). The EBL patterned area is marked in yellow dash line in (b). SEM image near EBL hole arrays is shown in (e).

This behavior of defect propagation (avoiding the nano-hole area) can be explained as follows. When an explosion occurs at a particular side creating a void channel, the local capacitance will drop. The inversion charges formed at the interface will also drop, making electron injection difficult.

Under the same electric field, the charge amount varies with the capacitance ($Q = CV$). The capacitance of SiO_2 is $C_{ox} = \varepsilon_0 \varepsilon_{ox} A/d$, where $\varepsilon_{ox} = 3.9$ is the dielectric constant of oxide, A is the area and d is the thickness. The nano-hole area can be treated as air capacitor with capacitance of $C_{air} = \varepsilon_0 \varepsilon_{air} A/d$, where $\varepsilon_{air} = 1.0$. The capacitance of SiO_2 area is 4 times greater than the nano-hole area, therefore 4 times larger charge density at the SiO_2/Si interface.

Also note that the carrier multiplication process in p-Si case involves a positive feedback effect (i.e., hole injection into Si) as discussed above. When a void channel develops this hole injection becomes impossible, disabling the carrier multiplication process at the explosion site. The inversion electrons will then look for fresh sites nearby and make explosions there. This explosion process will continue with random migration, forming a meandering pattern.

We also observed extra information from a detailed SEM image shown in Figure 57 (c) about the oxide breakdown propagation direction. The corrugation profile observed in the trench bottom suggests that local melt-explosions occurred and continuously migrated to adjacent sites leaving behind a particular pattern of wavefront after each explosion. From this corrugation pattern, the damage propagation direction is determined. The corrugate pattern of destruction left by explosion is bending toward one direction before the joint. It can be explained that the new breakdown spot will push and squeeze the explosion site left by the previous breakdown spot. Therefore, the corrugate pattern is protruding toward the opposite direction of propagation.

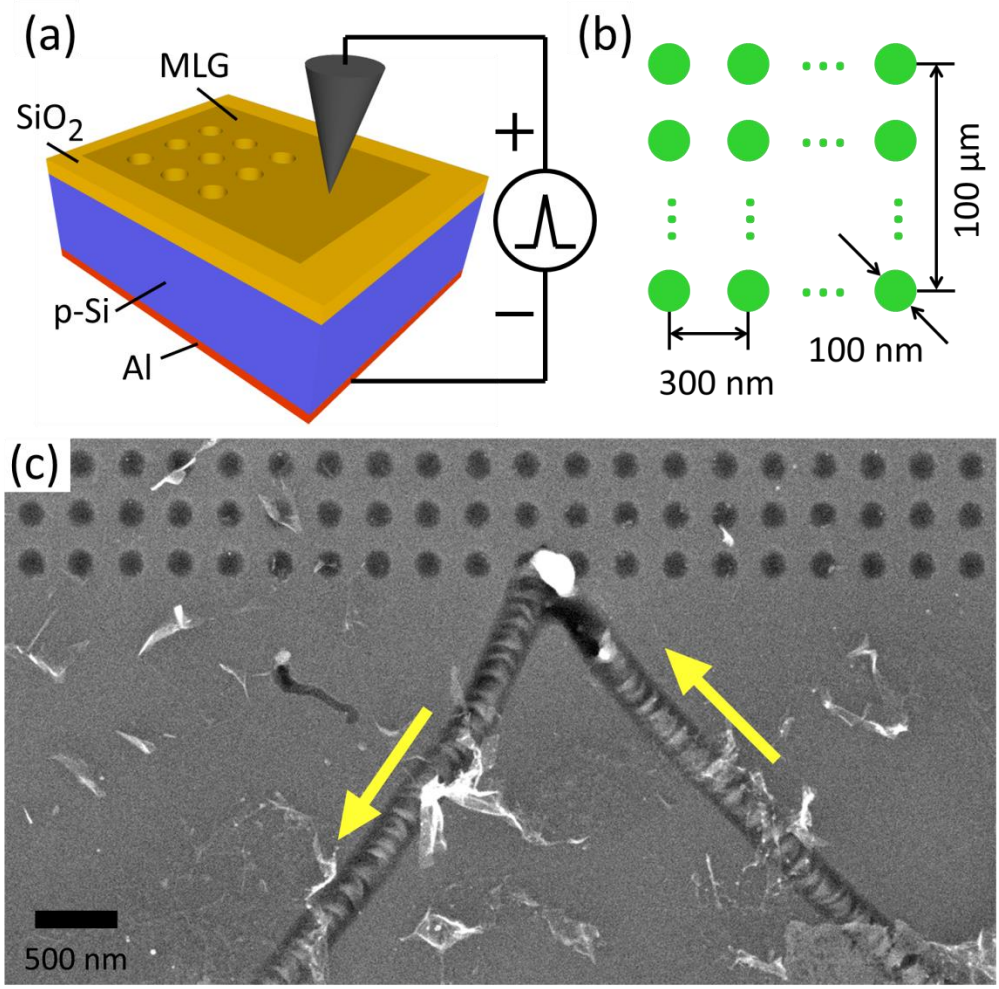

Figure 57 (a) 3D Scheme of system set-up for AES test on monolayer graphene/ 23 nm SiO_2/ p-Si with EBL made nano-hole arrays. (b) Dimension information for the hole arrays. (c) SEM image of oxide breakdown propagation track near EBL pattern. Yellow arrows indicate the proposed propagation direction.

4.4 PHYSICAL MECHANISM

To understand the principle of carrier transport and corresponding effect in our graphene/oxide/silicon (GOS) structure, we group and compare the working condition in three pairs: (1) p-Si versus n-Si as the substrate of GOS structure under positive gate voltage bias, (2) p-Si versus n-Si as the substrate of GOS structure under negative voltage bias and (3) GOS structure under inversion bias versus accumulation bias. Both experimental results and theoretical simulations are considered.

4.4.1 GOS substrate under positive gate voltage bias

When positive gate voltage is applied on the graphene, GOS device based on n-Si is working under accumulation bias while p-Si is operating under inversion bias. A depletion region of ~1 μm width will appear at the interface of siliocn and oxide with a few nanometer of inversion layer in between as well. As shown in Figure 59 and Figure 60, the electrons are attracted and moving upward via Fowler-Nordheim tunneling from silicon side to graphene side. Under a extreme high field, impact ionization occurs in both SiO_2 and the depletion region of Si. After intensive multiplication over distance, The current density reaches maximum at the interface of oxide and grahene, generates large Joule heat while flowing through oxide.

Our experimental work demonstrates that the inversion bias allows easier explosion and stronger atomic emission than the accumulation bias case. In both cases, electrons are injected upward from Si side to graphene anode. Note that the energy barrier for electron injection into

SiO_2 is significantly smaller than that of hole injection: 3.15eV conduction band offset at Si/SiO_2 versus 4.17eV valence band offset; the hole injection into SiO_2 is therefore expected to be negligible as shown in the flat band diagram (Figure 58). Injected electrons will get multiplied through impact ionization in SiO_2, generating electron-hole pairs under high-field voltage pulses. Electrons will drift up towards the graphene anode and holes will travel down to Si side. When holes enter the Si side they will become hot by gaining a certain amount of kinetic energy that corresponds to the valence band offset. The kinetic holes are expected to encounter different situations in Si, depending on the bias polarity and substrate conductivity: further impact ionization in the depletion region in the inversion p-Si case or recombination with electrons in the accumulation n-Si case. This differing situation in the Si side (presence or absence of a depletion region) would result in a different amount of current flow and therefore Joule heating and explosion. Our experimental study (SEM analysis of damaged surface morphology of inversion biased samples) reveals a large density of explosion sites scattered across the graphene anode. The explosion damage depth appears to be relatively shallow, compared to the inversion biased n-Si case. This difference suggests that less kinetic holes are involved in the carrier multiplication process, compared with more kinetic electron injection/multiplication in the inversion-biased p-Si case.

Experimentally, atomic emission of p-GOS can be triggered by using pulse drive with 50 V amplitude or less (down to 25 V) under inversion bias. However, atomic explosion of n-GOS device with same oxide thickness, silicon resistivity and gate voltage polarity which operate under accumulation bias can only be triggered by pulses drive with amplitude above 90 V. As shown in Figure 59, the depletion region in GOS device under inversion bias provides extra distance for impact ionization before electrons enter oxide. This process generates electrons with

high kinetic energy which provide more electrons and higher possiblity for impact ionization in oxide. In the meanwhile, holes tunneling through oxide are accelerated and seperated from electrons by the depletion field, avoiding electron-hole recombination at the interface of oxide and silicon.

The depletion region in GOS device under inversion bias generates electrons with high kinetic energy for impact ionization in oxide and also eliminates the surface recombination rate. A higher carrier concentration at the interface of oxide and graphene is obtained as a result of strong impact ionization. Eventually, atomic explosion triggered by Joule heating or Coulomb fission is observed.

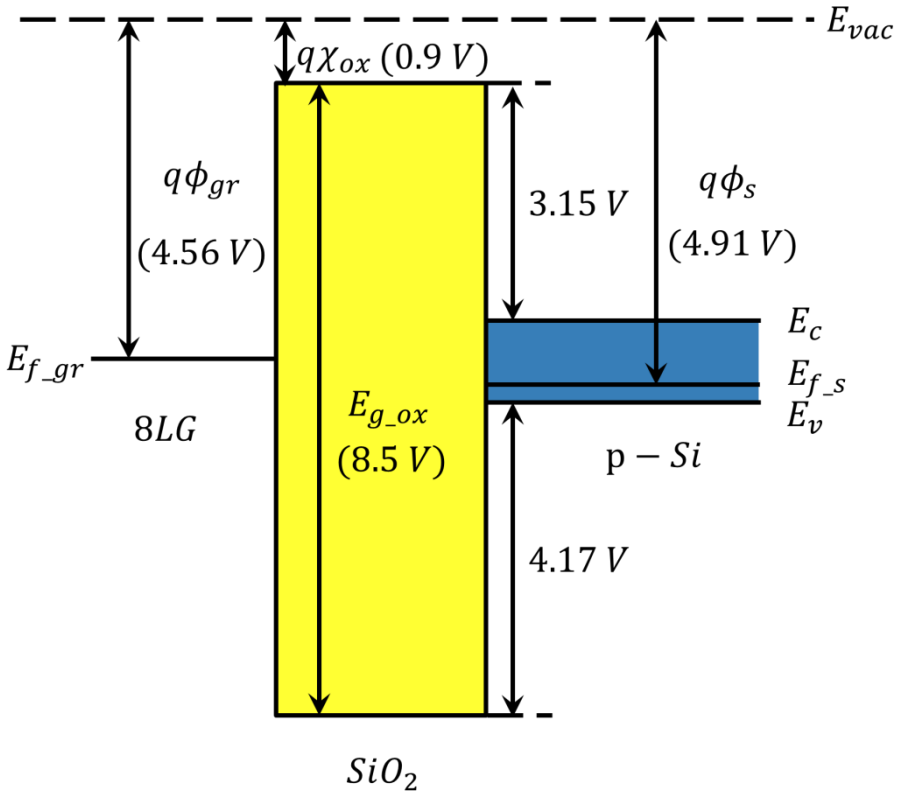

Figure 58 Flat band diagram of 8-layer-graphene/SiO_2/p-Si.

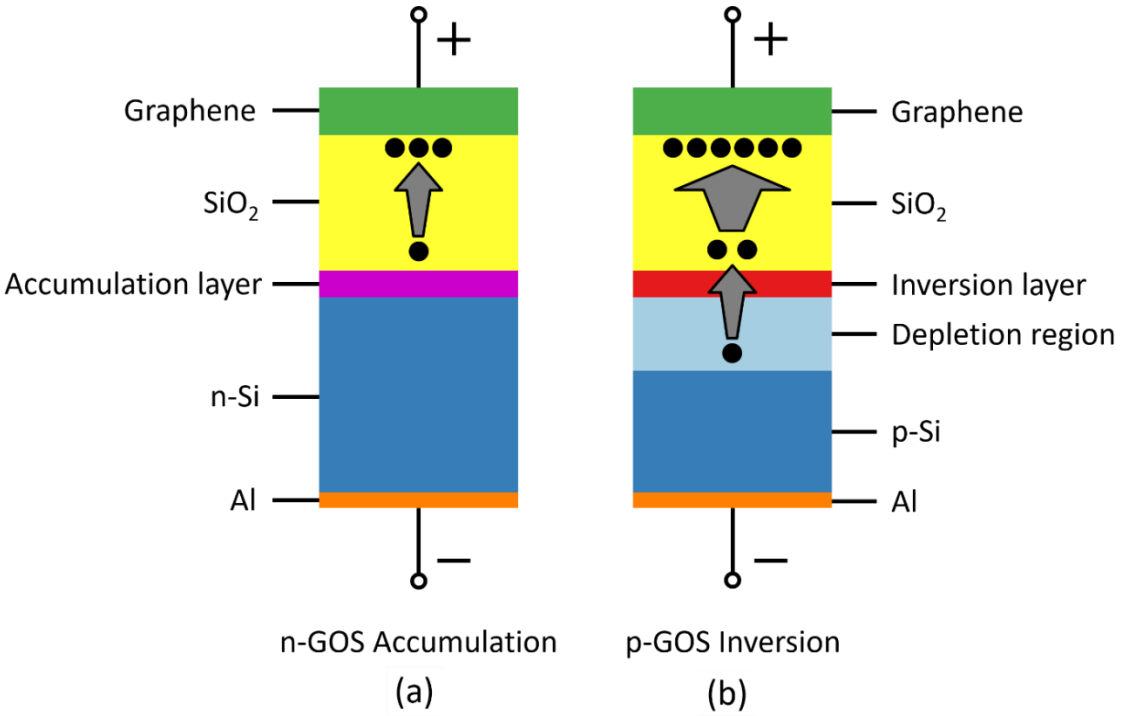

Figure 59 Graphene/SiO_2/Si under positive gate bias, which means accumulation bias for n-Si substrate (a) and inversion bias for p-Si substrate (b). The moving directions and multiplication process of electrons are indicated by black particles and arrows not to scale.

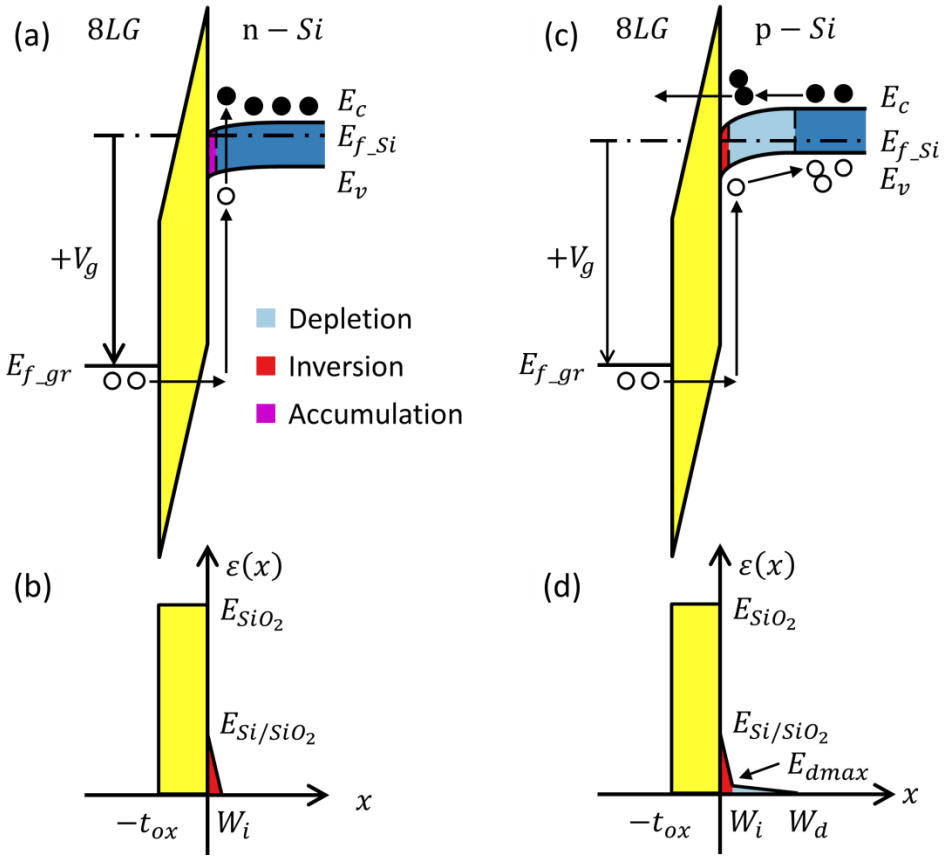

Figure 60 The band diagram and electric field distribution of the GOS devices shown in Figure 59 for (a) (b) n-Si substrate and (c) (d) p-Si substrate.

4.4.2 GOS substrate under negative gate voltage bias

Similar to positive gate bias, we observed a lower AES triggering requirement for inversion bias condition, which means applying negative pulses on n-Si based GOS device. Due to the limitation of our instrument, from which the maximum pulse amplitude is 100 V, we are unable to trigger the atomic explosion of p-Si by negative pulses (accumulation bias).

The scheme of carrier injection and flow under negtive gate bias is plotted in Figure 61. Band diagrams with carrier motions in depletion region and electric field distribution in silicon is shown in Figure 62. When the gate electrode is negatively biased, electrons impinge down through oxide into silicon. Impact ionization occurs intially in oxide and then further continues in depletion region, generating large current in Si. Without depletion field, the electrons tunneling through oxide will stop multiplication and recombine with accumulated holes immediately.

In Figure 61 we compare two different cases of bias polarities: (a) accumulation bias of p-Si GOS; (b) inversion bias of n-Si GOS. Note that in both cases electrons are injected down towards the Si side. Our experimental work demonstrates that an inversion bias operation more readily produces stronger atomic emission than the accumulation bias: this indicates that an oxide breakdown occurs more easily in the former case. This different characteristic can be understood in view of the carrier multiplication processes supported by the differently biased GOS structures. In the case of high-field accumulation bias of p-Si GOS, impact ionization is expected to occur in SiO_2, generating electron-hole pairs there as discussed above. The generated electrons then travel down and are injected into Si. Inside Si, however, accumulation holes (majority carriers in p-Si) are awaiting and readily recombine with incoming electrons. By contrast the electron flux in the inversion biased n-Si GOS will encounter a different situation:

the impinging electrons from the SiO_2 side will further induce impact ionization in the high field region near/around the depletion region in Si. The depletion region (~1 μm width) is then easily flooded with incoming electrons and newly generated electrons and holes there. The holes generated in Si side will be separated by the depletion field and flow up toward SiO_2 and graphene anode. The large current flow originating from the depletion region will result in Joule heating and explosive melting of Si and SiO_2. Our experimental work reveals major damage of GOS: local melt explosion of Si with penetration depth of ~1 μm, corresponding to the depletion region width.

4.4.3 GOS substrate under inversion bias

In previous two sections we concluded that inverison bias is more efficient in carrier multiplication because of the existance of depletion region. Experimentally, we found that p-Si under inversion bias has even lower triggering voltage requirement than n-Si under inverison bias. Also, post-breakdown topography is very different as we discussed in section 4.3.

The comparism of electron motions, band diagram and electric field distribution between p-Si and n-Si are plotted in Figure 63 and 64. As we disccussed in section 3.2, the thickness of inversion layer and accumulation layer is less than 1 nm and the depletion width is ~1 μm. The simulation also presents negligible difference between n-GOS and p-GOS in inversion layer thickness, depletion width, electric field strengh and distribution and surfac echarge density. Therefore, the direction of electron migration should be the primary factor causing the morphology differences after oxide breakdown.

For p-Si under inversion bias, ionization multiplication occurs in the depletion region first and the electrons are accelerated by the depletion field before entering oxide. The original

concentration of electrons and the electron energy is much higher than those in n-Si. As a result, impact ionization in oxide of p-Si is easily triggered. The multiplication process would end up at the interface of graphene and oxide where the most severe destructions locate, causing shallow damage with depth of ~20 nm.

For n-Si under inversion bias, impact ionization occurs in the oxide first which requires intense electric field for high energy electrons. After multiplication in oxide, the electrons are further accelerated by the depletion field and more carriers are generated via impact ionization in silicon. The multiplication process would ideally end up at the edge of depletion region which is ~1 μm deep into silicon. Therefore, the destruction depth in n-GOS is hundreds times deeper than in p-Si.

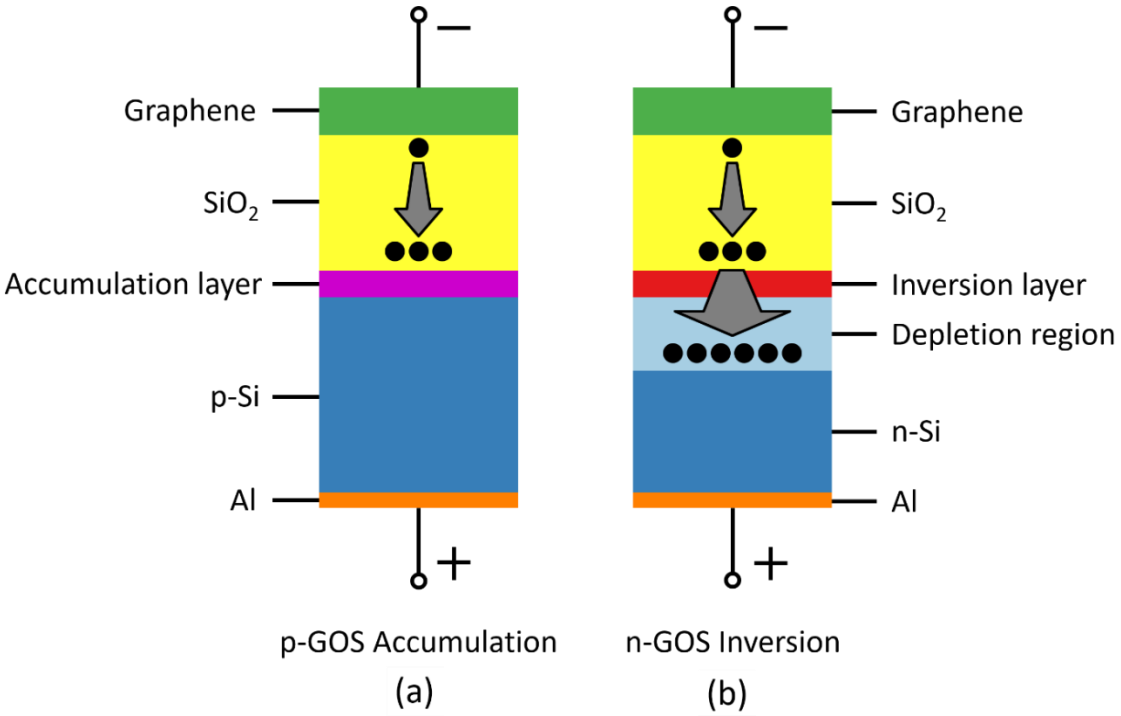

Figure 61 Graphene/SiO_2/Si under negative gate bias, which means accumulation bias for p-Si substrate (a) and inversion bias for n-Si substrate (b). The moving directions and multiplication process of electrons are indicated by black particles and arrows not to scale.

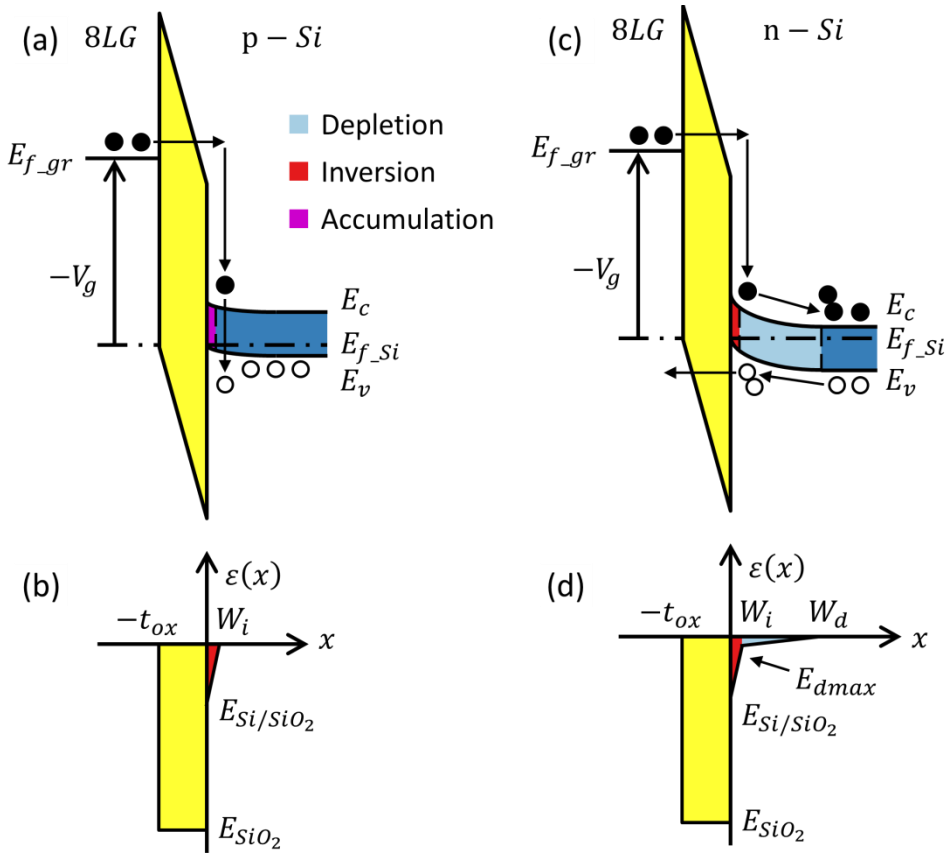

Figure 62 The band diagram and electric field distribution of the GOS devices shown in Figure 61 for (a) (b) p-Si substrate and (c) (d) n-Si substrate.

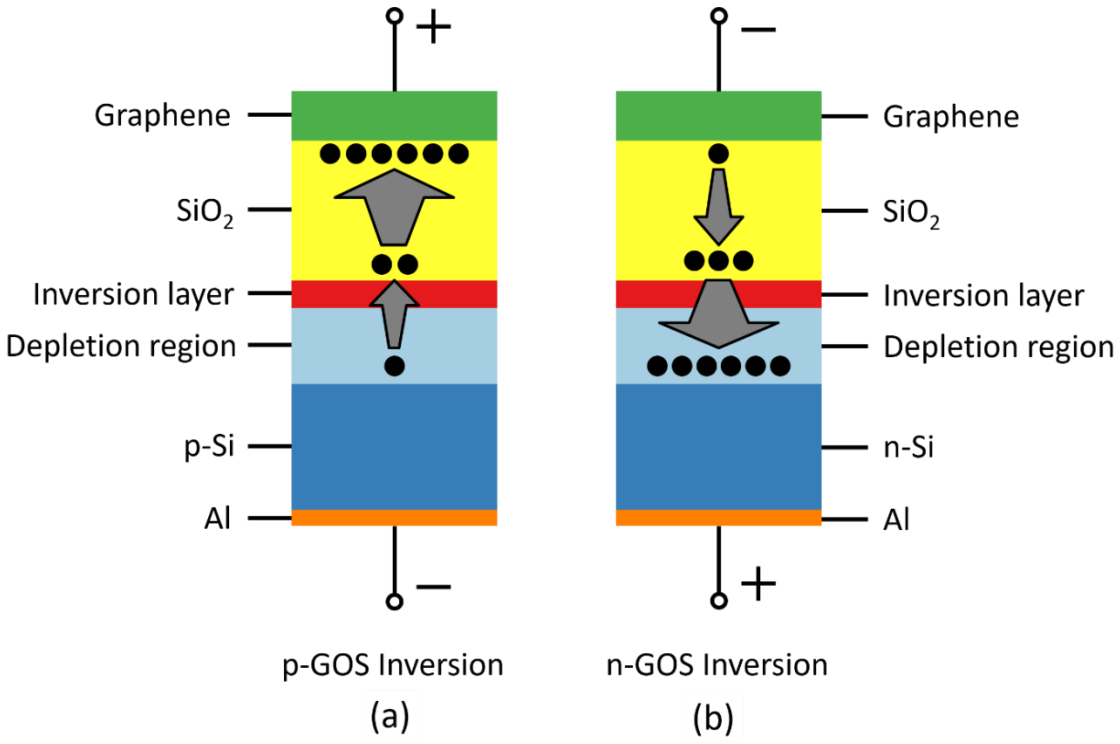

Figure 63 Graphene/SiO_2/Si under inversion bias, which means positive gate bias for p-Si substrate (a) and negative gate bias for n-Si substrate (b). The moving directions and multiplication process of electrons are indicated by black particles and arrows not to scale.

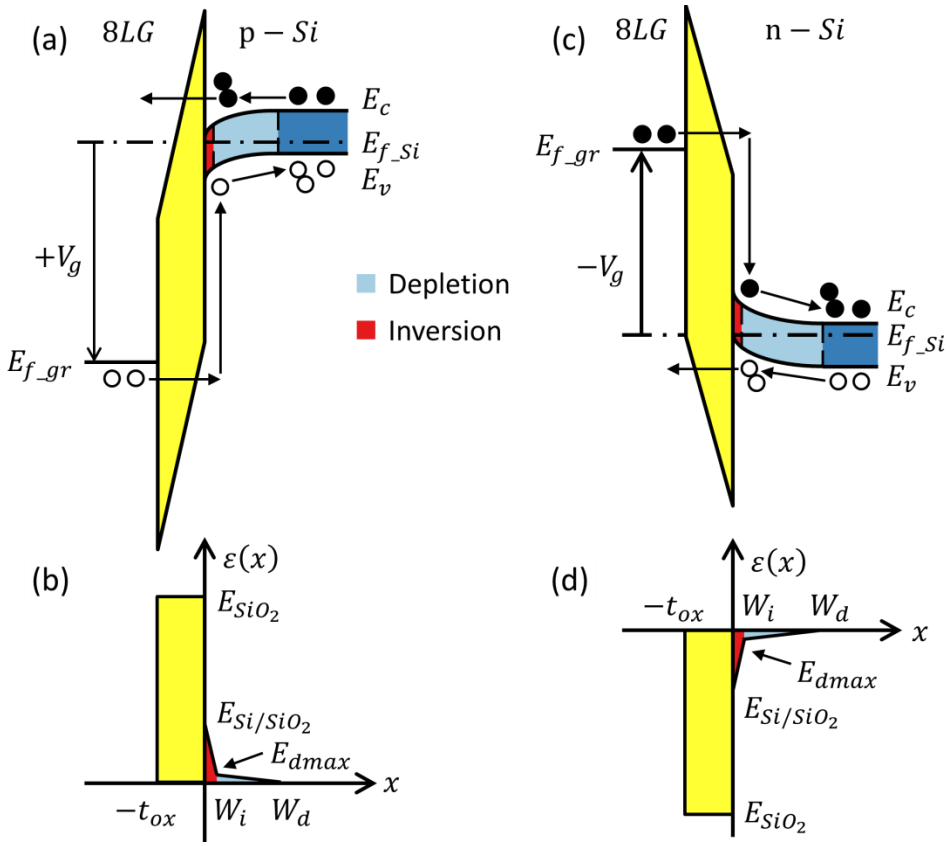

Figure 64 The band diagram and electric field distribution of the GOS devices shown in Figure 51 for (a) (b) p-Si substrate and (c) (d) n-Si substrate.

5.0 CONCLUSION

We present a chip-scale AES technique that operates at ambient temperature with low volume amount analytes and low voltage as a continued work of previous study [89] [90]. Analytes are placed on GOS substrate and are exploded by simply applying short voltage pulses.

The atomic spectra show major difference depending on the direction of the kinetic electron injection, which is controlled by the bias polarity of the pulses. When electrons impinge on the interface of graphene and oxide, atomic emission of analytes is strongly observed. However, the emission from silicon and oxide elements is dominant when electrons impinge at the interface of oxide and silicon. Emission intensity is enhanced in folded and wrinkled multilayer graphene area, because of better conductivity and more presence of analyte particles.

Supported by simulation and theoretical study, the impact ionization in silicon dioxide and silicon under high field is the primary reason for oxide breakdown which triggers atomic explosion. Experimentally, the analyte explosion is more easily triggered under inversion bias than accumulation bias because of the existence of depletion region. Carriers are accelerated and separated by strong electric field near the interface of silicon and oxide, providing sufficient electron energy required for impact ionization and multiplication in Si and SiO_2.

Post-AES surface morphology was characterized by SEM and AFM. Two different types of damages on the device surface are observed depending on the gate voltage polarity: widely spread meandering shallow destruction tracks and individual center-protruding deep destruction

sites. The high-quality interface between Si and SiO_2 with good compactness enables continuous propagation from one breakdown spot to adjacent defect site.

The depth and shape of destruction varies with the current density and electron migration direction. With electrons injected from graphene side into silicon, the impact ionization occurs in oxide first and then in the depletion region of silicon, creating destruction with depth of few hundred-nanometer. When electrons are injected from silicon to graphene side, impact ionization process would stop at the interface of oxide and graphene, resulting in shallow destruction with depth less than 50 nm. Center-protruding profile is formed by silicon ion migration upward under electrical field.

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