Radiation Hardening of Digital Color CMOS Camera-on-a-Chip Building Blocks for Multi-MGy Total Ionizing Dose Environments

Vincent Goiffon, Sébastien Rolando, Franck Corbière, Serena Rizzolo, Aziouz Chabane, Sylvain Girard, Jérémy Baer, Magali Estribeau, Pierre Magnan, Philippe Paillet, Marco Van Uffelen, Laura Mont Casellas, Robin Scott, Marc Gaillardin, Claude Marcandella, Olivier Marcelot and Timothé Allanche

***Abstract*—The Total Ionizing Dose (TID) hardness of digital color Camera-on-a-Chip (CoC) building blocks is explored in the Multi-MGy range using ^{60}Co gamma-ray irradiations. The performances of the following CoC subcomponents are studied: radiation hardened (RH) pixel and photodiode designs, RH readout chain, Color Filter Arrays (CFA) and column RH Analog-to-Digital Converters (ADC). Several radiation hardness improvements are reported (on the readout chain and on dark current). CFAs and ADCs degradations appear to be very weak at the maximum TID of 6 MGy(SiO_2), 600 Mrad. In the end, this study demonstrates the feasibility of a MGy rad-hard CMOS color digital camera-on-a-chip, illustrated by a color image captured after 6 MGy(SiO_2) with no obvious degradation. An original dark current reduction mechanism in irradiated CMOS Image Sensors is also reported and discussed.**

***Index Terms*—CMOS Image Sensors, CIS, Active Pixel Sensors, APS, Image Sensors, Radiation Hard, Rad Hard, Radiation Tolerant, Monolithic Active Pixel Sensor, MAPS, Ionizing Radiation, Total Ionizing Dose, TID, MGy, Grad, Gigarad, Dark Current, Quantum Efficiency, Enclosed Layout Transistors, ELT, Radiation Hardening, RHBD, Interface States, Trapped Charge, Shallow Trench Isolation (STI), Deep Submicron Process, DSM, CMOS,Integrated Circuit, Radiation Effects, Radiation Damage, X-rays, Gamma.**

I. Introduction

COLOR and miniature radiation hard cameras with multi-MGy hardness are a key solution for an increasing number of monitoring applications in highly radioactive environments (such as nuclear power plants, nuclear waste repositories and ITER fusion reactor). Beyond-Mrad-radiation-hardness is also becoming a requirement for the most challenging space imaging applications (e.g. Jupiter and its satellites). To build a compact multi-MGy rad-hard camera, one possibility is to integrate on a single CMOS radiation-hardened-by-design (RHBD) integrated circuit (IC) all the camera electronics. A simple digital color Camera-on-a-Chip [1] (CoC) with all the required functions for monitoring applications is presented in Fig. 1. The feasibility of such a MGy rad-hard digital color CoC has yet to be proven.

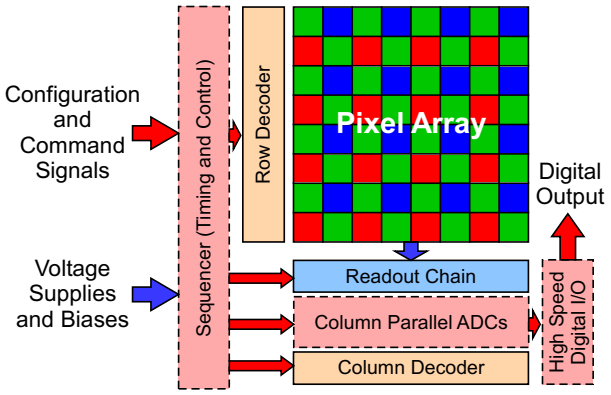


Figure 1. Basic digital color Camera-on-a-Chip architecture overview.

It has been recently demonstrated [2] that a 3.3 V CMOS image sensor (CIS) can absorb several MGy of Total Ionizing Dose (TID) without losing its ability to provide useful images. In particular, this work has shown that the required 1.8 V combinatorial logic functions (row and column decoders in Fig. 1) and 3.3 V analog circuits (pixels and readout chains) can be made Multi-MGy rad-hard. The radiation hardness of a RHBD CoC sequencer is expected to be sufficient for the targeted TID level thanks to the very good hardness of RHBD 1.8 V digital circuits demonstrated in [2]. Finally, as regards the remaining CoC functions presented in Fig. 1, there is no published quantitative result to date on the effect of TID on the transmission of CMOS Color Filter Arrays (CFA); nor on the radiation induced degradation in RHBD CIS column parallel Analog to Digital Converters (ADC).

The purpose of this work is to study the feasibility of a MGy rad-hard digital color CoC by exploring original mitigation techniques to improve the pixel performances achieved in [2]; and analyzing the effects of MGy TID on CIS color filter arrays and a basic CIS ADC architecture.

V. Goiffon, S. Rolando, F. Corbière, S. Rizzolo, A. Chabane, J. Baer, M. Estribeau, P. Magnan and O. Marcelot are with ISAE-SUPAERO, Université de Toulouse, Image Sensor Research Team, 10 avenue E. Belin, F-31055, Toulouse, France.

S. Girard and T. Allanche are with Université de Saint-Etienne, Laboratoire Hubert Curien, UMR-CNRS 5516, France.

P. Paillet, M. Gaillardin, and C. Marcandella are with CEA, DAM, DIF, F-91297 Arpajon, France.

M. Van Uffelen and L. Mont Casellas are with Fusion for Energy (F4E), c/Josep Pla, n° 2, Torres Diagonal Litoral, Ed. B3, 08019 Barcelona, Spain.

R. Scott is with Oxford Technologies Ltd.(OTL), 7 Nuffield Way, Abingdon OX14 1RL, UK.

Table I
1.8 V PIXEL DESIGN VARIATIONS OVERVIEW. PIXEL A AND E (IN BOLD) ARE STUDIED IN DETAIL IN THIS PAPER. PRESENTED OVERLAP DISTANCE D ARE DRAWN OVERLAP, NOT PHYSICAL OVERLAP.

Pixel	Photodiode isolation	Photodiode perimeter (µm)	Overlap d (µm)	MOSFET isolation	Additional capacitance
A	**P+**	**26.1**	**0.3**	**STI**	**No**
B	P+	23.7	0	STI	No
C	P+	7.6	0.3	STI	No
D	Gate	28.7	0.15	STI	No
E	**Gate**	**28.7**	**0.3**	**STI**	**No**
F	Gate	29.1	0.4	STI	No
G	Pwell	7.6	0.3	STI	Yes
H	Pwell	7.6	0.15	STI	No
I	Gate	29.7	0.3	Gate	No

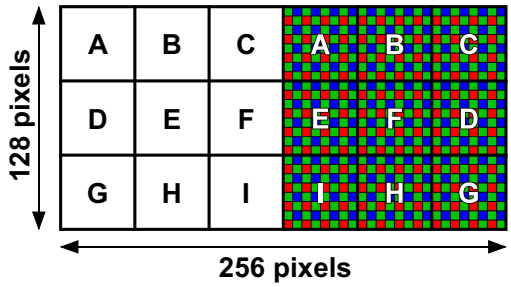


Figure 2. Studied 256×256-pixel-array organization overview. The right-hand part is covered by a CFA whereas the left hand part is not. Design rule constraints at the boundary of each pixel sub-array lead to a different pixel distribution in the color filter array part compared to the part without CFA.

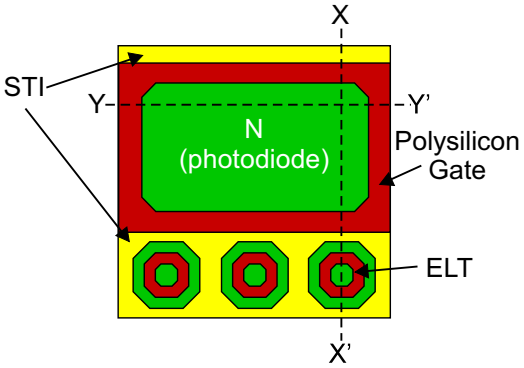
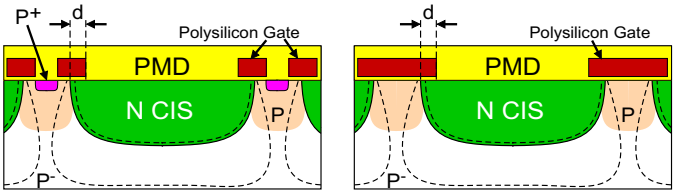


Figure 3. Top view illustration of the gate overlap pixel with gate isolation between pixels (i.e. pixels D, E and F). In pixels with a P+/Pwell isolation (A, B, C, G and H), the gate is interrupted between the pixels and a P+ or Pwell ring surrounds the gated photodiode. Pixel I layout is similar to the one illustrated here except that the photodiode gate also surrounds the ELTs to mitigate possible inter-device leakage inside the pixel.



(a) Gate overlap with P+ isolation

(b) Gate overlap with gate isolation

Figure 4. Cross sectional views of the studied photodiode layouts (along the Y-Y' axis shown in Fig. 3).

The targeted application for this research project is a video camera dedicated to monitor ITER remote handling operations [3] where the main threat is the TID induced by gamma irradiation (during remote handling maintenance operations, the plasma is not present and neutron generation becomes negligible). However, the single event effects (SEE) and the displacement damage constraints are also taken into account at the design and system levels to ensure a good tolerance in other type of radiation fields.

II. EXPERIMENTAL DETAILS

For this study, a CMOS IC has been designed and manufactured using a commercial grade CIS 180 nm process through a Multi-Project Wafer (MPW) access. The IC is constituted of an image sensor and an ADC test structure of which details are given hereafter. All the devices of this IC have been radiation-hardened-by-design by ISAE-SUPAERO except the I/O pads that come directly from the imec DARE UMC 180 nm platform.

A. Sensor design

Important radiation induced P-MOSFET threshold voltage shifts were reported in the 3.3 V analog parts of the sensors tested in [2] and two mitigation techniques have been proposed: to use a full 3.3 V N-MOSFET design or to use a full 1.8 V design. In this work we chose to investigate the second solution.

The studied CIS is a 10 μm-pitch-128×256-3T-pixel-array designed only with 1.8V enclosed layout transistors (ELT) [4], [5] to mitigate parasitic sidewall leakage current and radiation induced narrow channel effects (RINCE) [6]. The pixel array is divided into two 128×128 sub-arrays: one with a color filter array and the other without. Each 128×128 pixel area is subdivided into nine zones of 42×42 pixels with different features that are summarized in Tab. I. Their placement in the pixel array is described in Fig. 2 and Fig. 3 presents a top view illustrating the studied pixel layouts.

The gate overlap design appeared to be a promising solution to harden a CIS pixel for the MGy range but with some room for improvement, especially regarding dark current [2]. The use of simple gate oxide thickness (GO1) required by the 1.8V architecture is supposed to be a first way of reducing the radiation induced dark current. The two main pixel variants designed to possibly reduce the dark current are presented in Fig. 4: one using a P+ (or P-well) isolation between adjacent photodiodes (from adjacent pixels) and one using a gate isolation. This variation is used to analyze the role of P isolation between photodiodes in the radiation hardness. The other pixels simply differ by their gate-photodiode overlap distance or by their overall size (to modulate the perimeter dependent radiation induced dark current source) except pixel G which embeds an additional capacitance to increase its full well capacity (to minimize the magnitude of the radiation induced dark signal). Pixel I is a particular case where the transistors

are isolated from each other and from the photodiode by a polysilicon gate connected to the photodiode surrounding gate. The purpose of pixel I is to determine whether, in-pixel, inter-device-leakage has an influence on the observed degradation.

The accessible MPW manufacturing opportunity to test this image sensor design during the study timeframe offered a different photodiode doping profile than the one used in previous work. The photodiode N-doping profile is shallower than the one used in [2] and, according to basic simulation results, this particular N photodiode doping can not be implanted through the polysilicon gate (contrary to the photodiode studied in [2]). Hence, the manufactured overlap distance is not well controlled (at least not as well as originally planned) and analyzing the differences between pixel A and B or between D, E and F does not appear to be relevant with this photodiode doping profile (the measured results were similar). Hence, the optimization of the gate overlap distance, that was one of the original goal of this design, cannot be done properly with this shallow photo-detector.

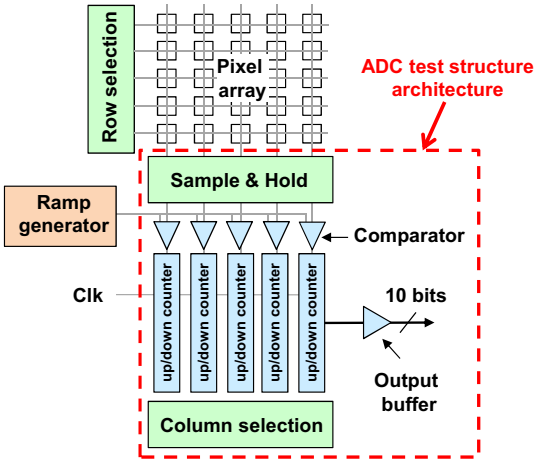


Figure 5. Column parallel ADC test structure architecture overview. All the sample and hold inputs are connected to a single analog input. The clock and the ramp generator are off-chip. The pixel array is presented here only for illustration, it is not connected to the ADC test structure in the studied device.

B. ADC test structure

In mass market CIS applications, analog to digital conversion is commonly performed with parallel column ADCs (one per column) [7] as illustrated in Fig. 1 and Fig. 5. This allows the device to maintain a reasonable conversion rate per ADC while supporting a high pixel rate. For this reason, CIS column ADCs can stay simple if the application is not too demanding in terms of signal-to-noise ratio and speed (which is the case here). Hence, we decided to target a 10-bit single slope ADC design for its simplicity and robustness. The studied ADC test structure is presented in Fig. 5 and it is constituted of 26 parallel ADCs, each of them being designed to fit in a 10 μm CIS column and to be operated at 25 k samples per second (required sampling rate per column for a 1000-row-imager with a 25 fps frame rate). They all share the same analog input. In this first test structure, the ramp and the clock are generated off-chip. ELTs cannot be used everywhere in an ADC design because of the inaccessible W/L ratios. Hence, wherever necessary, butterfly MOSFET layouts [8] have been used for N and P-MOSFETs (for RINCE mitigation). The analog part of the ADC is based on radiation hardened 3.3 V N and P-MOSFETs whereas the digital ADC circuitry is made of 1.8 V ELTs.

C. Irradiation conditions

For this intermediate exploration (the main purpose of this phase is to select the best design), the resources and investment required by multi-MGy ^{60}Co biased irradiations appeared to be too high and only grounded ^{60}Co expositions were considered. Indeed, in order to operate properly the CISs and ADCs in a gamma-ray environment up to several MGy, a MGy rad-hard test bench is required (it will not be the case for the final Camera-on-a-Chip IC which will not require any supporting electronics) and setting up such a bench in the selected facility also requires a significant amount of resources.

However, the previous study reported no significant difference between grounded and biased irradiations [2]. In order to remove any doubt about a possible important enhancement of the degradation induced by typical operating conditions, one sensor was exposed biased and sequenced (i.e. biased with nominal sequencing command signals) to 3 $\mathrm{MGy(SiO_2)}$ with 10 keV X-rays using an Aracor semiconductor irradiator at CEA, DAM, DIF.

Two ^{60}Co radiation test campaigns were performed at SCK-CEN Brigitte facility. For the first campaign, six CISs (two per TID) were exposed to 0.1 $\mathrm{MGy(SiO_2)}$, 1 $\mathrm{MGy(SiO_2)}$ and 3 $\mathrm{MGy(SiO_2)}$ and two ADCs to 1 $\mathrm{MGy(SiO_2)}$ with a dose rate of 17 kGy/h (Brigitte position B, temperature $= 42°\mathrm{C}$). During the second campaign, two CISs and two ADCs were exposed to 3 $\mathrm{MGy(SiO_2)}$ at 5 kGy/h while two CISs and two ADCs were irradiated up to 6 $\mathrm{MGy(SiO_2)}$ at 9 kGy/h (Brigitte position A, temperature $= 30°\mathrm{C}$).

In the following, the 10 keV X-rays biased irradiation results are presented only when a difference was observed with γ grounded irradiation. No noticeable difference was observed between the two ^{60}Co campaigns, so only the TID is indicated on the figures (not the specific ^{60}Co campaign).

III. Results and Discussions

A. Image Capture and Selection of Pixels to Study

Raw and color images captured before and after 6 $\mathrm{MGy(SiO_2)}$, 600 $\mathrm{Mrad(SiO_2)}$, are shown in Fig. 6 and Fig. 7. Whereas pixels A, B, D, E, F and I provide the expected image quality, very poor performances are achieved with the pixels based on a very small photodiode: pixels C, G and H. Indeed, these three pixel designs suffer from an intense diffusion cross-talk [9] leading to blurry images and to an overflow of uncollected photo-generated charges to the surrounding pixels (cause of the white border between pixels C, G, H and their neighbors). This very small size associated to a non-self-aligned radiation hardening technique (the use of a polysilicon gate) also leads to important pixel-to-pixel non-uniformity (visible in Fig. 6 and Fig. 7) and to very significant non linearities (not shown here). All these unwanted effects

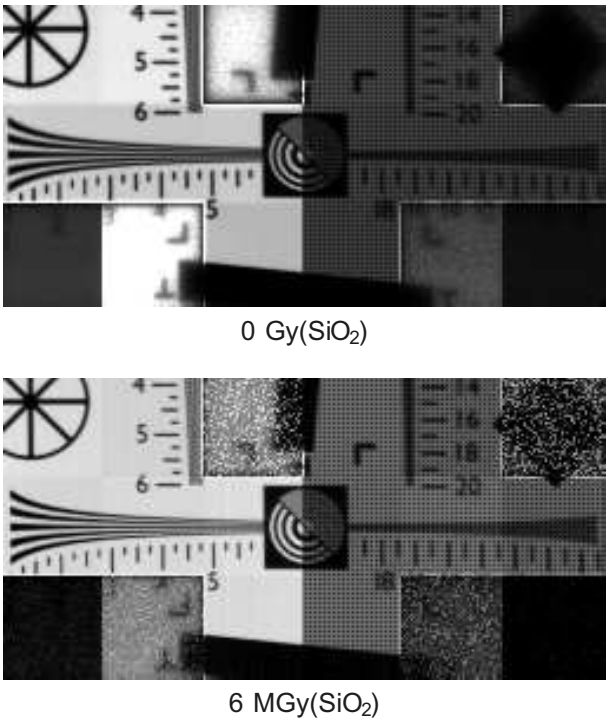


Figure 6. Raw image captured by the full 128x256 pixel array before and after 6 MGy(SiO_2), 600 Mrad(SiO_2), of TID with comparable illumination conditions. No image processing technique has been applied to enhance the image quality, especially no dark frame subtraction and no fixed pattern noise cancellation has been performed.

render it impossible to obtain reliable performance parameter values on these three pixel variations.

Because of the limitations induced by the available photodiode doping profile on this MPW discussed in sec. II-A, studying the difference between pixel A and B on one hand, and between pixel D, E and F on the other hand, appeared not to be relevant.

Therefore, only the results of pixel designs A and E (in bold in Tab. I) are presented in details in this paper. The main difference between these two pixels is the use of a P+ isolation in pixel A whereas pixel E is representative of the pixels with a gate isolation (see Fig. 4). They both exhibit a Charge-to-Voltage conversion Factor (CVF) of 10 $\mu V/e^-$. Pixel I results are not presented either because they are very close to pixel E results, even after irradiation. This demonstrates that inter-device leakage is not a limiting factor of the radiation hardness of CIS pixels. For sufficient positive gate voltages ($\approx$ 1 V), pixel I MOSFETs become short-circuited and the results start to differ between pixel I and E.

Concerning the radiation hardness of the designed sensor, Fig. 6 and Fig. 7 show no obvious degradation and they demonstrate the functionality of the studied image sensor (and all its sub-components) after the maximum TID, including the capability to discriminate colors.

The following sections analyze in more details the quantitative radiation induced degradation on each key parameters of the studied integrated circuits.

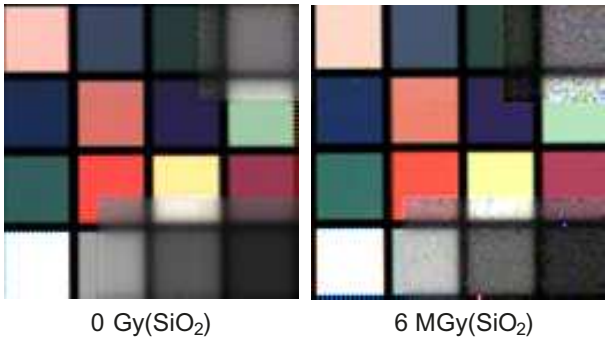


Figure 7. Color image captured before and after 6 MGy(SiO_2), 600 Mrad(SiO_2), of TID with the same illumination conditions. Color images can only be obtained on the sensor part that is covered by CFA. This 128×128-pixel-area covered by CFA corresponds to the right-half of the drawing in Fig. 2 and to the right-half of the raw images shown in Fig. 6. Only the most basic demosaicing method was used to render the color. The same processing was applied before and after irradiation.

B. Electrical Transfer Function

The quasi-static electrical transfer function (i.e. mean output of the readout chain as a function of an input voltage applied directly on the sense nodes of the whole array) of the 1.8 V CIS is presented in Fig. 8. Before irradiation, the 1.8 V readout chain exhibits a reasonable maximum output voltage swing of nearly 900 mV despite the use of low voltage MOSFETs (i.e. 1.8 V instead of 3.3 V). This has been made possible by making good use of the channel doping layers available in this technology to optimize the threshold voltages.

As in [2], P-MOSFET current source voltage bias had to be decreased to keep the same driving current in the output stage of the sensor. This voltage shift is presented in Fig. 9. The output P-MOSFET gate bias compensation directly shifts the sensor electrical transfer function toward higher voltage values (as shown in Fig. 8) leading to a reduction of the maximum output voltage swing for TID higher than 1 MGy(SiO_2). It indicates that even thin oxide (GO1) 1.8 V P-MOSFETs suffer from positive charge trapping[1] but with a much lower intensity than thick gate oxide (GO2) 3.3 V P-MOSFETs as illustrated in Fig. 9. Thanks to this radiation hardness improvement due to the use of (GO1) 1.8 V MOSFETs, no other degradation of the readout chain or of the digital circuit has been observed (contrary to [2] where several voltages biases had to be adjusted to ensure the functionality in the MGy range) providing a clear radiation hardness improvement compared to the previous sensor.

Fig. 9 also shows a comparison between the CIS irradiated grounded (γ-ray GND) and the one irradiated biased and sequenced (X-ray ON). Contrary to the previous study, a slight enhancement of the degradation can be observed when the sensor is biased during exposure. However, this difference is modest (about 20% additional degradation) and it confirms that grounded irradiations remain relevant for analyzing the

[1]It is still unclear why N-channel transistors do not suffer from this positive charge trapping degradation in the MGy range, contrary to P-MOSFETs. The recently proposed Radiation Induced Short Channel Effect (RISCE) [10] is a possible explanation but it is not likely in this technology node according to the I-V curve shifts reported in [11]

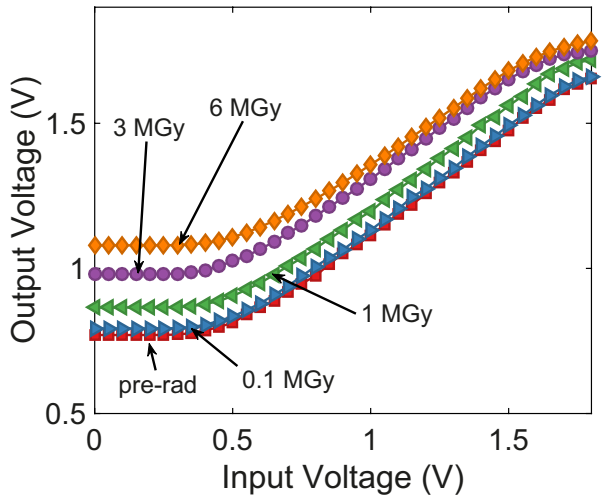


Figure 8. Quasi-static electrical transfer functions of the analog readout chain for several TID.

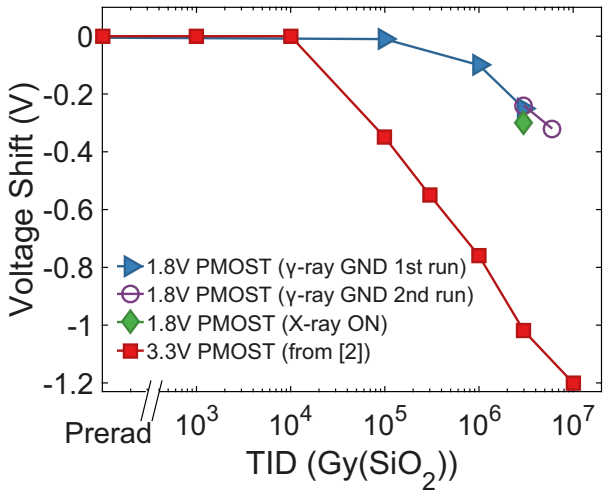


Figure 9. P-MOSFET current source voltage shifts with TID.

weaknesses of CMOS IC design in the MGy range (but not for an absolute radiation hardness evaluation or for a qualification test).

C. Opto-Electrical Transfer Function

The full opto-electrical transfer function of pixel E is presented before and after irradiation in Fig. 10. The typical radiation induced degradation can be recognized: a saturation voltage reduction (due to upward shift of the electrical transfer function characteristic shown in Fig. 8) and an increase in dark signal (higher output value for 0 photon fluence). After irradiation, two curves are presented, one with a negative gate voltage (accumulated gate) and one with a positive gate voltage (depleted gate). With the accumulated gate, the photodiode is well isolated from its surrounding environment and the transfer function exhibit a fairly linear behavior. If the gate is placed in the depletion regime, significant non-linearities appear in the photoresponse. They are probably due to a

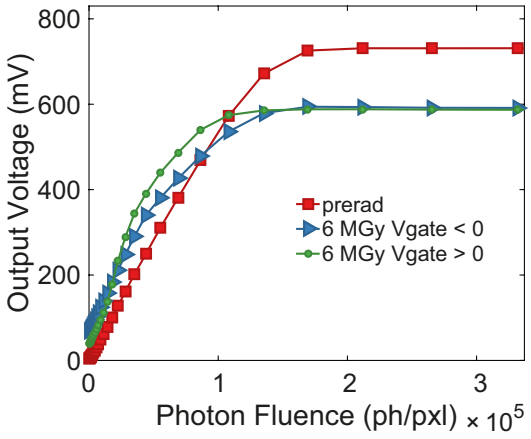


Figure 10. Opto-electrical transfer function of pixel E before irradiation and after 6 $\mathrm{MGy(SiO_2)}$, of $^{60}\mathrm{Co}$ grounded irradiation, at 650 nm.

change of photodiode capacitance induced by the variation of the depletion volume around the photodiode. Such non-linearities are unwanted but they are acceptable for monitoring application.

As regards the sensitivity, no obvious change of slope can be observed in the linear region, indicating that no important change of gain, CVF or quantum efficiency occurred (at least at 650 nm).

Further analyses of the dark signal and CFA transmission are provided in the following sections.

D. Dark Current

As in [2], the photodiode protecting gate voltage had to be optimized at each TID to provide the lowest possible dark current. Fig. 11 presents an example of dark current evolution with gate voltage (here after 0.1 MGy) of pixel A (gate overlap with P+ isolation) and pixel E (gate overlap with gate isolation between pixels) compared to the best value obtained at the same TID with the 3.3 V gate overlap design in [2]. The studied pixel A has the same design as the gate overlap pixel presented in [2] except that pixel A uses only GO1 thin gate oxides (whereas only GO2 gate oxides are used in the pixels in [2]). As discussed in sec. II-A, the photodiode doping profile is also different here due to manufacturing constraints.

This graph shows that for negative voltage values (hole accumulation regime below the gate), the type of isolation between pixels does not matter and both pixel designs are behaving the same. For positive voltages, the dark current rises for the pixel with a P+ isolation (pixel A) first because of the extension of the depletion region along the oxide interface. Then, when an inversion channel is created below the protecting gate, a high electric field junction is created between the inversion channel and the P+ isolation ring, leading to an intense tunneling current.

For gate isolated pixel (pixel E), after the optimum regime exhibited by pixel A, the dark current continues to drop with increasing gate voltage. This decrease allows gaining one or even two orders of magnitude of dark current reduction. It represents a huge improvement that could lead to almost no

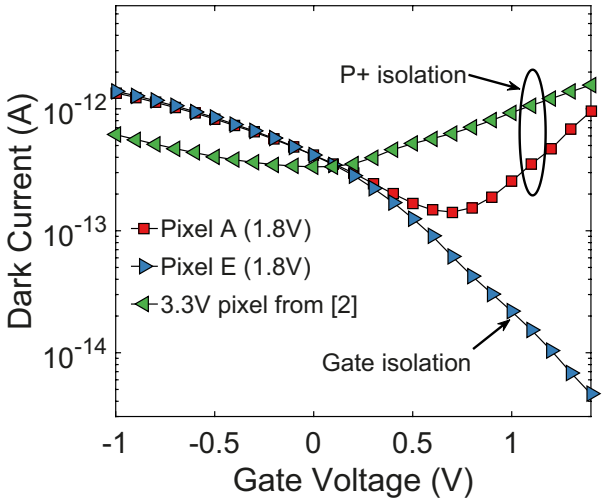


Figure 11. Dark Current as a function of gate bias at 0.1 MGy(SiO_2) for pixels A and E compared to the lowest value obtained at the same TID in [2]. Temperature = 22°C.

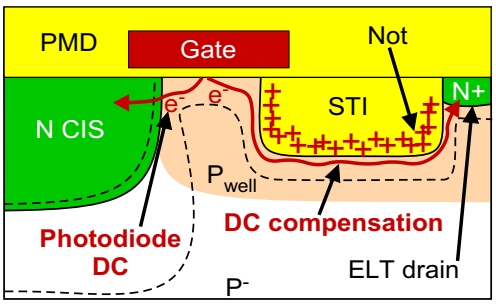


Figure 12. Illustration of the current sharing mechanism hypothesis in gate isolation pixels (cross-section along the X-X' axis shown in Fig. 3). Most of the thermally generated dark electron at the gate oxide interface diffuse toward the VDD N+ contact through the STI weak inversion layer (as in a classical MOSFET in sub-threshold regime). Most of the useful photo-signal is not influenced by this current compensation mechanism because the P-well prevents the photogenerated carriers to be collected by the STI depletion region. Not stands for radiation induced positive trapped charge and DC stands for Dark Current.

radiation induced dark current increase after 0.1 MGy. Gate oxide tunneling is not likely to be the cause of this dark current compensation because the minimum gate voltage at which the phenomenon starts to occur (around 0.4 V) is well below the photodiode voltage after reset (around 1.5 V), and thus if tunneling was influencing dark current, it should enhance it (by further discharging the photodiode). This will be confirmed by future measurements of gate leakage current. There are at least two other possible explanations for this phenomenon which are discussed hereafter.

(1) It is well known that the leakage current of a gated diode is significantly reduced when the strong inversion point condition is reached [12] because the inversion channel puts the Si-SiO_2 interface under equilibrium conditions and stops the thermal generation of electron-hole pairs. This could explain why for sufficiently positive voltages the dark current is reduced. However the inversion threshold is expected for a gate-to-source voltage (i.e. gate-to-diode voltage) larger

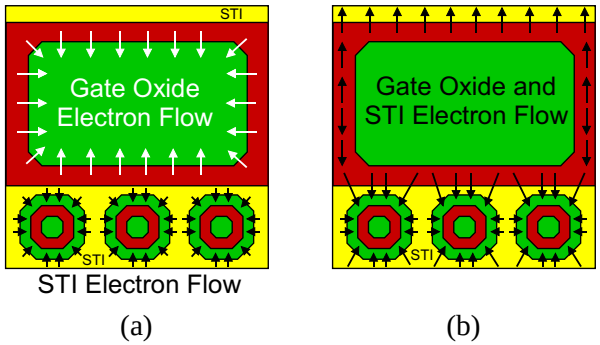


Figure 13. Top view illustration of the possible current sharing mechanism in a pixel with gate isolation. a) When the photodiode gate is accumulated, all the electrons thermally generated at the small depleted gate oxide area are collected by the photodiode. In the meantime, the free electrons thermally generated at the STI interface are collected by the ELT drains biased to VDD. b) When the photodiode gate is depleted, most of the electrons generated at the gate oxide depleted interface join the flow of STI electrons to be collected by the ELT drains (biased at a higher voltage than the photodiode). This mechanism does not occur in pixels with a P+ isolation since the P+ ring is preventing the electrons to flow from the photodiode gate to the ELT drains. In this case, all the generated dark electrons are collected by the photodiode (and not anymore by the ELT drains) leading to an intense dark current.

than the MOS structure threshold voltage (including body effect). According to Fig. 8, the typical photodiode voltage in the operating range is 0.5-1.5 V (and mainly near 1.5 V during dark current measurements) which means that this phenomenon cannot occur for gate potentials below +0.5 V and that the inversion threshold for the gated photodiode is probably well beyond 1 V. Moreover, in classical gated diode structure, the transition from the weak to strong inversion is very sharp whereas in Fig. 11 it is pretty smooth.

(2) The second hypothesis is a sharing mechanism of thermally generated dark current between the photodiode and the pixel N+ junctions connected to V_{DD} through merged depletion regions (as illustrated in Fig. 12 and Fig. 13). Indeed, beyond 10 kGy (1 Mrad) all the Shallow Trench Isolation (STI) interfaces are most likely in weak inversion [13] (or possibly even in strong inversion at the highest TID, but it would not change the principle), i.e. depleted, because of the radiation induced positive trapped charge. These inversion channels are connected to the external ELT terminals biased to V_{DD}. In this case, in the absence of photodiode inside the pixel, all the thermally generated parasitic charge at the STI interface would be drained by the V_{DD} N+ regions. With the photodiode and its positively biased protecting gate, the photodiode depletion region merges with the STI depleted surrounding volume and some of the dark charges generated below the photodiode protecting gate diffuse toward the V_{DD} N+ regions (through the STI depletion region). In this case, this dark current collected by the V_{DD} N+ regions is not integrated by the photodiode leading to an apparent dark current reduction. The higher the gate voltage, the more efficient is the dark current compensation since the connection to STI weak inversion regions is improved. This phenomenon does not lead to a sensitivity reduction because the photodiode itself is not directly connected to the STI inversion region (at least for reasonable positive gate voltages). Only the thermally

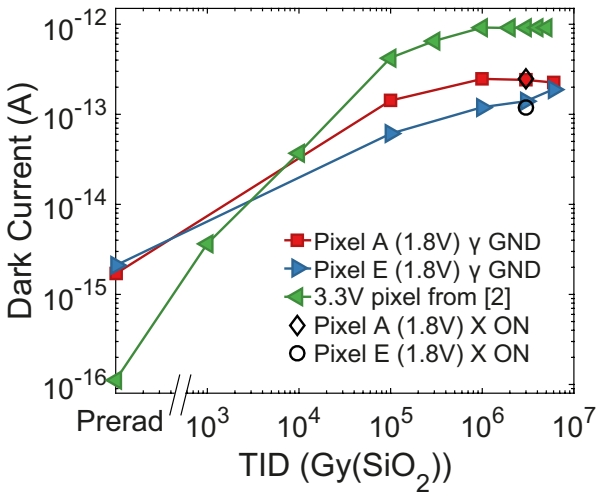


Figure 14. Mean dark current versus Total Ionizing Dose (TID) with optimum gate bias (< 700 mV) for pixel A and E compared to the results obtained with the 3.3 V Gate Overlap design of [2]. Temperature = 22°C.

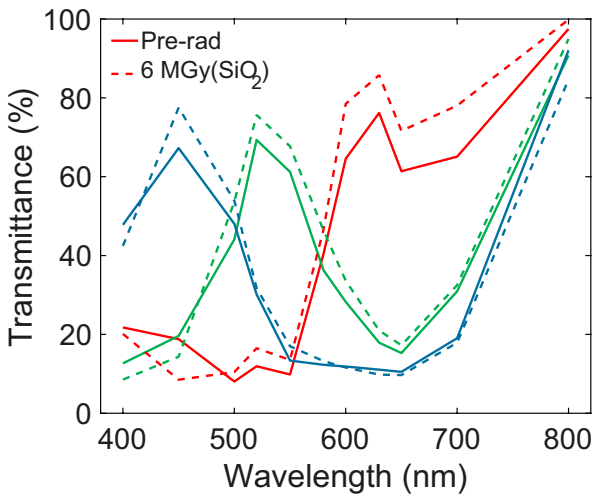


Figure 15. Color filter array transmittance of an unirradiated sensor and a sensor exposed to 6 $\mathrm{MGy(SiO_2)}$.

generated electrons below the gate are influenced by the STIs, not the main part of the photo-carriers that follow the electric field lines in the depleted volume of the photodiode. Such hypothetical explanation is in good agreement with the fact that this dark current drop at high gate voltage was not observed before irradiation (when the STI interfaces were not depleted/inverted).

To determine the exact nature of this dark current reduction mechanism (very efficient between 0.1 MGy and 1 MGy, but inefficient below and much less efficient beyond as illustrated in Fig. 14 by the difference between pixel A and E dark currents), one would need to study further what happens at higher gate voltages. Unfortunately, for gate voltage higher than 0.7 V, the pixels in the I region start to be short-circuited (because pixel I MOSFETs are isolated by the same polysilicon gate as the one used for the photodiodes as presented in Tab. I) and the overall pixel array performance begin to be significantly degraded for higher gate voltages ($> 1 - 1.5$ V). As a consequence, the confirmation of the previous hypothesis will be the subject of future work. If this is confirmed, this dark current reduction mechanism could possibly be enabled on purpose (i.e. by design) and be controlled to improve the sensor performances with limited unwanted effects.

It should be emphasized that using a positive gate voltage does not only present benefits for pixel E, it also has a limitation, it creates some non-linearities (see Fig. 10) as discussed in the previous section.

Because of this limitation, a safe margin has been considered to analyze the behavior of gate isolated pixels, and dark current values achieved with gate voltages higher than 0.7 V are excluded in the following.

A comparison between pixel A, E and the best 3.3 V pixel of [2] is presented in Fig. 14. For pixel A and E the lowest dark current value measured at each TID is presented (for gate voltage below 0.7 V to limit the influence of the short-circuit in pixel I sub-array as discussed in the previous paragraph). It shows that the pre-rad dark current is higher in the 1.8 V designs than in the 3.3 V one. This is most likely due to the different photodiode doping profile used in this MPW, but it can also be due to high pre-rad leakage of the 1.8 V RST ELT source that could possibly hide, before irradiation, the lower photodiode dark current. As discussed before, using a positive bias before irradiation does not reduce the dark current on pixel E, most likely because the STI are not yet in weak inversion. This is illustrated by the fact that pixel E dark current cannot be lowered below pixel A dark current in Fig. 14, contrary to what happens after irradiation.

After irradiation, the new 1.8 V designs bring an important improvement on the whole range if the gate voltage is carefully selected by reducing effectively the radiation induced dark current (between 5 and 10 times less dark current than the 3.3 V design). At 6 $\mathrm{MGy(SiO_2)}$, the gate voltage influence on dark current magnitude weakens and it becomes difficult to reduce the dark current by using positive gate voltage (below 0.7 V, but going further leads to further reduction). For this reason, pixel E dark current rises between 3 $\mathrm{MGy(SiO_2)}$ and 6 $\mathrm{MGy(SiO_2)}$ whereas the other pixel dark current curves saturate. It is interesting to notice that the dark current saturation regime seems to start in the same TID range (between 0.5 and 1 $\mathrm{MGy(SiO_2)}$) for both 1.8 V and 3.3 V sensors and that this range correspond to the saturation point reported in [14], [15] on different CMOS processes. A saturation of interface state density is probably the cause of this dark current saturation [2].

The final observation that can be made in Fig. 14 is the absence of obvious influence of biasing conditions during irradiation on the dark current as observed in previous studies.

E. Color Filter Array

For a compact color rad-hard camera, the use of red, green and blue color filters deposited on top of each pixel is mandatory (other solutions for color imaging lead to much bigger systems). Nevertheless, there is simply no published measurement about the behavior of CIS CFA under gamma-ray radiation and especially in the MGy range for which radiation

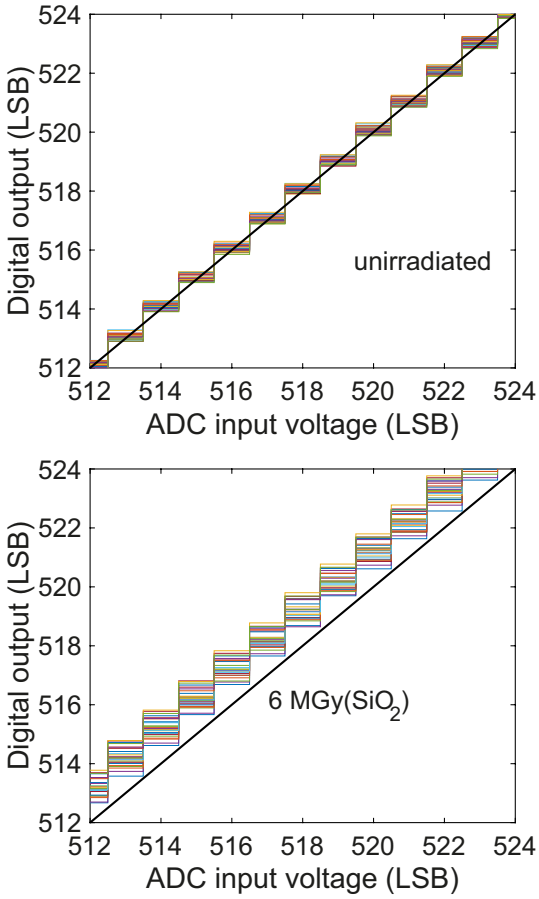


Figure 16. Transfer function of an unirradiated ADC test structure (top) and another one exposed to 6 $\mathrm{MGy(SiO_2)}$ (bottom) presented in the middle of the input range (codes 512 to 524). The response of the 26 column parallel ADCs are presented in this figure.

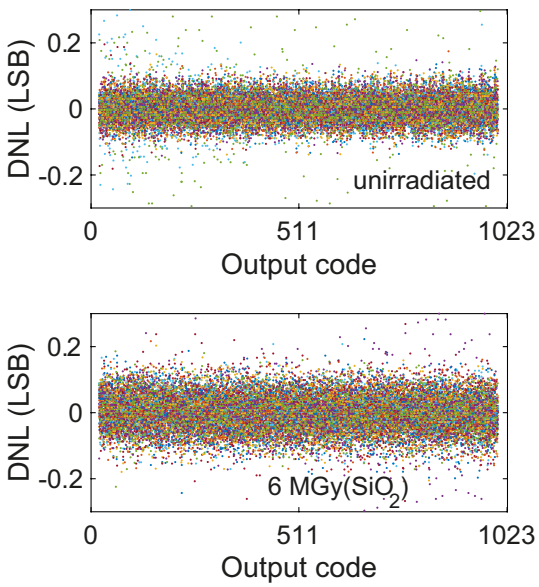


Figure 17. ADC test structure differential non-linearity (DNL) of an unirradiated IC (top) and an IC exposed to 6 $\mathrm{MGy(SiO_2)}$ (bottom). The response of the 26 column parallel ADCs are presented in this figure. First and last 20 codes are removed for the processing to cancel some edge effects due to the characterization technique.

test results are very rare in literature. To validate that a color CoC based on the use of CFA can still discriminate these three colors after the absorption of several MGy, the photo-response of the pixels from the sub-arrays with CFA has been directly compared to the photo-response of the same pixels in the sensor region without CFA. This direct ratio provides the transmittance spectrum shown in Fig. 15. This original measurement demonstrates clearly that MGy irradiations do not cause any particular issue for the use of CFA (at least up to 6 $\mathrm{MGy(SiO_2)}$). In other words, thanks to the very small thickness (typically below 1 μm) of the deposited color filters, color center generation or bleaching is not visible (but may possibly occur). The apparent slight increase in transmission after 6 $\mathrm{MGy(SiO_2)}$ is within measurement uncertainties (mainly due to small non-linearities induced by irradiation, as discussed previously). The good stability of color filter transmittance after irradiation is also confirmed by the color images presented in Fig. 7.

F. Column RHBD-ADC

Despite the fact that several CIS with integrated column parallel ADCs (non radiation-hardened) have been TID tested in the past (see for example [16]–[18]) at TID below 1 $\mathrm{kGy(SiO_2)}$, typical ADC performance figures of merit (such as differential non-linearity (DNL) and integral non-linearity (INL) [19]) have never been reported for irradiated CIS column parallel ADCs. Hence, before the presented study, there was no available information in literature to anticipate the behavior of CIS RHBD column parallel ADCs in the MGy range.

The static performance parameters (i.e. transfer function, DNL and INL) of the radiation hardened ADCs are presented before and after irradiation in Fig. 16, Fig. 17 and Fig. 18. Since this ADC design is partially based on 3.3 V P-MOSFET, the P current source bias voltage had to be decreased by about 1 V after 6 $\mathrm{MGy(SiO_2)}$ to compensate for the radiation induced positive trapped charge in the P-MOSFET gate oxide (as discussed in [2]). In the final design, auto-bias circuits will be used to avoid having to manually adjust the P-MOSFET bias voltage.

Compared to the studied CIS, the column ADC test structures integrate two new building blocks: an analog differential comparator and a digital up and down counter (which includes D flip-flops) as shown in Fig. 5. For this first exploration test structure, the clock and the ramp generation are performed off-chip.

After 6 $\mathrm{MGy(SiO_2)}$, TID has a slight effect on the DNL but it clearly degrades the INL, although this remains within an acceptable range for the application (+/- 2 LSB), especially when this non-linearity is compared to the intrinsic non-linearity of the analog pixel (much larger than 2 LSB). So it can be concluded from these first measurements that the selected simple ADC architecture, based on a combination of butterfly and ELT designs, allows us to maintain good column ADC performance after 6 $\mathrm{MGy(SiO_2)}$ of grounded

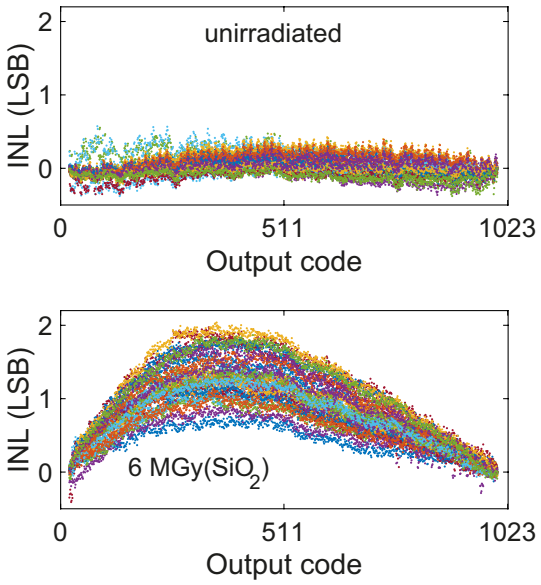


Figure 18. ADC test structure integral non-linearity (INL) of an unirradiated IC (top) and an IC exposed to 6 $\mathrm{MGy(SiO_2)}$ (bottom). The response of the 26 column parallel ADCs are presented in this figure. First and last 20 codes are removed for the processing to cancel some edge effects due to the characterization technique.

irradiation. These results will have to be confirmed with biased irradiations and the next phase will consist in adding the internal ramp generator.

IV. Summary and Conclusions

In this work the feasibility of a MGy rad-hard CMOS color digital camera-on-a-chip has been demonstrated. It will serve as a basis for the development of a full size camera including a rad-hard optics and a rad-hard illumination system (which are also currently developed in the frame of the same project). Several significant CIS radiation hardness improvements were presented by investigating some of the mitigation techniques proposed previously: a factor of 5 reduction in readout chain voltage shift, between 5 and 10 times dark current lowering after irradiation (up to 6 $\mathrm{MGy(SiO_2)}$) and the complete mitigation of all the other parasitic circuit effects reported in [2]. Additionally, the evaluation of the TID effects on CIS color filter arrays and simple column parallel single slope RHBD ADCs (with external ramp generation) has been reported in the MGy range. CFA were not degraded by the TID whereas the ADC test structure was clearly influenced by the exposure to ionizing radiation but the observed variations remain acceptable for the targeted application.

Future work will focus on exploring another mitigation approach: using a full N-MOSFET (3.3 V) based design for the pixel array (as proposed in [2]) and comparing the results to the full 1.8 V design studied here. Biased γ-ray irradiations and further development of the on-chip ADC are also targeted in the near future, to enhance the CoC performance under radiation and to establish an appropriate qualification procedure. Concerning dark current, the gate overlap optimization will be studied in an ensuing deep photodiode manufacturing opportunity, and the dark current reduction mechanism with positive gate bias reported here will also be studied in a more appropriate sensor (or test structure) with less limitation on the maximum gate voltage.

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