III-V Semiconductor Nanowire for Solid Oxide Fuel Cells

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Abstract

Solid oxide fuel cells (SOFC) have much promise as efficient devices for the direct conversion of the energy stored in chemical fuels into electricity. The development of highly robust SOFC that can operate on a range of fuels, however, requires improvement in the electrodes, especially the anode, where nanoscale engineering of the structure is required in order to maximize the number of sites where the electrochemical reactions take place. In this article, we briefly explained the growth of III-V semiconductor nanowire layer on GaAs substrate as an anode electrodes using metal organic chemical organic vapor deposition (MOCVD). Field-emission scanning electron microscopy (FE-SEM), transmission electron microscopy (TEM) and conductivity atomic force microscopy (CAFM) analysis were carried out to investigate the structural properties and current-voltage changes in the wires. Results show that the III-V nanowires grow with less defect structure, uniform in composition and diameters with optimal growth parameters. The current-voltage measurement showed similar to that of a p-n junction characteristic which is suitable in the SOFC application.

Keywords: Solid oxide fuel cell; MOCVD; III-V Semiconductor; Nanowire; VLS Technique

1.0 INTRODUCTION

Fuel cells are electrochemical reactors in which the energy contained in the chemical bonds within a fuel is converted directly into electrical energy. Fuel cells are inherently more efficient than most other methods of extracting energy from fuels and there has been much recent interest in the development of fuel cells as a more environmentally friendly energy conversion technology. From the multiple types of fuel cells, solid oxide fuel cells (SOFC) is one of the most attention received in recent years.[1-3] SOFC use of oxygen ion (O^{2-}) conducting ceramic membrane as the electrolyte. While they also can be powered using hydrogen they are inherently more fuel flexible and can in principle be powered by any combustible fuel including natural gas, liquid hydrocarbon and even solids derived from coal or biomass.[4] This fuel flexibility has led to SOFC being considered for a variety of distributed power applications. While the fuel flexibility of SOFC is one of their advantages, achieving robust system that can operate on a range of fuels for long periods requires nanoscale control of electrode structures and careful choice of the materials that are used in the anode where fuel combustion occurs.[5]

The emergence of nanotechnology in recent decades has given a great deal of new insight into theories previously widely assumed by the scientific community. This has resulted in industry showing considerable interest in nanostructured materials.[6] The use of nanomaterials has typically been restricted to low temperature devices, however advances in solid oxide fuel cells (SOFC) such as lowering operating temperatures allow new possibilities for their application.[7] The most advantageous

property of nanomaterials for SOFC application is their high surface area to volume ratio, which results in the increase of the active electrode area making them suited to adsorption and catalysis applications. Another significant advantange of nanomaterials is their ability to change their fundamental properties such as structural, optical properties, melting temperature and conductivity.[8] Some of these properties are directly related to surface interaction between nanoparticles but the electronic properties are controlled by quantum confinement effects. This effect does not come into play when moving from micro to macro dimensions but becomes dominant when the nanometer size range is reached. III-V materials exhibit many interesting electrical and optical properties due to their higher mobility carrier and that make them very good candidates for nanowire applications in several fields.[9-11] In the production of semiconductor nanowires that meet the criteria of an electronic device, epitaxial growth of nanowires need to be highlighted. The tiny, wire-shape structures with diameter less than 100 nanometers and length greater than 1 micron are effectively nanowires. The other requirement for the future advanced industrial application of nanowire materials are straight, uniform in compositional and uniform in diameters. In this article, we briefly explained the growth of III-V semiconductor nanowire layer on GaAs substrate as an anode electrodes using metal organic chemical organic vapor deposition (MOCVD). Field-emission scanning electron microscopy (FE-SEM), transmission electron microscopy (TEM) and conductivity atomic force microscopy (CAFM) analysis were carried out to investigate the structural properties and current-voltage changes in the wires.

2.0 EXPERIMENTAL

The experiment starts with semi insulating undoped GaAs substrates immersed in 0.1% poly-L-lysine (PLL) solution for 3 mins. After cleaning with deionize water and subsequent drying with N_2 , the 30 nm diameter gold colloids were dispersed on the substrate surface and immediately washed after 20 sec. Due to the positive charge on the surface of the PLL layer, they attract the negative charged of the gold colloids. Nanowires were grown by vertical flow MOCVD at a pressure of 76 Torr. Trimethylgallium (TMGa) and arsine (AsH_3; 10% in H_2) were used as the gases source and V/III ratio was set at 166. The substrate was annealed in situ at 600^{o}C under AsH_3 ambient for 10 min to desorbed surface contaminants and form eutectic alloy between Ga and gold colloid (Au). After annealing, the temperature was ramped down to the desired growth temperature range between 380^{o}C to 600^{o}C. TMGa was introduced to initiate nanowires growth. The nanowires growth time was kept constant for 30 min. All the grown samples were analyzed using field emission scanning electron microscope (FESEM), transmission electron microscopy (TEM) and energy dispersive X-Ray (EDX).

FE-SEM system was performed using a JEOL JSM-6701F operating at an acceleration voltage of 15 kV for one nm high resolution and 1 kV for 2.2 nm with the maximum 2nA probe current. TEM and HRTEM equipment system (JEM-2100) was operated at 200kV. Sample for TEM analysis is placed on a 3mm diameter Cu with 300 micromesh grid. The mesh number of a grid indicates the number of grid openings per linear inch. The smaller the grid number, the larger the hole size and the greater the ratio of open area to covered. The grid is coated with a support film that holds the sample in place. The film must be as transparent as possible to provide support for the sample. The substrate wafer was cut into small sizes and put in the sample bottle which contains acetone for NW extraction. It was then, sonicated in the Delta DC 150H Ultrasonic cleaner for 30 mins at 25^{o}C. The microlittre pipette was used to pick-up the acetones which contain NWs and dispersed them onto a carbon copper grid. The Scanning Probe Microscopy SPA 300HV with conductivity AFM probe was used for the electrical measurement studies. It operates in the contact mode under an ambient with a relative humidity of about 60% at 18^{o}C. The current was measured when electrical contact between the AFM tip and a tip of one of the GaAs NWs was formed.

3.0 RESULTS AND DISCUSSION

Figure 1 shows the microscopy electron images of GaAs NWs grown with three different V/III ratio. Figure 1 (a), (c) and (e) are FE-SEM images for the V/III ratio of 17, 166 dan 297 respectively, whereas Figure 1 (b), (d) dan (f) are TEM/HRTEM images for the corresponding V/III ratio. FE-SEM image describes the NW morphology, while TEM identify the structure of the NWs. Insets of Figure 1 (a), (c) and (e) depict the topview of GaAs NWs with the base NW clearly changed from cylindrical to hexagonal shape when the V/III ratio is increased. The tapered the NWs reflect the higher value of V/III ratio. Inset in TEM images is magnified of NW structure which consists of bright and dark stripes. Figure 2 shows the I-V characteristic of GaAs NW which were grown at V/III ratio of 17 (a), 166 (b) and 297(c). The direct current voltage supplied for the NW sample between the tip and the substrate is in the range of -5.0 to 5.0 Volt.

GaAs NWs were grown epitaxially underneath the droplet of Au particle through the Vapor-Liquid-Solid process when TMGa and AsH_3 are supplied. GaAs NWs grown with low V/III ratio produced few broken wires and not perpendicular to the substrate surface. This condition is caused by insufficient As or spill of Ga adatoms due to the incomplete decomposition of AsH_3 at low V/III ratio. It is possible that, with AsH_3 as the limiting reactant, the Ga content within each nanoparticle is significant. Because Ga has a lower surface tension than gold (γ_{Ga} = 0.72 J m^{-2} and γ_{Au} = 1.14 J m^{-2}),[12] a high Ga content is expected to lower the liquid-vapour surface tension and thereby increase the work of adhesion as reported by Roper.[13] When the work of adhesion is higher, a small perturbation such as gas flow may be sufficient to displace the catalyst from the NW tip, allowing kinking. With increasing V/III ratio to 166 and up to 297, the activation energy for two-dimensional planar growth is increased and will increases the growth rate that will caused the tapering of NWs especially at the base part. This situation occurs because the Ga adatoms, diffusing from the substrate and along the NW sidewalls towards the growing Au-capped NW tip, are consumed by this radial growth. These Ga adatoms would otherwise diffuse to the NW tip and contribute to axial growth. In short, radial growth competes with axial growth for these Ga adatoms. Therefore, with increasing V/III ratio, the increase in radial growth rate produces a decrease in axial growth rate and also the base will seem wider than the tip. This is consistent with previous reports by Dayeh [14] and Paiman [15] of growing InAs and InP NWs respectively. Hannah [16] and Soci [17] also found the same phenomenon in the growth of GaAs NWs using MOCVD horizontal reactor, which is radial growth rate increases with V/III ratio and results in more tapered NWs. Overall, the densities of NW growth at all three ratios are almost the same and not much difference except for lowest V/III ratio (17). This is because the lack of NW due to partly broken and lying on the substrate caused by factors described above.

TEM images in Figure 1 (b), (d) and (f) describes the crystal structure of a GaAs NW grown at V/III ratio 17, 166 and 297 respectively. Enlarged HRTEM images are shown in the insets to further confirm the crystal structure. The changes in crystal structure are shown by the density change of dark and bright regions. These suggest that a [111] rotational twins which cause the dark and bright regions of these stripes in TEM images (Figure 1 (d) and (f)), contribute to the mechanism of crystal structure change. The lowest V/III ratio (17) (Figure 1(b)), shows a zincblende (ZB) structure with no obvious planar defects. With increasing V/III ratio, the density of planar defects (such as twins and/or stacking faults) increases significantly. These planar defects create wurtzite (WZ) insertions in the ZB phase (and vice versa), as observed previously for almost all type III-V semiconductor NWs. [11,15,18] At V/III ratio of 297 (Figure 1(f)), the crystal structure is mainly (about 90%) WZ. It is expected that changes in V/III ratio must have affected the interfacial energy at the growth front and nucleation kinetics, resulting in this alternation of the crystal structures. Additionally, it has been proposed that a high V/III ratio can rapidly quench the growth, causing crystallisation in a WZ phase as found out by Dick.[19] ZB and WZ are based on face-centered cubic and hexagonal closed packed respectively, so both types are maximally

packed and the potential energy in the formers (111) planes and the latter's (001) planes are very close to each other. So they can easily form a stable combination under NW growth conditions.

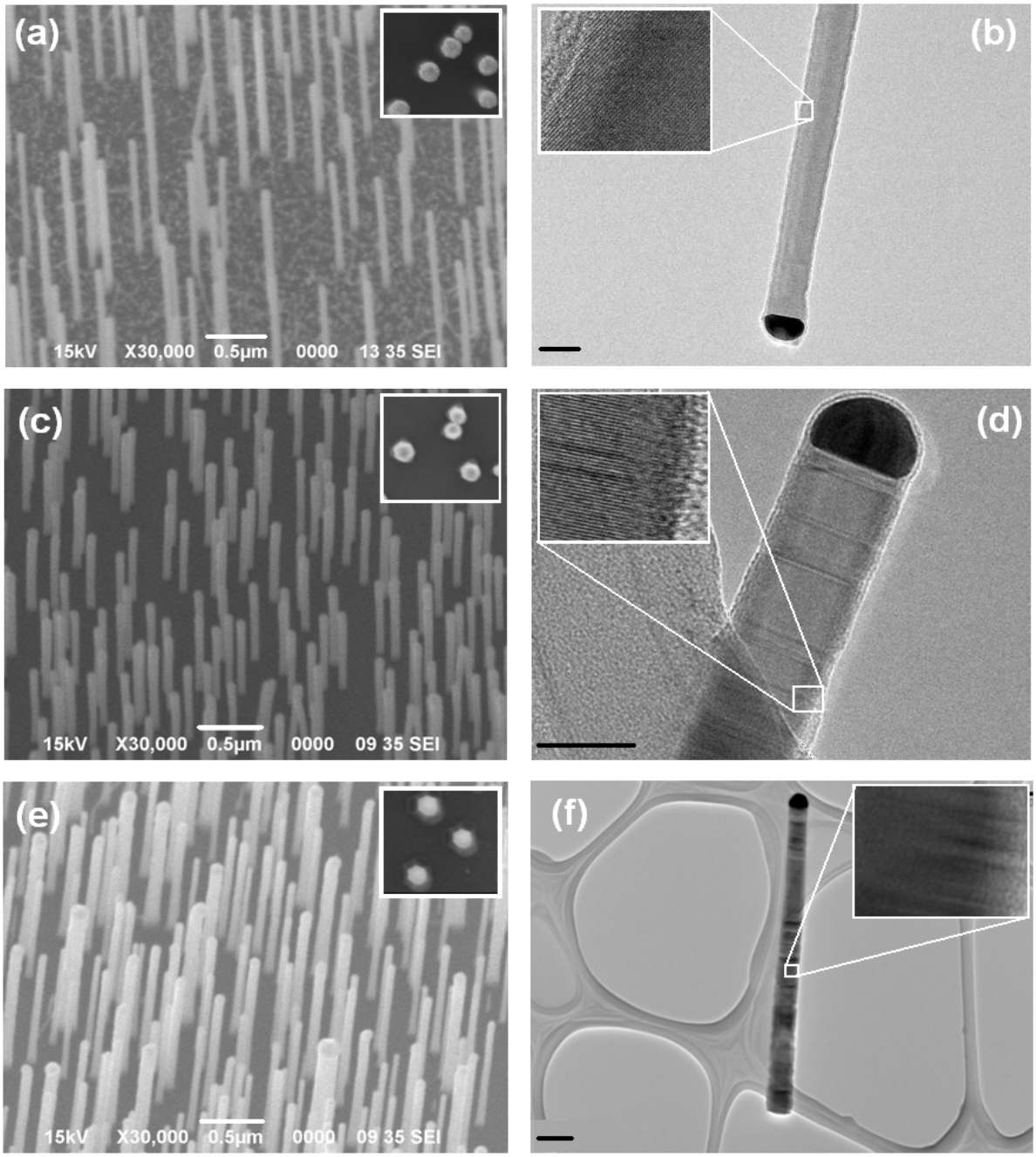

Figure 1 FE-SEM images for GaAs nanowires grown with V/III ratio of (a) 17, (c) 166 and (e) 297. Growth period and temperature was set at 30 mins and 500^{o}C respectively. Insets: Topview of GaAs nanowires with a clear change in the base of the circular to hexagonal shape as the V/III ratio increases. (b), (d) and (f) are TEM images for the corresponding V/III ratio. The bar scales shown in the TEM images represent distance of 100 nm. Insets: magnified TEM images at the middle of each NW.

Current voltage characteristic in Figure 2 shows that I-V curve of GaAs NWs with V/III ratio of 17 and 166 were nearly linear at forward bias voltage compared to 297 with oscillated curve. These linear curves indicate an ohmic contact between the tip to GaAs substrate. The ohmic contact was also possibly due to less of defect structure of GaAs NW with V/III ratio of 17 and 166. The range of V/III ratio from 17 to 166 observed are the optimum parameters (high resolution TEM) with resulting NW structure as lack of defects and uniform in diameters. This epitaxially grown NW also consists of zincblende structure as shown in Figure 1 (b and d). The measured resistance in the range of (0.07 - 0.09) x 10^9 Ω was calculated from the differential conductivity, i.e the slope of the I-V characteristic at higher current due to stabilization in current tunneling. These resistances are expected to come out from a thin oxide layer that formed on NW surface as similar to native oxide. However, some oscillating curve was detected at sample with V/III ratio of 17 as in Figure 2 (curve (a)) when voltage applied is higher than 3.0 V. As mention earlier, the GaAs NWs grown with low V/III ratio was in the pre-phase of growing matured structure. The higher voltage will damage the layer of GaAs structure. For GaAs NWs samples prepared at V/III ratio of 297, the measured current was oscillates at all range of forward bias voltage. This conductance oscillation might be attributed to charge trapping and de-trapping of GaAs nanowire.[20] The number of oscillation is proportional to the number of traps which might be due to hexagonal base shape at the base of NW as shown in Figure 1(f). Due to the enhanced surface-to-volume ratio in NWs, their electrical properties may depend sensitively on their surface conditions and geometrical configurations. The extracted I-V data sometimes show the non-equilibrium phase because of the electrons flowing through a NW that are scattered by absorption and emissions of phonons (lattice vibrations), boundary scattering, lattice and other structural defects and impurity atoms.[21] The transport behaviour of NWs can also be modified by their surface conditions such as extended defects and dopant. All the prepared samples were softly breakdown current measuring at nearly 4V with negative direct current voltage supplied.

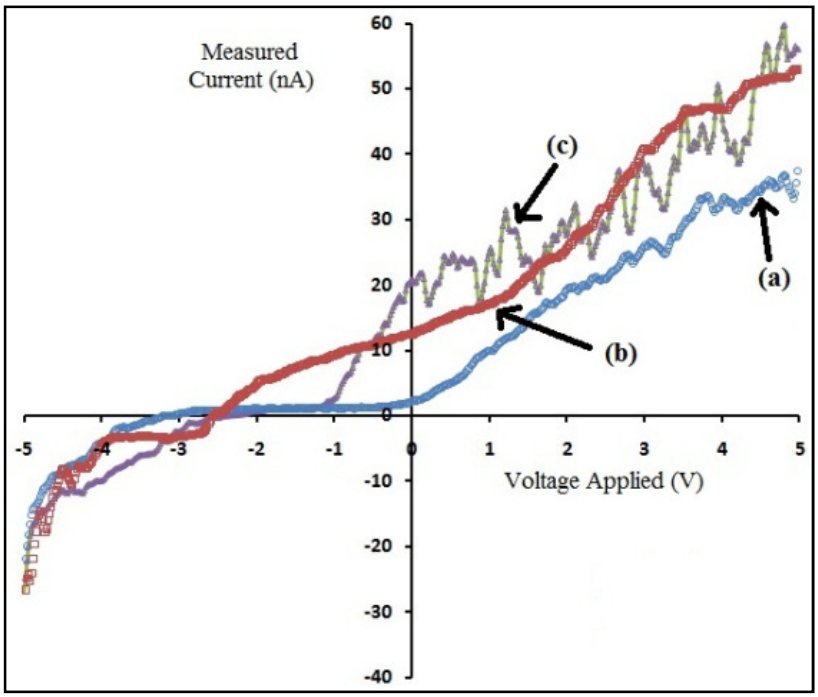

Figure 2 I-V characteristics of GaAs NWs with different V/III ratio (a) 17, (b) 166 and (c) 297. The measurement was conducted using conductivity atomic force microscopy (CAFM) by applying voltage in the range of -5 to 5 Volt.

4.0 CONCLUSION

Zincblende nanowires with the V/III ratio of 17 to 166 indicate ohmic characteristic compared to oscillation current for wurtzite structures at V/III ratio of 297. The optimum value of V/III growth parameters is 166, for achieving GaAs NWs with uniform diameters and chemical composition to absorbs high energy and ascertain low reflectivity of the carrier generated.

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