# Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes

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*Abstract*—**Conventional GaN vertical devices, though promising for high-power applications, need expensive GaN substrates. Recently, low-cost GaN-on-Si vertical diodes have been demonstrated for the first time. This paper presents a systematic study to understand and control the OFF-state leakage current in the GaN-on-Si vertical diodes. Various leakage sources were investigated and separated, including leakage through the bulk drift region, passivation layer, etch sidewall, and transition layers. To suppress the leakage along the etch sidewall, an advanced edge termination technology has been developed by combining plasma treatment, tetramethylammonium hydroxide wet etching, and ion implantation. With this advanced edge termination technology, an OFF-state leakage current similar to Si, SiC, and GaN lateral devices has been achieved in the GaN-on-Si vertical diodes with over 300 V breakdown voltage and 2.9-MV/cm peak electric field. The origin of the remaining OFF-state leakage current can be explained by a combination of electron tunneling at the p-GaN/drift-layer interface and carrier hopping between dislocation traps. The low leakage current achieved in these devices demonstrates the great potential of the GaN-on-Si vertical device as a new low-cost candidate for high-performance power electronics.**

*Index Terms*—**Edge termination, GaN-on-Si vertical device, leakage control, leakage origin, power electronics.**

## I. INTRODUCTION

GaN-BASED transistors and diodes are excellent candidates for high-voltage and high-power electronics, due to the superior material properties of GaN compared
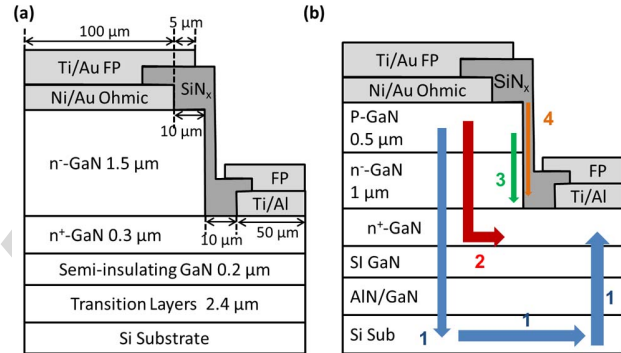
Fig. 1. Schematic of the GaN-on-Si vertical (a) Schottky and (b) p-n diodes. Four possible leakage paths in the GaN-on-Si vertical diodes are shown in (b).

with Si and GaAs. Currently, both vertical and lateral devices are being considered for GaN power devices [1]. Lateral structures, such as AlGaN/GaN high-electron-mobility transistors, though having been studied extensively, still face reliability and integration challenges [1]. GaN vertical devices have attracted increased attention recently, due to several potential advantages over GaN lateral devices: 1) higher breakdown voltage (BV) capability without enlarging chip size [2]; 2) superior reliability due to the peak electric field ($E_{peak}$) being far away from the surface; and 3) superior thermal performance [2]. Recent demonstrations of high-performance vertical GaN diodes [3] and transistors [4], [5] on GaN susbstrates have made vertical structures very promising for the GaN power devices.

Despite the excellent performance demonstrated by the GaN vertical devices, the high cost (>1000× higher than Si substrates) and the small diameter of GaN substrates have become one of the main challenges for the commercialization of the GaN vertical power devices. Thus, lower cost substrates, in particular Si substrates, for GaN vertical devices would be greatly preferred to make their market insertion easier. However, the demonstration of the GaN-on-Si vertical devices is extremely challenging mainly due to two reasons: 1) the high dislocation density in GaN-on-Si and 2) the relatively thin GaN drift regions that can be grown on Si substrates.

By overcoming some of these challenges, our group successfully demonstrated GaN-on-Si vertical Schottky and
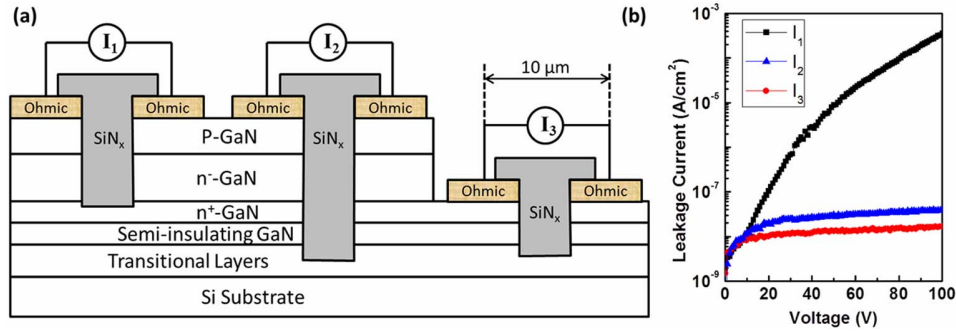
Fig. 2.    (a) Trench structures with different etching depths. $I_1$ measures the leakage of trench structure down to n$^+$-GaN. $I_2$ and $I_3$ measure the leakage of trench structures down to the transition layers. (b) Plot of the $I_1$, $I_2$, and $I_3$ measured from the trench structures. $I_2$ and $I_3$ are much smaller than $I_1$, indicating leakage through transition layers and Si substrates is negligible to the diode's total current.

p-n power diodes for the first time [6]. With a total GaN drift layer of only 1.5-$\mu$m think, a soft BV of 300 V was achieved for GaN-on-Si p-n diodes with an $E_{peak}$ of 2.9 MV/cm in GaN and a reverse leakage current ($\sim 10^{-2}$ A/cm$^2$ at $-200$ V) comparable with the lateral GaN devices. However, in order to compete with vertical GaN-on-GaN devices as well as commercial Si and SiC devices, the leakage current in the GaN-on-Si vertical devices needs to be further reduced, which also requires a thorough understanding on the origin of leakage.

In this paper, we conducted a systematic study on the origin of reverse leakage in the GaN-on-Si vertical diodes. We first identified the drift region and the etch sidewall as the major leakage paths in these structures. Then, by developing an advanced edge termination technology which combines plasma treatment, tetramethylammonium hydroxide (TMAH) wet etching, and ion implantation, we greatly reduced the OFF-state leakage current along the etch sidewalls and achieved a low leakage current in the GaN-on-Si vertical diodes, similar to the one in the state-of-the-art Si and SiC devices. The origin of this remaining OFF-state leakage current was further studied by TCAD simulations.

## II. DEVICE STRUCTURE AND LEAKAGE ANALYSIS

The schematic of the GaN-on-Si vertical Schottky and p-n diodes used in this paper is shown in Fig. 1(a) and (b). The p-n structure consists of 0.5-$\mu$m p-GaN (Mg: $1 \times 10^{19}$ cm$^{-3}$, $N_A \sim 1.5 \times 10^{17}$ cm$^{-3}$) and 1-$\mu$m n$^-$-GaN (Si: $5 \times 10^{16}$ cm$^{-3}$, $N_D \sim 2 \times 10^{16}$ cm$^{-3}$), 0.3-$\mu$m n$^+$-GaN (Si: $2 \times 10^{18}$ cm$^{-3}$) cathode contact region, 0.2-$\mu$m semi-insulating GaN, and 2.4-$\mu$m GaN/AlN transition layers, all grown on Si (111) substrates by metal–organic chemical vapor deposition [6]. The 1.6 $\mu$m of the top GaN layer was etched to form the cathode electrode. A Ti/Al ohmic contact ring and a Ni/Au circular ohmic were formed as the cathode and anode electrodes, respectively. A SiN$_x$ passivation layer ($\sim$200-nm thick) and a Ti/Au bilayer was further used for the field plate structure for both electrodes. The fabrication process has been reported in detail in [6].

The OFF-state leakage of the GaN-on-Si vertical p-n diode structures was analyzed in detail, as shown in Fig. 1(b). Four possible leakage paths exist in the GaN-on-Si
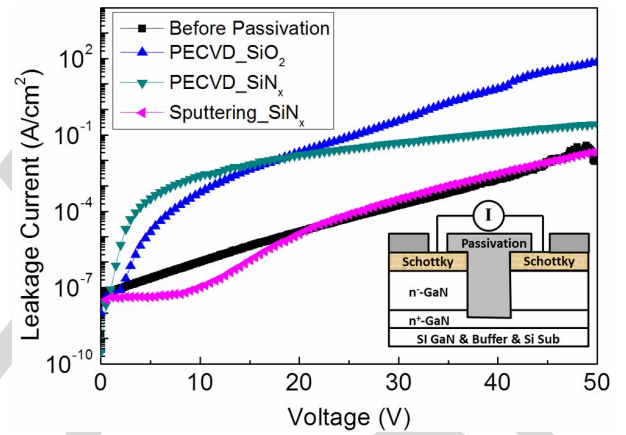


Fig. 3.    Leakage current before and after passivation by PECVD SiO$_2$, PECVD SiN$_x$, and sputtering SiN$_x$. Inset: structure used to measure leakage current.

vertical structures: 1) through the transition layers and Si substrate; 2) through the drift layer; 3) along the etch sidewall; and 4) through the passivation layer.

The contribution of leakage path #1 (through the transition layers and Si substrate) could be determined by measuring the leakage of trench structures with different etching depths, as shown in Fig. 2(a). When the trench is etched down to the transition layers, the leakage current reduces by more than three orders of magnitude compared with the leakage of the trench down to n$^+$-GaN layer, indicating the leakage path #1 is negligible in the diode's total leakage. The small leakage path #1 demonstrates the good vertical insulation of GaN-on-Si wafers.

The leakage path #4 (through the passivation layer) was made negligible through the use of a new GaN passivation technology based on a sputtering deposition system [6]. This technology, in contrast to traditional passivation schemes that use plasma-enhanced chemical vapor deposition (PECVD) [7], does not increase the leakage current with respect to the one in unpassivated samples, as shown in Fig. 3.

## III. SIDEWALL TREATMENT AND EDGE TERMINATION

The leakage path #3 (along etch sidewall) is typically due to etch-induced damage or defects (e.g., $N$ vacancies) created
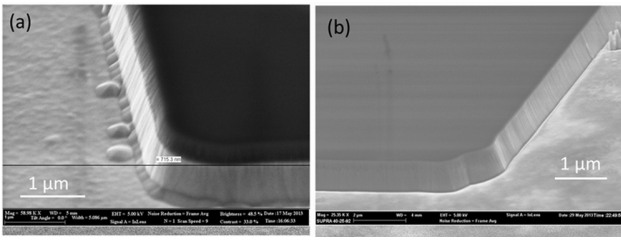
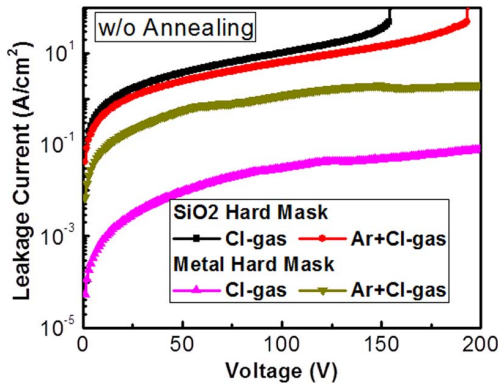Fig. 4. SEM image of the deep GaN etch sidewall for GaN-on-Si structures using (a) SiO$_2$ and (b) Ni hard mask.



Fig. 5. Leakage current through the sidewall of ICP-RIE etched samples using the SiO$_2$ and the Ni hard masks with and without Ar pretreatment. The Cl$_2$/BCl$_3$ etching with a metal hard mask and without Ar pretreatment leads to the lowest leakage current.



Fig. 6. Leakage current of the structure with different sidewall plasma treatments (CF$_4$, N$_2$, NH$_3$, and H$_2$) after GaN dry etching. Inset: structure for leakage current measurements.



Fig. 7. SEM images of GaN deep etch sidewalls without and with TMAH treatment for 60 min (in vertical p-n diodes).



Fig. 8. Leakage current using the TMAH wet etching after the GaN dry etching. Inset: structure used for leakage current measurements.

by the inductively coupled plasma (ICP) dry etching of GaN. Sugimoto *et al.* [8] reported, for example, that the surface of a p-GaN sidewall can be changed to a depleted or an n$^-$-GaN layer by ICP etching, which would induce a large leakage under high reverse bias.

Two technologies have been developed to reduce the leakage path #3: 1) GaN deep-etching technology and 2) advanced edge termination technology. The new GaN deep-etching technology was developed in an ICP reactive ion etching (ICP-RIE) system using a Cl$_2$/BCl$_3$/Ar gas combination and a metal hard mask. Compared with the oxide hard mask typically used in these etchings, the use of a metal hard mask enables a much smoother etch sidewall (Fig. 4), due to the lack of oxide edge erosion under high plasma energies. The smoother sidewall reduced the sidewall leakage current by four orders of magnitude, as shown in Fig. 5.

An advanced edge termination technology for the GaN-on-Si vertical device has been developed by combining plasma treatment, TMAH wet etching, and ion implantation. Various plasma treatments were studied to heal the damage of the ICP etching. As shown in Fig. 6, CF$_4$ and N$_2$ plasma treatment could effectively passivate the etch-induced $N$ vacancies and reduce the sidewall leakage. It is also worth noting that the CF$_4$ plasma was also applied in the GaN-based lateral devices to passivate interface defects [9], [10]. In contrast, H$_2$ plasma, which has been reported as able to create $N$ vacancies [11], induces a large sidewall leakage increase, indicating a strong correlation between sidewall leakage and $N$ vacancies in the GaN-on-Si vertical devices.

The TMAH wet etching (25% concentration) at 85 °C was found effective in removing the damage from the etch sidewall, especially near the p/n-GaN interface, as demonstrated in the sidewall topology images shown in Fig. 7. A TMAH treatment for 60 min reduces the sidewall leakage by more than 50×, as shown in Fig. 8. In addition, the forward characteristics

Fig. 9.  Diode forward characteristics by the TMAH wet etching for different times, from 15 to 60 min.



Fig. 10.  (a) Cross section and (b) top view of the GaN-on-Si vertical p-n diodes with ion implantation regions as edge termination.



Fig. 11.  Reverse characteristics of the GaN-on-Si vertical p-n diodes without and with ion implantation, as a function of different ion dose and energy.

of the GaN-on-Si vertical diodes were also enhanced by the TMAH treatment, as shown in Fig. 9. This improvement in forward characteristics may attribute to two factors: 1) a higher mobility and better material quality in the regions near etching sidewall, due to reduction of sidewall defects and 2) a mitigated current crowding due to the more vertical sidewall.
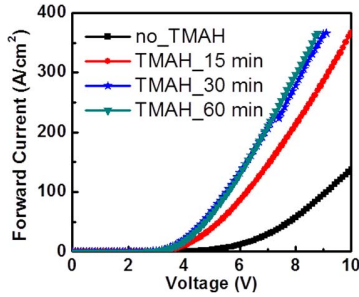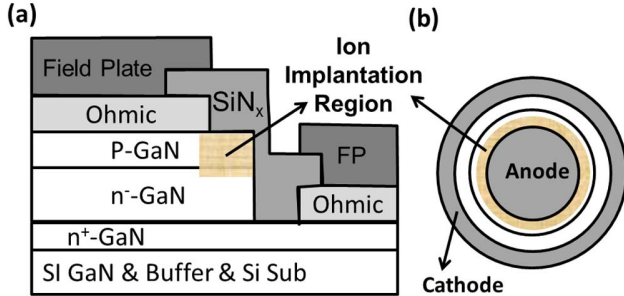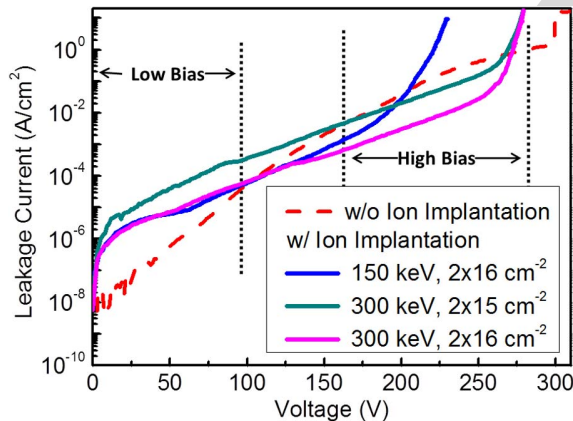
An ion implantation ring was introduced to isolate the main vertical current path from the etch sidewall, as shown in Fig. 10. Argon (Ar) was used for implantation [12]. As shown in Fig. 11, the ion implantation reduces the leakage at high reverse bias, due to a significant mitigation of leakage along the etch sidewall. However, the implantation slightly increases the device leakage at low bias due to a parasitic
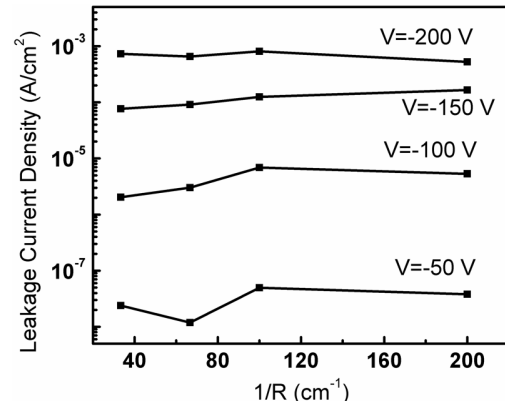


Fig. 12.  Total leakage current density of vertical p-n diodes with different anode radius $R$ ($R = 50$, 100, 150, and 300 $\mu$m), as a function of $1/R$ at a reverse voltage of 50, 100, 150, and 200 V.

leakage through the implanted region. Different implantation Ar dose and energies were also studied (Fig. 11). The ion dose mainly determines the insulating properties of the implant region and the device leakage current at low reverse bias, whereas the ion energy determines the depth of the implant region, with 150 keV for a depth of $\sim$0. 3 $\mu$m and 300 keV for $\sim$0.6 $\mu$m. High ion energy is needed to extend the implantation region beyond the p/n-GaN junction, in order to prevent the leakage from flowing toward the depleted p-GaN sidewall at a high bias.

## IV. ORIGIN OF BULK LEAKAGE COMPONENT

To further decouple the leakage path #2 (bulk component) and #3 (sidewall surface component) for devices with the advanced edge termination, the total leakage density of the vertical diodes with a radius of 50, 100, 150, and 300 $\mu$m was measured and plotted in Fig. 12. The total reverse leakage current density $J_{\text{total}}$ can be expressed as follows [13]:

$$J_{\text{total}} = J_2 + J_3 \times P/A = J_2 + 2J_3 \times 1/R \qquad (1)$$

where $J_2$ (A/cm$^2$) and $J_3$ (A/cm) are the bulk leakage current density (leakage path #2) and the perimeter leakage current density (leakage path #3), respectively. $P$ and $A$ are the perimeter and area of the vertical diodes, with $R$ defined as the anode radius. As shown in Fig. 12, the total leakage current exhibits almost no linear dependence on $1/R$, indicating that the sidewall leakage has been effectively suppressed by the edge terminations and the bulk component (leakage path #2) is the main contributor to the total device leakage current.

The OFF-state leakage mechanism of the bulk current component (leakage path #2) was further studied using TCAD simulation [14]. It is well known that dislocations in GaN Schottky diodes are the major paths of reverse leakage current [15], [16]. The conduction mechanism along the dislocations is probably due to hopping of carriers from trap to the nearest neighbor trap [17]. Therefore, it is postulated that the bulk component is a result of electron hopping along the dislocations. In the simulation, under reverse bias, electrons tunnel (either elastically or inelastically) from the p-GaN/drift-layer interface to the dislocation traps and then

TABLE I

LEAKAGE AND COST BENCHMARKING FOR THE GaN VERTICAL DEVICE ON DIFFERENT SUBSTRATES, GaN LATERAL DEVICE, Si AND SiC DEVICE

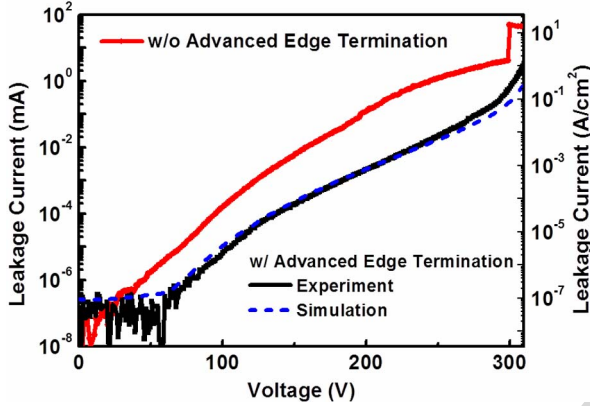| Diode Structure | Leakage Current (Density) at -200 V | $I_{on}/I_{off}$ ratio | Available Substrate | Substrate Cost per CM$^2$ |
|---|---|---|---|---|
| GaN-on-Si Vertical Diodes (This work) | < 1 µA ($10^{-4}$-$10^{-3}$ A/cm$^2$) | ~ $10^6$ | 200 mm Si | ~ $0.08 |
| GaN-on-Sapphire Vertical Diodes [19] | $10^{-3}$ A/cm$^2$ | ~ $10^5$ | 100 mm Sapphire | ~ $2.2 |
| GaN-on-GaN Vertical Diodes [20] | $10^{-5} - 10^{-6}$ A/cm$^2$ | ~ $10^9$ | 50 mm GaN | ~ $100 |
| AlGaN/GaN Lateral Diodes [21] | $10^{-2}$ A/cm$^2$ [6] | ~ $10^5$ | 200 mm Si | ~ $0.08 |
| Si Diode (NTE 588) | 5 µA | ~ $10^6$ | 200 mm Si | ~ $0.08 |
| SiC Diode (APT6SC60K) | < 1 µA | ~ $10^6$ | 75 mm SiC | ~ $6 |
| Si Power MOSFET (IRHNJ597230) | > 10 µA (10 µA at -160 V) | ~ $10^6$ | 200 mm Si | ~ $0.08 |



Fig. 13. Experimental and simulated leakage current of the GaN-on-Si vertical p-n diodes with advanced edge termination, and experimental leakage of vertical diodes without edge termination. The simulation is in good agreement with experiment. The edge termination is able to achieve a reduction of leakage by about two orders of magnitude and the elimination of the voltage hump at ∼300 V.



Fig. 14. Forward current characteristics of the GaN-on-Si vertical diodes with a diameter of 600 µm. Measurement in pulse-mode with different duty cycles shows no degradation in diode current. Inset: forward characteristics of diodes with a radius of 100 µm reveal an ON-resistance of 6 mΩ · cm$^2$ for Schottky and 10 mΩ · cm$^2$ for p-n diodes.

hop from trap to trap along the dislocation. Carrier hopping between dislocation traps is modeled using drift mobility in a Gaussian disorder model [18]. With this setup, the simulation matches the slope and magnitude of the experiment fairly well (Fig. 13). Impact ionization was also turned ON to match the steep increase of current at ∼300 V. The details of simulation will be elaborated in a follow-up paper.

## V. DEVICE PERFORMANCE AND BENCHMARKING

The reverse $I-V$ characteristics of optimized GaN-on-Si vertical p-n diodes with and without the advanced edge termination are shown in Fig. 13. As shown, the advanced edge termination is able to reduce the leakage by about two orders of magnitude while maintaining a soft BV of over 300 V and a peak electric field >2.9 MV/cm. In addition, the reverse characteristics of vertical diodes with the advanced edge termination does not exhibit a voltage hump at ∼300 V, which corresponds to the traps-filled-limited voltage of the acceptor traps according to our detailed analysis in [6]. This indicates that the large acceptor traps observed in the vertical diodes without the advanced edge termination [6] are located at the etch sidewall, and are probably due to $N$ vacancies and point defects produced in the etching process. With the elimination of the sidewall traps, good measurement reproducibility and BV uniformity have also been observed in the GaN-on-Si vertical p-n diodes throughout the whole wafer.
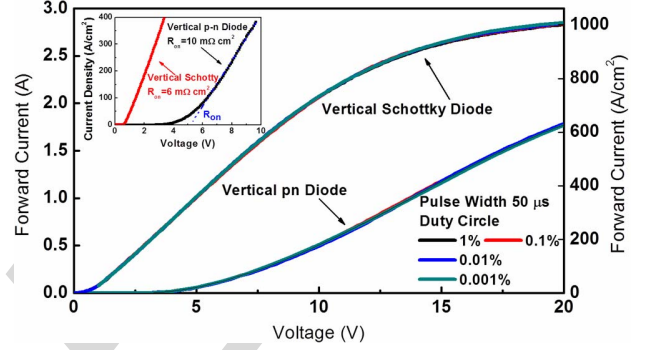
The forward transient behavior and current capability of diode are also enhanced. The forward $I-V$ characteristics of the GaN-on-Si vertical diodes with a diameter of 600 µm have demonstrated a current level >2 A and a current density >500 A/cm$^2$, with no degradation as a function of duty cycle (from 0.001% to 1%) in pulse measurements, as shown in Fig. 14. An ON-resistance of 6 and 10 mΩ · cm$^2$ was obtained for GaN-on-Si vertical Schottky and p-n diodes, respectively. The relatively high ON-resistance of our GaN-on-Si vertical diodes is due to the relatively high contact resistance of ohmic on p-GaN, low mobility of p-GaN (∼14 cm$^2$/V·s), and the current crowding near the corner of etching sidewall. An improvement of the p-GaN material quality is expected to further reduce the ON-resistance of our GaN-on-Si vertical diodes.

The BV capability of our GaN-on-Si vertical diodes has been benchmarked in detail in [6]. With a total drift layer of only 1.5-µm thick, our GaN-on-Si vertical diodes achieved a soft BV of 300 V, which is close to the theoretical limit for the GaN p-n diodes. This indicates the great potential of the GaN vertical devices to achieve a higher BV with thicker GaN epilayers.

The leakage characteristics are benchmarked in Table I. As shown, with over 1000× lower substrate cost than the GaN-on-GaN device, our GaN-on-Si vertical devices achieved an OFF-state leakage current lower than the GaN lateral devices and similar to the one in the state-of-the-art Si and SiC devices. The low-leakage and high-BV performances of

our GaN-on-Si vertical diodes have demonstrated the great potential of the GaN-on-Si vertical device as a new low-cost candidate for high-performance power electronics.

## VI. Conclusion

In this paper, we conducted a systematic study on the origin of reverse leakage in the GaN-on-Si vertical diodes. Various leakage sources were separated and clarified, including bulk drift region, passivation layer, etch sidewall, and transition layers. By developing an advanced edge termination technology which combines plasma treatment, TMAH wet etching and ion implantation, we greatly reduced the leakage along etch sidewalls and achieved a BV >300 V, an $E_{\text{peak}}$ of 2.9 MV/cm, and an OFF-state leakage current in the GaN-on-Si vertical diodes similar to the one in Si and SiC devices. The bulk component of the leakage can be explained by a combination of electron tunneling at the p-GaN/drift-layer interface and carrier hopping between dislocation traps. The high-BV and low-leakage capabilities have demonstrated the suitability of the GaN-on-Si vertical device for high-performance power electronics.

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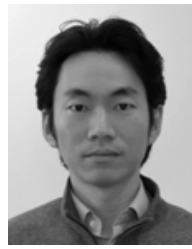**Nelson de Almeida Braga** received the B.S. degree in electrical engineering and the M.S. degree in electronic engineering from the University of São Paulo, São Paulo, Brazil, in 1986 and 1989, respectively, and the Ph.D. degree from North Carolina State University, Raleigh, NC, USA, in 1994.

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# Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes

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*Abstract*—**Conventional GaN vertical devices, though promising for high-power applications, need expensive GaN substrates. Recently, low-cost GaN-on-Si vertical diodes have been demonstrated for the first time. This paper presents a systematic study to understand and control the OFF-state leakage current in the GaN-on-Si vertical diodes. Various leakage sources were investigated and separated, including leakage through the bulk drift region, passivation layer, etch sidewall, and transition layers. To suppress the leakage along the etch sidewall, an advanced edge termination technology has been developed by combining plasma treatment, tetramethylammonium hydroxide wet etching, and ion implantation. With this advanced edge termination technology, an OFF-state leakage current similar to Si, SiC, and GaN lateral devices has been achieved in the GaN-on-Si vertical diodes with over 300 V breakdown voltage and 2.9-MV/cm peak electric field. The origin of the remaining OFF-state leakage current can be explained by a combination of electron tunneling at the p-GaN/drift-layer interface and carrier hopping between dislocation traps. The low leakage current achieved in these devices demonstrates the great potential of the GaN-on-Si vertical device as a new low-cost candidate for high-performance power electronics.**

*Index Terms*—**Edge termination, GaN-on-Si vertical device, leakage control, leakage origin, power electronics.**

## I. INTRODUCTION

GaN-BASED transistors and diodes are excellent candidates for high-voltage and high-power electronics, due to the superior material properties of GaN compared
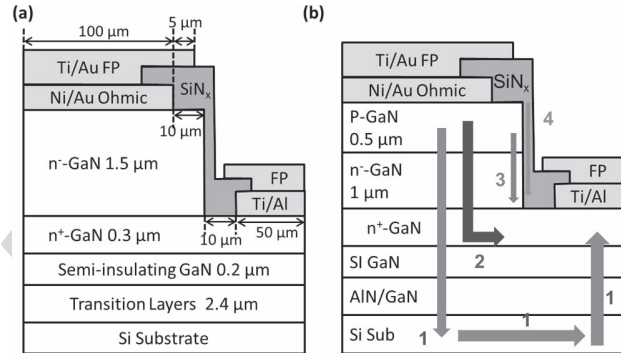
Fig. 1. Schematic of the GaN-on-Si vertical (a) Schottky and (b) p-n diodes. Four possible leakage paths in the GaN-on-Si vertical diodes are shown in (b).

with Si and GaAs. Currently, both vertical and lateral devices are being considered for GaN power devices [1]. Lateral structures, such as AlGaN/GaN high-electron-mobility transistors, though having been studied extensively, still face reliability and integration challenges [1]. GaN vertical devices have attracted increased attention recently, due to several potential advantages over GaN lateral devices: 1) higher breakdown voltage (BV) capability without enlarging chip size [2]; 2) superior reliability due to the peak electric field ($E_{peak}$) being far away from the surface; and 3) superior thermal performance [2]. Recent demonstrations of high-performance vertical GaN diodes [3] and transistors [4], [5] on GaN susbstrates have made vertical structures very promising for the GaN power devices.

Despite the excellent performance demonstrated by the GaN vertical devices, the high cost (>1000× higher than Si substrates) and the small diameter of GaN substrates have become one of the main challenges for the commercialization of the GaN vertical power devices. Thus, lower cost substrates, in particular Si substrates, for GaN vertical devices would be greatly preferred to make their market insertion easier. However, the demonstration of the GaN-on-Si vertical devices is extremely challenging mainly due to two reasons: 1) the high dislocation density in GaN-on-Si and 2) the relatively thin GaN drift regions that can be grown on Si substrates.

By overcoming some of these challenges, our group successfully demonstrated GaN-on-Si vertical Schottky and
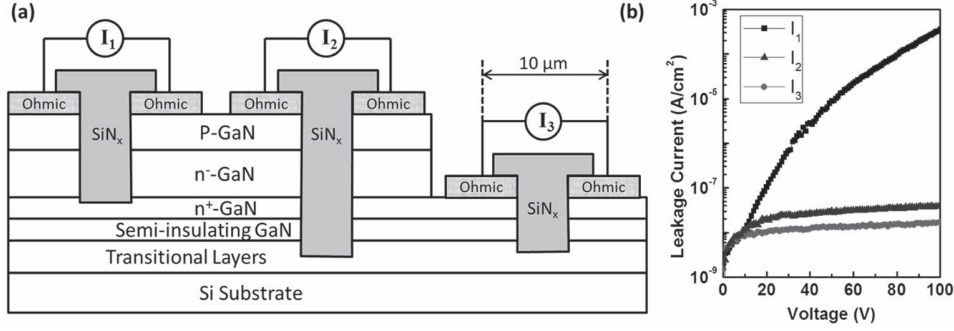
Fig. 2.    (a) Trench structures with different etching depths. $I_1$ measures the leakage of trench structure down to n$^+$-GaN. $I_2$ and $I_3$ measure the leakage of trench structures down to the transition layers. (b) Plot of the $I_1$, $I_2$, and $I_3$ measured from the trench structures. $I_2$ and $I_3$ are much smaller than $I_1$, indicating leakage through transition layers and Si substrates is negligible to the diode's total current.

p-n power diodes for the first time [6]. With a total GaN drift layer of only 1.5-$\mu$m think, a soft BV of 300 V was achieved for GaN-on-Si p-n diodes with an $E_{peak}$ of 2.9 MV/cm in GaN and a reverse leakage current ($\sim 10^{-2}$ A/cm$^2$ at $-200$ V) comparable with the lateral GaN devices. However, in order to compete with vertical GaN-on-GaN devices as well as commercial Si and SiC devices, the leakage current in the GaN-on-Si vertical devices needs to be further reduced, which also requires a thorough understanding on the origin of leakage.

In this paper, we conducted a systematic study on the origin of reverse leakage in the GaN-on-Si vertical diodes. We first identified the drift region and the etch sidewall as the major leakage paths in these structures. Then, by developing an advanced edge termination technology which combines plasma treatment, tetramethylammonium hydroxide (TMAH) wet etching, and ion implantation, we greatly reduced the OFF-state leakage current along the etch sidewalls and achieved a low leakage current in the GaN-on-Si vertical diodes, similar to the one in the state-of-the-art Si and SiC devices. The origin of this remaining OFF-state leakage current was further studied by TCAD simulations.

## II. Device Structure and Leakage Analysis

The schematic of the GaN-on-Si vertical Schottky and p-n diodes used in this paper is shown in Fig. 1(a) and (b). The p-n structure consists of 0.5-$\mu$m p-GaN (Mg: $1 \times 10^{19}$ cm$^{-3}$, $N_A \sim 1.5 \times 10^{17}$ cm$^{-3}$) and 1-$\mu$m n$^-$-GaN (Si: $5 \times 10^{16}$ cm$^{-3}$, $N_D \sim 2 \times 10^{16}$ cm$^{-3}$), 0.3-$\mu$m n$^+$-GaN (Si: $2 \times 10^{18}$ cm$^{-3}$) cathode contact region, 0.2-$\mu$m semi-insulating GaN, and 2.4-$\mu$m GaN/AlN transition layers, all grown on Si (111) substrates by metal–organic chemical vapor deposition [6]. The 1.6 $\mu$m of the top GaN layer was etched to form the cathode electrode. A Ti/Al ohmic contact ring and a Ni/Au circular ohmic were formed as the cathode and anode electrodes, respectively. A SiN$_x$ passivation layer ($\sim$200-nm thick) and a Ti/Au bilayer was further used for the field plate structure for both electrodes. The fabrication process has been reported in detail in [6].

The OFF-state leakage of the GaN-on-Si vertical p-n diode structures was analyzed in detail, as shown in Fig. 1(b). Four possible leakage paths exist in the GaN-on-Si
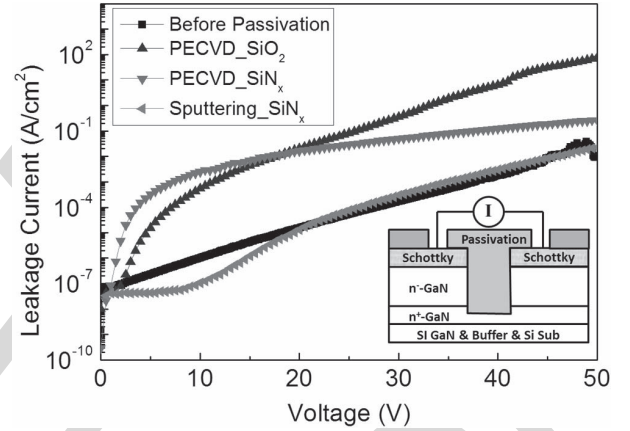


Fig. 3.    Leakage current before and after passivation by PECVD SiO$_2$, PECVD SiN$_x$, and sputtering SiN$_x$. Inset: structure used to measure leakage current.

vertical structures: 1) through the transition layers and Si substrate; 2) through the drift layer; 3) along the etch sidewall; and 4) through the passivation layer.

The contribution of leakage path #1 (through the transition layers and Si substrate) could be determined by measuring the leakage of trench structures with different etching depths, as shown in Fig. 2(a). When the trench is etched down to the transition layers, the leakage current reduces by more than three orders of magnitude compared with the leakage of the trench down to n$^+$-GaN layer, indicating the leakage path #1 is negligible in the diode's total leakage. The small leakage path #1 demonstrates the good vertical insulation of GaN-on-Si wafers.

The leakage path #4 (through the passivation layer) was made negligible through the use of a new GaN passivation technology based on a sputtering deposition system [6]. This technology, in contrast to traditional passivation schemes that use plasma-enhanced chemical vapor deposition (PECVD) [7], does not increase the leakage current with respect to the one in unpassivated samples, as shown in Fig. 3.

## III. Sidewall Treatment and Edge Termination

The leakage path #3 (along etch sidewall) is typically due to etch-induced damage or defects (e.g., $N$ vacancies) created
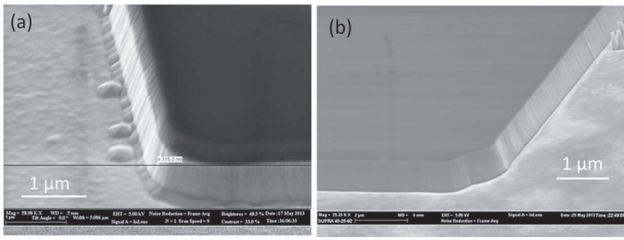
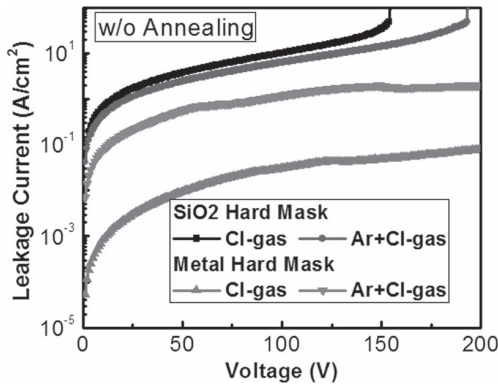Fig. 4. SEM image of the deep GaN etch sidewall for GaN-on-Si structures using (a) $SiO_2$ and (b) Ni hard mask.



Fig. 5. Leakage current through the sidewall of ICP-RIE etched samples using the $SiO_2$ and the Ni hard masks with and without Ar pretreatment. The $Cl_2/BCl_3$ etching with a metal hard mask and without Ar pretreatment leads to the lowest leakage current.

by the inductively coupled plasma (ICP) dry etching of GaN. Sugimoto *et al.* [8] reported, for example, that the surface of a p-GaN sidewall can be changed to a depleted or an $n^-$-GaN layer by ICP etching, which would induce a large leakage under high reverse bias.

Two technologies have been developed to reduce the leakage path #3: 1) GaN deep-etching technology and 2) advanced edge termination technology. The new GaN deep-etching technology was developed in an ICP reactive ion etching (ICP-RIE) system using a $Cl_2/BCl_3/Ar$ gas combination and a metal hard mask. Compared with the oxide hard mask typically used in these etchings, the use of a metal hard mask enables a much smoother etch sidewall (Fig. 4), due to the lack of oxide edge erosion under high plasma energies. The smoother sidewall reduced the sidewall leakage current by four orders of magnitude, as shown in Fig. 5.

An advanced edge termination technology for the GaN-on-Si vertical device has been developed by combining plasma treatment, TMAH wet etching, and ion implantation. Various plasma treatments were studied to heal the damage of the ICP etching. As shown in Fig. 6, $CF_4$ and $N_2$ plasma treatment could effectively passivate the etch-induced $N$ vacancies and reduce the sidewall leakage. It is also worth noting that the $CF_4$ plasma was also applied in the GaN-based lateral devices to passivate interface defects [9], [10]. In contrast, $H_2$ plasma, which has been reported as able to create $N$ vacancies [11], induces a large sidewall leakage increase, indicating a strong correlation between sidewall leakage and $N$ vacancies in the GaN-on-Si vertical devices.



Fig. 6. Leakage current of the structure with different sidewall plasma treatments ($CF_4$, $N_2$, $NH_3$, and $H_2$) after GaN dry etching. Inset: structure for leakage current measurements.
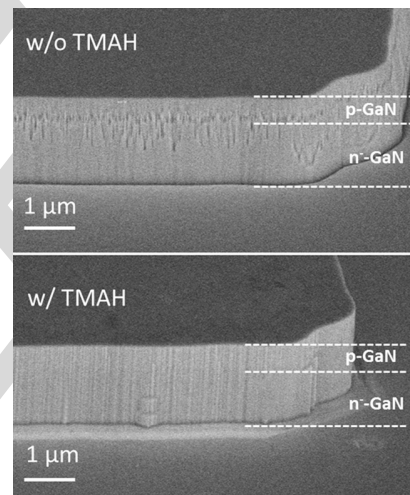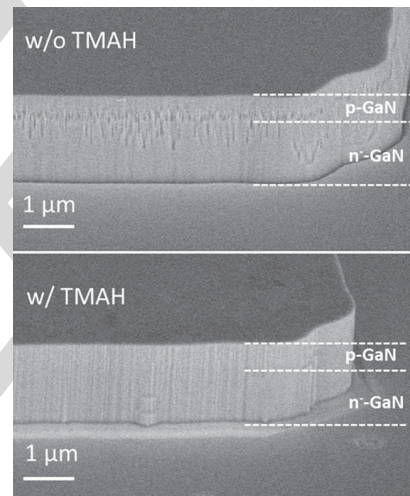


Fig. 7. SEM images of GaN deep etch sidewalls without and with TMAH treatment for 60 min (in vertical p-n diodes).
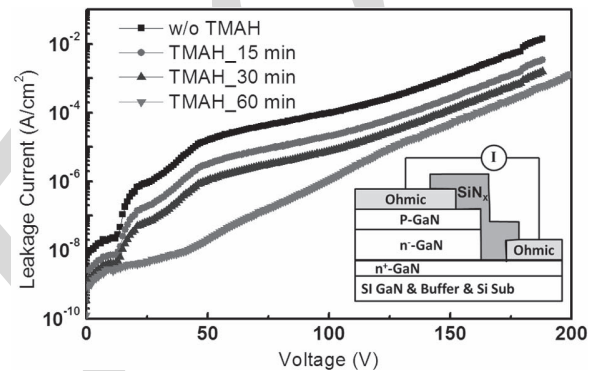


Fig. 8. Leakage current using the TMAH wet etching after the GaN dry etching. Inset: structure used for leakage current measurements.

The TMAH wet etching (25% concentration) at 85 °C was found effective in removing the damage from the etch sidewall, especially near the p/n-GaN interface, as demonstrated in the sidewall topology images shown in Fig. 7. A TMAH treatment for 60 min reduces the sidewall leakage by more than 50×, as shown in Fig. 8. In addition, the forward characteristics

Fig. 9.   Diode forward characteristics by the TMAH wet etching for different times, from 15 to 60 min.



Fig. 10.   (a) Cross section and (b) top view of the GaN-on-Si vertical p-n diodes with ion implantation regions as edge termination.



Fig. 11.   Reverse characteristics of the GaN-on-Si vertical p-n diodes without and with ion implantation, as a function of different ion dose and energy.

of the GaN-on-Si vertical diodes were also enhanced by the TMAH treatment, as shown in Fig. 9. This improvement in forward characteristics may attribute to two factors: 1) a higher mobility and better material quality in the regions near etching sidewall, due to reduction of sidewall defects and 2) a mitigated current crowding due to the more vertical sidewall.
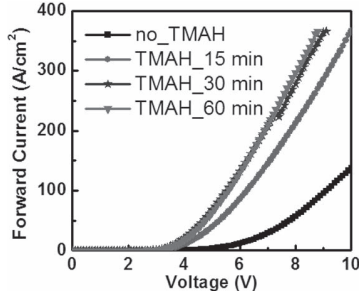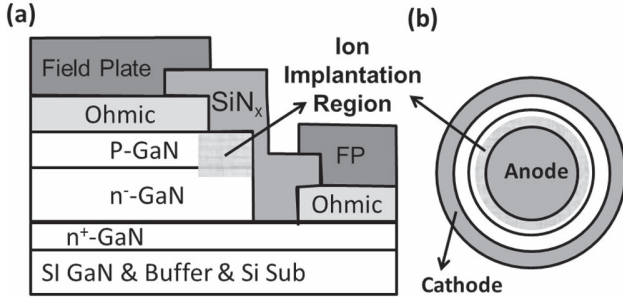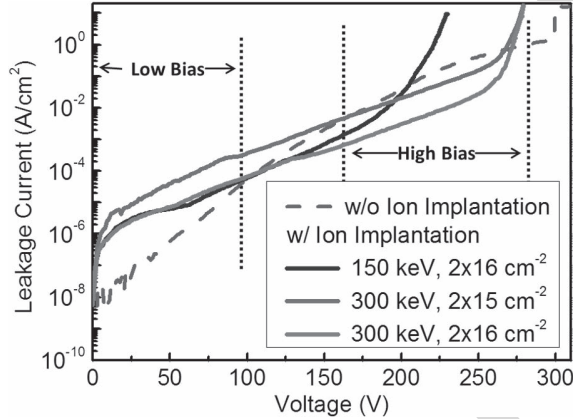
An ion implantation ring was introduced to isolate the main vertical current path from the etch sidewall, as shown in Fig. 10. Argon (Ar) was used for implantation [12]. As shown in Fig. 11, the ion implantation reduces the leakage at high reverse bias, due to a significant mitigation of leakage along the etch sidewall. However, the implantation slightly increases the device leakage at low bias due to a parasitic
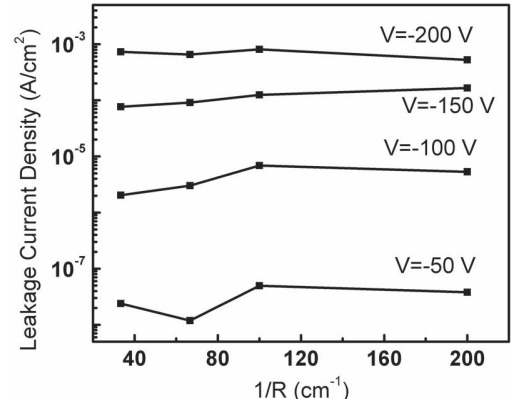


Fig. 12.   Total leakage current density of vertical p-n diodes with different anode radius $R$ ($R$ = 50, 100, 150, and 300 $\mu$m), as a function of $1/R$ at a reverse voltage of 50, 100, 150, and 200 V.

leakage through the implanted region. Different implantation Ar dose and energies were also studied (Fig. 11). The ion dose mainly determines the insulating properties of the implant region and the device leakage current at low reverse bias, whereas the ion energy determines the depth of the implant region, with 150 keV for a depth of $\sim$0. 3 $\mu$m and 300 keV for $\sim$0.6 $\mu$m. High ion energy is needed to extend the implantation region beyond the p/n-GaN junction, in order to prevent the leakage from flowing toward the depleted p-GaN sidewall at a high bias.

## IV.   ORIGIN OF BULK LEAKAGE COMPONENT

To further decouple the leakage path #2 (bulk component) and #3 (sidewall surface component) for devices with the advanced edge termination, the total leakage density of the vertical diodes with a radius of 50, 100, 150, and 300 $\mu$m was measured and plotted in Fig. 12. The total reverse leakage current density $J_{\text{total}}$ can be expressed as follows [13]:

$$J_{\text{total}} = J_2 + J_3 \times P/A = J_2 + 2J_3 \times 1/R \qquad (1)$$

where $J_2$ (A/cm$^2$) and $J_3$ (A/cm) are the bulk leakage current density (leakage path #2) and the perimeter leakage current density (leakage path #3), respectively. $P$ and $A$ are the perimeter and area of the vertical diodes, with $R$ defined as the anode radius. As shown in Fig. 12, the total leakage current exhibits almost no linear dependence on $1/R$, indicating that the sidewall leakage has been effectively suppressed by the edge terminations and the bulk component (leakage path #2) is the main contributor to the total device leakage current.

The OFF-state leakage mechanism of the bulk current component (leakage path #2) was further studied using TCAD simulation [14]. It is well known that dislocations in GaN Schottky diodes are the major paths of reverse leakage current [15], [16]. The conduction mechanism along the dislocations is probably due to hopping of carriers from trap to the nearest neighbor trap [17]. Therefore, it is postulated that the bulk component is a result of electron hopping along the dislocations. In the simulation, under reverse bias, electrons tunnel (either elastically or inelastically) from the p-GaN/drift-layer interface to the dislocation traps and then

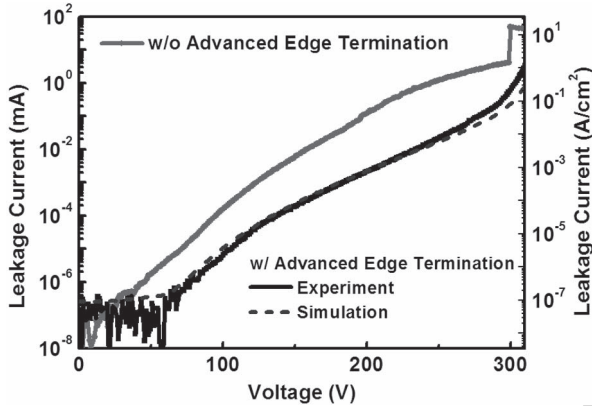| Diode Structure | Leakage Current (Density) at -200 V | $I_{on}/I_{off}$ ratio | Available Substrate | Substrate Cost per $CM^2$ |
|---|---|---|---|---|
| GaN-on-Si Vertical Diodes (This work) | < 1 $\mu$A ($10^{-4}$-$10^{-3}$ A/cm$^2$) | $\sim 10^6$ | 200 mm Si | $\sim$ $0.08 |
| GaN-on-Sapphire Vertical Diodes [19] | $10^{-3}$ A/cm$^2$ | $\sim 10^5$ | 100 mm Sapphire | $\sim$ $2.2 |
| GaN-on-GaN Vertical Diodes [20] | $10^{-5}$ – $10^{-6}$ A/cm$^2$ | $\sim 10^9$ | 50 mm GaN | $\sim$ $100 |
| AlGaN/GaN Lateral Diodes [21] | $10^{-2}$ A/cm$^2$ [6] | $\sim 10^5$ | 200 mm Si | $\sim$ $0.08 |
| Si Diode (NTE 588) | 5 $\mu$A | $\sim 10^6$ | 200 mm Si | $\sim$ $0.08 |
| SiC Diode (APT6SC60K) | < 1 $\mu$A | $\sim 10^6$ | 75 mm SiC | $\sim$ $6 |
| Si Power MOSFET (IRHNJ597230) | > 10 $\mu$A (10 $\mu$A at -160 V) | $\sim 10^6$ | 200 mm Si | $\sim$ $0.08 |



Fig. 13. Experimental and simulated leakage current of the GaN-on-Si vertical p-n diodes with advanced edge termination, and experimental leakage of vertical diodes without edge termination. The simulation is in good agreement with experiment. The edge termination is able to achieve a reduction of leakage by about two orders of magnitude and the elimination of the voltage hump at $\sim$300 V.



Fig. 14. Forward current characteristics of the GaN-on-Si vertical diodes with a diameter of 600 $\mu$m. Measurement in pulse-mode with different duty cycles shows no degradation in diode current. Inset: forward characteristics of diodes with a radius of 100 $\mu$m reveal an ON-resistance of 6 m$\Omega \cdot$cm$^2$ for Schottky and 10 m$\Omega \cdot$cm$^2$ for p-n diodes.

hop from trap to trap along the dislocation. Carrier hopping between dislocation traps is modeled using drift mobility in a Gaussian disorder model [18]. With this setup, the simulation matches the slope and magnitude of the experiment fairly well (Fig. 13). Impact ionization was also turned ON to match the steep increase of current at $\sim$300 V. The details of simulation will be elaborated in a follow-up paper.

## V. DEVICE PERFORMANCE AND BENCHMARKING

The reverse $I-V$ characteristics of optimized GaN-on-Si vertical p-n diodes with and without the advanced edge termination are shown in Fig. 13. As shown, the advanced edge termination is able to reduce the leakage by about two orders of magnitude while maintaining a soft BV of over 300 V and a peak electric field >2.9 MV/cm. In addition, the reverse characteristics of vertical diodes with the advanced edge termination does not exhibit a voltage hump at $\sim$300 V, which corresponds to the traps-filled-limited voltage of the acceptor traps according to our detailed analysis in [6]. This indicates that the large acceptor traps observed in the vertical diodes without the advanced edge termination [6] are located at the etch sidewall, and are probably due to $N$ vacancies and point defects produced in the etching process. With the elimination of the sidewall traps, good measurement reproducibility and BV uniformity have also been observed in the GaN-on-Si vertical p-n diodes throughout the whole wafer.
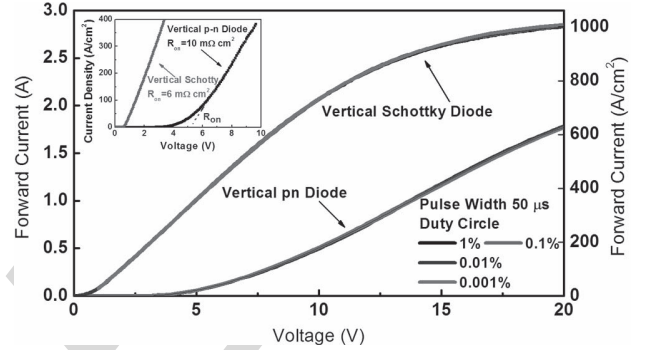
The forward transient behavior and current capability of diode are also enhanced. The forward $I-V$ characteristics of the GaN-on-Si vertical diodes with a diameter of 600 $\mu$m have demonstrated a current level >2 A and a current density >500 A/cm$^2$, with no degradation as a function of duty cycle (from 0.001% to 1%) in pulse measurements, as shown in Fig. 14. An ON-resistance of 6 and 10 m$\Omega \cdot$cm$^2$ was obtained for GaN-on-Si vertical Schottky and p-n diodes, respectively. The relatively high ON-resistance of our GaN-on-Si vertical diodes is due to the relatively high contact resistance of ohmic on p-GaN, low mobility of p-GaN ($\sim$14 cm$^2$/V$\cdot$s), and the current crowding near the corner of etching sidewall. An improvement of the p-GaN material quality is expected to further reduce the ON-resistance of our GaN-on-Si vertical diodes.

The BV capability of our GaN-on-Si vertical diodes has been benchmarked in detail in [6]. With a total drift layer of only 1.5-$\mu$m thick, our GaN-on-Si vertical diodes achieved a soft BV of 300 V, which is close to the theoretical limit for the GaN p-n diodes. This indicates the great potential of the GaN vertical devices to achieve a higher BV with thicker GaN epilayers.

The leakage characteristics are benchmarked in Table I. As shown, with over 1000$\times$ lower substrate cost than the GaN-on-GaN device, our GaN-on-Si vertical devices achieved an OFF-state leakage current lower than the GaN lateral devices and similar to the one in the state-of-the-art Si and SiC devices. The low-leakage and high-BV performances of

our GaN-on-Si vertical diodes have demonstrated the great potential of the GaN-on-Si vertical device as a new low-cost candidate for high-performance power electronics.

## VI. Conclusion

In this paper, we conducted a systematic study on the origin of reverse leakage in the GaN-on-Si vertical diodes. Various leakage sources were separated and clarified, including bulk drift region, passivation layer, etch sidewall, and transition layers. By developing an advanced edge termination technology which combines plasma treatment, TMAH wet etching and ion implantation, we greatly reduced the leakage along etch sidewalls and achieved a BV >300 V, an $E_{\text{peak}}$ of 2.9 MV/cm, and an OFF-state leakage current in the GaN-on-Si vertical diodes similar to the one in Si and SiC devices. The bulk component of the leakage can be explained by a combination of electron tunneling at the p-GaN/ drift-layer interface and carrier hopping between dislocation traps. The high-BV and low-leakage capabilities have demonstrated the suitability of the GaN-on-Si vertical device for high-performance power electronics.

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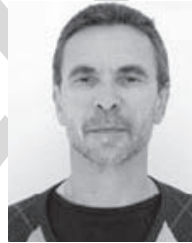
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